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H8SX Family

DTC Transfer with Transfer Information Read Skipping Processing

Introduction

The data transfer controller (DTC) is activated by an IRQ0 interrupt and transfers 64 bytes of data twice. In the second data transfer, the DTC skips reading of the transfer information.

Target Device

H8SX/1653

Contents

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2. Conditions for Application 3
3. Description of Modules Used 4
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5. Description of Software 8

1. Specifications

- Figure 1 shows a block diagram of data transfer by the DTC for this sample task.
- The DTC is activated by an IRQ0 interrupt and transfers two 64-byte data blocks.
- With read skipping processing specified, the DTC skips reading the vector address and transfer information when it transfers the second block of data.

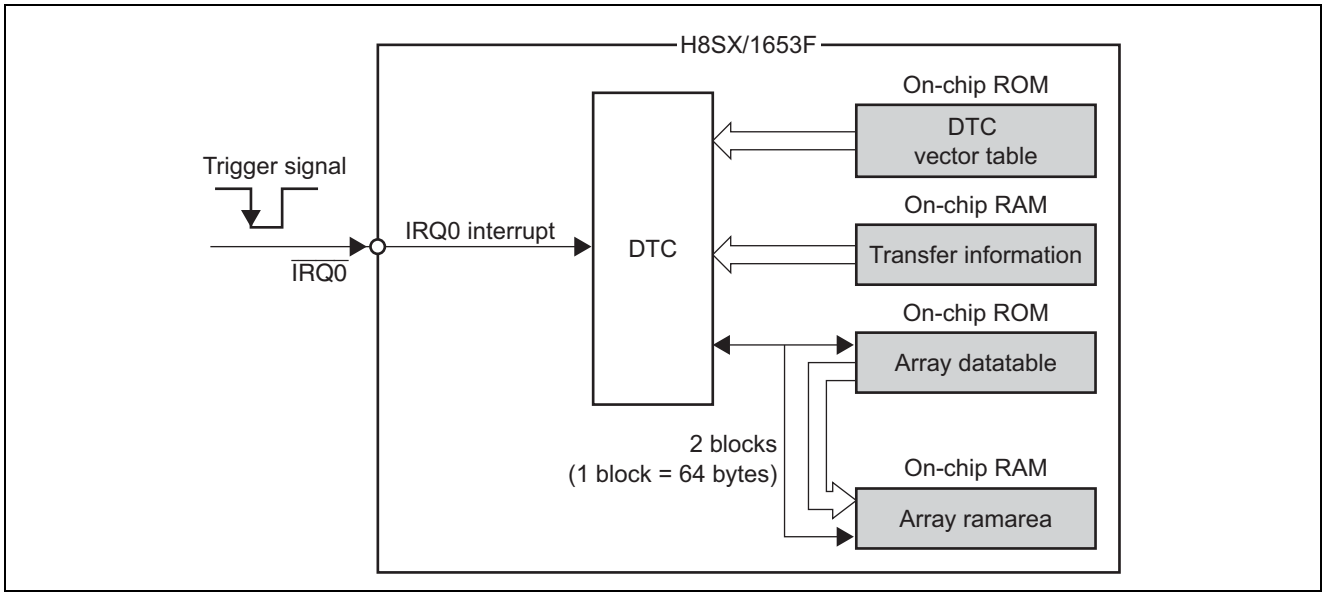


Figure 1 Block Data Transfer by the DTC with Transfer Information Read Skipping Processing

2. Conditions for Application

Table 1 Conditions for Application

Item	Contents
Operating frequency	Input clock: 12 MHz System clock (Iϕ): 48 MHz Peripheral module clock (Pϕ): 24 MHz External bus clock (Bϕ): 48 MHz
Operating mode	Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0)
Development tool	High-performance Embedded Workshop Version 4.00.03
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler Version 6.01.01 (from Renesas Technology Corp.)
Compile option	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3 -speed = (register, shift, struct, expression)

Table 2 Section Settings

Address	Section Name	Description
H'001000	P	Program area
	C	Data table storage area
H'002500	CDTCV	DTC vector address storage area
H'FF2000	B	Uninitialized data area (RAM area)

3. Description of Modules Used

Figure 2 shows a block diagram of the DTC. The block diagram of the DTC is described below.

The registers shown below cannot be directly accessed by the CPU. The values to be set in the registers should be stored in the data area as the transfer information. When a DTC activation source event occurs, the DTC reads the start address of the transfer information according to the vector address assigned to each activation source, copies the transfer information to the registers in the DTC, and transfers data. After transferring the data, the DTC writes the contents of these registers back to the data area.

- DTC mode register A (MRA)
  Selects the DTC operating mode. In this sample task, the transfer mode is set to the block transfer mode, the transfer data size is set to the byte units, and SAR is specified to be incremented after data transfer.
- DTC mode register B (MRB)
  Selects the DTC operating mode. In this sample task, the destination side is selected as the block area and DAR is specified to be incremented after data transfer.
- DTC source address register (SAR)
  Specifies the source address of data transfer.
- DTC destination address register (DAR)
  Specifies the destination address of data transfer.
- DTC transfer count register A (CRA)
  Specifies the number of times data is to be transferred by the DTC. In block transfer mode, CRA is divided into two parts: the upper eight bits (CRAH) and the lower eight bits (CRAL). CRAH holds the block size while CRAL functions as an 8-bit block-size counter (1 to 256 bytes, words, or longwords). In this sample task, the block size is set to 64 bytes.
- DTC transfer count register B (CRB)
  Specifies the number of times block data is to be transferred by the DTC in block transfer mode.

The registers shown below are in the interrupt controller or bus controller and can be directly accessed by the CPU.

- DTC enable registers A to E, G, and H (DTCERA to DTCERE, DTCERG, and DTCERH)
  The DTCER registers (DTCERA to DTCERE, DTCERG, and DTCERH) select the DTC activation interrupt sources. Refer to the hardware manual for the correspondence between the interrupt sources and DTCE bits. In this sample task, the IRQ0 interrupt is selected as the activation source.
- DTC control register (DTCCR)
  Specifies skipping of transfer information reading, etc.
- DTC vector base register (DTCVBR)
  Specifies the base address to be used to calculate the vector table address.

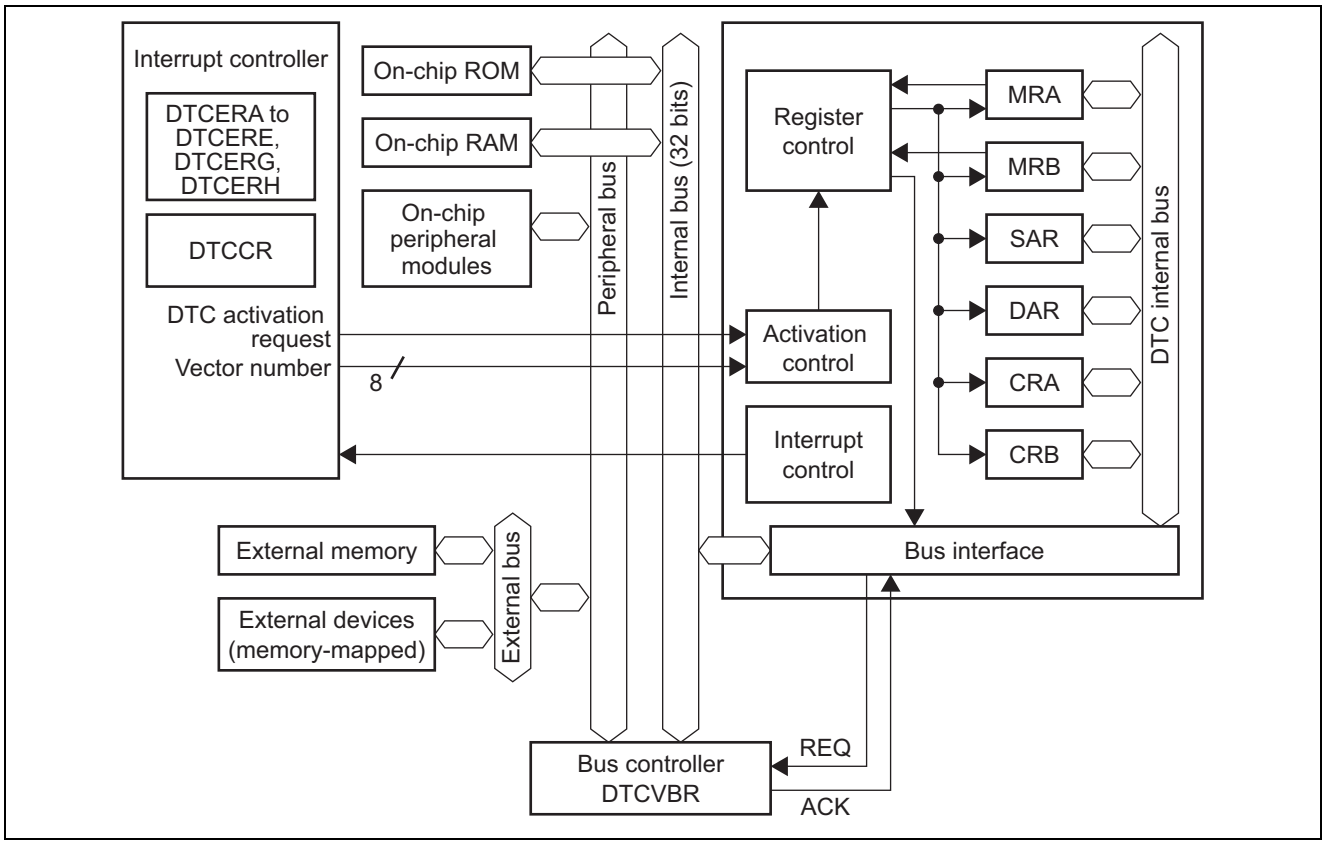


Figure 2 Block Diagram of DTC

4. Description of Operation

4.1 Overview

4.1.1 DTC Data Transfer

Figures 3 and 4 show the memory mapping for data transfer by the DTC.

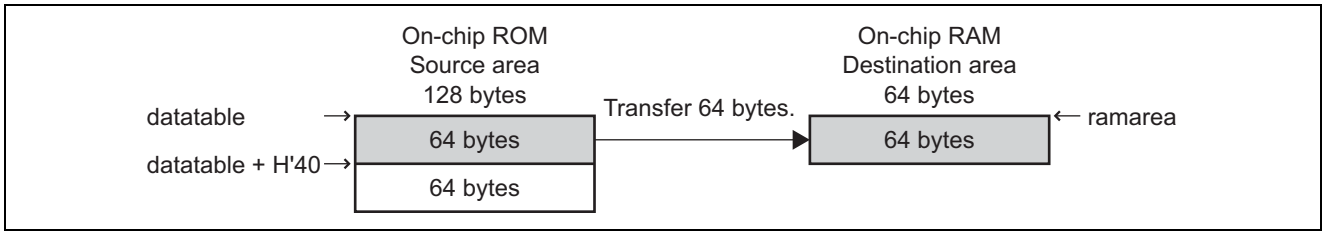


Figure 3 First Transfer

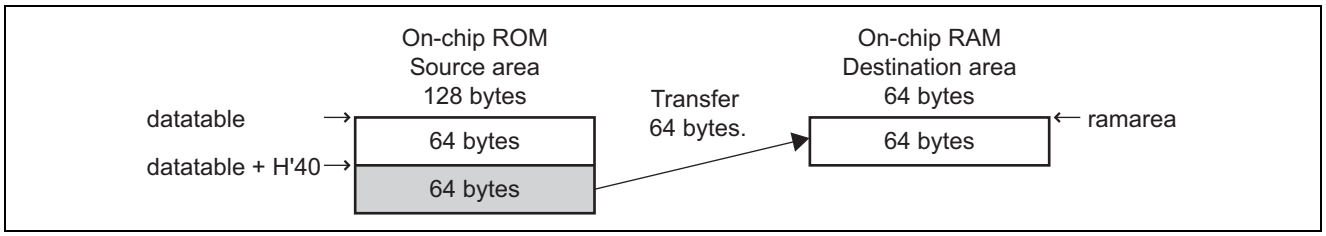
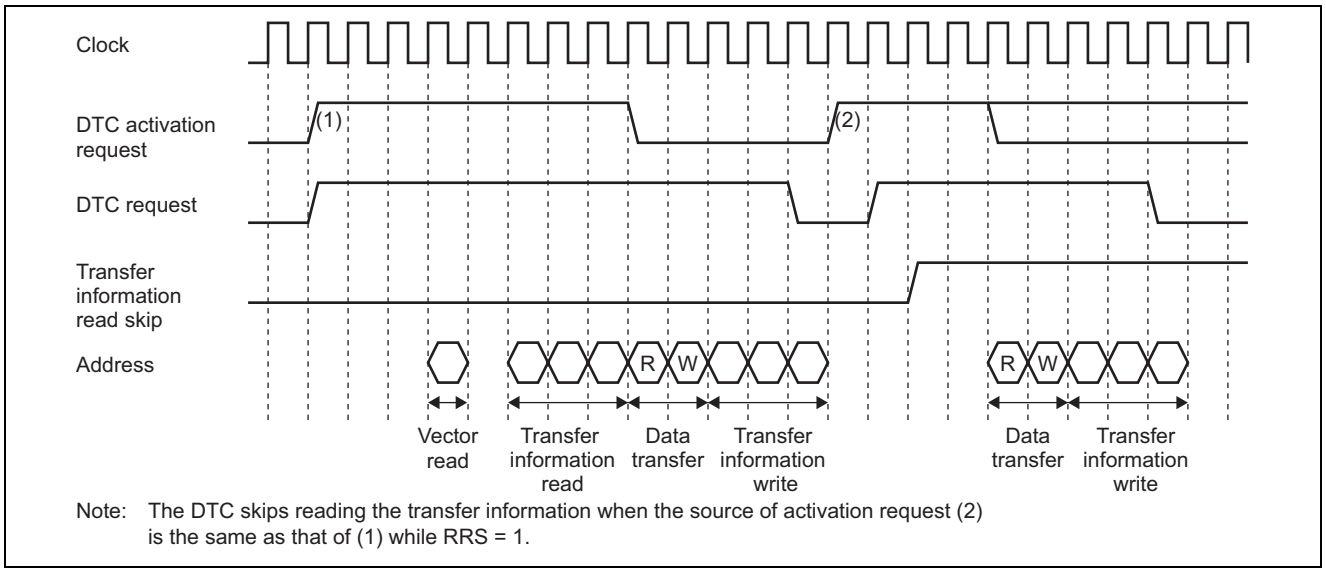


Figure 4 Second Transfer

4.1.2 Transfer Information Read Skip Timing

- Figure 5 shows the timing of the transfer information read skip processing.
- When the DTC is activated for the first transfer, the DTC reads the vector and then reads the transfer information after the DTC activation request (1).
- When RRS = 1, the DTC skips reading the vector and transfer information for the second DTC activation request (2).



Note: The DTC skips reading the transfer information when the source of activation request (2) is the same as that of (1) while RRS = 1.

Figure 5 Timing

4.2 DTC Transfer Information

4.2.1 Configuration of Transfer Information

Figure 6 shows the configuration of the transfer information in memory in short address mode. In this sample task, the transfer information is allocated at H'FFB000.

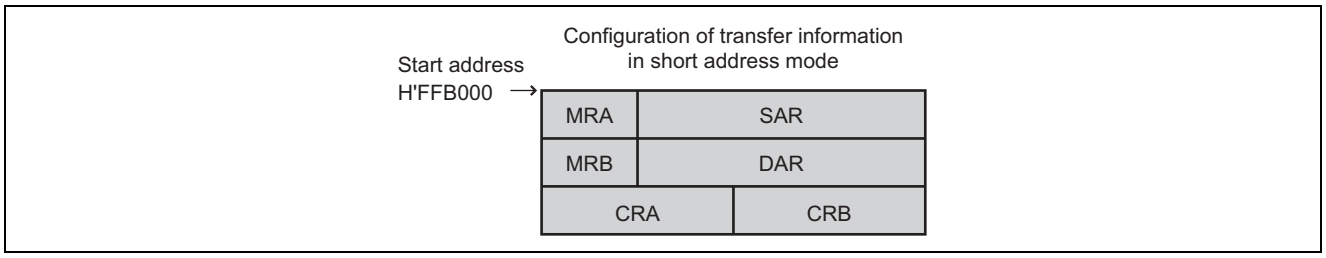


Figure 6 Configuration of Transfer Information

4.2.2 Correspondence between Vector Table and Transfer Information

Figure 7 shows the correspondence between the vector table and transfer information. In this sample task, the vector table address is calculated as H'00002500 based on the DTCVBR contents. The start address (H'FFB000) of transfer information is set in this vector table, which causes the transfer information to be read into the registers in the DTC.

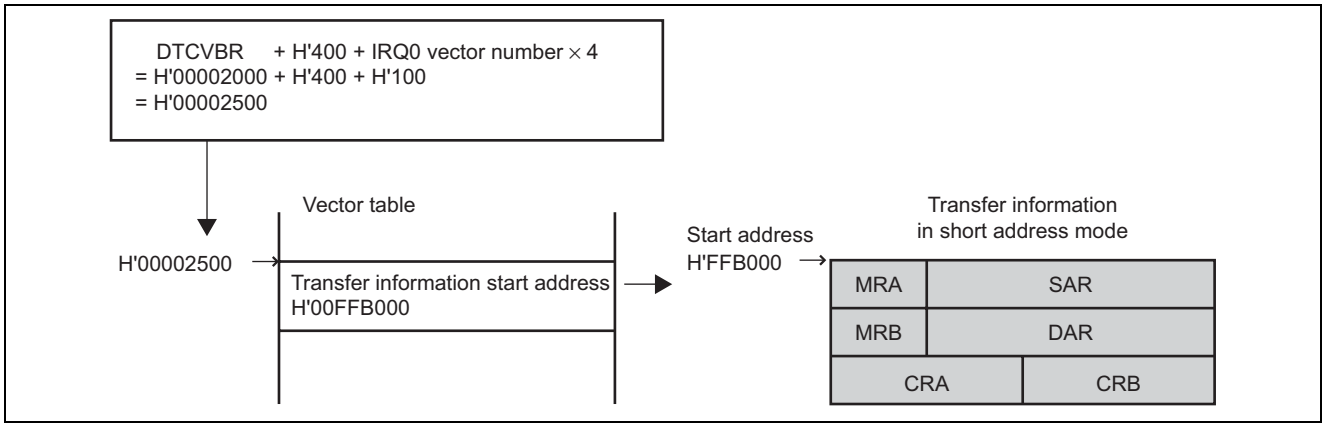


Figure 7 Correspondence between Vector Table and Transfer Information

5. Description of Software

5.1 List of Functions

Table 3 List of Functions

Function Name	Functions
init	Initialization routine Sets the CCR and configures the clocks, cancels the module stop mode, and calls the main function.
main	Main routine Makes the initial settings for the DTC, specifies skipping of transfer information read, and transfers two 64-byte data blocks.
irq0_int	IRQ0 interrupt handling routine

5.2 Vector Table

Table 4 Interrupt and Exception Handling Vector Table

Exception Handling Source	Vector Number	Vector Table Address	Exception Handling Routine
Reset	0	H'000000	main
IRQ0	64	H'000100	irq0_int

5.3 RAM Usage

Table 5 RAM Usage

Type	Variable Name	Description	Used In
unsigned char	ramarea[64]	Destination RAM area	main
DTC_tag	TRINFO	DTC transfer information (Start address: H'FFB000)	main

5.4 Data Table

Table 6 Data Table

Type	Array Name	Description	Used In
unsigned char	datatable[128]	Stores the source data. 128 bytes of data of H'00, H'01, ..., H'7F	main

5.5 Description of Functions

5.5.1 init Function

(1) Functional overview

Initialization routine which cancels the module stop mode, sets up the clocks, and calls the main function.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- System clock control register (SCKCR) Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Function
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock, which is
8	ICK0	0	R/W	supplied to the CPU, DMAC, and DTC. 000: Input clock × 4
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module
4	PCK0	1	R/W	clock. 001: Input clock × 2
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	0	R/W	000: Input clock × 4

- MSTPCRA, MSTPCRB, and MSTPCRC control module stop mode. Setting a bit in these registers to 1 places the corresponding module in module stop mode, while clearing the bit to 0 cancels module stop mode.

- Module stop control register A (MSTPCRA) Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Function
15	ACSE	0	R/W	All-module-clock-stop mode enable Enables or disables transition to all-module-clock-stop mode. If this bit is set to 1, all-module-clock-stop mode is entered when the SLEEP instruction is executed by the CPU while all the modules under control of the MSTPCR registers are placed in module stop mode. In all-module-clock-stop mode, even the bus controller and I/O ports are stopped to reduce the supply current. 0: Disables transition to all-module-clock-stop mode. 1: Enables transition to all-module-clock-stop mode.
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	0	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timer (TMR_3, TMR_2)
8	MSTPA8	1	R/W	8-bit timer (TMR_1, TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
0	MSTPA0	1	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

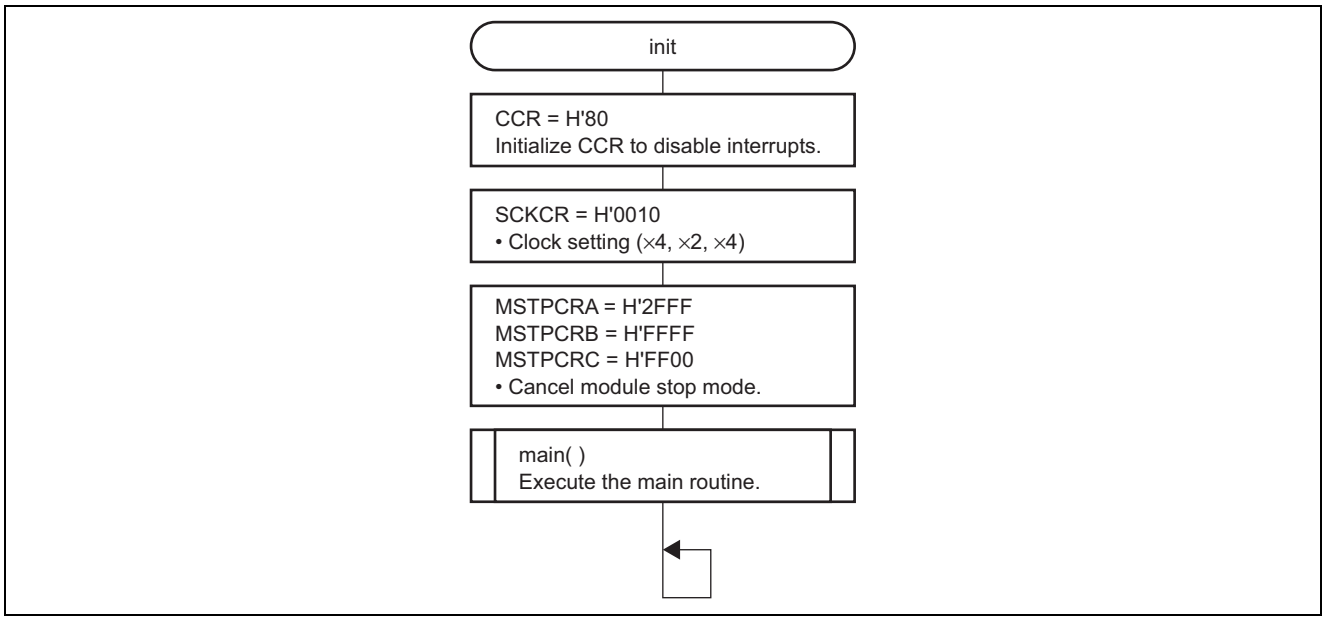
- Module stop control register B (MSTPCRB) Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Function
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communication interface_4 (SCI_4)
10	MSTPB10	1	R/W	Serial communication interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communication interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial communication interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus interface_1 (IIC_1)
6	MSTPB6	1	R/W	I^2C bus interface_0 (IIC_0)

- Module stop control register C (MSTPCRC) Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Function
15	MSTPC15	1	R/W	Serial communication interface_5 (SCI_5), (IrDA)
14	MSTPC14	1	R/W	Serial communication interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timer (TMR_4, TMR_5)
12	MSTPC12	1	R/W	8-bit timer (TMR_6, TMR_7)
11	MSTPC11	1	R/W	Universal serial bus interface (USB)
10	MSTPC10	1	R/W	Cyclic redundancy check
4	MSTPC4	0	R/W	On-chip RAM_4 (H'FF2000 to H'FF3FFF)
3	MSTPC3	0	R/W	On-chip RAM_3 (H'FF4000 to H'FF5FFF)
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF8000 to H'FF9FFF)
0	MSTPC0	0	R/W	On-chip RAM_0 (H'FFA000 to H'FFBFFF)

(5) Flowchart



5.5.2 main Function

(1) Functional overview

Makes settings for DTC transfer and starts transfer.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- DTC mode register A (MRA) (Cannot be directly accessed by the CPU.)

Bit	Bit Name	Setting	Function
7	MD1	1	DTC Mode 1, 0
6	MD0	0	10: Block transfer mode
5	Sz1	0	DTC Data Transfer Size 1, 0
4	Sz0	0	00: Byte-size transfer
3	SM1	1	Source Address Mode 1, 0
2	SM0	0	These bits specify the SAR operation after a data transfer. 10: Increments SAR after a transfer

- DTC mode register B (MRB) (Cannot be directly accessed by the CPU.)

Bit	Bit Name	Setting	Function
4	DTS	0	DTC Transfer Mode Select 0: Specifies the destination as the repeat or block area 1: Specifies the source as the repeat or block area
3	DM1	1	Destination Address Mode 1, 0
2	DM0	0	These bits specify the DAR operation after a data transfer. 10: Increments DAR after a transfer

- DTC source address register (SAR) (Cannot be directly accessed by the CPU.)
  Function: Specifies the source address of data transfer.
  Setting: Start address of array datatable
- DTC destination address register (DAR) (Cannot be directly accessed by the CPU.)
  Function: Specifies the destination address of data transfer.
  Setting: Start address of array ramarea
- DTC transfer count register A (CRA) (Cannot be directly accessed by the CPU.)
  Function: Specifies the block size in block transfer mode. When the Sz1 and Sz0 bits in MRA are set to B'00 (byte-size transfer) and CRA is set to H'4040, the block size is 64 bytes.
  Setting: H'4040

- DTC transfer count register B (CRB) (Cannot be directly accessed by the CPU.)
  Function: Specifies the number of times data is to be transferred in block transfer mode. This value is decremented (-1) after each data transfer.
  Setting: H'0002

- Port 5 input buffer control register (P5ICR) Address: H'FFFB94

Bit	Bit Name	Setting	R/W	Function
0	P50ICR	1	R/W	0: Disables the input buffer of the P50 pin 1: Enables the input buffer of the P50 pin

- Port function control register C (PFCRC) Address: H'FFFBCC

Bit	Bit Name	Setting	R/W	Function
0	ITS0	1	R/W	$\overline{\text{IRQ0}}$ Pin Select 0: Selects the P10 pin as the $\overline{\text{IRQ0}}$-A input 1: Selects the P50 pin as the $\overline{\text{IRQ0}}$-B input

- IRQ sense control register L (ISCRL) Address: H'FFFD6A

Bit	Bit Name	Setting	R/W	Function
1	IRQ0SR	0	R/W	IRQ0 Sense Control Rise
0	IRQ0SF	1	R/W	IRQ0 Sense Control Fall 01: Generates an interrupt request at the falling edge of the $\overline{\text{IRQ0}}$ input

- DTC vector base register (DTCVBR) Address: H'FFFD80
  Function: 32-bit register that specifies the base address used to calculate the vector table address.
  Setting: H'00002000

- DTC enable register A (DTCERA) Address: H'FFFF20

Bit	Bit Name	Setting	R/W	Function
15	DTCEA15	1	R/W	0: Does not select the IRQ0 interrupt as the DTC activation source. 1: Selects the IRQ0 interrupt as the DTC activation source.

- DTC control register (DTCCR) Address: H'FFFF30

Bit	Bit Name	Setting	R/W	Function
4	RRS	1	R/W	DTC Transfer Information Read Skip Enable 0: Disables skipping of transfer information read. 1: Skips reading transfer information when the vector numbers match.
0	ERR	0	R/(W)*	Transfer Stop Flag 0: Neither address error nor NMI interrupt request has occurred 1: An address error or an NMI interrupt request has occurred

Note: * Only 0 can be written to clear the flag.

- IRQ enable register (IER) Address: H'FFFF34

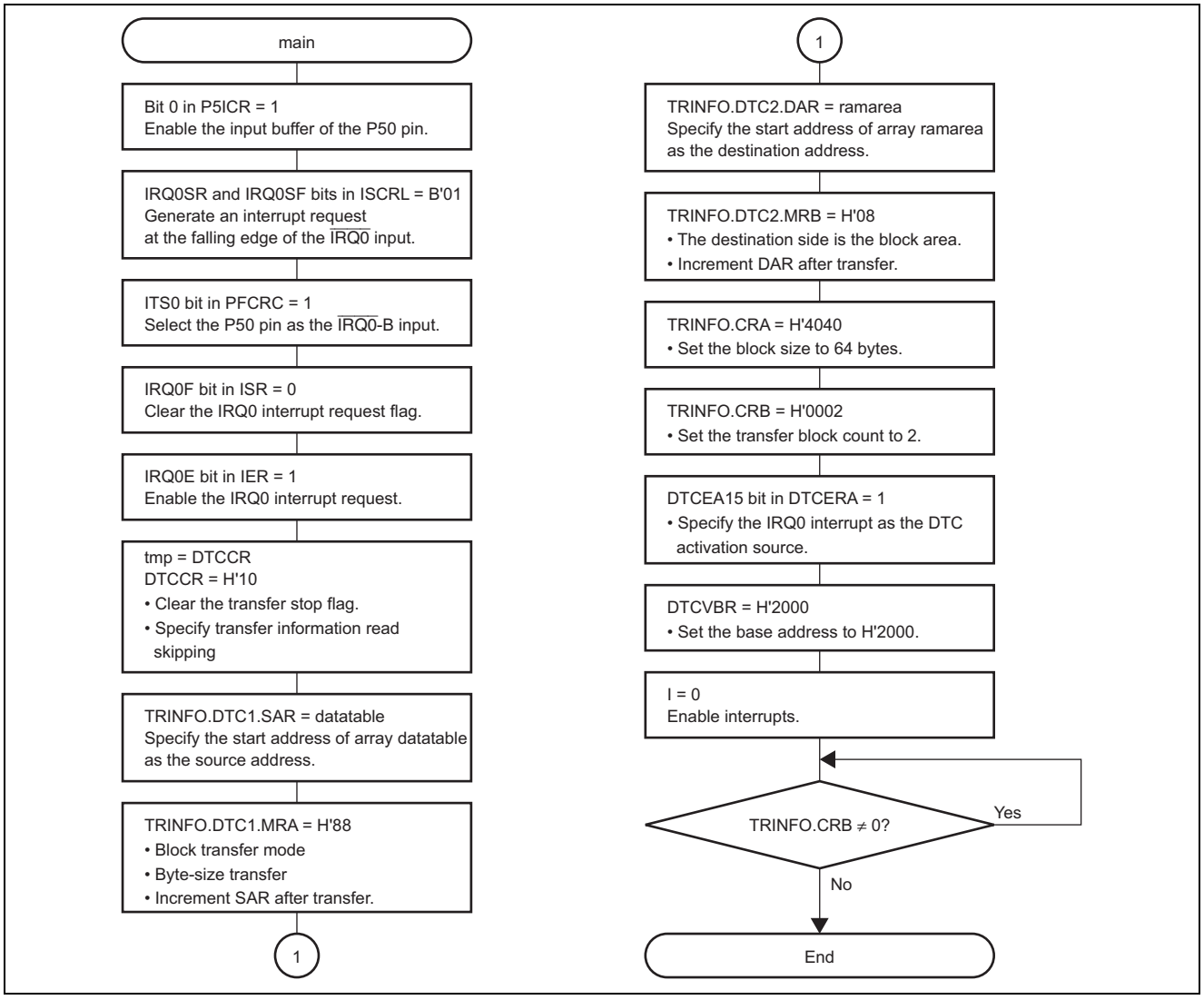
Bit	Bit Name	Setting	R/W	Function
0	IRQ0E	1	R/W	IRQ0 Enable 0: Disables the IRQ0 interrupt request 1: Enables the IRQ0 interrupt request

- IRQ status register (ISR) Address: H'FFFF36

Bit	Bit Name	Setting	R/W	Function
0	IRQ0F	0	R/(W)*	IRQ0 Status 0: IRQ0 interrupt has not occurred 1: IRQ0 interrupt has occurred

Note: * Only 0 can be written to clear the flag.

(5) Flowchart



5.5.3 irq0_int Function

(1) Functional overview

IRQ0 interrupt handling routine

(2) Argument

None

(3) Return value

None

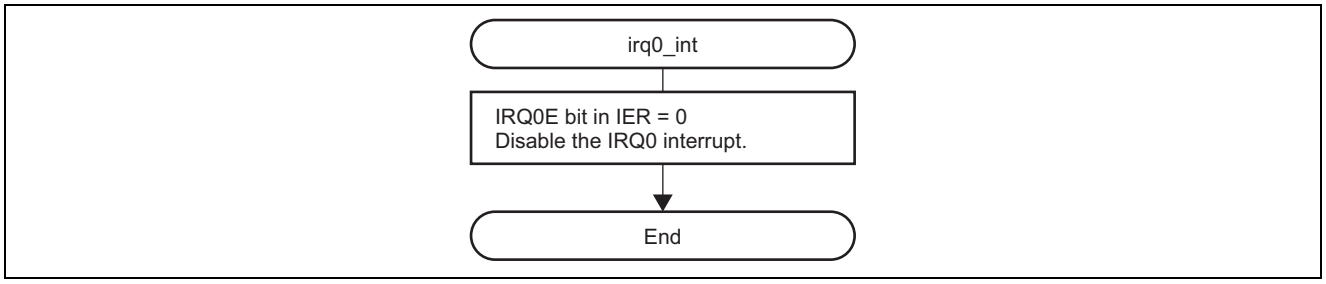
(4) Description of internal registers

The internal registers used in this sample task are described below. Note that the settings shown below are not initial values but the values used in this sample task.

- IRQ enable register (IER) Address: H'FFFF34

Bit	Bit Name	Setting	R/W	Function
0	IRQ0E	0	R/W	IRQ0 Enable 0: Disables the IRQ0 interrupt request 1: Enables the IRQ0 interrupt request

(5) Flowchart



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