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H8SX Family

DTC Data Transfer Initiated by IRQ Interrupt

Introduction

The DTC is activated by an IRQ interrupt and it performs data transfer of 128 bytes.

Target Device

H8SX/1582F

Contents

1. Specifications

- Figure 1 shows a block diagram of data transfer by the DTC.
- The DTC is activated by an IRQ0 interrupt and transfers data blocks, each of which is 128 bytes.
- Data blocks are transferred from on-chip ROM (array datatable) to on-chip RAM (array ramarea) by means of the DTC.

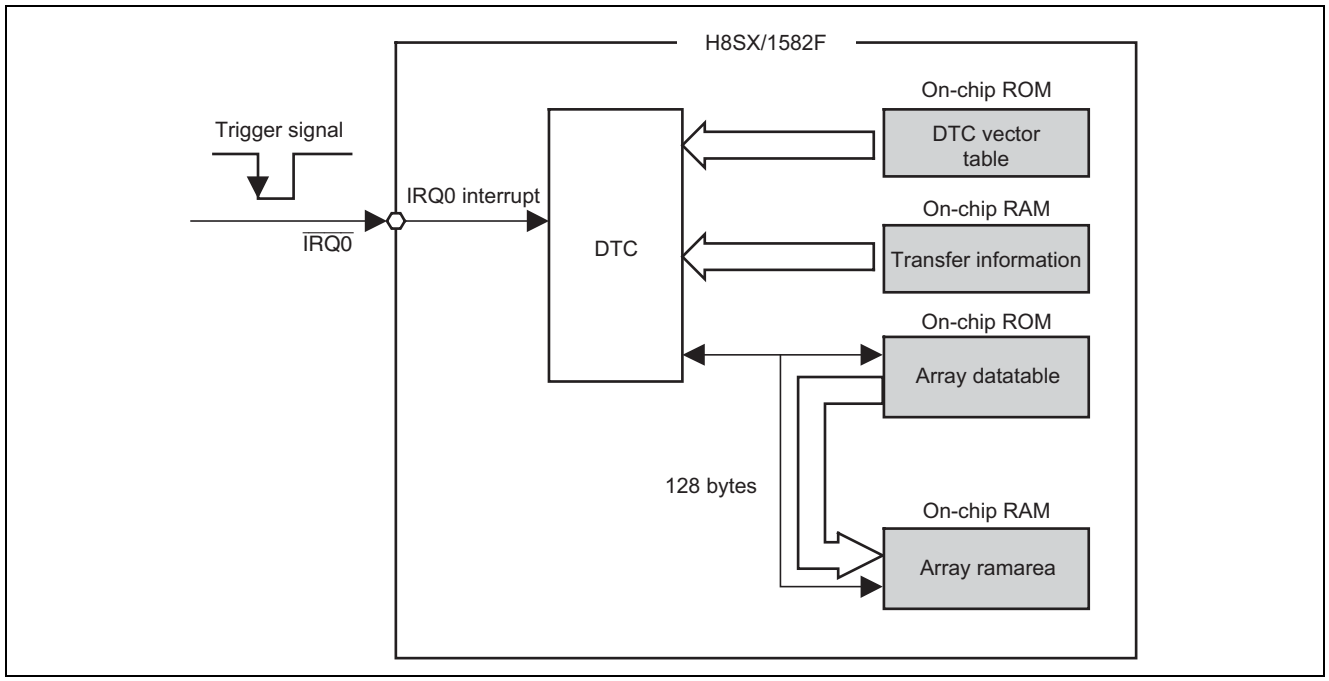


Figure 1 Block Diagram of DTC Data Transfer

2. Conditions for Application

Table 1 Conditions for Application

Item	Contents	
Operating frequency	Input clock:	5 MHz
	System clock (Iϕ):	40 MHz
	Peripheral module clock (Pϕ):	20 MHz
	External bus clock (Bϕ):	20 MHz
Operating mode	Mode 3 (MD1 = 1, MD0 = 1)	
Development tool	High-performance Embedded Workshop Version 4.00.02	
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler Version 6.01.00 (from Renesas Technology Corp.)	
Compile option	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3, -speed = (register, shift, struct, expression)	

Table 2 Section Settings

Address	Section Name	Description
H'001000	P	Program area
	C	Data table storage area
H'002500	CDTCV	DTC vector address storage area
H'FF9000	B	Uninitialized data area (RAM area)

3. Description of Modules Used

Figure 2 shows a block diagram of the DTC. The block diagram of the DTC is described below.

The registers shown below cannot be directly accessed by the CPU. These registers are located in the data area as the transfer information. When a DTC activation source event occurs, the start address of the transfer information is read in accordance with the vector address assigned to each activation source; the transfer information is transferred to the DTC and data transfer is performed. When transfer has finished, the contents of these registers are written back.

- DTC mode register A (MRA)
  Selects the operating mode of the DTC. In this sample task, the transfer mode is set as block transfer mode, the transfer data size as byte-wise, and SAR is set to be incremented after data transfer.
- DTC mode register B (MRB)
  Selects the operating mode of the DTC. In this sample task, the destination side is set as the block area and DAR is set to be incremented after data transfer.
- DTC source address register (SAR)
  Specifies the transfer source address.
- DTC destination address register (DAR)
  Specifies the transfer destination address.
- DTC transfer count register A (CRA)
  Specifies the number of data transfers by the DTC. In block transfer mode, this register is divided into the upper eight bits CRAH and the lower eight bits CRAL. CRAH specifies the number of transfers and CRAL is used as an 8-bit transfer counter.
- DTC transfer count register B (CRB)
  In block transfer mode, specifies the number of block data transfers by the DTC.

The following registers are located in the interrupt controller and bus controller, and can be directly accessed by the CPU.

- DTC enable registers A to H (DTCERA to DTCERH)
  The DTCER registers are used to select the interrupt sources for activation of the DTC. See the hardware manual for the correspondence between the interrupt sources and the DTCE bits in the DTCER registers. In the sample task, the DTCEA15 bit in DTCERA is set to 1 to select the IRQ0 interrupt request as the activation source.
- DTC control register (DTCCR)
  Sets the DTC to be activated by an IRQ0 interrupt.
- DTC vector base register (DTCVBR)
  Sets the base address used to calculate the vector table address.

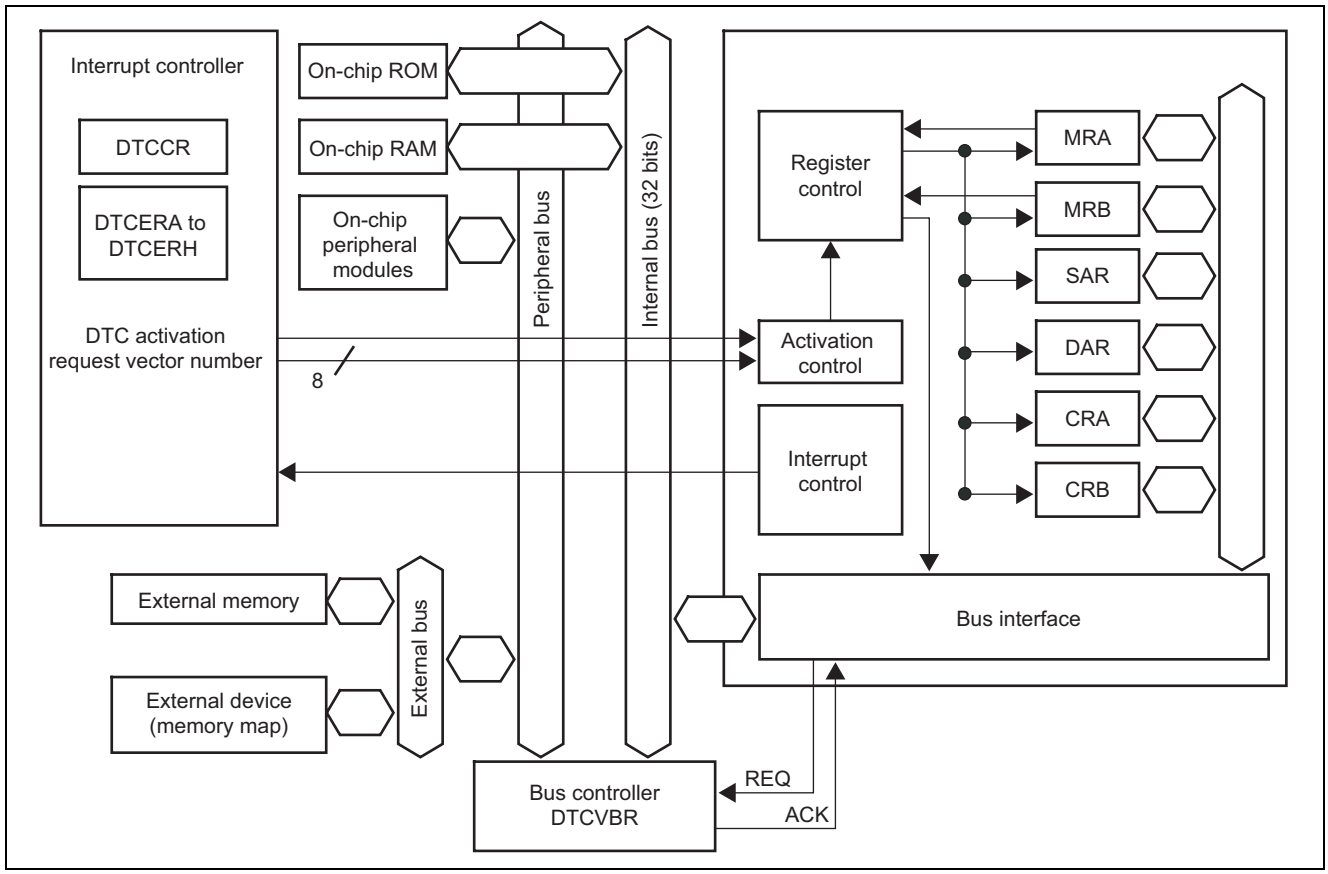


Figure 2 Block Diagram of DTC

4. Description of Operation

4.1 Overview

Figure 3 summarizes the operation when using DTC block transfer. The hardware processing and software processing are shown in table 3 for describing figure 3.

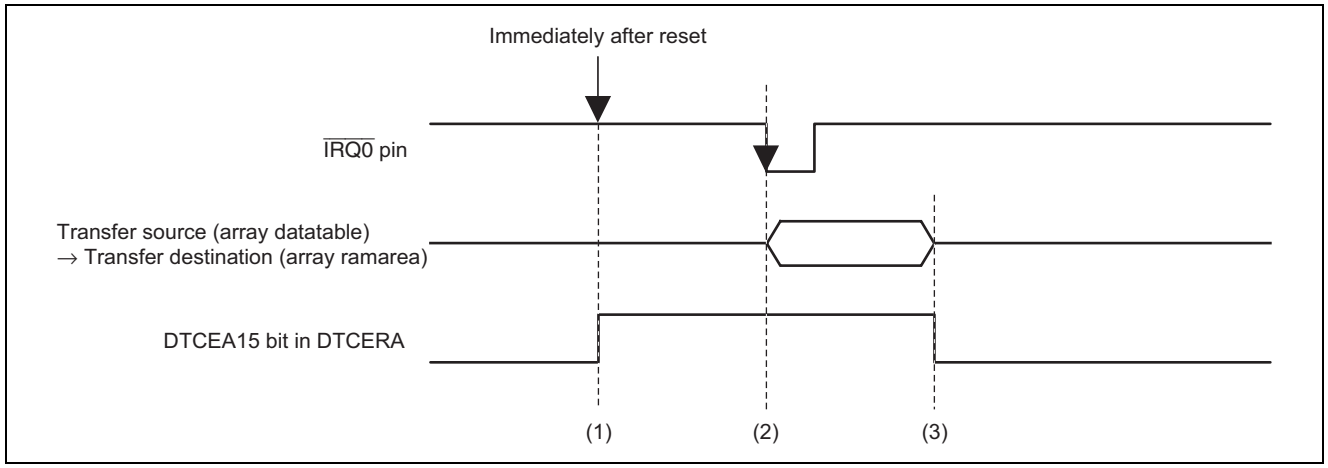


Figure 3 Data Transfer Operation Initiated by IRQ0 Interrupt

Table 3 Hardware and Software Processing

	Hardware Processing	Software Processing
(1)	None	DTC initial settings • Transfer source address: First address of array datatable • Transfer destination address: First address of array ramarea • Increment SAR and DAR after transfer. • Destination side is the block area. • Block transfer mode • Set the block size in CRA and the block transfer count in CRB. • Select the IRQ0 interrupt request as the DTC activation source. (Set DTCEA15 in DTCERA to 1.)
(2)	Activation of the DTC (a) Generate an IRQ0 interrupt request on the rising edge of the $\overline{\text{IRQ0}}$ pin. (b) Activate the DTC, which has been configured to be activated by the IRQ0 interrupt request. (c) Transfer 128 bytes of data from array datatable to array ramarea.	None
(3)	(a) Clear DTCEA15 in DTCERA to 0.	IRQ0 interrupt handling (a) Disable the IRQ0 interrupt.

4.2 DTC Transfer Information

Operation related to the DTC transfer information is summarized below.

- Configuration of transfer information
  In short address mode, transfer information should be placed in memory as shown in figure 4. In this sample task, the start address of the transfer information is set at H'FFB000.

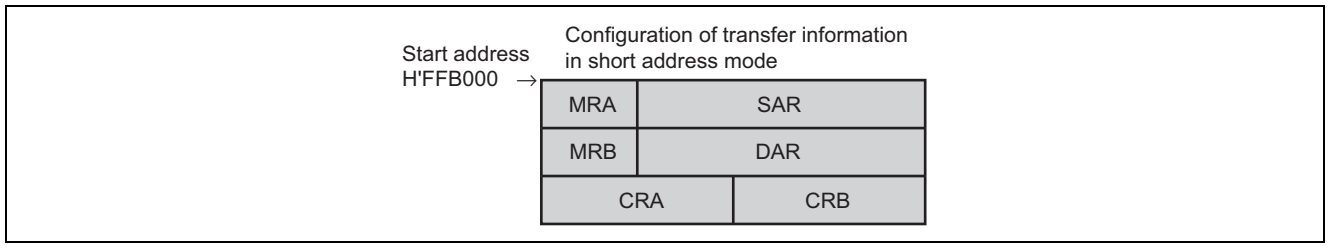


Figure 4 Configuration of Transfer Information in Short Address Mode

- Correspondence between vector table and transfer information
  Correspondence between the vector table and transfer information is shown in figure 5. In this sample task, the vector table address is set at H'00002500 based on the DTCVBR contents. If the transfer information start address (H'FFB000) is set in this vector table, the transfer information is read into the DTC registers.

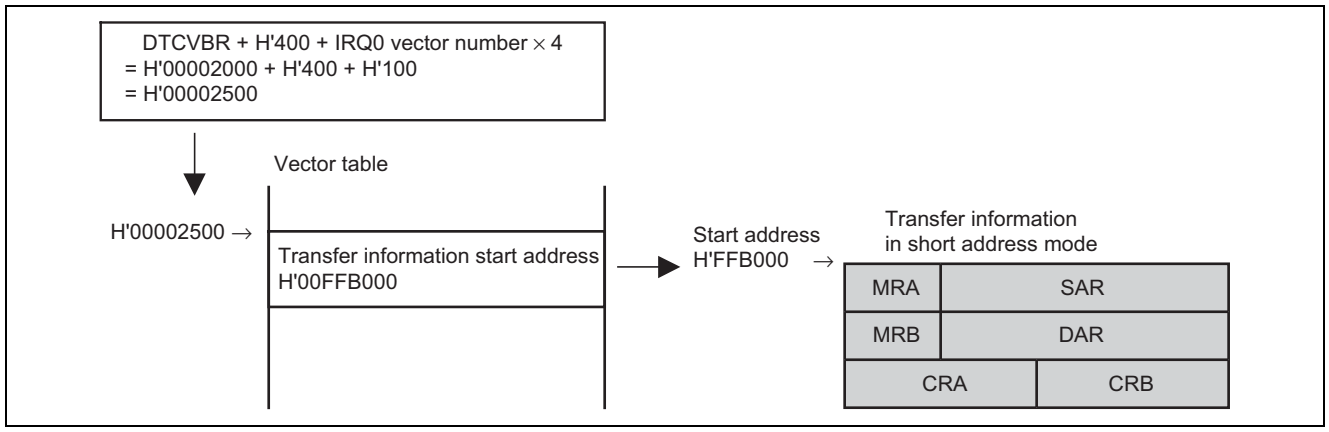


Figure 5 Correspondence between Vector Table and Transfer Information

5. Description of Software

5.1 List of Functions

Table 4 List of Functions

Function Name	Functions
init	Initialization routine Cancels module stop mode, sets the clock, and calls the main function.
main	Main routine Makes the initial settings for the DTC, and performs processing for the transfer of 128 bytes of data.
irq0_int	IRQ0 interrupt handling routine

5.2 RAM Usage

Table 5 RAM Usage

Type	Variable Name	Description	Used In
unsigned char	ramarea[128]	Destination RAM area	main
DTC_tag	TRINFO	DTC transfer information (Start address: H'FFB000)	main

5.3 Data Table

Table 6 Data Table

Type	Array Name	Description	Used In
unsigned char	datatable[128]	Stores the source data 128-byte data of H'00, H'01, ... H'7F	main

5.4 Description of Functions

5.4.1 init Function

(1) Functional overview

Initialization routine which cancels module stop mode, sets the clock, and calls the main function.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. The setting values shown in these tables are the values used in this sample task and differ from their initial values.

- System clock control register (SCKCR) Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Function
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0		These bits select the system clock frequency. The CPU, DMAC, and DTC modules are driven by the system clock.
8	ICK0	0		000: Input clock × 8
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0		These bits select the frequency of the peripheral module clock.
4	PCK0	1		001: Input clock × 4
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0		These bits select the frequency of the external bus clock.
0	BCK0	1		001: Input clock × 4

- MSTPCRA, MSTPCRB, and MSTPCRC are the registers that control module stop mode. Setting the bits in these registers places the corresponding modules in module stop mode, and clearing the bits cancels module stop mode.

- Module stop control register A (MSTPCRA) Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Function
15	ACSE	0	R/W	All-module-clock-stop mode enable Enables or disables transition to all-module-clock-stop mode. If this bit is set to 1, all-module-clock-stop mode is entered when the SLEEP instruction is executed by the CPU while all the modules under control of the MSTPCR registers are placed in module stop mode. In all-module-clock-stop mode, even the bus controller and I/O ports are stopped to reduce the supply current. 0: Disables transition to all-module-clock-stop mode. 1: Enables transition to all-module-clock-stop mode.
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	0	R/W	Data transfer controller (DTC)
4	MSTPA4	1	R/W	A/D converter (unit 1)
3	MSTPA3	1	R/W	A/D converter (unit 0)
1	MSTPA1	1	R/W	16-bit timer pulse unit (TPU channels 11 to 6)
0	MSTPA0	1	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

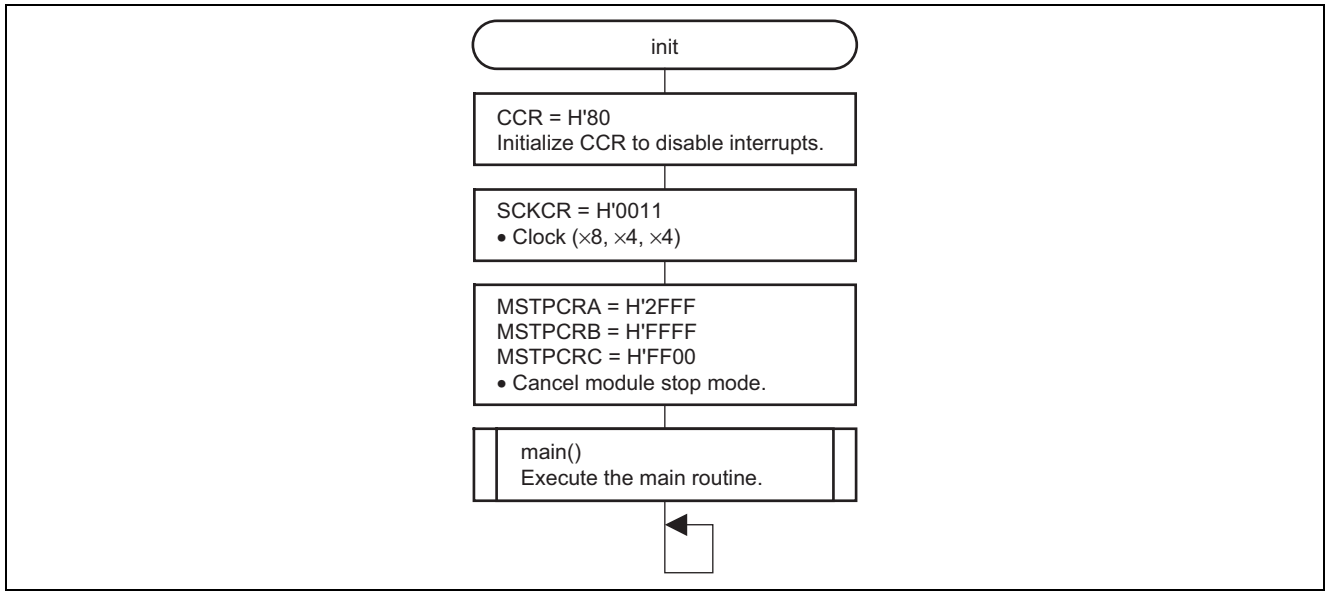
- Module stop control register B (MSTPCRB) Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Function
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communication interface_4 (SCI_4)
11	MSTPB11	1	R/W	Serial communication interface_3 (SCI_3)

- Module stop control register C (MSTPCRC) Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Function
10	MSTPC10	1	R/W	Synchronous serial communication unit 2 (SSU_2)
9	MSTPC9	1	R/W	Synchronous serial communication unit 1 (SSU_1)
8	MSTPC8	1	R/W	Synchronous serial communication unit 0 (SSU_0)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF9000 to H'FFBFFF)
0	MSTPC0	0	R/W	Always write the same value to the MSTPC1 and MSTPC0 bits.

(5) Flowchart



5.4.2 main Function

(1) Functional overview

Main routine which makes the initial settings for the DTC and performs the data transfer processing of 128 bytes.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. The setting values shown in these tables are the values used in this sample task and differ from their initial values.

- DTC mode register A (MRA) (Cannot be directly accessed by the CPU)

Bit	Bit Name	Setting	Function
7	MD1	1	DTC Mode 1, 0
6	MD0	0	10: Block transfer mode
5	Sz1	0	DTC Data Transfer Size 1, 0
4	Sz0	0	00: Byte-wise transfer
3	SM1	1	Source Address Mode 1, 0
2	SM0	0	These bits specify the operation of SAR after data transfer. 10: SAR is incremented after data transfer

- DTC mode register B (MRB) (Cannot be directly accessed by the CPU)

Bit	Bit Name	Setting	Function
4	DTS	0	DTC Transfer Mode Select 0: Destination side is repeat area or block area 1: Source side is repeat area or block area
3	DM1	1	Destination Address Mode 1, 0
2	DM0	0	These bits specify the operation of DAR after data transfer. 10: DAR is incremented after data transfer

- DTC source address register (SAR) (Cannot be directly accessed by the CPU)
  Function: Sets the transfer source address.
  Setting: Start address of array datatable

- DTC destination address register (DAR) (Cannot be directly accessed by the CPU)
  Function: Sets the transfer destination address.
  Setting: Start address of array ramarea

- DTC transfer count register A (CRA) (Cannot be directly accessed by the CPU)
  Function: Sets the block size in block transfer mode. When CRA = H'8080 with the Sz1 and Sz0 bits in MRA set to B'00 (byte-wise transfer), the block size is 128 bytes.
  Setting: H'8080

- DTC transfer count register B (CRB) (Cannot be directly accessed by the CPU)
  Function: Sets the number of transfers in block transfer mode. The value of this register will be decremented (–1) for each data transfer.
  Setting: H'0001

- DTC vector base register (DTCVBR) Address: H'FFFD80
  Function: 32-bit register which sets the base address used to calculate the vector table address.
  Setting: H'00002000

- DTC enable register A (DTCERA) Address: H'FFFF20

Bit	Bit Name	Setting	R/W	Function
15	DTCEA15	1	R/W	Transfer Stop Flag 0: IRQ0 interrupt is not selected as the DTC activation source 1: IRQ0 interrupt is selected as the DTC activation source

- DTC control register (DTCCR) Address: H'FFFF30

Bit	Bit Name	Setting	R/W	Function
0	ERR	0	R/(W)*	Transfer Stop Flag 0: Address error or NMI interrupt request has not occurred 1: Address error or NMI interrupt request has occurred

Note: * Only 0 can be written to clear the flag.

- Port 1 input buffer control register (P1ICR) Address: H'FFFB90

Bit	Bit Name	Setting	R/W	Function
0	P10ICR	1	R/W	0: Input buffer of pin P10 is disabled 1: Input buffer of pin P10 is enabled

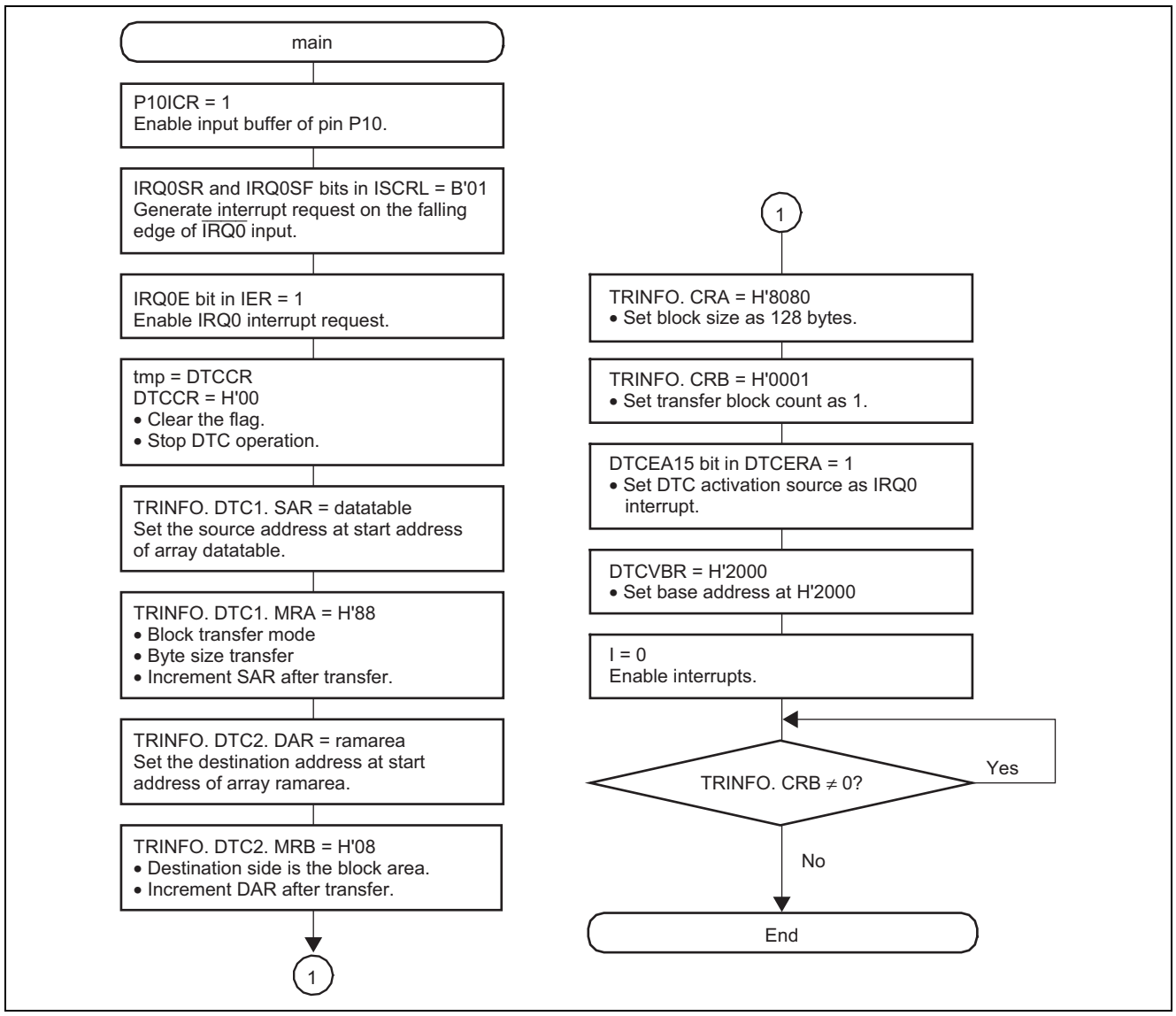
- IRQ sense control register L (ISCRL) Address: H'FFFD6A

Bit	Bit Name	Setting	R/W	Function
1	IRQ0SR	0	R/W	IRQ0 Sense Control Rise
0	IRQ0SF	1	R/W	IRQ0 Sense Control Fall 01: Interrupt request is generated on the falling edge of $\overline{\text{IRQ0}}$ input

- IRQ enable register (IER) Address: H'FFFF34

Bit	Bit Name	Setting	R/W	Function
0	IRQ0E	1	R/W	IRQ0 Enable 0: IRQ0 interrupt request is disabled 1: IRQ0 interrupt request is enabled

(5) Flowchart


main
P10ICR = 1
Enable input buffer of pin P10.
IRQ0SR and IRQ0SF bits in ISCRL = B'01
Generate interrupt request on the falling edge of IRQ0 input.
IRQ0E bit in IER = 1
Enable IRQ0 interrupt request.
tmp = DTCCR
DTCCR = H'00
• Clear the flag.
• Stop DTC operation.
TRINFO. DTC1. SAR = datatable
Set the source address at start address of array datatable.
TRINFO. DTC1. MRA = H'88
• Block transfer mode
• Byte size transfer
• Increment SAR after transfer.
TRINFO. DTC2. DAR = ramarea
Set the destination address at start address of array ramarea.
TRINFO. DTC2. MRB = H'08
• Destination side is the block area.
• Increment DAR after transfer.
1
1
TRINFO. CRA = H'8080
• Set block size as 128 bytes.
TRINFO. CRB = H'0001
• Set transfer block count as 1.
DTCEA15 bit in DTCERA = 1
• Set DTC activation source as IRQ0 interrupt.
DTCVBR = H'2000
• Set base address at H'2000
I = 0
Enable interrupts.
TRINFO. CRB ≠ 0?
Yes
No
End

5.4.3 irq0_int Function

(1) Functional overview

IRQ0 interrupt handling routine

(2) Argument

None

(3) Return value

None

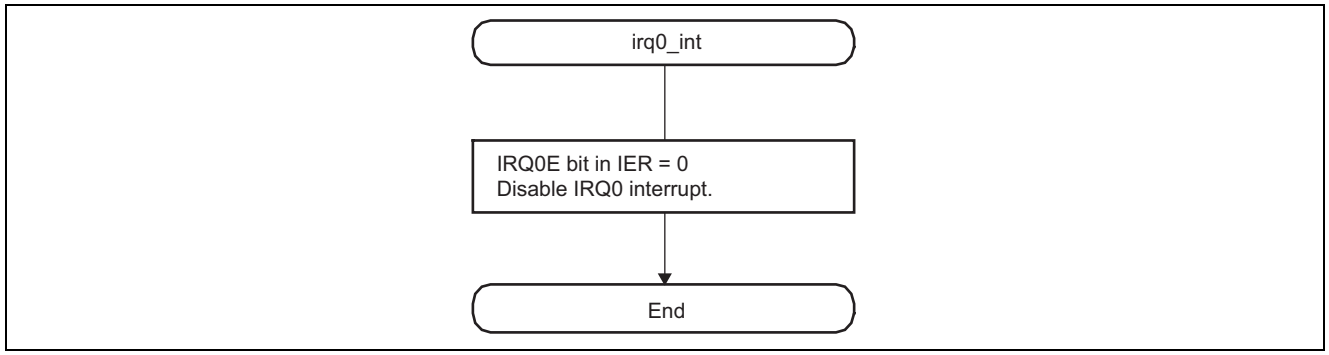
(4) Description of internal registers

The internal registers used in this sample task are described below. The setting values shown in these tables are the values used in this sample task and differ from their initial values.

- IRQ enable register (IER) Address: H'FFFF34

Bit	Bit Name	Setting	R/W	Function
0	IRQ0E	0	R/W	IRQ0 Enable 0: IRQ0 interrupt request is disabled 1: IRQ0 interrupt request is enabled

(5) Flowchart



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Rev.	Date	Page	Summary
1.00	Mar.10.06	—	First edition issued

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