

Driving Differential, Single-Ended, and/or Frequency Generator Crystal Inputs

Abstract

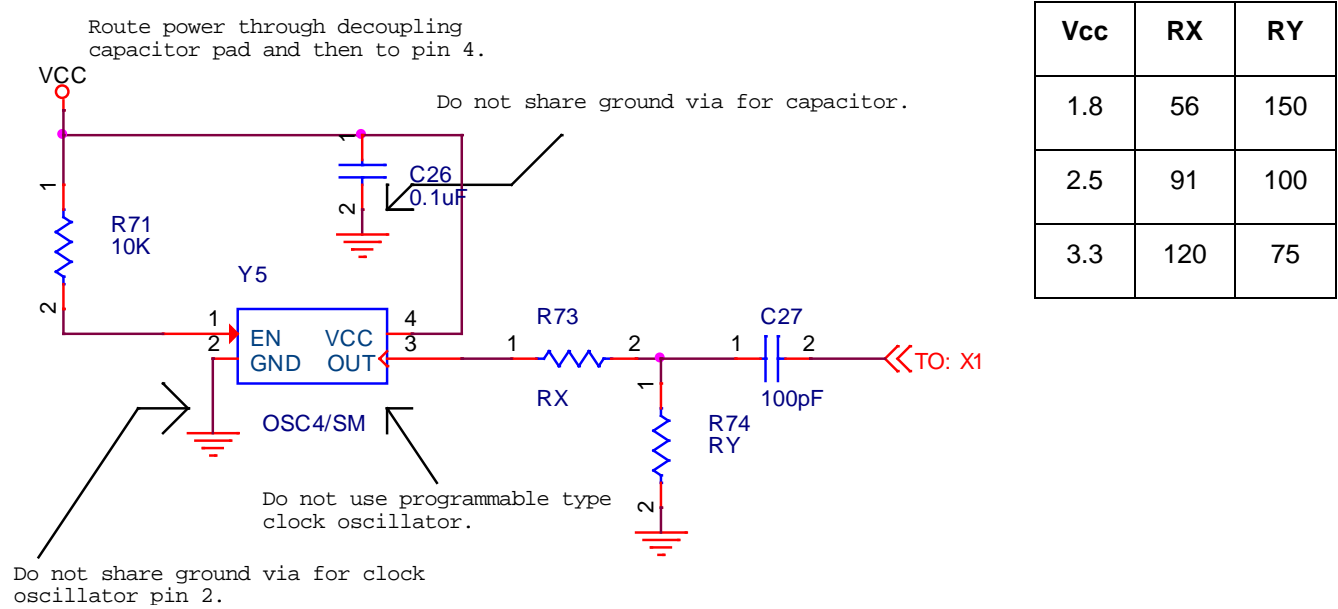
This application note describes various ways to drive the crystal input pin or a differential receiver. The input pin may be named X1 or Xin. If the input is AC coupled, the crystal oscillator circuit will bias the crystal input in its linear analog region. Directly driving Xin with a LVCMOS clock without a capacitor is allowed and is the most common way to connect a clock oscillator to Xin. The clock oscillator output buffer needs to match the impedance of the trace to the Xin pin. The common way to do this is with a series resistor. If this is not done there may be overshoot and undershoot on the input pin. If the clock is DC coupled it should not exceed Vdd of the input or undershoot below ground. If the clock is AC coupled the amplitude should be between 500mV and $V_{dd} * 2/3$.

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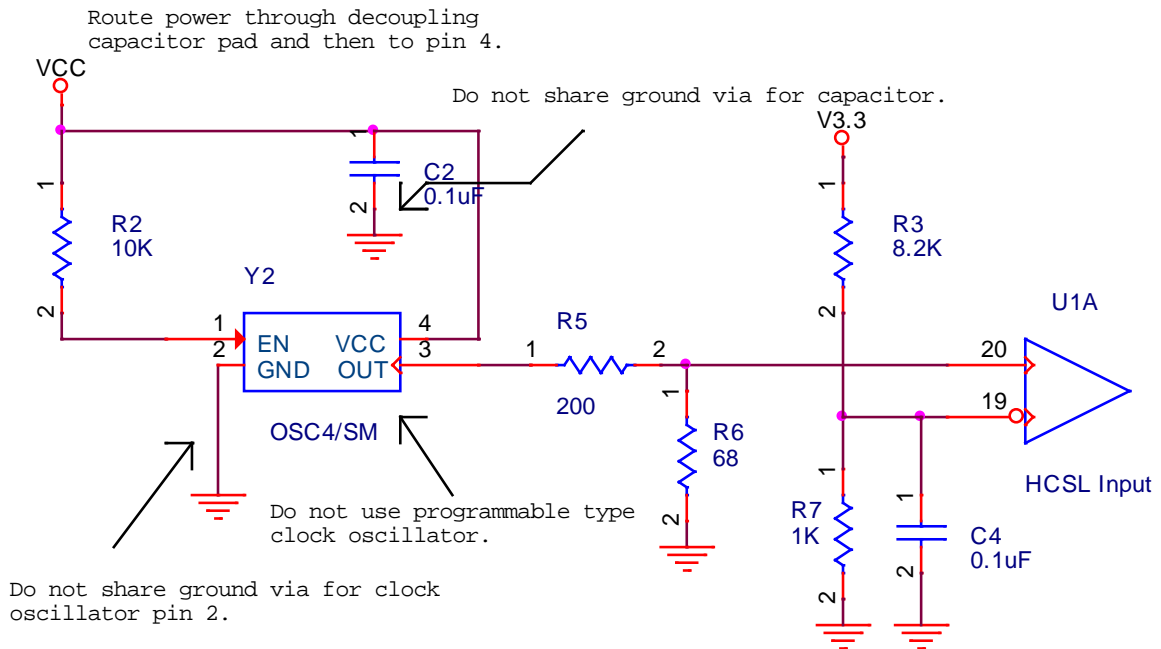
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1. Common LVCMOS Clock Oscillator to Crystal Input

On some devices the maximum V_{High} voltage is 1.2 volts for X_{in} . Verify maximum V_{High} . A resistor voltage divider can be used to reduce V_{High} . If it is not needed R_X should be 33 ohms and R_Y not used.

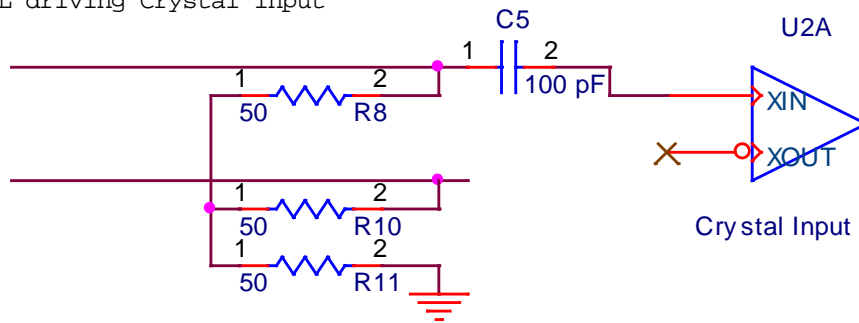


2. Clock Oscillator to Single-Ended HCSL Input



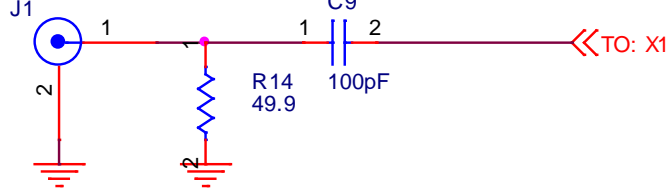
3. LVPECL Driving Crystal Input

LVPECL driving Crystal input



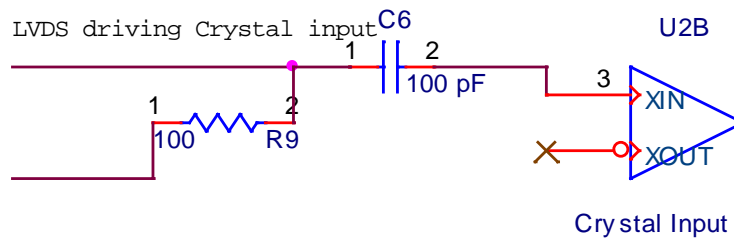
4. SMA or BNC Input

CONNECTOR COAX-50_OHM



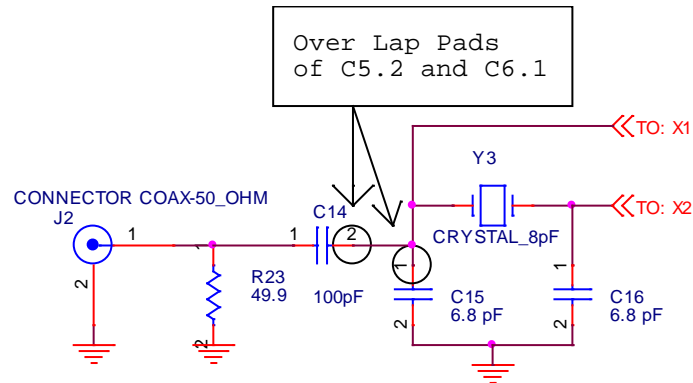
5. LVDS Driving Crystal

LVDS driving Crystal input



6. Stuff Option for Coax Input or Crystal Input

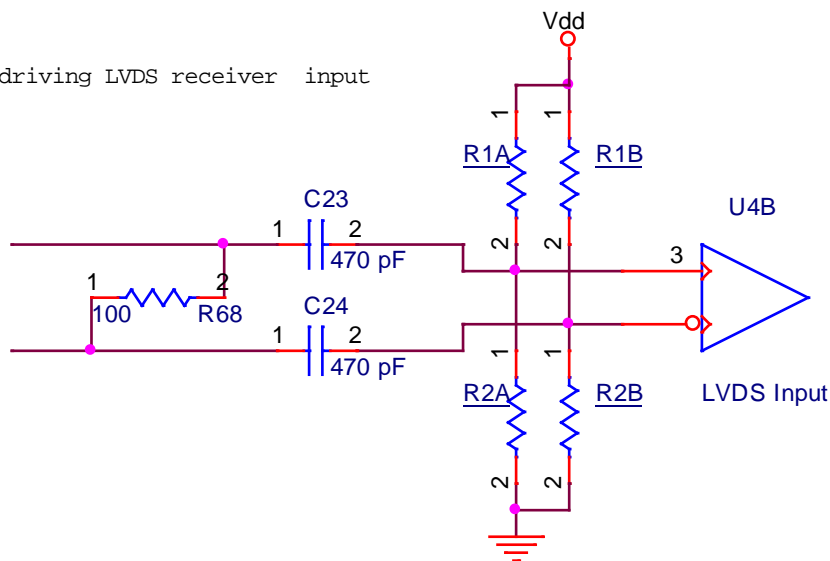
Crystal CL and load capacitors may be different.



Populate Y3, C6, and C7
or
J2, R9, C5.

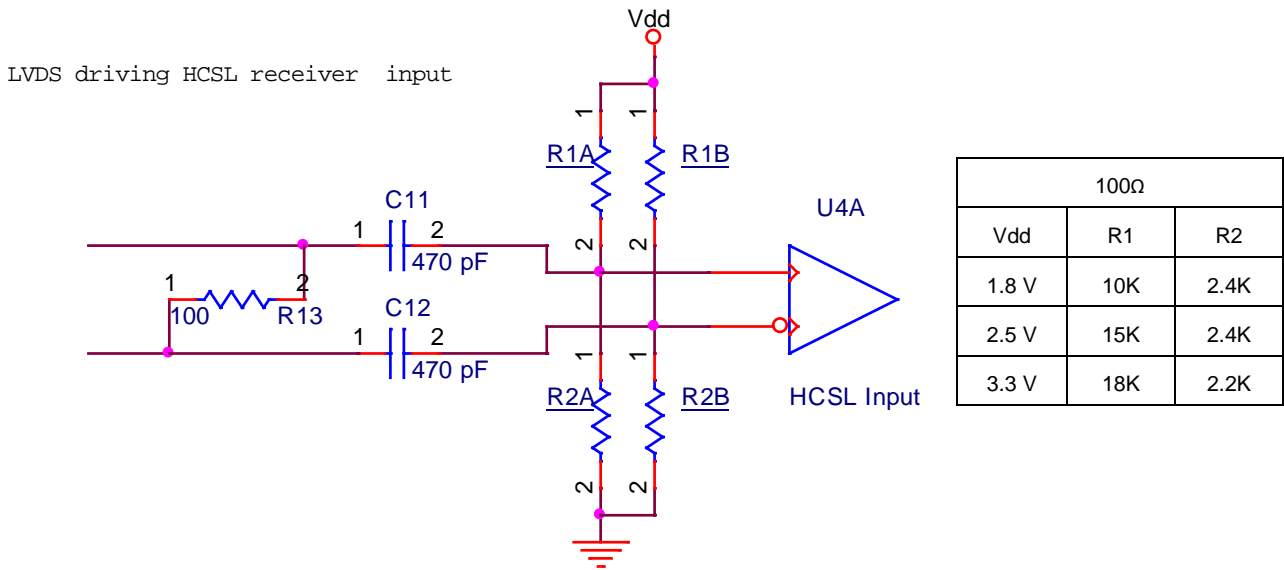
7. HSCL Driving LVDS Input

HSCL driving LVDS receiver input



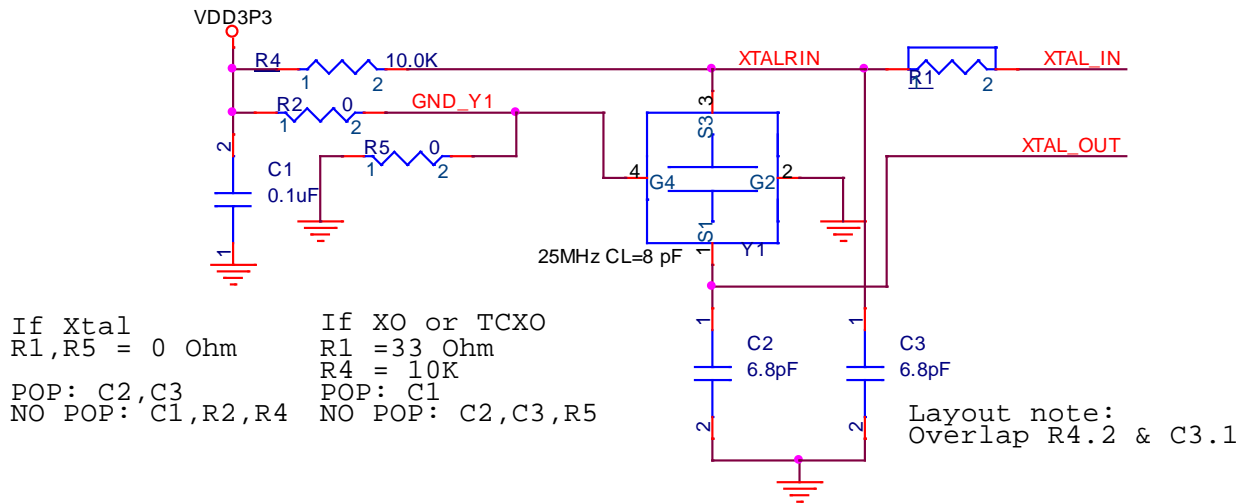
100Ω		
Vdd	R1	R2
1.8 V	3000	6800
2.5 V	4300	4300
3.3 V	5600	3300

8. LVDS Driving HCSL Input



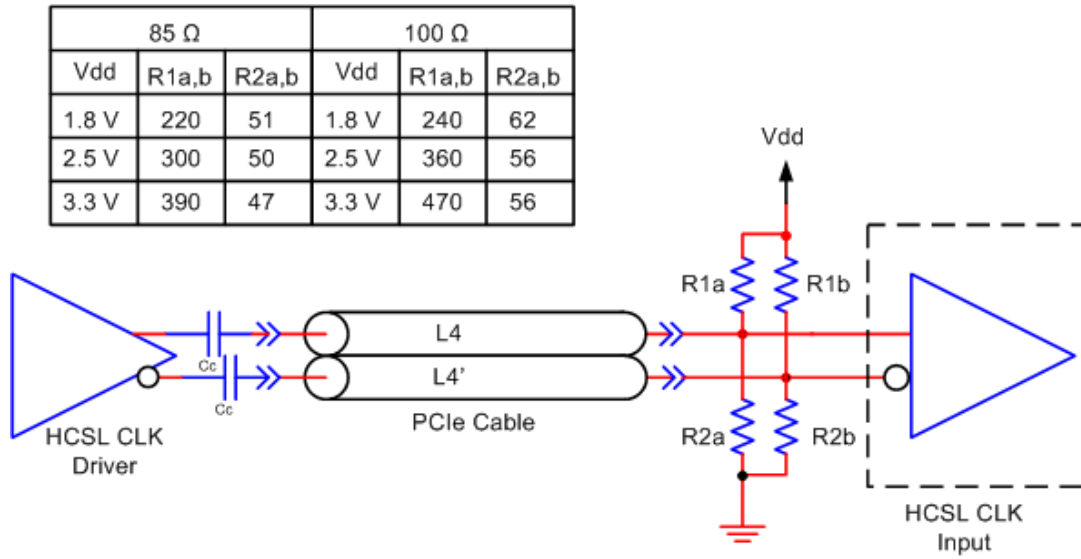
9. Dual Layout for Crystal or Clock Oscillator

Many clock generators have built-in crystal load capacitors. C2 and C3 are No Stuff in that application. TCXO or XO has square wave output. If TCXO sine wave output R1 = 100pF.

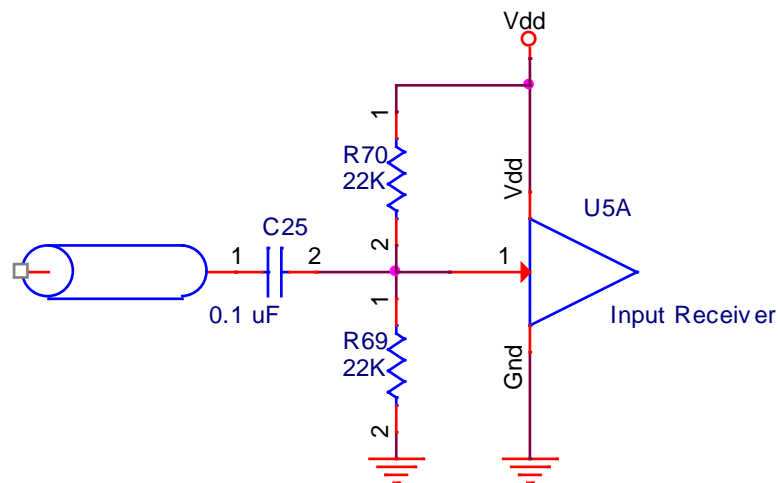


10. Cable-Connected HCSL Clock Termination

For more information, see the PCI Express External Cabling Specification.



11. Level Shifting Single-Ended LVCMOS Input



12. Revision History

Revision	Date	Description
1.0	Jun.18.20	Initial release.

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