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H8SX Family

DMAC Normal Mode Transfer

Introduction

The DMAC performs data transfer in normal transfer mode.

Target Device

H8SX/1582, H8SX/1638, H8SX/1648, H8SX/1658R, H8SX/1663, H8SX/1668R Groups

Preface

Although the writing of this application note is in accord with the hardware manual for the H8SX/1582 Group, the program covered in this application note can be run on the target devices indicated above. However, since some functional modules may be changed for the addition of functionality etc., be sure to perform a thorough evaluation by confirming the details with the hardware manual for the target device.

Contents

1. Specifications

- The DMAC is activated by software and transfers 128 bytes of data from on-chip ROM to on-chip RAM.
- The settings made for DMA transfer are listed in table 1.

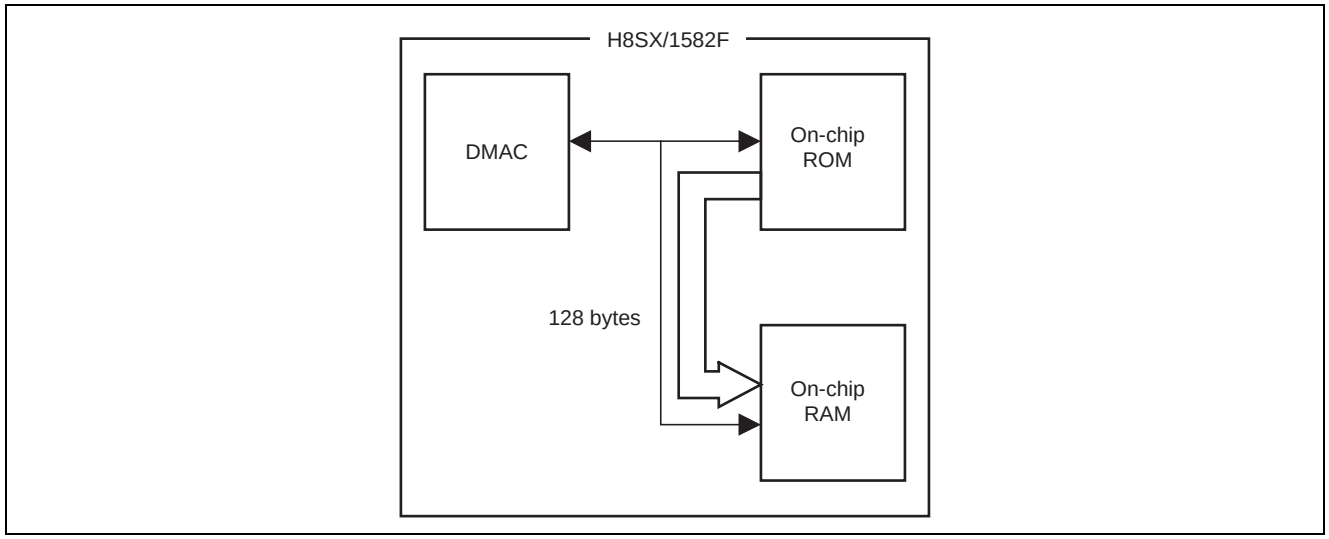


Figure 1 Transfer by DMAC

Table 1 DMA Transfer Settings

Item	Contents
DMA transfer request	Auto request
Bus mode	Cycle stealing mode
Transfer mode	Normal transfer mode
Address mode	Dual address mode
Transfer size	Byte size

2. Conditions for Application

Table 2 Conditions for Application

Item	Contents	
Operating frequency	Input clock:	5 MHz
	System clock (Iϕ):	40 MHz
	Peripheral module clock (Pϕ):	20 MHz
	External bus clock (Bϕ):	20 MHz
Operating mode	Mode 3 (MD1 = 1, MD0 = 1)	
Development tool	High-performance Embedded Workshop Version 4.00.02	
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler Version 6.01.00 (from Renesas Technology Corp.)	
Compile option	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3, -speed = (register, shift, struct, expression)	

Table 3 Section Settings

Address	Section Name	Description
H'001000	P	Program area
	C	Data table storage area
H'FF9000	B	Uninitialized data area (RAM area)

3. Description of Modules Used

Figure 2 shows a block diagram of the DMAC. The block diagram of the DMAC is described below.

- DMA source address register_0 (DSAR_0)
  A 32-bit readable/writable register that specifies the source address of a DMA transfer. The value of this register is automatically updated to the next source address after each transfer.
- DMA destination address register_0 (DDAR_0)
  A 32-bit readable/writable register that specifies the destination address of a DMA transfer. The value of this register is automatically updated to the next destination address after each transfer.
- DMA transfer count register_0 (DTCR_0)
  Sets the size of the data to be transferred (total transfer size). The value of this register will be decremented by a value corresponding to the access size of the transferred data for each data transfer. In this sample task, the transfer size is set as 128 bytes and the data access size as byte. The value of this register is decremented by one during DMA transfer, indicating the remaining transfer size.
- DMA mode control register_0 (DMDR_0)
  Controls operation of the DMAC.
- DMA address control register_0 (DACR_0)
  Sets the address-related operating mode and transfer mode.

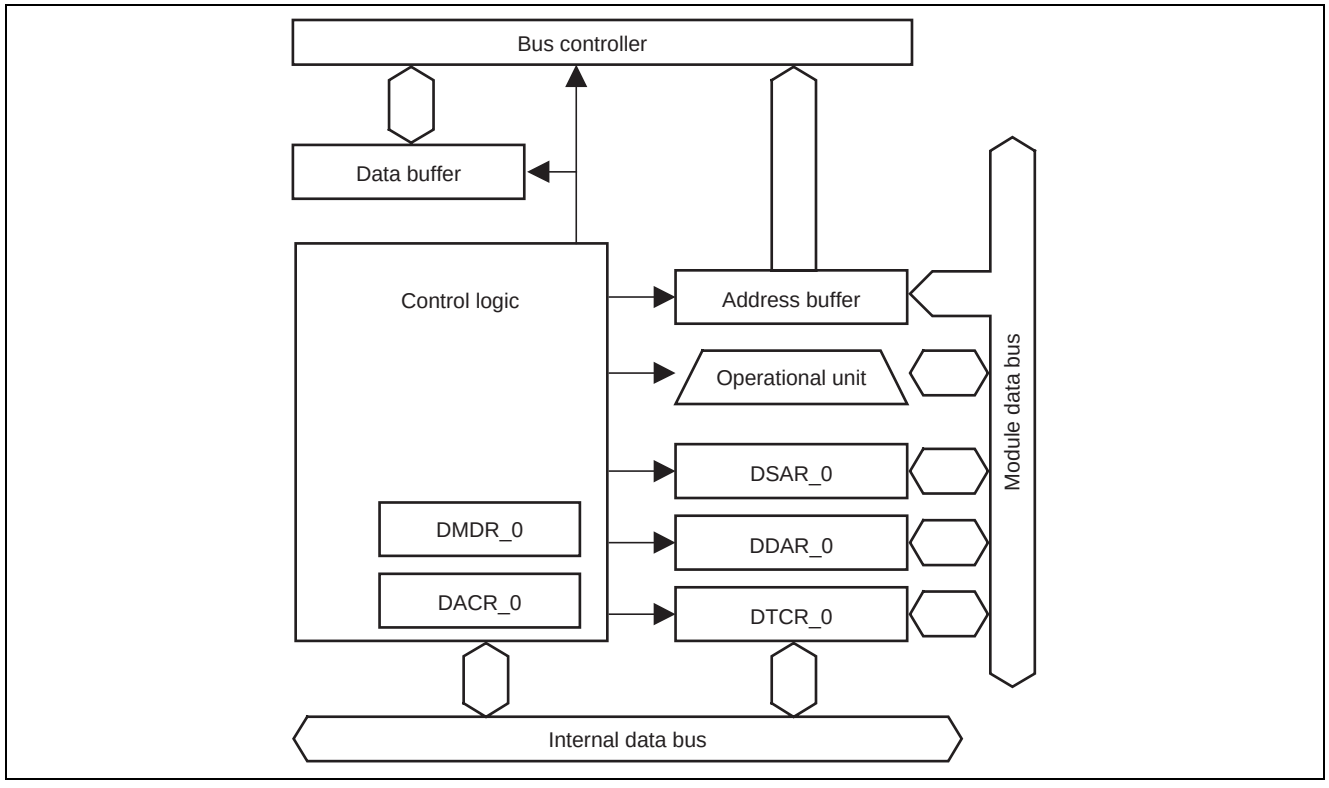


Figure 2 Block Diagram of DMAC

4. Description of Operation

Figure 3 gives an overview of the normal transfer operation in dual address mode.

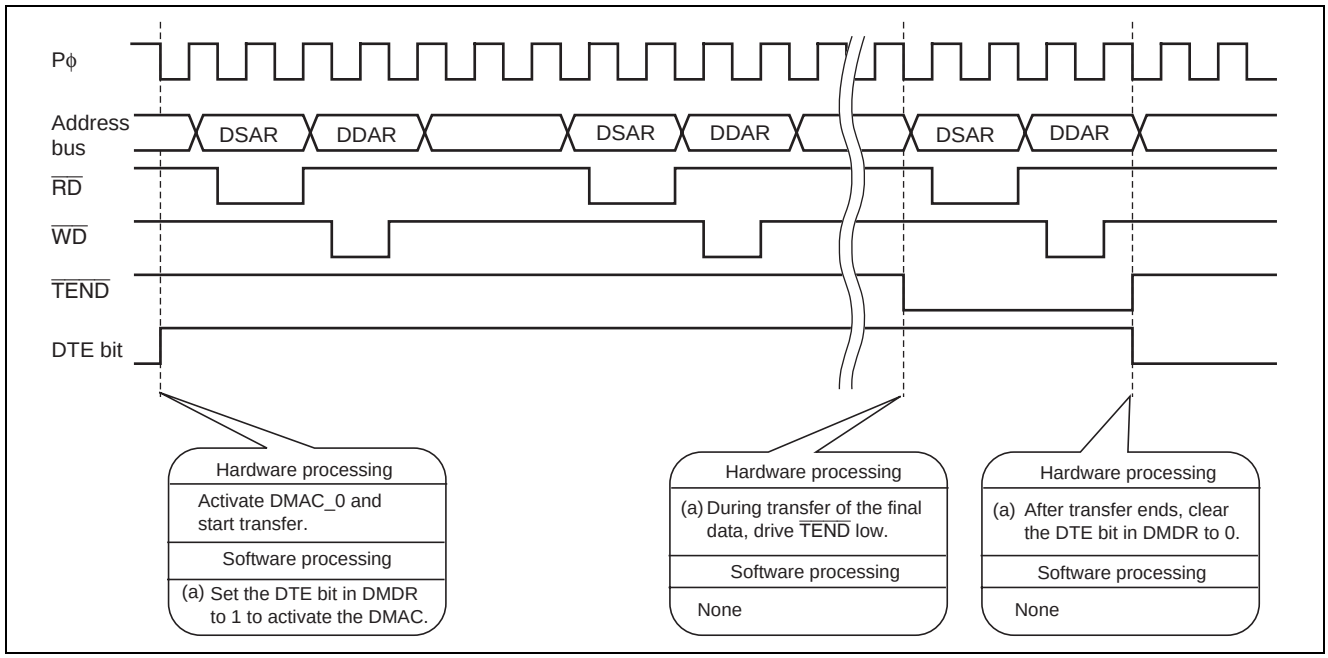


Figure 3 Example of DMA Transfer in Normal Mode

5. Description of Software

5.1 List of Functions

Table 4 List of Functions

Function Name	Functions
init	Initialization routine Sets CCR and the clock, cancels module stop mode, and calls the main function.
main	Main routine Makes the settings for transfer and starts transfer.

5.2 RAM Usage

Table 5 RAM Usage

Type	Variable Name	Description	Used In
unsigned char	ramarea[128]	Destination RAM area	main

5.3 Data Table

Table 6 Data Table

Type	Array Name	Description	Used In
unsigned char	datatable[128]	Stores the source data 128-byte data of H'00, H'01, ..., H'7F	main

5.4 Description of Functions

5.4.1 init Function

(1) Functional overview

Initialization routine which cancels module stop mode, sets the clock, and calls the main function.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. The setting values shown in these tables are the values used in this sample task and differ from their initial values.

- System clock control register (SCKCR) Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Function
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0		These bits select the system clock frequency. The CPU, DMAC,
8	ICK0	0		and DTC modules are driven by the system clock.
				000: Input clock × 8
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0		These bits select the frequency of the peripheral module clock.
4	PCK0	1		001: Input clock × 4
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0		These bits select the frequency of the external bus clock.
0	BCK0	1		001: Input clock × 4

- MSTPCRA, MSTPCRB, and MSTPCRC are the registers that control module stop mode. Setting the bits in these registers places the corresponding modules in module stop mode, and clearing the bits cancels module stop mode.

- Module stop control register A (MSTPCRA) Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Function
15	ACSE	0	R/W	All-module-clock-stop mode enable Enables or disables transition to all-module-clock-stop mode. If this bit is set to 1, all-module-clock-stop mode is entered when the SLEEP instruction is executed by the CPU while all the modules under control of the MSTPCR registers are placed in module stop mode. In all-module-clock-stop mode, even the bus controller and I/O ports are stopped to reduce the supply current. 0: Disables transition to all-module-clock-stop mode. 1: Enables transition to all-module-clock-stop mode.
13	MSTPA13	0	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
4	MSTPA4	1	R/W	A/D converter (unit 1)
3	MSTPA3	1	R/W	A/D converter (unit 0)
1	MSTPA1	1	R/W	16-bit timer pulse unit (TPU channels 11 to 6)
0	MSTPA0	1	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

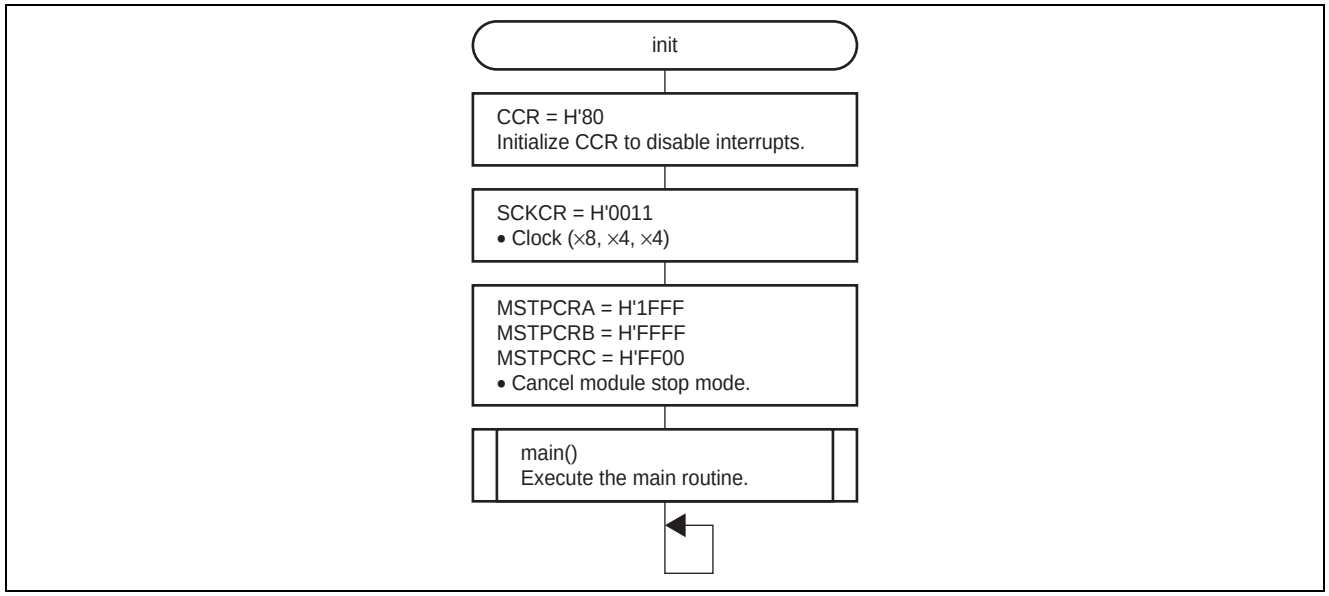
- Module stop control register B (MSTPCRB) Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Function
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communication interface_4 (SCI_4)
11	MSTPB11	1	R/W	Serial communication interface_3 (SCI_3)

- Module stop control register C (MSTPCRC) Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Function
10	MSTPC10	1	R/W	Synchronous serial communication unit 2 (SSU_2)
9	MSTPC9	1	R/W	Synchronous serial communication unit 1 (SSU_1)
8	MSTPC8	1	R/W	Synchronous serial communication unit 0 (SSU_0)
1	MSTPC1	0	R/W	On-chip RAM (H'FF9000 to H'FFBFFF)
0	MSTPC0	0	R/W	Always write the same value to the MSTPC1 and MSTPC0 bits.

(5) Flowchart



5.4.2 main Function

(1) Functional overview

Main routine which sets up the DMAC for transfer and performs the transfer start processing.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. The setting values shown in these tables are the values used in this sample task and differ from their initial values.

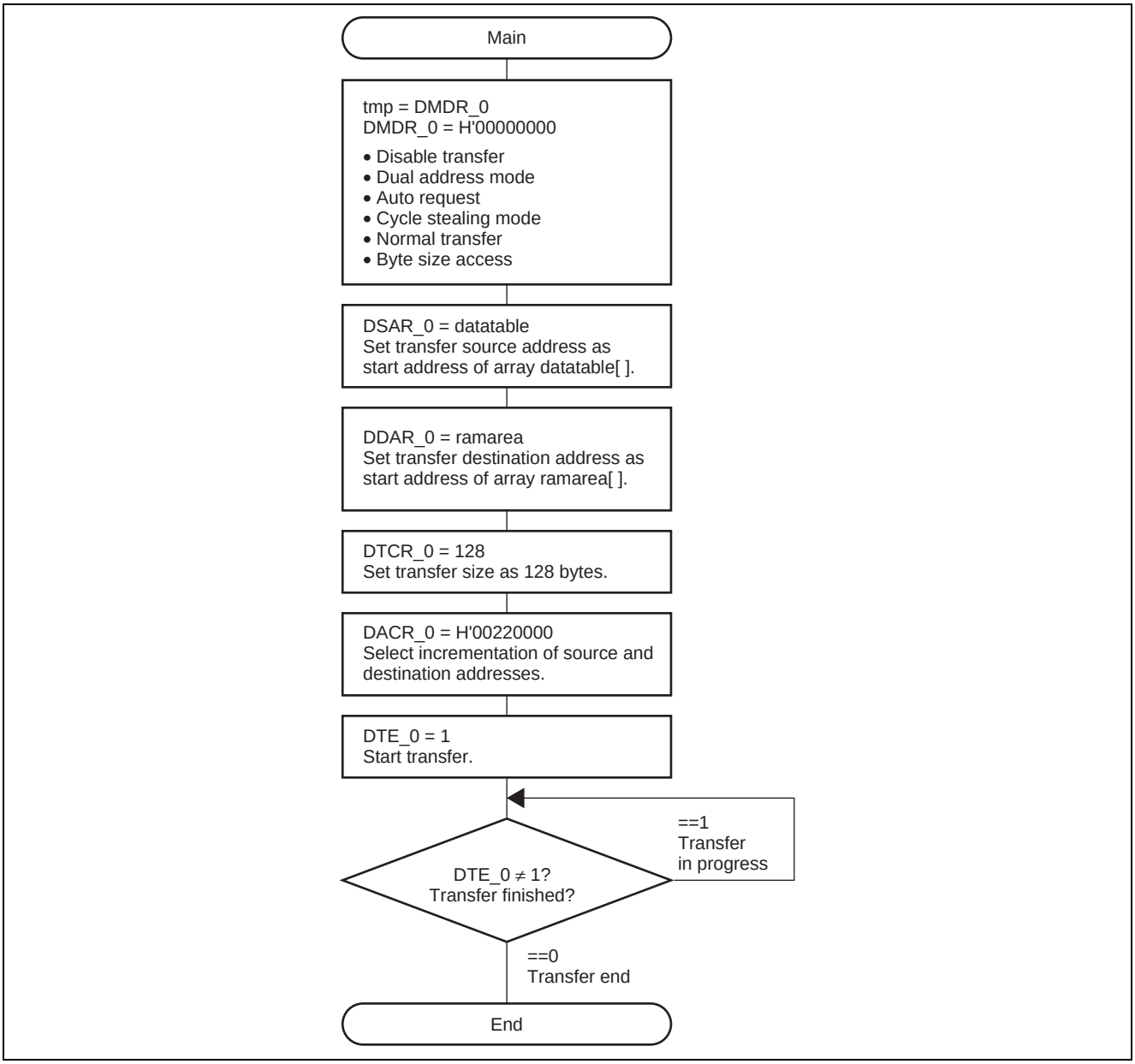
- DMA source address register_0 (DSAR_0) Address: H'FFFC00
  Function: Sets the transfer source address.
  Setting: First address of array datatable
- DMA destination address register_0 (DDAR_0) Address: H'FFFC04
  Function: Sets the transfer destination address.
  Setting: First address of array ramarea
- DMA transfer count register_0 (DTCR_0) Address: H'FFFC0C
  Function: Sets the size of the data for transfer.
  Setting: 128
- DMA mode control register_0 (DMDR_0) Address: H'FFFC14

Bit	Bit Name	Setting	Function
31	DTE	0/1	Data Transfer Enable 0: Data transfer is disabled 1: Data transfer is enabled
15	DTSZ1	0	Data Access Size 1, 0
14	DTSZ0	0	00: Byte size (8 bits)
13	MDS1	0	Transfer Mode Select 1, 0
12	MDS0	0	00: Normal transfer mode
7	DTF1	0	Data Transfer Factor 1, 0
6	DTF0	0	00: Auto request

- DMA address control register_0 (DACR_0) Address: H'FFFC18

Bit	Bit Name	Setting	Function
31	AMS	0	Address Mode Select 0: Dual address mode 1: Single address mode
21	SAT1	1	Source Address Update Mode 1, 0
20	SAT0	0	10: Source address is incremented When the data access size is byte size, incremented by +1
17	DAT1	1	Destination Address Update Mode 1, 0
16	DAT0	0	10: Destination address is incremented When the data access size is byte size, incremented by +1

(5) Flowchart


Main
tmp = DMDR_0
DMDR_0 = H'00000000
• Disable transfer
• Dual address mode
• Auto request
• Cycle stealing mode
• Normal transfer
• Byte size access
DSAR_0 = datatable
Set transfer source address as start address of array datatable[ ].
DDAR_0 = ramarea
Set transfer destination address as start address of array ramarea[ ].
DTCR_0 = 128
Set transfer size as 128 bytes.
DACR_0 = H'00220000
Select incrementation of source and destination addresses.
DTE_0 = 1
Start transfer.
DTE_0 ≠ 1?
Transfer finished?
==1
Transfer in progress
==0
Transfer end
End

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Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Mar.10.06	—	First edition issued
2.00	Mar.07.08	1	Target devices added

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