To our customers,

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April 1\(^{st}\), 2010
Renesas Electronics Corporation

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Introduction
The software DIVD divides an 8-digit binary-coded decimal (BCD) number by another 8-digit BCD number and places the result (an 8-digit BCD number) in general-purpose registers.

Target Device
H8/38024

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1. Arguments

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<thead>
<tr>
<th>Description</th>
<th>Memory area</th>
<th>Data length (bytes)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Dividend</td>
<td>R0, R1</td>
<td>4</td>
</tr>
<tr>
<td>Input Divisor</td>
<td>R2, R3</td>
<td>4</td>
</tr>
<tr>
<td>Output Result of division (quotient)</td>
<td>R0, R1</td>
<td>4</td>
</tr>
<tr>
<td>Output Result of division (remainder)</td>
<td>R4, R5</td>
<td>4</td>
</tr>
<tr>
<td>Output Occurrence of error</td>
<td>Z flag (CCR)</td>
<td>—</td>
</tr>
</tbody>
</table>

2. Changes to Internal Registers and Flags

<table>
<thead>
<tr>
<th>R0</th>
<th>R1</th>
<th>R2</th>
<th>R3</th>
<th>R4</th>
<th>R5</th>
<th>R6</th>
<th>R7</th>
</tr>
</thead>
<tbody>
<tr>
<td>○</td>
<td>○</td>
<td>—</td>
<td></td>
<td>○</td>
<td>○</td>
<td>×</td>
<td>—</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>I</th>
<th>U</th>
<th>H</th>
<th>U</th>
<th>N</th>
<th>Z</th>
<th>V</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>×</td>
<td>—</td>
<td>×</td>
<td>○</td>
<td>×</td>
<td>×</td>
</tr>
</tbody>
</table>

Legend
—: No change  
×: Undefined  
○: Result

3. Specifications

<table>
<thead>
<tr>
<th>Program memory (bytes)</th>
<th>84</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data memory (bytes)</td>
<td>0</td>
</tr>
<tr>
<td>Stack (bytes)</td>
<td>0</td>
</tr>
<tr>
<td>Clock cycle count</td>
<td>1162</td>
</tr>
<tr>
<td>Reentrant</td>
<td>Possible</td>
</tr>
<tr>
<td>Relocation</td>
<td>Possible</td>
</tr>
<tr>
<td>Interrupt</td>
<td>Possible</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>
4. Notes

The clock cycle count (1162) in the specifications is for division of 99999999 by 9999.

5. Description

5.1 Details of functions

1. The following arguments are used with the software DIVD:
   - R0: Sets the upper 4 digits of an 8-digit BCD dividend (32 bits long). After execution of the software DIVD, the upper 4 digits of the result of division (quotient) are placed in this register.
   - R1: Sets the lower 4 bits of the 8-digit BCD dividend (32 bits long). After execution of the software DIVD, the lower 4 digits of the result of division (quotient) are placed in this register.
   - R2: Sets the upper 4 digits of an 8-digit BCD divisor as an input argument.
   - R3: Sets the lower 4 digits of the 8-digit BCD divisor as an input argument.
   - R4: The upper 4 digits of an 8-digit BCD remainder are placed in this register as an output argument.
   - R5: The lower 4 digits of the 8-digit BCD remainder are placed in this register as an output argument.
   - Z flag (CCR): Indicates the occurrence of an error (division by 0) with the software DIVD as an output argument.
     - Z flag = 1: The divisor was 0, indicating an error.
     - Z flag = 0: The divisor was not 0.

2. The following figure illustrates the execution of the software DIVD. When the input arguments are set as shown in (1), the result of division is placed in the registers as shown in (2).

![Figure 1 Example of Software DIVD Execution](image)

3. Table 1 lists the result of division with 0 placed in input arguments.

<table>
<thead>
<tr>
<th>Input arguments</th>
<th>Output arguments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dividend (R0, R1)</td>
<td>Divisor (R2, R3)</td>
</tr>
<tr>
<td>H'**** ****</td>
<td>H'0000 0000</td>
</tr>
<tr>
<td>H'0000 0000</td>
<td>H'**** ****</td>
</tr>
<tr>
<td>H'0000 0000</td>
<td>H'0000 0000</td>
</tr>
</tbody>
</table>

Note: H'**** **** is a hexadecimal number.
5.2 Notes on usage

1. When the upper bits are not used (see figure 2), set them to 0; otherwise, a correct result cannot be obtained because division is done on the numbers including indeterminate data placed in the upper bits.

![Figure 2 Example of Division with Upper Bits Unused](image)

2. After execution of the software DIVD, the dividend will be lost because the quotient is placed in R0 and R1. When the dividend is still needed after software DIVD execution, save it in memory.

5.3 Data memory

The software DIVD uses no data memory.
### 5.4 Example of usage

Set a dividend and a divisor in the registers and call the software DIVD as a subroutine.

<table>
<thead>
<tr>
<th>WORK1</th>
<th>. RES. W</th>
<th>2</th>
<th>Reserve a data memory area in which the user program places an 8-digit BCD dividend.</th>
</tr>
</thead>
<tbody>
<tr>
<td>WORK2</td>
<td>. RES. W</td>
<td>2</td>
<td>Reserve a data memory area in which the user program places an 8-digit BCD divisor.</td>
</tr>
<tr>
<td>WORK3</td>
<td>. RES. W</td>
<td>2</td>
<td>Reserve a data memory area in which the user program places an 8-digit BCD quotient.</td>
</tr>
<tr>
<td>WORK4</td>
<td>. RES. W</td>
<td>2</td>
<td>Reserve a data memory area in which the user program places an 8-digit BCD remainder.</td>
</tr>
<tr>
<td></td>
<td>MOV. W @WORK1, R0</td>
<td></td>
<td>Place the 8-digit BCD dividend set by the user program in the input argument (R0 and R1).</td>
</tr>
<tr>
<td></td>
<td>MOV. W @WORK1+2, R1</td>
<td></td>
<td>Place the 8-digit BCD divisor set by the user program in the input argument (R2 and R3).</td>
</tr>
<tr>
<td></td>
<td>MOV. W @WORK2, R2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>MOV. W @WORK2+2 R3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>JSR</td>
<td>@DIVD</td>
<td></td>
<td>Call the software DIVD as a subroutine.</td>
</tr>
<tr>
<td>BEQ</td>
<td>ERROR</td>
<td></td>
<td>Branch to the error (division by 0) processing routine when an error (division by 0) has occurred as a result of division.</td>
</tr>
<tr>
<td></td>
<td>MOV. W R0, @WORK3</td>
<td></td>
<td>Place the result set in the output argument in the data memory of the user program.</td>
</tr>
<tr>
<td></td>
<td>MOV. W R1, @WORK3+2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>MOV. W R4, @WORK4</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>MOV. W R5, @WORK4+2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ERROR</td>
<td>Dividion-by-0 processing routine</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Division-by-0 processing routine

Reserve a data memory area in which the user program places an 8-digit BCD dividend.

Reserve a data memory area in which the user program places an 8-digit BCD divisor.

Reserve a data memory area in which the user program places an 8-digit BCD quotient.

Reserve a data memory area in which the user program places an 8-digit BCD remainder.
5.5 Operation

1. Division of decimal numbers can be done by performing a series of subtractions. Figure 3 shows an example of division (64733088 ÷ 5).

2. The program runs in the following steps:
   a. The dividend is shifted 4 bits (1 digit of the BCD) to the left to place the upper 4 bits of the dividend in the lower 4 bits of the result of division (remainder).
   b. The divisor is subtracted from the dividend. Subtractions are repeated until the result becomes negative. The number of subtractions thus done is placed in the lower 4 bits (the least significant digit) of the dividend ((2)→(3)→(1) in figure 3). When the result has become negative, the divisor is added to the result (remainder) to return to the value before subtractions ((4) in figure 3).
   c. Steps a to b are repeated as many times as 8 digits.
6. Flowchart

DIVD

\[
\begin{align*}
#H'0000 & \rightarrow R4 \\
R4 & \rightarrow R5 \\
R4 & = R2 \\
& \text{No} \\
& \text{Yes} \\
& \text{EXIT} \\
\text{No} & \rightarrow \text{LBL1} \\
\text{Yes} & \rightarrow \text{LBL2} \\
#H'08 & \rightarrow R6L \\
#H'04 & \rightarrow R6H \\
\text{R6H} & \neq 0 \\
& \text{No} \\
& \text{Yes} \\
& \text{LBL3} \\
\end{align*}
\]

- Clear R4 and R5 to 0.
- Exit when the divisor (R2, R3) is 0.
- Place the number of digits of the divisor data in R6L.
- Place the upper 4 bits of the dividend in the lower 4 bits of the result (remainder).

1

2

3
C flag (CCR) = 0

Yes

R5L - R3L → R5L
Decimal correction of R5L
R5H - R3H - C → R5H
Decimal correction of R5H
R4L - R2L - C → R4L
Decimal correction of R4L
R4H - R2H - C → R4H
Decimal correction of R4H

----- Add H'01 to R1L

No

----- Perform decimal subtraction of the divisor (R2, R3) from the remainder (R4, R5).

Branch when the result of decimal subtraction is positive. When it is negative, perform decimal addition of the divisor (R2, R3) to the remainder (R4, R5) and subtracts H'01 from R1L.

Yes

R5L - R3L → R5L
Decimal correction of R5L
R5H - R3H - C → R5H
Decimal correction of R5H
R4L - R2L - C → R4L
Decimal correction of R4L
R4H - R2H - C → R4H
Decimal correction of R4H

----- Decrement R6L (number of digits).

No

----- Branch when R6L is not #H'00.

0 → Z flag

----- Place 0 in the Z flag.

LBL2

3

R6L = 0

Yes

----- Add H'01 to R1L

No

R1L - #H'01 → R1L

2

EXIT

RTS
7. Program List

*** H8/300 ASSEMBLER VER 1.0B ** 08/18/92 10:02:05 PAGE 1

PROGRAM NAME =
1 ;***********************************************************************
2 ;*
3 ;*  00 - NAME  :MULTIPLE-PRECISION DECIMAL DIVISION (DIVD)
4 ;*
5 ;***********************************************************************
6 ;*
7 ;*  ENTRY  :R2,R3 (DIVISOR)
8 ;*   R0,R1 (DIVIDEND)
9 ;*
10 ;*  RETURNS  :R0,R1 (QUOTIENT)
11 ;*   R4,R5 (RESIDUAL)
12 ;*   Z flag OF CCR (Z=1;FALSE , Z=0;TRUE)
13 ;*
14 ;***********************************************************************
15 ;
16 DIVD_cod C 0000 .SECTION DIVD_code,CODE,ALIGN=2
17 .EXPORT DIVD
18 ;
19 ;
20 DIVD_cod C 0000 00000000 DIVD .EQU $ ;Entry point
21 DIVD_cod C 0004 0D45 MOV.W #H'0000,R4 ;Clear R4
22 DIVD_cod C 0006 1D42 CMP.W R4,R2
23 DIVD_cod C 0008 4604 BNE LBL1 ;Branch if Z=0
24 DIVD_cod C 000A 1D53 CMP.W R5,R3
25 DIVD_cod C 000C 4744 BEQ EXIT ;Branch if Z=1 then exit
26 DIVD_cod C 000E LBL1
27 DIVD_cod C 0010 FE08 MOV.B #H'08,R6L ;Set bit counter1
28 DIVD_cod C 0012 0A09 INC.B R1L ;Increment R1L
29 DIVD_cod C 0014 1201 SHLL.B R1L ;Shift dividend
30 DIVD_cod C 0016 1208 ROTXL.B R1H
31 DIVD_cod C 0018 1200 ROTXL.B R0L
32 DIVD_cod C 001A 1205 ROTXL.B R5L
33 DIVD_cod C 001C 1208 ROTXL.B R5H
34 DIVD_cod C 001E 1204 ROTXL.B R4L
35 DIVD_cod C 0020 1F0C DAS.B R4H
36 DIVD_cod C 0022 1A06 DEC.B R6H ;Decrement bit counter2
37 DIVD_cod C 0024 46EC BNE LBL3 ;Branch if Z=0
38 DIVD_cod C 0026 0409 INC.B R1L ;Increment R1L
39 DIVD_cod C 0028 18BD SUB.B R3L,R5L ;R5L - R3L -> R5L
40 DIVD_cod C 002A 1F0D DAS.B R5L ;Decimal adjust R5L
41 DIVD_cod C 002C 1E35 SUBX.B R3H,R5H ;R5H - R3H - C -> R3H
42 DIVD_cod C 002E 1F05 DAS.B R5H ;Decimal adjust R5H
43 DIVD_cod C 0030 1EAC SUBX.B R2L,R4L ;R4L - R2L - C -> R4L
44 DIVD_cod C 0032 1F0C DAS.B R4L ;Decimal adjust R4L
45 DIVD_cod C 0034 1E24 SUBX.B R2H,R4H ;R4H - R2H - C -> R4H
46 DIVD_cod C 0036 1F04 DAS.B R4H ;Decimal adjust R4H
51  DIVD_cod C  0038  44EC  BCC  LBL4  ;Branch if C = 0
52       
53  DIVD_cod C  003A  08BD  ADD.B  R3L,R5L  ;R3L + R5L -> R5L
54  DIVD_cod C  003C  0F0D  DAA.B  R5L  ;Decimal adjust R5L
55  DIVD_cod C  003E  0E35  ADDX.B  R3H,R5H  ;R3H + R5H + C -> R5H
56  DIVD_cod C  0040  0F05  DAA.B  R5H  ;Decimal adjust R5H
57  DIVD_cod C  0042  0EAC  ADDX.B  R2L,R4L  ;R2L + R4L + C -> R4L
58  DIVD_cod C  0044  0F0C  DAA.B  R4L  ;Decimal adjust R4L
59  DIVD_cod C  0046  0E24  ADDX.B  R2H,R4H  ;R2H + R4H + C -> R4H
60  DIVD_cod C  0048  0F04  DAA.B  R4H  ;Decimal adjust R4H
61  DIVD_cod C  004A  1A09  DEC.B  R1L  ;Decrement R1L
62  DIVD_cod C  004C  1A0E  DEC.B  R6L  ;Decrement bit counter1
63  DIVD_cod C  004E  46C0  BNE  LBL2  ;Branch if carry
64  DIVD_cod C  0050  06FB  ANDC.B  #B'11111011,CCR  ;Clear Z flag of CCR
65  DIVD_cod C  0052  EXIT  
66  DIVD_cod C  0052  5470  RTS  
67       
68       .END

*****TOTAL ERRORS 0
*****TOTAL WARNINGS 0
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csc@renesas.com

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