To our customers,

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M16C/80 Series

Dividing BCD

1.0 Abstract

This program divides 8-digit BCD by using registers.

2.0 Introduction

This program divides 8-digit BCD together by using registers. Set the dividend in A1 and A0 and the divisor in R3 and R1 beginning with the upper half, respectively. The quotient and the remainder are output to A1 and A0, and to R2 and R0, beginning with the upper half, respectively. The zero divide information is output to the Z flag.

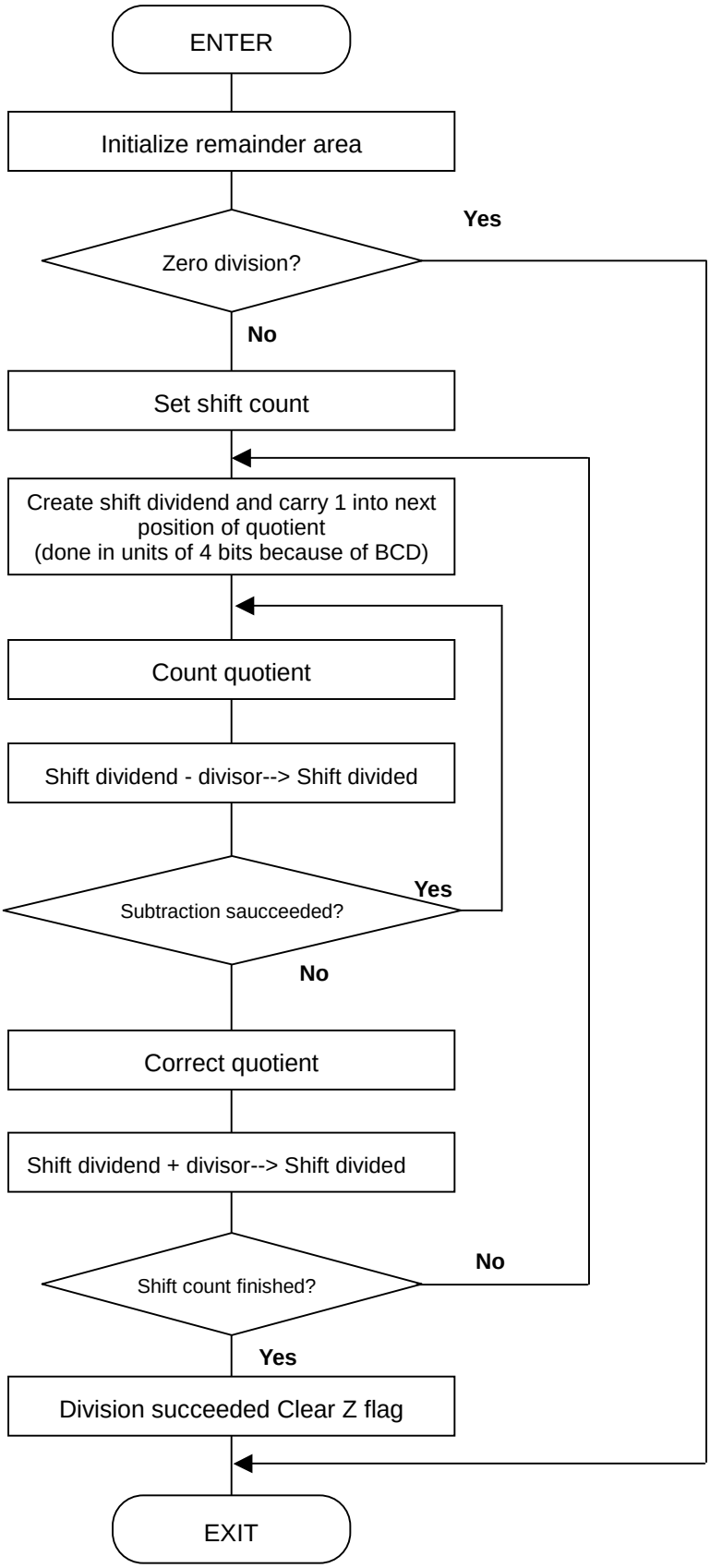
In this program, data for BCD calculation is loaded from the dividend 4 high-order bits at a time to create the dividend to be operated on and the divisor count can be subtracted is counted to obtain the quotient. A carry deriving from the divide operation is shifted in units of 4 bits to the next high-order digit.

Z	Meaning
0	Quotient and remainder are valid.
1	Quotient and remainder are invalid because division by zero is attempted.

Subroutine name : BCD_DIVIDE8	ROM capacity : 67byte
Interrupt during execution:Accepted	Number of stacks used : 3byte

Register/memory	Input	Output	Usage condition
R0	-	Lower half of remainder	←
R1	Lower half of divisor	Does not change	←
R2	-	Upper half of remainder	←
R3	Upper half of divisor	Does not change	←
A0	Lower half of dividend	Lower half of quotient	←
A1	Upper half of dividend	Upper half of quotient	←
CNT	-	Indeterminate	Shift count
Z flag	-	Zero divide information	←
Usage precautions	CNT is allocated in a stack area by configuring a stack frame as a temporary variable area in the program. Therefore, the value of CNT when program execution is completed is indeterminate. The dividend is destroyed as a result of program execution.		

3.0 Flowchart



4.0 Programming Code

```
;*****************************************************************
; *
;       M16C Program Collection
;       CPU : M16C/80 series
; *
;*****************************************************************
VromTOP         .EQU    0FE0000H                ; Declares start address of ROM
FBcnst          .EQU    001000H                 ; Assumed FB register value
;===================================================================
;    Title: Dividing 8-digit BCD
;    Outline: Divides 8-digit BCD using registers
;    Input:      ------------------------------>      Output:
;    R0()                                        R0(Lower half of remainder)
;    R1(Lower half of divisor)                   R1(Lower half of divisor)
;    R2()                                        R2(Upper half of remainder)
;    R3(Upper half of divisor)                   R3(Upper half of divisor)
;    A0(Lower half of dividend)                  A0(Lower half of quotient)
;    A1(Upper half of dividend)                  A1(Upper half of quotient)
;    Stack amount used: 3byte
;    Notes: A1A0 , R3R1
;           Zero division is returned by Z flag
;===================================================================
                .SECTION        PROGRAM,CODE
                .ORG            VromTOP                 ; ROM area
                .FB             FBcnst                  ; Sets provisional FB register value
BCD_DIVIDE8:                                            ;
;-----------------------------------------------------;
;Declaration of temporary variables;
;-----------------------------------------------------;
CNT             .EQU    -1                              ; Shift count counter
  ENTER         #1                                      ; Sets stack frame
  MOV.L         #0,R2R0                                 ; Initializes remainder area
  CMP.L         #0,R3R1                                 ;
  JEQ           BCD_DIVIDE8exit                         ; --> Zero division
BCD_DIVIDE8_10:                                         ;
  MOV.B         #8,CNT[FB]                              ; Sets number of digits to be divided
BCD_DIVIDE8_20:                                         ;
  OR.W          #1000H,R2                               ; Specifies 4-bit carry
BCD_DIVIDE8_30:                                         ;
  SHL.W         #1,A0                                   ; Pushes dividend and carries 1 in quotient
  ROLC.W        A1                                      ; Pushes dividend and carries 1 in quotient
  ROLC.W        R0                                      ; Creates dividend
  ROLC.W        R2                                      ;
  JNC           BCD_DIVIDE8_30                          ; --> 4-bit carry not completed
BCD_DIVIDE8_40:                                         ;
  ADD.L:S       #1,A0                                   ; Quotient + 1
  DSUB.W        R1,R0                                   ; Subtraction by divisor
  XCHG.W        R2,R0                                   ; Moves data
  XCHG.W        R3,R1                                   ;
  DSBB.W        R1,R0                                   ;
  XCHG.W        R2,R0                                   ; Moves data
  XCHG.W        R3,R1                                   ;
  JGEU          BCD_DIVIDE8_40                          ; --> Subtraction by divisor succeeded
  DEC.W         A0                                      ; Quotient corrected
  DADD.W        R1,R0                                   ; Restored to original data because divisor subtraction failed
  XCHG.W        R2,R0                                   ; Moves data
  XCHG.W        R3,R1                                   ;
  DADC.W        R1,R0                                   ;
```

```
    XCHG.W      R2,R0                       ; Moves data
    XCHG.W      R3,R1                       ;
    ADJNZ.B     #-1,CNT[FB],BCD_DIVIDE8_20  ; --> Executes next digit
    FCLR        Z                           ; Division succeeded
BCD_DIVIDE8exit:                            ;
    EXITD                                   ; Clears stack frame
    ;                                       ;
                .END ;
```

5.0 Reference

MCU Technical Information Homepage

http://www.infomicom.maec.co.jp/indexe.htm
(or http://www.mdece.com/ , http://www.mitsubishichips.com/products/mcu/index.html or your local Web Site.)

Technical Support

E-mail: support@apl.maec.co.jp
(or your local support E-mail address. A private e-mail address should NOT be used.)

Data Sheet

M16C/80 group
(Use the latest version on the Homepage: http://www.infomicom.maec.co.jp/indexe.htm)

User's Manual

M16C/80 group
(Use the latest version on the Homepage: http://www.infomicom.maec.co.jp/indexe.htm)

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Renesas Technology Corp.

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