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M16C/62P and M16C/63, 64, 64A, 65 Groups

Differences in Flash Memory CPU Rewrite Modes

1. Abstract

This document describes differences in flash memory CPU rewrite modes between the M16C/62P Group and M16C/63, 64, 64A and 65 Groups.

2. Introduction

The application example described in this document applies to the following microcomputers (MCUs):

- MCUs: M16C/62P Group
  M16C/63 Group
  M16C/64 Group
  M16C/64A Group
  M16C/65 Group

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above groups. Check the hardware manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Specification Comparison

Table 3.1 lists the differences in the flash memory CPU rewrite modes.

Table 3.1 Differences in Functions

Item			M16C/62P Group	M16C/63, 64, 64A and 65 Groups
Flash-related registers			FIDR, FMR0, FMR1	FMR0, FMR1, FMR2, FMR3 (M16C/63 only), FMR6, and PRG2C
Flash areas			User ROM Data flash (block A)	Program ROM 1 Program ROM 2 Data flash (block A, block B)
Registers used and settings in EW0 mode			FMR01 bit (1) is 1 FMR11 bit (2) is 0	FMR01 bit (1) is 1 FMR11 bit (2) is 1 FMR6 register is 02h
Registers used and settings in EW1 mode			FMR01 bit (1) is 1 FMR11 bit (2) is 1	FMR01 bit (1) is 1 FMR11 bit (2) is 1 FMR6 register is 03h
Software commands	Program	Program method	In 1-word (2-byte) units	In 2-word (4-byte) units
		Command code	xx40h	xx41h
	Erase all unlocked block		Yes	N/A
	Block blank check		N/A	Yes
User boot function			N/A	Yes (FMR05 bit is 1)
Suspend function			N/A	Yes: M16C/63 N/A: M16C/64, 64A, 65

Notes:
1. The FMR01 bit is bit 1 in the FMR0 register.
2. The FMR11 bit is bit 1 in the FMR1 register.

4. Detailed Comparison

4.1 Flash-related Register Comparison

Table 4.1 lists the differences in the flash memory CPU rewrite modes.

Table 4.1 Differences in Flash-related Registers

Item		M16C/62P Group	M16C/63, 64, 64A and 65 Groups
Flash Memory Control Register 0 (FMR0)	FMR05 bit	User ROM area select bit (1) 0: Boot ROM area is accessed 1: User ROM area is accessed	Reserved bit Set to 0 when not in user boot mode. Set to 1 in user boot mode.
Flash Memory Control Register 1 (FMR1)	FMR11 bit	EW1 mode select bit 0: EW0 mode 1: EW1 mode	Write to FMR6 register enable bit register 0: Disabled 1: Enabled
	FMR17 bit	Reserved bit	Data flash weight bit 0: One wait 1: Follow the setting of the PM17 bit.
Flash Memory Control Register 2 (FMR2)	FMR22 bit	N/A	Slow read mode enable bit 0: Disabled 1: Enabled
	FMR23 bit	N/A	Low current consumption read mode enable bit 0: Disabled 1: Enabled
Flash Memory Control Register 6 (FMR6)	FMR60 bit	N/A	EW1 mode select bit 0: EW0 mode 1: EW1 mode
Program 2 Area Control Register (PRG2C)	PRG2C0 bit	N/A	Program ROM 2 disable bit 0: Enable program ROM 2 1: Disable program ROM 2
	IRON bit	N/A	Program ROM 1 of addresses (40000h to 7FFFFh) (2) 0: Disabled 1: Enabled

Notes:
1. Only applies when in boot mode.
2. In the M16C/65 Group, only in products with program ROM 1 over 512 KB.

4.2 Memory Map of Flash Memory Area

The memory map of flash memory and its block size differ between the M16C/62P Group and the M16C/63, 64, 64A and 65 Groups.
Table 4.2 lists the differences in memory maps of their flash area. Figure 4.1 shows the comparison of memory maps.

Table 4.2 Differences in Flash Memory Area Memory Maps

Item		M16C/62P Group	M16C/63, 64, 64A and 65 Groups
Data flash	Block A (4 KB)	0F000h to 0FFFFh	0E000h to 0EFFFh
	Block B (4 KB)	N/A	0F000h to 0FFFFh
Program ROM	Program ROM 1 (1)	080000h to 0FFFFFh (2)	080000h to 0FFFFh (2)
	Program ROM 2	N/A	010000h to 013FFFh (3)

Notes:
1. User ROM area in the M16C/62P Group.
2. Applies to the 512 KB version.
3. Can be used when the PRG2C0 bit in the PRG2C register is 0 (enable program ROM 2).

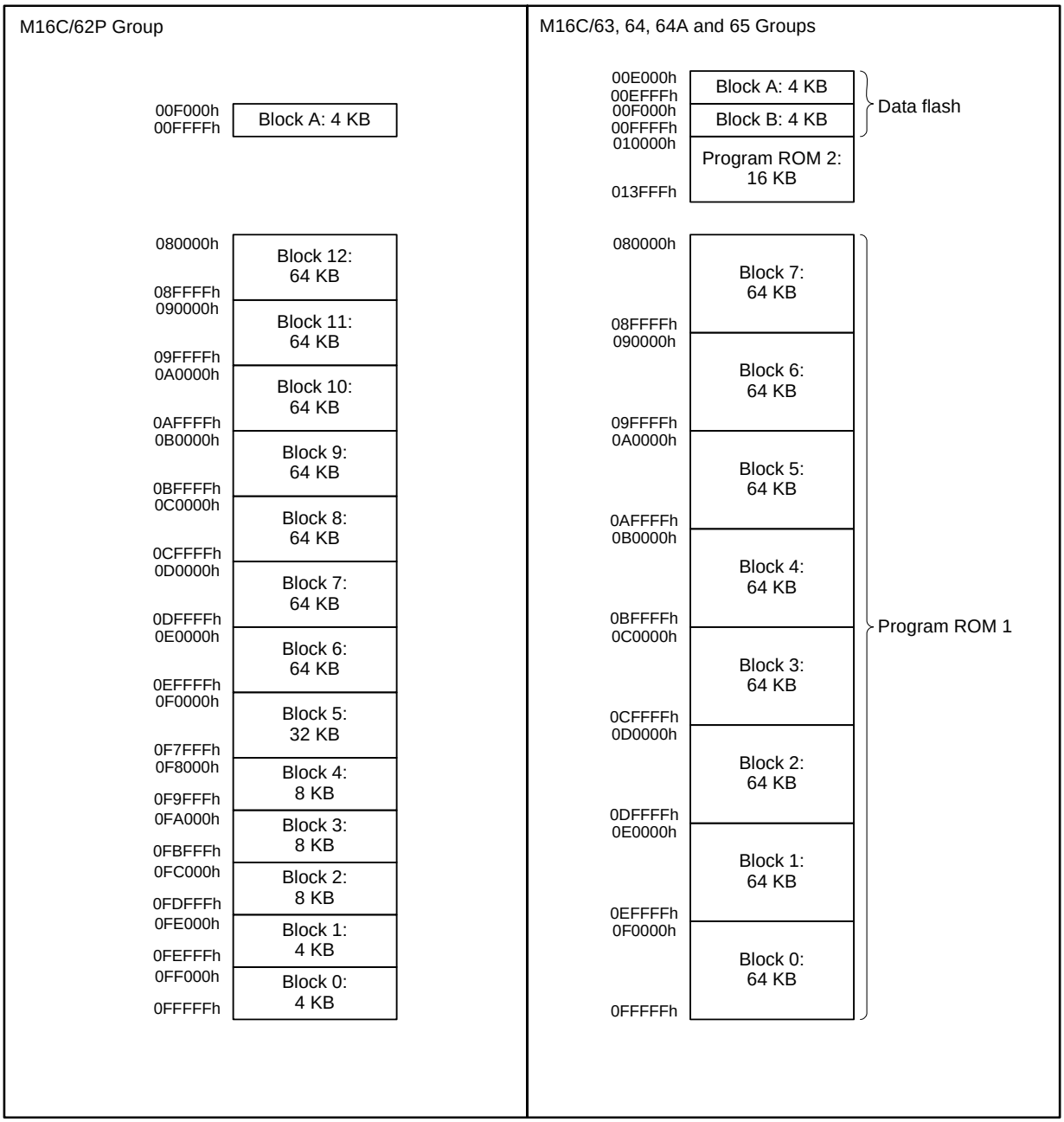

Figure 4.1 Comparison of Memory Maps (512 KB Version)

4.3 Setting and Resetting of CPU Rewrite Mode (EW0, EW1 Mode)

Figure 4.2 shows the Comparison of Setting and Resetting of CPU Rewrite Mode (EW0 Mode).
Figure 4.3 shows the Comparison of Setting and Resetting of CPU Rewrite Mode (EW1 Mode).

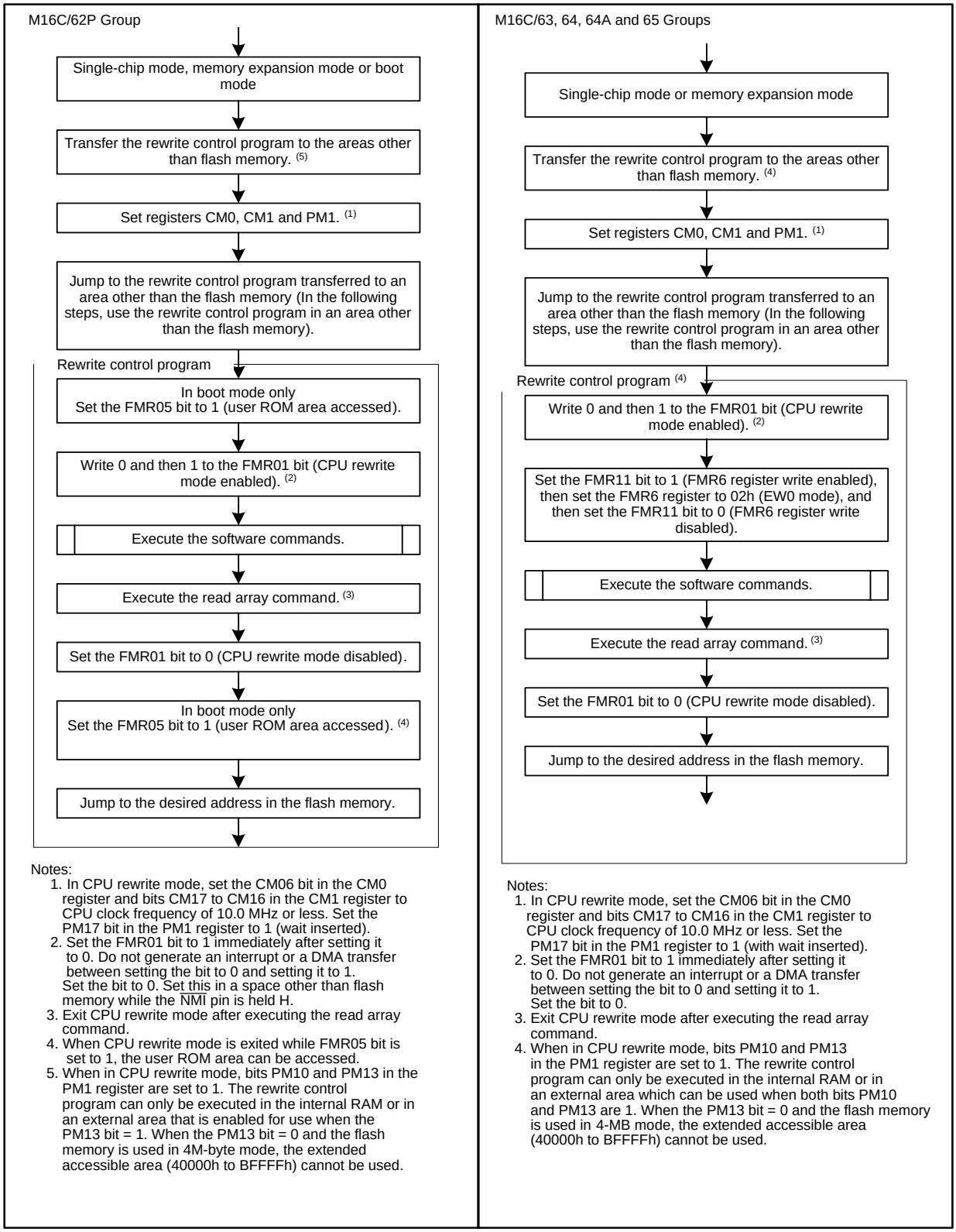

Figure 4.2 Comparison of Setting and Resetting of CPU Rewrite Mode (EW0 Mode)

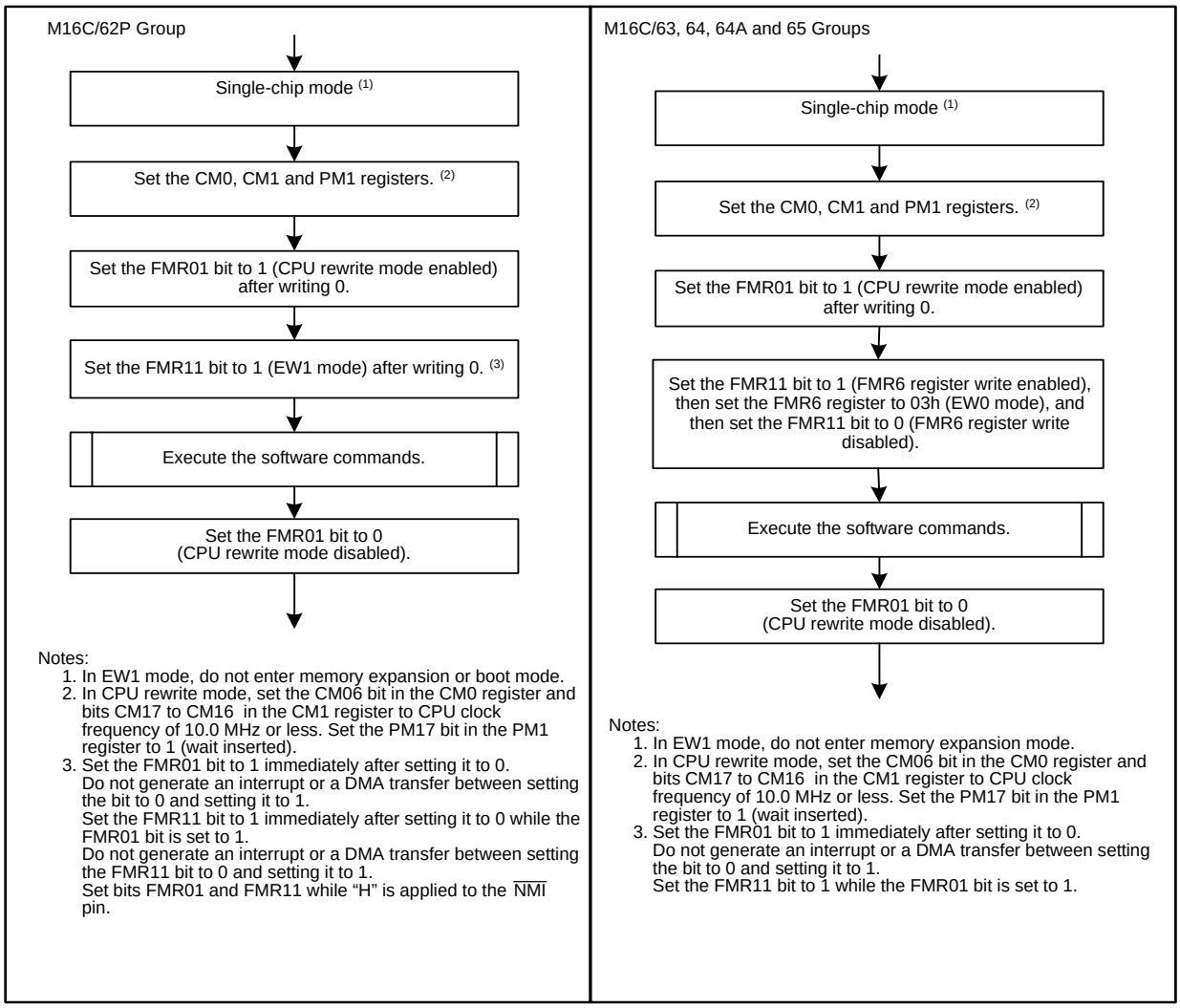

Figure 4.3 Comparison of Setting and Resetting of CPU Rewrite Mode (EW1 Mode)

4.4 Operation Example

Table 4.3 lists the differences in the software commands.

Table 4.3 Differences in Software Commands

Software Command	MCU	The First Bus Cycle		The Second Bus Cycle		The Third Bus Cycle	
		Address	Data	Address	Data	Address	Data
Read array	M16C/62P	x	xxFFh	-	-	-	-
	M16C/63, 64, 64A, 65 (1)	x	xxFFh	-	-	-	-
	M16C/65 (2)	B0-7	xxFFh	B8	xxFFh	-	-
Read status register	M16C/62P	x	xx70h	x	SRD	-	-
	M16C/63, 64, 64A, 65 (1)	x	xx70h	x	SRD	-	-
	M16C/65 (2)	BA	xx70h	x	SRD	-	-
Clear status register	M16C/62P	x	xx50h	-	-	-	-
	M16C/63, 64, 64A, 65 (1)	x	xx50h	-	-	-	-
	M16C/65 (2)	B0-7	xx50h	B8	xx50	-	-
Program	M16C/62P	WA	xx40h	WA	WD	-	-
	M16C/63, 64, 64A, 65 (1)	WA	xx41h	WA	WD0	WA	WD1
	M16C/65 (2)	WA	xx41h	WA	WD0	WA	WD1
Block erase	M16C/62P	x	xx20h	BA	xxD0h	-	-
	M16C/63, 64, 64A, 65 (1)	x	xx20h	BA	xxD0h	-	-
	M16C/65 (2)	BA	xx20h	BA	xxD0h	-	-
Erase all unlocked block	M16C/62P	x	xxA7h	x	xxD0h	-	-
	M16C/63, 64, 64A, 65 (1)	-	-	-	-	-	-
	M16C/65 (2)	-	-	-	-	-	-
Read lock bit status	M16C/62P	x	xx71h	BA	xxD0h	-	-
	M16C/63, 64, 64A, 65 (1)	x	xx71h	BA	xxD0h	-	-
	M16C/65 (2)	BA	xx71h	BA	xxD0h	-	-
Block blank check	M16C/62P	-	-	-	-	-	-
	M16C/63, 64, 64A, 65 (1)	x	xx25h	BA	xxD0h	-	-
	M16C/65 (2)	BA	xx25h	BA	xxD0h	-	-

Notes:
1. In the M16C/65 Group, only in products with program ROM 1 that is 512 KB or less.
2. In the M16C/65 Group, only in products with program ROM 1 over 512 KB.

SRD: Status register data (D7 to D0)
WA: Write address (Even address. Set the end of the address to 0h, 4h, 8h, or Ch in the M16C/63, 64, 64A and 65 Groups).
WD: Write data (16 bits).
WD0: Write data low-order word (16 bits).
WD1: Write data high-order word (16 bits).
BA: Highest-order block address (even address)
B0-7: Any even address in blocks 0 to 7, program ROM 2, or data flash
B8: Any even address in blocks after 8.
x: Any even address in user ROM area
xx: Eight high-order bits of command code (ignored)

4.5 Program

The program differs between the M16C/62P Group and the M16C/63, 64, 64A and 65 Groups.
Table 4.4 lists the differences in the programs.

Table 4.4 Differences in programs

Item	M16C/62P Group	M16C/63, M16C/64, M16C/64A and M16C/65 Groups
Write unit	In 1-word (2-byte) units	In 2-word (4-byte) units
Command code	xx40h	xx41h

4.6 User Boot Function

In the M16C/63, 64, 64A and 65 Groups, user boot functions is added to select boot mode and user boot mode by the status of a port. Refer to each device's hardware manual for details on the boot function.

4.7 Suspend Function

The M16C/63 Group includes a suspend function for suspending automatic programming and erasure.
Refer to the M16C/63 Group hardware manual for details.

5. Reference Documents

Hardware Manuals
M16C/62P Group Hardware Manual
M16C/63 Group Hardware Manual
M16C/64 Group Hardware Manual
M16C/64A Group Hardware Manual
M16C/65 Group Hardware Manual
The latest versions can be downloaded from the Renesas Technology website.

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