RX72T Group, RX66T Group

Differences Between the RX72T Group and the RX66T Group

Introduction

This application note is a reference document that lists differences in peripheral modules, I/O registers, and pin functions between the RX72T Group and the RX66T Group.

This document also provides important information that needs to be taken into account when replacing the MCU. Unless otherwise indicated the maximum MCU specifications of RX72T Group products with 144 pins (with programmable gain amplifier (PGA) pseudo-differential input and USB pins) and RX66T Group products with 144 pins (with programmable gain amplifier (PGA) pseudo-differential input and USB pins) are described. Refer to the User's Manual: Hardware of each MCU for details of differences in electrical characteristics, usage notes, and setting procedures.

Target Devices

RX72T Group

RX66T Group

Contents

1. Comparison of Built-In Functions of RX72T Group and RX66T Group

Table 1.1 is a comparative listing of the built-in functions of RX72T Group and RX66T Group.

For details of each function, refer to section 2, Comparative Overview of Specifications, as well as the documents listed in section 5, Reference Documents.

Table 1.1 Comparison of Built-In Functions of RX72T Group and RX66T Group

Function	RX66T	RX72T
CPU	●	
Operating Modes	○	
Address Space	○	
Resets	○	
Option-Setting Memory (OFSM)	○	
Voltage Detection Circuit (LVDA)	○	
Clock Generation Circuit	▲	
Clock Frequency Accuracy Measurement Circuit (CAC)	○	
Low Power Consumption	○	
Register Write Protection Function	○	
Exception Handling	○	
Interrupt Controller (ICUC)	○	
Buses	●	
Memory-Protection Unit (MPU)	○	
DMA Controller (DMACAa)	○	
Data Transfer Controller (DTCa)	○	
Event Link Controller (ELC)	○	
I/O Ports	○	
Multi-Function Pin Controller (MPC)	▲	
Multi-Function Timer Pulse Unit 3 (MTU3d)	○	
Port Output Enable 3 (POE3B)	○	
General PWM Timer (GPTW)	○	
High Resolution PWM Waveform Generation Circuit (HRPWM)	●	
GPTW Port Output Enable (POEG)	○	
8-Bit Timer (TMR)	○	
Compare Match Timer (CMT)	○	
Watchdog Timer (WDTA)	○	
Independent Watchdog Timer (IWDTa)	○	
USB 2.0 FS Host/Function Module (USBb)	○	
Serial Communications Interface (SCIj, SCIi, SCIh)	○	
I^2C-bus Interface (RIICa)	○	
CAN Module (CAN)	○	
Serial Peripheral Interface (RSPIc)	○	
CRC Calculator (CRCA)	○	
Arithmetic Unit for Trigonometric Functions (TFU)	×	○
Trusted Secure IP (TSIP-Lite)	○	
12-Bit A/D Converter (S12ADH)	○	
12-Bit D/A Converter (R12DAb)	○	
Temperature Sensor (TEMPS)	○	
Comparator C (CMPC)	○	
Data Operation Circuit (DOC)	○	
RAM	▲	

Function	RX66T	RX72T
Flash Memory (Code Flash Memory, Data Flash Memory)	▲	
Package	■	

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Differences in register specifications are not listed.

2.1 CPU

Table 2.1 is a comparative listing of CPU specifications.

Table 2.1 Comparison of CPU Specifications

Item	RX66T	RX72T
CPU	• Maximum operating frequency: 160 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per state (system clock cycle) • Address space: 4-GB linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit register • Basic instructions: 77 • Single-precision floating point instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32/32 → 32 bits • Barrel shifter: 32 bits	• Maximum operating frequency: 200 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per state (system clock cycle) • Address space: 4-GB linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • Basic instructions: 77 • Single-precision floating point instructions: 11 • DSP instructions: 23 • Instructions for register bank save function: 2 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32/32 → 32 bits • Barrel shifter: 32 bits
FPU	• Single-precision floating point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard	• Single-precision floating point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard
Register bank save function	—	• Fast collective saving and restoration of the values of CPU registers • 16 save register banks

2.2 Clock Generation Circuit

Table 2.2 is a comparative listing of clock generation circuit specifications.

Table 2.2 Comparison of Clock Generation Circuit Specifications

Item	RX66T	RX72T
Use	• Generates the system clock (ICLK) supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) supplied to the RSPI, SCIi, MTU3 (internal peripheral buses), GPTW (internal peripheral buses), and HRPWM (internal peripheral buses). • Generates the peripheral module clock (PCLKB) supplied to the peripheral modules. • Generates the counter reference clock for the peripheral module supplied to the MTU3 and GPTW and the reference clock (PCLKC) for the HRPWM. • Generates the peripheral module clocks (for analog conversion) (PCLKD) supplied to S12AD. • Generates the FlashIF clock (FCLK) supplied to the FlashIF. • Generates the external bus clock (BCLK) supplied to the external bus. • Generates the USB clock (UCLK) supplied to the USBb. • Generates the CAC clock (CACCLK) supplied to the CAC. • Generates the CAN clock (CANMCLK) supplied to the CAN. • Generates the IWDT-dedicated clock (IWDTCLK) supplied to the IWDT.	• Generates the system clock (ICLK) supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) supplied to the RSPI, SCIi, MTU3 (internal peripheral buses), GPTW (internal peripheral buses), and HRPWM (internal peripheral buses). • Generates the peripheral module clock (PCLKB) supplied to peripheral modules. • Generates the counter reference clock for the peripheral module supplied to the MTU3 and GPTW and the reference clock (PCLKC) for the HRPWM. • Generates the peripheral module clocks (for analog conversion) (PCLKD) supplied to S12AD. • Generates the FlashIF clock (FCLK) supplied to the FlashIF. • Generates the external bus clock (BCLK) supplied to the external bus. • Generates the USB clock (UCLK) supplied to the USBb. • Generates the CAC clock (CACCLK) supplied to the CAC. • Generates the CAN clock (CANMCLK) supplied to the CAN. • Generates the IWDT-dedicated clock (IWDTCLK) supplied to the IWDT.

Item	RX66T	RX72T
Operating frequency	• ICLK: 160 MHz (max.) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKC: 160 MHz (max.) • PCLKD: 8 MHz to 60 MHz (for conversion with 12-bit A/D converter) • FCLK: — 4 MHz to 60 MHz (for programming and erasing the code flash memory and data flash memory) — 60 MHz (max.) (for reading from the data flash memory) • BCLK: 60 MHz (max.) • BCLK pin output: 40 MHz (max.) • UCLK: 48 MHz (max.) • CACCLK: Same as clocks from respective oscillators. • CANMCLK: 24 MHz (max.) • IWDTCLK: 120 kHz	• ICLK: 200 MHz (max.) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKC: 200 MHz (max.) • PCLKD: 8 MHz to 60 MHz (for conversion with 12-bit A/D converter) • FCLK: — 4 MHz to 60 MHz (for programming and erasing the code flash memory and data flash memory) — 60 MHz (max.) (for reading from the data flash memory) • BCLK: 60 MHz (max.) • BCLK pin output: 40 MHz (max.) • UCLK: 48 MHz (max.) • CACCLK: Same as clocks from respective oscillators. • CANMCLK: 24 MHz (max.) • IWDTCLK: 120 kHz
Main clock oscillator	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop is detected on the main clock, the system clock source is switched to LOCO, and MTU3 and GPTW output can be forcedly driven high-impedance.	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop is detected on the main clock, the system clock source is switched to LOCO, and MTU3 and GPTW output can be forcedly driven high-impedance.
PLL frequency synthesizer	• Input clock source: Main clock, HOCO • Input pulse frequency division ratio: Selectable among 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable from 10 to 30 (in increments of 0.5) • Output clock frequency of the PLL frequency synthesizer: 120 MHz to 240 MHz	• Input clock source: Main clock, HOCO • Input pulse frequency division ratio: Selectable among 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable from 10 to 30 (in increments of 0.5) • Output clock frequency of the PLL frequency synthesizer: 120 MHz to 240 MHz
High-speed on-chip oscillator (HOCO)	• Selectable among 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control	• Selectable among 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 240 kHz	Oscillation frequency: 240 kHz

Item	RX66T	RX72T
IWDT-dedicated on-chip oscillator	Oscillation frequency: 120 kHz	Oscillation frequency: 120 kHz
Control of output on the BCLK pin	• Selectable between BCLK clock output or high output • Selectable between BCLK or BCLK/2	• Selectable between BCLK clock output or high output • Selectable between BCLK or BCLK/2
Event linking (output)	Detection of stopping of the main clock oscillator	Detection of stopping of the main clock oscillator
Event linking (input)	Switching of the clock source to the low-speed on-chip oscillator	Switching of the clock source to the low-speed on-chip oscillator

2.3 Buses

Table 2.3 is a comparative listing of bus specifications.

Table 2.3 Comparison of Bus Specifications

Item		RX66T	RX72T
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Memory bus	Memory bus 1	Connected to RAM	Connected to RAM
	Memory bus 2	Connected to code flash memory	Connected to code flash memory
	Memory bus 3	Connected to ECCRAM	Connected to ECCRAM
Internal main buses	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DMAC and DTC • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the DMAC and DTC • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (TFU, DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 3	• Connected to peripheral modules (USBb and CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (USBb and CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)

Item		RX66T	RX72T
Internal peripheral buses	Internal peripheral bus 4	• Connected to peripheral modules (MTU3, GPTW, HRPWM, RSPI, and SCIi) • Operates in synchronization with the peripheral-module clock (PCLKA)	• Connected to peripheral modules (MTU3, GPTW, HRPWM, RSPI, and SCIi) • Operates in synchronization with the peripheral-module clock (PCLKA)
	Internal peripheral bus 5	Reserved area	Reserved area
	Internal peripheral bus 6	• Connected to code flash (in P/E) and data flash memory • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to code flash (in P/E) and data flash memory • Operates in synchronization with the FlashIF clock (FCLK)
External bus	CS area	• Connected to external devices • Operates in synchronization with the external-bus clock (BCLK: 40 MHz (max.))	• Connected to external devices • Operates in synchronization with the external-bus clock (BCLK: 40 MHz (max.))

2.4 Multi-Function Pin Controller

Table 2.4 is a comparative listing of multi-function pin controller registers.

Table 2.4 Comparison of Multi-Function Pin Controller Registers

Register	Bit	RX66T (MPC)	RX72T (MPC)
PFBCR0	ADRLE	A0 to A7 output enable bits **Products with 64 KB of RAM** 0: PB0, PA2, PF0, PB4 to PB7, and PD0 to PD2 are set as I/O ports. 1: PB0, PA2, PF0, PB4 to PB7, and PD0 to PD2 are set as external address bus A0 to A7. **Products with 128 KB of RAM** 0: PB0, PA2, PF0, PA3 to PA5, PB0 to PB3, PB4 to PB7, and PD0 to PD2 are set as I/O ports. 1: PB0, PA2, PF0, PA3 to PA5, PB0 to PB3, PB4 to PB7, and PD0 to PD2 are set as external address bus A0 to A7.	A0 to A7 output enable bits 0: PB0, PA2, PF0, PA3 to PA5, PB0 to PB3, PB4 to PB7, and PD0 to PD2 are set as I/O ports. 1: PB0, PA2, PF0, PA3 to PA5, PB0 to PB3, PB4 to PB7, and PD0 to PD2 are set as external address bus A0 to A7.
	ADRHMS	A12 to A20 output selection bits **Products with 64 KB of RAM** 0: P65 to P60, P55 to P53 are set as external address bus A12 to A20. 1: Setting prohibited. **Products with 128 KB of RAM** This bit is used in conjunction with the PFBCR4.ADRHMS2 bit to select external address bus pins.	A12 to A20 output selection bits This bit is used in conjunction with the PFBCR4.ADRHMS2 bit to select external address bus pins.

2.5 High Resolution PWM Waveform Generation Circuit

Table 2.5 provides a comparative overview of the high resolution PWM waveform generation circuit, and Table 2.6 is a comparative listing of the registers of the high resolution PWM waveform generation circuit.

Table 2.5 Comparative Overview of High Resolution PWM Waveform Generation Circuit

Item	RX66T (HRPWM)	RX72T (HRPWM)
Function	• High-resolution output of complementary PWM waveforms on up to four channels • High resolution of up to 1/32 a PCLKC period (minimum approx. 195 ps) using delay locked loop (DLL) circuit • Ability to individually adjust timing for rising and falling of PWM waveforms • Ability to directly output waveforms generated by the GPTW, bypassing the HRPWM	• High-resolution output of complementary PWM waveforms on up to four channels • High resolution of up to 1/32 a HRCK period (minimum approx. 195 ps) using delay locked loop (DLL) circuit • Ability to individually adjust timing for rising and falling of PWM waveforms • Ability to directly output waveforms generated by the GPTW, bypassing the HRPWM
Operating clock (PCLKC: RX66T) (HRCK: RX72T)	PCLKC	Selectable between PCLKC and PCLKA
Operating frequency (f(PCLKC): RX66T) (f(HRCK): RX72T)	80 to 160 MHz	80 to 160 MHz*1

Note: 1. PCLKC cannot be used if the GPTW operation frequency exceeds 160 MHz. Use PCLKA in this case.

Table 2.6 Comparison of Registers of High Resolution PWM Waveform Generation Circuit

Register	Bit	RX66T (HRPWM)	RX72T (HRPWM)
HRCKSR	—	—	HRPWM operation clock select register

2.6 RAM

Table 2.7 is a comparative listing of RAM specifications.

Table 2.7 Comparison of RAM Specifications

Item	RX66T		RX72T	
	Without ECC Error Correction (RAM)	**With ECC Error Correction (ECCRAM)**	**Without ECC Error Correction (RAM)**	**With ECC Error Correction (ECCRAM)**
Capacity	64 KB 128 KB	16 KB	 128 KB	16 KB
Address	• RAM capacity: 64 KB 0000 0000h to 0000 FFFFh • RAM capacity: 128 KB 0000 0000h to 0001 FFFFh	00FF C000h to 00FF FFFFh	0000 0000h to 0001 FFFFh	00FF C000h to 00FF FFFFh
Memory bus	Memory bus 1	Memory bus 3	Memory bus 1	Memory bus 3
Data retention function	Not available in deep software standby mode		Not available in deep software standby mode	
Low power consumption function	Transition to module stop state can be enabled separately for RAM and ECCRAM.		Transition to module stop state can be enabled separately for RAM and ECCRAM.	
Error checking	• Detection of 1-bit errors • A non-maskable interrupt or interrupt is generated in response to an error.	• ECC error correction: Correction of 1-bit errors and detection of 2-bit errors • A non-maskable interrupt or interrupt is generated in response to an error.	• Detection of 1-bit errors • A non-maskable interrupt or interrupt is generated in response to an error.	• ECC error correction: Correction of 1-bit errors and detection of 2-bit errors • A non-maskable interrupt or interrupt is generated in response to an error.

Item	RX66T		RX72T	
	Without ECC Error Correction (RAM)	**With ECC Error Correction (ECCRAM)**	**Without ECC Error Correction (RAM)**	**With ECC Error Correction (ECCRAM)**
Access	• Single-cycle access is possible for both reading and writing. • RAM can be enabled or disabled.	The ECC function can be enabled or disabled. **When MEMWAIT is set to 0** • The ECC function is disabled: Access takes two cycles for reading or writing. • The ECC function is enabled (when no error has occurred): Access takes two cycles for reading or writing. • The ECC function is enabled (when an error has occurred): Access takes three cycles for reading or writing. **When MEMWAIT is set to 1** • The ECC function is disabled: Access takes three cycles for reading or writing. • The ECC function is enabled (when no error has occurred): Reading takes three cycles and writing takes four cycles. • The ECC function is enabled (when an error has occurred): Access takes five cycles for reading or writing.	• Single-cycle access is possible for both reading and writing. • RAM can be enabled or disabled.	The ECC function can be enabled or disabled. **When MEMWAIT is set to 0** • The ECC function is disabled: Access takes two cycles for reading or writing. • The ECC function is enabled (when no error has occurred): Access takes two cycles for reading or writing. • The ECC function is enabled (when an error has occurred): Access takes three cycles for reading or writing. **When MEMWAIT is set to 1** • The ECC function is disabled: Access takes three cycles for reading or writing. • The ECC function is enabled (when no error has occurred): Reading takes three cycles and writing takes four cycles. • The ECC function is enabled (when an error has occurred): Access takes five cycles for reading or writing.

2.7 Flash Memory

Table 2.8 is a comparative listing of flash memory specifications.

Table 2.8 Comparison of Flash Memory Specifications

Item	RX66T		RX72T	
	Code Flash Memory	**Data Flash Memory**	**Code Flash Memory**	**Data Flash Memory**
Memory capacity	• User area: — 256 KB — 512 KB — 1 MB • User boot area: 32 KB	• Data area: 32 KB	• User area: — 512 KB — 1 MB • User boot area: 32 KB	• Data area: 32 KB
Address	**User area** • Capacity: 256 KB FFFC 0000h to FFFF FFFFh • Capacity: 512 KB FFF8 0000h to FFFF FFFFh • Capacity: 1 MB FFF0 0000h to FFFF FFFFh **User boot area** FF7F 8000h to FF7F FFFFh	0010 0000h to 0010 7FFFh	**User area** • Capacity: 512 KB FFF8 0000h to FFFF FFFFh • Capacity: 1 MB FFF0 0000h to FFFF FFFFh **User boot area** FF7F 8000h to FF7F FFFFh	0010 0000h to 0010 7FFFh
ROM cache	• Capacity: 8 KB • Mapping method: direct mapping • Line size: 16 bytes	—	• Capacity: 8 KB • Mapping method: direct mapping • Line size: 16 bytes	—
Read cycle	• While ROM cache operation is enabled: When the cache is hit, one cycle; when the cache is missed: — One to two cycles if ICLK ≤ 120 MHz — Two to three cycles if ICLK > 120 MHz • When ROM cache operation is disabled: — One cycle if ICLK ≤ 120 MHz — Two cycles if ICLK > 120 MHz	8 cycles of FCLK for 16-bit or 8-bit access	• While ROM cache operation is enabled: When the cache is hit, one cycle; when the cache is missed: — One to two cycles if ICLK ≤ 120 MHz — Two to three cycles if ICLK > 120 MHz • When ROM cache operation is disabled: — One cycle if ICLK ≤ 120 MHz — Two cycles if ICLK > 120 MHz	8 cycles of FCLK for 16-bit or 8-bit access
Value after erasure	FFh	Undefined	FFh	Undefined

Item	RX66T		RX72T	
	Code Flash Memory	**Data Flash Memory**	**Code Flash Memory**	**Data Flash Memory**
Programming/ erasing method	• Programming and erasing the code flash memory/data flash memory are handled using FACI commands specified in the FACI command issuing area (007E 0000h). • Programming/erasure through transfer by a flash-memory programmer via a serial interface (serial programming) • Programming/erasure of flash memory by a user program (self-programming)		• Programming and erasing the code flash memory/data flash memory are handled using FACI commands specified in the FACI command issuing area (007E 0000h). • Programming/erasure through transfer by a flash-memory programmer via a serial interface (serial programming) • Programming/erasure of flash memory by a user program (self-programming)	
Security function	Protects against illicit tampering or reading of data in flash memory		Protects against illicit tampering or reading of data in flash memory	
Protection function	Protects against erroneous rewriting of the flash memory (software protection, error protection, and boot program protection)		Protects against erroneous rewriting of the flash memory (software protection, error protection, and boot program protection)	
Trusted memory (TM) function	Protects against illicit reading of blocks 8 and 9 in the code flash memory		Protects against illicit reading of blocks 8 and 9 in the code flash memory	
Background operation (BGO)	The user area can be read while the data area is being programmed or erased.		The user area can be read while the data area is being programmed or erased.	
Units of programming and erasure	• Unit of programming for the user area or user boot area: 256 bytes • Unit of erasure for the user area: Block	• Unit of programming for the data area: 4 bytes • Unit of erasure for the data area: Block	• Unit of programming for the user area or user boot area: 256 bytes • Unit of erasure for the user area: Block	• Unit of programming for the data area: 4 bytes • Unit of erasure for the data area: Block
Other functions	Interrupts can be accepted during self-programming.		Interrupts can be accepted during self-programming.	
On-board programming (serial programming/ self-programming)	• Programming/erasure in boot mode (for the SCI interface) — The asynchronous serial interface (SCI1) is used. — The transfer rate is adjusted automatically. — The user boot area can also be programmed or erased. • Programming/erasure in boot mode (USB interface) — USBb is used. — Dedicated hardware is not required, so direct connection to a PC is possible. • Programming/erasure in boot mode (FINE interface) — FINE is used. • Programming/erasure in user boot mode — Support for original boot programs created by the user. • Programming/erasure by self-programming — Allows user area/data area programming and erasure without resetting the system.		• Programming/erasure in boot mode (for the SCI interface) — The asynchronous serial interface (SCI1) is used. — The transfer rate is adjusted automatically. — The user boot area can also be programmed or erased. • Programming/erasure in boot mode (USB interface) — USBb is used. — Dedicated hardware is not required, so direct connection to a PC is possible. • Programming/erasure in boot mode (FINE interface) — FINE is used. • Programming/erasure in user boot mode — Support for original boot programs created by the user. • Programming/erasure by self-programming — Allows user area/data area programming and erasure without resetting the system.	

Item	RX66T		RX72T	
	Code Flash Memory	Data Flash Memory	Code Flash Memory	Data Flash Memory
Off-board programming (programming and erasure using parallel programmer)	Programming and erasure of the user area and user boot area by a parallel programmer is possible.	Programming or erasure of the data area by a parallel programmer is not possible.	Programming and erasure of the user area and user boot area by a parallel programmer is possible.	Programming or erasure of the data area by a parallel programmer is not possible.
Unique ID	A 12-byte ID code provided for each MCU		A 12-byte ID code provided for each MCU	

2.8 Package

As indicated in Table 2.9, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage.

Table 2.9 Package

Package Type	RENESAS Code	
	RX66T	RX72T
112-pin LQFP	○	×
80-pin LQFP	○	×
80-pin LFQFP	○	×
64-pin LFQFP	○	×

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

The pin functions of the RX72T Group and RX66T Group (128 KB RAM capacity) are identical for the following packages:

- 144-pin package
- 100-pin package (with PGA pseudo-differential input and USB pin)
- 100-pin package (with PGA pseudo-differential input and without USB pin)
- 100-pin package (without PGA pseudo-differential input and USB pin)

Some pin functions differ between the RX72T Group and RX66T Group (64 KB RAM capacity) on the following package configurations. Items that are not implemented on one of the two groups are shown in **light blue**, and items where the specifications of the two groups do not differ are shown in **black**.

- 100-pin package (with PGA pseudo-differential input and without USB pins)
- 100-pin package (without PGA pseudo-differential input and USB pins)

3.1 100-Pin Package (with PGA Pseudo-Differential Input and without USB pins, RX66T: 64 KB RAM Capacity)

Table 3.1 shows a comparison of pin functions on the 100-pin package product (with PGA pseudo-differential input and without USB pins, RX66T: 64 KB RAM capacity)

Table 3.1 Comparison of Pin Functions on 100-Pin Package (with PGA Pseudo-Differential Input and without USB pins, RX66T: 64 KB RAM Capacity)

100-Pin	RX66T (64 KB RAM Capacity)	RX72T
1	PE5/BCLK/MTIOC9D/MTIOC9D#/GTIOC3A/ GTETRGB/GTIOC3A#/GTETRGD/SCK9/ CTS9#/RTS9#/SS9#/IRQ0/ADST0	PE5/BCLK/MTIOC9D/MTIOC9D#/GTIOC3A/ GTETRGB/GTIOC3A#/GTETRGD/SCK9/ CTS9#/RTS9#/SS9#/IRQ0/ADST0
2	EMLE	EMLE
3	VSS	VSS
4	UB/P00/A11/MTIOC9A/MTIOC9A#/CACREF/ RXD9/SMISO9/SSCL9/RXD12/SMISO12/ SSCL12/RXDX12/IRQ2/ADST1/COMP0	UB/P00/A11/MTIOC9A/MTIOC9A#/CACREF/ RXD9/SMISO9/SSCL9/RXD12/SMISO12/ SSCL12/RXDX12/IRQ2/ADST1/COMP0
5	VCL	VCL
6	MD/FINED	MD/FINED
7	P01/A10/MTIOC9C/MTIOC9C#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE12#/ TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/IRQ4/ADST2/ COMP1	P01/A10/MTIOC9C/MTIOC9C#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE12#/ TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/IRQ4/ADST2/ COMP1
8	PE4/A9/MTCLKC/MTCLKC#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE10#/ SCK9/IRQ1	PE4/A9/MTCLKC/MTCLKC#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE10#/ SCK9/IRQ1
9	PE3/A8/MTCLKD/MTCLKD#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE11#/ CTS9#/RTS9#/SS9#/IRQ2-DS	PE3/A8/MTCLKD/MTCLKD#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE11#/ CTS9#/RTS9#/SS9#/IRQ2-DS
10	RES#	RES#
11	XTAL/P37	XTAL/P37
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36
14	VCC	VCC
15	PE2/POE10#/NMI	PE2/POE10#/NMI
16	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/ TMO5/CTS5#/RTS5#/SS5#/CTS12#/ RTS12#/SS12#/SSLA3/IRQ15	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/ TMO5/CTS5#/RTS5#/SS5#/CTS12#/ RTS12#/SS12#/SSLA3/IRQ15

100-Pin	RX66T (64 KB RAM Capacity)	RX72T
17	PE0/WR1#/BC1#/WAIT#/MTIOC9B/ MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/ SSCL5/SSLA2/CRX0/IRQ7	PE0/WR1#/BC1#/WAIT#/MTIOC9B/ MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/ SSCL5/SSLA2/CRX0/IRQ7
18	TRST#/PD7/MTIOC9A/MTIOC9A#/ GTIOC0A/GTIOC3A/GTIOC0A#/ GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/ SSDA5/SSLA1/CTX0/IRQ8	TRST#/PD7/MTIOC9A/MTIOC9A#/ GTIOC0A/GTIOC3A/GTIOC0A#/ GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/ SSDA5/SSLA1/CTX0/IRQ8
19	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/ GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/ CTS1#/RTS1#/SS1#/CTS11#/RTS11#/ SS11#/SSLA0/IRQ5/ADST0	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/ GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/ CTS1#/RTS1#/SS1#/CTS11#/RTS11#/ SS11#/SSLA0/IRQ5/ADST0
20	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6
21	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/ TMCI0/TMCI6/SCK1/SCK11/IRQ2	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/ TMCI0/TMCI6/SCK1/SCK11/IRQ2
22	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11
23	TRCLK/PD2/A7/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/TMCI1/TMO4/ SCK5/SCK8/MOSIA	TRCLK/PD2/A7/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/TMCI1/TMO4/ SCK5/SCK8/MOSIA
24	TRDATA3/PD1/A6/GTIOC3A/GTIOC0B/ GTIOC3A#/GTIOC0B#/TMO2/RXD8/ SMISO8/SSCL8/MISOA	TRDATA3/PD1/A6/GTIOC3A/GTIOC0B/ GTIOC3A#/GTIOC0B#/TMO2/RXD8/ SMISO8/SSCL8/MISOA
25	TRDATA2/PD0/A5/GTIOC3B/GTIOC1A/ GTIOC3B#/GTIOC1A#/TMO6/TXD8/ SMOSI8/SSDA8/RSPCKA	TRDATA2/PD0/A5/GTIOC3B/GTIOC1A/ GTIOC3B#/GTIOC1A#/TMO6/TXD8/ SMOSI8/SSDA8/RSPCKA
26	TRDATA1/PB7/A4/GTIOC1B/GTIOC1B#/ SCK5/SCK11/SCK12	TRDATA1/PB7/A4/GTIOC1B/GTIOC1B#/ SCK5/SCK11/SCK12
27	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/ RXD5/SMISO5/SSCL5/RXD11/SMISO11/ SSCL11/RXD12/SMISO12/SSCL12/ RXDX12/CRX0/IRQ2	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/ RXD5/SMISO5/SSCL5/RXD11/SMISO11/ SSCL11/RXD12/SMISO12/SSCL12/ RXDX12/CRX0/IRQ2
28	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/ TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/ SSDA11/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/ TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/ SSDA11/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0
29	VCC	VCC
30	PB4/A1/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/IRQ3-DS	PB4/A1/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/IRQ3-DS
31	VSS	VSS
32	PB3/MTIOC0A/MTIOC0A#/CACREF/ SCK6/RSPCKA/IRQ9	PB3/A7/MTIOC0A/MTIOC0A#/CACREF/ SCK6/RSPCKA/IRQ9
33	PB2/MTIOC0B/MTIOC0B#/GTADSM0/ TMRI0/TXD6/SMOSI6/SSDA6/SDA/ADSM0	PB2/A6/MTIOC0B/MTIOC0B#/GTADSM0/ TMRI0/TXD6/SMOSI6/SSDA6/SDA/ADSM0
34	PB1/MTIOC0C/MTIOC0C#/GTADSM1/ TMCI0/RXD6/SMISO6/SSCL6/SCL/IRQ4/ ADSM1	PB1/A5/MTIOC0C/MTIOC0C#/GTADSM1/ TMCI0/RXD6/SMISO6/SSCL6/SCL/IRQ4/ ADSM1
35	PB0/A0/BC0#/MTIOC0D/MTIOC0D#/ TMO0/TXD6/SMOSI6/SSDA6/CTS11#/ RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#	PB0/A0/A4/BC0#/MTIOC0D/MTIOC0D#/ TMO0/TXD6/SMOSI6/SSDA6/CTS11#/ RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
36	PA5/MTIOC1A/MTIOC1A#/TMCI3/ RXD6/SMISO6/SSCL6/RXD8/SMISO8/ SSCL8/MISOA/IRQ1/ADTRG1#	PA5/A3/MTIOC1A/MTIOC1A#/TMCI3/ RXD6/SMISO6/SSCL6/RXD8/SMISO8/ SSCL8/MISOA/IRQ1/ADTRG1#

100-Pin	RX66T (64 KB RAM Capacity)	RX72T
37	PA4/MTIOC1B/MTIOC1B#/TMCI7/ SCK6/TXD8/SMOSI8/SSDA8/RSPCKA/ ADTRG0#	PA4/A2/MTIOC1B/MTIOC1B#/TMCI7/ SCK6/TXD8/SMOSI8/SSDA8/RSPCKA/ ADTRG0#
38	PA3/MTIOC2A/MTIOC2A#/GTADSM0/ TMRI7/TXD9/SMOSI9/SSDA9/SCK8/SSLA0	PA3/A1/MTIOC2A/MTIOC2A#/GTADSM0/ TMRI7/TXD9/SMOSI9/SSDA9/SCK8/SSLA0
39	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/ GTADSM1/TMO7/CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/SSLA1	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/ GTADSM1/TMO7/CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/SCK11/SSLA1
40	PA1/MTIOC6A/MTIOC6A#/TMO4/TXD9/ SMOSI9/SSDA9/RXD11/SMISO11/SSCL11/ SSLA2/CRX0/IRQ14-DS/ADTRG0#	PA1/MTIOC6A/MTIOC6A#/TMO4/TXD9/ SMOSI9/SSDA9/RXD11/SMISO11/SSCL11/ SSLA2/CRX0/IRQ14-DS/ADTRG0#
41	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK9/ TXD11/SMOSI11/SSDA11/SSLA3/CTX0	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK9/ TXD11/SMOSI11/SSDA11/SSLA3/CTX0
42	VCC	VCC
43	P96/CS0#/WAIT#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE4#/CTS8#/ RTS8#/SS8#/IRQ4-DS	P96/CS0#/WAIT#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE4#/CTS8#/ RTS8#/SS8#/IRQ4-DS
44	VSS	VSS
45	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#
46	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#
47	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#
48	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#
49	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#
50	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#
51	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#
52	P75/D1[A1/D1]/MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#	P75/D1[A1/D1]/MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#
53	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#
54	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#
55	P72/D4[A4/D4]/MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#	P72/D4[A4/D4]/MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#
56	P71/D5[A5/D5]/MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#	P71/D5[A5/D5]/MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#
57	P70/D6[A6/D6]/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE0#/CTS9#/ RTS9#/SS9#/IRQ5-DS	P70/D6[A6/D6]/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE0#/CTS9#/ RTS9#/SS9#/IRQ5-DS
58	P33/D7[A7/D7]/MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/GTIOC3B/ GTIOC3B#/TMO0/SSLA3/IRQ13-DS	P33/D7[A7/D7]/MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/GTIOC3B/ GTIOC3B#/TMO0/SSLA3/IRQ13-DS
59	P32/D8[A8/D8]/MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/GTIOC3A/ GTIOC3A#/TMO6/SSLA2/IRQ12-DS	P32/D8[A8/D8]/MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/GTIOC3A/ GTIOC3A#/TMO6/SSLA2/IRQ12-DS
60	VCC	VCC
61	P31/D9[A9/D9]/MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6	P31/D9[A9/D9]/MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6
62	VSS	VSS

100-Pin	RX66T (64 KB RAM Capacity)	RX72T
63	P30/D10[A10/D10]/MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/TMCI6/SCK8/ CTS8#/RTS8#/SS8#/SSLA0/IRQ7/COMP3	P30/D10[A10/D10]/MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/TMCI6/SCK8/ CTS8#/RTS8#/SS8#/SSLA0/IRQ7/COMP3
64	P27/MTIOC1A/MTIOC0C/ MTIOC1A#/MTIOC0C#/POE9#/IRQ15	P27/CS3#/MTIOC1A/MTIOC0C/ MTIOC1A#/MTIOC0C#/POE9#/IRQ15
65	P24/D11[A11/D11]/MTIC5U/MTIC5U#/ TMCI2/TMO6/CTS8#/RTS8#/SS8#/SCK8/ RSPCKA/IRQ4/COMP0	P24/D11[A11/D11]/MTIC5U/MTIC5U#/ TMCI2/TMO6/CTS8#/RTS8#/SS8#/SCK8/ RSPCKA/IRQ4/COMP0
66	P23/D12[A12/D12]/MTIC5V/MTIC5V#/ TMO2/CACREF/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/ SIOX12/MOSIA/CTX0/IRQ11/COMP1	P23/D12[A12/D12]/MTIC5V/MTIC5V#/ TMO2/CACREF/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/ SIOX12/MOSIA/CTX0/IRQ11/COMP1
67	P22/D13[A13/D13]/MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/ TMO4/RXD8/SMISO8/SSCL8/RXD12/ SMISO12/SSCL12/RXDX12/MISOA/CRX0/ IRQ10/ADTRG2#/COMP2	P22/D13[A13/D13]/MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/ TMO4/RXD8/SMISO8/SSCL8/RXD12/ SMISO12/SSCL12/RXDX12/MISOA/CRX0/ IRQ10/ADTRG2#/COMP2
68	P21/D14[A14/D14]/MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/TMCI4/TXD8/ SMOSI8/SSDA8/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/MOSIA/ IRQ6-DS/AN217/ADTRG1#/COMP5	P21/D14[A14/D14]/MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/TMCI4/TXD8/ SMOSI8/SSDA8/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/MOSIA/ IRQ6-DS/AN217/ADTRG1#/COMP5
69	P20/D15[A15/D15]/MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/TMRI4/CTS8#/ RTS8#/SS8#/SCK8/RSPCKA/IRQ7-DS/ AN216/ADTRG0#/COMP4	P20/D15[A15/D15]/MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/TMRI4/CTS8#/ RTS8#/SS8#/SCK8/RSPCKA/IRQ7-DS/ AN216/ADTRG0#/COMP4
70	P65/A12/IRQ9/AN211/CMPC53/DA1	P65/A12/IRQ9/AN211/CMPC53/DA1
71	P64/A13/IRQ8/AN210/CMPC33/DA0	P64/A13/IRQ8/AN210/CMPC33/DA0
72	AVCC2	AVCC2
73	AVSS2	AVSS2
74	P63/A14/IRQ7/AN209/CMPC23	P63/A12/A14/IRQ7/AN209/CMPC23
75	P62/A15/IRQ6/AN208/CMPC43	P62/A13/A15/IRQ6/AN208/CMPC43
76	P61/A16/IRQ5/AN207/CMPC13	P61/A14/A16/IRQ5/AN207/CMPC13
77	P60/A17/IRQ4/AN206/CMPC03	P60/A15/A17/IRQ4/AN206/CMPC03
78	P55/A18/IRQ3/AN203/CMPC32	P55/A16/A18/IRQ3/AN203/CMPC32
79	P54/A19/IRQ2/AN202/CMPC22	P54/A17/A19/IRQ2/AN202/CMPC22
80	P53/A20/IRQ1/AN201/CMPC12	P53/A18/A20/IRQ1/AN201/CMPC12
81	P52/IRQ0/AN200/CMPC02	P52/IRQ0/AN200/CMPC02
82	P47/AN103	P47/AN103
83	P46/AN102/CMPC50/CMPC51	P46/AN102/CMPC50/CMPC51
84	P45/AN101/CMPC40/CMPC41	P45/AN101/CMPC40/CMPC41
85	P44/AN100/CMPC30/CMPC31	P44/AN100/CMPC30/CMPC31
86	PH4/AN107/PGAVSS1	PH4/AN107/PGAVSS1
87	P43/AN003	P43/AN003
88	P42/AN002/CMPC20/CMPC21	P42/AN002/CMPC20/CMPC21
89	P41/AN001/CMPC10/CMPC11	P41/AN001/CMPC10/CMPC11
90	P40/AN000/CMPC00/CMPC01	P40/AN000/CMPC00/CMPC01
91	PH0/AN007/PGAVSS0	PH0/AN007/PGAVSS0
92	AVCC1	AVCC1
93	AVCC0	AVCC0
94	AVSS0	AVSS0
95	AVSS1	AVSS1
96	P82/ALE/WAIT#/MTIC5U/MTIC5U#/ TMO4/SCK6/SCK12/IRQ3/COMP5	P82/ALE/WAIT#/MTIC5U/MTIC5U#/ TMO4/SCK6/SCK12/IRQ3/COMP5

100-Pin	RX66T (64 KB RAM Capacity)	RX72T
97	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/ TXD6/SMOSI6/SSDA6/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/COMP4	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/ TXD6/SMOSI6/SSDA6/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/COMP4
98	P80/CS1#/MTIC5W/MTIC5W#/TMRI4/ RXD6/SMISO6/SSCL6/RXD12/SMISO12/ SSCL12/RXDX12/IRQ5/COMP3	P80/CS1#/MTIC5W/MTIC5W#/TMRI4/ RXD6/SMISO6/SSCL6/RXD12/SMISO12/ SSCL12/RXDX12/IRQ5/COMP3
99	P11/RD#/MTIOC3A/MTCLKC/ MTIOC3A#/MTCLKC#/MTIOC9D/ GTIOC3B/GTETRGA/GTIOC3B#/ GTETRGC/TMO3/POE9#/IRQ1-DS	P11/RD#/MTIOC3A/MTCLKC/ MTIOC3A#/MTCLKC#/MTIOC9D/ GTIOC3B/GTETRGA/GTIOC3B#/ GTETRGC/TMO3/POE9#/IRQ1-DS
100	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0-DS	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0-DS

3.2 100-Pin Package (without PGA Pseudo-Differential Input and USB pins, RX66T: 64 KB RAM Capacity)

Table 3.2 shows a comparison of pin functions on the 100-pin package product (without PGA pseudo-differential input and USB pins, RX66T: 64 KB RAM capacity)

Table 3.2 Comparison of Pin Functions on 100-Pin Package (without PGA Pseudo-Differential Input and USB pins, RX66T: 64 KB RAM Capacity)

100-Pin	RX66T (64 KB RAM Capacity)	RX72T
1	PE5/BCLK/MTIOC9D/MTIOC9D#/GTIOC3A/ GTETRGB/GTIOC3A#/GTETRGD/SCK9/ CTS9#/RTS9#/SS9#/IRQ0/ADST0	PE5/BCLK/MTIOC9D/MTIOC9D#/GTIOC3A/ GTETRGB/GTIOC3A#/GTETRGD/SCK9/ CTS9#/RTS9#/SS9#/IRQ0/ADST0
2	EMLE	EMLE
3	VSS	VSS
4	UB/P00/A11/MTIOC9A/MTIOC9A#/CACREF/ RXD9/SMISO9/SSCL9/RXD12/SMISO12/ SSCL12/RXDX12/IRQ2/ADST1/COMP0	UB/P00/A11/MTIOC9A/MTIOC9A#/CACREF/ RXD9/SMISO9/SSCL9/RXD12/SMISO12/ SSCL12/RXDX12/IRQ2/ADST1/COMP0
5	VCL	VCL
6	MD/FINED	MD/FINED
7	P01/A10/MTIOC9C/MTIOC9C#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE12#/ TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/IRQ4/ADST2/ COMP1	P01/A10/MTIOC9C/MTIOC9C#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE12#/ TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/IRQ4/ADST2/ COMP1
8	PE4/A9/MTCLKC/MTCLKC#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE10#/ SCK9/IRQ1	PE4/A9/MTCLKC/MTCLKC#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE10#/ SCK9/IRQ1
9	PE3/A8/MTCLKD/MTCLKD#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE11#/ CTS9#/RTS9#/SS9#/IRQ2_DS	PE3/A8/MTCLKD/MTCLKD#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE11#/ CTS9#/RTS9#/SS9#/IRQ2_DS
10	RES#	RES#
11	XTAL/P37	XTAL/P37
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36
14	VCC	VCC
15	PE2/POE10#/NMI	PE2/POE10#/NMI
16	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/ TMO5/CTS5#/RTS5#/SS5#/CTS12#/ RTS12#/SS12#/SSLA3/IRQ15	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/ TMO5/CTS5#/RTS5#/SS5#/CTS12#/ RTS12#/SS12#/SSLA3/IRQ15
17	PE0/WR1#/BC1#/WAIT#/MTIOC9B/ MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/ SSCL5/SSLA2/CRX0/IRQ7	PE0/WR1#/BC1#/WAIT#/MTIOC9B/ MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/ SSCL5/SSLA2/CRX0/IRQ7
18	TRST#/PD7/MTIOC9A/MTIOC9A#/ GTIOC0A/GTIOC3A/GTIOC0A#/ GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/ SSDA5/SSLA1/CTX0/IRQ8	TRST#/PD7/MTIOC9A/MTIOC9A#/ GTIOC0A/GTIOC3A/GTIOC0A#/ GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/ SSDA5/SSLA1/CTX0/IRQ8
19	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/ GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/ CTS1#/RTS1#/SS1#/CTS11#/RTS11#/ SS11#/SSLA0/IRQ5/ADST0	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/ GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/ CTS1#/RTS1#/SS1#/CTS11#/RTS11#/ SS11#/SSLA0/IRQ5/ADST0
20	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6
21	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/ TMCI0/TMCI6/SCK1/SCK11/IRQ2	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/ TMCI0/TMCI6/SCK1/SCK11/IRQ2

100-Pin	RX66T (64 KB RAM Capacity)	RX72T
22	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11
23	TRCLK/PD2/A7/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/TMCI1/TMO4/ SCK5/SCK8/MOSIA	TRCLK/PD2/A7/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/TMCI1/TMO4/ SCK5/SCK8/MOSIA
24	TRDATA3/PD1/A6/GTIOC3A/GTIOC0B/ GTIOC3A#/GTIOC0B#/TMO2/RXD8/ SMISO8/SSCL8/MISOA	TRDATA3/PD1/A6/GTIOC3A/GTIOC0B/ GTIOC3A#/GTIOC0B#/TMO2/RXD8/ SMISO8/SSCL8/MISOA
25	TRDATA2/PD0/A5/GTIOC3B/GTIOC1A/ GTIOC3B#/GTIOC1A#/TMO6/TXD8/ SMOSI8/SSDA8/RSPCKA	TRDATA2/PD0/A5/GTIOC3B/GTIOC1A/ GTIOC3B#/GTIOC1A#/TMO6/TXD8/ SMOSI8/SSDA8/RSPCKA
26	TRDATA1/PB7/A4/GTIOC1B/GTIOC1B#/ SCK5/SCK11/SCK12	TRDATA1/PB7/A4/GTIOC1B/GTIOC1B#/ SCK5/SCK11/SCK12
27	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/ RXD5/SMISO5/SSCL5/RXD11/SMISO11/ SSCL11/RXD12/SMISO12/SSCL12/ RXDX12/CRX0/IRQ2	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/ RXD5/SMISO5/SSCL5/RXD11/SMISO11/ SSCL11/RXD12/SMISO12/SSCL12/ RXDX12/CRX0/IRQ2
28	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/ TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/ SSDA11/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/ TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/ SSDA11/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0
29	VCC	VCC
30	PB4/A1/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/IRQ3_DS	PB4/A1/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/IRQ3_DS
31	VSS	VSS
32	PB3/MTIOC0A/MTIOC0A#/CACREF/ SCK6/ RSPCKA/IRQ9	PB3/A7/MTIOC0A/MTIOC0A#/CACREF/ SCK6/ RSPCKA/IRQ9
33	PB2/MTIOC0B/MTIOC0B#/GTADSM0/ TMRI0/TXD6/SMOSI6/SSDA6/SDA/ADSM0	PB2/A6/MTIOC0B/MTIOC0B#/GTADSM0/ TMRI0/TXD6/SMOSI6/SSDA6/SDA/ADSM0
34	PB1/MTIOC0C/MTIOC0C#/GTADSM1/ TMCI0/RXD6/SMISO6/SSCL6/SCL/IRQ4/ ADSM1	PB1/A5/MTIOC0C/MTIOC0C#/GTADSM1/ TMCI0/RXD6/SMISO6/SSCL6/SCL/IRQ4/ ADSM1
35	PB0/A0/BC0#/MTIOC0D/MTIOC0D#/ TMO0/TXD6/SMOSI6/SSDA6/CTS11#/ RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#	PB0/A0/A4/BC0#/MTIOC0D/MTIOC0D#/ TMO0/TXD6/SMOSI6/SSDA6/CTS11#/ RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
36	PA5/MTIOC1A/MTIOC1A#/TMCI3/ RXD6/SMISO6/SSCL6/RXD8/SMISO8/ SSCL8/MISOA/IRQ1/ADTRG1#	PA5/A3/MTIOC1A/MTIOC1A#/TMCI3/ RXD6/SMISO6/SSCL6/RXD8/SMISO8/ SSCL8/MISOA/IRQ1/ADTRG1#
37	PA4/MTIOC1B/MTIOC1B#/TMCI7/ SCK6/TXD8/SMOSI8/SSDA8/RSPCKA/ ADTRG0#	PA4/A2/MTIOC1B/MTIOC1B#/TMCI7/ SCK6/TXD8/SMOSI8/SSDA8/RSPCKA/ ADTRG0#
38	PA3/MTIOC2A/MTIOC2A#/GTADSM0/ TMRI7/TXD9/SMOSI9/SSDA9/SCK8/SSLA0	PA3/A1/MTIOC2A/MTIOC2A#/GTADSM0/ TMRI7/TXD9/SMOSI9/SSDA9/SCK8/SSLA0
39	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/ GTADSM1/TMO7/CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/SSLA1	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/ GTADSM1/TMO7/CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/SCK11/SSLA1
40	PA1/MTIOC6A/MTIOC6A#/TMO4/TXD9/ SMOSI9/SSDA9/RXD11/SMISO11/SSCL11/ SSLA2/CRX0/IRQ14_DS/ADTRG0#	PA1/MTIOC6A/MTIOC6A#/TMO4/TXD9/ SMOSI9/SSDA9/RXD11/SMISO11/SSCL11/ SSLA2/CRX0/IRQ14_DS/ADTRG0#
41	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK9/ TXD11/SMOSI11/SSDA11/SSLA3/CTX0	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK9/ TXD11/SMOSI11/SSDA11/SSLA3/CTX0
42	VCC	VCC

100-Pin	RX66T (64 KB RAM Capacity)	RX72T
43	P96/CS0#/WAIT#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/ POE4#/CTS8#/RTS8#/SS8#/IRQ4_DS	P96/CS0#/WAIT#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/ POE4#/CTS8#/RTS8#/SS8#/IRQ4_DS
44	VSS	VSS
45	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#
46	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#
47	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#
48	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#
49	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#
50	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#
51	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#
52	P75/D1[A1/D1]/MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#	P75/D1[A1/D1]/MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#
53	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#
54	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#
55	P72/D4[A4/D4]/MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#	P72/D4[A4/D4]/MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#
56	P71/D5[A5/D5]/MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#	P71/D5[A5/D5]/MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#
57	P70/D6[A6/D6]/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE0#/CTS9#/ RTS9#/SS9#/IRQ5_DS	P70/D6[A6/D6]/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE0#/CTS9#/ RTS9#/SS9#/IRQ5_DS
58	P33/D7[A7/D7]/MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/GTIOC3B/ GTIOC3B#/TMO0/SSLA3/IRQ13_DS	P33/D7[A7/D7]/MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/GTIOC3B/ GTIOC3B#/TMO0/SSLA3/IRQ13_DS
59	P32/D8[A8/D8]/MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/GTIOC3A/ GTIOC3A#/TMO6/SSLA2/IRQ12_DS	P32/D8[A8/D8]/MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/GTIOC3A/ GTIOC3A#/TMO6/SSLA2/IRQ12_DS
60	VCC	VCC
61	P31/D9[A9/D9]/MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6	P31/D9[A9/D9]/MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6
62	VSS	VSS
63	P30/D10[A10/D10]/MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/TMCI6/SCK8/ CTS8#/RTS8#/SS8#/SSLA0/IRQ7/COMP3	P30/D10[A10/D10]/MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/TMCI6/SCK8/ CTS8#/RTS8#/SS8#/SSLA0/IRQ7/COMP3
64	P24/D11[A11/D11]/MTIC5U/MTIC5U#/ TMCI2/TMO6/CTS8#/RTS8#/SS8#/SCK8/ RSPCKA/IRQ4/COMP0	P24/D11[A11/D11]/MTIC5U/MTIC5U#/ TMCI2/TMO6/CTS8#/RTS8#/SS8#/SCK8/ RSPCKA/IRQ4/COMP0
65	P23/D12[A12/D12]/MTIC5V/MTIC5V#/ TMO2/CACREF/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/ SIOX12/MOSIA/CTX0/IRQ11/COMP1	P23/D12[A12/D12]/MTIC5V/MTIC5V#/ TMO2/CACREF/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/ SIOX12/MOSIA/CTX0/IRQ11/COMP1

100-Pin	RX66T (64 KB RAM Capacity)	RX72T
66	P22/D13[A13/D13]/MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/ TMO4/RXD8/SMISO8/SSCL8/RXD12/ SMISO12/SSCL12/RXDX12/MISOA/CRX0/ IRQ10/ADTRG2#/COMP2	P22/D13[A13/D13]/MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/ TMO4/RXD8/SMISO8/SSCL8/RXD12/ SMISO12/SSCL12/RXDX12/MISOA/CRX0/ IRQ10/ADTRG2#/COMP2
67	P21/D14[A14/D14]/MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/TMCI4/TXD8/ SMOSI8/SSDA8/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/MOSIA/ IRQ6_DS/AN217/ADTRG1#/COMP5	P21/D14[A14/D14]/MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/TMCI4/TXD8/ SMOSI8/SSDA8/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/MOSIA/ IRQ6_DS/AN217/ADTRG1#/COMP5
68	P20/D15[A15/D15]/MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/TMRI4/CTS8#/ RTS8#/SS8#/SCK8/RSPCKA/IRQ7_DS/ AN216/ADTRG0#/COMP4	P20/D15[A15/D15]/MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/TMRI4/CTS8#/ RTS8#/SS8#/SCK8/RSPCKA/IRQ7_DS/ AN216/ADTRG0#/COMP4
69	P65/A12/IRQ9/AN211/CMPC53/DA1	P65/A12/IRQ9/AN211/CMPC53/DA1
70	P64/A13/IRQ8/AN210/CMPC33/DA0	P64/A13/IRQ8/AN210/CMPC33/DA0
71	AVCC2	AVCC2
72	AVCC2	AVCC2
73	AVSS2	AVSS2
74	P63/A14/IRQ7/AN209/CMPC23	P63/A12/A14/IRQ7/AN209/CMPC23
75	P62/A15/IRQ6/AN208/CMPC43	P62/A13/A15/IRQ6/AN208/CMPC43
76	P61/A16/IRQ5/AN207/CMPC13	P61/A14/A16/IRQ5/AN207/CMPC13
77	P60/A17/IRQ4/AN206/CMPC03	P60/A15/A17/IRQ4/AN206/CMPC03
78	P55/A18/IRQ3/AN203/CMPC32	P55/A16/A18/IRQ3/AN203/CMPC32
79	P54/A19/IRQ2/AN202/CMPC22	P54/A17/A19/IRQ2/AN202/CMPC22
80	P53/A20/IRQ1/AN201/CMPC12	P53/A18/A20/IRQ1/AN201/CMPC12
81	P52/IRQ0/AN200/CMPC02	P52/IRQ0/AN200/CMPC02
82	P51/AN205/CMPC52	P51/AN205/CMPC52
83	P50/AN204/CMPC42	P50/AN204/CMPC42
84	P47/AN103	P47/AN103
85	P46/AN102/CMPC50/CMPC51	P46/AN102/CMPC50/CMPC51
86	P45/AN101/CMPC40/CMPC41	P45/AN101/CMPC40/CMPC41
87	P44/AN100/CMPC30/CMPC31	P44/AN100/CMPC30/CMPC31
88	P43/AN003	P43/AN003
89	P42/AN002/CMPC20/CMPC21	P42/AN002/CMPC20/CMPC21
90	P41/AN001/CMPC10/CMPC11	P41/AN001/CMPC10/CMPC11
91	P40/AN000/CMPC00/CMPC01	P40/AN000/CMPC00/CMPC01
92	AVCC1	AVCC1
93	AVCC0	AVCC0
94	AVSS0	AVSS0
95	AVSS1	AVSS1
96	P82/ALE/WAIT#/MTIC5U/MTIC5U#/ TMO4/SCK6/SCK12/IRQ3/COMP5	P82/ALE/WAIT#/MTIC5U/MTIC5U#/ TMO4/SCK6/SCK12/IRQ3/COMP5
97	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/ TXD6/SMOSI6/SSDA6/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/COMP4	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/ TXD6/SMOSI6/SSDA6/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/COMP4
98	P80/CS1#/MTIC5W/MTIC5W#/TMRI4/ RXD6/SMISO6/SSCL6/RXD12/SMISO12/ SSCL12/RXDX12/IRQ5/COMP3	P80/CS1#/MTIC5W/MTIC5W#/TMRI4/ RXD6/SMISO6/SSCL6/RXD12/SMISO12/ SSCL12/RXDX12/IRQ5/COMP3
99	P11/RD#/MTIOC3A/MTCLKC/ MTIOC3A#/MTCLKC#/MTIOC9D/ GTIOC3B/GTETRGA/GTIOC3B#/ GTETRGC/TMO3/POE9#/IRQ1_DS	P11/RD#/MTIOC3A/MTCLKC/ MTIOC3A#/MTCLKC#/MTIOC9D/ GTIOC3B/GTETRGA/GTIOC3B#/ GTETRGC/TMO3/POE9#/IRQ1_DS

100-Pin	RX66T (64 KB RAM Capacity)	RX72T
100	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0_DS	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0_DS

4. Important Information when Migrating Between MCUs

This section presents important information on differences between the RX72T Group and the RX66T Group. 4.1, Notes on Pin Design, presents information regarding the hardware, and 4.2, Notes on Functional Design, presents information regarding the software.

4.1 Notes on Pin Design

4.1.1 Capacitors Connected to Analog Power Supply Pins

If the A/D conversion clock frequency exceeds 40 MHz, add the capacitor listed in Table 4.1 between the 0.1 µF capacitor and the analog power supply pin.

Table 4.1 Comparison of Capacitor Ratings

RX66T		
RAM 64 KB	**RAM 128 KB**	**RX72T**
Add a 1,000 pF capacitor to the 0.1 µF capacitor.	Add a 0.01 µF capacitor to the 0.1 µF capacitor.	Add a 0.01 µF capacitor to the 0.1 µF capacitor.

4.2 Notes on Functional Design

Some software that runs on the RX66T Group is compatible with the RX72T Group. However, careful evaluation is required since specifications such as operating timing and electrical characteristics differ between the groups.

This section presents notes on software regarding the settings of functions that differ between the RX72T Group and the RX66T Group.

For differences in modules and functions, refer to 2, Comparative Overview of Specifications. For further information, refer to the User's Manual: Hardware listed in 5, Reference Documents.

4.2.1 Performing RAM Self-Diagnostics on Save Register Banks

On the RX72T the RAM is configured as save register banks. The save register banks are provided with a buffer, so when a SAVE instruction is used to write data to a register and then a RSTR instruction is used to read data from the same register, the data is actually read from the buffer and not from the RAM memory cells. When performing self-diagnostics on the RAM in a save register bank, use the following sequence of steps for checking the written data in order to prevent the data from being read from the buffer:

1. Use the SAVE instruction to write data to the bank that is the target of the diagnostic test.
2. Use the SAVE instruction to write data to a bank other than that written to in step 1.
3. Use the RSTR instruction to read data from the bank written to in step 1.

4.2.2 Selecting the GPTW Count Clock

When PCLKA is selected as the operation clock for the high resolution PWM waveform generation circuit on the RX72T, select one of the following as the GPTW count clock: PCLKC/2, PCLKC/4, PCLKC/8, PCLKC/16, PCLKC/32, PCLKC/64, PCLKC/256, or PCLKC/1024. PWM waveforms may not be generated as intended if PCLKC/1, GTETRGA, GTETRGB, GTETRGC, or GTETRGD is selected.

5. Reference Documents

User's Manual: Hardware

RX66T Group User's Manual: Hardware, Rev. 1.10 (R01UH0749EJ0110)
(The latest version can be downloaded from the Renesas Electronics website.)

RX72T Group User's Manual: Hardware, Rev. 1.00 (R01UH0803EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Updates/Technical News
(The latest version can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This module reflects the content of the following technical updates:

- TN-RX*-A0213A/E
- TN-RX*-A0218A/E
- TN-RX*-A0219A/E
- TN-RX*-A0227A/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Feb.13, 2019	—	First edition issued
1.10	Feb. 2, 2021	15	Revised 2.7 “Table 2.8 Comparison of Flash Memory Specifications”
		17	Revised 2.8 “Table 2.9 Package”
		18	Revised “3. Comparison of Pin Functions”
			Added “Table 3.1 Comparison of Pin Functions on 100-Pin Package (with PGA Pseudo-Differential Input and without USB pins, RX66T: 64 KB RAM Capacity)”
		23	Added “Table 3.2 Comparison of Pin Functions on 100-Pin Package (without PGA Pseudo-Differential Input and USB pins, RX66T: 64 KB RAM Capacity)”
		29	Revised “5. Reference Documents”
		30	Revised “Related Technical Updates”

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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