RX66T Group, RX62T/RX62G Group

Differences Between the RX66T Group and the RX62T Group

Summary

This application note is intended as a reference to points of difference between the peripheral functions, I/O registers, and pin functions of the RX66T Group and RX62T Group, as well as a guide to key points to consider when migrating between the two groups.

Unless specifically otherwise noted, the information in this application note applies to the 144-pin package version (with programmable gain amplifier (PGA), pseudo-differential input, and USB pins) of the RX66T Group and the 112-pin package version of the RX62T Group as the maximum specifications. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the User's Manual: Hardware of the products in question.

Target Devices

RX66T Group and RX62T Group

Contents

1. Comparison of Built-In Functions of RX66T Group and RX62T Group

A comparison of the built-in functions of the RX66T Group and RX62T Group is provided below. For details of the functions, see section 2, Comparative Overview of Specifications and section 5, Reference Documents.

Table 1.1 is a comparison of built-in functions of RX66T Group and RX62T Group.

Table 1.1 Comparison of Built-In Functions of RX66T Group and RX62T Group

Function	RX62T	RX66T
CPU	●	
Operating modes	●	
Address space	▲	
Resets	●	
Option-setting memory (OFSM)	*1	○
Voltage detection circuit (LVD): RX62T, (LVDA): RX66T	●	
Clock generation circuit	●	
Clock frequency accuracy measurement circuit (CAC)	×	○
Low power consumption	●	
Register write protection function	×	○
Exception handling	▲	
Interrupt controller (ICU): RX62T, (ICUC): RX66T	●	
Buses	●	
Memory-protection unit (MPU)	▲	
DMA controller (DMACAa)	×	○
Data transfer controller (DTC): RX62T, (DTCa): RX66T	●	
Event link controller (ELC)	×	○
I/O ports	●	
Multi-function pin controller (MPC)	*2	○
Multi-function timer pulse unit 3 (MTU3): RX62T, (MTU3d): RX66T	●	
Port output enable 3 (POE3): RX62T, (POE3B): RX66T	●	
General PWM timer (GPT/GPTa): RX62T, (GPTW): RX66T	● *3	
High resolution pwm waveform generation circuit (HRPWM)	*4	○
GPTW port output enable (POEG)	×	○
8-Bit Timer (TMR)	×	○
Compare match timer (CMT)	●	
Watchdog timer (WDT): RX62T, (WDTA): RX66T	●/▲	
Independent watchdog timer (IWDT): RX62T, (IWDTa): RX66T	●	
USB 2.0 FS Host/Function module (USBb)	×	○
Serial communications interface (SCIb): RX62T, (SCIj, SCIi, SCIh): RX66T	●	
I²C-bus interface (RIIC): RX62T, (RIICa): RX66T	●	
CAN module (CAN)	●	
Serial peripheral interface (RSPI): RX62T, (RSPIc): RX66T	●	
CRC calculator (CRC): RX62T, (CRCA): RX66T	●	
Trusted secure IP (TSIP-Lite)	×	○
LIN module (LIN)	○	*5
12-Bit A/D converter (S12ADA): RX62T, (S12ADH): RX66T	●	
10-Bit A/D converter (ADA)	○	×
12-Bit D/A converter (R12DAb)	×	○
Temperature sensor (TEMPS)	×	○
Comparator C (CMPC)	*6	○

Function	RX62T	RX66T
Data operation circuit (DOC)	×	○
RAM	● / ▲	
Flash memory	● / ▲	
Packages	▲ / ■	

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

Notes: 1. Functions of the RX62T Group and RX62G Group listed in the ROM (Flash Memory for Code Storage) section correspond to functions of the RX66T Group listed in the Option-Setting Memory (OFSM) section of the respective User's Manual: Hardware. Refer to section 4, Important Information when Migrating Between MCUs, for details.
2. Functions of the RX62T Group and RX62G Group listed in the I/O Ports section correspond to functions of the RX66T Group listed in the Multi-Function Pin Controller (MPC) section of the respective User's Manual: Hardware. Refer to section 4, Important Information when Migrating Between MCUs, for details.
3. The GPTa is implemented on the RX62G Group only.
4. Functions of the RX62T Group and RX62G Group listed in the General PWM Timer (GPT/GPTa) section correspond to functions of the RX66T Group listed in the High Resolution PWM Waveform Generation Circuit (HRPWM) section of the respective User's Manual: Hardware.
5. Functions of the RX66T Group listed in the Serial Communications Interface (SCIh) section correspond to functions of the RX62T Group and RX62G Group listed in the LIN Module (LIN) section of the respective User's Manual: Hardware.
6. Comparator functions of the RX62T Group and RX62G Group are listed in the 12-Bit A/D Converter (S12ADA) section of RX62T Group, RX62G Group: User's Manual: Hardware.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and black text indicates registers which are included only in one of the MCU groups. Differences in register specifications are not listed.

2.1 CPU

Table 2.1 is a comparative overview of CPUs, and Table 2.2 is a comparison of CPU registers.

Table 2.1 Comparative Overview of CPUs

Item	RX62T	RX66T
CPU	• Maximum operating frequency: 100 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4 GB linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Nine 32-bit registers — Accumulator: One 64-bit register • Basic instructions: 73 • Floating-point instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement — Instructions: Little endian — Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32/32 → 32 bits • Barrel shifter: 32 bits • Memory-protection unit (MPU)	• Maximum operating frequency: 160 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4 GB linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • Basic instructions: 77 • Single precision floating point instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32/32 → 32 bits • Barrel shifter: 32 bits • Memory-protection unit (MPU)
FPU	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard

Table 2.2 Comparison of CPU Registers

Register	Bit	RX62T	RX66T
EXTB	—	—	Exception table register
ACC (RX62T) ACC0, ACC1 (RX66T)	—	Accumulator	Accumulator 0, accumulator 1

2.2 Operating Modes

Table 2.3 is a comparative overview of operating modes, and Table 2.4 is a comparison of operating mode–related registers.

Table 2.3 Comparative Overview of Operating Modes

Item	RX62T	RX66T
Selection of operating modes by mode-setting pins on release from reset state	Single-chip mode	Single-chip mode
	Boot mode	Boot mode (SCI interface)
	—	Boot mode (USB interface)
	—	Boot mode (FINE interface)
	—	User boot mode
Selection of operating modes by register settings	Single-chip mode	Single-chip mode
	—	User boot mode
	—	On-chip ROM disabled extended mode
	—	On-chip ROM enabled extended mode
Selection of endian	MDE pin	MDE register

Table 2.4 Comparison of Operating Mode–Related Registers

Register	Bit	RX62T	RX66T
MDMONR	MD	—	MD Pin Status Flag
	MD0	MD0 status flag	—
	MD1	MD1 status flag	—
	MDE	MDE status flag	—
MDSR	IROM	On-chip ROM startup status flag	—
	BOTS	Boot mode startup flag	—
	UBTS	—	User boot mode startup flag
SYSCR0	EXBE	—	External bus enable
SYSCR1	—	System control register 1	System control register 1
		Initial values after a reset are different.	
	ECCRAME	—	ECCRAM enable
VOLSR	—	—	Voltage level setting register

2.3 Address Space

Figure 2.1 is a comparative memory map of single-chip mode (RX62T: R5F562TAxxxx), Figure 2.2 is a comparative memory map of single-chip mode (RX62T: R5F562T7xxxx), and Figure 2.3 is a comparative memory map of single-chip mode (RX62T: R5F562T6xxxx).

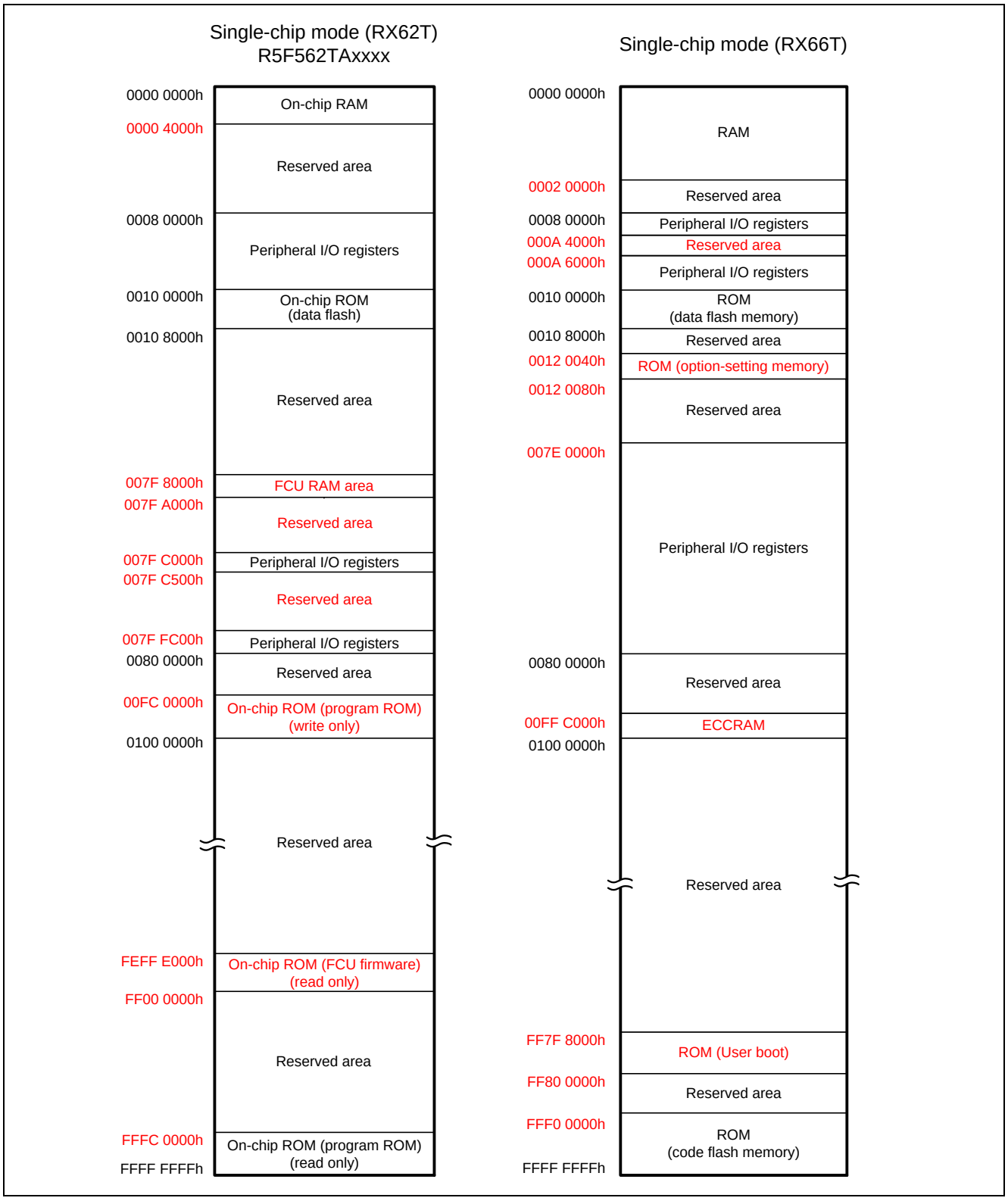


Figure 2.1 Comparative Memory Map of Single-Chip Mode (RX62T: R5F562TAxxxx)

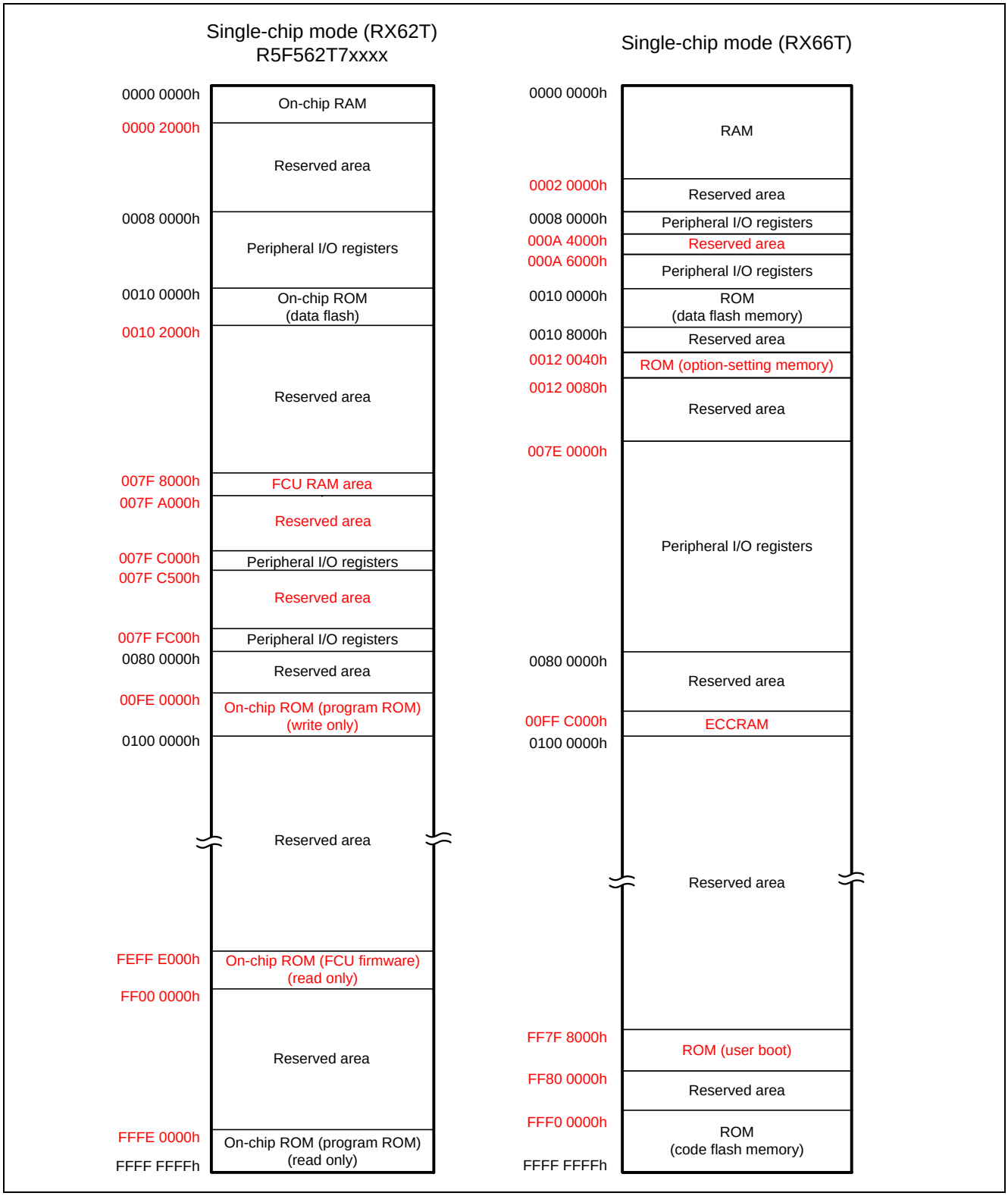


Figure 2.2 Comparative Memory Map of Single-Chip Mode (RX62T: R5F562T7xxxx)

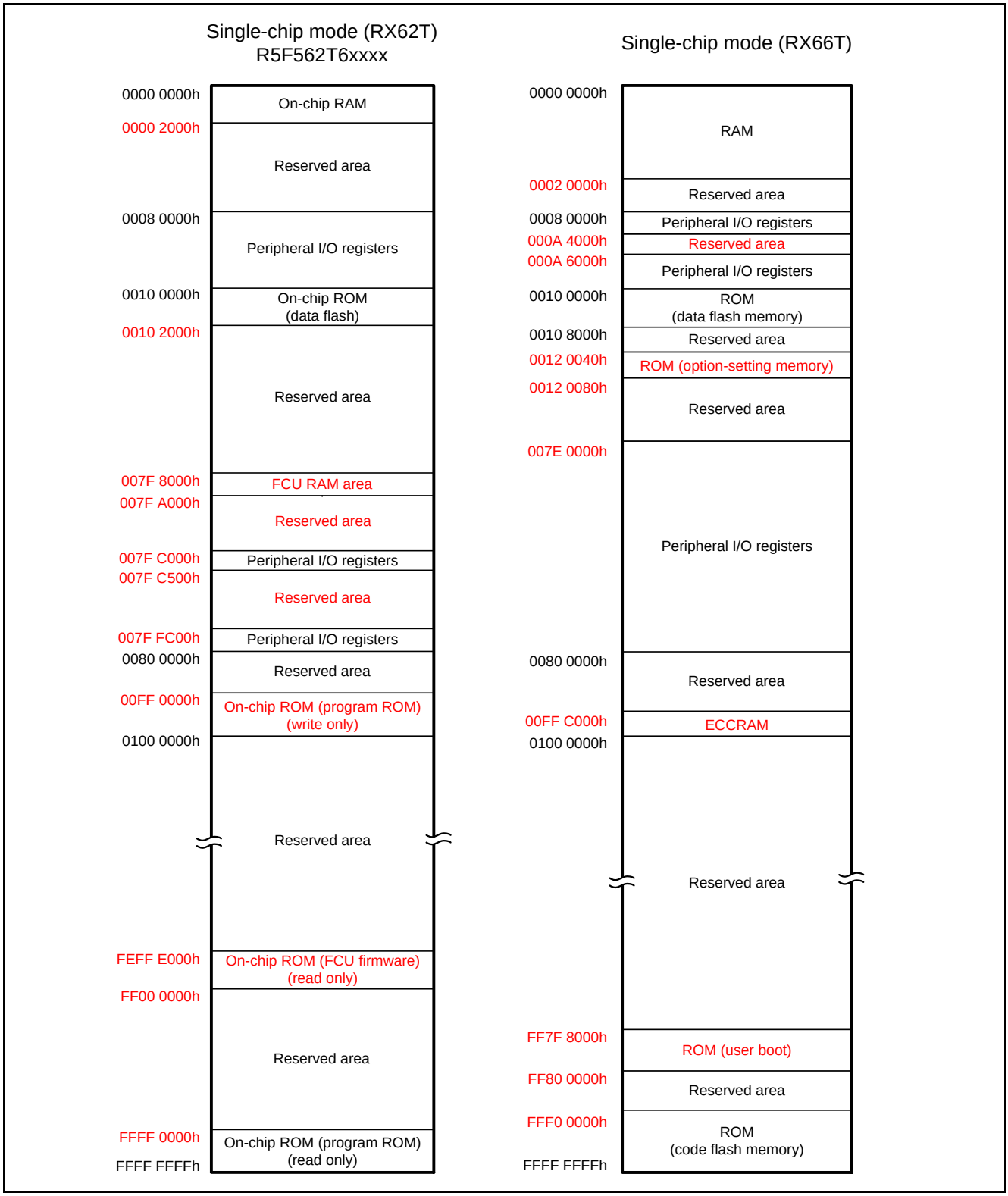


Figure 2.3 Comparative Memory Map of Single-Chip Mode (RX62T: R5F562T6xxxx)

2.4 Resets

Table 2.5 is a comparative overview of resets, and Table 2.6 is a comparison of reset-related registers.

Table 2.5 Comparative Overview of Resets

Item	RX62T	RX66T
RES# pin reset	Generated when the RES# pin is driven low.	Generated when the RES# pin is driven low.
Power-on reset	Generated when VCC rises or VCC falls (monitored voltage: VPOR).	Generated when VCC rises (monitored voltage: VPOR).
Voltage-monitoring 0 reset	—	Generated when VCC falls (monitored voltage: Vdet0).
Voltage-monitoring 1 reset	Generated when VCC falls (monitored voltage: Vdet1).	Generated when VCC falls (monitored voltage: Vdet1).
Voltage-monitoring 2 reset	Generated when VCC falls (monitored voltage: Vdet2).	Generated when VCC falls (monitored voltage: Vdet2).
Deep software standby reset	Generated in response to an interrupt to trigger release from deep software standby.	Generated in response to an interrupt to trigger release from deep software standby.
Independent watchdog timer reset	Generated when the independent watchdog timer underflows.	Generated when the independent watchdog timer underflows, or a refresh error occurs.
Watchdog timer reset	Generated when the independent watchdog timer overflows.	Generated when the watchdog timer underflows, or a refresh error occurs.
Software reset	—	Generated by register setting.

Table 2.6 Comparison of Registers for Resets

Register	Bit	RX62T	RX66T
RSTSR	—	Reset status register	—
RSTSR0	—	—	Reset status register 0
RSTSR1	—	—	Reset status register 1
RSTSR2	—	—	Reset status register 2
RSTCSR	—	Reset control/status register	—
IWDTSR	—	IWDT status register	—
SWRR	—	—	Software reset register

2.5 Voltage Detection Circuit

Table 2.7 is a comparative overview of the voltage detection circuits, and Table 2.8 is a comparison of voltage detection circuit registers.

Table 2.7 Comparative Overview of Voltage Detection Circuits

Item		RX62T (LVD)		RX66T (LVDA)		
		Voltage Monitoring 1	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detected event	Voltage drops past Vdet1	Voltage drops past Vdet2	Voltage drops past Vdet0	Voltage rises or drops past Vdet1	Voltage rises or drops past Vdet2
	Detection voltage	One level only	One level only	Selectable from among two different levels by using OFS1.VDSEL[1:0] bits	Selectable from among five different levels by using LVDLVLR.LVD1LVL[3:0] bits	Selectable from among five different levels by using LVDLVLR.LVD2LVL[3:0] bits
	Monitoring flag	None	None	None	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2
		RSTSR.LVD1F flag: Vdet1 passage detection	RSTSR.LVD2F flag: Vdet2 passage detection	None	LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2DET flag: Vdet2 passage detection
Process upon voltage detection	Reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet1 > VCC: CPU restart after specified time with VCC > Vdet1	Reset when Vdet2 > VCC: CPU restart after specified time with VCC > Vdet2	Reset when Vdet0 > VCC: CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet2 or Vdet2 > VCC
	Interrupt	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	No interrupt	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
		Non-maskable interrupt	Non-maskable interrupt		Non-maskable interrupt or maskable interrupt selectable	Non-maskable interrupt or maskable interrupt selectable
		Interrupt request issued when Vdet1 > VCC	Interrupt request issued when Vdet2 > VCC		Interrupt request issued when Vdet1 > VCC and VCC > Vdet1, or either	Interrupt request issued when Vdet2 > VCC and VCC > Vdet2, or either
Digital filter	Enable/disable switching	Digital filter function not available	Digital filter function not available	Digital filter function not available	Available	Available
	Sampling time	—	—	—	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)
Event linking		None	None	None	Available Output of event signals on detection of Vdet crossings	Available Output of event signals on detection of Vdet crossings

Table 2.8 Comparison of Voltage Detection Circuit Registers

Register	Bit	RX62T (LVD)	RX66T (LVDA)
RSTSR	—	Reset status register	—
LVDKEYR	—	Key code register for low-voltage detection control register	—
LVDCR	—	Low-voltage detection control register	—
LVD1CR1	—	—	Voltage monitoring 1 circuit control register 1
LVD1SR	—	—	Voltage monitoring 1 circuit status register
LVD2CR1	—	—	Voltage monitoring 2 circuit control register 1
LVD2SR	—	—	Voltage monitoring 2 circuit status register
LVCMPCR	—	—	Voltage monitoring circuit control register
LVDLVLR	—	—	Voltage detection level select register
LVD1CR0	—	—	Voltage monitoring 1 circuit control register 0
LVD2CR0	—	—	Voltage monitoring 2 circuit control register 0

2.6 Clock Generation Circuit

Table 2.9 is a comparative overview of the clock generation circuits, and Table 2.10 is a comparison of clock generation circuit registers.

Table 2.9 Comparative Overview of Clock Generation Circuits

Item	RX62T	RX66T
Use	• Generates the system clock (ICLK) to be supplied to the CPU, DTC, MTU3, GPT, ROM, and RAM.	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the RSPI, SCIi, MTU3 (internal peripheral buses), GPTW (internal peripheral buses), and HRPWM (internal peripheral buses).
	• Generates the peripheral module clock (PCLK) to be supplied to peripheral modules.	• Generates the peripheral module clock (PCLKB) to be supplied to peripheral modules. • Generates the counter reference clock for the peripheral module to be supplied to the MTU3 and GPTW, and the reference clock (PCLKC) for the HRPWM. • Generates the peripheral module clocks (for analog conversion) (PCLKD) to be supplied to S12AD. • Generates the flash-IF clock (FCLK) to be supplied to the flash interface. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the USB clock (UCLK) to be supplied to the PHY in the USBb. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CAN clock (CANMCLK) to be supplied to the CAN.
	• Generates the on-chip oscillator clock (IWDTCLK) to be supplied to the IWDT.	• Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.

Item	RX62T	RX66T
Operating frequency	• ICLK: 8 MHz to 100 MHz • PCLK: 8 MHz to 50 MHz • IWDTCLK: 125 kHz (typ.) • Restrictions for setting clock frequencies: ICLK ≥ PCLK	• ICLK: 160 MHz (max.) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKC: 160 MHz (max.) • PCLKD: 8 MHz to 60 MHz (for conversion with 12-bit A/D converter) • FCLK: — 4 MHz to 60 MHz (for programming and erasing the code flash memory and data flash memory) — 60 MHz (max.) (for reading from the data flash memory) • BCLK: 60 MHz (max.) • BCLK pin output: 40 MHz (max.) • UCLK: 48 MHz (max.) • CACCLK: Same as the clock from respective oscillators • CANMCLK: 24 MHz (max.) • IWDTCLK: 120 kHz • Restrictions for setting clock frequencies: ICLK ≥ BCLK, PCLKC ≥ PCLKA ≥ PCLKB
Main clock oscillator	• Resonator frequency: 8 MHz to 12.5 MHz • Connectable resonator or additional circuit: ceramic resonator, crystal resonator • Connection pin: EXTAL, XTAL • Oscillation stop detection function: Switches to internal oscillation upon detection of main clock oscillator stop, Sets the MTU3 and GPT pins to the high-impedance state	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal resonator • Connection pin: EXTAL, XTAL • Oscillation stop detection function: When an oscillation stop is detected with the main clock, the system clock source is switched to LOCO. MTU3 and GPTW output can be forcedly driven to the high-impedance.
PLL frequency synthesizer	• Input clock source: Main clock • Input pulse frequency division ratio: 1 • Input frequency: 8 MHz to 12.5 MHz • Frequency multiplication ratio: 8 • Output clock frequency of the PLL frequency synthesizer: 64 MHz to 100 MHz	• Input clock source: Main clock, HOCO • Input pulse frequency division ratio: Selectable from 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable from 10 to 30 • Output clock frequency of the PLL frequency synthesizer: 120 MHz to 240 MHz
High-speed on-chip oscillator (HOCO)	—	• Selectable from 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control
Low-speed on-chip oscillator (LOCO)	—	Oscillation frequency: 240 kHz

Item	RX62T	RX66T
IWDT-dedicated on-chip oscillator	Oscillation frequency: 125 kHz	Oscillation frequency: 120 kHz
Control of output on the BCLK pin	—	• BCLK clock output or high output is selectable • BCLK or BCLK/2 is selectable
Event linking (output)	—	Detection of stopping of the main clock oscillator
Event linking (input)	—	Switching of the clock source to the low-speed on-chip oscillator

Table 2.10 Comparison of Clock Generation Circuit Registers

Register	Bit	RX62T	RX66T
SCKCR	—	System control register	System control register
		Initial values after a reset are different.	
	PCKD[3:0]	—	Peripheral module clock D (PCLKD) select bits
	PCKC[3:0]	—	Peripheral module clock C (PCLKC) select bits
	PCK[3:0]	Peripheral Module Clock Select bits	—
	PCKB[3:0]	—	Peripheral module clock B (PCLKB) select bits
	PCKA[3:0]	—	Peripheral module clock A (PCLKA) select bits
	BCK[3:0]	—	External bus clock (BCLK) select bits
	PSTOP1	—	BCLK pin output control bit
	ICK[3:0]	System clock select bits b27 b24 0 0 0 0: ×8 0 0 0 1: ×4 0 0 1 0: ×2 0 0 1 1: ×1 Settings other than the above are prohibited.	System clock (ICLK) select bits b27 b24 0 0 0 0: ×1/1 0 0 0 1: ×1/2 0 0 1 0: ×1/4 0 0 1 1: ×1/8 0 1 0 0: ×1/16 0 1 0 1: ×1/32 0 1 1 0: ×1/64 Settings other than the above are prohibited.
	FCK[3:0]	—	Flash-IF clock (FCLK) select bit
MEMWAIT	—	—	Memory wait cycle setting
SCKCR2	—	—	System clock control register 2
SCKCR3	—	—	System clock control register 3
PLLCR	—	—	PLL control register
PLLCR2	—	—	PLL control register 2
BCKCR	—	—	External bus clock control register
MOSCCR	—	—	Main clock oscillator control register
LOCOCR	—	—	Low-speed on-chip oscillator control register
ILOCOCR	—	—	IWDT-dedicated on-chip oscillator control register

Register	Bit	RX62T	RX66T
HOCOCR	—	—	High-speed on-chip oscillator control register
HOCOCR2	—	—	High-speed on-chip oscillator control register 2
OSCOVFSR	—	—	Oscillation stabilization flag register
OSTDCR	OSTDIE	—	Oscillation stop detection interrupt enable bit
	OSTDF	Oscillation stop detection flag	—
	KEY[7:0]	OSTDCR key code	—
OSTDSR	—	—	Oscillation stop detection status register
MOSCWTCR	—	—	Main clock oscillator wait control register
MOFCR	—	—	Main clock oscillator function control register
HOCOPCR	—	—	High-speed on-chip oscillator power supply control register

2.7 Low Power Consumption

Table 2.11 is a comparative overview of low power consumption, Table 2.12 is a comparison of procedures for entering and exiting low power consumption modes and operating states in each mode, and Table 2.13 is a comparison of low power consumption registers.

Table 2.11 Comparative Overview of Low Power Consumption

Item	RX62T	RX66T
Reducing power consumption by switching clock signals	The frequency division ratio is settable independently for the system clock (ICLK) and peripheral module clock (PCLK)	The frequency division ratio is settable independently for the system clock (ICLK), peripheral module clock (PCLKA, PCLKB, PCLKC, PCLKD), external bus clock (BCLK), and flash interface clock (FCLK).
BCLK output control function	—	BCLK output or high-level output can be selected.
Module-stop function	Functions can be stopped independently for each peripheral module.	Functions can be stopped independently for each peripheral module.
Function for transition to low power consumption mode	Transition to low power consumption mode is enabled to stop the CPU, peripheral modules, and oscillator.	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.
Low power consumption function	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode

Table 2.12 Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX62T	RX66T
Sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operating	Operating possible
	High-speed on-chip oscillator	—	Operating possible
	Low-speed on-chip oscillator	—	Operating possible
	IWDT-dedicated on-chip oscillator	Operating	Operating possible
	PLL	Operating	Operating possible
	CPU	Stopped (retained)	Stopped (retained)
	On-chip RAM (0000 0000h to 0000 3FFFh): RX62T RAM and ECCRAM: RX66T	Operating (retained)	Operating possible (retained)
	Flash memory	Operating	Operating
	USB 2.0 Host/Function module (USBb)	—	Operating possible
	Watchdog timer (WDT: RX62T, WDTA: RX66T)	Operating	Stopped (retained)
	Independent watchdog timer (IWDT: RX62T, IWDTa: RX66T)	Operating	Operating possible
	Port output enable (POE3: RX62T, POE3B: RX66T)	Operating possible	Operating possible
	8-bit timer (unit 0, unit 1) (TMR)	—	Operating possible
	Voltage detection circuit (LVDA)	Operating	Operating possible
	Power-on reset circuit	Operating	Operating
	Peripheral modules	Operating	Operating possible
	I/O ports	Operating	Operating
All-module clock stop mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operating	Operating possible
	High-speed on-chip oscillator	—	Operating possible
	Low-speed on-chip oscillator	—	Operating possible
	IWDT-dedicated on-chip oscillator	Operating	Operating possible
	PLL	Operating	Operating possible
	CPU	Stopped (retained)	Stopped (retained)
	On-chip RAM (0000 0000h to 0000 3FFFh): RX62T RAM and ECCRAM: RX66T	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	USB 2.0 Host/Function module (USBb)	—	Stopped

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX62T	RX66T
All-module clock stop mode	Watchdog timer (WDT: RX62T, WDTA: RX66T)	Operating	Stopped (retained)
	Independent watchdog timer (IWDT: RX62T, IWDTa: RX66T)	Operating	Operating possible
	Port output enable (POE3: RX62T, POE3B: RX66T)	Operating possible	Operating possible*1
	8-bit timer (unit 0, unit 1) (TMR)	—	Operating possible
	Voltage detection circuit (LVDA)	Operating	Operating possible
	Power-on reset circuit	Operating	Operating
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained
Software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Stopped	Stopped
	High-speed on-chip oscillator	—	Stopped
	Low-speed on-chip oscillator	—	Stopped
	IWDT-dedicated on-chip oscillator	Stopped	Operating possible
	PLL	Stopped	Stopped
	CPU	Stopped (retained)	Stopped (retained)
	On-chip RAM (0000 0000h to 0000 3FFFh): RX62T RAM and ECCRAM: RX66T	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	USB 2.0 Host/Function module (USBb)	—	Stopped
	Watchdog timer (WDT: RX62T, WDTA: RX66T)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT: RX62T, IWDTa: RX66T)	Stopped (retained)	Operating possible
	Port output enable (POE3: RX62T, POE3B: RX66T)	Stopped (retained)	Stopped (retained)
	8-bit timer (unit 0, unit 1) (TMR)	—	Stopped (retained)
	Voltage detection circuit (LVDA)	Operating	Operating possible
	Power-on reset circuit	Operating	Operating
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX62T	RX66T
Deep Software Standby Mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (reset processing)	Program execution state (reset processing)
	Main clock oscillator	Stopped	Stopped
	High-speed on-chip oscillator	—	Stopped
	Low-speed on-chip oscillator	—	Stopped
	IWDT-dedicated on-chip oscillator	Stopped	Stopped (undefined)
	PLL	Stopped	Stopped
	CPU	Stopped (undefined)	Stopped (undefined)
	On-chip RAM (0000 0000h to 0000 3FFFh): RX62T RAM and ECCRAM: RX66T	Stopped (undefined)	Stopped (undefined)
	Flash memory	Stopped (undefined)	Stopped (retained)
	USB 2.0 Host/Function module (USBb)	—	Stopped (undefined)
	Watchdog timer (WDT: RX62T, WDTA: RX66T)	Stopped (undefined)	Stopped (undefined)
	Independent watchdog timer (IWDT: RX62T, IWDTa: RX66T)	Stopped (undefined)	Stopped (undefined)
	Port output enable (POE3: RX62T, POE3B: RX66T)	Stopped (undefined)	Stopped (undefined)
	8-bit timer (unit 0, unit 1) (TMR)	—	Stopped (undefined)
	Voltage detection circuit (LVDA)	Operating	Operating possible
	Power-on reset circuit	Operating	Operating
	Peripheral modules	Stopped (undefined)	Stopped (undefined)
	I/O ports	Retained	Retained

Notes: “Operation possible” means that whether the state is operating or stopped is controlled by the control register setting.

“Stopped (retained)” means that internal register values are retained and internal operations are suspended.

“Stopped (undefined)” means that internal register values are undefined and power is not supplied to the internal circuit.

1. If POE interrupts are enabled and a POE interrupt source occurs while the chip is in all-module clock stop mode, return from all-module clock stop mode does not occur but the state of the interrupt source flag is retained. If a different source initiates return from all-module clock stop mode in this state, the POE interrupt is generated after the return.

Table 2.13 Comparison of Low Power Consumption Registers

Register	Bit	RX62T	RX66T
SBYCR	STS[4:0]	Standby timer select	—
	OPE	—	Output port enable bit
MSTPCRA	MSTPA2	—	8-bit timer 7/6 (unit 3) module stop bit
	MSTPA3	—	8-bit timer 5/4 (unit 2) module stop bit
	MSTPA4	—	8-bit timer 3/2 (unit 1) module stop bit
	MSTPA5	—	8-bit timer 1/0 (unit 0) module stop bit
	MSTPA7	General PWM timer module stop bit	General pwm timer/high resolution PWM/GPTW-dedicated port output enable module stop bit
	MSTPA19	—	12-bit D/A converter module stop bit
	MSTPA23	10-bit A/D converter module stop bit	12-bit A/D converter (unit 2) module stop bit
	MSTPA24	12-bit A/D converter control section module stop bit	Module stop A24 bit
	MSTPA27	—	Module Stop A27 bit
	MSTPA28	Data transfer controller module stop bit	DMA controller/data transfer controller module stop bit
	MSTPA29	—	Module stop A29 bit
MSTPCRB	MSTPB4	—	Serial communication interface 12 module stop bit
	MSTPB6	—	Data operation circuit module stop bit
	MSTPB7	LIN module stop bit	—
	MSTPB9	—	Event link controller module stop bit
	MSTPB10	—	Comparator C module stop bit
	MSTPB19	—	Universal serial bus 2.0 FS interface module stop bit
	MSTPB25	—	Serial communication interface 6 module stop bit
	MSTPB26	—	Serial communication interface 5 module stop bit
	MSTPB29	Serial communication interface 2 module stop bit	—
	MSTPB31	Serial communication interface 0 module stop bit	—
MSTPCRC	MSTPC6	—	ECCRAM module stop bit
	MSTPC19	—	CAC Module Stop bit
	MSTPC24	—	Serial communications interface 11 module stop bit
	MSTPC26	—	Serial communications interface 9 module stop bit
	MSTPC27	—	Serial communications interface 8 module stop bit

Register	Bit	RX62T	RX66T
MSTPCRD	—	—	Module stop control register D
RSTCKCR	—	—	Sleep mode return clock source switching register
DPSBYCR	—	Deep standby control register	Deep standby control register
		Initial values after a reset are different.	
DPSWCR	—	Deep standby wait control register	—
DPSIER	—	Deep standby interrupt enable register	—
DPSIER0	—	—	Deep standby interrupt enable register 0
DPSIER1	—	—	Deep standby interrupt enable register 1
DPSIER2	—	—	Deep standby interrupt enable register 2
DPSIFR	—	Deep standby interrupt flag register	—
DPSIFR0	—	—	Deep standby interrupt flag register 0
DPSIFR1	—	—	Deep standby interrupt flag register 1
DPSIFR2	—	—	Deep standby interrupt flag register 2
DPSIEGR	—	Deep standby interrupt edge register	—
DPSIEGR0	—	—	Deep standby interrupt edge register 0
DPSIEGR1	—	—	Deep standby interrupt edge register 1
DPSIEGR2	—	—	Deep standby interrupt edge register 2
RSTSR	—	Reset status register	—

2.8 Exception Handling

Table 2.14 is a comparative listing of vectors, and Table 2.15 is a comparative listing of instructions for returning from exception handling routines.

Table 2.14 Comparison of Vectors

Item		RX62T	RX66T
Undefined instruction exception		Fixed vector table	Exception vector table (EXTB)
Privileged instruction exception		Fixed vector table	Exception vector table (EXTB)
Access exception		Fixed vector table	Exception vector table (EXTB)
Floating-point exception (RX62T)/ single-precision floating-point exception (RX66T)		Fixed vector table	Exception vector table (EXTB)
Reset		Fixed vector table	Exception vector table (EXTB)
Non-maskable interrupt		Fixed vector table	Exception vector table (EXTB)
Interrupt	Fast interrupt	FINTV	FINTV
	Other than fast interrupt	Relocatable vector table (INTB)	Interrupt vector table (INTB)
Unconditional trap		Relocatable vector table (INTB)	Interrupt vector table (INTB)

Table 2.15 Comparison of Instructions for Returning from Exception Handling Routines

Item		RX62T	RX66T
Undefined instruction exception		RTE	RTE
Privileged instruction exception		RTE	RTE
Access exception		RTE	RTE
Floating-point exception (RX62T)/ single-precision floating-point exception (RX66T)		RTE	RTE
Reset		Return not possible	Return not possible
Non-maskable interrupt		Return not possible	Prohibited
Interrupt	Fast interrupt	RTFI	RTFI
	Other than fast interrupt	RTE	RTE
Unconditional trap		RTE	RTE

2.9 Interrupt Controller

Table 2.16 is a comparative overview of interrupt controllers, and Table 2.17 is a comparison of interrupt controller registers.

Table 2.16 Comparative Overview of Interrupt Controllers

Item		RX62T (ICU)	RX66T (ICUC)
Interrupts	Peripheral function interrupts	• Interrupts from peripheral modules • Number of sources: 101 • Interrupt detection: Edge detection/level detection Edge detection or level detection is determined for each source of connected peripheral modules.	• Interrupts from peripheral modules • Number of sources: 256 • Interrupt detection method: Edge detection/level detection (fixed for each interrupt source) • Group interrupt: Multiple interrupt sources are grouped together and treated as an interrupt source. — Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) — Group BL0/BL1 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) — Group AL0 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.
	External pin interrupts	Interrupts from pins IRQ7 to IRQ0 • Number of sources: 8 • Interrupt detection: Low level/falling edge/rising edge/rising and falling edges One of these detection methods can be set for each source.	Interrupt by the input signal to the IRQi pin (i = 0 to 15) • Number of sources: 16 • Interrupt detection method: Detection of low level, falling edge, rising edge, rising and falling edges One of these detection methods can be set for each source. • Digital filter can be used to remove noise.

Item		RX62T (ICU)	RX66T (ICUC)
Interrupts	Software interrupts	• Interrupt generated by writing to a register • One interrupt source	• Interrupt request can be generated by writing to a register. • Two interrupt sources
	Interrupt priority levels	Specified by registers.	Priority level can be set with interrupt source priority register r (IPRr) (r = 000 to 255).
	Fast interrupt function	Faster interrupt processing of the CPU can be set only for a single interrupt source.	CPU interrupt response time can be reduced. This function can be used for only one interrupt source.
	DTC control	The DTC can be activated by interrupt sources. • Number of DTC activating sources: 87 (78 peripheral function interrupts + 8 external pin interrupts + 1 software interrupt)	Interrupt sources can be used to start the DTC. • Number of DTC activating sources: 129 (111 peripheral function interrupts + 16 external pin interrupts + 2 software interrupt)
	DMAC control	—	Interrupt sources can be used to start the DMAC.
Non-maskable interrupts	NMI pin interrupt	• Interrupt from the NMI pin — Interrupt detection: Falling edge/rising edge	• Interrupt by the input signal to the NMI pin — Interrupt detection: Falling edge/rising edge — Digital filter can be used to remove noise.
	Voltage monitoring interrupt	Interrupt during power-voltage fall detection	Interrupt during power-voltage rise/fall detection from voltage detection circuit 1 (LVD1) or voltage detection circuit 2 (LVD2)
	Oscillation stop detection interrupt	Interrupt during oscillation stop detection	This interrupt occurs when the main clock oscillator stop is detected.
	WDT underflow/ refresh error interrupt	—	This interrupt occurs when the watchdog timer (WDT) underflows or a refresh error occurs.
	IWDT underflow/refresh error interrupt	—	This interrupt occurs when the independent watchdog timer (IWDT) underflows or a refresh error occurs.
	RAM error interrupt	—	This interrupt occurs when a parity check error is detected in the RAM or an ECC error is detected in the ECCRAM.

Item		RX62T (ICU)	RX66T (ICUC)
Return from low power consumption state	Sleep mode	Return is initiated by non-maskable interrupts or any other interrupt source.	Exit sleep mode by any interrupt source.
	All-module clock stop mode	Return is initiated by non-maskable interrupts, IRQ7 to IRQ0 interrupts, and WDT interrupts.	Exit all-module clock stop mode by the NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection interrupt, USB resume, IWDT, TMR0 to TMR3).
	Software standby mode	Return is initiated by non-maskable interrupts and IRQ7 to IRQ0 interrupts.	Exit software standby mode by the NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, IWDT).
	Deep software standby mode	Return is initiated by the NMI pin interrupt, external interrupts, and some internal interrupts (voltage monitor).	Exit deep software standby mode by the NMI pin interrupt, specific external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2).

Table 2.17 Comparison of Interrupt Controller Registers

Register	Bit	RX62T (ICU)	RX66T (ICUC)
IRn*1	—	Interrupt request register n (n = 016 to 254)	Interrupt request register n (n = 016 to 255)
IPRm*1	—	Interrupt priority register m (m = 00h to 90h)	Interrupt source priority register m (m = 000 to 255)
SWINT2R	—	—	Software interrupt 2 generation register
DTCERn*1	—	DTC activation enable register n (n = 027 to 254)	DTC transfer request enable register n (n = 026 to 255)
DMRSRm	—	—	DMAC trigger select register m (m = 0 to 7)
IRQCRn	—	IRQ control register n (n = 0 to 7)	IRQ control register n (n = 0 to 15)
IRQFLTE0	—	—	IRQ pin digital filter enable register 0
IRQFLTE1	—	—	IRQ pin digital filter enable register 1
IRQFLTC0	—	—	IRQ pin digital filter setting register 0
IRQFLTC1	—	—	IRQ pin digital filter setting register 1

Register	Bit	RX62T (ICU)	RX66T (ICUC)
NMISR	LVDST	Voltage-monitoring interrupt detection status flag	—
	OSTST	Oscillation stop detection interrupt status flag (b2)	Oscillation stop detection interrupt status flag (b1)
	WDTST	—	WDT underflow/refresh error status flag
	IWDTST	—	IWDT underflow/refresh error status flag
	LVD1ST	—	Voltage monitoring 1 interrupt status flag
	LVD2ST	—	Voltage monitoring 2 interrupt status flag
	RAMST	—	RAM error interrupt status flag
NMIER	LVDEN	Voltage-monitoring interrupt enable bit	—
	OSTEN	Oscillation stop detection interrupt enable bit (b2)	Oscillation stop detection interrupt enable bit (b1)
	WDTEN	—	WDT underflow/refresh error enable bit
	IWDTEN	—	IWDT underflow/refresh error enable bit
	LVD1EN	—	Voltage monitoring 1 interrupt enable bit
	LVD2EN	—	Voltage monitoring 2 interrupt enable bit
	RAMEN	—	RAM error interrupt enable bit
NMICLR	OSTCLR	OST clear bit (b2)	OST clear bit (b1)
	WDTCLR	—	WDT clear bit
	IWDTCLR	—	IWDT clear bit
	LVD1CLR	—	LVD1 clear bit
	LVD2CLR	—	LVD2 clear bit
NMIFLTE	—	—	NMI pin digital filter enable register
NMIFLTC	—	—	NMI pin digital filter setting register
GRPBE0, GRPBL0/GRPBL1, GRPAL0	—	—	Group BE0, BL0/1, AL0 interrupt request register,
GENBE0, GENBL0/GENBL1, GENAL0	—	—	Group BE0, BL0/1, AL0 interrupt request enable register
GCRBE0	—	—	Group BE0 interrupt clear register
PIARk	—	—	Software configurable interrupt A request register k (k = 0h to 12h)
SLIARn	—	—	Software configurable interrupt A source select register n (n = 208 to 255)
SLIPRCR	—	—	Software configurable interrupt source select register write protect register

Note: 1. On the RX62T Group n = 255 correspond to a reserved area.

2.10 Buses

Table 2.18 is a comparative overview of buses, and Table 2.19 is a comparison of bus registers.

Table 2.18 Comparative Overview of Buses

Bus Type		RX62T	RX66T
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (on-chip RAM, on-chip ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (on-chip RAM, on-chip ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	Connected to on-chip RAM	Connected to RAM
	Memory bus 2	Connected to on-chip ROM	Connected to code flash memory
	Memory bus 3	—	Connected to ECCRAM
Internal main buses	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DTC • Connected to on-chip memory (on-chip RAM, on-chip ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the DMAC and DTC • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (such as a bus error monitoring section and an interrupt) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules(such as WDT, CMT, CRC, and SCI) • Operates in synchronization with the peripheral-module clock (PCLK)	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, 4, or 5) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 3	—	• Connected to peripheral modules (USBb and CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 4	• Connected to peripheral modules (MTU3 and GPT) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (MTU3, GPTW, HRPWM, RSPI and SCIi) • Operates in synchronization with the peripheral-module clock (PCLKA)

Bus Type		RX62T	RX66T
Internal peripheral buses	Internal peripheral bus 5	—	Reserved area
	Internal peripheral bus 6	• Connected to on-chip ROM (for programming and erasure) and data-flash memory • Operates in synchronization with the peripheral-module clock (PCLK)	• Connected to code flash (in P/E) and data flash memory • Operates in synchronization with the FlashIF clock (FCLK)
External bus	CS area	—	• Connected to the external devices • Operates in synchronization with the external-bus clock (BCLK)

Table 2.19 Comparison of Bus Registers

Register	Bit	RX62T	RX66T
CSnCR	—	—	CSn control register (n = 0 to 3)
CSnREC	—	—	CSn recovery cycle register (n = 0 to 3)
CSRECEN	—	—	CS recovery cycle insertion enable register
CSnMOD	—	—	CSn mode register (n = 0 to 3)
CSnWCR1	—	—	CSn wait control register 1 (n = 0 to 3)
CSnWCR2	—	—	CSn wait control register 2 (n = 0 to 3)
BEREN	TOEN	—	Timeout detection enable
BERSR1	TO	—	Timeout
BUSPRI	—	—	Bus priority control register

2.11 Memory-Protection Unit

Table 2.20 is a comparison of memory-protection unit registers.

Table 2.20 Comparison of Memory-Protection Unit Registers

Register	Bit	RX62T (MPU)	RX66T (MPU)
MPESTS	IA (RX62T) IMPER (RX66T)	Instruction memory-protection error generated bit	Instruction memory-protection error generation bit
	DA (RX62T) DMPER (RX66T)	Data memory-protection error generated bit	Data memory-protection error generation bit

2.12 Data Transfer Controller

Table 2.21 is a comparative overview of data transfer controller.

Table 2.21 Comparative Overview of Data Transfer Controller

Item	RX62T (DTC)	RX66T (DTCa)
Transfer modes	• Normal transfer mode — A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address is returned to the transfer start address after the number of data transfers corresponding to "repeat size". — The maximum repeat size is 256. • Block transfer mode — A single activation leads to the transfer of a single block. — The maximum block size is 255.	• Normal transfer mode — A single transfer request leads to a single data transfer. • Repeat transfer mode — A single transfer request leads to a single data transfer. — The transfer address is returned to the transfer start address after the number of data transfers corresponding to “repeat size”. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, 1024 bytes. • Block transfer mode — A single transfer request leads to the transfer of a single block. — The maximum block size is 256 × 32 bits = 1024 bytes.
Number of transfer channels	Channel transfer corresponding to the interrupt source is possible (transferred by DTC activation request from the ICU).	The same number as all interrupt sources that can start the DTC transfer.
Chain transfer function	• Data of multiple channels can be transferred on a single activation source (chain transfer). • Either “executed when the counter is 0” or “always executed” can be selected for chain transfer.	• Multiple types of data transfers can sequentially be executed in response to a single request. • Either “performed only when the transfer counter becomes 0” or “every time” can be selected.
Transfer space	• In short-address mode: 16 MB (Areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh excepting reserved areas) • In full-address mode: 4 GB (Area from 0000 0000h to FFFF FFFFh excepting reserved areas)	• In short-address mode: 16 MB (Areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh except reserved areas) • In full-address mode: 4 GB (Area from 0000 0000h to FFFF FFFFh except reserved areas)
Data transfer units	• Length of a single data: 8, 16, or 32 bits • Number of data for a single block: 1 to 255 data	• Single data: 1 byte (8 bits), 1 word (16 bits), 1 longword (32 bits) • Single block size: 1 to 256 data

Item	RX62T (DTC)	RX66T (DTCa)
CPU interrupt source	• An interrupt request can be generated to the CPU on a DTC activation interrupt. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of specified volume.	• An interrupt request can be generated to the CPU on a request source for a data transfer. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of specified volume.
Event link function	—	An event link request is generated after one data transfer (for block, after one block transfer).
Read skip	Transfer data read skip can be specified.	Reading of the transfer information can be skipped when the same transfer is repeated.
Write-back skip	When "fixed" is selected for transfer source address and/or transfer destination address, write-back skip execution is provided.	Write-back of the transferred data that is not updated can be skipped when the address of the transfer source and/or destination is fixed.
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

2.13 I/O Ports

Table 2.22 to Table 2.27 are comparative overviews of I/O ports for each package, Table 2.28 is a comparison of I/O port functions, and Table 2.29 is a comparison of I/O port registers.

Table 2.22 Comparative Overview of I/O Ports on 112-Pin Packages

Item	RX62T (112-Pin)	RX66T (112-Pin) (With PGA Pseudo-Differential Input and Without USB Pin)
PORT0	—	P00, P01
PORT1	P10, P11	P10 to P17
PORT2	P20 to P24	P20 to P24, P27
PORT3	P30 to P33	P30 to P33, P36, P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P55	P52 to P55
PORT6	P60 to P65	P60 to P65
PORT7	P70 to P76	P70 to P76
PORT8	P80 to P82	P80 to P82
PORT9	P90 to P96	P90 to P96
PORTA	PA0 to PA5	PA0 to PA5
PORTB	PB0 to PB7	PB0 to PB7
PORTC	—	PC0 to PC2
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE5	PE0 to PE5
PORTG	PG0 to PG5	PG0 to PG2
PORTH	—	PH0, PH4

Table 2.23 Comparative Overview of I/O Ports on 100-Pin Packages (RX66T: With PGA Pseudo-Differential Input)

Item	RX62T (100-Pin)	RX66T (100-Pin)	
		With PGA Pseudo-Differential Input and USB Pin	With PGA Pseudo-Differential Input and Without USB Pin
PORT0	—	P00, P01	P00, P01
PORT1	P10, P11	P10, P11	P10, P11
PORT2	P20 to P24	P20 to P24, P27	P20 to P24, P27
PORT3	P30 to P33	P30 to P33, P36, P37	P30 to P33, P36, P37
PORT4	P40 to P47	P40 to P47	P40 to P47
PORT5	P50 to P55	P52 to P55	P52 to P55
PORT6	P60 to P65	P60 to P65	P60 to P65
PORT7	P70 to P76	P70 to P76	P70 to P76
PORT8	P80 to P82	P80 to P82	P80 to P82
PORT9	P90 to P96	P90 to P96	P90 to P96
PORTA	PA0 to PA5	PA0 to PA5	PA0 to PA5
PORTB	PB0 to PB7	PB0 to PB6	PB0 to PB7
PORTD	PD0 to PD7	PD2 to PD7	PD0 to PD7
PORTE	PE0 to PE5	PE0 to PE5	PE0 to PE5
PORTH	—	PH0, PH4	PH0, PH4

Table 2.24 Comparative Overview of I/O Ports on 100-Pin Packages (RX66T: Without PGA Pseudo-Differential Input)

Item	RX62T (100-Pin)	RX66T (100 Pins) (Without PGA Pseudo-Differential Input and USB Pin)
PORT0	—	P00, P01
PORT1	P10, P11	P10, P11
PORT2	P20 to P24	P20 to P24
PORT3	P30 to P33	P30 to P33, P36, P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P55	P50 to P55
PORT6	P60 to P65	P60 to P65
PORT7	P70 to P76	P70 to P76
PORT8	P80 to P82	P80 to P82
PORT9	P90 to P96	P90 to P96
PORTA	PA0 to PA5	PA0 to PA5
PORTB	PB0 to PB7	PB0 to PB7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE5	PE0 to PE5

Table 2.25 Comparative Overview of I/O Ports on 80-Pin Packages (RX62T: Except for R5F562TxGDFF)

Item	RX62T (80-Pin) (Except for R5F562TxGDFF)	RX66T (80-Pin) (With PGA Pseudo-Differential Input and Without USB Pin)
PORT0	—	P00, P01
PORT1	P10, P11	P10, P11
PORT2	P20 to P24	P20 to P22, P27
PORT3	P30 to P33	P30, P31, P36, P37
PORT4	P40 to P47	P40 to P47
PORT5	—	P52 to P55
PORT6	P60 to P63	P62, P64, P65
PORT7	P70 to P76	P70 to P76
PORT9	P91 to P96	P90 to P96
PORTA	PA2 to PA4, PA5	PA3, PA5
PORTB	PB0 to PB7	PB0 to PB6
PORTD	PD3 to PD7	PD2 to PD7
PORTE	PE0, PE2 to PE4	PE2 to PE4
PORTH	—	PH0, PH4

Table 2.26 Comparative Overview of I/O Ports on 80-Pin Packages (RX62T: R5F562TxGDFF)

Item	RX62T (80 Pins) (R5F562TxGDFF)	RX66T (80 Pins) (With PGA Pseudo-Differential Input and Without USB Pin)
PORT0	—	P00, P01
PORT1	P10	P10, P11
PORT2	P20, P22 to P24	P20 to P22, P27
PORT3	P30 to P33	P30, P31, P36, P37
PORT4	P40 to P47	P40 to P47
PORT5	—	P52 to P55
PORT6	—	P62, P64, P65
PORT7	P70 to P76	P70 to P76
PORT8	P80 to P82	—
PORT9	P90 to P96	P90 to P96
PORTA	PA3, PA5	PA3, PA5
PORTB	PB0 to PB7	PB0 to PB6
PORTD	PD2 to PD7	PD2 to PD7
PORTE	PE0 to PE5	PE2 to PE4
PORTH	—	PH0, PH4

Table 2.27 Comparative Overview of I/O Ports on 64-Pin Packages

Item	RX62T (64 Pins)	RX66T (64 Pins) (With PGA Pseudo-Differential Input and Without USB Pin)
PORT0	—	P00, P01
PORT1	P10, P11	P11
PORT2	P22 to P24	P20 to P22
PORT3	P30 to P33	P36, P37
PORT4	P40 to P47	P40 to P42, P44 to P46
PORT5	—	P52 to P54
PORT6	—	P64, P65
PORT7	P70 to P76	P70 to P76
PORT9	P91 to P94	P90 to P96
PORTA	PA2 to PA5	—
PORTB	PB0 to PB7	PB0 to PB6
PORTD	PD3 to PD7	PD3 to PD7
PORTE	PE2	PE2
PORTH	—	PH0, PH4

Table 2.28 Comparison of I/O Port Functions

Item	Port Symbol	RX62T	RX66T
Input pull-up function	PORT0	—	P00, P01
	PORT1	—	P10 to P17
	PORT2	—	P20 to P27
	PORT3	—	P30 to P37
	PORT4	—	P43, P47
	PORT5	—	P50 to P55
	PORT6	—	P60 to P65
	PORT7	—	P70 to P76
	PORT8	—	P80 to P82
	PORT9	—	P90 to P96
	PORTA	—	PA0 to PA7
	PORTB	—	PB0 to PB7
	PORTC	—	PC0 to PC6
	PORTD	—	PD0 to PD7
	PORTE	—	PE0, PE1, PE3 to PE6
	PORTF	—	PF0 to PF3
	PORTG	—	PG0 to PG2
	PORTH	—	PH1 to PH3, PH5 to PH7
	PORTK	—	PK0 to PK2
Open-drain output function	PORT0	—	P00, P01
	PORT1	—	P10 to P17
	PORT2	—	P20 to P27
	PORT3	—	P30 to P37
	PORT4	—	P43, P47
	PORT5	—	P50 to P55
	PORT6	—	P60 to P65
	PORT7	—	P70 to P76
	PORT8	—	P80 to P82
	PORT9	—	P90 to P96
	PORTA	—	PA0 to PA7
	PORTB	PB1, PB2	PB0 to PB7
	PORTC	—	PC0 to PC6
	PORTD	—	PD0 to PD7
	PORTE	—	PE0, PE1, PE3 to PE6
	PORTF	—	PF0 to PF3
	PORTG	—	PG0 to PG2
	PORTH	—	PH1 to PH3, PH5 to PH7
	PORTK	—	PK0 to PK2

Item	Port Symbol	RX62T	RX66T
Drive capacity switching function	PORT0	—	P00, P01
	PORT1	—	P10 to P17
	PORT2	—	P20 to P27
	PORT3	—	P30 to P37
	PORT4	—	P43, P47
	PORT5	—	P50 to P55
	PORT6	—	P60 to P65
	PORT7	—	P70 to P76
	PORT8	—	P80 to P82
	PORT9	—	P90 to P96
	PORTA	—	PA0 to PA7
	PORTB	—	PB0 to PB7
	PORTC	—	PC0 to PC6
	PORTD	—	PD0 to PD7
	PORTE	—	PE0, PE1, PE3 to PE6
	PORTF	—	PF0 to PF3
	PORTG	—	PG0 to PG2
	PORTH	—	PH1 to PH3, PH5 to PH7
	PORTK	—	PK0 to PK2
5 V tolerant	PORTB	—	PB1, PB2
	PORTC	—	PC0*1
	PORTD	—	PD2*1

Note: 1. Implemented only on products with a RAM capacity of 128 KB.

Table 2.29 Comparison of I/O Port Registers

Register	Bit	RX62T	RX66T
DDR (RX62T) PDR (RX66T)	B0 to B7	Pn0 to Pn7 I/O select bits (n = 1 to 3, 7 to 9, A, B, D, E and G)	Pm0 to Pm7 I/O select bits (m = 0 to 9, A to H and K)
DR (RX62T) PODR (RX66T)	B0 to B7	Pn0 to Pn7 output data store bits (n = 1 to 3, 7 to 9, A, B, D, E and G)	Pm0 to Pm7 output data store bits (m = 0 to 9, A to H and K)
PORT (RX62T) PIDR (RX66T)	B0 to B7	Pn0 to Pn7 bits (n = 1 to 9, A, B, D, E and G)	Pm0 to Pm7 bits (m = 0 to 9, A to H and K)
PMR	—	—	Port Mode Register
ICR	—	Input buffer control register	—
PF8IRQ	—	Port function register 8	—
PF9IRQ	—	Port function register 9	—
PFAADC	—	Port function register A	—
PFCMTU	—	Port function register C	—
PFDGPT	—	Port function register D	—
PFFSCI	—	Port function register F	—
PFGSPI	—	Port function register G	—
PFHSPI	—	Port function register H	—
RFJCAN	—	Port function register J	—
PFKLIN	—	Port function register K	—
PFMPOE	—	Port function register M	—
PFNPOE	—	Port function register N	—
ODR0	—	—	Open-drain control register 0
ODR1	—	—	Open-drain control register 1
PCR	—	—	Pull-up resistor control register
DSCR	—	—	Drive capacity control register
DSCR2	—	—	Drive capacity control register 2

2.14 Multi-Function Timer Pulse Unit 3

Table 2.30 is a comparative overview of multi-function timer pulse unit 3, Table 2.31 is a comparison of multi-function timer pulse unit 3 registers, and Table 2.32 and Table 2.33 are comparative listings of TPSC bit settings.

Table 2.30 Comparative Overview of Multi-Function Timer Pulse Unit 3

Item	RX62T (MTU3)	RX66T (MTU3d)
Pulse input/output	24 lines max.	28 lines max.
Pulse input	3 lines	3 lines
Count clock	Six to eight clocks for each channel (four clocks for MTU5)	11 clocks for each channel (14 clocks for MTU0 and MTU9, 12 clocks for MTU2, 10 clocks for MTU5, and four clocks for MTU1 & MTU2 (LWA = 1))
Operating frequency	8 to 100 MHz	Up to 160 MHz
Available operations	[MTU0 to MTU4, MTU6, and MTU7] • Waveform output on compare match • Input capture function • Counter-clearing operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing on compare match or input capture • Simultaneous input and output to registers in synchronization with counter operations • Up to 12-phase PWM output in combination with synchronous operation	[MTU0 to MTU4, MTU6, MTU7, MTU9] • Waveform output on compare match • Input capture function (noise filter setting available) • Counter-clearing operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing on compare match or input capture • Simultaneous input and output to registers in synchronization with counter operations • Up to 14-phase PWM output in combination with synchronous operation
	[MTU0, MTU3, MTU4, MTU6, and MTU7] Buffer operation specifiable	[MTU0, MTU3, MTU4, MTU6, MTU7, and MTU9] Buffer operation specifiable
	[MTU3, MTU4, MTU6, and MTU7] • Through interlocked operation of MTU3, MTU4, MTU6, and MTU7, output of positive and negative signals in six phases (for a total of 12 phases) in complementary-PWM and reset-PWM operation • In complementary PWM mode, transfer of values from buffer registers to temporary registers on peaks and troughs of the timer-counter values or writing to the buffer registers (MTU4.TGRD and MTU7.TGRD) • Double-buffering selectable in complementary PWM mode	[MTU3, MTU4, MTU6, MTU7] • Through interlocked operation of MTU3/4 and MTU6/7, the positive and negative signals in six phases (12 phases in total) can be output in complementary PWM and reset-synchronized PWM operation. • In complementary PWM mode, transfer of values from buffer registers to temporary registers on crests and troughs of the timer-counter values or writing to the buffer registers (MTU4.TGRD and MTU7.TGRD) • Double-buffering selectable in complementary PWM mode

Item	RX62T (MTU3)	RX66T (MTU3d)
Available operations	[MTU1 and MTU2] • Independently specifiable phase-counting mode • Capable of cascade-connected operation	[MTU1, MTU2] • Phase counting mode can be specified independently • 32-bit phase counting mode can be specified for interlocked operation of MTU1 and MTU2 (when TMDR3.LWA = 1) • Cascade connection operation available
	[MTU3 and MTU4] Through interlocking with MTU0, a mode for driving AC synchronous motors (brushless DC motors) by using complementary PWM output and reset PWM output is settable and allows the selection of two types of waveform output (chopping or level)	[MTU3, MTU4] Through interlocking with MTU0, a mode for driving AC synchronous motors (brushless DC motors) by using complementary PWM output and reset-synchronized PWM output is settable and allows the selection of two types of waveform output (chopping or level)
	[MTU5] Capable of operation as a dead-time compensation counter	[MTU5] Capable of operation as a dead-time compensation counter
	—	[MTU6, MTU7] Through interlocking with MTU9, a mode for driving AC synchronous motors (brushless DC motors) by using complementary PWM output and reset-synchronized PWM output is settable and allows the selection of two types of waveform output (chopping or level)
Interrupt-skipping function	In complementary PWM mode, interrupts on crests and troughs of counter values and triggers to start conversion by the A/D converter can be skipped	In complementary PWM mode, interrupts on crests and troughs of counter values and triggers to start conversion by the A/D converter can be skipped
Interrupt sources	38 sources	45 sources
Buffer operation	Automatic transfer of register data (transfer from the buffer register to the timer register)	Automatic transfer of register data (transfer from the buffer register to the timer register)
Trigger generation	• A/D converter start triggers can be generated • A/D converter start request delaying function enables A/D converter to be started with any desired timing and to be synchronized with PWM output	• A/D converter start triggers can be generated • A/D converter start request delaying function enables A/D converter to be started with any desired timing and to be synchronized with PWM output
Low power consumption function	Module stop mode can be set.	Module stop mode can be set
Complementary PWM mode	Set (PWM duty value −1) as the value to be output to the buffer registers (MTU3.TGRE, MTU4.TGRE, MTU4.TGRF (MTU6.TGRE, MTU7.TGRE, MTU7.TGRF)) only when using the double buffer function	Set the PWM duty value to be output to the buffer registers (MTU3.TGRE, MTU4.TGRE, MTU4.TGRF (MTU6.TGRE, MTU7.TGRE, MTU7.TGRF)) only when using the double buffer function

Table 2.31 Comparison of Multi-Function Timer Pulse Unit 3 Registers

Register		Bit	RX62T (MTU3)	RX66T (MTU3d)
TCR		TPSC[2:0] TPSC[1:0]	Time prescaler select bits Refer to Table 2.32 and Table 2.33 for details.	Time prescaler select bits Refer to Table 2.32 and Table 2.33 for details.
TCR2		—	—	Timer control register 2
TMDR1		MD[3:0]	Mode select bits b3 b0 0 0 0 0: Normal mode 0 0 0 1: Setting prohibited 0 0 1 0: PWM mode 1 0 0 1 1: PWM mode 2 0 1 0 0: Phase counting mode 1 0 1 0 1: Phase counting mode 2 0 1 1 0: Phase counting mode 3 0 1 1 1: Phase counting mode 4 1 0 0 0: Reset-synchronized PWM mode 1 0 0 1: Setting prohibited 1 0 1 x: Setting prohibited 1 1 0 0: Setting prohibited 1 1 0 1: Complementary PWM mode 1 (transfer at crest) 1 1 1 0: Complementary PWM mode 2 (transfer at trough) 1 1 1 1: Complementary PWM mode 3 (transfer at crest and trough) x: Don't care	Mode select bits b3 b0 0 0 0 0: Normal mode 0 0 0 1: Setting prohibited 0 0 1 0: PWM mode 1 0 0 1 1: PWM mode 2 0 1 0 0: Phase counting mode 1 0 1 0 1: Phase counting mode 2 0 1 1 0: Phase counting mode 3 0 1 1 1: Phase counting mode 4 1 0 0 0: Reset-synchronized PWM mode 1 0 0 1: Phase counting mode 5 1 0 1 x: Setting prohibited 1 1 0 0: Setting prohibited 1 1 0 1: Complementary PWM mode 1 (transfer at crest) 1 1 1 0: Complementary PWM mode 2 (transfer at trough) 1 1 1 1: Complementary PWM mode 3 (transfer at crest and trough) x: Don't care
TMDR3		—	—	Timer mode register 3
TSR	TSR	TGFA	Input capture/output compare flag A	—
		TGFB	Input capture/output compare flag B	—
		TGFC	Input capture/output compare flag C	—
		TGFD	Input capture/output compare flag D	—
		TCFV	Overflow flag	—
		TCFU	Underflow flag	—
		CMFW5	Compare match/input capture flag W5	—
		CMFV5	Compare match/input capture flag V5	—
		CMFU5	Compare match/input capture flag U5	—
	TSR2	TGFE	Compare match flag E	—
		TGFF	Compare match flag F	—
TCNTLW		—	—	Timer longword counter

Register	Bit	RX62T (MTU3)	RX66T (MTU3d)
TGRALW, TGRBLW	—	—	Timer longword general registers
TSTRA	CST9	—	Counter start 9
TSYRA	SYNC9	—	Timer synchronous operation 9
TCSYSTR	SCH9	—	Synchronous start 9
TGCRB	—	—	Timer control register
NFCRn	—	—	Noise filter control register n (n = 0 to 4, 6, 7, 9, and C)
NFCR5	—	—	Noise filter control register 5
TADSTRGR0	—	—	A/D conversion start request select register 0
TADSTRGR1	—	—	A/D conversion start request select register 1

Table 2.32 Comparison of TPSC Bit Settings (Other Than MTU5)

Channel	RX62T (MTU3)		RX66T (MTU3d)		
	TCR.TPSC [2:0]	Description	TCR2.TPSC2 [2:0]	TCR.TPSC [2:0]	Description
MTU0 (RX62T)	0 0 0	Internal clock: counts on ICLK/1	0 0 0	0 0 0	Internal clock: counts on PCLKC/1
MTU0, MTU9 (RX66T)	0 0 1	Internal clock: counts on ICLK/4	0 0 0	0 0 1	Internal clock: counts on PCLKC/4
	0 1 0	Internal clock: counts on ICLK/16	0 0 0	0 1 0	Internal clock: counts on PCLKC/16
	0 1 1	Internal clock: counts on ICLK/64	0 0 0	0 1 1	Internal clock: counts on PCLKC/64
	1 0 0	External clock: counts on MTCLKA pin input	0 0 0	1 0 0	External clock: counts on MTCLKA pin input
	1 0 1	External clock: counts on MTCLKB pin input	0 0 0	1 0 1	External clock: counts on MTCLKB pin input
	1 1 0	External clock: counts on MTCLKC pin input	0 0 0	1 1 0	External clock: counts on MTCLKC pin input
	1 1 1	External clock: counts on MTCLKD pin input	0 0 0	1 1 1	External clock: counts on MTCLKD pin input
			0 0 1	x x x	Internal clock: counts on PCLKC/2
			0 1 0	x x x	Internal clock: counts on PCLKC/8
			0 1 1	x x x	Internal clock: counts on PCLKC/32
			1 0 0	x x x	Internal clock: counts on PCLKC/256
			1 0 1	x x x	Internal clock: counts on PCLKC/1024
			1 1 0	x x x	Setting prohibited
			1 1 1	x x x	External clock: counts on MTIOC1A pin input

Channel	RX62T (MTU3)		RX66T (MTU3d)		
	TCR.TPSC [2:0]	Description	TCR2.TPSC2 [2:0]	TCR.TPSC [2:0]	Description
MTU1	0 0 0	Internal clock: counts on ICLK/1	0 0 0	0 0 0	Internal clock: counts on PCLKC/1
	0 0 1	Internal clock: counts on ICLK/4	0 0 0	0 0 1	Internal clock: counts on PCLKC/4
	0 1 0	Internal clock: counts on ICLK/16	0 0 0	0 1 0	Internal clock: counts on PCLKC/16
	0 1 1	Internal clock: counts on ICLK/64	0 0 0	0 1 1	Internal clock: counts on PCLKC/64
	1 0 0	External clock: counts on MTCLKA pin input	0 0 0	1 0 0	External clock: counts on MTCLKA pin input
	1 0 1	External clock: counts on MTCLKB pin input	0 0 0	1 0 1	External clock: counts on MTCLKB pin input
	1 1 0	Internal clock: counts on ICLK/256	0 0 0	1 1 0	Internal clock: counts on PCLKC/256
	1 1 1	Counts on MTU2.TCNT overflow/underflow	0 0 0	1 1 1	Counts on MTU2.TCNT overflow/underflow
			0 0 1	x x x	Internal clock: counts on PCLKC/2
			0 1 0	x x x	Internal clock: counts on PCLKC/8
			0 1 1	x x x	Internal clock: counts on PCLKC/32
			1 0 0	x x x	Internal clock: counts on PCLKC/1024
			1 0 1	x x x	Setting prohibited
			1 1 0	x x x	Setting prohibited
			1 1 1	x x x	Setting prohibited
MTU2	0 0 0	Internal clock: counts on ICLK/1	0 0 0	0 0 0	Internal clock: counts on PCLKC/1
	0 0 1	Internal clock: counts on ICLK/4	0 0 0	0 0 1	Internal clock: counts on PCLKC/4
	0 1 0	Internal clock: counts on ICLK/16	0 0 0	0 1 0	Internal clock: counts on PCLKC/16
	0 1 1	Internal clock: counts on ICLK/64	0 0 0	0 1 1	Internal clock: counts on PCLKC/64
	1 0 0	External clock: counts on MTCLKA pin input	0 0 0	1 0 0	External clock: counts on MTCLKA pin input
	1 0 1	External clock: counts on MTCLKB pin input	0 0 0	1 0 1	External clock: counts on MTCLKB pin input
	1 1 0	External clock: counts on MTCLKC pin input	0 0 0	1 1 0	External clock: counts on MTCLKC pin input
	1 1 1	Internal clock: counts on ICLK/1024	0 0 0	1 1 1	Internal clock: counts on PCLKC/1024
			0 0 1	x x x	Internal clock: counts on PCLKC/2
			0 1 0	x x x	Internal clock: counts on PCLKC/8
			0 1 1	x x x	Internal clock: counts on PCLKC/32

Channel	RX62T (MTU3)		RX66T (MTU3d)		
	TCR.TPSC [2:0]	Description	TCR2.TPSC2 [2:0]	TCR.TPSC [2:0]	Description
MTU2			1 0 0	x x x	Internal clock: counts on PCLKC/256
			1 0 1	x x x	Setting prohibited
			1 1 0	x x x	Setting prohibited
			1 1 1	x x x	Setting prohibited
MTU3 MTU4 MTU6 MTU7	0 0 0	Internal clock: counts on ICLK/1	0 0 0	0 0 0	Internal clock: counts on PCLKC/1
	0 0 1	Internal clock: counts on ICLK/4	0 0 0	0 0 1	Internal clock: counts on PCLKC/4
	0 1 0	Internal clock: counts on ICLK/16	0 0 0	0 1 0	Internal clock: counts on PCLKC/16
	0 1 1	Internal clock: counts on ICLK/64	0 0 0	0 1 1	Internal clock: counts on PCLKC/64
	1 0 0	Internal clock: counts on ICLK/256	0 0 0	1 0 0	Internal clock: counts on PCLKC/256
	1 0 1	Internal clock: counts on ICLK/1024	0 0 0	1 0 1	Internal clock: counts on PCLKC/1024
	1 1 0	External clock: counts on MTCLKA pin input*1	0 0 0	1 1 0	External clock: counts on MTCLKA pin input
	1 1 1	External clock: counts on MTCLKB pin input*1	0 0 0	1 1 1	External clock: counts on MTCLKB pin input
			0 0 1	x x x	Internal clock: counts on PCLKC/2
			0 1 0	x x x	Internal clock: counts on PCLKC/8
			0 1 1	x x x	Internal clock: counts on PCLKC/32
			1 0 0	x x x	Setting prohibited
			1 0 1	x x x	Setting prohibited
			1 1 0	x x x	Setting prohibited
			1 1 1	x x x	Setting prohibited

x: Don't care

Note: 1. This setting is not available on MTU6 or MTU7.

Table 2.33 Comparison of TPSC Bit Settings (MTU5)

	RX62T (MTU3)		RX66T (MTU3d)		
Channel	TCR.TPSC [1:0]	Description	TCR2.TPSC2 [2:0]	TCR.TPSC [1:0]	Description
MTU5	0 0	Internal clock: counts on ICLK/1	0 0 0	0 0	Internal clock: counts on PCLKC/1
	0 1	Internal clock: counts on ICLK/4	0 0 0	0 1	Internal clock: counts on PCLKC/4
	1 0	Internal clock: counts on ICLK/16	0 0 0	1 0	Internal clock: counts on PCLKC/16
	1 1	Internal clock: counts on ICLK/64	0 0 0	1 1	Internal clock: counts on PCLKC/64
			0 0 1	x x	Internal clock: counts on PCLKC/2
			0 1 0	x x	Internal clock: counts on PCLKC/8
			0 1 1	x x	Internal clock: counts on PCLKC/32
			1 0 0	x x	Internal clock: counts on PCLKC/256
			1 0 1	x x	Internal clock: counts on PCLKC/1024
			1 1 0	x x	Setting prohibited
			1 1 1	x x	External clock: counts on MTIOC1A pin input

x: Don’t care

2.15 Port Output Enable 3

Table 2.34 is a comparative overview of port output enable 3, and Table 2.35 is a comparison of port output enable 3 registers.

Table 2.34 Comparative Overview of Port Output Enable 3

Item	RX62T (POE3)	RX66T (POE3B)
Function	• Each of the POE0#, POE4#, POE8#, POE10#, and POE11# input pins can be set for falling edge, PCLK/8 × 16, PCLK/16 × 16, or PCLK/128 × 16 low-level sampling.	• Each of the POE0#, POE4#, POE8#, POE9#, POE10#, POE11#, POE12#, POE13#, and POE14# pins can be set for falling-edge or low-level detection. When setting a low-level detection, a sampling clock can be selected from PCLK/1, PCLK/2, PCLK/4, PCLK/8, PCLK/16, and PCLK/128, while the number of samples can be selected from four, eight, or 16.
	• Pins for the MTU complementary PWM output, MTU0 pins, and GPT pins can be placed in high-impedance state by POE0#, POE4#, POE8#, POE10#, and POE11# pin falling-edge or low-level sampling.	• The outputs of the target pins can be disabled by detecting falling-edge or low-level of input to the POE0#, POE4#, POE8#, POE9#, POE10#, POE11#, POE12#, POE13#, and POE14# pins.
	• Pins for the MTU complementary PWM output, MTU0 pins, and GPT pins can be placed in high-impedance state when the oscillation-stop detection circuit in the clock pulse generator detects stopped oscillation.	• The outputs of the target pins can be disabled when oscillation stop is detected by the oscillation stop detection function of the clock generator.
	• Output levels of MTU complementary PWM output pins or GPT large-current output pins are compared. If active-level continues for one cycle or more on compared pins simultaneously, MTU complementary PWM output pins or GPT large-current output pins can be placed in high-impedance state.	• The MTU complementary PWM outputs can be disabled when output levels of the MTU complementary PWM output pins are compared and simultaneous active-level output continues for one cycle or more.
		• The GPTW outputs can be disabled when output levels of the GPTW output pins (GPTW0 to GPTW2, GPTW4 to GPTW6, and GPTW7 to GPTW9 pins) are compared and simultaneous active-level output continues for one cycle or more.
	• Pins for the MTU complementary PWM output, MTU0 pins, and GPT pins can be placed in the high-impedance state in response to comparator detection on the 12-bit A/D converter (S12ADA).	• The outputs of the target pins can be disabled in response to comparator C (CMPC) output detection.

Item	RX62T (POE3)	RX66T (POE3B)
Function	• Pins for the MTU complementary PWM output, MTU0 pins, and GPT pins can be placed in the high-impedance state by setting the POE registers. • Interrupts can be generated by input-level sampling or output-level comparison results.	• The outputs of the target pins can be disabled by modifying the settings of the POE registers. • Interrupts can be generated by input-level sampling or output-level comparison results.
Pin status while output is disabled	High-impedance	• High-impedance • General I/O port
Target pins for switching to disabling of signal output	• MTU output pins — MTU0 pins (MTIOC0A-A, MTIOC0A-B, MTIOC0B-A, MTIOC0B-B, MTIOC0C, MTIOC0D) — MTU3 pins (MTIOC3B, MTIOC3D) — MTU4 pins (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) — MTU6 pins (MTIOC6B, MTIOC6D) — MTU7 pins (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D) • GPT output pins — GPT0 pins (GTIOC0A-A, GTIOC0B-A, GTIOC0A-B, GTIOC0B-B) — GPT1 pins (GTIOC1A-A, GTIOC1B-A, GTIOC1A-B, GTIOC1B-B) — GPT2 pins (GTIOC2A-A, GTIOC2B-A, GTIOC2A-B, GTIOC2B-B) — GPT3 pins (GTIOC3A, GTIOC3B)	• MTU output pins — MTU0 pins (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) — MTU3 pins (MTIOC3B, MTIOC3D) — MTU4 pins (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) — MTU6 pins (MTIOC6B, MTIOC6D) — MTU7 pins (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D) — MTU9 pins (MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D) • GPTW output pins — GPTW0 pins (GTIOC0A, GTIOC0B) — GPTW1 pins (GTIOC1A, GTIOC1B) — GPTW2 pins (GTIOC2A, GTIOC2B) — GPTW3 pins (GTIOC3A, GTIOC3B) — GPTW4 pins (GTIOC4A, GTIOC4B) — GPTW5 pins (GTIOC5A, GTIOC5B) — GPTW6 pins (GTIOC6A, GTIOC6B) — GPTW7 pins (GTIOC7A, GTIOC7B) — GPTW8 pins (GTIOC8A, GTIOC8B) — GPTW9 pins (GTIOC9A, GTIOC9B)

Item	RX62T (POE3)	RX66T (POE3B)
Conditions for generating the output disable request	• Input signal detection: Detection of the POE0#, POE4#, POE8#, POE10#, and POE11# signal level. • Simultaneous conduction between output pins: A match (simultaneous conduction) between the output signal levels (active level) for one or more cycles with the following combinations of pins [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D — MTIOC6B and MTIOC6D — MTIOC7A and MTIOC7C — MTIOC7B and MTIOC7D [GPT output pins] — GTIOC0A-A and GTIOC0B-A — GTIOC1A-A and GTIOC1B-A — GTIOC2A-A and GTIOC2B-A • SPOER register setting being made • Detection that the main clock oscillator had stopped oscillating • Comparator output detection in the 12-bit A/D converter (S12ADA)	• Input signal detection: Detection of the POE0#, POE4#, POE8#, POE9#, POE10#, POE11#, POE12#, POE13#, and POE14# signal level. • Simultaneous conduction between output pins: A match (simultaneous conduction) between the output signal levels at the active level over one or more cycles on the following combination of pins [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D — MTIOC6B and MTIOC6D — MTIOC7A and MTIOC7C — MTIOC7B and MTIOC7D [GPTW output pins] — GTIOC0A and GTIOC0B — GTIOC1A and GTIOC1B — GTIOC2A and GTIOC2B — GTIOC4A and GTIOC4B — GTIOC5A and GTIOC5B — GTIOC6A and GTIOC6B — GTIOC7A and GTIOC7B — GTIOC8A and GTIOC8B — GTIOC9A and GTIOC9B • SPOER register setting being made • Detection that the main clock oscillator had stopped oscillating • Comparator output detection in the comparator C (CMPC)

Table 2.35 Comparison of Port Output Enable 3 Registers

Register	Bit	RX62T (POE3)	RX66T (POE3B)
ICSR1	POE0M[1:0] (RX62T) POE0M[3:0] (RX66T)	POE0 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE0# input. 0 1: Accepts a request when POE0# input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE0# input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE0# input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	POE0 mode select bits (b3 to b0) b3 b0 0 0 0 0: Accepts a request on the falling edge of POE0# pin input. 0 0 0 1: Samples the level of the POE0# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 0: Samples the level of the POE0# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 1: Samples the level of the POE0# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 0: Samples the level of the POE0# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 1: Samples the level of the POE0# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 1 0: Samples the level of the POE0# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified times. Settings other than the above are prohibited.
	POE0M2[3:0]	—	POE0 sampling count select bits

Register	Bit	RX62T (POE3)	RX66T (POE3B)
ICSR1	POE0F	POE0 flag [Setting condition] When the input set by POE0M[1:0] occurs at the POE0# pin [Clearing conditions] By writing 0 to POE0F after reading POE0F = 1	POE0 flag [Setting condition] When the input set by the POE0M[3:0] and POE0M2[3:0] bits occurs at the POE0# pin [Clearing condition] By writing 0 to the POE0F flag after reading POE0F = 1 When low-level sampling is set by the POE0M[3:0] bits, the high level needs to be input to the POE0# pin to write 0 to this flag.
ICSR2	POE4M[1:0] (RX62T) POE4M[3:0] (RX66T)	POE4 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE4# input. 0 1: Accepts a request when POE4# input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE4# input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE4# input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	POE4 mode select bits (b3 to b0) b3 b0 0 0 0 0: Accepts a request on the falling edge of POE4# pin input. 0 0 0 1: Samples the level of the POE4# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 0: Samples the level of the POE4# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 1: Samples the level of the POE4# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 0: Samples the level of the POE4# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 1: Samples the level of the POE4# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified times.

Register	Bit	RX62T (POE3)	RX66T (POE3B)
ICSR2	POE4M[1:0] (RX62T) POE4M[3:0] (RX66T)		0 1 1 0: Samples the level of the POE4# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified times. Settings other than the above are prohibited.
	POE4M2[3:0]	—	POE4 sampling count select bits
	POE4F	POE4 Flag [Setting condition] When the input set by POE4M[1:0] occurs at the POE4# pin [Clearing condition] By writing 0 to POE4F after reading POE4F = 1	POE4 Flag [Setting condition] When the input set by the POE4M[3:0] and POE4M2[3:0] bits occurs at the POE4# pin [Clearing condition] By writing 0 to POE4F after reading POE4F = 1 When low-level sampling is set by the POE4M[3:0] bits, the high level needs to be input to the POE4# pin to write 0 to this flag.
ICSR3	POE8M[1:0] (RX62T) POE8M[3:0] (RX66T)	POE8 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE8# input 0 1: Accepts a request when POE8# input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE8# input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE8# input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	POE8 mode select bits (b3 to b0) b3 b0 0 0 0 0: Accepts a request on the falling edge of POE8# pin input. 0 0 0 1: Samples the level of the POE8# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 0: Samples the level of the POE8# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 1: Samples the level of the POE8# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified times.

Register	Bit	RX62T (POE3)	RX66T (POE3B)
ICSR3	POE8M[1:0] (RX62T) POE8M[3:0] (RX66T)		0 1 0 0: Samples the level of the POE8# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 1: Samples the level of the POE8# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 1 0: Samples the level of the POE8# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified times. Settings other than the above are prohibited.
	POE8M2[3:0]	—	POE8 sampling count select bits
	POE8F	POE8 flag [Setting condition] When the input set by POE8M[1:0] occurs at the POE8# pin [Clearing condition] By writing 0 to POE8F after reading POE8F = 1	POE8 flag [Setting condition] When the input set by the POE8M[3:0] and POE8M2[3:0] bits occurs at the POE8# pin [Clearing condition] By writing 0 to the POE8F flag after reading POE8F = 1 When low-level sampling is set by the POE8M[3:0] bits, the high level needs to be input to the POE8# pin to write 0 to this flag.
ICSR4	POE10M[1:0] (RX62T) POE10M[3:0] (RX66T)	POE10 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE10# input 0 1: Accepts a request when POE10# input has been sampled 16 times at PCLK/8 clock pulses and all are low level.	POE10 mode select bits (b3 to b0) b3 b0 0 0 0 0: Accepts a request on the falling edge of POE10# pin input. 0 0 0 1: Samples the level of the POE10# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified times.

Register	Bit	RX62T (POE3)	RX66T (POE3B)
ICSR4	POE10M[1:0] (RX62T) POE10M[3:0] (RX66T)	1 0: Accepts a request when POE10# input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE10# input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	0 0 1 0: Samples the level of the POE10# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 1: Samples the level of the POE10# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 0: Samples the level of the POE10# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 1: Samples the level of the POE10# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 1 0: Samples the level of the POE10# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified times. Settings other than the above are prohibited.
	POE10M2[3:0]	—	POE10 sampling count select bits
	POE10F	POE10 Flag [Setting condition] When the input set by POE10M[1:0] occurs at the POE10# pin [Clearing condition] By writing 0 to POE10F after reading POE10F = 1	POE10 Flag [Setting condition] When the input set by the POE10M[3:0] and POE10M2[3:0] bits occurs at the POE10# pin [Clearing condition] By writing 0 to the POE10F flag after reading POE10F = 1 When low-level sampling is set by the POE10M[3:0] bits, the high level needs to be input to the POE10# pin to write 0 to this flag.

Register	Bit	RX62T (POE3)	RX66T (POE3B)
ICSR5	POE11M[1:0] (RX62T) POE11M[3:0] (RX66T)	POE11 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE11# input 0 1: Accepts a request when POE11# input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE11# input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE11# input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	POE11 mode select bits (b3 to b0) b3 b0 0 0 0 0: Accepts a request on the falling edge of POE11# pin input. 0 0 0 1: Samples the level of the POE11# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 0: Samples the level of the POE11# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 1: Samples the level of the POE11# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 0: Samples the level of the POE11# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 1: Samples the level of the POE11# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 1 0: Samples the level of the POE11# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified times. Settings other than the above are prohibited.
	POE11M2[3:0]	—	POE11 sampling count select bits

Register	Bit	RX62T (POE3)	RX66T (POE3B)
ICSR5	POE11F	POE11 Flag [Setting condition] When the input set by POE11M[1:0] occurs at the POE11# pin [Clearing condition] By writing 0 to POE11F after reading POE11F = 1	POE11 Flag [Setting condition] When the input set by the POE11M[3:0] and POE11M2[3:0] bits occurs at the POE11# pin [Clearing condition] By writing 0 to the POE11F flag after reading POE11F = 1 When low-level sampling is set by the POE11M[3:0] bits, the high level needs to be input to the POE11# pin to write 0 to this flag.
ICSR6	—	—	Input level control/status register 6
ICSR7	—	—	Input level control/status register 7
ICSR8	—	—	Input level control/status register 8
ICSR9	—	—	Input level control/status register 9
ICSR10	—	—	Input level control/status register 10
OCSR1	OSF1	Output short flag 1 This flag indicates that any one of the three pairs of two-phase MTU3 and MTU4 pins for MTU complementary PWM output or GPT0 to GPT2 pins for the GPT large-current output to be compared has simultaneously become an active level. [Setting condition] When any one of the three pairs of two-phase outputs has simultaneously become an active level	Simultaneous conduction flag 1 This flag indicates that at least one of the three pairs of two-phase output pins for MTU complementary PWM output (MTU3 and MTU4) has simultaneously become active level. If the output disabling control for the corresponding pins is not enabled, this flag does not become 1. [Setting condition] • When the MTIOC3B and MTIOC3D pins simultaneously go to the active level for at least one cycle of PCLK while the value of the POECR2.MTU3BDZE bit, or either or both of the PMMCR1.MTU3BME and PMMCR1.MTU3DME bits, is 1.

Register	Bit	RX62T (POE3)	RX66T (POE3B)
OCSR1	OSF1	[Clearing condition] By writing 0 to OSF1 after reading OSF1 = 1	• When the MTIOC4A and MTIOC4C pins simultaneously go to the active level for at least one cycle of PCLK while the value of the POECR2.MTU4ACZE bit, or either or both of the PMMCR1.MTU4AME and PMMCR1.MTU4CME bits, is 1. • When the MTIOC4B and MTIOC4D pins simultaneously go to the active level for at least one cycle of PCLK while the value of the POECR2.MTU4BDZE bit, or either or both of the PMMCR1.MTU4BME and PMMCR1.MTU4DME bits, is 1. [Clearing condition] By writing 0 to the OSF1 flag after reading OSF1 = 1 To write 0 to this flag, the inactive level needs to be output from the MTU complementary PWM output pins.
OCSR2	OSF2	Output short flag 2 This flag indicates that any one of the three pairs of two-phase MTU6 and MTU7 pins for MTU complementary PWM output to be compared has simultaneously become an active level. [Setting condition] When any one of the three pairs of two-phase outputs has simultaneously become an active level	Simultaneous conduction flag 2 This flag indicates that at least one of the three pairs of two-phase output pins for MTU complementary PWM output (MTU6 and MTU7) has simultaneously become active level. If the output disabling control for the corresponding pins is not enabled, this flag does not become 1. [Setting condition] • When the MTIOC6B and MTIOC6D pins simultaneously go to the active level for at least one cycle of PCLK while the value of the POECR2.MTU6BDZE bit, or either or both of the PMMCR1.MTU6BME and PMMCR1.MTU6DME bits, is 1.

Register	Bit	RX62T (POE3)	RX66T (POE3B)
OCSR2	OSF2	[Clearing condition] By writing 0 to OSF2 after reading OSF2 = 1	• When the MTIOC7A and MTIOC7C pins simultaneously go to the active level for at least one cycle of PCLK while the value of the POECR2.MTU7ACZE bit, or either or both of the PMMCR1.MTU7AME and PMMCR1.MTU7CME bits, is 1. • When the MTIOC7B and MTIOC7D pins simultaneously go to the active level for at least one cycle of PCLK while the value of the POECR2.MTU7BDZE bit, or either or both of the PMMCR1.MTU7BME and PMMCR1.MTU7DME bits, is 1. [Clearing condition] By writing 0 to the OSF2 flag after reading OSF2 = 1 To write 0 to this flag, the inactive level needs to be output from MTU complementary PWM output pins.
OCSR3	—	—	Output level control/status register 3
OCSR4	—	—	Output level control/status register 4
OCSR5	—	—	Output level control/status register 5
ALR1	OLSG0A	MTIOC3B/GTIOC0A-A active level setting bit	MTIOC3B pin active level setting bit
	OLSG0B	MTIOC3D/GTIOC0B-A active level setting bit	MTIOC3D pin active level setting bit
	OLSG1A	MTIOC4A/GTIOC1A-A active level setting bit	MTIOC4A pin active level setting bit
	OLSG1B	MTIOC4C/GTIOC1B-A active level setting bit	MTIOC4C pin active level setting bit
	OLSG2A	MTIOC4B/GTIOC2A-A active level setting bit	MTIOC4B pin active level setting bit
	OLSG2B	MTIOC4D/GTIOC2B-A active level setting bit	MTIOC4D pin active level setting bit
ALR2	—	—	Active level setting register 2
ALR3	—	—	Active level setting register 3
ALR4	—	—	Active level setting register 4
ALR5	—	—	Active level setting register 5

Register	Bit	RX62T (POE3)	RX66T (POE3B)
SPOER	MTUCH34HIZ*1	MTU3 and MTU4 output high-impedance enable bit	MTU3 and MTU4 pin output disable bit
	GPT01HIZ	GPT0 and GPT1 output high-impedance enable bit	GPTW0 and GPTW1 pin output disable bit
	GPT23HIZ	GPT2 and GPT3 output high-impedance enable bit	GPTW2 and GPTW3 pin output disable bit
	MTUCH9HIZ	—	MTU9 pin output disable bit
	GPT02HIZ	—	GPTW0 to GPTW2 pin output disable bit
	GPT46HIZ	—	GPTW4 to GPTW6 pin output disable bit
	GPT79HIZ	—	GPTW7 to GPTW9 pin output disable bit
POECR2	MTU4BDZE*1	MTU CH4BD high-impedance enable bit	MTIOC4B/MTIOC4D pin high-impedance enable bit
	MTU4ACZE*1	MTU CH4AC high-impedance enable bit	MTIOC4A/MTIOC4C pin high-impedance enable bit
	MTU3BDZE*1	MTU CH3BD high-impedance enable bit	MTIOC3B/MTIOC3D pin high-impedance enable bit
POECR3	—	Port output enable control register 3	Port output enable control register 3
		Initial values after a reset are different.	
	GPT2ABZE	GPT CH2AB high-impedance enable bit (b8)	GTIOC2A/GTIOC2B pin high-impedance enable bit (b2)
	GPT3ABZE	GPT CH3AB high-impedance enable bit (b9)	GTIOC3A/GTIOC3B pin high-impedance enable bit (b3)
	GPT4ABZE to GPT9ABZE	—	GTIOC4A/GTIOC4B to GTIOC9A/GTIOC9B pin high-impedance enable bit
POECR4	CMADDMT34ZE*1	MTU CH34 high-impedance CFLAG add bit	MTU3 and MTU4 output disabling condition CFLAG add bit
	IC1ADDMT34ZE	—	MTU3 and MTU4 output disabling condition POE0F add bit
	IC2ADDMT34ZE*1	MTU CH34 high-impedance POE4F add bit	MTU3 and MTU4 output disabling condition POE4F add bit
	IC3ADDMT34ZE*1	MTU CH34 high-impedance POE8F add bit	MTU3 and MTU4 output disabling condition POE8F add bit
	IC4ADDMT34ZE*1	MTU CH34 high-impedance POE10F add bit	MTU3 and MTU4 output disabling condition POE10F add bit
	IC5ADDMT34ZE*1	MTU CH34 high-impedance POE11F add bit	MTU3 and MTU4 output disabling condition POE11F add bit
	IC6ADDMT34ZE	—	MTU3 and MTU4 output disabling condition POE12F add bit
	IC8ADDMT34ZE	—	MTU3 and MTU4 output disabling condition POE9F add bit
	IC9ADDMT34ZE	—	MTU3 and MTU4 output disabling condition POE13F add bit
	IC10ADDMT34ZE	—	MTU3 and MTU4 output disabling condition POE14F add bit
	CMADDMT67ZE	MTU CH67 high-impedance CFLAG add bit	—

Register	Bit	RX62T (POE3)	RX66T (POE3B)
POECR4	IC1ADDMT67ZE	MTU CH67 high-impedance POE0F add bit	—
	IC3ADDMT67ZE	MTU CH67 high-impedance POE8F add bit	—
	IC4ADDMT67ZE	MTU CH67 high-impedance POE10F add bit	—
	IC5ADDMT67ZE	MTU CH67 high-impedance POE11F add bit	—
POECR4B	—	—	Port Output enable control register 4B
POECR5	IC3ADDMT0ZE	—	MTU0 Output disabling condition POE8F add bit
	IC6ADDMT0ZE	—	MTU0 output disabling condition POE12F add bit
	IC8ADDMT0ZE	—	MTU0 output disabling condition POE9F add bit
	IC9ADDMT0ZE	—	MTU0 output disabling condition POE13F add bit
	IC10ADDMT0ZE	—	MTU0 output disabling condition POE14F add bit
POECR6	IC4ADDGPT01ZE	—	GPTW0 and GPTW1 output disabling condition POE10F add bit
	IC6ADDGPT01ZE	—	GPTW0 and GPTW1 output disabling condition POE12F add bit
	IC8ADDGPT01ZE	—	GPTW0 and GPTW1 output disabling condition POE9F add bit
	IC9ADDGPT01ZE	—	GPTW0 and GPTW1 output disabling condition POE13F add bit
	IC10ADDGPT01ZE	—	GPTW0 and GPTW1 output disabling condition POE14F add bit
	CMADDGPT23ZE	GPT CH23 high-impedance CFLAG add bit	—
	IC1ADDGPT23ZE	GPT CH23 high-impedance POE0F add bit	—
	IC2ADDGPT23ZE	GPT CH23 high-impedance POE4F add bit	—
	IC3ADDGPT23ZE	GPT CH23 high-impedance POE8F add bit	—
	IC4ADDGPT23ZE	GPT CH23 high-impedance POE10F add bit	—
POECR6B	—	—	Port output enable control register 6B
POECR7	—	—	Port output enable control register 7
POECR8	—	—	Port output enable control register 8
POECR9	—	—	Port output enable control register 9

Register	Bit	RX62T (POE3)	RX66T (POE3B)
POECR10	—	—	Port output enable control register 10
POECR11	—	—	Port output enable control register 11
PMMCR0	—	—	Port mode mask control register 0
PMMCR1	—	—	Port mode mask control register 1
PMMCR2	—	—	Port mode mask control register 2
PMMCR3	—	—	Port mode mask control register 3
POECMPFR	—	—	Port output enable comparator output detection flag register
POECMPSEL	—	—	Port output enable comparator request select register
POECMPEXm	—	—	Port output enable comparator request extended selection register m (m = 0 to 8)
M0SELR1	—	—	MTU0 pin select register 1
M0SELR2	—	—	MTU0 pin select register 2
M3SELR	—	—	MTU3 pin select register
M4SELR1	—	—	MTU4 pin select register 1
M4SELR2	—	—	MTU4 pin select register 2
M6SELR	—	—	MTU6 pin select register
M7SELR1	—	—	MTU7 pin select register 1
M7SELR2	—	—	MTU7 pin select register 2
M9SELR1	—	—	MTU9 pin select register 1
M9SELR2	—	—	MTU9 pin select register 2
G0SELR	—	—	GPTW0 pin select register
G1SELR	—	—	GPTW1 pin select register
G2SELR	—	—	GPTW2 pin select register
G3SELR	—	—	GPTW3 pin select register
G4SELR	—	—	GPTW4 pin select register
G5SELR	—	—	GPTW5 pin select register
G6SELR	—	—	GPTW6 pin select register
G7SELR	—	—	GPTW7 pin select register
G8SELR	—	—	GPTW8 pin select register
G9SELR	—	—	GPTW9 pin select register

Note: 1. The GPT and MTU pins are controlled by this register on the RX62T, but the GPT and MTU pins are controlled by separate registers on the RX66T.

2.16 General PWM Timer

Table 2.36 is a comparative overview of general PWM timers, Table 2.37 is a comparison of general PWM timer registers, and Table 2.38 is a comparative listing of GTIOA and GTIOB bit settings.

The GPTa is implemented on the RX62G Group only.

Table 2.36 Comparative Overview of General PWM Timer

Item	RX62T (GPT/GPTa)	RX66T (GPTW)
Functions	• 16 bits × 4 channels • Up-count or down-count operation (saw waves) or up/down-count operation (triangle waves) for each counter. • Clock sources independently selectable for each channel • Two input/output pins per channel • Two output compare/input capture registers per channel • For the two output compare/input capture registers of each channel, four registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms. • Registers for setting up frame cycles in each channel (with capability for generating interrupts at overflow or underflow) • Synchronizable operation of the several counters • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Operation of count start/count stop/counter clearing by an external trigger • Output disable function by a dead time error, detection of short-circuited output, or comparator-detection	• 32 bits × 10 channels • Up-counting or down-counting (saw waves) or up/down-counting (triangle waves) for each counter. • Clock sources independently selectable for each channel • Two I/O pins per channel • Two output compare/input capture registers per channel • For the two output compare/input capture registers of each channel, four registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms. • Registers for setting up frame cycles in each channel (with capability for generating interrupts at overflow or underflow) • Simultaneous start/stop/clearing of desired channel counters • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Operation of count start/count stop/counter clearing/up-counting/down-counting/input capture by maximum of eight ELC events based on the ELC setting • Operation of count start/count stop/counter clearing/up-counting/down-counting/input capture by detecting two input signal conditions • Operation of count start/count stop/counter clearing/up-counting/down-counting/input capture by maximum of four external triggers • Function to control output negation by requests for disabling of output from the POEG

Item	RX62T (GPT/GPTa)	RX66T (GPTW)
Functions	• A/D converter start trigger generation function	• A/D converter start trigger generation function • Event signals for compare match A to F and for overflow/underflow can be output to the ELC • Input capture input can select noise filter function • Bus clock: PCLKA, GPTW count reference clock: PCLKC, Frequency ratio between PCLKA and PCLKC = 1: N (N = 1/2)
	• Through combination of three counters, generation of three-phase PWM waveforms incorporating dead times • Starting, clearing, and stopping counters in response to external or internal triggers • Internal trigger sources: output of the comparator detection, software, and compare match • The frequency-divided system clock (ICLK) can be used as a counter clock for measuring timing of the edges of signals produced by frequency-dividing the IWDT-dedicated low-speed on-chip oscillator clock signal (to detect abnormal oscillation). • PWM delay generation can control the timing with which signals on the two PWM output pins for each channel rise and fall to an accuracy of up to 1/32 times the period of the system clock (ICLK) (only for the RX62G Group).	• Through combination of three counters, generation of three-phase PWM waveforms incorporating dead times • Starting, clearing, and stopping counters in response to external or internal triggers • Internal trigger sources: output of software, and compare match • Monitors the clock output from the main clock oscillator, low- and high-speed on-chip oscillators, the PLL frequency synthesizer, IWDT-dedicated on-chip oscillator, and PCLKB (refer to the Clock Frequency Accuracy Measurement Circuit (CAC) chapter.) • Capable of adjusting rising/falling timing at PWM waveforms with resolution of PCLKC cycles × 1/32 for maximum of 4 channels of complementary PWM output pins (refer to the High Resolution PWM Waveform Generation Circuit (HRPWM) chapter.)

Table 2.37 Comparison of General PWM Timer Registers

Register	Bit	RX62T (GPT/GPTa)	RX66T (GPTW)
GTWP	WP0 to WP3 (RX62T) WP (RX66T)	GPT0 to GPT3 register write enable bits	Register write disabled bits
	STRWP	—	GTSTR.CSTRT bit write disabled bit
	STPWP	—	GTSTP.CSTOP bit write disabled bit
	CLRWP	—	GTCLR.CCLR bit write disabled bit
	CMNWP	—	Common Register write disabled bit
	PRKEY[7:0]	—	GTWP key code
GTSTR	CST0 (RX62T) CSTRT0 (RX66T)	GPT0.GTCNT count start bit	Channel 0 count start bit
	CST1 (RX62T) CSTRT1 (RX66T)	GPT1.GTCNT count start bit	Channel 1 count start bit
	CST2 (RX62T) CSTRT2 (RX66T)	GPT2.GTCNT count start bit	Channel 2 count start bit
	CST3 (RX62T) CSTRT3 (RX66T)	GPT3.GTCNT count start bit	Channel 3 count start bit
	CSTRT4 to CSTRT9	—	Channel 4 count start to channel 9 count start bits
GTSTP	—	—	General PWM timer software stop register
GTHSCR	—	General PWM timer hardware source start control register	—
GTHCCR	—	General PWM timer hardware source clear control register	—
GTCLR	—	—	General PWM timer software clear register
GTHSSR	—	General PWM timer hardware start source select register	—
GTSSR	—	—	General PWM timer start source select register
GTHPSR	—	General PWM timer hardware stop/clear source select register	—
GTPSR	—	—	General PWM timer stop source select register
GTCSR	—	—	General PWM timer clear source select register
GTUPSR	—	—	General PWM timer count-up source select register
GTDNSR	—	—	General PWM timer count-down source select register
GTICASR	—	—	General PWM timer input capture source select register A

Register	Bit	RX62T (GPT/GPTa)	RX66T (GPTW)
GTICBSR	—	—	General PWM timer input capture source select register B
GTSYNC	—	General PWM timer sync register	—
GTETINT	—	General PWM timer external trigger input interrupt register	—
GTBDR	—	General PWM timer buffer operation disable register	—
GTSWP	—	General PWM timer start write protection register	—
LCCR	—	LOCO count control register	—
LCST	—	LOCO count status register	—
LCNT	—	LOCO count value register	—
LCNTA	—	LOCO count result average register	—
LCNTn	—	LOCO count result register n (n = 0 to 15)	—
LCNTDU, LCNTDL	—	LOCO count upper/lower permissible deviation register	—
GTCR	CST	—	Count start bit
	ICDS	—	Input capture operation select at count stop bit
	MD[2:0]	Mode select bit (b2 to b0)	Mode select bit (b18 to b16)
	TPCS[1:0] (RX62T) TPCS[3:0] (RX66T)	Timer prescaler select bits (b9, b8) b9 b8 0 0: ICLK (system clock) 0 1: ICLK/2 (system clock/2) 1 0: ICLK/4 (system clock/4) 1 1: ICLK/8 (system clock/8)	Timer prescaler select bits (b26 to b23) b26 b23 0 0 0 0: PCLKC 0 0 0 1: PCLKC/2 0 0 1 0: PCLKC/4 0 0 1 1: PCLKC/8 0 1 0 0: PCLKC/16 0 1 0 1: PCLKC/32 0 1 1 0: PCLKC/64 0 1 1 1: Setting prohibited 1 0 0 0: PCLKC/256 1 0 0 1: Setting prohibited 1 0 1 0: PCLKC/1024 1 0 1 1: Setting prohibited 1 1 0 0: GTETRGA (via the POEG) 1 1 0 1: GTETRGB (via the POEG) 1 1 1 0: GTETRGC (via the POEG) 1 1 1 1: GTETRGD (via the POEG)
	CCLR[1:0]	Counter clear source select bits	—
GTUDC	—	General PWM timer count direction register	—
GTUDDTYC	—	—	General PWM timer count direction and duty setting register

Register	Bit	RX62T (GPT/GPTa)	RX66T (GPTW)
GTIOR	GTIOA[5:0] (RX62T) GTIOA[4:0] (RX66T)	GTIOCnA pin function select bits (b5 to b0) Refer to Table 2.38 for details.	GTIOCnA pin function select bits (b4 to b0) Refer to Table 2.38 for details.
	OAE	—	GTIOCnA pin output enable bit
	OADF[1:0]	—	GTIOCnA pin negate value setting bits
	NFAEN	—	GTIOCnA pin input noise filter enable bit
	NFCSA[1:0]	—	GTIOCnA pin input noise filter sampling clock select bits
	GTIOB[5:0] (RX62T) GTIOB[4:0] (RX66T)	GTIOCnB pin function select bits (b13 to b8) Refer to Table 2.38 for details.	GTIOCnB pin function select bits (b20 to b16) Refer to Table 2.38 for details.
	OBDFLT	Output value at GTIOCnB pin count stop bit (b14)	GTIOCnB pin output value setting at the count stop bit (b22)
	OBHLD	Output retain at GTIOCnB pin count start/stop bit (b15)	GTIOCnB pin output retention at the start/stop count bit (b23)
	OBE	—	GTIOCnB pin output enable bit
	OBDF[1:0]	—	GTIOCnB pin negate value Setting bits
	NFBEN	—	GTIOCnB pin input noise filter Enable bit
	NFCSB[1:0]	—	GTIOCnB pin input noise filter sampling clock select bits
GTINTAD	EINT	Dead time error interrupt enable bit	—
	ADTRAUEN	GTADTRA compare match (up-counting) A/D converter start request enable bit (b12)	GTADTRA register compare match (up-counting) A/D converter start request enable bit (b16)
	ADTRADEN	GTADTRA Compare match (down-counting) A/D converter start request enable bit (b13)	GTADTRA register compare match (down-counting) A/D converter start request enable bit (b17)
	ADTRBUEN	GTADTRB compare match (up-counting) A/D converter start request enable bit (b14)	GTADTRB register compare match (up-counting) A/D converter start request enable bit (b18)
	ADTRBDEN	GTADTRB compare match (down-counting) A/D converter start request enable bit (b15)	GTADTRB register compare match (down-counting) A/D converter start request enable bit (b19)
	GRP[1:0]	—	Output stop group select bits
	GRPDTE	—	Dead time error output stop detection enable bit
	GRPABH	—	Simultaneous high output stop detection enable bit
	GRPABL	—	Simultaneous low output stop detection enable bit

Register	Bit	RX62T (GPT/GPTa)	RX66T (GPTW)
GTST	TCFA	Input capture/compare match flag A	—
	TCFB	Input capture/compare match flag B	—
	TCFC to TCFF	Compare match flag C to compare match flag F	—
	TCFPO	Overflow flag	—
	TCFPU	Underflow flag	—
	ITCNT[2:0]	GTCIV interrupt skipping count counter	GTCIV/GTCIU interrupt skipping count counter
	DTEF	Dead time error flag (b11)	Dead time error flag (b28)
	ADTRAUF	—	GTADTRA register compare match (up-counting) A/D converter start request flag
	ADTRADF	—	GTADTRA register compare match (down-counting) A/D converter start request flag
	ADTRBUF	—	GTADTRB register compare match (up-counting) A/D converter start request flag
	ADTRBDF	—	GTADTRB register compare match (down-counting) A/D converter start request flag
	ODF	—	Output stop request flag
	OABHF	—	Simultaneous high output flag
	OABLF	—	Simultaneous low output flag
GTBER	BD[0]	—	GTCCRA/GTCCRB registers buffer operation disable bit
	BD[1]	—	GTPR Register buffer operation disable bit
	BD[2]	—	GTADTRA/GTADTRB registers buffer operation disable bit
	BD[3]	—	GTDVU/GTDVD registers buffer operation disable bit
	DBRTECA	—	GTCCRA register double buffer repeat operation enable bit
	DBRTECB	—	GTCCRB register double buffer repeat operation enable bit
	CCRA[1:0]	GTCCRA buffer operation bits (b1, b0)	GTCCRA register buffer operation bits (b17, b16)
	CCRB[1:0]	GTCCRB buffer operation bits (b3, b2)	GTCCRB register buffer Operation bits (b19, b18)
	PR[1:0]	GTPR buffer operation bits (b5, b4)	GTPR register buffer operation bits (b21, b20)
	CCRSWT	GTCCRA and GTCCRB forcible buffer operation bit (b6)	GTCCRA and GTCCRB registers forcible buffer operation bit (b22)
	ADTTA[1:0]	GTADTRA buffer transfer timing select bits (b9, b8)	GTADTRA register buffer transfer timing select bits (b25, b24)
	ADTDA	GTADTRA double buffer operation bit (b10)	GTADTRA register double buffer operation bit (b26)
	ADTTB[1:0]	GTADTRB buffer transfer timing select bits (b13, b12)	GTADTRB register buffer transfer timing select bits (b29, b28)

Register	Bit	RX62T (GPT/GPTa)	RX66T (GPTW)
GTBER	ADTDB	GTADTRB double buffer operation bit (b14)	GTADTRB register double buffer operation bit (b30)
GTITC	IVTC[1:0]	GTCIV interrupt skipping function select bits	GTCIV/GTCIU interrupt skipping function select bits
	IVTT[2:0]	GTCIV interrupt skipping count select bits	GTCIV/GTCIU interrupt skipping count select bits
GTCNT	—	General PWM timer counter GTCNT is a 16-bit register. Access in 8-bit units is prohibited. GTCNT should always be accessed in 16-bits.	General PWM timer counter GTCNT is a 32-bit register. Access in 8-bit or 16-bit units to GTCNT is prohibited. GTCNT should be accessed in 32-bit units.
GTCCRm	—	General PWM timer compare capture register m (m = A to F) GTCCRm is a 16-bit register.	General PWM timer compare capture register m (m = A to F) GTCCRm is a 32-bit register. Access in 8-bit or 16-bit units to GTCCRm is prohibited. GTCCRm should be accessed in 32-bit units.
GTPR	—	General PWM timer cycle setting register GTPR is a 16-bit register.	General PWM timer period setting register GTPR is a 32-bit register. Access in 8-bit or 16-bit units to GTPR is prohibited. GTPR should be accessed in 32-bit units.
GTPBR	—	General PWM timer cycle setting buffer register GTPBR is a 16-bit register.	General PWM timer period setting buffer register GTPBR is a 32-bit register. Access in 8-bit or 16-bit units to GTPBR is prohibited. GTPBR should be accessed in 32-bit units.
GTPDBR	—	General PWM timer cycle setting double-buffer register GTPDBR is a 16-bit register.	General PWM timer period setting double-buffer register GTPDBR is a 32-bit register. Access in 8-bit or 16-bit units to GTPDBR is prohibited. GTPDBR should be accessed in 32-bit units.
GTADTRm	—	A/D converter start request timing register m (m = A, B) GTADTRm is a 16-bit register. Access in 8-bit units is prohibited. GTADTRm should always be accessed in 16-bits.	A/D converter start request timing register m (m = A, B) GTADTRm is a 32-bit register. Access in 8-bit or 16-bit units to GTADTRm is prohibited. GTADTRm should be accessed in 32-bit units.

Register	Bit	RX62T (GPT/GPTa)	RX66T (GPTW)
GTADTBRm	—	A/D converter start request timing buffer register m (m = A, B) GTADTBRm is a 16-bit register. Access in 8-bit units is prohibited. GTADTBRm should always be accessed in 16-bits.	A/D converter start request timing buffer register m (m = A, B) GTADTBRm is a 32-bit register. Access in 8-bit or 16-bit units to GTADTBRm is prohibited. GTADTBRm should be accessed in 32-bit units.
GTADTDBRm	—	A/D converter start request timing double-buffer register m (m = A, B) GTADTDBRm is a 16-bit register. Access in 8-bit units is prohibited. GTADTDBRm should always be accessed in 16-bits.	A/D converter start request timing double-buffer register m (m = A, B) GTADTDBRm is a 32-bit register. Access in 8-bit or 16-bit units to GTADTDBRm is prohibited. GTADTDBRm should be accessed in 32-bit units.
GTDVm	—	General PWM timer dead time value register m (m = U, D) GTDVm is a 16-bit register. Access in 8-bit units is prohibited. GTDVm should always be accessed in 16-bits.	General PWM timer dead time value register m (m = U, D) GTDVm is a 32-bit register. Access in 8-bit or 16-bit units to GTDVm is prohibited. GTDVm should be accessed in 32-bit units.
GTDBm	—	General PWM timer dead time buffer register m (m = U, D) GTDBm is a 16-bit register. Access in 8-bit units is prohibited. GTDBm should always be accessed in 16-bits.	General PWM timer dead time value buffer register m (m = U, D) GTDBm is a 32-bit register. Access in 8-bit or 16-bit units to GTDBm is prohibited. GTDBm should be accessed in 32-bit units.
GTONCR	—	General PWM timer output negate control register	—
GTADSMR	—	—	General PWM timer A/D converter start request signal monitoring register
GTEITC	—	—	General PWM timer extended interrupt skipping counter control register
GTEITLI1	—	—	General PWM timer extended interrupt skipping setting register 1
GTEITLI2	—	—	General PWM timer extended interrupt skipping setting register 2
GTEITLB	—	—	General PWM timer extended buffer transfer skipping setting register
GTSECSR	—	—	General PWM timer operation enable bit simultaneous control channel select register

Register	Bit	RX62T (GPT/GPTa)	RX66T (GPTW)
GTSECR	—	—	General PWM timer operation enable bit simultaneous control register
GTDLYCR	—	PWM output delay control register	—
GTDLYRA	—	GTIOCA rising output delay register	—
GTDLYFA	—	GTIOCA falling output delay register	—
GTDLYRB	—	GTIOCB rising output delay register	—
GTDLYFB	—	GTIOCB falling output delay register	—

Table 2.38 Comparative Listing of GTIOA and GTIOB Bit Settings

Bit	RX62T (GPT/GPTa) GTIOA/GTIOB[5:0] Bits	RX66T (GPTW) GTIOA/GTIOB[4:0] Bits
b5	0: Compare match 1: Input capture	—
b4	• When b5 = 0 0: Initial output is low-level 1: Initial output is high-level • When b5 = 1 x: Don't care	0: Initial output is low-level 1: Initial output is high-level
b3, b2	• When b5 = 0 0 0: Output retained at cycle end 0 1: Low-level output at cycle end 1 0: High-level output at cycle end 1 1: Toggle output at cycle end • When b5 = 1 x: Don't care	0 0: Output retained at cycle end 0 1: Low-level output at cycle end 1 0: High-level output at cycle end 1 1: Toggle output at cycle end
b1, b0	• When b5 = 0 0 0: Output retained at GPTn.GTCCRA/GPTn.GTCCRB compare match 0 1: Low-level output at GPTn.GTCCRA/GPTn.GTCCRB compare match 1 0: High-level output at GPTn.GTCCRA/GPTn.GTCCRB compare match 1 1: Toggle output at GPTn.GTCCRA/GPTn.GTCCRB compare match • When b5 = 1 0 0: Input capture at rising edge 0 1: Input capture at falling edge 1 0: Input capture at both edges 1 1: Input capture at both edges	0 0: Output retained at GTCCRA/GTCCRB register compare match 0 1: Low-level output at GTCCRA/GTCCRB register compare match 1 0: High-level output at GTCCRA/GTCCRB register compare match 1 1: Toggle output at GTCCRA/GTCCRB register compare match

2.17 Compare Match Timer

Table 2.39 is a comparative overview of compare match timer.

Table 2.39 Comparative Overview of Compare Match Timer

Item	RX62T (CMT)	RX66T (CMT)
Count clocks	Four internal clocks: One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected individually for each channel.	Four frequency dividing clocks: One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.
Interrupt	A compare match interrupt can be requested individually for each channel.	A compare match interrupt can be requested for each channel.
Event link function (output)	—	An event signal is output upon a CMT1 compare match.
Event link function (input)	—	• Linking to the specified module is possible. • CMT1 count start, event counter, or count restart operation is possible.
Low power consumption function	Each unit can be placed in a module stop state.	Each unit can be placed in a module stop state.

2.18 Watchdog Timer

Table 2.40 is a comparative overview of watchdog timers, and Table 2.41 is a comparison of watchdog timer registers.

Table 2.40 Comparative Overview of Watchdog Timers

Item	RX62T (WDT)	RX66T (WDTA)
Count source	Peripheral module clock (PCLK)	Peripheral module clock (PCLK)
Count clocks	PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192, PCLK/32768, and PCLK/131072	PCLK divide by 4, 64, 128, 512, 2048, or 8192
Counter operation	Counting up using a 8-bit up-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Watchdog timer mode: The TCSR.TMS bit is set to 1 (Watchdog timer mode) and the TCSR.TME bit is set to 1 (TCNT starts counting) • Interval timer mode: The TCSR.TMS bit is set to 0 (interval timer mode) and the TCSR.TME bit is set to 1 (TCNT starts counting)	• Auto-start mode: Counting automatically starts after a reset is released • Register start mode: Counting is started by refresh operation (writing 00h and then FFh to the WDTRR register)
Conditions for stopping the counter	• Reset (up-counter and other registers return to their initial values) • A counter overflows • When the value of the TCSR.TME bit is 0. (The TCNT counter is initializes to 00h.)	• Reset (down-counter and other registers return to their initial values) • In low power consumption states • A counter underflows or a refresh error occurs (only in register start mode)
Window function	—	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Watchdog timer reset sources	It is possible to select whether or not the WDTOVF# signal is output externally and the microcontroller is simultaneously reset internally when the counter overflows in watchdog timer mode.	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt/ interrupt sources	In interval timer mode, an interval timer interrupt (WOVI) is generated when the TCNT counter overflows.	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	The up-counter value can be read by the TCNT register.	The down-counter value can be read by the WDTSR register.

Item	RX62T (WDT)	RX66T (WDTA)
Number of channels	8 bits × 1 channel	14 bits × 1 channel
Operating modes	Switchable between watchdog timer mode and interval timer mode	Switchable between auto-start mode and register-start mode

Table 2.41 Comparison of Watchdog Timer Registers

Register	Bit	RX62T (WDT)	RX66T (WDTA)
TCNT	—	Timer counter	—
WDTRR	—	—	WDT refresh register
TCSR	—	Timer control/status register	—
WDTCR	—	—	WDT control register
RSTCSR	—	Reset control/status register	—
WDTSR	—	—	WDT status register
WINA	—	Write window A register	—
WINB	—	Write window B register	—
WDTRCR	—	—	WDT reset control register

2.19 Independent Watchdog Timer

Table 2.42 is a comparative overview of independent watchdog timer, and Table 2.43 is a comparison of independent watchdog timer registers.

Table 2.42 Comparative Overview of Independent Watchdog Timer

Item	RX62T (IWDT)	RX66T (IWDTa)
Count source	On-chip oscillator clock (IWDTCLK)	IWDT-dedicated clock (IWDTCLK)
Clock divide ratio	IWDTCLK, IWDTCLK/16, IWDTCLK/32, IWDTCLK/64, IWDTCLK/128, IWDTCLK/256	Divide by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down by a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	Counting can be started by refreshing the down-counter (write FFh after 00h has been written to the IWDTRR register).	• Auto-start mode: Counting automatically starts after a reset is released • Register start mode: Counting is started by refresh operation (writing 00h and then FFh to the IWDTRR register).
Conditions for stopping the counter	• Pin reset (the down-counter and other registers return to their initial values) • Generation of an underflow	• Reset (the down-counter and other registers return to their initial values) • In low power consumption states (depends on the register setting) • A counter underflows or a refresh error occurs (only in register start mode)
Window function	—	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Reset output sources	Underflow of the down-counter	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt/ interrupt sources	—	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	The value reached in counting by the down-counter can be read out from a register (the IWDTSR).	The down-counter value can be read by the IWDTSR register.
Output signal (internal signal)	Reset output	• Reset output • Interrupt request output • Sleep mode count stop control output

Item	RX62T (IWDT)	RX66T (IWDTa)
Auto-start mode (controlled by option function select register 0 (OFS0))	—	• Selecting the clock frequency divide ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)
Event link function (output)	—	• Down-counter underflow event output • Refresh error event output
Register start mode (controlled by the IWDT registers)	• Selecting the clock frequency divide ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits)	• Selecting the clock frequency divide ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)

Table 2.43 Comparison of Independent Watchdog Timer Registers

Register	Bit	RX62T (IWDT)	RX66T (IWDTa)
IWDTCR	—	IWDT control register	IWDT control register
		Initial values after a reset are different.	
	CKS[3:0]	Clock selection bits b7 b4 0 0 — : IWDTCLK 0 1 0 0: IWDTCLK/16 0 1 0 1: IWDTCLK/32 0 1 1 0: IWDTCLK/64 0 1 1 1: IWDTCLK/128 1 ——: IWDTCLK/256	Clock frequency dividing ratio selection bits b7 b4 0 0 0 0: No frequency division 0 0 1 0: Division by 16 0 0 1 1: Division by 32 0 1 0 0: Division by 64 0 1 0 1: Division by 256 1 1 1 1: Division by 128
	RPES[1:0]	—	Window end position select bits
	RPSS[1:0]	—	Window start position select bits
IWDTSR	REFEF	—	Refresh error flag
IWDTRCR	—	—	IWDT reset control register
IWDTCSTPR	—	—	IWDT count stop control register

2.20 Serial Communications Interface

Table 2.44 is a comparative overview of serial communications interfaces, Table 2.45 is a comparative listing of serial communications interface channels, and Table 2.46 is a comparison of serial communications interface registers.

Table 2.44 Comparative Overview of Serial Communications Interfaces

Item		RX62T (SCIb)	RX66T (SCIj, SCIi, SCIh)
Serial communications mode		• Asynchronous • Clock synchronous • Smart card interface	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C-bus • Simple SPI bus
Transfer speed		Bit rate specifiable with on-chip baud rate generator.	Bit rate specifiable with the on-chip baud rate generator.
Full-duplex communication		• Transmitter: Enables continuous transmission by double-buffering. • Receiver: Enables continuous reception by double-buffering.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable from LSB-first or MSB-first transfer	Selectable as LSB first or MSB first transfer
Interrupt sources		• Transmit-end, transmit-data-empty, receive-data-full, and receive error	• Transmit end, transmit data empty, receive data full, receive error, receive data ready (SCI11), and data match (SCI1, SCI5, SCI6, SCI8, SCI9, SCI11) • Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)
Low power consumption function		Module stop state can be set for each unit.	Module stop state can be set for each channel.
Asynchronous mode	Data length	7 or 8 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even, odd, or none	Even parity, odd parity, or no parity
	Receive error detection function	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	—	CTSn# and RTSn# pins can be used in controlling transmission/ reception
	Transmit/receive FIFO	—	16-stage FIFOs for transmit and receive buffers (SCI11)
	Data match detection	—	Compares receive data and comparison data, and generates interrupt when they are matched (SCI1, SCI5, SCI6, SCI8, SCI9, SCI11)
	Start-bit detection	Low level or falling edge is selectable.	Low level or falling edge is selectable.

Item		RX62T (SCIb)	RX66T (SCIj, SCIi, SCIh)
Asynchronous mode	Break detection	Break can be detected by reading RXDn (n = 0 to 2) pin level directly in case of a framing error	When a framing error occurs, a break can be detected by reading the RXDn pin level directly or reading the SPTR.RXDMON flag.
	Clock source	Selectable from internal or external clock	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used. (SCI5, SCI6, SCI12)
	Double-speed mode	—	Baud rate generator double-speed mode is selectable.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	Capable of canceling noise on the RXDn (n = 0 to 2) pin.	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun errors	Overrun error
	Hardware flow control	—	CTSn# and RTSn# pins can be used in controlling transmission/ reception.
	Transmit/receive FIFO	—	16-stage FIFOs for transmit and receive buffers (SCI11)
Smart card interface mode	Error processing	• An error signal can be automatically transmitted on detection of a parity error during reception • Data can be automatically re-transmitted on receiving an error signal during transmission	• An error signal can be automatically transmitted when detecting a parity error during reception • Data can be automatically retransmitted when receiving an error signal during transmission
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	—	I^2C-bus format
	Operating mode	—	Master (single-master operation only)
	Transfer speed	—	Fast mode is supported (refer to section 32.2.13, Bit Rate Register (BRR) to set the transfer rate).
	Noise cancellation	—	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.

Item		RX62T (SCIb)	RX66T (SCIj, SCIi, SCIh)
Simple SPI bus	Data length	—	8 bits
	Detection of errors	—	Overrun error
	SS input pin function	—	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	—	Four kinds of settings for clock phase and clock polarity are selectable.
Event link function (supported by SCI5 only)		—	Error (receive error or error signal detection) event output
		—	Receive data full event output
		—	Transmit data empty event output
		—	Transmit end event output
Extended serial mode (supported by SCI 12 only)	Start frame transmission	—	• Output of a low level as the Break Field over a specified width and generation of interrupts on completion • Detection of bus collisions and the generation of interrupts on detection
	Start frame reception	—	• Detection of the Break Field low width and generation of an interrupt on detection • Comparison of Control Fields 0 and 1 and generation of an interrupt when the two match • Two kinds of data for comparison (primary and secondary) can be set in Control Field 1. • A priority interrupt bit can be set in Control Field 1. • Handling of Start Frames that do not include a Break Field • Handling of Start Frames that do not include a Control Field 0 • Function for measuring bit rates
	I/O control function	—	• Selectable polarity for TXDX12 and RXDX12 signals • Selection of a digital filter for the RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Selectable timing for the sampling of data received through RXDX12
	Timer function	—	Usable as a reloading timer
Bit rate modulation function		—	Correction of outputs from the on-chip baud rate generator can reduce errors.

Table 2.45 Comparative Listing of Serial Communications Interface Channels

Item	RX62T (SCIb)	RX66T (SCIj, SCIi, SCIh)
Asynchronous mode	SCI0, SCI1, SCI2	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12
Clock synchronous mode	SCI0, SCI1, SCI2	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12
Smart card interface mode	SCI0, SCI1, SCI2	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12
Simple I^2C mode	—	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12
Simple SPI mode	—	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12
FIFO mode	—	SCI11
Data match detection	—	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11
Extended serial mode	—	SCI12
TMR clock input	—	SCI5, SCI6, SCI12
Event link function	—	SCI5
Peripheral module clock	PCLK	PCLKB: SCI1, SCI5, SCI6, SCI8, SCI9, SCI12 PCLKA: SCI11

Table 2.46 Comparison of Serial Communications Interface Registers

Register	Bit	RX62T (SCIb)	RX66T (SCIj, SCIi, SCIh)
RDRH	—	—	Receive Data Register H
RDRL	—	—	Receive Data Register L
RDRHL	—	—	Receive Data Register HL
FRDR	—	—	Receive FIFO Data Register
TDRH	—	—	Transmit Data Register H
TDRL	—	—	Transmit Data Register L
RDRHL	—	—	Transmit Data Register HL
FTDR	—	—	Transmit FIFO Data Register
SMR (When SCMR.SMIF = 0)	CHR	Character length bit (Valid only in asynchronous mode) 0: Selects 8 bits as the data length 1: Selects 7 bits as the data length	Character length bit (Valid only in asynchronous mode) Selects in combination with the SCMR.CHR1 bit. CHR1 CHR 0 0: Transmit/receive in 9-bit data length 0 1: Transmit/receive in 9-bit data length 1 0: Transmit/receive in 8-bit data length (initial value) 1 1: Transmit/receive in 7-bit data length
	CM	Communications mode bit 0: Asynchronous mode 1: Clock synchronous mode	Communications mode bit 0: Asynchronous mode or simple I^2C mode 1: Clock synchronous mode or simple SPI mode

Register	Bit	RX62T (SCIb)	RX66T (SCIj, SCIi, SCIh)
SCR (When SCMR.SMIF = 0)	CKE[1:0]	Clock enable bits (Asynchronous mode) b1 b0 0 0: On-chip baud rate generator The SCKn pin functions as I/O port. 0 1: On-chip baud rate generator The clock with the same frequency as the bit rate is output from the SCKn pin. 1 0: External clock Input a clock signal with a frequency 16 times the bite rate from the SCKn pin. Input a clock signal with a frequency eight times the bit rate when the SEMR.ABCS bit is 1. 1 1: External clock Input a clock signal with a frequency 16 times the bite rate from the SCKn pin. Input a clock signal with a frequency eight times the bit rate when the SEMR.ABCS bit is 1. (Clock synchronous mode) b1 b0 0 0: Internal clock The SCKn pin functions as the clock output pin. 0 1: Internal clock The SCKn pin functions as the clock output pin. 1 0: External clock The SCKn pin functions as the clock input pin. 1 1: External clock The SCKn pin functions as the clock input pin.	Clock enable bits (Asynchronous mode) b1 b0 0 0: On-chip baud rate generator The SCKn pin becomes high-impedance. 0 1: On-chip baud rate generator The clock with the same frequency as the bit rate is output from the SCKn pin. 1 x: External clock or TMR clock The clock with a frequency 16 times the bit rate should be input from the SCKn pin. Input a clock signal with a frequency eight times the bit rate when the SEMR.ABCS bit is 1. When using the TMR clock, the SCKn pin enters the high-impedance state. The TMR clock is selectable for SCI5, SCI6, and SCI12. (Clock synchronous mode) b1 b0 0 x: Internal clock The SCKn pin functions as the clock output pin. 1 x: External clock The SCKn pin functions as the clock input pin.
SSRFIFO	—	—	Serial status register

Register	Bit	RX62T (SCIb)	RX66T (SCIj, SCIi, SCIh)
SCMR	SDIR	Bit order select bit This bit can be used in the following modes: • Smart card interface mode • Asynchronous mode (multi-processor mode) • Clock synchronous mode 0: Transfer with LSB-first 1: Transfer with MSB-first	Transmitted/received data transfer direction bit This bit can be used in the following modes: • Smart card interface mode • Asynchronous mode (multi-processor mode) • Clock synchronous mode • Simple SPI mode • Set this bit to 1 if operation is to be in simple I²C mode. 0: Transfer with LSB first 1: Transfer with MSB first
	CHR1	—	Character length bit 1
MDDR	—	—	Modulation duty register
SEMR	ACS0	—	Asynchronous mode clock source select bit
	BRME	—	Bit rate modulation enable bit
	ABCSE	—	Asynchronous mode base clock select extended bit
	NFEN	Noise cancelling function select bit (Valid only in asynchronous mode) 0: Disables noise cancellation for the RXDn pin 1: Enables noise cancellation for the RXDn pin	Digital noise filter function enable bit (In asynchronous mode) 0: Noise cancellation function for the RXDn input signal is disabled. 1: Noise cancellation function for the RXDn input signal is enabled. (In simple I²C mode) 0: Noise cancellation function for the SSCLn and SSDAn input signals is disabled. 1: Noise cancellation function for the SSCLn and SSDAn input signals is enabled. The NFEN bit should be 0 in any mode other than above.
	BGDM	—	Baud rate generator double-speed mode select bit
SNFR	—	—	Noise filter setting register
SIMR1	—	—	I²C mode register 1
SIMR2	—	—	I²C mode register 2
SIMR3	—	—	I²C mode register 3
SISR	—	—	I²C status register
SPMR	—	—	SPI mode register
FCR	—	—	FIFO control register
FDR	—	—	FIFO data count register
LSR	—	—	Line status register
CDR	—	—	Comparison data register

Register	Bit	RX62T (SCIb)	RX66T (SCIj, SCIi, SCIh)
DCCR	—	—	Data comparison control register
SPTR	—	—	Serial port register
ESMER	—	—	Extended serial module enable register
CR0	—	—	Control register 0
CR1	—	—	Control register 1
CR2	—	—	Control register 2
CR3	—	—	Control register 3
PCR	—	—	Port control register
ICR	—	—	Interrupt control register
STR	—	—	Status register
STCR	—	—	Status clear register
CF0DR	—	—	Control field 0 data register
CF0CR	—	—	Control field 0 compare enable register
CF0RR	—	—	Control field 0 receive data register
PCF1DR	—	—	Primary control field 1 data register
SCF1DR	—	—	Secondary control field 1 data register
CF1CR	—	—	Control field 1 compare enable register
CF1RR	—	—	Control field 1 receive data register
TCR	—	—	Timer control register
TMR	—	—	Timer mode register
TPRE	—	—	Timer prescaler register
TCNT	—	—	Timer count register

2.21 I²C Bus Interface

Table 2.47 is a comparative overview of I²C bus interface, and Table 2.48 is a comparison of I²C bus interface registers.

Table 2.47 Comparative Overview of I²C Bus Interface

Item	RX62T (RIIC)	RX66T (RIICa)
Communications format	• I²C bus format or SMBus format • Master mode or slave mode selectable • Automatic securing of the various set-up times, hold times, and bus-free times for the transfer rate	• I²C-bus format or SMBus format • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate
Transfer speed	Up to 400 kbps	Fast-mode is supported (up to 400 kbps)
SCL clock	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%.	For master operation, the duty cycle of the SCL clock is selectable in the range from 4 to 96%.
Issuing and detecting conditions	• Start, restart, and stop conditions are automatically generated. • Start conditions (including restart conditions) and stop conditions are detectable.	• Start, restart, and stop conditions are automatically generated. • Start conditions (including restart conditions) and stop conditions are detectable.
Slave address	• Up to three slave-address settings can be made. • Seven- and ten-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.
Acknowledgment	• For transmission, the acknowledge bit is automatically loaded. — Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. — If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.	• For transmission, the acknowledge bit is automatically loaded. — Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. — If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.
Wait function	In reception, the following periods of waiting can be obtained by holding the clock signal (SCL) at the low level: • Waiting between the eighth and ninth clock cycles • Waiting between the ninth clock cycle and the first clock cycle of the next transfer (WAIT function)	In reception, the following periods of waiting can be obtained by holding the SCL clock at the low level: • Waiting between the eighth and ninth clock cycles • Waiting between the ninth clock cycle and the first clock cycle of the next transfer

Item	RX62T (RIIC)	RX66T (RIICa)
SDA output delay function	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.
Arbitration	• For multi-master operation — Operation to synchronize the SCL (clock) signal in cases of conflict with the SCL signal from another master is possible. — When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the internal signal for the SDA line and the level on the SDA line not matching is detectable. • Loss of arbitration due to non-matching of internal and line levels for data is detectable in slave transmission.	• For multi-master operation — Operation to synchronize the SCL clock in cases of conflict with the SCL signal from another master is possible. — When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the internal signal for the SDA line and the level on the SDA line not matching is detectable. • Loss of arbitration due to non-matching of internal and line levels for data is detectable in slave transmission.
Timeout detection function	The internal time-out function is capable of detecting long-interval stoppages of the SCL (clock signal).	The internal timeout function is capable of detecting long-interval stop of the SCL clock.
Noise cancellation	The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable.	The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable by software.
Interrupt sources	Four sources: • Error in transfer or occurrence of events (detection of AL, NACK, time-out, a start condition including a restart condition, or a stop condition) • Receive-data-full (including matching with a slave address) • Transmit-data-empty (including matching with a slave address) • Transmission complete	Four sources: • Error in transfer or occurrence of events Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end

Item	RX62T (RIIC)	RX66T (RIICa)
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state
RIIC operating modes	Four modes: • Master transmit mode • Master receive mode • Slave transmit mode • Slave receive mode	Four modes: • Master transmit mode • Master receive mode • Slave transmit mode • Slave receive mode
Event link function (output)	—	Four sources: • Error in transfer or occurrence of events Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end

Table 2.48 Comparison of I²C Bus Interface Registers

Register		Bit	RX62T (RIIC)	RX66T (RIICa)
ICMR2		TMWE	Timeout internal counter write enable bit	—
TMOCNT	TMOCNTL	—	Timeout Internal Counter	—
	TMOCNTU	—	Timeout Internal Counter	—

2.22 CAN Module

Table 2.49 is a comparative overview of CAN module, and Table 2.50 is a comparison of CAN module registers.

Table 2.49 Comparative Overview of CAN Module

Item	RX62T (CAN)	RX66T (CAN)
Protocol	ISO11898-1 compliant (standard and extended frames)	ISO 11898-1 compliant (standard and extended frames)
Bit rate	• Programmable bit rate up to 1 Mbps (fCAN ≥ 8 MHz) • fCAN: CAN clock source	• Programmable bit rate up to 1 Mbps (fCAN ≥ 8 MHz) • fCAN: CAN clock source
Message box	• 32 mailboxes: Two selectable mailbox modes • Normal mailbox mode: 32 mailboxes can be configured for either transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for either transmission or reception. Of the other mailboxes, four FIFO stages can be configured for transmission and four FIFO stages for reception.	• 32 mailboxes: Two selectable mailbox modes • Normal mailbox mode: 32 mailboxes can be configured for either transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for either transmission or reception. Of the other mailboxes, four FIFO stages can be configured for transmission and four FIFO stages for reception.
Reception	• Data frame and remote frame can be received. • Selectable receiving ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot reception function • Selectable from overwrite mode (message overwritten) and overrun mode (message discarded) • The reception complete interrupt can be individually enabled or disabled for each mailbox.	• Data frame and remote frame can be received. • Selectable receiving ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot reception function • Selectable from overwrite mode (message overwritten) and overrun mode (message discarded) • The reception complete interrupt can be individually enabled or disabled for each mailbox.
Acceptance filter	• Eight acceptance masks (one mask for every four mailboxes) • The mask can be individually enabled or disabled for each mailbox.	• Eight acceptance masks (one mask for every four mailboxes) • The mask can be individually enabled or disabled for each mailbox.

Item	RX62T (CAN)	RX66T (CAN)
Transmission	• Data frame and remote frame can be transmitted. • Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot transmission function • Selectable from ID priority mode and mailbox number priority mode • Transmission request can be aborted (the completion of abort can be confirmed with a flag) • The transmission complete interrupt can be individually enabled or disabled for each mailbox.	• Data frame and remote frame can be transmitted. • Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot transmission function • Selectable from ID priority mode and mailbox number priority mode • Transmission request can be aborted (the completion of abort can be confirmed with a flag) • The transmission complete interrupt can be individually enabled or disabled for each mailbox.
Mode transition for bus-off recovery	Mode transition for the recovery from the bus-off state can be selected: • ISO11898-1 Specifications compliant • Automatic entry to CAN halt mode at bus-off entry • Automatic entry to CAN halt mode at bus-off end • Entry to CAN halt mode by a program • Transition into error-active state by a program	Mode transition for the recovery from the bus-off state can be selected: • ISO 11898-1 Standards compliant • Automatic entry to CAN halt mode at bus-off entry • Automatic entry to CAN halt mode at bus-off end • Entry to CAN halt mode by a program • Transition into error-active state by a program
Error status monitoring	• CAN bus errors (stuff error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored. • Transition to error states can be detected (error-warning, error-passive, bus-off entry, and bus-off recovery). • The error counters can be read.	• CAN bus errors (stuff error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored. • Transition to error states can be detected (error-warning, error-passive, bus-off entry, and bus-off recovery). • The error counters can be read.
Time stamp function	• Time stamp function using a 16-bit counter • The reference clock can be selected from 1-, 2-, 4- and 8-bit time periods.	• Time stamp function using a 16-bit counter • The reference clock can be selected from 1-, 2-, 4- and 8-bit time periods.
Interrupt function	Five types of interrupt sources (reception complete, transmission complete, receive FIFO, transmit FIFO, and error interrupts)	Five types of interrupt sources (reception complete, transmission complete, receive FIFO, transmit FIFO, and error interrupts)
CAN sleep mode	Current consumption can be reduced by stopping the CAN clock.	Current consumption can be reduced by stopping the CAN clock.

Item	RX62T (CAN)	RX66T (CAN)
Software support units	Three software support units: • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support	Three software support units: • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support
CAN clock source	Peripheral module clock (PCLK)	Peripheral module clock (PCLKB) or CANMCLK
Test modes	Three test modes available for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback)	Three test modes available for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback)
Low power consumption function	Module-stop state can be set.	Module-stop state can be set.

Table 2.50 Comparison of CAN Module Registers

Register		Bit	RX62T (CAN)	RX66T (CAN)
BCR		CCLKS	—	CAN clock source selection bit
MKIVLR		— (RX62T) MB31 to MB0 (RX66T)	Mask invalid register	Mask invalid register
MIER	Normal mail box mode	— (RX62T) MB31 to MB0 (RX66T)	Interrupt enable bits	Interrupt enable bits
	FIFO mail box mode	— (RX62T) MB23 to MB0 (RX66T)	Interrupt enable bits	Interrupt enable bits
		— (RX62T) MB24 (RX66T)	Transmit FIFO interrupt enable bit	Transmit FIFO interrupt enable bit
		— (RX62T) MB25 (RX66T)	Transmit FIFO interrupt generation timing control bit	Transmit FIFO interrupt generation timing control bit
		— (RX62T) MB28 (RX66T)	Receive FIFO interrupt enable	Receive FIFO interrupt enable
		— (RX62T) MB29 (RX66T)	Receive FIFO interrupt generation timing control bit	Receive FIFO interrupt generation timing control bit
STR		—	Status register	Status register
			Initial values after a reset are different.	

2.23 Serial Peripheral Interface

Table 2.51 is a comparative overview of serial peripheral interface, and Table 2.52 is a comparison of serial peripheral interface registers.

Table 2.51 Comparative Overview of Serial Peripheral Interface

Item	RX62T (RSPI)	RX66T (RSPIc)
Number of channels	One channel	One channel
RSPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (four-wire method) or clock synchronous operation (three-wire method). • Transmit-only operation is available. • Capable of serial communications in master/slave mode • Switching of the polarity of the serial transfer clock • Switching of the phase of the serial transfer clock	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK
Data format	• MSB-first/LSB-first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits).	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits). • Byte swapping of transmit and receive data is selectable
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 8 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 8). — Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4). — Width at high level: 2 cycles of PCLK; width at low level: 2 cycles of PCLK
Buffer configuration	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers

Item	RX62T (RSPI)	RX66T (RSPIc)
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection
Interrupt sources	Maskable interrupt sources • RSPI receive interrupt (receive buffer full) • RSPI transmit interrupt (transmit buffer empty) • RSPI error interrupt (mode fault, overrun, parity error) • RSPI idle interrupt (RSPI idle)	Interrupt sources • Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, underrun, or parity error) • RSPI idle interrupt (RSPI idle)
SSL control function	• Four SSL signals (SSL0 to SSL3) for each channel • In single-master mode, SSL0 to SSL3 signals are output. • In multi-master mode, SSL0 signal for input, and SSL1 to SSL3 signals for either output or high-impedance. • In slave mode, SSL0 signal for input, and SSL1 to SSL3 signals for high-impedance. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stoppage to SSL output negation (SSL negation delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode, SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode, SSLA0 pin for input, and SSLA1 to SSLA3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity
Control during master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, LSB/MSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function

Item	RX62T (RSPI)	RX66T (RSPIc)
Event link function (output)	—	The following events can be output to the event link controller. (RSPI0) • Receive buffer full signal • Transmit buffer empty signal • Mode fault, overrun, underrun, or parity error signal • RSPI idle signal • Transmission-completed signal
Other functions	• Function for disabling (initializing) the RSPI • Loopback mode	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Table 2.52 Comparison of Serial Peripheral Interface Registers

Register	Bit	RX62T (RSPI)	RX66T (RSPIc)
SPSR	MODF	Mode fault error flag 0: No mode fault error occurs 1: A mode fault error occurs	Mode fault error flag 0: Neither a mode fault error nor an underrun error occurs 1: A mode fault error or an underrun error occurs
	UDRF	—	Underrun error flag
SPDR	—	RSPI data register Available access size: • Longwords (SPDCR.SPLW = 1) • Words (SPDCR.SPLW = 0)	RSPI data register Available access size: • Longwords (SPDCR.SPLW = 1, SPBYTE = 0) • Words (SPDCR.SPLW = 0, SPBYTE = 0) • Bytes (SPDCR.SPBYT = 1)
SPBR	SPR0 to SPR7 (RX62T) — (RX66T)	RSPI bit rate register	RSPI bit rate register
SPDCR	SLSEL[1:0]	SSI pin output selection bits	—
	SPBYT	—	RSPI byte access specification
SPCR2	SCKASE	—	RSPCK auto-stop function enable
SPDCR2	—	—	RSPI data control register 2

2.24 CRC Calculator

Table 2.53 is a comparative overview of CRC calculator, and Table 2.54 is a comparison of CRC calculator registers.

Table 2.53 Comparative Overview of CRC Calculator

Item	RX62T (CRC)	RX66T (CRCA)	
Data size	8 bits	8 bits	32 bits
Data for CRC calculation	CRC code generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 32n-bit units (where n is a whole number)
CRC processor unit	Operation executed on eight bits in parallel	8-bit parallel processing	32-bit parallel processing
CRC generating polynomial	One of three generating polynomials is selectable 8-bit CRC: • $X^8 + X^2 + X + 1$ 16-bit CRC: • $X^{16} + X^{15} + X^2 + 1$ • $X^{16} + X^{12} + X^5 + 1$	One of three generating polynomials is selectable 8-bit CRC: • $X^8 + X^2 + X + 1$ 16-bit CRC: • $X^{16} + X^{15} + X^2 + 1$ • $X^{16} + X^{12} + X^5 + 1$	One of two generating polynomials is selectable 32-bit CRC: • $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ • $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$
CRC calculation switching	CRC code generation for LSB-first or MSB-first communication selectable	The order of the bits produced by CRC calculation can be switched for LSB first or MSB first communication	
Low power consumption	Module stop state can be set	Ability to transition to module stop state	

Table 2.54 Comparison of CRC Calculator Registers

Register	Bit	RX62T (CRC)	RX66T (CRCA)
CRCCR	GPS[1:0]:RX62T GPS[2:0]:RX66T	CRC generating polynomial switching bits (b1, b0) b1 b0 0 0: No calculation is executed. 0 1: $X^8 + X^2 + X + 1$ 1 0: $X^{16} + X^{15} + X^2 + 1$ 1 1: $X^{16} + X^{12} + X^5 + 1$	CRC generating polynomial switching bits (b2 to b0) b2 b0 0 0 0: No calculation is executed. 0 0 1: 8-bit CRC ($X^8 + X^2 + X + 1$) 0 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$) 0 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$) 1 0 0: 32-bit CRC ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1: 32-bit CRC ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) 1 1 0: No calculation is executed. 1 1 1: No calculation is executed.
	LMS	CRC calculation switching bit (b2)	CRC calculation switching bit (b6)
CRCDIR	—	CRC data input register Available access size: • Bytes	CRC data input register Available access size: • Longwords (when generating a 32-bit CRC) • Bytes (When generating a 16-bit/8-bit CRC)
CRCDOR	—	CRC data output register Available access size: • Words When generating 8-bit CRC, the valid CRC code is obtained from the lower-order byte (b7 to b0).	CRC data output register Available access size: • Longwords (when generating a 32-bit CRC) Words (when generating a 16-bit CRC) • Bytes (when generating a 8-bit CRC)

2.25 12-Bit A/D Converter

Table 2.55 is a comparative overview of 12-Bit A/D converters, Table 2.56 is a comparison of 12-Bit A/D converter registers, and Table 2.57 is a comparative listing A/D conversion start triggers.

Table 2.55 Comparative Overview of 12-Bit A/D Converters

Item	RX62T (S12ADA)	RX66T (S12ADH)
Number of units	Two units (S12AD0 and S12AD1)	Three units (S12AD, S12AD1, and S12AD2)
Input channels	Eight channels (four channels x two units)	Eight channels for S12AD, eight channels for S12AD1, and 14 channels for S12AD2
Extended analog function	—	Temperature sensor output, internal reference voltage (S12AD2 only)
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	• 1.0 µs per 1 channel (when operating with A/D conversion clock ADCLK = 50 MHz and AVCC0 = 4.0 to 5.5V) • 2.0 µs per 1 channel (when operating with A/D conversion clock ADCLK = 25 MHz and AVCC0 = 3.0 to 3.6V)	• 0.9 µs per channel (when A/D conversion clock ADCLK = 60 MHz)
Data registers	• Ten data registers • The A/D conversion result is held in a 12-bit A/D data register.	• 30 registers for analog input (eight for S12AD, eight for S12AD1, and 14 for S12AD2), 1 for A/D-converted data duplication in double trigger mode per unit, and 2 for A/D-converted data duplication during extended operation in double trigger mode per unit. • One register for temperature sensor (S12AD2) • One register for internal reference (S12AD2) • One register for self-diagnosis per unit • The results of A/D conversion are stored in 12-bit A/D data registers. • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.

Item	RX62T (S12ADA)	RX66T (S12ADH)
Data registers	• For AN000 and AN100 inputs, two A/D data registers are provided, which are switched according to the trigger type.	• Extended operation in double trigger mode (available for specific triggers): A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.
A/D conversion clock	• Four types: PCLK, PCLK/2, PCLK/4, PCLK/8	• Peripheral module clock PCLK and A/D conversion clock ADCLK can be set with one of the following frequency ratio: PCLK to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1 • ADCLK is set using the clock generation circuit. • A/D conversion clock (ADCLK) can operate between 8 MHz at a minimum and 60 MHz at a maximum.
Operating modes	• Single mode: Analog inputs of one channel are converted only once. • Scan mode — Single-cycle scan mode: Analog inputs of up to four channels are converted only once. — Continuous scan mode: Analog inputs of up to four channels are converted repeatedly. — 2-channel scan mode: Channels in each unit are divided into two groups and the conversion startup source can be separately selected for each group.	Operating modes can be set independently for three units. • Single scan mode: — A/D conversion is performed only once on the analog inputs arbitrarily selected. — A/D conversion is performed only once on the temperature sensor output (S12AD2). — A/D conversion is performed only once on the internal reference voltage (S12AD2). • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs arbitrarily selected. • Group scan mode: — Two (groups A and B) or three (groups A, B, and C) can be selected as the number of the groups to be used. (Only the combination of groups A and B can be selected when the number of the groups is two.) — Analog inputs, temperature sensor output (S12AD2), and internal reference voltage (S12AD2) that are arbitrarily selected are divided into two groups (group A and B) or three groups (group A, B, and C), and A/D conversion of the analog input selected on a group basis is performed only once.

Item	RX62T (S12ADA)	RX66T (S12ADH)
Operating modes		— The conditions for scanning start of groups A, B, and C (synchronous trigger) can be independently selected, thus allowing A/D conversion of each group to be started independently. • Group scan mode (when group priority control selected): — If a priority-group trigger is input during scanning of the low-priority group, scan of the low-priority group is stopped and scan of the priority group is started. The priority order is group A (highest) > group B > group C (lowest). Whether or not to restart scanning of the low-priority group after processing for the high-priority group completes, is selectable. Rescan can also be set to start either from the beginning of the selected channel or the channel on which A/D conversion is not completed.
Conditions for A/D conversion start	• Software trigger • Conversion start trigger by the multifunction timer pulse unit 3 (MTU3) or general PWM timer (GPT). • External trigger — A/D conversion can be externally triggered from the ADTRG0# pin in S12AD0 and from the ADTRG1# pin in S12AD1.	• Software trigger • Synchronous trigger — Trigger by the multi-function timer pulse unit (MTU), 8-bit timer (TMR), or event link controller (ELC). • Asynchronous trigger — A/D conversion can be triggered by the external trigger ADTRG0# (S12AD), ADTRG1# (S12AD1), or ADTRG2# (S12AD2) pin (independently for three units).
Functions	• Sample-and-hold function (three channels per unit) A dedicated sample-and-hold circuit is provided for each of channels 0 to 2 (AN000 to AN002) of S12AD0 and channels 0 to 2 (AN100 to AN102) of S12AD1, which enables simultaneous sampling in multiple channels (up to three channels) in each unit. • Self-diagnostic functions for A/D converter	• Channel-dedicated sample-and-hold function (three channels for S12AD and three channels for S12AD1) (Constant sampling can be set) • Variable sampling time (can be set per channel) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode

Item	RX62T (S12ADA)	RX66T (S12ADH)
Functions		• Analog input disconnection detection assist function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data)
	• A/D data register auto-clear function	• Automatic clear function of A/D data registers
	• Window comparator function (three channels per unit)	• For the function equivalent to the window comparator function of RX62T, refer to the Comparator C chapter in the User's Manual: Hardware. • Comparison function (windows A and B) • Order of channel conversion in each unit can be set.
	• Input signal amplification function provided through programmable gain amplifier (three channels per unit)	• Input signal amplification function of the programmable gain amplifier (each unit has 3 channels; either single-ended input or pseudo-differential input can be selected)
Interrupt sources	• Interrupt request (S12ADI) can be generated on completion of A/D conversion in each unit.	• In the modes except double trigger mode and group scan mode, a scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of single scan (independently for three units). • In double trigger mode, a scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of double scan (independently for three units). • In group scan mode, a scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of group A scan, whereas a group B scan end interrupt request (S12GBADI, S12GBADI1, or S12GBADI2) can be generated on completion of group B scan, and a group C scan end interrupt request (S12GCADI, S12GCADI1, or S12GCADI2) can be generated on completion of group C scan.

Item	RX62T (S12ADA)	RX66T (S12ADH)
Interrupt sources	• Interrupt request (CMPI) can be generated when a specified comparison condition is detected (can also be used for a POE source). • A S12ADI interrupt can activate the data transfer controller (DTC).	• When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of double scan of group A, and the corresponding scan end interrupt request (S12GBADI/S12GCADI, S12GBADI1/S12GCADI1, or S12GBADI2/S12GCADI2) can be generated on completion of group B and group C scan. • A compare interrupt request (S12CMPAI, S12CMPAI1, S12CMPAI2, S12CMPBI, S12CMPBI1, or S12CMPBI2) can be generated upon a match with the comparison condition for the digital compare function. • The S12ADI/S12ADI1/S12ADI2, S12GBADI/S12GBADI1/S12GBADI2, and S12GCADI/S12GCADI1/ S12GCADI2 interrupts can trigger the DMA controller (DMAC) and data transfer controller (DTC).
Event link function	—	• The event signal is generated when all scans are finished. • The event signal is generated depending on conditions for comparison function window in single scan mode. • Able to start scanning by a trigger from the ELC.
Low power consumption function	Module stop state can be specified in each unit.	Module stop state can be set.

Table 2.56 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX62T (S12ADA)	RX66T (S12ADH)
ADDRy	—	A/D data registers y (y = 0A, 0B, and 1 to 3)	A/D data registers y (S12AD: y = 0 to 7, S12AD1: y = 0 to 7, S12AD2: y = 0 to 11, 16, 17)
ADDBLDR	—	—	A/D data duplication register
ADDBLDRA	—	—	A/D data duplication register A
ADDBLDRB	—	—	A/D data duplication register B
ADTSDR	—	—	A/D temperature sensor data register
ADOCDR	—	—	A/D internal reference voltage data register
ADRD	AD11 to AD0 (RX62T) — (RX66T)	A/D converted value 11 to 0	12-bit A/D-converted value
	DIAGST[1:0] (RX62T) — (RX66T)	Self diagnostic status bits	Self diagnosis status bits
ADCSR	EXTRG	Trigger select bit (b0)	Trigger select bit (b8)
	TRGE	Trigger enable bit (b1)	Trigger start enable bit (b9)
	CKS[1:0]	Clock select bits	—
	DBLANS[4:0]	—	Double trigger channel select bits
	GBADIE	—	Group B scan end interrupt enable bit
	DBLE	—	Double trigger mode select bit
	ADIE	A/D conversion end interrupt enable bit (b4)	Scan end interrupt enable bit (b12)
	ADCS[1:0]	A/D conversion mode select bits (b6, b5) b6 b5 0 0: Single mode 0 1: Single-cycle scan mode 1 0: Continuous scan mode 1 1: 2-channel scan mode	Scan mode select bits (b14, b13) b14 b13 0 0: Single mode 0 1: Group scan mode 1 0: Continuous scan mode 1 1: Setting prohibited
	ADST	A/D start bit (b7)	A/D conversion start bit (b15)
ADANS	—	A/D channel select register	—
ADANSA0	—	—	A/D channel select register A0
ADANSA1	—	—	A/D channel select register A1
ADANSB0	—	—	A/D channel select register B0
ADANSB1	—	—	A/D channel select register B1
ADANSC0	—	—	A/D channel select register C0
ADANSC1	—	—	A/D channel select register C1
ADSCSn	—	—	A/D channel conversion order setting register n (n = 0 to 13)
ADADS0	—	—	A/D-converted value addition/average function channel select register 0
ADADS1	—	—	A/D-converted value addition/average function channel select register 1

Register	Bit	RX62T (S12ADA)	RX66T (S12ADH)
ADADC	—	—	A/D-converted value addition/average count select register
ADCER	SHBYP	Dedicated sample-and-hold circuit select bit	—
	ADPRC[1:0]	A/D data register bit precision set bits	—
	ADIE2	2-channel scan interrupt select bit	—
	ADIEW	Double trigger interrupt select bit	—
ADSTRGR	ADSTRS0[4:0] (RX62T) TRSA[5:0] (RX66T)	A/D start trigger group 0 select bits (b4 to b0) Refer to Table 2.57 for details.	A/D conversion start trigger select bits (b13 to b8) Refer to Table 2.57 for details.
	ADSTRS1[4:0] (RX62T) TRSB[5:0] (RX66T)	A/D start trigger group 1 select bits (b12 to b8) Refer to Table 2.57 for details.	A/D conversion start trigger select for group B bits (b5 to b0) Refer to Table 2.57 for details.
ADPG	—	A/D programmable gain amplifier register	—
ADCMPMD0	—	Comparator operating mode select register 0	—
ADCMPMD1	—	Comparator operating mode select register 1	—
ADCMPNR0	—	Comparator filter mode register 0	—
ADCMPNR1	—	Comparator filter mode register 1	—
ADCMPFR	—	Comparator detection flag register	—
ADCMPSEL	—	Comparator interrupt select register	—
ADEXICR	—	—	A/D conversion extended input control register
ADGCEXCR	—	—	A/D group C extended input control register
ADGCTRGR	—	—	A/D group C trigger select register
ADSSTRn	—	A/D sampling state register	A/D sampling state register n (n = 0 to 11, L, T, O)
		Initial values after a reset are different.	
ADSHCR	—	—	A/D sample-and-hold circuit control register
ADSHMSR	—	—	A/D sample-and-hold operating mode select register
ADDISCR	—	—	A/D disconnection detection control register
ADELCCR	—	—	A/D event link control register
ADGSPCR	—	—	A/D group scan priority control register
ADCMPCR	—	—	A/D comparison function control register
ADCMPANSR0	—	—	A/D comparison function window A channel select register 0

Register	Bit	RX62T (S12ADA)	RX66T (S12ADH)
ADCMPANSR1	—	—	A/D comparison function window A channel select register 1
ADCMPANSER	—	—	A/D comparison function window A extended input select register
ADCMPLR0	—	—	A/D comparison function window A comparison condition setting register 0
ADCMPLR1	—	—	A/D comparison function window A comparison condition setting register 1
ADCMPLER	—	—	A/D comparison function window A extended input comparison condition setting register
ADCMPDR0	—	—	A/D comparison function window A lower level setting register
ADCMPDR1	—	—	A/D comparison function window A upper level setting register
ADCMPSR0	—	—	A/D comparison function window A channel status register 0
ADCMPSR1	—	—	A/D comparison function window A channel status register 1
ADCMPSER	—	—	A/D comparison function window A extended input channel status register
ADWINMON	—	—	A/D comparison function window A/B status monitoring register
ADCMPBNSR	—	—	A/D comparison function window B channel select register
ADWINLLB	—	—	A/D comparison function window B lower level setting register
ADWINULB	—	—	A/D comparison function window B upper level setting register
ADCMPBSR	—	—	A/D comparison function window B channel status register
ADPGACR	—	—	A/D programmable gain amplifier control register
ADPGAGS0	—	—	A/D programmable gain amplifier gain setting register 0
ADPGADCR0	—	—	A/D programmable gain amplifier differential input control register
ADVMONCR	—	—	A/D internal reference voltage monitoring circuit enable register
ADVMONO	—	—	A/D internal reference voltage monitoring circuit output enable register

Table 2.57 Comparative Listing A/D Conversion Start Triggers

Bit	RX62T (S12ADA)	RX66T (S12ADH)
ADSTRS1[4:0] (RX62T) TRSB[5:0] (RX66T)	A/D start trigger group 1 select bits b12 b8 0 0 0 0 0: ADTRGn# 0 0 0 0 1: TRGA0N 0 0 0 1 0: TRGA1N 0 0 0 1 1: TRGA2N 0 0 1 0 0: TRGA3N 0 0 1 0 1: TRGA4N 0 0 1 1 0: TRGA6N 0 0 1 1 1: TRGA7N 0 1 0 0 0: TRG0N 0 1 0 0 1: TRG4AN 0 1 0 1 0: TRG4BN 0 1 0 1 1: TRG4AN or TRG4BN 0 1 1 0 0: TRG4ABN 0 1 1 0 1: TRG7AN 0 1 1 1 0: TRG7BN 0 1 1 1 1: TRG7AN or TRG7BN 1 0 0 0 0: TRG7ABN 1 0 0 0 1: GTADTRA0N 1 0 0 1 0: GTADTRB0N 1 0 0 1 1: GTADTRA1N 1 0 1 0 0: GTADTRB1N 1 0 1 0 1: GTADTRA2N 1 0 1 1 0: GTADTRB2N 1 0 1 1 1: GTADTRA3N 1 1 0 0 0: GTADTRB3N 1 1 0 0 1: GTADTRA0N or GTADTRB0N 1 1 0 1 0: GTADTRA1N or GTADTRB1N 1 1 0 1 1: GTADTRA2N or GTADTRB2N 1 1 1 0 0: GTADTRA3N or GTADTRB3N	Group B A/D conversion start trigger select bits b5 b0 1 1 1 1 1 1: No trigger source selected state 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 0 1 1 0: TRGA6N 0 0 0 1 1 1: TRGA7N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 0 1 1 0 1: TRG7AN 0 0 1 1 1 0: TRG7BN 0 0 1 1 1 1: TRG7AN or TRG7BN 0 1 0 0 0 0: TRG7ABN 0 1 0 0 1 1: TRGA9N 0 1 0 1 0 0: TRG9N 0 1 1 0 0 1: TRGA0N or TRG0N 0 1 1 0 1 0: TRGA9N or TRG9N 0 1 1 0 1 1: TRGA0N or TRGA9N 0 1 1 1 0 0: TRG0N or TRG9N 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1 0 1 1 1 1 1: TMTRG0AN_2 1 0 0 0 0 0: TMTRG0AN_3 1 0 0 0 0 1: TRG9AEN 1 0 0 0 1 0: TRG0AEN 1 0 0 0 1 1: TRGA09N 1 0 0 1 0 0: TRG09N 1 1 0 0 1 0: ELCTRG00N*1/ELCTRG10N*2/ ELCTRG20N*3 1 1 0 0 1 1: ELCTRG01N*1/ELCTRG11N*2/ ELCTRG21N*3 1 1 1 0 1 0: ELCTRG00N or ELCTRG01N*1 ELCTRG10N or ELCTRG11N*2 ELCTRG20N or ELCTRG21N*3

Bit	RX62T (S12ADA)	RX66T (S12ADH)
ADSTRS1[4:0] (RX62T) TRSA[5:0] (RX66T)	A/D start trigger group 0 select bits b4 b0 0 0 0 0 0: ADTRGn# 0 0 0 0 1: TRGA0N 0 0 0 1 0: TRGA1N 0 0 0 1 1: TRGA2N 0 0 1 0 0: TRGA3N 0 0 1 0 1: TRGA4N 0 0 1 1 0: TRGA6N 0 0 1 1 1: TRGA7N 0 1 0 0 0: TRG0N 0 1 0 0 1: TRG4AN 0 1 0 1 0: TRG4BN 0 1 0 1 1: TRG4AN or TRG4BN 0 1 1 0 0: TRG4ABN 0 1 1 0 1: TRG7AN 0 1 1 1 0: TRG7BN 0 1 1 1 1: TRG7AN or TRG7BN 1 0 0 0 0: TRG7ABN 1 0 0 0 1: GTADTRA0N 1 0 0 1 0: GTADTRB0N 1 0 0 1 1: GTADTRA1N 1 0 1 0 0: GTADTRB1N 1 0 1 0 1: GTADTRA2N 1 0 1 1 0: GTADTRB2N 1 0 1 1 1: GTADTRA3N 1 1 0 0 0: GTADTRB3N 1 1 0 0 1: GTADTRA0N or GTADTRB0N 1 1 0 1 0: GTADTRA1N or GTADTRB1N 1 1 0 1 1: GTADTRA2N or GTADTRB2N 1 1 1 0 0: GTADTRA3N or GTADTRB3N	A/D conversion start trigger select bits b13 b8 1 1 1 1 1 1: No trigger source selected state 0 0 0 0 0 0: ADTRGn# 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 0 1 1 0: TRGA6N 0 0 0 1 1 1: TRGA7N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 0 1 1 0 1: TRG7AN 0 0 1 1 1 0: TRG7BN 0 0 1 1 1 1: TRG7AN or TRG7BN 0 1 0 0 0 0: TRG7ABN 0 1 0 0 1 1: TRGA9N 0 1 0 1 0 0: TRG9N 0 1 1 0 0 1: TRGA0N or TRG0N 0 1 1 0 1 0: TRGA9N or TRG9N 0 1 1 0 1 1: TRGA0N or TRGA9N 0 1 1 1 0 0: TRG0N or TRG9N 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1 0 1 1 1 1 1: TMTRG0AN_2 1 0 0 0 0 0: TMTRG0AN_3 1 0 0 0 0 1: TRG9AEN 1 0 0 0 1 0: TRG0AEN 1 0 0 0 1 1: TRGA09N 1 0 0 1 0 0: TRG09N 1 1 0 0 1 0: ELCTRG00N*1/ELCTRG10N*2/ ELCTRG20N*3 1 1 0 0 1 1: ELCTRG01N*1/ELCTRG11N*2/ ELCTRG21N*3 1 1 1 0 1 0: ELCTRG00N or ELCTRG01N*1 ELCTRG10N or ELCTRG11N*2 ELCTRG20N or ELCTRG21N*3

Notes: 1. Unit 0
2. Unit 1
3. Unit 2

2.26 RAM

Table 2.58 is a comparative overview of RAM, and Table 2.59 is a comparison of RAM registers.

Table 2.58 Comparative Overview of RAM

Item	RX62T (RAM)	RX66T	
		Without ECC Error Correction (RAM)	With ECC Error Correction (ECCRAM)
Capacity	8 KB, 16 KB	64 KB, 128 KB	16 KB
Memory bus	Memory bus 1	Memory bus 1	Memory bus 3
Access	• Single-cycle access is possible for both reading and writing. • Enabling or disabling of on-chip RAM is selectable.	• Single-cycle access is possible for both reading and writing. • Enabling or disabling of the RAM is selectable.	• Enabling or disabling of the ECC function is selectable. [When MEMWAIT is set to 0] • The ECC function is disabled: Access takes two cycles whether for reading or writing. • The ECC function is enabled (when no error has occurred): Access takes two cycles whether for reading or writing. • The ECC function is enabled (when an error has occurred): Access takes three cycles whether for reading or writing. [When MEMWAIT is set to 1] • The ECC function is disabled: Access takes three cycles whether for reading or writing. • The ECC function is enabled (when no error has occurred): Reading takes three cycles and writing takes four cycles. • The ECC function is enabled (when an error has occurred): Access takes five cycles whether for reading or writing.

Item	RX62T (RAM)	RX66T	
		Without ECC Error Correction (RAM)	With ECC Error Correction (ECCRAM)
Address	• 0000 0000h to 0000 1FFFh (8 KB) • 0000 0000h to 0000 3FFFh (16 KB)	• RAM capacity: 64 KB 0000 0000h to 0000 FFFFh • RAM capacity: 128 KB 0000 0000h to 0001 FFFFh	00FF C000h to 00FF FFFFh
Data retention function	Not available in deep software standby mode	Not available in deep software standby mode	
Low power consumption function	The module stop function is independently selectable	Transition to the module stop state is separately possible for the RAM and ECCRAM.	
Error checking	—	• Detection of 1-bit errors • A non-maskable interrupt or interrupt is generated in response to an error.	• ECC Error Correction: Correction of 1-bit errors and detection of 2-bit errors • A non-maskable interrupt or interrupt is generated in response to an error.

Table 2.59 Comparison of RAM Registers

Register	Bit	RX62T (RAM)	RX66T (RAM, ECCRAM)
ECCRAMMODE	—	—	ECCRAM operating mode control register
ECCRAM2STS	—	—	ECCRAM 2-bit error status register
ECCRAM1STSEN	—	—	ECCRAM 1-bit error information update enable register
ECCRAM1STS	—	—	ECCRAM 1-bit error status register
ECCRAMPRCR	—	—	ECCRAM protection register
ECCRAM2ECAD	—	—	ECCRAM 2-bit error address capture register
ECCRAM1ECAD	—	—	ECCRAM 1-bit error address capture register
ECCRAMPRCR2	—	—	ECCRAM protection register 2
ECCRAMETST	—	—	ECCRAM test control register
RAMMODE	—	—	RAM operating mode control register
RAMSTS	—	—	RAM error status register
RAMECAD	—	—	RAM error address capture register
RAMPRCR	—	—	RAM protection register

2.27 Flash Memory

Table 2.60 is a comparative overview of flash memory, and Table 2.61 is a comparison of flash memory registers.

Table 2.60 Comparative Overview of Flash Memory

Item	RX62T		RX66T	
	Flash Memory for Code Storage	**Flash Memory for Data Storage**	**Code Flash Memory**	**Data Flash Memory**
Memory capacity	User area: 256 KB, 128 KB, or 64 KB	Data area: 32 KB, or 8 KB	• User area: 1 MB, 512 KB, 256 KB • User boot area: 32 KB	• Data area: 32 KB
ROM cache			• Capacity: 8 KB • Mapping method: direct mapping • Line size: 16 bytes	—
Read cycle	One cycle of ICLK (high-speed reading)	Three cycles of PCLK when accessing in words or bytes	• While ROM cache operation is enabled: • When the cache is hit, one cycle; • When the cache is missed, — One to two cycles if ICLK ≤ 120 MHz — Two to three cycles if ICLK > 120 MHz • When ROM cache operation is disabled: — One cycle if ICLK ≤ 120 MHz — Two cycles if ICLK > 120 MHz	A read operation takes eight cycles of FCLK in word or byte access

Item	RX62T		RX66T	
	Flash Memory for Code Storage	**Flash Memory for Data Storage**	**Code Flash Memory**	**Data Flash Memory**
Programming/ erasing method	• The dedicated sequencer (FCU) is incorporated for programming of the ROM. • Programming and erasing the ROM are handled by issuing commands to the FCU. • Programming/erasure through transfer by a flash-memory programmer via a serial interface (serial programming) • Programming/erasure of flash memory by a user program (self-programming)	• The dedicated sequencer (FCU) is incorporated for programming of the data flash. • Programming and erasing the data flash are handled by issuing commands to the FCU. • Programming/erasure through transfer by a flash-memory programmer via a serial interface (serial programming) • Programming/erasure of flash memory by a user program (self-programming)	• The dedicated sequencer (FCU) is incorporated for programming of the flash memory. • Programming and erasing the code flash memory/data flash memory is handled by the FACI commands specified in the FACI command issuing area (007E 0000h). • Programming/erasure through transfer by a flash-memory programmer via a serial interface (serial programming) • Programming/erasure of flash memory by a user program (self-programming)	
Value after erasure	FFh	Undfined	FFh	Undfined
Unique ID	—		A 12-byte ID code provided for each MCU	
Security function	Protects against illicit tampering with or reading out of data in flash memory		Protects against illicit tampering with or reading out of data in flash memory	
Protection function	Protects against erroneous rewriting of the flash memory (software protection and error protection)		Protects against erroneous rewriting of the flash memory (software protection, error protection, and boot program protection)	
Trusted memory (TM) function	—		Protects against illicit reading of blocks 8 and 9 in the code flash memory	
Background operation (BGO)	• The CPU is able to execute program code from areas other than the ROM or data flash while the ROM is being programmed or erased. • Execution of program code from the ROM is possible while the data flash memory is being programmed or erased.		• The CPU is able to execute program code from areas other than the ROM or data flash while the ROM is being programmed or erased. • The user area can be read while the data area is being programmed or erased.	

Item	RX62T		RX66T	
	Flash Memory for Code Storage	**Flash Memory for Data Storage**	**Code Flash Memory**	**Data Flash Memory**
Units of programming and erasure	• Unit of programming for the user area: 256 bytes • Unit of erasure for the user area: Block units	• Unit of programming for the data area: 8 or 128 bytes • Unit of erasure for the data area: Block units	• Unit of programming for the user area or user boot area: 256 bytes • Unit of erasure for the user area: Block units	• Unit of programming for the data area: 4 bytes • Unit of erasure for the data area: Block units
Blank checking	—	• The blank checking command can be executed to check the erasure state of data flash. • The size of the area to be blank-checked is 8 bytes or 2 KB.	—	• The blank checking command can be executed to check the erasure state of data flash. • The size of the area to be blank-checked is 4 bytes to 32 KB (specify in 4 bytes).
On-board programming (Serial programming/ Self-programming)	• Programming in boot mode: — The asynchronous serial interface (SCI1) is used. — The transfer rate is adjusted automatically. • Programming by a routine for flash memory programming within the user program: — This allows ROM programming without resetting the system.		• Programming/erasure in boot mode (for the SCI interface): — The asynchronous serial interface (SCI1) is used. — The transfer rate is adjusted automatically. — The user boot area can also be programmed or erased. • Programming/erasure in boot mode (for the USB interface): — USBb is used. — Dedicated hardware is not required, so direct connection to a PC is possible. • Programming/erasure in boot mode (for the FINE interface): — FINE is used. • Programming/erasure in user boot mode: — Able to create original boot programs of the user's making. • Programming/erasure by self-programming: — This allows user area/data area programming and erasure without resetting the system.	

Item	RX62T		RX66T	
	Flash Memory for Code Storage	Flash Memory for Data Storage	Code Flash Memory	Data Flash Memory
Off-board programming (Programming and erasure by parallel programmer)	A PROM programmer can be used to program the user area.	The data area cannot be programmed using a PROM programmer.	Programming and erasure of the user area and user boot area by using a parallel programmer is possible.	The data area cannot be programmed or erased using a parallel programmer.

Table 2.61 Comparison of Flash Memory Registers

Register	Bit Name	RX62T	RX66T
ROMCE	—	—	ROM cache enable register
ROMCIV	—	—	ROM cache invalidate register
NCRGn	—	—	Non-cacheable area n address register (n = 0, 1)
NCRCn	—	—	Non-cacheable area n setting register (n = 0, 1)
FMODR	—	Flash mode register	—
FASTAT	DFLWPE	Data flash programming/erasure protection violation bit	—
	DFLRPE	Data flash read protection violation bit	—
	DFLAE (RX62T) DFAE (RX66T)	Data Flash access violation bit	Data flash memory access violation flag
	ROMAE (RX62T) CFAE (RX66T)	ROM access violation bit	Code flash memory access violation flag
FAEINT	DFLWPEIE	Data flash programming/erasure protection violation interrupt enable bit	—
	DFLRPEIE	Data flash read protection violation interrupt enable bit	—
	DFLAEIE (RX62T) DFAEIE (RX66T)	Data flash access violation interrupt enable bit	Data flash memory access violation interrupt enable bit
	ROMAEIE (RX62T) CFAEIE (RX66T)	ROM access violation interrupt enable bit	Code flash memory access violation interrupt enable bit
FCURAME	—	FCU RAM enable register	—
FSTATR0 (RX62T) FSTATR (RX66T)	FLWEERR	—	Flash write/erase protect error flag
	PRGSPD	Programming suspend status bit (b0)	Programming suspend status flag (b8)
	ERSSPD	Erasure suspend status bit (b1)	Erasure suspend status flag (b9)
	DBFULL	—	Data buffer full flag
	SUSRDY	Suspend ready bit (b3)	Suspend ready flag (b11)
	PRGERR	Programming error bit (b4)	Programming error flag (b12)
	ERSERR	Erasure error bit (b5)	Erasure error flag (b13)
	ILGLERR	Illegal command error bit (b6)	Illegal error command flag (b14)
	FRDY	Flash ready bit (b7)	Flash ready flag (b15)
FSTATR1	—	Flash status register 1	—

Register	Bit Name	RX62T	RX66T
FSADDR	—	—	FACI command processing start address register
FEADDR	—	—	FACI command processing end address register
FENTRYR	FENTRY0 (RX62T) FENTRYC (RX66T)	ROM P/E mode entry 0	Code flash memory p/e mode entry
	FEKEY[7:0] (RX62T) KEY[7:0] (RX66T)	Key code bits	Key code bits
FPROTR	FPKEY[7:0] (RX62T) KEY[7:0](RX66T)	Key code bits	Key code bits
FRESETR	—	Flash reset register	—
FSUINITR	—	—	Flash sequencer set-up initialization register
FLKSTAT	—	—	Lock bit status register
PCKAR (RX62T) FPCKAR (RX66T)	PCKA[7:0]	Peripheral clock notification bits These bits are used to set the peripheral clock (PCLK) at the programming/erasure for the ROM/data flash.	Flash sequencer processing clock frequency notification bits These bits are used to set the frequency of the FlashIF clock (FCLK) and notify the flash sequencer of the frequency used
	KEY[7:0]	—	Key code
DFLRE0	—	Data flash read enable register 0	—
DFLRE1	—	Data flash read enable register 1	—
DFLWE0	—	Data flash programming/erasure enable register 0	—
DFLWE1	—	Data flash programming/erasure enable register 1	—
DFLBCCNT	—	Data flash blank check control register	—
FBCCNT	—	—	Data flash blank check control register
DFLBCSTAT (RX62T) FBCSTAT (RX66T)	BCST	Blank check status bit DFLBCSTAT is a 16-bit register.	Blank check status flag FBCSTAT is an 8-bit register.
FPSADDR	—	—	Data flash programming start address register
UIDRn	—	—	Unique ID register n (n = 0 to 2)

2.28 Packages

As indicated in Table 2.62, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage. For details, refer to Design Guide for Migration between RX Family: Differences in Package External form (R01AN4591EJ).

Table 2.62 Packages

Package Type	Renesas Code	
	RX62T	**RX66T**
112-pin LQFP	PLQP0112JA-A	PLQP0112JA-B
100-pin LFQFP	PLQP0100KB-A	PLQP0100KB-B
64-pin LFQFP	PLQP0064KB-A	PLQP0064KB-C
64-pin LQFP	○	×

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by **blue text**. Items that exists on both groups with different specifications are indicated by **red text**. **Black text** indicates there is no differences in the item's specifications between groups.

3.1 112-Pin Package

Table 3.1 is a comparative listing of the pin functions of 112-pin package products.

Table 3.1 Comparative Listing of 112-Pin Package Pin Functions

112-Pin	RX62T	RX66T (With PGA Pseudo-Differential Input and Without USB Pins)
1	PE5/IRQ0-B	P14/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC9A/GTIOC2A#/GTIOC9A#/IRQ11
2	EMLE	P13/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC8A/GTIOC1A#/GTIOC8A#/IRQ10
3	VSS	P12/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC7A/GTIOC0A#/GTIOC7A#/IRQ9
4	MDE	PE5/BCLK/MTIOC9D/MTIOC9D#/GTIOC3A/ GTETRGB/GTIOC3A#/GTETRGD/SCK9/ CTS9#/RTS9#/SS9#/IRQ0/ADST0
5	VCL	EMLE
6	MD1	VSS
7	MD0	UB/P00/A11/MTIOC9A/MTIOC9A#/CACREF/ RXD9/SMISO9/SSCL9/RXD12/SMISO12/ SSCL12/RXDX12/IRQ2/ADST1/COMP0
8	PE4/MTCLKC-C/IRQ1-B/POE10#-B	VCL
9	PE3/MTCLKD-C/IRQ2-A/POE11#	MD/FINED
10	RES#	P01/A10/MTIOC9C/MTIOC9C#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE12#/ TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/IRQ4/ADST2/ COMP1
11	XTAL	PE4/A9/MTCLKC/MTCLKC#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE10#/ SCK9/IRQ1
12	VSS	PE3/A8/MTCLKD/MTCLKD#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE11#/ CTS9#/RTS9#/SS9#/IRQ2_DS
13	EXTAL	RES#
14	VCC	XTAL/P37
15	PE2/NMI/POE10#-A	VSS
16	PE1/SSL3-C	EXTAL/P36
17	PE0/CRX-C/SSL2-C	VCC
18	PD7/GTIOC0A-B/CTX-C/SSL1-C	PE2/POE10#/NMI
19	PD6/GTIOC0B-B/SSL0-C	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/ TMO5/CTS5#/RTS5#/SS5#/CTS12#/ RTS12#/SS12#/SSLA3/IRQ15

112-Pin	RX62T	RX66T (With PGA Pseudo-Differential Input and Without USB Pins)
20	PD5/GTIOC1A-B/RXD1	PE0/WR1#/BC1#/WAIT#/MTIOC9B/ MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/ SSCL5/SSLA2/CRX0/IRQ7
21	PD4/GTIOC1B-B/SCK1	TRST#/PD7/MTIOC9A/MTIOC9A#/GTIOC0A/ GTIOC3A/GTIOC0A#/GTIOC3A#/TMRI1/ TMRI5/TXD5/SMOSI5/SSDA5/SSLA1/CTX0/ IRQ8
22	PD3/GTIOC2A-B/TXD1	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/ GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/ CTS1#/RTS1#/SS1#/CTS11#/RTS11#/ SS11#/SSLA0/IRQ5/ADST0
23	PD2/GTIOC2B-B/MOSI-C	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6
24	PD1/GTIOC3A/MISO-C	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/ TMCI0/TMCI6/SCK1/SCK11/IRQ2
25	PD0/GTIOC3B/RSPCK-C	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11
26	TDI	TRCLK/PD2/A7/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/TMCI1/TMO4/SCK5/ SCK8/MOSIA
27	TCK	TRDATA3/PD1/A6/GTIOC3A/GTIOC0B/ GTIOC3A#/GTIOC0B#/TMO2/RXD8/ SMISO8/SSCL8/MISOA
28	TDO	TRDATA2/PD0/A5/GTIOC3B/GTIOC1A/ GTIOC3B#/GTIOC1A#/TMO6/TXD8/ SMOSI8/SSDA8/RSPCKA
29	PB7/SCK2-A	TRDATA1/PB7/A4/GTIOC1B/GTIOC1B#/ SCK5/SCK11/SCK12
30	PB6/RXD2-A/CRX-A	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/ RXD5/SMISO5/SSCL5/RXD11/SMISO11/ SSCL11/RXD12/SMISO12/SSCL12/RXDX12/ CRX0/IRQ2
31	PB5/TXD2-A/CTX-A	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/ TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/ SSDA11/TXD12/SMOSI12/SSDA12/TXDX12/ SIOX12/CTX0
32	PLLVCC	VCC
33	PB4/GTETRG/POE8#/IRQ3	PB4/A1/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/IRQ3_DS
34	PLLVSS	VSS
35	PB3/MTIOC0A-A/SCK0	PC2/CS1#/MTIOC0D/MTIOC0D#/GTADSM0/ SCK8/IRQ15/ADSM0/COMP5
36	PB2/MTIOC0B-A/TXD0/SDA	PC1/A16/MTIOC0C/MTIOC0C#/GTADSM1/ TXD8/SMOSI8/SSDA8/IRQ13/ADSM1/ COMP4
37	PB1/MTIOC0C/RXD0/SCL	PC0/CS0#/MTIOC0B/MTIOC0B#/RXD8/ SMISO8/SSCL8/IRQ12/COMP3

112-Pin	RX62T	RX66T (With PGA Pseudo-Differential Input and Without USB Pins)
38	PB0/MTIOC0D/MOSI-B	PB3/MTIOC0A/MTIOC0A#/CACREF/SCK6/RSPCKA/IRQ9
39	PA5/ADTRG1#-A/MTIOC1A/MISO-B	PB2/MTIOC0B/MTIOC0B#/GTADSM0/TMRI0/TXD6/SMOSI6/SSDA6/SDA/ADSM0
40	PA4/ADTRG0#-A/MTIOC1B/RSPCK-B	PB1/MTIOC0C/MTIOC0C#/GTADSM1/TMCI0/RXD6/SMISO6/SSCL6/SCL/IRQ4/ADSM1
41	PA3/MTIOC2A/SSL0-B	PB0/A0/BC0#/MTIOC0D/MTIOC0D#/TMO0/TXD6/SMOSI6/SSDA6/CTS11#/RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
42	PA2/MTIOC2B/SSL1-B	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/SMISO6/SSCL6/RXD8/SMISO8/SSCL8/MISOA/IRQ1/ADTRG1#
43	PA1/MTIOC6A/SSL2-B	PA4/MTIOC1B/MTIOC1B#/TMCI7/SCK6/TXD8/SMOSI8/SSDA8/RSPCKA/ADTRG0#
44	PA0/MTIOC6C/SSL3-B	PA3/MTIOC2A/MTIOC2A#/GTADSM0/TMRI7/TXD9/SMOSI9/SSDA9/SCK8/SSLA0
45	VCC	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/GTADSM1/TMO7/CTS6#/RTS6#/SS6#/RXD9/SMISO9/SSCL9/SSLA1
46	P96/IRQ4/POE4#	PA1/MTIOC6A/MTIOC6A#/TMO4/TXD9/SMOSI9/SSDA9/RXD11/SMISO11/SSCL11/SSLA2/CRX0/IRQ14_DS/ADTRG0#
47	VSS	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK9/TXD11/SMOSI11/SSDA11/SSLA3/CTX0
48	P95/MTIOC6B	VCC
49	P94/MTIOC7A	P96/CS0#/WAIT#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE4#/CTS8#/RTS8#/SS8#/IRQ4_DS
50	P93/MTIOC7B	VSS
51	P92/MTIOC6D	P95/MTIOC6B/MTIOC6B#/GTIOC4A/GTIOC7A/GTIOC4A#/GTIOC7A#
52	P91/MTIOC7C	P94/MTIOC7A/MTIOC7A#/GTIOC5A/GTIOC8A/GTIOC5A#/GTIOC8A#
53	P90/MTIOC7D	P93/MTIOC7B/MTIOC7B#/GTIOC6A/GTIOC9A/GTIOC6A#/GTIOC9A#
54	PG5/TRCLK	P92/MTIOC6D/MTIOC6D#/GTIOC4B/GTIOC7B/GTIOC4B#/GTIOC7B#
55	PG4/TRDATA3	P91/MTIOC7C/MTIOC7C#/GTIOC5B/GTIOC8B/GTIOC5B#/GTIOC8B#
56	PG3/TRDATA2	P90/MTIOC7D/MTIOC7D#/GTIOC6B/GTIOC9B/GTIOC6B#/GTIOC9B#
57	PG2/IRQ2-B/TRDATA1	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#
58	PG1/IRQ1-C/TRDATA0	P75/D1[A1/D1]/MTIOC4C/MTIOC4C#/GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#
59	PG0/IRQ0-C/TRSYNC	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#
60	P76/MTIOC4D/GTIOC2B-A	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#

112-Pin	RX62T	RX66T (With PGA Pseudo-Differential Input and Without USB Pins)
61	P75/MTIOC4C/GTIOC1B-A	P72/D4[A4/D4]/MTIOC4A/MTIOC4A#/GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#
62	P74/MTIOC3D/GTIOC0B-A	P71/D5[A5/D5]/MTIOC3B/MTIOC3B#/GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#
63	P73/MTIOC4B/GTIOC2A-A	P70/D6[A6/D6]/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE0#/CTS9#/RTS9#/SS9#/IRQ5_DS
64	P72/MTIOC4A/GTIOC1A-A	PG2/D11[A11/D11]/GTETRGA/GTIOC0B/GTIOC0B#/SCK9/IRQ2/COMP0
65	P71/MTIOC3B/GTIOC0A-A	PG1/D12[A12/D12]/GTIOC0A/GTIOC0A#/TXD9/SMOSI9/SSDA9/IRQ1/COMP1
66	P70/IRQ5/POE0#	PG0/D13[A13/D13]/GTIOC1B/GTIOC1B#/RXD9/SMISO9/SSCL9/IRQ0/COMP2
67	P33/MTIOC3A/MTCLKA-A/SSL3-A	P33/D7[A7/D7]/MTIOC3A/MTCLKA/MTIOC3A#/MTCLKA#/GTIOC3B/GTIOC3B#/TMO0/SSLA3/IRQ13_DS
68	P32/MTIOC3C/MTCLKB-A/SSL2-A	P32/D8[A8/D8]/MTIOC3C/MTCLKB/MTIOC3C#/MTCLKB#/GTIOC3A/GTIOC3A#/TMO6/SSLA2/IRQ12_DS
69	VCC	VCC
70	P31/MTIOC0A-B/MTCLKC-A/SSL1-A	P31/D9[A9/D9]/MTIOC0A/MTCLKC/MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6
71	VSS	VSS
72	P30/MTIOC0B-B/MTCLKD-A/SSL0-A	P30/D10[A10/D10]/MTIOC0B/MTCLKD/MTIOC0B#/MTCLKD#/TMCI6/SCK8/CTS8#/RTS8#/SS8#/SSLA0/IRQ7/COMP3
73	P24/RSPCK-A	P27/MTIOC1A/MTIOC0C/MTIOC1A#/MTIOC0C#/POE9#/IRQ15
74	P23/CTX-B/LTX/MOSI-A	P24/D11[A11/D11]/MTIC5U/MTIC5U#/TMCI2/TMO6/CTS8#/RTS8#/SS8#/SCK8/RSPCKA/IRQ4/COMP0
75	P22/ADTRG#/CRX-B/LRX/MISO-A	P23/D12[A12/D12]/MTIC5V/MTIC5V#/TMO2/CACREF/TXD8/SMOSI8/SSDA8/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/MOSIA/CTX0/IRQ11/COMP1
76	P21/ADTRG1#-B/MTCLKA-B/IRQ6	P22/D13[A13/D13]/MTIC5W/MTCLKD/MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/TMO4/RXD8/SMISO8/SSCL8/RXD12/SMISO12/SSCL12/RXDX12/MISOA/CRX0/IRQ10/ADTRG2#/COMP2
77	P20/ADTRG0#-B/MTCLKB-B/IRQ7	P21/D14[A14/D14]/MTIOC9A/MTCLKA/MTIOC9A#/MTCLKA#/TMCI4/TXD8/SMOSI8/SSDA8/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/MOSIA/IRQ6_DS/AN217/ADTRG1#/COMP5
78	P65/AN5	P20/D15[A15/D15]/MTIOC9C/MTCLKB/MTIOC9C#/MTCLKB#/TMRI4/CTS8#/RTS8#/SS8#/SCK8/RSPCKA/IRQ7_DS/AN216/ADTRG0#/COMP4
79	P64/AN4	P65/A12/IRQ9/AN211/CMPC53/DA1
80	AVCC	P64/A13/IRQ8/AN210/CMPC33/DA0

112-Pin	RX62T	RX66T (With PGA Pseudo-Differential Input and Without USB Pins)
81	VREF	AVCC2
82	AVSS	AVSS2
83	P63/AN3	P63/A14/IRQ7/AN209/CMPC23
84	P62/AN2	P62/A15/IRQ6/AN208/CMPC43
85	P61/AN1	P61/A16/IRQ5/AN207/CMPC13
86	P60/AN0	P60/A17/IRQ4/AN206/CMPC03
87	P55/AN11	P55/A18/IRQ3/AN203/CMPC32
88	P54/AN10	P54/A19/IRQ2/AN202/CMPC22
89	P53/AN9	P53/A20/IRQ1/AN201/CMPC12
90	P52/AN8	P52/IRQ0/AN200/CMPC02
91	P51/AN7	P47/AN103
92	P50/AN6	P46/AN102/CMPC50/CMPC51
93	P47/AN103/CVREFH	P45/AN101/CMPC40/CMPC41
94	P46/AN102	P44/AN100/CMPC30/CMPC31
95	P45/AN101	PH4/AN107/PGAVSS1
96	P44/AN100	P43/AN003
97	P43/AN003/CVREFL	P42/AN002/CMPC20/CMPC21
98	P42/AN002	P41/AN001/CMPC10/CMPC11
99	P41/AN001	P40/AN000/CMPC00/CMPC01
100	P40/AN000	PH0/AN007/PGAVSS0
101	AVCC0	AVCC1
102	VREFH0	AVCC0
103	VREFL0	AVSS0
104	AVSS0	AVSS1
105	P82/MTIC5U/SCK2-B	P82/ALE/WAIT#/MTIC5U/MTIC5U#/TMO4/SCK6/SCK12/IRQ3/COMP5
106	P81/MTIC5V/TXD2-B	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/TXD6/SMOSI6/SSDA6/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/COMP4
107	P80/MTIC5W/RXD2-B	P80/CS1#/MTIC5W/MTIC5W#/TMRI4/RXD6/SMISO6/SSCL6/RXD12/SMISO12/SSCL12/RXDX12/IRQ5/COMP3
108	WDTOVF#	P11/RD#/MTIOC3A/MTCLKC/MTIOC3A#/MTCLKC#/MTIOC9D/GTIOC3B/GTETRGA/GTIOC3B#/GTETRGC/TMO3/POE9#/IRQ1_DS
109	P11/MTCLKC-B/IRQ1-A	P10/MTIOC9B/MTCLKD/MTIOC9B#/MTCLKD#/GTETRGB/GTETRGD/TMRI3/POE12#/CTS6#/RTS6#/SS6#/IRQ0_DS
110	P10/MTCLKD-B/IRQ0-A	P17/MTIOC4D/MTIOC4D#/GTIOC2B/GTIOC9B/GTIOC2B#/GTIOC9B#/IRQ14
111	TRST#	P16/MTIOC4C/MTIOC4C#/GTIOC1B/GTIOC8B/GTIOC1B#/GTIOC8B#/IRQ13
112	TMS	P15/MTIOC3D/MTIOC3D#/GTIOC0B/GTIOC7B/GTIOC0B#/GTIOC7B#/IRQ12

3.2 100-Pin Package (RX66T: With PGA Pseudo-Differential Input and USB Pins)

Table 3.2 is a comparative listing of the pin functions of 100-pin package products (RX66T: with PGA pseudo-differential input and USB pins).

Table 3.2 Comparative Listing of 100-Pin Package Pin Functions (RX66T: With PGA Pseudo-Differential Input and USB Pins)

100-Pin	RX62T	RX66T (With PGA Pseudo-Differential Input and USB Pins)
1	PE5/IRQ0-B	PE5/BCLK/MTIOC9D/MTIOC9D#/GTIOC3A/GTETRGB/GTIOC3A#/GTETRGD/SCK9/CTS9#/RTS9#/SS9#/IRQ0/ADST0
2	EMLE	EMLE
3	VSS	VSS
4	MDE	UB/P00/A11/MTIOC9A/MTIOC9A#/CACREF/RXD9/SMISO9/SSCL9/RXD12/SMISO12/SSCL12/RXDX12/IRQ2/ADST1/COMP0
5	VCL	VCL
6	MD1	MD/FINED
7	MD0	P01/A10/MTIOC9C/MTIOC9C#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE12#/TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/IRQ4/ADST2/COMP1
8	PE4/MTCLKC-C/POE10#-B/IRQ1-B	PE4/A9/MTCLKC/MTCLKC#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE10#/SCK9/IRQ1
9	PE3/MTCLKD-C/POE11#/IRQ2-A	PE3/A8/MTCLKD/MTCLKD#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE11#/CTS9#/RTS9#/SS9#/IRQ2_DS
10	RES#	RES#
11	XTAL	XTAL/P37
12	VSS	VSS
13	EXTAL	EXTAL/P36
14	VCC	VCC
15	PE2/POE10#-A/NMI	UPSEL/PE2/POE10#/NMI
16	PE1/SSL3-C	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/CTS12#/RTS12#/SS12#/SSLA3/IRQ15
17	PE0/SSL2-C/CRX-C	PE0/WR1#/BC1#/WAIT#/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/SSCL5/SSLA2/CRX0/USB0_OVRCURB/IRQ7
18	TRST#/PD7/GTIOC0A-B/SSL1-C/CTX-C	TRST#/PD7/MTIOC9A/MTIOC9A#/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/SSDA5/SSLA1/CTX0/IRQ8
19	TMS/PD6/GTIOC0B-B/SSL0-C	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/CTS1#/RTS1#/SS1#/CTS11#/RTS11#/SS11#/SSLA0/IRQ5/ADST0

100-Pin	RX62T	RX66T (With PGA Pseudo-Differential Input and USB Pins)
20	TDI/PD5/GTIOC1A-B/RXD1	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/TMRI0/TMRI6/RXD1/SMISO1/SSCL1/RXD11/SMISO11/SSCL11/IRQ6
21	TCK/PD4/GTIOC1B-B/SCK1	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/TMCI0/TMCI6/SCK1/SCK11/IRQ2
22	TDO/PD3/GTIOC2A-B/TXD1	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/TMO0/TXD1/SMOSI1/SSDA1/TXD11/SMOSI11/SSDA11
23	TRCLK/PD2/GTIOC2B-B/MOSI-C	TRCLK/PD2/A7/GTIOC2B/GTIOC0A/GTIOC2B#/GTIOC0A#/TMCI1/TMO4/SCK5/SCK8/MOSIA/USB0_VBUS
24	TRDATA3/PD1/GTIOC3A/MISO-C	USB0_DM
25	TRDATA2/PD0/GTIOC3B/RSPCK-C	USB0_DP
26	TRDATA1/PB7/SCK2-A	VCC_USB
27	TRDATA0/PB6/RXD2-A/CRX-A	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/RXD5/SMISO5/SSCL5/RXD11/SMISO11/SSCL11/RXD12/SMISO12/SSCL12/RXDX12/CRX0/USB0_OVRCURA/IRQ2
28	TRSYNC/PB5/TXD2-A/CTX-A	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/SSDA11/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/CTX0/USB0_VBUSEN
29	PLLVCC	VCC
30	PB4/GTETRG/POE8#/IRQ3	PB4/A1/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE8#/CTS5#/RTS5#/SS5#/SCK11/CTS11#/RTS11#/SS11#/USB0_OVRCURB/IRQ3_DS
31	PLLVSS	VSS/VSS_USB
32	PB3/MTIOC0A-A/SCK0	PB3/A7/MTIOC0A/MTIOC0A#/CACREF/SCK6/RSPCKA/IRQ9
33	PB2/MTIOC0B-A/TXD0/SDA	PB2/A6/MTIOC0B/MTIOC0B#/GTADSM0/TMRI0/TXD6/SMOSI6/SSDA6/SDA/ADSM0
34	PB1/MTIOC0C/RXD0/SCL	PB1/A5/MTIOC0C/MTIOC0C#/GTADSM1/TMCI0/RXD6/SMISO6/SSCL6/SCL/IRQ4/ADSM1
35	PB0/MTIOC0D/MOSI-B	PB0/A0/A4/BC0#/MTIOC0D/MTIOC0D#/TMO0/TXD6/SMOSI6/SSDA6/CTS11#/RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
36	PA5/MTIOC1A/MISO-B/ADTRG1#-A	PA5/A3/MTIOC1A/MTIOC1A#/TMCI3/RXD6/SMISO6/SSCL6/RXD8/SMISO8/SSCL8/MISOA/IRQ1/ADTRG1#
37	PA4/MTIOC1B/RSPCK-B/ADTRG0#-A	PA4/A2/MTIOC1B/MTIOC1B#/TMCI7/SCK6/TXD8/SMOSI8/SSDA8/RSPCKA/ADTRG0#
38	PA3/MTIOC2A/SSL0-B	PA3/A1/MTIOC2A/MTIOC2A#/GTADSM0/TMRI7/TXD9/SMOSI9/SSDA9/SCK8/SSLA0
39	PA2/MTIOC2B/SSL1-B	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/GTADSM1/TMO7/CTS6#/RTS6#/SS6#/RXD9/SMISO9/SSCL9/SCK11/SSLA1

100-Pin	RX62T	RX66T (With PGA Pseudo-Differential Input and USB Pins)
40	PA1/MTIOC6A/SSL2-B	PA1/MTIOC6A/MTIOC6A#/TMO4/TXD9/SMOSI9/SSDA9/RXD11/SMISO11/SSCL11/SSLA2/CRX0/USB0_ID/USB0_OVRCURA/IRQ14_DS/ADTRG0#
41	PA0/MTIOC6C/SSL3-B	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK9/TXD11/SMOSI11/SSDA11/SSLA3/CTX0/USB0_EXICEN/USB0_VBUSEN
42	VCC	VCC
43	P96/POE4#/IRQ4	P96/CS0#/WAIT#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE4#/CTS8#/RTS8#/SS8#/IRQ4_DS
44	VSS	VSS
45	P95/MTIOC6B	P95/MTIOC6B/MTIOC6B#/GTIOC4A/GTIOC7A/GTIOC4A#/GTIOC7A#
46	P94/MTIOC7A	P94/MTIOC7A/MTIOC7A#/GTIOC5A/GTIOC8A/GTIOC5A#/GTIOC8A#
47	P93/MTIOC7B	P93/MTIOC7B/MTIOC7B#/GTIOC6A/GTIOC9A/GTIOC6A#/GTIOC9A#
48	P92/MTIOC6D	P92/MTIOC6D/MTIOC6D#/GTIOC4B/GTIOC7B/GTIOC4B#/GTIOC7B#
49	P91/MTIOC7C	P91/MTIOC7C/MTIOC7C#/GTIOC5B/GTIOC8B/GTIOC5B#/GTIOC8B#
50	P90/MTIOC7D	P90/MTIOC7D/MTIOC7D#/GTIOC6B/GTIOC9B/GTIOC6B#/GTIOC9B#
51	P76/MTIOC4D/GTIOC2B-A	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#
52	P75/MTIOC4C/GTIOC1B-A	P75/D1[A1/D1]/MTIOC4C/MTIOC4C#/GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#
53	P74/MTIOC3D/GTIOC0B-A	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#
54	P73/MTIOC4B/GTIOC2A-A	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#
55	P72/MTIOC4A/GTIOC1A-A	P72/D4[A4/D4]/MTIOC4A/MTIOC4A#/GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#
56	P71/MTIOC3B/GTIOC0A-A	P71/D5[A5/D5]/MTIOC3B/MTIOC3B#/GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#
57	P70/POE0#/IRQ5	P70/D6[A6/D6]/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE0#/CTS9#/RTS9#/SS9#/IRQ5_DS
58	P33/MTIOC3A/MTCLKA-A/SSL3-A	P33/D7[A7/D7]/MTIOC3A/MTCLKA/MTIOC3A#/MTCLKA#/GTIOC3B/GTIOC3B#/TMO0/SSLA3/IRQ13_DS
59	P32/MTIOC3C/MTCLKB-A/SSL2-A	P32/D8[A8/D8]/MTIOC3C/MTCLKB/MTIOC3C#/MTCLKB#/GTIOC3A/GTIOC3A#/TMO6/SSLA2/IRQ12_DS
60	VCC	VCC
61	P31/MTIOC0A-B/MTCLKC-A/SSL1-A	P31/D9[A9/D9]/MTIOC0A/MTCLKC/MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6
62	VSS	VSS

100-Pin	RX62T	RX66T (With PGA Pseudo-Differential Input and USB Pins)
63	P30/MTIOC0B-B/MTCLKD-A/SSL0-A	P30/D10[A10/D10]/MTIOC0B/MTCLKD/MTIOC0B#/MTCLKD#/TMCI6/SCK8/CTS8#/RTS8#/SS8#/SSLA0/IRQ7/COMP3
64	P24/RSPCK-A	P27/CS3#/MTIOC1A/MTIOC0C/MTIOC1A#/MTIOC0C#/POE9#/IRQ15
65	P23/CTX-B/LTX/MOSI-A	P24/D11[A11/D11]/MTIC5U/MTIC5U#/TMCI2/TMO6/CTS8#/RTS8#/SS8#/SCK8/RSPCKA/IRQ4/COMP0
66	P22/CRX-B/LRX/MISO-A/ADTRG#	P23/D12[A12/D12]/MTIC5V/MTIC5V#/TMO2/CACREF/TXD8/SMOSI8/SSDA8/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/MOSIA/CTX0/IRQ11/COMP1
67	P21/MTCLKA-B/IRQ6/ADTRG1#-B	P22/D13[A13/D13]/MTIC5W/MTCLKD/MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/TMO4/RXD8/SMISO8/SSCL8/RXD12/SMISO12/SSCL12/RXDX12/MISOA/CRX0/IRQ10/ADTRG2#/COMP2
68	P20/MTCLKB-B/IRQ7/ADTRG0#-B	P21/D14[A14/D14]/MTIOC9A/MTCLKA/MTIOC9A#/MTCLKA#/TMCI4/TXD8/SMOSI8/SSDA8/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/MOSIA/IRQ6_DS/AN217/ADTRG1#/COMP5
69	P65/AN5	P20/D15[A15/D15]/MTIOC9C/MTCLKB/MTIOC9C#/MTCLKB#/TMRI4/CTS8#/RTS8#/SS8#/SCK8/RSPCKA/IRQ7_DS/AN216/ADTRG0#/COMP4
70	P64/AN4	P65/A12/IRQ9/AN211/CMPC53/DA1
71	AVCC	P64/A13/IRQ8/AN210/CMPC33/DA0
72	VREF	AVCC2
73	AVSS	AVSS2
74	P63/AN3	P63/A12/A14/IRQ7/AN209/CMPC23
75	P62/AN2	P62/A13/A15/IRQ6/AN208/CMPC43
76	P61/AN1	P61/A14/A16/IRQ5/AN207/CMPC13
77	P60/AN0	P60/A15/A17/IRQ4/AN206/CMPC03
78	P55/AN11	P55/A16/A18/IRQ3/AN203/CMPC32
79	P54/AN10	P54/A17/A19/IRQ2/AN202/CMPC22
80	P53/AN9	P53/A18/A20/IRQ1/AN201/CMPC12
81	P52/AN8	P52/IRQ0/AN200/CMPC02
82	P51/AN7	P47/AN103
83	P50/AN6	P46/AN102/CMPC50/CMPC51
84	P47/AN103/CVREFH	P45/AN101/CMPC40/CMPC41
85	P46/AN102	P44/AN100/CMPC30/CMPC31
86	P45/AN101	PH4/AN107/PGAVSS1
87	P44/AN100	P43/AN003
88	P43/AN003/CVREFL	P42/AN002/CMPC20/CMPC21
89	P42/AN002	P41/AN001/CMPC10/CMPC11
90	P41/AN001	P40/AN000/CMPC00/CMPC01
91	P40/AN000	PH0/AN007/PGAVSS0
92	AVCC0	AVCC1
93	VREFH0	AVCC0

100-Pin	RX62T	RX66T (With PGA Pseudo-Differential Input and USB Pins)
94	VREFL0	AVSS0
95	AVSS0	AVSS1
96	P82/MTIC5U/SCK2-B	P82/ALE/WAIT#/MTIC5U/MTIC5U#/TMO4/SCK6/SCK12/IRQ3/COMP5
97	P81/MTIC5V/TXD2-B	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/TXD6/SMOSI6/SSDA6/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/COMP4
98	P80/MTIC5W/RXD2-B	P80/CS1#/MTIC5W/MTIC5W#/TMRI4/RXD6/SMISO6/SSCL6/RXD12/SMISO12/SSCL12/RXDX12/IRQ5/COMP3
99	P11/MTCLKC-B/IRQ1-A	P11/RD#/MTIOC3A/MTCLKC/MTIOC3A#/MTCLKC#/MTIOC9D/GTIOC3B/GTETRGA/GTIOC3B#/GTETRGC/TMO3/POE9#/IRQ1_DS
100	P10/MTCLKD-B/IRQ0-A	P10/MTIOC9B/MTCLKD/MTIOC9B#/MTCLKD#/GTETRGB/GTETRGD/TMRI3/POE12#/CTS6#/RTS6#/SS6#/IRQ0_DS

3.3 100-Pin Package (RX66T: With PGA Pseudo-Differential Input and Without USB Pins)

Table 3.3 is a comparative listing of the pin functions of 100-pin package products (RX66T: with PGA pseudo-differential input and without USB pins).

Table 3.3 Comparative Listing of 100-Pin Package Pin Functions (RX66T: With PGA Pseudo-Differential Input and Without USB Pins)

100-Pin	RX62T	RX66T (With PGA Pseudo-Differential Input and Without USB Pins)
1	PE5/IRQ0-B	PE5/BCLK/MTIOC9D/MTIOC9D#/GTIOC3A/GTETRGB/GTIOC3A#/GTETRGD/SCK9/CTS9#/RTS9#/SS9#/IRQ0/ADST0
2	EMLE	EMLE
3	VSS	VSS
4	MDE	UB/P00/A11/MTIOC9A/MTIOC9A#/CACREF/RXD9/SMISO9/SSCL9/RXD12/SMISO12/SSCL12/RXDX12/IRQ2/ADST1/COMP0
5	VCL	VCL
6	MD1	MD/FINED
7	MD0	P01/A10/MTIOC9C/MTIOC9C#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE12#/TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/IRQ4/ADST2/COMP1
8	PE4/MTCLKC-C/POE10#-B/IRQ1-B	PE4/A9/MTCLKC/MTCLKC#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE10#/SCK9/IRQ1
9	PE3/MTCLKD-C/POE11#/IRQ2-A	PE3/A8/MTCLKD/MTCLKD#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE11#/CTS9#/RTS9#/SS9#/IRQ2_DS
10	RES#	RES#
11	XTAL	XTAL/P37
12	VSS	VSS
13	EXTAL	EXTAL/P36
14	VCC	VCC
15	PE2/POE10#-A/NMI	PE2/POE10#/NMI
16	PE1/SSL3-C	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/CTS12#/RTS12#/SS12#/SSLA3/IRQ15
17	PE0/SSL2-C/CRX-C	PE0/WR1#/BC1#/WAIT#/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/SSCL5/SSLA2/CRX0/IRQ7
18	TRST#/PD7/GTIOC0A-B/SSL1-C/CTX-C	TRST#/PD7/MTIOC9A/MTIOC9A#/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/SSDA5/SSLA1/CTX0/IRQ8
19	TMS/PD6/GTIOC0B-B/SSL0-C	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/CTS1#/RTS1#/SS1#/CTS11#/RTS11#/SS11#/SSLA0/IRQ5/ADST0

100-Pin	RX62T	RX66T (With PGA Pseudo-Differential Input and Without USB Pins)
20	TDI/PD5/GTIOC1A-B/RXD1	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/TMRI0/TMRI6/RXD1/SMISO1/SSCL1/RXD11/SMISO11/SSCL11/IRQ6
21	TCK/PD4/GTIOC1B-B/SCK1	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/TMCI0/TMCI6/SCK1/SCK11/IRQ2
22	TDO/PD3/GTIOC2A-B/TXD1	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/TMO0/TXD1/SMOSI1/SSDA1/TXD11/SMOSI11/SSDA11
23	TRCLK/PD2/GTIOC2B-B/MOSI-C	TRCLK/PD2/A7/GTIOC2B/GTIOC0A/GTIOC2B#/GTIOC0A#/TMCI1/TMO4/SCK5/SCK8/MOSIA
24	TRDATA3/PD1/GTIOC3A/MISO-C	TRDATA3/PD1/A6/GTIOC3A/GTIOC0B/GTIOC3A#/GTIOC0B#/TMO2/RXD8/SMISO8/SSCL8/MISOA
25	TRDATA2/PD0/GTIOC3B/RSPCK-C	TRDATA2/PD0/A5/GTIOC3B/GTIOC1A/GTIOC3B#/GTIOC1A#/TMO6/TXD8/SMOSI8/SSDA8/RSPCKA
26	TRDATA1/PB7/SCK2-A	TRDATA1/PB7/A4/GTIOC1B/GTIOC1B#/SCK5/SCK11/SCK12
27	TRDATA0/PB6/RXD2-A/CRX-A	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/RXD5/SMISO5/SSCL5/RXD11/SMISO11/SSCL11/RXD12/SMISO12/SSCL12/RXDX12/CRX0/IRQ2
28	TRSYNC/PB5/TXD2-A/CTX-A	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/TXD5/ SMOSI5/SSDA5/TXD11/SMOSI11/SSDA11/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/CTX0
29	PLLVCC	VCC
30	PB4/GTETRG/POE8#/IRQ3	PB4/A1/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE8#/CTS5#/RTS5#/SS5#/SCK11/CTS11#/RTS11#/SS11#/IRQ3_DS
31	PLLVSS	VSS
32	PB3/MTIOC0A-A/SCK0	PB3/A7*1/MTIOC0A/MTIOC0A#/CACREF/SCK6/RSPCKA/IRQ9
33	PB2/MTIOC0B-A/TXD0/SDA	PB2/A6*1/MTIOC0B/MTIOC0B#/GTADSM0/TMRI0/TXD6/SMOSI6/SSDA6/SDA/ADSM0
34	PB1/MTIOC0C/RXD0/SCL	PB1/A5*1/MTIOC0C/MTIOC0C#/GTADSM1/TMCI0/RXD6/SMISO6/SSCL6/SCL/IRQ4/ADSM1
35	PB0/MTIOC0D/MOSI-B	PB0/A0/A4*1/BC0#/MTIOC0D/MTIOC0D#/TMO0/TXD6/SMOSI6/SSDA6/CTS11#/RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
36	PA5/MTIOC1A/MISO-B/ADTRG1#-A	PA5/A3*1/MTIOC1A/MTIOC1A#/TMCI3/RXD6/SMISO6/SSCL6/RXD8/SMISO8/SSCL8/MISOA/IRQ1/ADTRG1#
37	PA4/MTIOC1B/RSPCK-B/ADTRG0#-A	PA4/A2*1/MTIOC1B/MTIOC1B#/TMCI7/SCK6/TXD8/SMOSI8/SSDA8/RSPCKA/ADTRG0#
38	PA3/MTIOC2A/SSL0-B	PA3/A1*1/MTIOC2A/MTIOC2A#/GTADSM0/TMRI7/TXD9/SMOSI9/SSDA9/SCK8/SSLA0

100-Pin	RX62T	RX66T (With PGA Pseudo-Differential Input and Without USB Pins)
39	PA2/MTIOC2B/SSL1-B	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/GTADSM1/TMO7/CTS6#/RTS6#/SS6#/RXD9/SMISO9/SSCL9/SCK11*1/SSLA1
40	PA1/MTIOC6A/SSL2-B	PA1/MTIOC6A/MTIOC6A#/TMO4/TXD9/SMOSI9/SSDA9/RXD11/SMISO11/SSCL11/SSLA2/CRX0/IRQ14_DS/ADTRG0#
41	PA0/MTIOC6C/SSL3-B	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK9/TXD11/SMOSI11/SSDA11/SSLA3/CTX0
42	VCC	VCC
43	P96/POE4#/IRQ4	P96/CS0#/WAIT#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE4#/CTS8#/RTS8#/SS8#/IRQ4_DS
44	VSS	VSS
45	P95/MTIOC6B	P95/MTIOC6B/MTIOC6B#/GTIOC4A/GTIOC7A/GTIOC4A#/GTIOC7A#
46	P94/MTIOC7A	P94/MTIOC7A/MTIOC7A#/GTIOC5A/GTIOC8A/GTIOC5A#/GTIOC8A#
47	P93/MTIOC7B	P93/MTIOC7B/MTIOC7B#/GTIOC6A/GTIOC9A/GTIOC6A#/GTIOC9A#
48	P92/MTIOC6D	P92/MTIOC6D/MTIOC6D#/GTIOC4B/GTIOC7B/GTIOC4B#/GTIOC7B#
49	P91/MTIOC7C	P91/MTIOC7C/MTIOC7C#/GTIOC5B/GTIOC8B/GTIOC5B#/GTIOC8B#
50	P90/MTIOC7D	P90/MTIOC7D/MTIOC7D#/GTIOC6B/GTIOC9B/GTIOC6B#/GTIOC9B#
51	P76/MTIOC4D/GTIOC2B-A	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#
52	P75/MTIOC4C/GTIOC1B-A	P75/D1[A1/D1]/MTIOC4C/MTIOC4C#/GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#
53	P74/MTIOC3D/GTIOC0B-A	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#
54	P73/MTIOC4B/GTIOC2A-A	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#
55	P72/MTIOC4A/GTIOC1A-A	P72/D4[A4/D4]/MTIOC4A/MTIOC4A#/GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#
56	P71/MTIOC3B/GTIOC0A-A	P71/D5[A5/D5]/MTIOC3B/MTIOC3B#/GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#
57	P70/POE0#/IRQ5	P70/D6[A6/D6]/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE0#/CTS9#/RTS9#/SS9#/IRQ5_DS
58	P33/MTIOC3A/MTCLKA-A/SSL3-A	P33/D7[A7/D7]/MTIOC3A/MTCLKA/MTIOC3A#/MTCLKA#/GTIOC3B/GTIOC3B#/TMO0/SSLA3/IRQ13_DS
59	P32/MTIOC3C/MTCLKB-A/SSL2-A	P32/D8[A8/D8]/MTIOC3C/MTCLKB/MTIOC3C#/MTCLKB#/GTIOC3A/GTIOC3A#/TMO6/SSLA2/IRQ12_DS
60	VCC	VCC
61	P31/MTIOC0A-B/MTCLKC-A/SSL1-A	P31/D9[A9/D9]/MTIOC0A/MTCLKC/MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6
62	VSS	VSS

100-Pin	RX62T	RX66T (With PGA Pseudo-Differential Input and Without USB Pins)
63	P30/MTIOC0B-B/MTCLKD-A/SSL0-A	P30/D10[A10/D10]/MTIOC0B/MTCLKD/MTIOC0B#/MTCLKD#/TMCI6/SCK8/CTS8#/RTS8#/SS8#/SSLA0/IRQ7/COMP3
64	P24/RSPCK-A	P27/CS3#*1/MTIOC1A/MTIOC0C/MTIOC1A#/MTIOC0C#/POE9#/IRQ15
65	P23/CTX-B/LTX/MOSI-A	P24/D11[A11/D11]/MTIC5U/MTIC5U#/TMCI2/TMO6/CTS8#/RTS8#/SS8#/SCK8/RSPCKA/IRQ4/COMP0
66	P22/CRX-B/LRX/MISO-A/ADTRG#	P23/D12[A12/D12]/MTIC5V/MTIC5V#/TMO2/CACREF/TXD8/SMOSI8/SSDA8/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/MOSIA/CTX0/IRQ11/COMP1
67	P21/MTCLKA-B/IRQ6/ADTRG1#-B	P22/D13[A13/D13]/MTIC5W/MTCLKD/MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/TMO4/RXD8/SMISO8/SSCL8/RXD12/SMISO12/SSCL12/RXDX12/MISOA/CRX0/IRQ10/ADTRG2#/COMP2
68	P20/MTCLKB-B/IRQ7/ADTRG0#-B	P21/D14[A14/D14]/MTIOC9A/MTCLKA/MTIOC9A#/MTCLKA#/TMCI4/TXD8/SMOSI8/SSDA8/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/MOSIA/IRQ6_DS/AN217/ADTRG1#/COMP5
69	P65/AN5	P20/D15[A15/D15]/MTIOC9C/MTCLKB/MTIOC9C#/MTCLKB#/TMRI4/CTS8#/RTS8#/SS8#/SCK8/RSPCKA/IRQ7_DS/AN216/ADTRG0#/COMP4
70	P64/AN4	P65/A12/IRQ9/AN211/CMPC53/DA1
71	AVCC	P64/A13/IRQ8/AN210/CMPC33/DA0
72	VREF	AVCC2
73	AVSS	AVSS2
74	P63/AN3	P63/A12*1/A14/IRQ7/AN209/CMPC23
75	P62/AN2	P62/A13*1/A15/IRQ6/AN208/CMPC43
76	P61/AN1	P61/A14*1/A16/IRQ5/AN207/CMPC13
77	P60/AN0	P60/A15*1/A17/IRQ4/AN206/CMPC03
78	P55/AN11	P55/A16*1/A18/IRQ3/AN203/CMPC32
79	P54/AN10	P54/A17*1/A19/IRQ2/AN202/CMPC22
80	P53/AN9	P53/A18*1/A20/IRQ1/AN201/CMPC12
81	P52/AN8	P52/IRQ0/AN200/CMPC02
82	P51/AN7	P47/AN103
83	P50/AN6	P46/AN102/CMPC50/CMPC51
84	P47/AN103/CVREFH	P45/AN101/CMPC40/CMPC41
85	P46/AN102	P44/AN100/CMPC30/CMPC31
86	P45/AN101	PH4/AN107/PGAVSS1
87	P44/AN100	P43/AN003
88	P43/AN003/CVREFL	P42/AN002/CMPC20/CMPC21
89	P42/AN002	P41/AN001/CMPC10/CMPC11
90	P41/AN001	P40/AN000/CMPC00/CMPC01
91	P40/AN000	PH0/AN007/PGAVSS0
92	AVCC0	AVCC1
93	VREFH0	AVCC0

100-Pin	RX62T	RX66T (With PGA Pseudo-Differential Input and Without USB Pins)
94	VREFL0	AVSS0
95	AVSS0	AVSS1
96	P82/MTIC5U/SCK2-B	P82/ALE/WAIT#/MTIC5U/MTIC5U#/TMO4/SCK6/SCK12/IRQ3/COMP5
97	P81/MTIC5V/TXD2-B	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/TXD6/SMOSI6/SSDA6/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/COMP4
98	P80/MTIC5W/RXD2-B	P80/CS1#/MTIC5W/MTIC5W#/TMRI4/RXD6/SMISO6/SSCL6/RXD12/SMISO12/SSCL12/RXDX12/IRQ5/COMP3
99	P11/MTCLKC-B/IRQ1-A	P11/RD#/MTIOC3A/MTCLKC/MTIOC3A#/MTCLKC#/MTIOC9D/GTIOC3B/GTETRGA/GTIOC3B#/GTETRGC/TMO3/POE9#/IRQ1_DS
100	P10/MTCLKD-B/IRQ0-A	P10/MTIOC9B/MTCLKD/MTIOC9B#/MTCLKD#/GTETRGB/GTETRGD/TMRI3/POE12#/CTS6#/RTS6#/SS6#/IRQ0_DS

Note: 1. These pins are only enabled for products with 128 KB of RAM.

3.4 100-Pin Package (RX66T: Without PGA Pseudo-Differential Input and USB Pins)

Table 3.4 is a comparative listing of the pin functions of 100-pin package products (RX66T: without PGA pseudo-differential input and USB pins).

Table 3.4 Comparative Listing of 100-Pin Package Pin Functions (RX66T: Without PGA Pseudo-Differential Input and USB Pins)

100-Pin	RX62T	RX66T (Without PGA Pseudo-Differential Input and USB Pins)
1	PE5/IRQ0-B	PE5/BCLK/MTIOC9D/MTIOC9D#/GTIOC3A/GTETRGB/GTIOC3A#/GTETRGD/SCK9/CTS9#/RTS9#/SS9#/IRQ0/ADST0
2	EMLE	EMLE
3	VSS	VSS
4	MDE	UB/P00/A11/MTIOC9A/MTIOC9A#/CACREF/RXD9/SMISO9/SSCL9/RXD12/SMISO12/SSCL12/RXDX12/IRQ2/ADST1/COMP0
5	VCL	VCL
6	MD1	MD/FINED
7	MD0	P01/A10/MTIOC9C/MTIOC9C#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE12#/TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/IRQ4/ADST2/COMP1
8	PE4/MTCLKC-C/POE10#-B/IRQ1-B	PE4/A9/MTCLKC/MTCLKC#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE10#/SCK9/IRQ1
9	PE3/MTCLKD-C/POE11#/IRQ2-A	PE3/A8/MTCLKD/MTCLKD#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE11#/CTS9#/RTS9#/SS9#/IRQ2_DS
10	RES#	RES#
11	XTAL	XTAL/P37
12	VSS	VSS
13	EXTAL	EXTAL/P36
14	VCC	VCC
15	PE2/POE10#-A/NMI	PE2/POE10#/NMI
16	PE1/SSL3-C	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/CTS12#/RTS12#/SS12#/SSLA3/IRQ15
17	PE0/SSL2-C/CRX-C	PE0/WR1#/BC1#/WAIT#/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/SSCL5/SSLA2/CRX0/IRQ7
18	TRST#/PD7/GTIOC0A-B/SSL1-C/CTX-C	TRST#/PD7/MTIOC9A/MTIOC9A#/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/SSDA5/SSLA1/CTX0/IRQ8
19	TMS/PD6/GTIOC0B-B/SSL0-C	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/CTS1#/RTS1#/SS1#/CTS11#/RTS11#/SS11#/SSLA0/IRQ5/ADST0
20	TDI/PD5/GTIOC1A-B/RXD1	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/TMRI0/TMRI6/RXD1/SMISO1/SSCL1/RXD11/SMISO11/SSCL11/IRQ6

100-Pin	RX62T	RX66T (Without PGA Pseudo-Differential Input and USB Pins)
21	TCK/PD4/GTIOC1B-B/SCK1	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/TMCI0/TMCI6/SCK1/SCK11/IRQ2
22	TDO/PD3/GTIOC2A-B/TXD1	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/TMO0/TXD1/SMOSI1/SSDA1/TXD11/SMOSI11/SSDA11
23	TRCLK/PD2/GTIOC2B-B/MOSI-C	TRCLK/PD2/A7/GTIOC2B/GTIOC0A/GTIOC2B#/GTIOC0A#/TMCI1/TMO4/SCK5/SCK8/MOSIA
24	TRDATA3/PD1/GTIOC3A/MISO-C	TRDATA3/PD1/A6/GTIOC3A/GTIOC0B/GTIOC3A#/GTIOC0B#/TMO2/RXD8/SMISO8/SSCL8/MISOA
25	TRDATA2/PD0/GTIOC3B/RSPCK-C	TRDATA2/PD0/A5/GTIOC3B/GTIOC1A/GTIOC3B#/GTIOC1A#/TMO6/TXD8/SMOSI8/SSDA8/RSPCKA
26	TRDATA1/PB7/SCK2-A	TRDATA1/PB7/A4/GTIOC1B/GTIOC1B#/SCK5/SCK11/SCK12
27	TRDATA0/PB6/CRX-A/RXD2-A	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/RXD5/SMISO5/SSCL5/RXD11/SMISO11/SSCL11/RXD12/SMISO12/SSCL12/RXDX12/CRX0/IRQ2
28	TRSYNC/PB5/TXD2-A/CTX-A	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/SSDA11/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/CTX0
29	PLLVCC	VCC
30	PB4/GTETRG/POE8#/IRQ3	PB4/A1/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE8#/CTS5#/RTS5#/SS5#/SCK11/CTS11#/RTS11#/SS11#/IRQ3_DS
31	PLLVSS	VSS
32	PB3/MTIOC0A-A/SCK0	PB3/A7*1/MTIOC0A/MTIOC0A#/CACREF/SCK6/ RSPCKA/IRQ9
33	PB2/MTIOC0B-A/TXD0/SDA	PB2/A6*1/MTIOC0B/MTIOC0B#/GTADSM0/TMRI0/TXD6/SMOSI6/SSDA6/SDA/ADSM0
34	PB1/MTIOC0C/RXD0/SCL	PB1/A5*1/MTIOC0C/MTIOC0C#/GTADSM1/TMCI0/RXD6/SMISO6/SSCL6/SCL/IRQ4/ADSM1
35	PB0/MTIOC0D/MOSI-B	PB0/A0/A4*1/BC0#/MTIOC0D/MTIOC0D#/TMO0/TXD6/SMOSI6/SSDA6/CTS11#/RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
36	PA5/MTIOC1A/MISO-B/ADTRG1#-A	PA5/A3*1/MTIOC1A/MTIOC1A#/TMCI3/RXD6/SMISO6/SSCL6/RXD8/SMISO8/SSCL8/MISOA/IRQ1/ADTRG1#
37	PA4/MTIOC1B/RSPCK-B/ADTRG0#-A	PA4/A2*1/MTIOC1B/MTIOC1B#/TMCI7/SCK6/TXD8/SMOSI8/SSDA8/RSPCKA/ADTRG0#
38	PA3/MTIOC2A/SSL0-B	PA3/A1*1/MTIOC2A/MTIOC2A#/GTADSM0/TMRI7/TXD9/SMOSI9/SSDA9/SCK8/SSLA0
39	PA2/MTIOC2B/SSL1-B	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/GTADSM1/TMO7/CTS6#/RTS6#/SS6#/RXD9/SMISO9/SSCL9/SCK11*1/SSLA1

100-Pin	RX62T	RX66T (Without PGA Pseudo-Differential Input and USB Pins)
40	PA1/MTIOC6A/SSL2-B	PA1/MTIOC6A/MTIOC6A#/TMO4/TXD9/SMOSI9/SSDA9/RXD11/SMISO11/SSCL11/SSLA2/CRX0/IRQ14_DS/ADTRG0#
41	PA0/MTIOC6C/SSL3-B	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK9/TXD11/SMOSI11/SSDA11/SSLA3/CTX0
42	VCC	VCC
43	P96/POE4#/IRQ4	P96/CS0#/WAIT#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE4#/CTS8#/RTS8#/SS8#/IRQ4_DS
44	VSS	VSS
45	P95/MTIOC6B	P95/MTIOC6B/MTIOC6B#/GTIOC4A/GTIOC7A/GTIOC4A#/GTIOC7A#
46	P94/MTIOC7A	P94/MTIOC7A/MTIOC7A#/GTIOC5A/GTIOC8A/GTIOC5A#/GTIOC8A#
47	P93/MTIOC7B	P93/MTIOC7B/MTIOC7B#/GTIOC6A/GTIOC9A/GTIOC6A#/GTIOC9A#
48	P92/MTIOC6D	P92/MTIOC6D/MTIOC6D#/GTIOC4B/GTIOC7B/GTIOC4B#/GTIOC7B#
49	P91/MTIOC7C	P91/MTIOC7C/MTIOC7C#/GTIOC5B/GTIOC8B/GTIOC5B#/GTIOC8B#
50	P90/MTIOC7D	P90/MTIOC7D/MTIOC7D#/GTIOC6B/GTIOC9B/GTIOC6B#/GTIOC9B#
51	P76/MTIOC4D/GTIOC2B-A	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#
52	P75/MTIOC4C/GTIOC1B-A	P75/D1[A1/D1]/MTIOC4C/MTIOC4C#/GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#
53	P74/MTIOC3D/GTIOC0B-A	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#
54	P73/MTIOC4B/GTIOC2A-A	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#
55	P72/MTIOC4A/GTIOC1A-A	P72/D4[A4/D4]/MTIOC4A/MTIOC4A#/GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#
56	P71/MTIOC3B/GTIOC0A-A	P71/D5[A5/D5]/MTIOC3B/MTIOC3B#/GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#
57	P70/POE0#/IRQ5	P70/D6[A6/D6]/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE0#/CTS9#/RTS9#/SS9#/IRQ5_DS
58	P33/MTIOC3A/MTCLKA-A/SSL3-A	P33/D7[A7/D7]/MTIOC3A/MTCLKA/MTIOC3A#/MTCLKA#/GTIOC3B/GTIOC3B#/TMO0/SSLA3/IRQ13_DS
59	P32/MTIOC3C/MTCLKB-A/SSL2-A	P32/D8[A8/D8]/MTIOC3C/MTCLKB/MTIOC3C#/MTCLKB#/GTIOC3A/GTIOC3A#/TMO6/SSLA2/IRQ12_DS
60	VCC	VCC
61	P31/MTIOC0A-B/MTCLKC-A/SSL1-A	P31/D9[A9/D9]/MTIOC0A/MTCLKC/MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6
62	VSS	VSS
63	P30/MTIOC0B-B/MTCLKD-A/SSL0-A	P30/D10[A10/D10]/MTIOC0B/MTCLKD/MTIOC0B#/MTCLKD#/TMCI6/SCK8/CTS8#/RTS8#/SS8#/SSLA0/IRQ7/COMP3

100-Pin	RX62T	RX66T (Without PGA Pseudo-Differential Input and USB Pins)
64	P24/RSPCK-A	P24/D11[A11/D11]/MTIC5U/MTIC5U#/TMCI2/TMO6/CTS8#/RTS8#/SS8#/SCK8/RSPCKA/IRQ4/COMP0
65	P23/LTX/MOSI-A/CTX-B	P23/D12[A12/D12]/MTIC5V/MTIC5V#/TMO2/CACREF/TXD8/SMOSI8/SSDA8/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/MOSIA/CTX0/IRQ11/COMP1
66	P22/LRX/MISO-A/CRX-B/ADTRG#	P22/D13[A13/D13]/MTIC5W/MTCLKD/MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/TMO4/RXD8/SMISO8/SSCL8/RXD12/SMISO12/SSCL12/RXDX12/MISOA/CRX0/IRQ10/ADTRG2#/COMP2
67	P21/MTCLKA-B/IRQ6/ADTRG1#-B	P21/D14[A14/D14]/MTIOC9A/MTCLKA/MTIOC9A#/MTCLKA#/TMCI4/TXD8/SMOSI8/SSDA8/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/MOSIA/IRQ6_DS/AN217/ADTRG1#/COMP5
68	P20/MTCLKB-B/IRQ7/ADTRG0#-B	P20/D15[A15/D15]/MTIOC9C/MTCLKB/MTIOC9C#/MTCLKB#/TMRI4/CTS8#/RTS8#/SS8#/SCK8/RSPCKA/IRQ7_DS/AN216/ADTRG0#/COMP4
69	P65/AN5	P65/A12/IRQ9/AN211/CMPC53/DA1
70	P64/AN4	P64/A13/IRQ8/AN210/CMPC33/DA0
71	AVCC	AVCC2
72	VREF	AVCC2
73	AVSS	AVSS2
74	P63/AN3	P63/A12*1/A14/IRQ7/AN209/CMPC23
75	P62/AN2	P62/A13*1/A15/IRQ6/AN208/CMPC43
76	P61/AN1	P61/A14*1/A16/IRQ5/AN207/CMPC13
77	P60/AN0	P60/A15*1/A17/IRQ4/AN206/CMPC03
78	P55/AN11	P55/A16*1/A18/IRQ3/AN203/CMPC32
79	P54/AN10	P54/A17*1/A19/IRQ2/AN202/CMPC22
80	P53/AN9	P53/A18*1/A20/IRQ1/AN201/CMPC12
81	P52/AN8	P52/IRQ0/AN200/CMPC02
82	P51/AN7	P51/AN205/CMPC52
83	P50/AN6	P50/AN204/CMPC42
84	P47/AN103/CVREFH	P47/AN103
85	P46/AN102	P46/AN102/CMPC50/CMPC51
86	P45/AN101	P45/AN101/CMPC40/CMPC41
87	P44/AN100	P44/AN100/CMPC30/CMPC31
88	P43/AN003/CVREFL	P43/AN003
89	P42/AN002	P42/AN002/CMPC20/CMPC21
90	P41/AN001	P41/AN001/CMPC10/CMPC11
91	P40/AN000	P40/AN000/CMPC00/CMPC01
92	AVCC0	AVCC1
93	VREFH0	AVCC0
94	VREFL0	AVSS0
95	AVSS0	AVSS1
96	P82/MTIC5U/SCK2-B	P82/ALE/WAIT#/MTIC5U/MTIC5U#/TMO4/SCK6/SCK12/IRQ3/COMP5

100-Pin	RX62T	RX66T (Without PGA Pseudo-Differential Input and USB Pins)
97	P81/MTIC5V/TXD2-B	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/TXD6/SMOSI6/SSDA6/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/COMP4
98	P80/MTIC5W/RXD2-B	P80/CS1#/MTIC5W/MTIC5W#/TMRI4/RXD6/SMISO6/SSCL6/RXD12/SMISO12/SSCL12/RXDX12/IRQ5/COMP3
99	P11/MTCLKC-B/IRQ1-A	P11/RD#/MTIOC3A/MTCLKC/MTIOC3A#/MTCLKC#/MTIOC9D/GTIOC3B/GTETRGA/GTIOC3B#/GTETRGC/TMO3/POE9#/IRQ1_DS
100	P10/MTCLKD-B/IRQ0-A	P10/MTIOC9B/MTCLKD/MTIOC9B#/MTCLKD#/GTETRGB/GTETRGD/TMRI3/POE12#/CTS6#/RTS6#/SS6#/IRQ0_DS

Note: 1. These pins are only enabled for products with 128 KB of RAM.

3.5 80-Pin Package (RX62T: LQFP (Other Than R5F562TxGDFF))

Table 3.5 is a comparative listing of the pin functions of 80-pin package products (RX62T: LQFP (other than R5F562TxGDFF)).

Table 3.5 Comparative Listing of 80-Pin Package Pin Functions (RX62T: LQFP (Other Than R5F562TxGDFF))

80-Pin	RX62T (Other Than R5F562TxGDFF)	RX66T (With PGA Pseudo-Differential Input and Without USB Pins)
1	EMLE	EMLE
2	VSS	VSS
3	MDE	UB/P00/MTIOC9A/MTIOC9A#/CACREF/ RXD9/SMISO9/SSCL9/RXD12/SMISO12/ SSCL12/RXDX12/IRQ2/ADST1/COMP0
4	VCL	VCL
5	MD1	MD/FINED
6	MD0	P01/MTIOC9C/MTIOC9C#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE12#/ TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/IRQ4/ADST2/ COMP1
7	PE4/MTCLKC-C/POE10#-B/IRQ1-B	PE4/MTCLKC/MTCLKC#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE10#/ SCK9/IRQ1
8	PE3/MTCLKD-C/POE11#/IRQ2-A	PE3/MTCLKD/MTCLKD#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE11#/ CTS9#/RTS9#/SS9#/IRQ2_DS
9	RES#	RES#
10	XTAL	XTAL/P37
11	VSS	VSS
12	EXTAL	EXTAL/P36
13	VCC	VCC
14	PE2/POE10#-A/NMI	PE2/POE10#/NMI
15	PE0/CRX-C	TRST#/PD7/MTIOC9A/MTIOC9A#/GTIOC0A/ GTIOC3A/GTIOC0A#/GTIOC3A#/TMRI1/ TMRI5/TXD5/SMOSI5/SSDA5/SSLA1/CTX0/ IRQ8
16	PD7/GTIOC0A-B/CTX-C/TRST#	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/ GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/ CTS1#/RTS1#/SS1#/CTS11#/RTS11#/ SS11#/SSLA0/IRQ5/ADST0
17	PD6/GTIOC0B-B/TMS	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6
18	PD5/GTIOC1A-B/RXD1/TDI	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/ TMCI0/TMCI6/SCK1/SCK11/IRQ2
19	PD4/GTIOC1B-B/SCK1/TCK	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11
20	PD3/GTIOC2A-B/TXD1/TDO	PD2/GTIOC2B/GTIOC0A/GTIOC2B#/ GTIOC0A#/TMCI1/TMO4/SCK5/SCK8/ MOSIA

80-Pin	RX62T (Other Than R5F562TxGDFF)	RX66T (With PGA Pseudo-Differential Input and Without USB Pins)
21	PB7/SCK2-A	PB6/GTIOC2A/GTIOC2A#/RXD5/SMISO5/SSCL5/RXD11/SMISO11/SSCL11/RXD12/SMISO12/SSCL12/RXDX12/CRX0/IRQ2
22	PB6/CRX-A/RXD2-A	PB5/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/SSDA11/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/CTX0
23	PB5/CTX-A/TXD2-A	VCC
24	PLLVCC	PB4/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE8#/CTS5#/RTS5#/SS5#/SCK11/CTS11#/RTS11#/SS11#/IRQ3_DS
25	PB4/GTETRG/IRQ3/POE8#	VSS
26	PLLVSS	PB3/MTIOC0A/MTIOC0A#/CACREF/SCK6/RSPCKA/IRQ9
27	PB3/MTIOC0A-A/SCK0	PB2/MTIOC0B/MTIOC0B#/GTADSM0/TMRI0/TXD6/SMOSI6/SSDA6/SDA/ADSM0
28	PB2/MTIOC0B-A/TXD0/SDA	PB1/MTIOC0C/MTIOC0C#/GTADSM1/TMCI0/RXD6/SMISO6/SSCL6/SCL/IRQ4/ADSM1
29	PB1/MTIOC0C/RXD0/SCL	PB0/MTIOC0D/MTIOC0D#/TMO0/TXD6/SMOSI6/SSDA6/CTS11#/RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
30	PB0/MTIOC0D/MOSI-B	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/SMISO6/SSCL6/RXD8/SMISO8/SSCL8/MISOA/IRQ1/ADTRG1#
31	PA3/MTIOC2A/SSL0-B	PA3/MTIOC2A/MTIOC2A#/GTADSM0/TMRI7/TXD9/SMOSI9/SSDA9/SCK8/SSLA0
32	PA2/MTIOC2B/SSL1-B	VCC
33	VCC	P96/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE4#/CTS8#/RTS8#/SS8#/IRQ4_DS
34	P96/IRQ4/POE4#	VSS
35	VSS	P95/MTIOC6B/MTIOC6B#/GTIOC4A/GTIOC7A/GTIOC4A#/GTIOC7A#
36	P95/MTIOC6B	P94/MTIOC7A/MTIOC7A#/GTIOC5A/GTIOC8A/GTIOC5A#/GTIOC8A#
37	P94/MTIOC7A	P93/MTIOC7B/MTIOC7B#/GTIOC6A/GTIOC9A/GTIOC6A#/GTIOC9A#
38	P93/MTIOC7B	P92/MTIOC6D/MTIOC6D#/GTIOC4B/GTIOC7B/GTIOC4B#/GTIOC7B#
39	P92/MTIOC6D	P91/MTIOC7C/MTIOC7C#/GTIOC5B/GTIOC8B/GTIOC5B#/GTIOC8B#
40	P91/MTIOC7C	P90/MTIOC7D/MTIOC7D#/GTIOC6B/GTIOC9B/GTIOC6B#/GTIOC9B#
41	P76/MTIOC4D/GTIOC2B-A	P76/MTIOC4D/MTIOC4D#/GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#
42	P75/MTIOC4C/GTIOC1B-A	P75/MTIOC4C/MTIOC4C#/GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#
43	P74/MTIOC3D/GTIOC0B-A	P74/MTIOC3D/MTIOC3D#/GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#
44	P73/MTIOC4B/GTIOC2A-A	P73/MTIOC4B/MTIOC4B#/GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#

80-Pin	RX62T (Other Than R5F562TxGDFF)	RX66T (With PGA Pseudo-Differential Input and Without USB Pins)
45	P72/MTIOC4A/GTIOC1A-A	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC5A/GTIOC1A#/GTIOC5A#
46	P71/MTIOC3B/GTIOC0A-A	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC4A/GTIOC0A#/GTIOC4A#
47	P70/POE0#/IRQ5	P70/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE0#/CTS9#/RTS9#/SS9#/ IRQ5_DS
48	P33/MTIOC3A/MTCLKA-A/SSL3-A	VCC
49	P32/MTIOC3C/MTCLKB-A/SSL2-A	P31/MTIOC0A/MTCLKC/MTIOC0A#/ MTCLKC#/TMRI6/SSLA1/IRQ6
50	VCC	VSS
51	P31/MTIOC0A-B/MTCLKC-A/SSL1-A	P30/MTIOC0B/MTCLKD/MTIOC0B#/ MTCLKD#/TMCI6/SCK8/CTS8#/RTS8#/ SS8#/SSLA0/IRQ7/COMP3
52	VSS	P27/MTIOC1A/MTIOC0C/MTIOC1A#/ MTIOC0C#/POE9#/IRQ15
53	P30/MTIOC0B-B/MTCLKD-A/SSL0-A	P22/MTIC5W/MTCLKD/MTIC5W#/ MTCLKD#/MTIOC9B/TMRI2/TMO4/RXD8/ SMISO8/SSCL8/RXD12/SMISO12/SSCL12/ RXDX12/MISOA/CRX0/IRQ10/ADTRG2#/ COMP2
54	P24/RSPCK-A	P21/MTIOC9A/MTCLKA/MTIOC9A#/ MTCLKA#/TMCI4/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ MOSIA/IRQ6_DS/AN217/ADTRG1#/COMP5
55	P23/CTX-B/LTX/MOSI-A	P20/MTIOC9C/MTCLKB/MTIOC9C#/ MTCLKB#/TMRI4/CTS8#/RTS8#/SS8#/ SCK8/RSPCKA/IRQ7_DS/AN216/ADTRG0#/ COMP4
56	P22/ADTRG#/CRX-B/LRX/MISO-A	P65/IRQ9/AN211/CMPC53/DA1
57	P21/ADTRG1#-B/MTCLKA-B/IRQ6	P64/IRQ8/AN210/CMPC33/DA0
58	P20/ADTRG0#-B/MTCLKB-B/IRQ7	AVCC2
59	AVCC	AVSS2
60	AVSS	P62/IRQ6/AN208/CMPC43
61	P63/AN3	P55/IRQ3/AN203/CMPC32
62	P62/AN2	P54/IRQ2/AN202/CMPC22
63	P61/AN1	P53/IRQ1/AN201/CMPC12
64	P60/AN0	P52/IRQ0/AN200/CMPC02
65	P47/AN103/CVREFH	P47/AN103
66	P46/AN102	P46/AN102/CMPC50/CMPC51
67	P45/AN101	P45/AN101/CMPC40/CMPC41
68	P44/AN100	P44/AN100/CMPC30/CMPC31
69	P43/AN003/CVREFL	PH4/AN107/PGAVSS1
70	P42/AN002	P43/AN003
71	P41/AN001	P42/AN002/CMPC20/CMPC21
72	P40/AN000	P41/AN001/CMPC10/CMPC11
73	AVCC0	P40/AN000/CMPC00/CMPC01
74	VREFH0	PH0/AN007/PGAVSS0
75	VREFL0	AVCC1
76	AVSS0	AVCC0

80-Pin	RX62T (Other Than R5F562TxGDFF)	RX66T (With PGA Pseudo-Differential Input and Without USB Pins)
77	P11/MTCLKC-B/IRQ1-A	AVSS0
78	P10/MTCLKD-B/IRQ0-A	AVSS1
79	PA5/ADTRG1#-A/MTIOC1A/MISO-B	P11/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/MTIOC9D/GTIOC3B/GTETRGA/ GTIOC3B#/GTETRGC/TMO3/POE9#/ IRQ1_DS
80	PA4/ADTRG0#-A/MTIOC1B/RSPCK-B	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0_DS

3.6 80-Pin Package (RX62T: LQFP (R5F562TxGDFF))

Table 3.6 is a comparative listing of the pin functions of 80-pin package products (RX62T: LQFP (R5F562TxGDFF)).

Table 3.6 Comparative Listing of 80-Pin Package Pin Functions (RX62T: LQFP (R5F562TxGDFF))

80-Pin	RX62T (R5F562TxGDFF)	RX66T (With PGA Pseudo-Differential Input and Without USB Pins)
1	EMLE	EMLE
2	VSS	VSS
3	MDE	UB/P00/MTIOC9A/MTIOC9A#/CACREF/ RXD9/SMISO9/SSCL9/RXD12/SMISO12/ SSCL12/RXDX12/IRQ2/ADST1/COMP0
4	VCL	VCL
5	MD1	MD/FINED
6	MD0	P01/MTIOC9C/MTIOC9C#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE12#/ TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/IRQ4/ADST2/ COMP1
7	PE4/MTCLKC-C/POE10#-B/IRQ1-B	PE4/MTCLKC/MTCLKC#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE10#/ SCK9/IRQ1
8	PE3/MTCLKD-C/POE11#/IRQ2-A	PE3/MTCLKD/MTCLKD#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE11#/ CTS9#/RTS9#/SS9#/IRQ2_DS
9	RES#	RES#
10	XTAL	XTAL/P37
11	VSS	VSS
12	EXTAL	EXTAL/P36
13	VCC	VCC
14	PE2/POE10#-A/NMI	PE2/POE10#/NMI
15	TRST#/PD7/GTIOC0A-B	TRST#/PD7/MTIOC9A/MTIOC9A#/GTIOC0A/ GTIOC3A/GTIOC0A#/GTIOC3A#/TMRI1/ TMRI5/TXD5/SMOSI5/SSDA5/SSLA1/CTX0/ IRQ8
16	TMS/PD6/GTIOC0B-B	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/ GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/ CTS1#/RTS1#/SS1#/CTS11#/RTS11#/ SS11#/SSLA0/IRQ5/ADST0
17	TDI/PD5/GTIOC1A-B/RXD1	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6
18	TCK/PD4/GTIOC1B-B/SCK1	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/ TMCI0/TMCI6/SCK1/SCK11/IRQ2
19	TDO/PD3/GTIOC2A-B/TXD1	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11
20	PD2/GTIOC2B-B	PD2/GTIOC2B/GTIOC0A/GTIOC2B#/ GTIOC0A#/TMCI1/TMO4/SCK5/SCK8/ MOSIA

80-Pin	RX62T (R5F562TxGDFF)	RX66T (With PGA Pseudo-Differential Input and Without USB Pins)
21	PB7/SCK2-A	PB6/GTIOC2A/GTIOC2A#/RXD5/SMISO5/SSCL5/RXD11/SMISO11/SSCL11/RXD12/SMISO12/SSCL12/RXDX12/CRX0/IRQ2
22	PB6/CRX-A/RXD2-A	PB5/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/SSDA11/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/CTX0
23	PB5/CTX-A/TXD2-A	VCC
24	PLLVCC	PB4/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE8#/CTS5#/RTS5#/SS5#/SCK11/CTS11#/RTS11#/SS11#/IRQ3_DS
25	PB4/GTETRG/IRQ3/POE8#	VSS
26	PLLVSS	PB3/MTIOC0A/MTIOC0A#/CACREF/SCK6/RSPCKA/IRQ9
27	PB3/MTIOC0A-A/SCK0	PB2/MTIOC0B/MTIOC0B#/GTADSM0/TMRI0/TXD6/SMOSI6/SSDA6/SDA/ADSM0
28	PB2/MTIOC0B-A/TXD0/SDA	PB1/MTIOC0C/MTIOC0C#/GTADSM1/TMCI0/RXD6/SMISO6/SSCL6/SCL/IRQ4/ADSM1
29	PB1/MTIOC0C/RXD0/SCL	PB0/MTIOC0D/MTIOC0D#/TMO0/TXD6/SMOSI6/SSDA6/CTS11#/RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
30	PB0/MTIOC0D	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/SMISO6/SSCL6/RXD8/SMISO8/SSCL8/MISOA/IRQ1/ADTRG1#
31	PA5/ADTRG1#-A/MTIOC1A	PA3/MTIOC2A/MTIOC2A#/GTADSM0/TMRI7/TXD9/SMOSI9/SSDA9/SCK8/SSLA0
32	PA3/MTIOC2A	VCC
33	VCC	P96/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE4#/CTS8#/RTS8#/SS8#/IRQ4_DS
34	P96/IRQ4/POE4#	VSS
35	VSS	P95/MTIOC6B/MTIOC6B#/GTIOC4A/GTIOC7A/GTIOC4A#/GTIOC7A#
36	P95/MTIOC6B	P94/MTIOC7A/MTIOC7A#/GTIOC5A/GTIOC8A/GTIOC5A#/GTIOC8A#
37	P94/MTIOC7A	P93/MTIOC7B/MTIOC7B#/GTIOC6A/GTIOC9A/GTIOC6A#/GTIOC9A#
38	P93/MTIOC7B	P92/MTIOC6D/MTIOC6D#/GTIOC4B/GTIOC7B/GTIOC4B#/GTIOC7B#
39	P92/MTIOC6D	P91/MTIOC7C/MTIOC7C#/GTIOC5B/GTIOC8B/GTIOC5B#/GTIOC8B#
40	P91/MTIOC7C	P90/MTIOC7D/MTIOC7D#/GTIOC6B/GTIOC9B/GTIOC6B#/GTIOC9B#
41	P90/MTIOC7D	P76/MTIOC4D/MTIOC4D#/GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#
42	P76/MTIOC4D/GTIOC2B-A	P75/MTIOC4C/MTIOC4C#/GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#
43	P75/MTIOC4C/GTIOC1B-A	P74/MTIOC3D/MTIOC3D#/GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#
44	P74/MTIOC3D/GTIOC0B-A	P73/MTIOC4B/MTIOC4B#/GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#

80-Pin	RX62T (R5F562TxGDFF)	RX66T (With PGA Pseudo-Differential Input and Without USB Pins)
45	P73/MTIOC4B/GTIOC2A-A	P72/MTIOC4A/MTIOC4A#/GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#
46	P72/MTIOC4A/GTIOC1A-A	P71/MTIOC3B/MTIOC3B#/GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#
47	P71/MTIOC3B/GTIOC0A-A	P70/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE0#/CTS9#/RTS9#/SS9#/IRQ5_DS
48	P70/IRQ5/POE0#	VCC
49	P33/MTIOC3A/MTCLKA-A/SSL3-A	P31/MTIOC0A/MTCLKC/MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6
50	P32/MTIOC3C/MTCLKB-A/SSL2-A	VSS
51	VCC	P30/MTIOC0B/MTCLKD/MTIOC0B#/MTCLKD#/TMCI6/SCK8/CTS8#/RTS8#/SS8#/SSLA0/IRQ7/COMP3
52	P31/MTIOC0A-B/MTCLKC-A/SSL1-A	P27/MTIOC1A/MTIOC0C/MTIOC1A#/MTIOC0C#/POE9#/IRQ15
53	VSS	P22/MTIC5W/MTCLKD/MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/TMO4/RXD8/SMISO8/SSCL8/RXD12/SMISO12/SSCL12/RXDX12/MISOA/CRX0/IRQ10/ADTRG2#/COMP2
54	P30/MTIOC0B-B/MTCLKD-A/SSL0-A	P21/MTIOC9A/MTCLKA/MTIOC9A#/MTCLKA#/TMCI4/TXD8/SMOSI8/SSDA8/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/MOSIA/IRQ6_DS/AN217/ADTRG1#/COMP5
55	P24/RSPCK-A	P20/MTIOC9C/MTCLKB/MTIOC9C#/MTCLKB#/TMRI4/CTS8#/RTS8#/SS8#/SCK8/RSPCKA/IRQ7_DS/AN216/ADTRG0#/COMP4
56	P23/CTX-B/LTX/MOSI-A	P65/IRQ9/AN211/CMPC53/DA1
57	P22/ADTRG#/CRX-B/LRX/MISO-A	P64/IRQ8/AN210/CMPC33/DA0
58	P20/ADTRG0#-B/MTCLKB-B/IRQ7	AVCC2
59	AVCC	AVSS2
60	AVSS	P62/IRQ6/AN208/CMPC43
61	P63/AN3	P55/IRQ3/AN203/CMPC32
62	P62/AN2	P54/IRQ2/AN202/CMPC22
63	P61/AN1	P53/IRQ1/AN201/CMPC12
64	P60/AN0	P52/IRQ0/AN200/CMPC02
65	P47/AN103/CVREFH	P47/AN103
66	P46/AN102	P46/AN102/CMPC50/CMPC51
67	P45/AN101	P45/AN101/CMPC40/CMPC41
68	P44/AN100	P44/AN100/CMPC30/CMPC31
69	P43/AN003/CVREFL	PH4/AN107/PGAVSS1
70	P42/AN002	P43/AN003
71	P41/AN001	P42/AN002/CMPC20/CMPC21
72	P40/AN000	P41/AN001/CMPC10/CMPC11
73	AVCC0	P40/AN000/CMPC00/CMPC01
74	VREFH0	PH0/AN007/PGAVSS0
75	VREFL0	AVCC1
76	AVSS0	AVCC0

80-Pin	RX62T (R5F562TxGDFF)	RX66T (With PGA Pseudo-Differential Input and Without USB Pins)
77	P82/MTIC5U/SCK2-B	AVSS0
78	P81/MTIC5V/TXD2-B	AVSS1
79	P80/MTIC5W/RXD2-B	P11/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/MTIOC9D/GTIOC3B/GTETRGA/ GTIOC3B#/GTETRGC/TMO3/POE9#/ IRQ1_DS
80	P10/MTCLKD-B/IRQ0-A	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0_DS

3.7 64-Pin Package

Table 3.7 is a comparative listing of the pin functions of 64-pin package products.

Table 3.7 Comparative Listing of 64-Pin Package Pin Functions

64-Pin	RX62T	RX66T (With PGA Pseudo-Differential Input and Without USB Pins)
1	EMLE	EMLE
2	MDE	UB/P00/MTIOC9A/MTIOC9A#/CACREF/RXD9/SMISO9/SSCL9/RXD12/SMISO12/SSCL12/RXDX12/IRQ2/ADST1/COMP0
3	VCL	VCL
4	MD1	MD/FINED
5	MD0	P01/MTIOC9C/MTIOC9C#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE12#/TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/IRQ4/ADST2/COMP1
6	RES#	RES#
7	XTAL	XTAL/P37
8	VSS	VSS
9	EXTAL	EXTAL/P36
10	VCC	VCC
11	PE2/POE10#-A/NMI	PE2/POE10#/NMI
12	TRST#/PD7/GTIOC0A-B	TRST#/PD7/MTIOC9A/MTIOC9A#/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/SSDA5/SSLA1/CTX0/IRQ8
13	TMS/PD6/GTIOC0B-B	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/CTS1#/RTS1#/SS1#/CTS11#/RTS11#/SS11#/SSLA0/IRQ5/ADST0
14	TDI/PD5/GTIOC1A-B/RXD1	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/TMRI0/TMRI6/RXD1/SMISO1/SSCL1/RXD11/SMISO11/SSCL11/IRQ6
15	TCK/PD4/GTIOC1B-B/SCK1	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/TMCI0/TMCI6/SCK1/SCK11/IRQ2
16	TDO/PD3/GTIOC2A-B/TXD1	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/TMO0/TXD1/SMOSI1/SSDA1/TXD11/SMOSI11/SSDA11
17	PB7/SCK2-A	PB6/GTIOC2A/GTIOC2A#/RXD5/SMISO5/SSCL5/RXD11/SMISO11/SSCL11/RXD12/SMISO12/SSCL12/RXDX12/CRX0/IRQ2
18	PB6/CRX-A/RXD2-A	PB5/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/SSDA11/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/CTX0
19	PB5/CTX-A/TXD2-A	PB4/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE8#/CTS5#/RTS5#/SS5#/SCK11/CTS11#/RTS11#/SS11#/IRQ3_DS
20	PLLVCC	PB3/MTIOC0A/MTIOC0A#/CACREF/SCK6/RSPCKA/IRQ9

64-Pin	RX62T	RX66T (With PGA Pseudo-Differential Input and Without USB Pins)
21	PB4/GTETRG/IRQ3/POE8#	PB2/MTIOC0B/MTIOC0B#/GTADSM0/ TMRI0/TXD6/SMOSI6/SSDA6/SDA/ADSM0
22	PLLVSS	PB1/MTIOC0C/MTIOC0C#/GTADSM1/ TMCI0/RXD6/SMISO6/SSCL6/SCL/IRQ4/ ADSM1
23	PB3/MTIOC0A-A/SCK0	PB0/MTIOC0D/MTIOC0D#/TMO0/TXD6/ SMOSI6/SSDA6/CTS11#/RTS11#/SS11#/ MOSIA/IRQ8/ADTRG2#
24	PB2/MTIOC0B-A/TXD0/SDA	VCC
25	PB1/MTIOC0C/RXD0/SCL	P96/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE4#/CTS8#/RTS8#/SS8#/ IRQ4_DS
26	PB0/MTIOC0D/MOSI-B	VSS
27	PA3/MTIOC2A/SSL0-B	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#
28	PA2/MTIOC2B/SSL1-B	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#
29	P94/MTIOC7A	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#
30	P93/MTIOC7B	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#
31	P92/MTIOC6D	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#
32	P91/MTIOC7C	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#
33	P76/MTIOC4D/GTIOC2B-A	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC6B/GTIOC2B#/GTIOC6B#
34	P75/MTIOC4C/GTIOC1B-A	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC5B/GTIOC1B#/GTIOC5B#
35	P74/MTIOC3D/GTIOC0B-A	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC4B/GTIOC0B#/GTIOC4B#
36	P73/MTIOC4B/GTIOC2A-A	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC6A/GTIOC2A#/GTIOC6A#
37	P72/MTIOC4A/GTIOC1A-A	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC5A/GTIOC1A#/GTIOC5A#
38	P71/MTIOC3B/GTIOC0A-A	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC4A/GTIOC0A#/GTIOC4A#
39	P70/POE0#/IRQ5	P70/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE0#/CTS9#/RTS9#/SS9#/ IRQ5_DS
40	P33/MTIOC3A/MTCLKA-A/SSL3-A	VCC
41	P32/MTIOC3C/MTCLKB-A/SSL2-A	VSS
42	VCC	P22/MTIC5W/MTCLKD/MTIC5W#/ MTCLKD#/MTIOC9B/TMRI2/TMO4/RXD8/ SMISO8/SSCL8/RXD12/SMISO12/SSCL12/ RXDX12/MISOA/CRX0/IRQ10/ADTRG2#/ COMP2
43	P31/MTIOC0A-B/MTCLKC-A/SSL1-A	P21/MTIOC9A/MTCLKA/MTIOC9A#/ MTCLKA#/TMCI4/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ MOSIA/IRQ6_DS/AN217/ADTRG1#/COMP5

64-Pin	RX62T	RX66T (With PGA Pseudo-Differential Input and Without USB Pins)
44	VSS	P20/MTIOC9C/MTCLKB/MTIOC9C#/ MTCLKB#/TMRI4/CTS8#/RTS8#/SS8#/ SCK8/RSPCKA/IRQ7_DS/AN216/ADTRG0#/ COMP4
45	P30/MTIOC0B-B/MTCLKD-A/SSL0-A	P65/IRQ9/AN211/CMPC53/DA1
46	P24/RSPCK-A	P64/IRQ8/AN210/CMPC33/DA0
47	P23/CTX-B/LTX/MOSI-A	AVCC2
48	P22/CRX-B/LRX/MISO-A	AVSS2
49	P47/AN103/CVREFH	P54/IRQ2/AN202/CMPC22
50	P46/AN102	P53/IRQ1/AN201/CMPC12
51	P45/AN101	P52/IRQ0/AN200/CMPC02
52	P44/AN100	P46/AN102/CMPC50/CMPC51
53	P43/AN003/CVREFL	P45/AN101/CMPC40/CMPC41
54	P42/AN002	P44/AN100/CMPC30/CMPC31
55	P41/AN001	PH4/AN107/PGAVSS1
56	P40/AN000	P42/AN002/CMPC20/CMPC21
57	AVCC0	P41/AN001/CMPC10/CMPC11
58	VREFH0	P40/AN000/CMPC00/CMPC01
59	VREFL0	PH0/AN007/PGAVSS0
60	AVSS0	AVCC1
61	P11/MTCLKC-B/IRQ1-A	AVCC0
62	P10/MTCLKD-B/IRQ0-A	AVSS0
63	PA5/ADTRG1#-A/MTIOC1A/MISO-B	AVSS1
64	PA4/ADTRG0#-A/MTIOC1B/RSPCK-B	P11/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/MTIOC9D/GTIOC3B/GTETRGA/ GTIOC3B#/GTETRGC/TMO3/POE9#/ IRQ1_DS

4. Important Information when Migrating Between MCUs

This section presents important information on differences between the RX66T Group and the RX62T/RX62G Group. 4.1, Notes on Pin Design, presents information regarding the hardware, and 4.2, Notes on Functional Design, presents information regarding the software.

4.1 Notes on Pin Design

Migration between the RX62T/RX62G Group (100 pins) and the RX66T Group (100 pins: without PGA pseudo-differential input and USB) is simple because are largely pin-to-pin compatible with only a few suggestions. Note that some pins need to be handled differently between the two groups. Refer to Table 3.4, Comparative Listing of 100-Pin Package Pin Functions (RX66T: Without PGA Pseudo-Differential Input and USB Pins), for details.

4.1.1 VCL Pin (External Capacitor)

When using a smoothing capacitor connected to the VCL pin to stabilize the internal power supply, use a 0.1 µF capacitor for the RX62T/RX62G Group and a 0.47 µF capacitor for the RX66T Group.

4.1.2 PLLVCC Pin

The RX66T Group does not have a PLLVCC pin.

4.1.3 Mode Setting Pins

On the RX62T/RX62G Group the pins for setting the mode on release from the reset state are MD0, MD1, and MDE, but on the RX66T Group they are MD and UB (multiplexed with P00).

4.1.4 Inputting an External Clock

When an external clock is input on the EXTAL pin, the counter-phase clock can be input on the XTAL pin on the RX62T/RX62G Group, but the XTAL pin must be left open on the RX66T Group.

4.1.5 PGA Pseudo-Differential Input–Related Pins (P40 to P42, P44 to P46, PH0, and PH4)

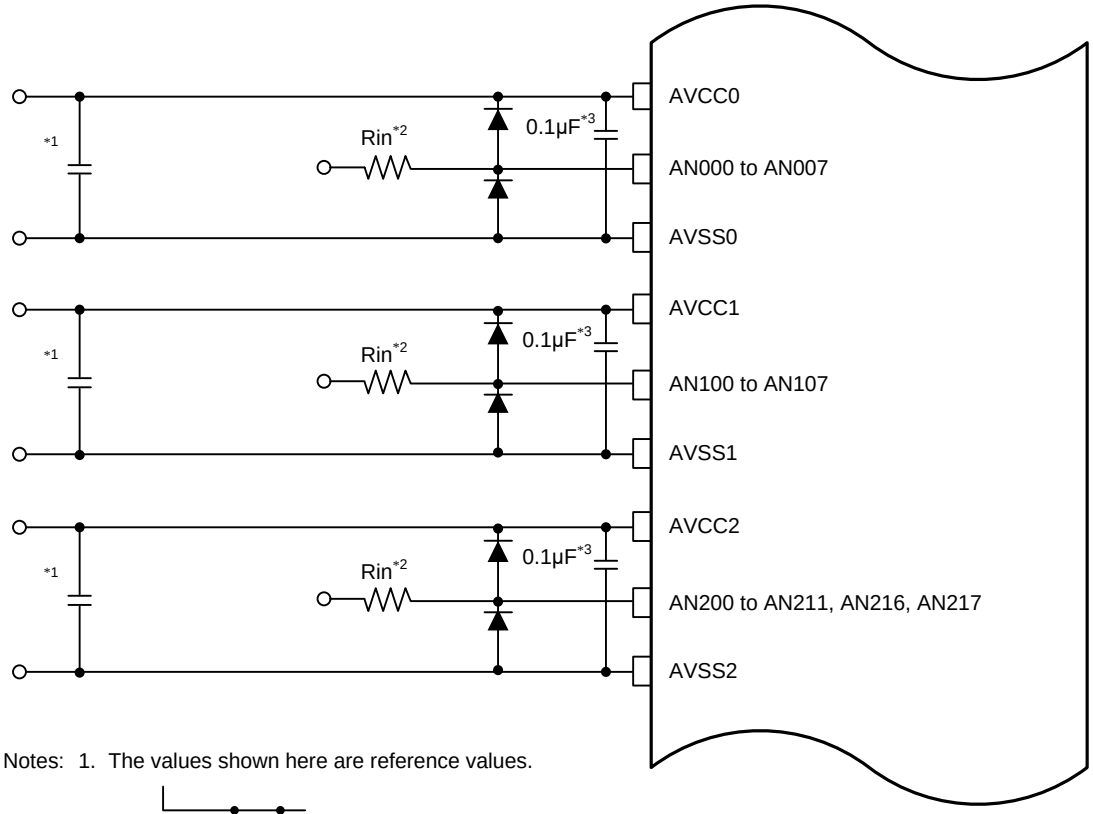
On the RX66T Group a negative voltage may be input on the PGA pseudo-differential input pins from the reset state. Therefore, regardless of whether or not the PGA is used, it is necessary to change the settings of the PGA-related registers in order to use the pin functions of P40 to P42, P44 to P46, PH0, and PH4 after cancellation of a reset.

For details, refer to the descriptions of the VOLSR.PGAVLS bit, the initial setting sequence of the A/D converter, and the PIDR register in RX66T Group User’s Manual: Hardware.

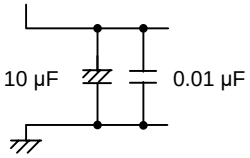
Note that the above-mentioned setting changes are necessary even on products not equipped with PGA pseudo-differential inputs.

4.1.6 Inserting Decoupling Capacitors between AVCC and AVSS Pins

To prevent destruction of the analog input pins (AN000 to AN007, AN100 to AN107, AN200 to AN211, AN216, and AN217) caused by abnormal voltages such as excessively large surges, insert capacitors between the AVCCn and AVSSn pins as shown in the figure below. Also connect suitable protective circuits to the analog input pins (AN000 to AN007, AN100 to AN107, AN200 to AN211, AN216, and AN217).



Notes: 1. The values shown here are reference values.



2. Rin: Signal source impedance
3. Place the capacitors to be inserted between the power supply pins AVCC0 and AVSS0, AVCC1 and AVSS1, and AVCC2 and AVSS2 as close to the pins as possible to improve A/D conversion accuracy. When operating the A/D converter at a frequency higher than 40 MHz, take the following steps to satisfy the required electrical characteristics:
   (1) Add a 1,000 pF capacitor to the 0.1 μF capacitor.
   (2) Place the 1,000 pF capacitor closer to the MCU than the 0.1 μF capacitor.
   (3) Place the capacitor on the AVCC1 side closer to the MCU than that on the AVCC0 side.

4.2 Notes on Functional Design

Some software that runs on the RX62T/RX62G Group is compatible with the RX66T Group. However, careful evaluation is required since specifications such as operating timing and electrical characteristics differ between the groups.

This section presents notes on software regarding the settings of functions that differ between the RX66T Group and the RX62T/RX62G Group.

For differences in modules and functions, refer to 2, Comparative Overview of Specifications. For further information, refer to the User's Manual: Hardware listed in 5, Reference Documents.

4.2.1 RIIC Operating Voltage Setting

When using the RIIC on the RX66T Group, it is necessary to specify the power supply voltage range in order to maintain the proper slope characteristics.

The initial setting is VCC = 4.5 V or greater. If a power supply voltage lower than 4.5 V will be used, change the voltage range setting before starting RIIC operation.

For details, refer to the description of the VOLSR.RICVLS bit in RX66T Group User's Manual: Hardware.

4.2.2 USB Operating Voltage Setting

When using the USB module on the RX66T Group, it is necessary to set the UBS power supply control bit to 1 before starting USB operation.

For details, refer to the description of the VOLSR.USBVON bit in RX66T Group User's Manual: Hardware.

4.2.3 Exception Vector Table

Addresses allocated in the vector table are fixed on the RX62T/RX62G Group. On the RX66T Group, the vector table addresses are relocatable using the value set in the exception table register (EXTB) as the start address.

4.2.4 Voltage Level Setting

On the RX66T Group, values for the voltage level setting register (VOLSR) for operating modes, the voltage detection level select register (LVDLVLR) of the voltage detection circuit, and option function select register 1 (OFS1) for the option-setting memory need to be changed to appropriate values depending on the operating voltage. Make sure to set these values using a program.

4.2.5 Endian Setting

On the RX62T/RX62G Group the endian setting is specified by the MDE pin, but on the RX66T Group the endian setting is specified in the MDE register in the option-setting memory.

4.2.6 Option-Setting Memory

ID codes used for ID code protection and ID code protection on connection of the on-chip debugger are located in the ROM (flash memory for code storage) on the RX62T/RX62G Group and in the option-setting memory on the RX66T Group. Note that the setting procedures differ between the two groups.

4.2.7 Clock Frequency Settings

On the RX62T/RX62G Group the clock frequency settings must be such that ICLK ≥ PCLK, but on the RX66T Group the settings must be as indicated below:

Requirements for clock frequency settings: ICLK ≥ BCLK, PCLKC ≥ PCLKA ≥ PCLKB

Requirements for clock frequency ratios: (N: integer)

ICLK:FCLK = N:1 or 1:N,

ICLK:PCLKA = N:1 or 1:N,

ICLK:PCLKB = N:1 or 1:N,

ICLK:PCLKC = N:1 or 1:N,

ICLK:PCLKD = N:1 or 1:N,

PCLKA:PCLKC = 1:1 or 1:2,

PCLKB:PCLKD = 1:1, 2:1, 4:1, or 1:2

Also, on the RX66T Group it is necessary to change the value of the MEMWAIT register when setting the frequency of ICLK to a frequency greater than 120 MHz.

4.2.8 Main Clock Oscillator

On the RX62T/RX62G Group the main clock starts oscillating after a reset is canceled, but on the RX66T Group the LOCO clock is used for operation after a reset is canceled, so it is necessary to use a program to start oscillation of the main clock.

4.2.9 PLL Circuit

On the RX62T/RX62G Group the multiplication factor setting range of the PLL circuit is 8×, but on the RX66T Group it is 10× to 30× (in 0.5× increments). Change the setting to an appropriate value when using the PLL circuit. Also, on the RX66T Group use a program to switch the PLL clock.

4.2.10 Operation of Main Clock Oscillation Stop Detection Function

The oscillation stop detection function detects when the operation of the main clock oscillator stops and supplies a LOCO clock using the output of the low-speed on-chip oscillator as the clock source for the system clock, instead of the main clock or PLL clock.

Note that on the RX66T Group, when the HOCO clock is selected as the PLL clock source and the PLL clock is selected as the system clock source, the system clock does not switch to the LOCO clock even if main clock oscillation stop is detected.

4.2.11 All-Module Clock Stop Mode

On the RX66T Group, 1 must be written to MSTPA24, MSTPA27, MSTPA29, and MSTPD0 to MSTPD7 when a transition is made to all-module clock stop mode.

4.2.12 Input Buffer Control by DIRQnE Bits (n = 0 to 15)

On the RX66T Group, setting the DPSIERy.DIRQnE (y = 0 or 1, n = 0 to 15) bit to 1 enables the input buffer of the corresponding pin among IRQ0-DS to IRQ15-DS. Note that once the input buffer is enabled, inputs on these pins are sent to the corresponding DPSIFRy.DIRQnF (y = 0 or 1, n = 0 to 15) bits, but they are not sent to the interrupt controller, peripheral modules, and I/O ports.

4.2.13 Register Write Protection Function

A register write protection function has been added on the RX66T Group to prevent important registers from being overwritten in case of program runaway. The initial setting is protection enabled, but the value of the protect bit needs to be changed in order to use functions that utilize the protected registers.

4.2.14 Software Configurable Interrupts

On the RX62T/RX62G Group the interrupt sources have fixed vector numbers, but on the RX66T Group the MTU and GPTW interrupt sources are classified as software configurable interrupt A and set in software configurable interrupt A source select register n (SLIARn). This allows interrupt sources to be allocated to 208 to 255 in the interrupt vector table.

4.2.15 Initialization of Port Direction Register (PDR)

The method of initializing the PDR differs between the RX62T Group and RX66T Group, even on products with the same pin count.

4.2.16 Note on Controlling Switching to General I/O Port Pin Operation by POE3

On the RX66T Group, when an output disable request is generated by making a setting in POE3, pins for which the setting is 1 in the corresponding PMMCRn register (n = 0 to 3) of the POE3 are switched to general I/O port pin operation. Therefore, set the bits in the corresponding POECRn register (n = 0 to 3) to 0 beforehand.

4.2.17 Bus Priority

On the RX62T/RX62G Group the bus priority is fixed at internal main bus 2 > internal main bus 1, but on the RX66T Group the bus priority can be set in the bus priority control register (BUSPRI).

4.2.18 Pin Assignments

On the RX62T/RX62G Group the port function registers listed in section 15, I/O Ports, in RX62T Group, RX62G Group User's Manual: Hardware are used to assign pins to module functions, but on the RX66T Group the pin function control registers described in the multi-function pin controller section of the documentation of the RX66T Group can be used to assign functions of multiple modules to the pins corresponding to the registers. Note that the pin function control registers are covered by the register write protection function. It is necessary to disable protection before writing to these registers.

4.2.19 Operating Frequencies of the GPTW and MTU3d

On the RX66T Group, the count clock for the GPTW and MTU3d is PCLKC, and the bus clock is PCLKA. Note that restrictions apply to the combinations of frequencies that may be used.

4.2.20 DMAC Activation by the MTU

On the RX66T Group, if the DMAC is activated by the MTU, the activation source is cleared when the DMAC requests ownership of the internal bus. Accordingly, the state of the internal bus may lead to a wait before the DMA transfer starts, even though the activation source has been cleared.

4.2.21 MTIOC Pin Output Level when Counter Stopped

When operating with the MTIOC pin in the output state, clearing the CSTn bit to 0 causes the counter to stop. When this happens in complementary PWM mode or reset synchronous PWM mode on the RX66T Group, the initial output level set in the TOCR1A or TOCR2A register is output on the MTIOC pin.

When operating in other than complementary PWM mode or reset synchronous PWM mode, the output compare output level of the MTIOC is maintained.

When a write to the TIOR register occurs while the value of the CSTn bit is 0, the output level of the pin is updated to the initial output value setting.

4.2.22 Note on Timer Mode Register Setting for ELC Event Input

When using the MTU for ELC operation on the RX66T Group, set the timer mode register (TMDR) of the relevant channel to its initial value (00h).

4.2.23 Port Output Enable

The port output enable registers on the RX66T Group are quite different from those on the RX62T/RX62G Group. Note that software compatibility is low with regard to this function.

4.2.24 Control in Response to Output Disabling Request on Port Output Enable 3

When a request to disable outputs is generated on the RX66T Group, pins for which the corresponding bits in the POECR1 to POECR3 and POECR7 registers are set to 1 enter the high-impedance state, and pins for which the corresponding bits in the PMMCR0 to PMMCR3 registers are set to 1 are switched to general I/O port pin operation.

When both bits are set to 1 for the same pin, the settings of the POECR1 to POECR3 and POECR7 registers take priority, and the pins enter the high-impedance state.

After a pin is switched to general I/O port pin operation, the settings of the corresponding bits in the PDR and PODR registers determine the state of the pin.

4.2.25 Setting the Active Level with MTU or GPTW Set to Inverted Output

On the RX66T Group the MPC.PmnPFS register can be used to specify normal output or inverted output for the MTU and GPTW.

When inverted output is selected on the MTU, the active level specified by the MTU.TOCR1j and MTU.TOCR2j registers (j = A, B) and the active level of the signals which are output to the pins is inverted. To use detection of simultaneous conduction in this case, specify in the ALR1 and ALR2 registers the active level based on the signals which are output to the pins.

When inverted output is selected on the GPTW, the active level of the signals which are output to the pins is inverted. To use detection of simultaneous conduction in this case, specify in the ALR3 to ALR5 registers the active level based on the signals which are output to the pins.

4.2.26 Reading Pins in High-Impedance State

When pins are put into the high-impedance state by the POE on the RX66T Group, their level cannot be read. The value when read is undefined. To read the level of the pins, release them from the high-impedance state.

This limitation does not apply when port switching control is selected instead of high-impedance control.

4.2.27 Note on Using POE and POEG Together

When using the POE and POEG together on the RX66T Group, do not apply output disable control by both the POE and POEG to the same GPTW output pin.

4.2.28 General PWM Timer

Registers for the general PWM timer on the RX66T Group are quite different from those on the RX62T/RX62G Group. Note that software compatibility is low with regard to this function.

4.2.29 Watchdog Timer and Independent Watchdog Timer

On the RX66T Group it is possible to select either maskable or non-maskable as the type of the WDT underflow and refresh error interrupts and the IWDT underflow and refresh error interrupts.

4.2.30 Eliminating I^2C Bus Interface Noise

The RX62T Group has integrated analog noise filters on the SCL and SDA lines, but the RX66T Group has no integrated analog noise filters.

4.2.31 12-Bit A/D Converter

Registers for the 12-bit A/D converter on the RX66T Group are quite different from those on the RX62T/RX62G Group. Note that software compatibility is low with regard to this function.

4.2.32 A/D Conversion Start Bit

On the RX66T Group, when the single-scan continuous function is used (ADGSPCR.GBRP bit = 1) with group priority control operation mode enabled on the 12-bit A/D converter (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), the value of the ADCSR.ADST bit is maintained as 1.

4.2.33 Restrictions on Comparison Function

On the RX66T Group the comparison function of the 12-bit A/D converter has the following restrictions:

1. Use of self-diagnostics and double trigger mode are prohibited. (ADRD, ADDBLDR, ADDBLDRA, and ADDBLDRB are not covered by the comparison function)
2. To use matching or unmatching output, it is necessary to select single scan mode.
3. When temperature sensor or internal reference voltage is selected for window A, operation of window B is prohibited.
4. When temperature sensor or internal reference voltage is selected for window B, operation of window A is prohibited.
5. The same channel cannot be set for both window A and window B.
6. It is necessary to make settings such that high-side reference value ≥ low-side reference value.

4.2.34 Generation of A/D Scan Conversion End Interrupt

On the RX66T Group, when scanning was started by a software trigger, an A/D scan conversion end interrupt is generated if the ADCSR.ADIE bit is set to 1 when the scan ends, even when double-trigger mode has been selected.

4.2.35 D/A Converter Settings

When making D/A converter settings on the RX66T Group, first set comparator C as the output destination using the D/A destination select register (DADSELR), then wait for the D/A converter output to stabilize before enabling comparator operation.

Similarly, stop the comparator temporarily before making changes to the settings of the D/A converter, then wait for the D/A converter output to stabilize before enabling comparator operation.

4.2.36 Transferring Firmware to FCU RAM

On the RX62T/RX62G Group it is necessary to store FCU firmware in the FCU RAM in order to use FCU commands, but this processing is not needed on the RX66T Group.

4.2.37 ROM Cache

The RX66T Group has an 8 KB ROM cache, and ROM cache operation is disabled after a reset is canceled.

To use the ROM cache, set the ROMCE.ROMCEN bit to 1.

4.2.38 Using Flash Memory Programming Commands

On the RX62T/RX62G Group, programming and erasing the flash memory are performed by issuing commands to the FCU. On the RX66T Group, programming and erasing the flash memory are performed by controlling the FCU with the FACI commands specified in the FACI command issuing area.

Table 4.1 is a comparative listing of FCU and FACI commands.

Table 4.1 Comparison of FCU and FACI Command Specifications

Item	FCU Command (RX62T)	FACI Command (RX66T)
Command issuing area	ROM programming/erasure address (00FC 0000h to 00FF FFFFh)	FACI command issuing area (007E 0000h)
Available command	• P/E normal mode transition • Status read mode transition • Lock bit read mode transition (lock bit read 1) • Peripheral clock notification • Programming • Block erase • P/E suspend • P/E resume • Status register clear • Lock bit read 2/blank check • Lock bit programming	• Programming • Block erase • P/E suspend • P/E resume • Status clear • Forced stop • Lock-bit read • Blank check • Configuration setting • Lock-bit programming

5. Reference Documents

User's Manual: Hardware

RX62T Group, RX62G Group User's Manual: Hardware Rev.2.00 (R01UH0034EJ0200)
(The latest version can be downloaded from the Renesas Electronics website.)

RX66T Group User's Manual: Hardware Rev.1.10 (R01UH0749EJ0110)
(The latest version can be downloaded from the Renesas Electronics website.)

Application Note

Design Guide for Migration between RX Family: Differences in Package External form (R01AN4591EJ)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News
(The latest version can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This application note reflects the content of the following technical updates:

- TN-RX*-A094A/E
- TN-RX*-A095A/E
- TN-RX*-A096A/E
- TN-RX*-A098A/E
- TN-RX*-A099A/E
- TN-RX*-A119A/E
- TN-RX*-A141A/E
- TN-RX*-A152A/E
- TN-RX*-A161A/E
- TN-RX*-A185A/E
- TN-RX*-A190A/E
- TN-RX*-A193A/E
- TN-RX*-A0213A/E
- TN-RX*-A0218A/E
- TN-RX*-A0219A/E
- TN-RX*-A0227A/E
- TN-RX*-A0231A/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Sep. 20, 2018	—	First edition issued
1.10	Oct. 23, 2020	5	1 Table 1.1 Comparison of Built-In Functions of RX66T Group and RX62T Group revised
		7	2.1 Table 2.1 Comparative Overview of CPUs revised
			2.1 Table 2.2 Comparison of CPU Registers revised
		8	2.2 Table 2.3 Comparative Overview of Operating Modes and Table 2.4 Comparison of Operating Mode–Related Registers revised
		9	2.3 Address Space added
		12	2.4 Table 2.5 Comparative Overview of Resets revised
		15	2.6 Table 2.9 Comparative Overview of Clock Generation Circuits revised
		17	2.6 Table 2.10 Comparison of Clock Generation Circuit Registers revised
		23	2.7 Table 2.13 Comparison of Low Power Consumption Registers revised
		25	2.8 Exception Handling added
		26	2.9 Table 2.16 Comparative Overview of Interrupt Controllers revised
		28	2.9 Table 2.17 Comparison of Interrupt Controller Registers revised
		31	2.10 Table 2.19 Comparative Overview of Buses revised
		35	2.13 Table 2.22 Comparative Overview of I/O Ports on 112-Pin Packages and Table 2.23 Comparative Overview of I/O Ports on 100-Pin Packages (RX66T: With PGA Pseudo-Differential Input) revised
		36	2.13 Table 2.24 Comparative Overview of I/O Ports on 100-Pin Packages (RX66T: Without PGA Pseudo-Differential Input) and Table 2.25 Comparative Overview of I/O Ports on 80-Pin Packages (RX62T: Other Than R5F562TxGDFF) revised
		37	2.13 Table 2.26 Comparative Overview of I/O Ports on 80-Pin Packages (RX62T: R5F562TxGDFF) and Table 2.27 Comparative Overview of I/O Ports on 64-Pin Packages revised
		38	2.13 Table 2.28 Comparison of I/O Port Functions added
		40	2.13 Table 2.29 Comparison of I/O Port Registers revised
		43	2.14 Table 2.31 Comparison of Multi-Function Timer Pulse Unit 3 Registers revised
		44	2.14 Table 2.32 Comparison of TPSC Bit Settings (Other Than MTU5) added
		48	2.15 Table 2.34 Comparative Overview of Port Output Enable 3 revised
		51	2.15 Table 2.35 Comparison of Port Output Enable 3 Registers revised
		65	2.16 Table 2.37 Comparison of General PWM Timer Registers revised
		71	2.16 Table 2.38 Comparative Listing of GTIOA and GTIOB Bit Settings added

Rev.	Date	Description	
		Page	Summary
1.10	Oct. 23, 2020	73	2.18 Table 2.40 Comparative Overview of Watchdog Timers revised
		77	2.19 Table 2.43 Comparison of Independent Watchdog Timer Registers revised
		81	2.20 Table 2.45 Comparative Listing of Serial Communications Interface Channels revised
			2.20 Table 2.46 Comparison of Serial Communications Interface Registers revised
		95	2.24 Table 2.54 Comparison of CRC Calculator Registers revised
		96	2.25 Table 2.55 Comparative Overview of 12-Bit A/D Converters revised
		101	2.25 Table 2.56 Comparison of 12-Bit A/D Converter Registers revised
		104	2.25 Table 2.57 Comparative Listing A/D Conversion Start Triggers added
		106	2.26 Table 2.58 Comparative Overview of RAM revised
		108	2.27 Table 2.60 Comparative Overview of Flash Memory revised
		111	2.27 Table 2.61 Comparison of Flash Memory Registers revised
		119	3.2 Table 3.2 Comparative Listing of 100-Pin Package Pin Functions (RX66T: With PGA Pseudo-Differential Input and USB Pins) revised
		124	3.3 Table 3.3 Comparative Listing of 100-Pin Package Pin Functions (RX66T: With PGA Pseudo-Differential Input and Without USB Pins) revised
		129	3.4 Table 3.4 Comparative Listing of 100-Pin Package Pin Functions (RX66T: Without PGA Pseudo-Differential Input and USB Pins) revised
		134	3.5 Table 3.5 Comparative Listing of 80-Pin Package Pin Functions (RX62T: LQFP (Other Than R5F562TxGDFF)) revised
		138	3.6 Table 3.6 Comparative Listing of 80-Pin Package Pin Functions (RX62T: LQFP (R5F562TxGDFF)) revised
		142	3.7 Table 3.7 Comparative Listing of 64-Pin Package Pin Functions revised
		145	4.1.4 General I/O Ports deleted
		147	4.2.3 Exception Vector Table revised
		148	4.2.10 Operation of Main Clock Oscillation Stop Detection Function added
		148, 149	4.2.12, 4.2.15, and 4.2.16 added
		150	4.2.21, 4.2.22, and 4.2.24 to 4.2.26 added
		150, 151	4.2.27, 4.2.29, 4.2.30, and 4.2.32 to 4.2.34 added
		151	4.2.35 D/A Converter Settings added
		152	4.2.38 Table 4.1 Comparison of FCU and FACI Command Specifications revised
		153	5 Reference Documents revised
		154	Related Technical Updates revised

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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