RX66T Group, RX23T Group

Differences Between the RX66T Group and the RX23T Group

Summary

This application note is intended as a reference to points of difference between the peripheral functions, I/O registers, and pin functions of the RX66T Group and RX23T Group, as well as a guide to key points to consider when migrating between the two groups.

Unless specifically otherwise noted, the information in this application note applies to the 144-pin package version (with programmable gain amplifier (PGA), pseudo-differential input, and USB pins) of the RX66T Group and the 64-pin package version of the RX23T Group as the maximum specifications. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the User's Manual: Hardware of the products in question.

Target Devices

RX66T Group and RX23T Group

Contents

1. Comparison of Built-In Functions of RX66T Group and RX23T Group

A comparison of the built-in functions of the RX66T Group and RX23T Group is provided below. For details of the functions, see section 2, Comparative Overview of Specifications and section 5, Reference Documents.

Table 1.1 is a comparison of built-in functions of RX66T Group and RX23T Group.

Table 1.1 Comparison of Built-In Functions of RX66T Group and RX23T Group

<table>
<tr><th>Function</th><th>RX23T</th><th>RX66T</th></tr>
<tr><td>CPU</td><td colspan="2">●</td></tr>
<tr><td>Operating modes</td><td colspan="2">●</td></tr>
<tr><td>Address space</td><td colspan="2">▲</td></tr>
<tr><td>Resets</td><td colspan="2">●</td></tr>
<tr><td>Option-setting memory (OSFM)</td><td colspan="2">●</td></tr>
<tr><td>Voltage detection circuit (LVDAb): RX23T, (LVDA): RX66T</td><td colspan="2">▲</td></tr>
<tr><td>Clock generation circuit</td><td colspan="2">●</td></tr>
<tr><td>Clock frequency accuracy measurement circuit (CAC)</td><td colspan="2">○</td></tr>
<tr><td>Low power consumption</td><td colspan="2">●/■</td></tr>
<tr><td>Register write protection function</td><td colspan="2">●/▲</td></tr>
<tr><td>Exception handling</td><td colspan="2">○</td></tr>
<tr><td>Interrupt controller (ICUb): RX23T, (ICUC): RX66T</td><td colspan="2">●</td></tr>
<tr><td>Buses</td><td colspan="2">●</td></tr>
<tr><td>Memory-protection unit (MPU)</td><td colspan="2">○</td></tr>
<tr><td>DMA controller (DMACAa)</td><td>×</td><td>○</td></tr>
<tr><td>Data transfer controller (DTCa)</td><td colspan="2">●</td></tr>
<tr><td>Event link controller (ELC)</td><td>×</td><td>○</td></tr>
<tr><td>I/O ports</td><td colspan="2">●/■</td></tr>
<tr><td>Multi-function pin controller (MPC)</td><td colspan="2">▲</td></tr>
<tr><td>Multi-function timer pulse unit 3 (MTU3c): RX23T, (MTU3d): RX66T</td><td colspan="2">●</td></tr>
<tr><td>Port output enable 3 (POE3b): RX23T, (POE3B): RX66T</td><td colspan="2">●</td></tr>
<tr><td>General PWM timer (GPTW)</td><td>×</td><td>○</td></tr>
<tr><td>High resolution PWM waveform generation circuit (HRPWM)</td><td>×</td><td>○</td></tr>
<tr><td>GPTW port output enable (POEG)</td><td>×</td><td>○</td></tr>
<tr><td>8-bit timer (TMR)</td><td colspan="2">●</td></tr>
<tr><td>Compare match timer (CMT)</td><td colspan="2">●</td></tr>
<tr><td>Watchdog timer (WDTA)</td><td>×</td><td>○</td></tr>
<tr><td>Independent watchdog timer (IWDTa)</td><td colspan="2">●</td></tr>
<tr><td>USB 2.0 FS Host/Function module (USBb)</td><td>×</td><td>○</td></tr>
<tr><td>Serial communications interface (SCIg): RX23T, (SCIj, SCIi, SCIh): RX66T</td><td colspan="2">●</td></tr>
<tr><td>I²C bus interface (RIICa)</td><td colspan="2">●</td></tr>
<tr><td>CAN module (CAN)</td><td>×</td><td>○</td></tr>
<tr><td>Serial peripheral interface (RSPIa): RX23T, (RSPIc): RX66T</td><td colspan="2">●</td></tr>
<tr><td>CRC calculator (CRC): RX23T, (CRCA): RX66T</td><td colspan="2">●</td></tr>
<tr><td>Trusted Secure IP (TSIP-Lite)</td><td>×</td><td>○</td></tr>
<tr><td>12-bit A/D converter (S12ADE): RX23T, (S12ADH): RX66T</td><td colspan="2">●</td></tr>
<tr><td>D/A converter for generating comparator C reference voltage (DA): RX23T,
12-bit D/A converter (R12DAb): RX66T</td><td colspan="2">●</td></tr>
<tr><td>Temperature sensor (TEMPS)</td><td>×</td><td>○</td></tr>
<tr><td>Comparator C (CMPC)</td><td colspan="2">●/■</td></tr>
<tr><td>Data operation circuit (DOC)</td><td colspan="2">●</td></tr>
<tr><td>RAM</td><td colspan="2">●</td></tr>
</table>

Function	RX23T	RX66T
Flash memory	●	
Packages	●/■	

○: Available, ✕: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Differences in register specifications are not listed.

2.1 CPU

Table 2.1 is a comparative overview of CPU.

Table 2.1 Comparative Overview of CPU

Item	RX23T	RX66T
CPU	• Maximum operating frequency: 40 MHz • 32-bit RX CPU (RXv2) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • Basic instructions: 75, variable-length instruction format • Floating point instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory-protection unit (MPU)	• Maximum operating frequency: 160 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • Basic instructions: 77 instruction format • Single-precision floating point instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory-protection unit (MPU)
FPU	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard

2.2 Operating Modes

Table 2.2 is a comparative overview of operating modes, and Table 2.3 is a comparison of operating mode registers.

Table 2.2 Comparative Overview of Operating Modes

Item	RX23T	RX66T
Operating modes by the mode-setting pins	Single-chip mode	Single-chip mode
	Boot mode (SCI)	Boot mode (SCI interface)
	—	Boot mode (USB interface)
	—	Boot mode (FINE interface)
	—	User boot mode
Operating mode by register setting	—	Single-chip mode
		User boot mode
		On-chip ROM disabled extended mode
		On-chip ROM enabled extended mode
Selection of endian	MDE (Endian select register)	MDE (Endian select register)

Table 2.3 Comparison of Operating Mode Registers

Register	Bit	RX23T	RX66T
MDSR	—	—	Mode status register
SYSCR0	—	—	System control register 0
SYSCR1	—	System control register 1	System control register 1
		Initial value after a reset differs.	
	ECCRAME	—	ECCRAM enable bit
VOLSR	—	—	Voltage level setting register

2.3 Address space

Figure 2.1 is a comparative memory map of single-chip mode.

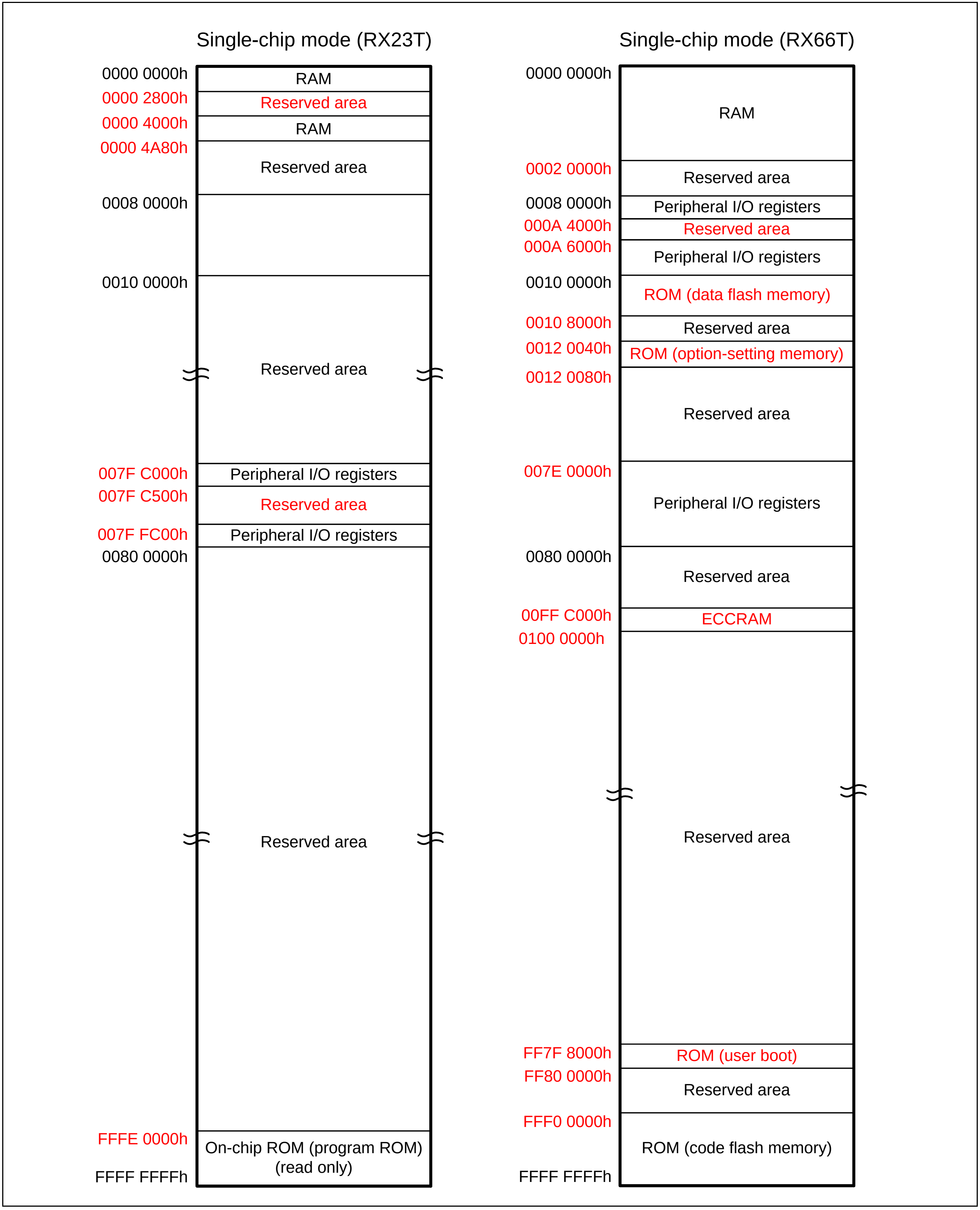

Figure 2.1 Comparative Memory Map of Single-Chip Mode

2.4 Resets

Table 2.4 is a comparative overview of resets, and Table 2.5 is a comparison of reset-related registers.

Table 2.4 Comparative Overview of Resets

Item	RX23T	RX66T
RES# pin reset	Voltage input to the RES# pin is driven low.	Voltage input to the RES# pin is driven low.
Power-on reset	VCC rises (voltage monitored: VPOR)	VCC rises (voltage detection: VPOR)
Voltage-monitoring 0 reset	VCC falls (voltage monitored: Vdet0)	VCC falls (voltage detection: Vdet0)
Voltage-monitoring 1 reset	VCC falls (voltage monitored: Vdet1)	VCC falls (voltage detection: Vdet1)
Voltage-monitoring 2 reset	VCC falls (voltage monitored: Vdet2)	VCC falls (voltage detection: Vdet2)
Deep software standby reset	—	Deep software standby mode is canceled by an interrupt.
Independent watchdog timer reset	Independent watchdog timer underflows, or refresh error occurs.	Independent watchdog timer underflows, or refresh error occurs.
Watchdog timer reset	—	Watchdog timer underflows, or refresh errors.
Software reset	Register setting	Register setting

Table 2.5 Comparison of Reset-Related Registers

Register	Bit	RX23T	RX66T
RSTSR0	DPSRSTF	—	Deep software standby reset flag
RSTSR2	WDTRF	—	Watchdog timer reset detect flag

2.5 Option-Setting Memory

Figure 2.2 is a comparison of option-setting memory areas, and Table 2.6 is a comparison of option-setting memory registers.

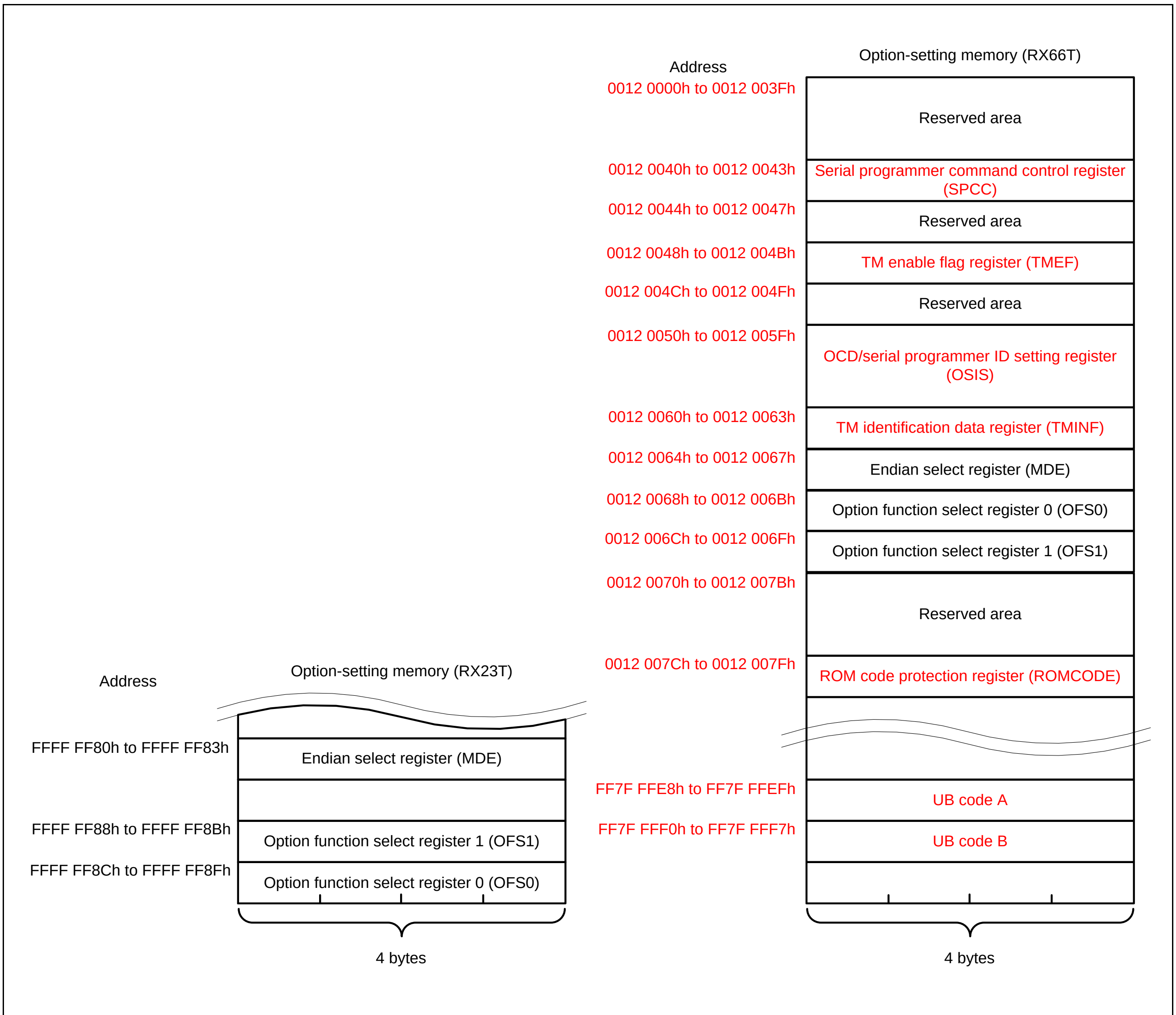

Figure 2.2 Comparison of Option-Setting Memory Areas

Table 2.6 Comparison of Option-Setting Memory Registers

Register	Bit	RX23T	RX66T (OFSM)
SPCC	—	—	Serial programmer command control register
OSIS	—	—	OCD/serial programmer ID setting register
OFS0	IWDTTOPS [1:0]	IWDT timeout period select bits b3 b2 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1,024 cycles (03FFh) 1 1: 2,048 cycles (07FFh)	IWDT timeout period select bits b3 b2 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh)
	IWDTRSTIRQS	IWDT reset interrupt request select bit 0: Non-maskable interrupt request is enabled 1: Reset is enabled	IWDT reset interrupt request select bit 0: Non-maskable interrupt request or interrupt request is enabled 1: Reset is enabled
	IWDTSLCSTP	IWDT sleep mode count stop control bit 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, or deep sleep mode	IWDT sleep mode count stop control bit 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, deep software standby, or all-module clock stop mode
	WDTSTRT	—	WDT start mode select bit
	WDTTOPS [1:0]	—	WDT timeout period select bits
	WDTCKS [3:0]	—	WDT clock frequency division ratio select bits
	WDTRPES [1:0]	—	WDT window end position select bits
	WDTRPSS [1:0]	—	WDT window start position select bits
	WDTRSTIRQS	—	WDT reset interrupt request select bit
OFS1	VDSEL [1:0]	Voltage detection 0 level select bits b1 b0 0 0: 3.84 V is selected 1 0: 2.51 V is selected Settings other than the above are prohibited when the voltage detection 0 circuit is used.	Voltage detection 0 level select bits b1 b0 0 0: Reserved 0 1: Reserved 1 0: Selects 2.83 V 1 1: Selects 4.22 V
TMEF	—	—	TM enable flag register
TMINF	—	—	TM identification data register
ROMCODE	—	—	ROM code protection register

2.6 Voltage Detection Circuit

Table 2.7 is a comparative overview of the voltage detection circuits, and Table 2.8 is a comparison of voltage detection circuit registers.

In addition, Table 2.9 is a comparative listing of the setting procedures for monitoring against Vdet1, Table 2.10 is a comparative listing of the setting procedures for monitoring against Vdet2, and Table 2.11 to Table 2.14 are comparative listings of the setting procedures for bits related to the voltage monitoring 1 and 2 interrupts and the voltage monitoring 1 and 2 resets.

Table 2.7 Comparative Overview of Voltage Detection Circuits

Item		RX23T (LVDAb)			RX66T (LVDA)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	Voltage drops past Vdet0	When voltage rises above or drops below Vdet1	When voltage rises above or drops below Vdet2	Voltage drops past Vdet0	Voltage rises or drops past Vdet1	Voltage rises or drops past Vdet2
	Detection voltage	Voltage selectable from two levels using OFS1.VDSEL[1:0] bits	Voltage selectable from nine levels using the LVDLVLR.LVD1LVL[3:0] bits	Voltage selectable from four levels using the LVDLVLR.LVD2LVL[1:0] bits	Selectable from among two different levels by using OFS1.VDSEL[1:0] bits	Selectable from among five different levels by using LVDLVLR.LVD1LVL[3:0] bits	Selectable from among five different levels by using LVDLVLR.LVD2LVL[3:0] bits
	Monitoring flag	Not available	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2	None	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2
			LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2DET flag: Vdet2 passage detection		LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2DET flag: Vdet2 passage detection
Process upon voltage detection	Reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet0 > VCC: CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet2 or after specified time with Vdet2 > VCC	Reset when Vdet0 > VCC: CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet2 or Vdet2 > VCC

Item		RX23T (LVDAb)			RX66T (LVDA)		
		Voltage Monitoring 0	Voltage Monitoring 1	Voltage Monitoring 2	Voltage Monitoring 0	Voltage Monitoring 1	Voltage Monitoring 2
Process upon voltage detection	Interrupt	Not available	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	No interrupt	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
			Non-maskable or maskable interrupt is selectable	Non-maskable or maskable interrupt is selectable		Non-maskable interrupt or maskable interrupt selectable	Non-maskable interrupt or maskable interrupt selectable
			Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either	Interrupt request issued when Vdet2 > VCC and VCC > Vdet2 or either		Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either	Interrupt request issued when Vdet2 > VCC and VCC > Vdet2 or either
Digital filter	Enable/ disable switching	—	—	—	Digital filter function not available	Available	Available
	Sampling time	—	—	—	—	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)
Event linking function		—	—	—	None	Available Output of event signals on detection of Vdet crossings	Available Output of event signals on detection of Vdet crossings

Table 2.8 Comparison of Voltage Detection Circuit Registers

Register	Bit	RX23T (LVDAb)	RX66T (LVDA)
LVDLVLR	—	Voltage detection level select register	Voltage detection level select register
		Initial value after a reset differs.	
	LVD1LVL[3:0]	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 0 0 0: 4.29 V 0 0 0 1: 4.14 V 0 0 1 0: 4.02 V 0 0 1 1: 3.84 V 0 1 0 0: 3.10 V 0 1 0 1: 3.00 V 0 1 1 0: 2.90 V 0 1 1 1: 2.79 V 1 0 0 0: 2.68 V Settings other than the above are prohibited.	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 1 0 0: 4.57 V (Vdet1_0) 0 1 0 1: 4.47 V (Vdet1_1) 0 1 1 0: 4.32 V (Vdet1_2) 1 0 1 0: 2.93 V (Vdet1_3) 1 0 1 1: 2.88 V (Vdet1_4) Settings other than the above are prohibited.
	LVD2LVL[1:0] (RX23T) LVD2LVL[3:0] (RX66T)	Voltage detection 2 level select bits (Standard voltage during drop in voltage) b5 b4 0 0: 4.29 V 0 1: 4.14 V 1 0: 4.02 V 1 1: 3.84 V	Voltage detection 2 level select bits (Standard voltage during drop in voltage) b7 b4 0 1 0 0: 4.57 V (Vdet2_0) 0 1 0 1: 4.47 V (Vdet2_1) 0 1 1 0: 4.32 V (Vdet2_2) 1 0 1 0: 2.93 V (Vdet2_3) 1 0 1 1: 2.88 V (Vdet2_4) Settings other than the above are prohibited.
LVD1CR0	—	Voltage monitoring 1 circuit control register 0	Voltage monitoring 1 circuit control register 0
		Initial value after a reset differs.	
	LVD1DFDIS	—	Voltage monitoring 1 digital filter disable mode select bit
	LVD1FSAMP [1:0]	—	Sampling clock select bits
LVD2CR0	—	Voltage monitoring 2 circuit control register 0	Voltage monitoring 2 circuit control register 0
		Initial value after a reset differs.	
	LVD2DFDIS	—	Voltage monitoring 2 digital filter disable mode select bit
	LVD2FSAMP [1:0]	—	Sampling clock select bits

Table 2.9 Comparison of Setting Procedures for Monitoring Against Vdet1

Item		RX23T (LVDAb)	RX66T (LVDA)
Setting procedure for monitoring against Vdet1	1	Specify the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits (voltage detection 1 level select).	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.
	2	Set the LVCMPCR.LVD1E bit to 1 (voltage detection 1 circuit enabled).	Set LVCMPCR.LVD1E = 1 (enabling the voltage detection 1 circuit).
	3	Wait for at least td(E-A).	Wait for at least td(E-A): LVD operation stabilization time (after LVD is enabled).
	4	— (No action needed because there is no digital filter.)	• When the digital filter is in use Select the sampling clock for the digital filter by setting the LVD1CR0.LVD1FSAMP[1:0] bits. • When the digital filter is not in use — (No procedure)
	5	— (No action needed because there is no digital filter.)	• When the digital filter is in use Set LVD1CR0.LVD1DFDIS = 0 (enabling the digital filter). • When the digital filter is not in use — (No procedure)
	6	— (No action needed because there is no digital filter.)	• When the digital filter is in use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the digital filter is not in use — (No procedure)
	7	Set the LVD1CR0.LVD1CMPE bit to 1 (voltage monitoring 1 circuit comparison results output enabled).	Set LVD1CR0.LVD1CMPE = 1 (enabling output of the results of comparison by voltage monitoring 1).

Table 2.10 Comparison of Setting Procedures for Monitoring Against Vdet2

Item		RX23T (LVDAb)	RX66T (LVDA)
Setting procedure for monitoring against Vdet2	1	Specify the detection voltage by setting the LVDLVLR.LVD2LVL[1:0] bits (voltage detection 2 level select).	Select the detection voltage by setting the LVDLVLR.LVD2LVL[3:0] bits.
	2	Set the LVCMPCR.LVD2E bit to 1 (voltage detection 2 circuit enabled).	Set LVCMPCR.LVD2E = 1 (enabling the voltage detection 2 circuit).
	3	Wait for at least td(E-A).	Wait for at least td(E-A): LVD operation stabilization time (after LVD is enabled).
	4	— (No action needed because there is no digital filter.)	• When the digital filter is in use Select the sampling clock for the digital filter by setting the LVD2CR0.LVD2FSAMP[1:0] bits. • When the digital filter is not in use — (No procedure)
	5	— (No action needed because there is no digital filter.)	• When the digital filter is in use Set LVD2CR0.LVD2DFDIS = 0 (enabling the digital filter). • When the digital filter is not in use — (No procedure)
	6	— (No action needed because there is no digital filter.)	• When the digital filter is in use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the digital filter is not in use — (No procedure)
	7	Set the LVD2CR0.LVD2CMPE bit to 1 (voltage monitoring 2 circuit comparison results output enabled).	Set LVD2CR0.LVD2CMPE = 1 (enabling output of the results of comparison by voltage monitoring 2).

Table 2.11 Comparison of Operation-Enable Setting Procedures for Bits Related to Voltage Monitoring 1 Interrupt and Voltage Monitoring 1 Reset

Item		RX23T (LVDAb)	RX66T (LVDA)
Operation-enable setting procedure for bits related to voltage monitoring 1 interrupt	1	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.
	2	Set the LVD1CR0.LVD1RI bit to 0 (voltage monitoring 1 interrupt).	Set LVCMPCR.LVD1E = 1 (enabling the voltage detection 1 circuit).
	3	• Select the timing of interrupt requests by setting the LVD1CR1.LVD1IDTSEL[1:0] bits. • Select the type of interrupt by setting the LVD1CR1.LVD1IRQSEL bit.	Wait for at least td(E-A): LVD operation stabilization time (after LVD is enabled).
	4	— (No action needed because there is no digital filter.)	• When the digital filter is in use Select the sampling clock for the digital filter by setting the LVD1CR0.LVD1FSAMP[1:0] bits. • When the digital filter is not in use — (No procedure)
	5	— (No action needed because there is no digital filter.)	• When the digital filter is in use Set LVD1CR0.LVD1DFDIS = 0 (enabling the digital filter). • When the digital filter is not in use — (No procedure)
	6	— (No action needed because there is no digital filter.)	• When the digital filter is in use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the digital filter is not in use — (No procedure)
	7	Set the LVCMPCR.LVD1E bit to 1 (voltage detection 1 circuit enabled).	Set LVD1CR0.LVD1RI = 0 (selecting the voltage monitoring 1 interrupt).
	8	Wait for at least td(E-A).	• Select the timing of interrupt requests by setting the LVD1CR1.LVD1IDTSEL[1:0] bits. • Select the type of interrupt by setting the LVD1CR1.LVD1IRQSEL bit.
	9	Set the LVD1CR0.LVD1CMPE bit to 1 (voltage monitoring 1 circuit comparison results output enabled).	— (No procedure)
	10	Wait for at least 2 μs.	— (No procedure)
	11	Set the LVD1SR.LVD1DET bit to 0.	Set LVD1SR.LVD1DET = 0.
	12	Set the LVD1CR0.LVD1RIE bit to 1 (voltage monitoring 1 interrupt/reset enabled).	Set LVD1CR0.LVD1RIE = 1 (enabling the voltage monitoring 1 interrupt or reset).
	13	— (No procedure)	Set LVD1CR0.LVD1CMPE = 1 (enabling output of the results of comparison by voltage monitoring 1).

Item		RX23T (LVDAb)	RX66T (LVDA)
Operation-enable setting procedure for bits related to voltage monitoring 1 reset	1	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.
	2	• Set the LVD1CR0.LVD1RI bit to 1 (voltage monitoring 1 reset). • Select the type of reset negation by setting the LVD1CR0.LVD1RN bit.	Set LVCMPCR.LVD1E = 1 (enabling the voltage detection 1 circuit).
	3	Set the LVD1CR0.LVD1RIE bit to 1 (voltage monitoring 1 interrupt/reset enabled).	Wait for at least td(E-A): LVD operation stabilization time (after LVD is enabled).
	4	— (No action needed because there is no digital filter.)	• When the digital filter is in use Select the sampling clock for the digital filter by setting the LVD1CR0.LVD1FSAMP[1:0] bits. • When the digital filter is not in use — (No procedure)
	5	— (No action needed because there is no digital filter.)	• When the digital filter is in use Set LVD1CR0.LVD1DFDIS = 0 (enabling the digital filter). • When the digital filter is not in use — (No procedure)
	6	— (No action needed because there is no digital filter.)	• When the digital filter is in use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the digital filter is not in use — (No procedure)
	7	Set the LVCMPCR.LVD1E bit to 1 (voltage detection 1 circuit enabled).	• Set LVD1CR0.LVD1RI = 1 (selecting the voltage monitoring 1 reset). • Select the type of the reset negation by setting the LVD1CR0.LVD1RN bit.
	8	Wait for at least td(E-A).	Set LVD1SR.LVD1DET = 0.
	9	— (No procedure)	Set LVD1CR0.LVD1RIE = 1 (enabling the voltage monitoring 1 interrupt or reset).
	10	Set the LVD1CR0.LVD1CMPE bit to 1 (voltage monitoring 1 circuit comparison results output enabled).	Set LVD1CR0.LVD1CMPE = 1 (enabling output of the results of comparison by voltage monitoring 1).

Table 2.12 Comparison of Operation-Disable Setting Procedures for Bits Related to Voltage Monitoring 1 Interrupt and Voltage Monitoring 1 Reset

Item		RX23T (LVDAb)	RX66T (LVDA)
Operation-disable setting procedure for bits related to voltage monitoring 1 interrupt	1	Set the LVD1CR0.LVD1RIE bit to 0 (voltage monitoring 1 interrupt/reset disabled).	Set LVD1CR0.LVD1CMPE = 0 (disabling output of the results of comparison by voltage monitoring 1).
	2	— (No action needed because there is no digital filter.)	• When the digital filter is in use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the digital filter is not in use — (No procedure)
	3	Set the LVD1CR0.LVD1CMPE bit to 0 (voltage monitoring 1 circuit comparison results output disabled).	Set LVD1CR0.LVD1RIE = 0 (disabling the voltage monitoring 1 interrupt or reset).
	4	— (No action needed because there is no digital filter.)	• When the digital filter is in use Set LVD1CR0.LVD1DFDIS = 1 (disabling the digital filter). • When the digital filter is not in use — (No procedure)
	5	Set the LVCMPCR.LVD1E bit to 0 (voltage detection 1 circuit disabled).	Set LVCMPCR.LVD1E = 0 (disabling the voltage detection 1 circuit).
	6	Modify settings of bits related to the voltage detection circuit registers other than LVCMPCR.LVD1E, LVD1CR0.LVD1RIE, and LVD1CR0.LVD1CMPE.	— (No procedure)

Item		RX23T (LVDAb)	RX66T (LVDA)
Operation-disable setting procedure for bits related to voltage monitoring 1 reset	1	Set the LVD1CR0.LVD1CMPE bit to 0 (voltage monitoring 1 circuit comparison results output disabled).	Set LVD1CR0.LVD1CMPE = 0 (disabling output of the results of comparison by voltage monitoring 1).
	2	— (No action needed because there is no digital filter.)	• When the digital filter is in use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the digital filter is not in use — (No procedure)
	3	Set the LVCMPCR.LVD1E bit to 0 (voltage detection 1 circuit disabled).	Set LVD1CR0.LVD1RIE = 0 (disabling the voltage monitoring 1 interrupt or reset).
	4	— (No action needed because there is no digital filter.)	• When the digital filter is in use Set LVD1CR0.LVD1DFDIS = 1 (disabling the digital filter). • When the digital filter is not in use — (No procedure)
	5	Set the LVD1CR0.LVD1RIE bit to 0 (voltage monitoring 1 interrupt/reset disabled).	Set LVCMPCR.LVD1E = 0 (disabling the voltage detection 1 circuit).
	6	Modify settings of bits related to the voltage detection circuit registers other than LVCMPCR.LVD1E, LVD1CR0.LVD1RIE, and LVD1CR0.LVD1CMPE.	— (No procedure)

Table 2.13 Comparison of Operation-Enable Setting Procedures for Bits Related to Voltage Monitoring 2 Interrupt and Voltage Monitoring 2 Reset

Item		RX23T (LVDAb)	RX66T (LVDA)
Operation-enable setting procedure for bits related to voltage monitoring 2 interrupt	1	Select the detection voltage by setting the LVDLVLR.LVD2LVL[1:0] bits.	Select the detection voltage by setting the LVDLVLR.LVD2LVL[3:0] bits.
	2	Set the LVD2CR0.LVD2RI bit to 0 (voltage monitoring 2 interrupt).	Set LVCMPCR.LVD2E = 1 (enabling the voltage detection 2 circuit).
	3	• Select the timing of interrupt requests by setting the LVD2CR1.LVD2IDTSEL[1:0] bits. • Select the type of interrupt by setting the LVD2CR1.LVD2IRQSEL bit.	Wait for at least td(E-A): LVD operation stabilization time (after LVD is enabled).
	4	— (No action needed because there is no digital filter.)	• When the digital filter is in use Select the sampling clock for the digital filter by setting the LVD2CR0.LVD2FSAMP[1:0] bits. • When the digital filter is not in use — (No procedure)
	5	— (No action needed because there is no digital filter.)	• When the digital filter is in use Set LVD2CR0.LVD2DFDIS = 0 (enabling the digital filter). • When the digital filter is not in use — (No procedure)
	6	— (No action needed because there is no digital filter.)	• When the digital filter is in use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the digital filter is not in use — (No procedure)
	7	Set the LVCMPCR.LVD2E bit to 1 (voltage detection 2 circuit enabled).	Set LVD2CR0.LVD2RI = 0 (selecting the voltage monitoring 2 interrupt).
	8	Wait for at least td(E-A).	• Select the timing of interrupt requests by setting the LVD2CR1.LVD2IDTSEL[1:0] bits. • Select the type of interrupt by setting the LVD2CR1.LVD2IRQSEL bit.
	9	Set the LVD2CR0.LVD2CMPE bit to 1 (voltage monitoring 2 circuit comparison results output enabled).	— (No procedure)
	10	Wait for at least 2 μs.	— (No procedure)
	11	Set the LVD2SR.LVD2DET bit to 0.	Set LVD2SR.LVD2DET = 0.
	12	Set the LVD2CR0.LVD2RIE bit to 1 (voltage monitoring 2 interrupt/reset enabled)	Set LVD2CR0.LVD2RIE = 1 (enabling the voltage monitoring 2 interrupt or reset).
	13	— (No procedure)	Set LVD2CR0.LVD2CMPE = 1 (enabling output of the results of comparison by voltage monitoring 2).

Item		RX23T (LVDAb)	RX66T (LVDA)
Operation-enable setting procedure for bits related to voltage monitoring 2 reset	1	Select the detection voltage by setting the LVDLVLR.LVD2LVL[1:0] bits.	Select the detection voltage by setting the LVDLVLR.LVD2LVL[3:0] bits.
	2	• Set the LVD2CR0.LVD2RI bit to 1 (voltage monitoring 2 reset). • Select the type of reset negation by setting the LVD2CR0.LVD2RN bit.	Set LVCMPCR.LVD2E = 1 (enabling the voltage detection 2 circuit).
	3	Set the LVD2CR0.LVD2RIE bit to 1 (voltage monitoring 2 interrupt/reset enabled).	Wait for at least td(E-A): LVD operation stabilization time (after LVD is enabled).
	4	— (No action needed because there is no digital filter.)	• When the digital filter is in use Select the sampling clock for the digital filter by setting the LVD2CR0.LVD2FSAMP[1:0] bits. • When the digital filter is not in use — (No procedure)
	5	— (No action needed because there is no digital filter.)	• When the digital filter is in use Set LVD2CR0.LVD2DFDIS = 0 (enabling the digital filter). • When the digital filter is not in use — (No procedure)
	6	— (No action needed because there is no digital filter.)	• When the digital filter is in use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the digital filter is not in use — (No procedure)
	7	Set the LVCMPCR.LVD2E bit to 1 (voltage detection 2 circuit enabled).	• Set LVD2CR0.LVD2RI = 1 (selecting the voltage monitoring 2 reset). • Select the type of the reset negation by setting the LVD2CR0.LVD2RN bit.
	8	Wait for at least td(E-A).	Set LVD2SR.LVD2DET = 0.
	9	— (No procedure)	Set LVD2CR0.LVD2RIE = 1 (enabling the voltage monitoring 2 interrupt or reset).
	10	Set the LVD2CR0.LVD2CMPE bit to 1 (voltage monitoring 2 circuit comparison results output enabled).	Set LVD2CR0.LVD2CMPE = 1 (enabling output of the results of comparison by voltage monitoring 2).

Table 2.14 Comparison of Operation-Disable Setting Procedures for Bits Related to Voltage Monitoring 2 Interrupt and Voltage Monitoring 2 Reset

Item		RX23T (LVDAb)	RX66T (LVDA)
Operation-disable setting procedure for bits related to voltage monitoring 2 interrupt	1	Set the LVD2CR0.LVD2RIE bit to 0 (voltage monitoring 2 interrupt/reset disabled).	Set LVD2CR0.LVD2CMPE = 0 (disabling output of the results of comparison by voltage monitoring 2).
	2	— (No action needed because there is no digital filter.)	• When the digital filter is in use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the digital filter is not in use — (No procedure)
	3	Set the LVD2CR0.LVD2CMPE bit to 0 (voltage monitoring 2 circuit comparison results output disabled).	Set LVD2CR0.LVD2RIE = 0 (disabling the voltage monitoring 2 interrupt or reset).
	4	— (No action needed because there is no digital filter.)	• When the digital filter is in use Set LVD2CR0.LVD2DFDIS = 1 (disabling the digital filter). • When the digital filter is not in use — (No procedure)
	5	Set the LVCMPCR.LVD2E bit to 0 (voltage monitoring 2 circuit disabled).	Set LVCMPCR.LVD2E = 0 (disabling the voltage detection 2 circuit).
	6	Modify settings of bits related to the voltage detection circuit registers other than LVCMPCR.LVD2E, LVD2CR0.LVD2RIE, and LVD2CR0.LVD2CMPE.	—

Item		**RX23T (LVDAb)**	**RX66T (LVDA)**
Operation-disable setting procedure for bits related to voltage monitoring 2 reset	1	Set the LVD2CR0.LVD2CMPE bit to 0 (voltage monitoring 2 circuit comparison results output disabled).	Set LVD2CR0.LVD2CMPE = 0 (disabling output of the results of comparison by voltage monitoring 2).
	2	— (No action needed because there is no digital filter.)	• When the digital filter is in use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the digital filter is not in use — (No procedure)
	3	Set the LVCMPCR.LVD2E bit to 0 (voltage monitoring 2 circuit disabled).	Set LVD2CR0.LVD2RIE = 0 (disabling the voltage monitoring 2 interrupt or reset).
	4	— (No action needed because there is no digital filter.)	• When the digital filter is in use Set LVD2CR0.LVD2DFDIS = 1 (disabling the digital filter). • When the digital filter is not in use — (No procedure)
	5	Set the LVD2CR0.LVD2RIE bit to 0 (voltage monitoring 2 interrupt/reset disabled).	Set LVCMPCR.LVD2E = 0 (disabling the voltage detection 2 circuit).
	6	Modify settings of bits related to the voltage detection circuit registers other than LVCMPCR.LVD2E, LVD2CR0.LVD2RIE, and LVD2CR0.LVD2CMPE.	— (No procedure)

2.7 Clock Generation Circuit

Table 2.15 is a comparative overview of the clock generation circuits, and Table 2.16 is a comparison of clock generation circuit registers.

Table 2.15 Comparative Overview of Clock Generation Circuits

Item	RX23T	RX66T
Use	• Generates the system clock (ICLK) to be supplied to the CPU, DTC, ROM, and RAM. • Generates the peripheral module clocks (PCLKA, PCLKB, and PCLKD) to be supplied to peripheral modules. The peripheral module clock PCLKA is the operating clock for the MTU3, the peripheral module clock PCLKD is for the S12AD, and PCLKB is for modules other than MTU3 and S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the IWDT-dedicated low-speed clock (IWDTCLK) to be supplied to the IWDT.	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the RSPI, SCIi, MTU3 (internal peripheral buses), GPTW (internal peripheral buses), and HRPWM (internal peripheral buses). • Generates the peripheral module clock (PCLKB) to be supplied to peripheral modules. • Generates the counter reference clock for the peripheral module to be supplied to the MTU3 and GPTW and the reference clock (PCLKC) for the HRPWM. • Generates the peripheral module clocks (for analog conversion) (PCLKD) to be supplied to S12AD. • Generates the flash-IF clock (FCLK) to be supplied to the flash interface. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the USB clock (UCLK) to be supplied to the USBb. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.
Operating frequency	• ICLK: 40 MHz (max.) • PCLKA: 40 MHz (max.) • PCLKB: 40 MHz (max.) • PCLKD: 40 MHz (max.)	• ICLK: 160 MHz (max.) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKC: 160 MHz (max.) • PCLKD: 8 MHz to 60 MHz (for conversion with 12-bit A/D converter)

Item	RX23T	RX66T
Operating frequency	• FCLK: 1 MHz to 32 MHz (ROM) • CACCLK: Same frequency as each oscillator • IWDTCLK: 15 kHz	• FCLK: — 4 MHz to 60 MHz (for programming and erasing the code flash memory and data flash memory) — 60 MHz (max.) (for reading from the data flash memory) • BCLK: 60 MHz (max.) • BCLK pin output: 40 MHz (max.) • UCLK: 48 MHz (max.) • CACCLK: Same as the clock from respective oscillators. • CANMCLK: 24 MHz (max.) • IWDTCLK: 120 kHz
Main clock oscillator	• Resonator frequency: 1 MHz to 20 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When main clock oscillation stop is detected, the system clock source switches to LOCO, MTU pin output stops, and a non-maskable interrupt is generated. • Drive capacity switching function	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal resonator • Connection pin: EXTAL, XTAL • Oscillation stop detection function: When main clock oscillation stop is detected, the system clock source switches to LOCO, MTU3 and GPTW output is driven high-impedance. • Drive capacity switching function
PLL frequency synthesizer	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 12.5 MHz • Frequency multiplication ratio: Selectable from 4 to 10 (increments of 0.5) • Oscillation frequency: 40 MHz to 80 MHz	• Input clock source: Main clock, HOCO • Input pulse frequency division ratio: Selectable from 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable from 10 to 30 (increments of 0.5) • Output clock frequency of the PLL frequency synthesizer: 120 MHz to 240 MHz
High-speed on-chip oscillator (HOCO)	Oscillation frequency: 32 MHz	• Oscillation frequency: Selectable from 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 4 MHz	Oscillation frequency: 240 kHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 15 kHz	Oscillation frequency: 120 kHz
Control of output on BCLK pin	—	• BCLK clock output or high output is selectable • BCLK or BCLK/2 is selectable
Event linking function (output)	—	Detection of stopping of the main clock oscillator
Event linking function (input)	—	Switching of the clock source to the low-speed on-chip oscillator

Table 2.16 Comparison of Clock Generation Circuit Registers

Register	Bit	RX23T	RX66T
SCKCR	—	System clock control register	System clock control register
		Initial value after a reset differs.	
	PCKC[3:0]	—	Peripheral module clock C (PCLKC) select bits
	BCK[3:0]	—	External bus clock (BCLK) select bits
	PSTOP1	—	BCLK pin output control bit
SCKCR2	—		System clock control register 2
PLLCR	—	PLL control register	PLL control register
		Initial value after a reset differs.	
	PLIDIV[1:0]	PLL input frequency division ratio select bits b1 b0 0 0: ×1 0 1: ×1/2 1 0: ×1/4 1 1: Setting prohibited	PLL input frequency division ratio select bits b1 b0 0 0: ×1 0 1: ×1/2 1 0: ×1/3 1 1: Setting prohibited
	PLLSRCSEL	—	PLL clock source select bit
	STC[5:0]	Frequency multiplication factor select bits b13 b8 0 0 0 1 1 1: ×4 0 0 1 0 0 0: ×4.5 0 0 1 0 0 1: ×5 0 0 1 0 1 0: ×5.5 0 0 1 0 1 1: ×6 0 0 1 1 0 0: ×6.5 0 0 1 1 0 1: ×7 0 0 1 1 1 0: ×7.5 0 0 1 1 1 1: ×8 0 1 0 0 0 0: ×8.5 0 1 0 0 0 1: ×9 0 1 0 0 1 0: ×9.5 0 1 0 0 1 1: ×10 Settings other than the above are prohibited.	Frequency multiplication factor select bits b13 b8 0 1 0 0 1 1: ×10.0 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11.0 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12.0 0 1 1 0 0 0: ×12.5 : 1 1 1 0 0 1: ×29.0 1 1 1 0 1 0: ×29.5 1 1 1 0 1 1: ×30.0 Settings other than the above are prohibited.
BCKCR	—	—	External bus clock control register
HOCOCR2	—	—	High-speed on-chip oscillator control register 2
HOCOWTCR	—	High-speed on-chip oscillator wait control register	—

Register	Bit	RX23T	RX66T
OSCOVFSR	—	Oscillation stabilization flag register	Oscillation stabilization flag register
		Initial value after a reset differs.*1	
	ILCOVF	—	IWDT-dedicated clock oscillation stabilization flag
OSTDCR	OSTDIE	Oscillation stop detection interrupt enable bit 0: The oscillation stop detection interrupt is disabled. Oscillation stop detection is not reported to the POE. 1: The oscillation stop detection interrupt is enabled. Oscillation stop detection is reported to the POE.	Oscillation stop detection interrupt enable bit 0: The oscillation stop detection interrupt is disabled. Oscillation stop detection is not reported to the POE/POEG. 1: The oscillation stop detection interrupt is enabled. Oscillation stop detection is reported to the POE/POEG.
MOSCWTCR	—	Main clock oscillator wait control register	Main clock oscillator wait control register
		Initial value after a reset differs.	
	MSTS[4:0] (RX23T) MSTS[7:0] (RX66T)	Main clock oscillator wait time bits b4 b0 0 0 0 0 0: Wait time = 2 cycles (0.5 µs) 0 0 0 0 1: Wait time = 1,024 cycles (256 µs) 0 0 0 1 0: Wait time = 2,048 cycles (512 µs) 0 0 0 1 1: Wait time = 4,096 cycles (1.024 ms) 0 0 1 0 0: Wait time = 8,192 cycles (2.048 ms) 0 0 1 0 1: Wait time = 16,384 cycles (4.096 ms) 0 0 1 1 0: Wait time = 32,768 cycles (8.192 ms) 0 0 1 1 1: Wait time = 65,536 cycles (16.384 ms) Settings other than the above are prohibited. Wait time when LOCO = 4.0 MHz (0.25 µs, TYP.)	Waiting time until output of main clock oscillator is supplied to internal circuits MSTS[7:0] > [tMAINOSC × (fLOCO_max) + 16] / 32 (tMAINOSC: main clock oscillation stabilization time; fLOCO_max: maximum frequency for fLOCO)
MOFCR	MODRV21 (RX23T) MODRV2 [1:0] (RX66T)	Main clock oscillator drive capability switch bit 0: 1 MHz or higher and lower than 10 MHz 1: 10 MHz to 20 MHz	Main clock oscillator driving ability 2 switching bits b5 b4 0 0: 20.1 to 24 MHz 0 1: 16.1 to 20 MHz 1 0: 8.1 to 16 MHz 1 1: 8 MHz
HOCOPCR	—	—	High-speed on-chip oscillator power supply control register

Note: 1. On the RX66T Group, when the value of the OFS0.IWDTSTRT bit is 0, the value of the ILCOVF flag after a reset will be 1, and when the value of the OFS0.IWDTSTRT bit is 1, the value of the ILCOVF flag after a reset will be 0.

2.8 Low Power Consumption

Table 2.17 is a comparative overview of the low power consumption functions, Table 2.18 is a comparison of procedures for entering and exiting low power consumption modes and operating states in each mode, and Table 2.19 is a comparison of low power consumption registers.

Table 2.17 Comparative Overview of Low Power Consumption Functions

Item	RX23T	RX66T
Reducing power consumption by switching clock signals	The frequency division ratio can be set independently for the system clock (ICLK), high speed peripheral module clock (PCLKA), peripheral module clock (PCLKB), S12AD clock (PCLKD), and FlashIF clock (FCLK).	The frequency division ratio is settable independently for the system clock (ICLK), peripheral module clock (PCLKA, PCLKB, PCLKC, PCLKD), external bus clock (BCLK), and flash interface clock (FCLK).
BCLK output control function	—	BCLK output or high-level output can be selected.
Module-stop function	Each peripheral module can be stopped independently by the module stop control register.	Functions can be stopped independently for each peripheral module.
Function for transition to low power consumption mode	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.
Low power consumption modes	• Sleep mode • Software standby mode • Deep sleep mode	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode
Operating power control modes	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Two operating power control modes are available — High-speed operating mode — Middle-speed operating mode	—

Table 2.18 Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX23T	RX66T
Sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX23T	RX66T
Sleep mode	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM0: RX23T RAM and ECCRAM: RX66T	Operation possible (retained)	Operation possible (retained)
	DTC	Operation possible	Operation possible
	Flash memory	Operation	Operation
	USB FS Host/Function module (USBb)	—	Operation possible
	Watchdog timer (WDTA)	—	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Port output enable (POE)	Operation possible	Operation possible
	8-bit timer (unit 0, unit 1) (TMR)	Operation possible	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Operation possible	Operation possible
	I/O ports	Operation	Operation
	Comparator C	Operation possible	Operation possible
Software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Stopped	Stopped
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Stopped
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Stopped	Stopped
	CPU	Stopped (retained)	Stopped (retained)
	RAM0: RX23T RAM and ECCRAM: RX66T	Stopped (retained)	Stopped (retained)
	DTC	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	USB FS Host/Function module (USBb)	—	Stopped
	Watchdog timer (WDTA)	—	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Port output enable (POE)	Stopped (retained)	Stopped (retained)
	8-bit timer (unit 0, unit 1) (TMR)	Stopped (retained)	Stopped (retained)
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained
	Comparator C	Operation possible	Operation possible

Note: "Operation possible" means that whether the state is operating or stopped is controlled by the control register setting.
"Stopped (retained)" means that internal register values are retained and internal operations are suspended.
"Stopped (undefined)" means that internal register values are undefined and power is not supplied to the internal circuit.

Table 2.19 Comparison of Low Power Consumption Registers

Register	Bit	RX23T	RX66T
SBYCR	OPE	—	Output port enable bit
	SSBY	Software standby bit 0: Set entry to sleep mode or deep sleep mode after the WAIT instruction is executed 1: Set entry to software standby mode after the WAIT instruction is executed	Software standby bit 0: Shifts to sleep mode or all-module clock stop mode after the WAIT instruction is executed 1: Shifts to software standby mode after the WAIT instruction is executed
MSTPCRA	—	Module stop control register A	Module stop control register A
		Initial value after a reset differs.	
	MSTPA2	—	8-bit timer 7/6 (unit 3) module stop bit
	MSTPA3	—	8-bit timer 5/4 (unit 2) module stop bit
	MSTPA7	—	General PWM timer/ high resolution PWM/ GPTW-dedicated port output enable module stop bit
	MSTPA16	—	12-bit A/D converter (unit 1) module stop bit
	MSTPA23	—	12-bit A/D converter (unit 2) module stop bit
	MSTPA24	—	Module stop A24 bit
	MSTPA27	—	Module stop A27 bit
	MSTPA28	Data transfer controller module stop bit	DMA controller/data transfer controller module stop bit
	MSTPA29	—	Module stop A29 bit
	ACSE	—	All-module clock stop mode enable bit
MSTPCRB	MSTPB0	—	CAN module 0 module stop bit
	MSTPB4	—	Serial communication interface 12 module stop bit
	MSTPB9	—	Event link controller module stop bit
	MSTPB19	—	Universal serial bus 2.0 FS interface module stop bit
	MSTPB25	—	Serial communications interface 6 module stop bit
MSTPCRC	MSTPC6	—	ECCRAM module stop bit
	MSTPC24	—	Serial communications interface 11 module stop bit
	MSTPC26	—	Serial communications interface 9 module stop bit
	MSTPC27	—	Serial communications interface 8 module stop bit
	DSLPE	Deep sleep mode enable bit	—
MSTPCRD	—	—	Module stop control register D
RSTCKCR	—	—	Sleep mode return clock source switching register
DPSBYCR	—	—	Deep standby control register
DPSIER0	—	—	Deep standby interrupt enable register 0

Register	Bit	RX23T	RX66T
DPSIER1	—	—	Deep standby interrupt enable register 1
DPSIER2	—	—	Deep standby interrupt enable register 2
DPSIFR0	—	—	Deep standby interrupt flag register 0
DPSIFR1	—	—	Deep standby interrupt flag register 1
DPSIFR2	—	—	Deep standby interrupt flag register 2
DPSIEGR0	—	—	Deep standby interrupt edge register 0
DPSIEGR1	—	—	Deep standby interrupt edge register 1
DPSIEGR2	—	—	Deep standby interrupt edge register 2
DPSBKRy	—	—	Deep standby backup register (y = 0 to 31)
OPCCR	—	Operating power control register	—

2.9 Register Write Protection Function

Table 2.20 is a comparative overview of the register write protection functions, and Table 2.21 is a comparison of register write protection function registers.

Table 2.20 Comparative Overview of Register Write Protection Functions

Item	RX23T	RX66T
PRC0 bit	Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, MEMWAIT	Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, OSTDCR, OSTDSR
PRC1 bit	• Register related to the operating modes: SYSCR1 • Registers related to low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR • Registers related to the clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR	• Registers related to the operating modes: SYSCR0, SYSCR1, VOLSR • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, RSTCKCR, DPSBYCR, DPSIER0 to DPSIER2, DPSIFR0 to DPSIFR2, DPSIEGR0 to DPSIEGR2 • Registers related to clock generation circuit: MOSCWTCR, MOFCR, HOCOPCR • Software reset register: SWRR
PRC2 bit	Register related to the clock generation circuit: HOCOWTCR	—
PRC3 bit	Registers related to the LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	Registers related to the LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

Table 2.21 Comparison of Register Write Protection Function Registers

Register	Bit	RX23T	RX66T
PRCR	PRC2	Protect bit 2	—

2.10 Interrupt Controller

Table 2.22 is a comparative overview of the interrupt controllers, and Table 2.23 is a comparison of interrupt controller registers.

Table 2.22 Comparative Overview of Interrupt Controllers

Item		**RX23T (ICUb)**	**RX66T (ICUC)**
Interrupts	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection Edge detection or level detection is fixed for each source of connected peripheral modules.	• Interrupts from peripheral modules • Interrupt detection method: Edge detection/level detection (fixed for each interrupt source) • Group interrupt: Multiple interrupt sources are grouped together and treated as an interrupt source. — Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) — Group BL0/BL1 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) — Group AL0 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.
	External pin interrupts	• Interrupts from pins IRQ0 to IRQ5 • Number of sources: 6 • Interrupt detection: Low level/falling edge/rising edge/rising and falling edges One of these detection methods can be set for each source. • Digital filter function: Supported	• Interrupt by the input signal to the IRQi pin (i = 0 to 15) • Interrupt detection method: Detection of low level, falling edge, rising edge, rising and falling edges One of these detection methods can be set for each source. • Digital filter can be used to remove noise.
	Software interrupt	• Interrupt generated by writing to a register • One interrupt source	• Interrupt request can be generated by writing to a register. • Two interrupt sources

Item		RX23T (ICUb)	RX66T (ICUC)
Interrupts	Interrupt priority level	Specified by registers.	Priority level can be set with interrupt source priority register r (IPRr) (r = 000 to 255).
	Fast interrupt function	Enables faster processing of CPU interrupts. Only a single interrupt source can be specified.	CPU interrupt response time can be reduced. This function can be used for only one interrupt source.
	DTC and DMAC control	Interrupt sources can be used to start the DTC.	Interrupt sources can be used to start the DTC and DMAC.
Non-maskable interrupts	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter function: Supported	• Interrupt by the input signal to the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter can be used to remove noise.
	Oscillation stop detection interrupt	Interrupt on detection of oscillation having stopped	This interrupt occurs when the main clock oscillator stop is detected.
	WDT underflow/ refresh error interrupt	—	This interrupt occurs when the watchdog timer underflows or a refresh error occurs.
	IWDT underflow/ refresh error interrupt	This interrupt occurs when the down counter underflows or a refresh error occurs.	This interrupt occurs when the independent watchdog timer underflows or a refresh error occurs.
	Voltage monitoring 1 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)	Interrupt from voltage detection circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)	Interrupt from voltage detection circuit 2 (LVD2)
	RAM error interrupt	—	This interrupt occurs when a RAM parity check error or an ECCRAM ECC error occurs.
Return from low power consumption state	Sleep mode	Return is initiated by non-maskable interrupts or any other interrupt source.	Exit sleep mode by any interrupt source.
	All-module clock stop mode	—	Exit all-module clock stop mode by the NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection interrupt, USB resume, IWDT, TMR0 to TMR3).
	Deep sleep mode	Return is initiated by non-maskable interrupts or any other interrupt source.	—
	Software standby mode	Return is initiated by non-maskable interrupts, IRQ0 to IRQ5 interrupts, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, IWDT).	Exit software standby mode by the NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, IWDT).

Item		RX23T (ICUb)	RX66T (ICUC)
Return from low power consumption state	Deep software standby mode	—	Exit deep software standby mode by the NMI pin interrupt, specific external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2).

Table 2.23 Comparison of Interrupt Controller Registers

Register	Bit	RX23T (ICUb)	RX66T (ICUC)
IRn*1	—	Interrupt request register n (n = 016 to 249)	Interrupt request register n (n = 016 to 255)
IPRn*1	—	Interrupt source priority register n (n = 000 to 249)	Interrupt source priority register n (n = 000 to 255)
SWINT2R	—	—	Software interrupt 2 generation register
DTCERn*1	—	DTC transfer request enable register n (n = 027 to 248)	DTC transfer request enable register n (n = 026 to 255)
DMRSRm	—	—	DMAC trigger select register m (m = 0 to 7)
IRQCRi	—	IRQ control register i (i = 0 to 5)	IRQ control register i (i = 0 to 15)
IRQFLTE0	FLTEN6	—	IRQ6 digital filter enable bit
	FLTEN7	—	IRQ7 digital filter enable bit
IRQFLTE1	—	—	IRQ pin digital filter enable register 1
IRQFLTC0	FCLKSEL6 [1:0]	—	IRQ6 digital filter sampling clock bits
	FCLKSEL7 [1:0]	—	IRQ7 digital filter sampling clock bits
IRQFLTC1	—	—	IRQ pin digital filter setting register 1
NMISR	WDTST	—	WDT underflow/refresh error status flag
	RAMST	—	RAM error interrupt status flag
NMIER	WDTEN	—	WDT underflow/refresh error enable bit
	RAMEN	—	RAM error interrupt enable bit
NMICLR	WDTCLR	—	WDT clear bit
GRPBE0	—	—	Group BE0 interrupt request register
GRPBL0/GRPBL1	—	—	Group BL0/BL1 interrupt request register
GRPAL0	—	—	Group AL0 interrupt request register
GENBE0	—	—	Group BE0 interrupt request register
GENBL0/GENBL1	—	—	Group BL0/BL1 interrupt request enable register
GENAL0	—	—	Group AL0 interrupt request enable register
GCRBE0	—	—	Group BE0 interrupt clear register

Register	Bit	RX23T (ICUb)	RX66T (ICUC)
PIARk	—	—	Software configurable interrupt A request register k (k = 0h to 12h)
SLIARn	—	—	Software configurable interrupt A source select register n (n = 208 to 255)
SLIPRCR	—	—	Software configurable interrupt source select register write protect register

Note: 1. On the RX23T Group n = 250 to 255 correspond to a reserved area.

2.11 Buses

Table 2.24 is a comparative overview of the buses, Table 2.25 is a comparative overview of the external buses, and Table 2.26 is a comparison of bus registers.

Table 2.24 Comparative Overview of Buses

Item		RX23T	RX66T
CPU bus	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Memory bus	Memory bus 1	Connected to RAM	Connected to RAM
	Memory bus 2	Connected to ROM	Connected to code flash memory
	Memory bus 3	—	Connected to ECCRAM
Internal main bus	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the DMAC and DTC • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Internal peripheral bus	Internal peripheral bus 1	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, and 4) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 3	• Connected to peripheral modules (CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (USBb and CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 4	• Connected to peripheral modules (MTU3) • Operates in synchronization with the peripheral-module clock (PCLKA)	• Connected to peripheral modules (MTU3, GPTW, HRPWM, RSPI and SCIi) • Operates in synchronization with the peripheral-module clock (PCLKA)

Item		RX23T	RX66T
Internal peripheral bus	Internal peripheral bus 5	—	Reserved area
	Internal peripheral bus 6	• Connected to the flash control module • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to code flash (in P/E) and data flash memory • Operates in synchronization with the FlashIF clock (FCLK)
External bus	CS area	—	• Connected to the external devices • Operates in synchronization with the external-bus clock (BCLK: 40 MHz (max.))

Table 2.25 Comparative Overview of External Buses

Item	RX23T	RX66T
External address space	—	• An external address space is divided into four CS areas (CS0 to CS3) for management. • Chip select signals can be output for each area. • Bus width can be set for each area. — Separate bus: An 8 or 16-bit bus space is selectable. — Address/data multiplexed bus: An 8 or 16-bit bus space is selectable. • An endian mode can be specified for each area.
CS area controller	—	• Recovery cycles can be inserted. — Read recovery: Up to 15 cycles — Write recovery: Up to 15 cycles • Cycle wait function: Wait for up to 31 cycles (page access: up to 7 cycles) • Wait control can be used to set up the following. — Timing of assertion and negation for chip-select signals (CS0# to CS3#) — The timing of assertion of the read signal (RD#) and write signals (WR0#/WR# to WR1#) — The timing with which data output starts and ends • Write access mode: Single write strobe mode/byte strobe mode • Separate bus or address/data multiplexed bus can be set for each area.
Write buffer function	—	When write data from the bus master has been written to the write buffer, write access by the bus master is completed.

Item	RX23T	RX66T
Frequency	—	The CS area controller (CSC) operates in synchronization with the external-bus clock (BCLK).

Table 2.26 Comparison of Bus Registers

Register	Bit	RX23T	RX66T
CSnCR	—	—	CSn control register (n = 0 to 3)
CSnREC	—	—	CSn recovery cycle register (n = 0 to 3)
CSRECEN	—	—	CS recovery cycle insertion enable register
CSnMOD	—	—	CSn mode register (n = 0 to 3)
CSnWCR1	—	—	CSn wait control register 1 (n = 0 to 3)
CSnWCR2	—	—	CSn wait control register 2 (n = 0 to 3)
BERSR1	MST[2:0]	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved
BUSPRI	BPRA[1:0]	Memory bus 1 (RAM) priority control bits	Memory bus 1 and 3 (RAM/ECCRAM) priority control bits
	BPEB[1:0]	—	External bus priority control bits

2.12 Data Transfer Controller

Table 2.27 is a comparative overview of the data transfer controllers.

Table 2.27 Comparative Overview of Data Transfer Controllers

Item	RX23T (DTCa)	RX66T (DTCa)
Number of transfer channels	The same number as all interrupt sources that can start the DTC transfer.	The same number as all interrupt sources that can start the DTC transfer.
Transfer modes	• Normal transfer mode A single transfer request leads to a single data transfer. • Repeat transfer mode — A single transfer request leads to a single data transfer. — The transfer address is returned to the transfer start address after the number of data transfers corresponding to “repeat size”. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, 1,024 bytes. • Block transfer mode — A single transfer request leads to the transfer of a single block. — The maximum block size is 256 × 32 bits = 1,024 bytes.	• Normal transfer mode A single transfer request leads to a single data transfer. • Repeat transfer mode — A single transfer request leads to a single data transfer. — The transfer address is returned to the transfer start address after the number of data transfers corresponding to “repeat size”. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, 1,024 bytes. • Block transfer mode — A single transfer request leads to the transfer of a single block. — The maximum block size is 256 × 32 bits = 1,024 bytes.
Chain transfer function	• Multiple data units can be transferred by a single activation source (chain transfer). • Either “executed when the counter is 0” or “always executed” can be selected for chain transfer.	• Multiple types of data transfers can sequentially be executed in response to a single request. • Either “performed only when the transfer counter becomes 0” or “every time” can be selected.
Transfer space	• In short-address mode: 16 MB (Areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh except reserved areas) • In full-address mode: 4 GB (Area from 0000 0000h to FFFF FFFFh except reserved areas)	• In short-address mode: 16 MB (Areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh except reserved areas) • In full-address mode: 4 GB (Area from 0000 0000h to FFFF FFFFh except reserved areas)
Data transfer units	• Single data: 1 byte (8 bits), 1 word (16 bits), 1 longword (32 bits) • Single block size: 1 to 256 data	• Single data: 1 byte (8 bits), 1 word (16 bits), 1 longword (32 bits) • Single block size: 1 to 256 data
CPU interrupt requests	• An interrupt request can be generated to the CPU on a request source for a data transfer. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of specified volume.	• An interrupt request can be generated to the CPU on a request source for a data transfer. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of specified volume.
Event linking function	—	An event link request is generated after one data transfer (for block, after one block transfer).

Item	RX23T (DTCa)	RX66T (DTCa)
Read skip	Transfer information read skipping can be specified.	Reading of the transfer information can be skipped when the same transfer is repeated.
Write-back skip	Write-back skipping can be specified when “fixed” is selected for the transfer source address or transfer destination address.	Write-back of the transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

2.13 I/O Ports

Table 2.28 is a comparative overview of the I/O ports of 64-pin products, Table 2.30 is a comparison of I/O port functions, and Table 2.31 is a comparison of I/O port registers.

Table 2.28 Comparative Overview of I/O Ports of 64-Pin Products

Item	RX23T (64-Pin)	RX66T (64-Pin)
PORT0	P00 to P02	P00, P01
PORT1	P10, P11	P11
PORT2	P22 to P24	P20 to P22
PORT3	P30 to P33, P36, P37	P36, P37
PORT4	P40 to P47	P40 to P42, P44 to P46
PORT5	—	P52 to P54
PORT6	—	P64, P65
PORT7	P70 to P76	P70 to P76
PORT9	P91 to P94	P90 to P96
PORTA	PA2 to PA5	—
PORTB	PB0 to PB7	PB0 to PB6
PORTD	PD3 to PD7	PD3 to PD7
PORTE	PE2	PE2
PORTH	—	PH0, PH4

Table 2.29 Comparative Overview of I/O Ports of 48-Pin Products

Item	RX23T (48-Pin)	RX66T (48-Pin)
PORT0	—	P00
PORT1	P10, P11	P10, P11
PORT2	P22 to P24	—
PORT3	P36, P37	P36, P37
PORT4	P40 to P47	P40 to P44
PORT6	—	P62, P64, P65
PORT7	P70 to P76	P71 to P76
PORT9	P93, P94	P94
PORTA	PA2, PA3	PA3, PA5
PORTB	PB0 to PB6	PB0 to PB6
PORTD	PD3 to PD6	PD3, PD5, PD7
PORTE	PE2	PE2

Table 2.30 Comparison of I/O Port Functions

Item	Port Symbol	RX23T	RX66T
Input pull-up function	PORT0	P00 to P02	P00, P01
	PORT1	P10, P11	P10 to P17
	PORT2	P22 to P24	P20 to P27
	PORT3	P30 to P33, P36, P37	P30 to P37
	PORT4	P40 to P47	P43, P47
	PORT5	—	P50 to P55
	PORT6	—	P60 to P65
	PORT7	P70, P71 to P76	P70 to P76
	PORT8	—	P80, P81, P82
	PORT9	P91 to P94	P90 to P96
	PORTA	PA2 to PA5	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7

Item	Port Symbol	RX23T	RX66T
Input pull-up function	PORTC	—	PC0 to PC6
	PORTD	PD3 to PD7	PD0 to PD7
	PORTE	—	PE0, PE1, PE3 to PE6
	PORTF	—	PF0 to PF3
	PORTG	—	PG0 to PG2
	PORTH	—	PH1 to PH3, PH5 to PH7
	PORTK	—	PK0 to PK2
Open-drain output function	PORT0	P00 to P02	P00, P01
	PORT1	P10, P11	P10 to P17
	PORT2	P22 to P24	P20 to P27
	PORT3	P30 to P33, P36, P37	P30 to P37
	PORT4	—	P43, P47
	PORT5	—	P50 to P55
	PORT6	—	P60 to P65
	PORT7	P70, P71 to P76	P70 to P76
	PORT8	—	P80, P81, P82
	PORT9	P91 to P94	P90 to P96
	PORTA	PA2 to PA5	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	—	PC0 to PC6
	PORTD	PD3 to PD7	PD0 to PD7
	PORTE	—	PE0, PE1, PE3 to PE6
	PORTF	—	PF0 to PF3
	PORTG	—	PG0 to PG2
	PORTH	—	PH1 to PH3, PH5 to PH7
	PORTK	—	PK0 to PK2
Drive capacity switching function	PORT0	P00 to P02	P00, P01
	PORT1	P10, P11	P10 to P17
	PORT2	P22 to P24	P20 to P27
	PORT3	P30 to P33, P36, P37	P30 to P37
	PORT4	P40 to P47	P43, P47
	PORT5	—	P50 to P55
	PORT6	—	P60 to P65
	PORT7	P70, P71 to P76	P70 to P76
	PORT8	—	P80, P81, P82
	PORT9	P91 to P94	P90 to P96
	PORTA	PA2 to PA5	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	—	PC0 to PC6
	PORTD	PD3 to PD7	PD0 to PD7
	PORTE	—	PE0, PE1, PE3 to PE6
	PORTF	—	PF0 to PF3
	PORTG	—	PG0 to PG2
	PORTH	—	PH1 to PH3, PH5 to PH7
	PORTK	—	PK0 to PK2
5 V tolerant	PORTB	PB1, PB2	PB1, PB2
	PORTC	—	PC0*1
	PORTD	—	PD2*1

Note: 1. Implemented only on products with a RAM capacity of 128 KB.

Table 2.31 Comparison of I/O Port Registers

Register	Bit	RX23T	RX66T
PDR	B0 to B7	Pm0 to Pm7 I/O select bits (m = 0 to 4, 7, 9, A, B, D)	Pm0 to Pm7 I/O select bits (m = 0 to 9, A to H, K)
PODR	B0 to B7	Pm0 to Pm7 output data store bits (m = 0 to 4, 7, 9, A, B, D)	Pm0 to Pm7 output data store bits (m = 0 to 9, A to H, K)
PIDR	B0 to B7	Pm0 to Pm7 bits (m = 0 to 4, 7, 9, A, B, D, E)	Pm0 to Pm7 bits (m = 0 to 9, A to H, K)
PMR	B0 to B7	Pm0 pin mode control bits (m = 0 to 3, 7, 9, A, B, D, E)	Pm0 to Pm7 pin mode control bits (m = 0 to 9, A to H, K)
ODR0	B0, B2, B4, B6	Pm0 to Pm3 output type select bit (m = 0, 1 to 3, 7, 9, A, B, D)	Pm0 to Pm3 output type select bit (m = 0 to 9, A to H, K)
ODR1	B0, B2, B4, B6	Pm4 to Pm7 output type select bit (m = 2, 3, 7, 9, A, B, D)	Pm4 to Pm7 output type select bit (m = 1 to 7, 9, A to E, H)
PCR	B0 to B7	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 4, 7, 9, A, B, D)	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A to H, K)
DSCR	B0 to B7	Pm0 to Pm7 drive capacity control bits (m = 0 to 3, 7, 9, A, B, D)	Pm0 to Pm7 drive capacity control bits (m = 0 to 3, 7 to 9, A to G, K)
DSCR2	—	—	Drive capacity control register 2

2.14 Multi-Function Pin Controller

Table 2.32 is a comparison of the assignments of multiplexed pins, and Table 2.33 to Table 2.52 are comparisons of multi-function pin controller registers.

In the following comparison of the assignments of multiplexed pins, **light blue text** designates pins that exist on the RX66T Group only and **orange text** pins that exist on the RX23T Group only. A circle (○) indicates that a function is assigned, a cross (×) that the pin does not exist or that no function is assigned, and grayed out items mean that the function is not implemented.

Table 2.32 Comparison of Multiplexed Pin Assignments

Module/ Function	Pin Function	Port Allocation	RX23T (MPC) 64-Pin	RX66T (MPC) 64-Pin
Interrupt	NMI (input)	PE2	○	○
	IRQ0 (input)	P10	○	×
		P93	○	×
		P52	×	○
	IRQ1-DS (input)	P11		○
	IRQ1 (input)	P11	○	×
		P94	○	×
		P53	×	○
	IRQ2 (input)	P00	○	○
		P22	○	×
		PB1	○	×
		PD4	○	○
		P54	×	○
		PB6	×	○
	IRQ3-DS (input)	PB4		○
	IRQ3 (input)	P24	○	×*1
		PB4	○	×*1
		PD5	○	×*1
	IRQ4-DS (input)	P96		○
	IRQ4 (input)	P01	○	○
		P23	○	×
		PA2	○	×
		PB1	×	○
	IRQ5-DS (input)	P70		○
	IRQ5 (input)	P02	○	×
		P70	○	×
		PB6	○	×
		PD6	○	○
	IRQ6-DS (input)	P21		○
	IRQ6 (input)	PD5		○
	IRQ7-DS (input)	P20		○
	IRQ8 (input)	P64		○
		PB0		○
		PD7		○
	IRQ9 (input)	P65		○
		PB3		○
	IRQ10 (input)	P22		○

Module/ Function	Pin Function	Port Allocation	RX23T (MPC) 64-Pin	RX66T (MPC) 64-Pin
Multi-function timer unit 3	MTIOC0A (input/output)/ MTIOC0A# (input/output)	P31	○	×
		PB3	○	○
	MTIOC0B (input/output)/ MTIOC0B# (input/output)	P30	○	×
		P93	○	×
		PB2	○	○
	MTIOC0C (input/output)/ MTIOC0C# (input/output)	P94	○	×
		PB1	○	○
	MTIOC0D (input/output)/ MTIOC0D# (input/output)	PB0	○	○
	MTIOC1A (input/output)/ MTIOC1A# (input/output)	PA5	○	×*1
	MTIOC1B (input/output)/ MTIOC1B# (input/output)	PA4	○	×*1
	MTIOC2A (input/output)/ MTIOC2A# (input/output)	PA3	○	×*1
	MTIOC2B (input/output)/ MTIOC2B# (input/output)	PA2	○	×*1
	MTIOC3A (input/output)/ MTIOC3A# (input/output)	P11	○	○
		P33	○	×
	MTIOC3B (input/output)/ MTIOC3B# (input/output)	P71	○	○
	MTIOC3C (input/output)/ MTIOC3C# (input/output)	P32	○	×*1
	MTIOC3D (input/output)/ MTIOC3D# (input/output)	P74	○	○
	MTIOC4A (input/output)/ MTIOC4A# (input/output)	P72	○	○
	MTIOC4B (input/output)/ MTIOC4B# (input/output)	P73	○	○
	MTIOC4C (input/output)/ MTIOC4C# (input/output)	P75	○	○
	MTIOC4D (input/output)/ MTIOC4D# (input/output)	P76	○	○
	MTIC5U (input)/ MTIC5U# (input/output)	P24	○	×*1
	MTIC5V (input)/ MTIC5V# (input/output)	P23	○	×*1
	MTIC5W (input)/ MTIC5W# (input)	P22	○	○
	MTIOC6B (input/output)/ MTIOC6B# (input/output)	P95		○
	MTIOC6D (input/output)/ MTIOC6D# (input/output)	P92		○
	MTIOC7A (input/output)/ MTIOC7A# (input/output)	P94		○
	MTIOC7B (input/output)/ MTIOC7B# (input/output)	P93		○
	MTIOC7C (input/output)/ MTIOC7C# (input/output)	P91		○
	MTIOC7D (input/output)/ MTIOC7D# (input/output)	P90		○

Module/ Function	Pin Function	Port Allocation	RX23T (MPC) 64-Pin	RX66T (MPC) 64-Pin
Multi-function timer unit 3	MTIOC9A (input/output)/ MTIOC9A# (input/output)	P00		○
		P21		○
		PD7		○
	MTIOC9B (input/output)	P22		○
	MTIOC9C (input/output)/ MTIOC9C# (input/output)	P01		○
		PD6		○
	MTIOC9D (input/output)	P11		○
	MTCLKA (input)/ MTCLKA# (input)	P33	○	×
		P21	×	○
	MTCLKB (input)/ MTCLKB# (input)	P32	○	×
		P20	×	○
	MTCLKC (input)/ MTCLKC# (input)	P11	○	○
		P31	○	×
	MTCLKD (input)/ MTCLKD# (input)	P10	○	×
		P30	○	×
		P22	×	○
	ADSM0 (output)	PB2	○	○
	ADSM1 (output)	PB1		○
8-bit timer	TMO0 (output)	PD3	○	○
		PB0	×	○
	TMCI0 (input)	PD4	○	○
		PB1	×	○
	TMRI0 (input)	PD5	○	○
		PB2	×	○
	TMO1 (output)	P94	○	×
		PD6	○	○
	TMCI1 (input)	P92	○	×*1
	TMRI1 (input)	P93	○	×
		PD7	○	○
	TMO2 (output)	P23	○	×*1
	TMCI2 (input)	P24	○	×*1
	TMRI2 (input)	P22	○	○
	TMO3 (output)	P11	○	○
	TMCI3 (input)	PA5	○	×*1
	TMRI3 (input)	P10	○	×*1
	TMO4 (output)	P22		○
	TMCI4 (input)	P21		○
	TMRI4 (input)	P20		○
	TMRI5 (input)	PD7		○
	TMCI6 (input)	PD4		○
	TMRI6 (input)	PD5		○
Port output enable 3	POE0# (input)	P70	○	○
	POE4# (input)	P96		○
	POE8# (input)	PB4	○	○
	POE9# (input)	P11		○
	POE10# (input)	PE2	○	○

Module/ Function	Pin Function	Port Allocation	RX23T (MPC) 64-Pin	RX66T (MPC) 64-Pin
Serial communications interface	RXD1 (input)/ SMISO1 (input/output)/ SSCL1 (input/output)	PD5	○	○
	TXD1 (output)/ SMOSI1 (input/output)/ SSDA1 (input/output)	PD3	○	○
	SCK1 (input/output)	PD4	○	○
	CTS1# (input)/ RTS1# (output)/ SS1# (input)	P02	○	×
		PD6	○	○
	RXD5 (input)/ SMISO5 (input/output)/ SSCL5 (input/output)	PB1	○	×
		PB6	○	○
	TXD5 (output)/ SMOSI5 (input/output)/ SSDA5 (input/output)	PB2	○	×
		PB5	○	○
		PD7	×	○
	SCK5 (input/output)	P93	○	×*1
		PB3	○	×*1
		PB7	○	×*1
	CTS5# (input)/ RTS5# (output)/ SS5# (input)	PA2	○	×
		PB4	×	○
	RXD6 (input)/ SMISO6 (input/output)/ SSCL6 (input/output)	PB1		○
	TXD6 (output)/ SMOSI6 (input/output)/ SSDA6 (input/output)	PB0		○
		PB2		○
	SCK6 (input/output)	PB3		○
	RXD8 (input)/ SMISO8 (input/output)/ SSCL8 (input/output)	P22		○
	TXD8 (output)/ SMOSI8 (input/output)/ SSDA8 (input/output)	P21		○
	SCK8 (input/output)	P20		○
	CTS8# (input)/ RTS8# (output)/ SS8# (input)	P20		○
	RXD9 (input)/ SMISO9 (input/output)/ SSCL9 (input/output)	P00		○
	TXD9 (output)/ SMOSI9 (input/output)/ SSDA9 (input/output)	P01		○
	CTS9# (input)/ RTS9# (output)/ SS9# (input)	P70		○
	RXD11 (input)/ SMISO11 (input/output)/ SSCL11 (input/output)	PB6		○
		PD5		○

Module/ Function	Pin Function	Port Allocation	RX23T (MPC) 64-Pin	RX66T (MPC) 64-Pin
Serial communications interface	TXD11 (output)/ SMOSI11 (input/output)/ SSDA11 (input/output)	PB5		○
		PD3		○
	SCK11 (input/output)	PB4		○
		PD4		○
	RXD12 (input)/ SMISO12 (input/output)/ SSCL12 (input/output)/ RXDX12 (input)	P00		○
		P22		○
		PB6		○
	TXD12 (output)/ SMOSI12 (input/output)/ SSDA12 (input/output)/ TXDX12 (output)/ SIOX12 (input/output)	P01		○
		P21		○
		PB5		○
I^{2}C bus interface	SCL0 (input/output)	PB1	○	○
	SDA0 (input/output)	PB2	○	○
Serial peripheral interface	RSPCKA (input/output)	P24	○	×
		P93	○	×
		PA4	○	×
		PB3	○	○
		P20	×	○
	MOSIA (input/output)	P23	○	×
		PB0	○	○
		P21	×	○
	MISOA (input/output)	P22	○	○
		P94	○	×
		PA5	○	×
	SSLA0 (input/output)	P30	○	×
		PA3	○	×
		PD6	○	○
	SSLA1 (output)	P31	○	×
		PA2	○	×
		PD7	○	○
	SSLA2 (output)	P32	○	×*1
		P92	○	×*1
	SSLA3 (output)	P33	○	×*1
		P91	○	×*1
12-bit A/D converter	AN000 (input)*2	P40	○	○
	AN001 (input)*2	P41	○	○
	AN002 (input)*2	P42	○	○
	AN003 (input)	P43	○	×*1
	AN004 (input)	P44	○	×*1
	AN005 (input)	P45	○	×*1
	AN006 (input)	P46	○	×*1
	AN007 (input)*2	P47	○	×
		PH0	×	○
	AN016 (input)	P11	○	
	AN017 (input)	P10	○	

Module/ Function	Pin Function	Port Allocation	RX23T (MPC) 64-Pin	RX66T (MPC) 64-Pin
12-bit A/D converter	ADTRG0# (input)	PA4	○	×
		P20	×	○
	ADST0 (output)	P02	○	×
		PD6	○	○
	PGAVSS0 (input)*2	PH0		○
	AN100 (input)*2	P44		○
	AN101 (input)*2	P45		○
	AN102 (input)*2	P46		○
	AN107 (input)*2	PH4		○
	ADTRG1# (input)	P21		○
	ADST1 (output)	P00		○
	PGAVSS1 (input)*2	PH4		○
	AN200 (input)*2	P52		○
	AN201 (input)*2	P53		○
	AN202 (input)*2	P54		○
	AN210 (input)*2	P64		○
	AN211 (input)*2	P65		○
	AN216 (input)*2	P20		○
	AN217 (input)*2	P21		○
	ADTRG2# (input)	P22		○
		PB0		○
	ADST2 (output)	P01		○
Clock frequency accuracy measurement circuit	CACREF (input)	P01	○	×
		P23	○	×
		PB3	○	○
		P00	×	○
Comparator	CMPC00 (input)*2	P40	○	○
	CMPC01 (input)*2	P43	○	×
		P40	×	○
	CMPC02 (input)*2	P46	○	×
		P52	×	○
	CMPC10 (input)*2	P41	○	○
	CMPC11 (input)*2	P44	○	×
		P41	×	○
	CMPC12 (input)*2	P47	○	×
		P53	×	○
	CMPC20 (input)*2	P42	○	○
	CMPC21 (input*2	P45	○	×
		P42	×	○
	CMPC22 (input)*2	P47	○	×
		P54	×	○
	CMPC30 (input)*2	P44		○
	CMPC31 (input)*2	P44		○
	CMPC33 (input)*2	P64		○
	CMPC40 (input)*2	P45		○
	CMPC41 (input)*2	P45		○
	CMPC50 (input)*2	P46		○
	CMPC51 (input)*2	P46		○
	CMPC53 (input)*2	P65		○

Module/ Function	Pin Function	Port Allocation	RX23T (MPC) 64-Pin	RX66T (MPC) 64-Pin
Comparator	COMP0 (output)	P24	○	×
		P00	×	○
	COMP1 (output)	P23	○	×
		P01	×	○
	COMP2 (output)	P22	○	○
	COMP4 (output)	P20		○
	COMP5 (output)	P21		○
	CVREFC0 (input)*2	P11	○	×*1
	CVREFC1 (input)*2	P10	○	×*1
General PWM timer	GTIOC0A (input/output)/ GTIOC0A# (input/output)	P71		○
		PD7		○
	GTIOC0B (input/output)/ GTIOC0B# (input/output)	P74		○
		PD6		○
	GTIOC1A (input/output)/ GTIOC1A# (input/output)	P72		○
		PD5		○
	GTIOC1B (input/output)/ GTIOC1B# (input/output)	P75		○
		PD4		○
	GTIOC2B (input/output)/ GTIOC2B# (input/output)	PD7		○
	GTIOC3B (input/output)/ GTIOC3B# (input/output)	P11		○
		PD6		○
	GTIOC4A (input/output)/ GTIOC4A# (input/output)	P71		○
		P95		○
	GTIOC4B (input/output)/ GTIOC4B# (input/output)	P74		○
		P92		○
	GTIOC5A (input/output)/ GTIOC5A# (input/output)	P72		○
		P94		○
	GTIOC5B (input/output)/ GTIOC5B# (input/output)	P75		○
		P91		○
	GTIOC6A (input/output)/ GTIOC6A# (input/output)	P73		○
		P93		○
	GTIOC6B (input/output)/ GTIOC6B# (input/output)	P76		○
		P90		○
	GTIOC7A (input/output)/ GTIOC7A# (input/output)	P95		○
	GTIOC7B (input/output)/ GTIOC7B# (input/output)	P92		○
	GTIOC8A (input/output)/ GTIOC8A# (input/output)	P94		○
	GTIOC8B (input/output)/ GTIOC8B# (input/output)	P91		○
	GTIOC9A (input/output)/ GTIOC9A# (input/output)	P93		○
	GTIOC9B (input/output)/ GTIOC9B# (input/output)	P90		○

Module/ Function	Pin Function	Port Allocation	RX23T (MPC) 64-Pin	RX66T (MPC) 64-Pin
General PWM timer	GTETRGA (input)	P01		○
		P11		○
		P70		○
		P96		○
		PB4		○
		PD5		○
	GTETRGB (input)	P01		○
		P70		○
		P96		○
		PB4		○
		PD4		○
	GTETRGC (input)	P01		○
		P11		○
		P70		○
		P96		○
		PB4		○
		PD3		○
	GTETRGD (input)	P01		○
		P70		○
		P96		○
		PB4		○
	GTADSM0 (output)	PB2		○
	GTADSM1 (output)	PB1		○
CAN module	CTX0 (output)	PB5		○
		PD7		○
	CRX0 (input)	P22		○
		PB6		○
12-bit D/A converter	DA0 (output)*2	P64		○
	DA1 (output)*2	P65		○

Notes: 1. RX66T Group products with a 64-bit package do not have this function.
2. To use these pins on the RX66T Group, set each respective pin to general-purpose input (PORTm.PDR.Bn and PORTm.PMR.Bn bits cleared to 0).

Table 2.33 Comparison of P0n Pin Function Control Register (P0nPFS)

Register	Bit	RX23T (n = 0 to 2)	RX66T (n = 0, 1)
P00PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00111b: CACREF	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9A 000011b: MTIOC9A# 000111b: CACREF 001001b: ADST1 001010b: RXD9/SMISO9/SSCL9 001100b: RXD12/SMISO12/ SSCL12/RXDX12 011110b: COMP0
P01PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 01001b: ADST0 01010b: CTS1#/RTS1#/SS1#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9C 000011b: MTIOC9C# 000111b: POE12# 001001b: ADST2 001010b: TXD9/SMOSI9/SSDA9 001100b: TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD 011110b: COMP1
P02PFS	—	P02 pin function select register	—
P0nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P00: IRQ2 (64-pin) P01: IRQ4 (64-pin) P02: IRQ5 (64/52-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P00: IRQ2 (64/80/100/112/144-pin) P01: IRQ4 (64/80/100/112/144-pin)

Table 2.34 Comparison of P1n Pin Function Control Register (P1nPFS)

Register	Bit	RX23T (n = 0, 1)	RX66T (n = 0 to 7)
P10PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00010b: MTCLKD 00101b: TMRI3	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9B 000010b: MTCLKD 000011b: MTIOC9B# 000100b: MTCLKD# 000101b: TMRI3 000111b: POE12# 001010b: CTS6#/RTS6#/SS6# 010101b: GTETRGB 010111b: GTETRGD
P11PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKC 00101b: TMO3	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKC 000011b: MTIOC3A# 000100b: MTCLKC# 000101b: TMO3 000111b: POE9# 001000b: MTIOC9D 010100b: GTIOC3B 010101b: GTETRGA 010110b: GTIOC3B# 010111b: GTETRGC
P12PFS	—	—	P12 pin function select register
P13PFS	—	—	P13 pin function select register
P14PFS	—	—	P14 pin function select register
P15PFS	—	—	P15 pin function select register
P16PFS	—	—	P16 pin function select register
P17PFS	—	—	P17 pin function select register
P1nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P10: IRQ0 (64/52/48-pin) P11: IRQ1 (64/52/48-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P10: IRQ0-DS (80/100/112/144-pin) P11: IRQ1-DS (64/80/100/112/144-pin) P12: IRQ9 (112/144-pin) P13: IRQ10 (112/144-pin) P14: IRQ11 (112/144-pin) P15: IRQ12 (112/144-pin) P16: IRQ13 (112/144-pin) P17: IRQ14 (112/144-pin)
	ASEL	Analog input function select bit	—

Table 2.35 Comparison of P2n Pin Function Control Register (P2nPFS)

Register	Bit	RX23T (n = 2 to 4)	RX66T (n = 0 to 7)
P20PFS	—	—	P20 pin function control register
P21PFS	—	—	P21 pin function control register
P22PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5W 00101b: TMRI2 01101b: MISOA 11110b: COMP2	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIC5W 000010b: MTCLKD 000011b: MTIC5W# 000100b: MTCLKD# 000101b: TMRI2 000110b: TMO4 001000b: MTIOC9B 001001b: ADTRG2# 001010b: RXD8/SMISO8/SSCL8 001100b: RXD12/SMISO12/ SSCL12/RXDX12 001101b: MISOA 010000b: CRX0 011110b: COMP2
P23PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5V 00101b: TMO2 00111b: CACREF 01101b: MOSIA 11110b: COMP1	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIC5V 000011b: MTIC5V# 000101b: TMO2 000111b: CACREF 001010b: TXD8/SMOSI8/SSDA8 001100b: TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12 001101b: MOSIA 010000b: CTX0 011110b: COMP1
P24PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5U 00101b: TMCI2 01101b: RSPCKA 11110b: COMP0	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIC5U 000011b: MTIC5U# 000101b: TMCI2 000110b: TMO6 001010b: CTS8#/RTS8#/SS8# 001011b: SCK8 001101b: RSPCKA 011110b: COMP0
P25PFS	—	—	P25 pin function control register
P26PFS	—	—	P26 pin function control register
P27PFS	—	—	P27 pin function control register

Register	Bit	RX23T (n = 2 to 4)	RX66T (n = 0 to 7)
P2nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P22: IRQ2 (64/52/48-pin) P23: IRQ4 (64/52/48-pin) P24: IRQ3 (64/52/48-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P20: IRQ7-DS (64/80/100/112/144-pin) P21: IRQ6-DS (64/80/100/112/144-pin) P22: IRQ10 (64/80/100/112/144-pin) P23: IRQ11 (100/112/144-pin) P24: IRQ4 (100/112/144-pin) P25: IRQ10 (144-pin) P26: IRQ11 (144-pin) P27: IRQ15 (80/100*[1]/112/144-pin)
	ASEL	—	Analog input function select bit

Note: 1. Only applies to products with PGA pseudo-differential input.

Table 2.36 Comparison of P3n Pin Function Control Register (P3nPFS)

Register	Bit	RX23T (n = 0 to 3)	RX66T (n = 0 to 5)
P30PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKD 01101b: SSLA0	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKD 000011b: MTIOC0B# 000100b: MTCLKD# 000101b: TMCI6 001010b: SCK8 001011b: CTS8#/RTS8#/SS8# 001101b: SSLA0 011110b: COMP3
P31PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0A 00010b: MTCLKC 01101b: SSLA1	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0A 000010b: MTCLKC 000011b: MTIOC0A# 000100b: MTCLKC# 000101b: TMRI6 001101b: SSLA1
P32PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTCLKB 01101b: SSLA2	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTCLKB 000011b: MTIOC3C# 000100b: MTCLKB# 000101b: TMO6 001101b: SSLA2 010100b: GTIOC3A 010110b: GTIOC3A#
P33PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKA 01101b: SSLA3	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKA 000011b: MTIOC3A# 000100b: MTCLKA# 000101b: TMO0 001101b: SSLA3 010100b: GTIOC3B 010110b: GTIOC3B#
P34PFS	—	—	P34 pin function control register
P35PFS	—	—	P35 pin function control register
P3nPFS	ISEL	—	Interrupt input function select bit

Table 2.37 Comparison of P4n Pin Function Control Register (P4nPFS)

Register	Bit	RX23T (n = 0 to 7)	RX66T (n = 0 to 7)
P4nPFS	ASEL	0: Used as other than as analog pin 1: Used as analog pin P40: AN000 (64/52/48-pin) P41: AN001 (64/52/48-pin) P42: AN002 (64/52/48-pin) P43: AN003 (64/52/48-pin) P44: AN004 (64/52/48-pin) P45: AN005 (64/52/48-pin) P46: AN006 (64/52/48-pin) P47: AN007 (64/52/48-pin)	0: Used as other than as analog pin 1: Used as analog pin P40: AN000, CMPC00, CMPC01 (64/80/100/112/144-pin) P41: AN001, CMPC10, CMPC11 (64/80/100/112/144-pin) P42: AN002, CMPC20, CMPC21 (64/80/100/112/144-pin) P43: AN003 (80/100/112/144-pin) P44: AN100, CMPC30, CMPC31 (64/80/100/112/144-pin) P45: AN101, CMPC40, CMPC41 (64/80/100/112/144-pin) P46: AN102, CMPC50, CMPC51 (64/80/100/112/144-pin) P47: AN103 (80/100/112/144-pin)

Table 2.38 Comparison of P5n Pin Function Control Register (P5nPFS)

Register	Bit	RX23T	RX66T
P5nPFS	—	—	P5n pin function control register (n = 0 to 5)

Table 2.39 Comparison of P6n Pin Function Control Register (P6nPFS)

Register	Bit	RX23T	RX66T
P6nPFS	—	—	P6n pin function control register (n = 0 to 5)

Table 2.40 Comparison of P7n Pin Function Control Register (P7nPFS)

Register	Bit	RX23T (n = 0 to 6)	RX66T (n = 0 to 6)
P70PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00111b: POE0#	Pin function select bits b5 b0 000000b: Hi-Z 000111b: POE0# 001010b: CTS9#/RTS9#/SS9# 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD
P71PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3B	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3B 000011b: MTIOC3B# 010100b: GTIOC0A 010101b: GTIOC4A 010110b: GTIOC0A# 010111b: GTIOC4A#

Register	Bit	RX23T (n = 0 to 6)	RX66T (n = 0 to 6)
P72PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4A	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4A 000011b: MTIOC4A# 010100b: GTIOC1A 010101b: GTIOC5A 010110b: GTIOC1A# 010111b: GTIOC5A#
P73PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4B	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4B 000011b: MTIOC4B# 010100b: GTIOC2A 010101b: GTIOC6A 010110b: GTIOC2A# 010111b: GTIOC6A#
P74PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3D	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3D 000011b: MTIOC3D# 010100b: GTIOC0B 010101b: GTIOC4B 010110b: GTIOC0B# 010111b: GTIOC4B#
P75PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4C	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4C 000011b: MTIOC4C# 010100b: GTIOC1B 010101b: GTIOC5B 010110b: GTIOC1B# 010111b: GTIOC5B#
P76PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4D	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4D 000011b: MTIOC4D# 010100b: GTIOC2B 010101b: GTIOC6B 010110b: GTIOC2B# 010111b: GTIOC6B#

Register	Bit	RX23T (n = 0 to 6)	RX66T (n = 0 to 6)
P7nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P70: IRQ5 (64/52/48-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P70: IRQ5-DS (64/80/100/112/144-pin)

Table 2.41 Comparison of P8n Pin Function Control Register (P8nPFS)

Register	Bit	RX23T	RX66T
P8nPFS	—	—	P8n pin function control register (n = 0 to 2)

Table 2.42 Comparison of P9n Pin Function Control Register (P9nPFS)

Register	Bit	RX23T (n = 1 to 4)	RX66T (n = 0 to 6)
P90PFS	—	—	P90 pin function control register
P91PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 01101b: SSLA3	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC7C 000011b: MTIOC7C# 010100b: GTIOC5B 010101b: GTIOC8B 010110b: GTIOC5B# 010111b: GTIOC8B#
P92PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMCI1 01101b: SSLA2	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC6D 000011b: MTIOC6D# 010100b: GTIOC4B 010101b: GTIOC7B 010110b: GTIOC4B# 010111b: GTIOC7B#
P93PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0B 00101b: TMRI1 01010b: SCK5 01101b: RSPCKA	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC7B 000011b: MTIOC7B# 010100b: GTIOC6A 010101b: GTIOC9A 010110b: GTIOC6A# 010111b: GTIOC9A#

Register	Bit	RX23T (n = 1 to 4)	RX66T (n = 0 to 6)
P94PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0C 00101b: TMO1 01101b: MISOA	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC7A 000011b: MTIOC7A# 010100b: GTIOC5A 010101b: GTIOC8A 010110b: GTIOC5A# 010111b: GTIOC8A#
P95PFS	—	—	P95 pin function control register
P96PFS	—	—	P96 pin function control register
P9nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P93: IRQ0 (64/52/48-pin) P94: IRQ1 (64/52/48-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P96: IRQ4-DS (64/80/100/112/144-pin)

Table 2.43 Comparison of PAn Pin Function Control Register (PAnPFS)

Register	Bit	RX23T (n = 2 to 5)	RX66T (n = 0 to 7)
PA0PFS	—	—	PA0 pin function control register
PA1PFS	—	—	PA1 pin function control register
PA2PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC2B 01010b: CTS5#/RTS5#/SS5# 01101b: SSLA1	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC2B 000011b: MTIOC2B# 000101b: TMO7 001010b: CTS6#/RTS6#/SS6# 001011b: RXD9/SMISO9/SSCL9 001100b: SCK11 001101b: SSLA1 010100b: GTADSM1
PA3PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC2A 01101b: SSLA0	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC2A 000011b: MTIOC2A# 000101b: TMRI7 001010b: TXD9/SMOSI9/SSDA9 001011b: SCK8 001101b: SSLA0 010100b: GTADSM0

Register	Bit	RX23T (n = 2 to 5)	RX66T (n = 0 to 7)
PA4PFS	PSEL[4:0] (RX23T) PSEL[5:0] RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC1B 01001b: ADTRG0# 01101b: RSPCKA	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC1B 000011b: MTIOC1B# 000101b: TMCI7 001001b: ADTRG0# 001010b: SCK6 001011b: TXD8/SMOSI8/SSDA8 001101b: RSPCKA
PA5PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC1A 00101b: TMCI3 01101b: MISOA	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC1A 000011b: MTIOC1A# 000101b: TMCI3 001001b: ADTRG1# 001010b: RXD6/SMISO6/SSCL6 001011b: RXD8/SMISO8/SSCL8 001101b: MISOA
PA6PFS	—	—	PA6 pin function control register
PA7PFS	—	—	PA7 pin function control register
PAnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA2: IRQ4 (64/52/48-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA1: IRQ14-DS (100/112/144-pin) PA5: IRQ1 (80/100/112/144-pin) PA6: IRQ7 (144-pin)

Table 2.44 Comparison of PBn Pin Function Control Register (PBnPFS)

Register	Bit	RX23T (n = 0 to 7)	RX66T (n = 0 to 7)
PB0PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0D 01101b: MOSIA	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0D 000011b: MTIOC0D# 000101b: TMO0 001001b: ADTRG2# 001010b: TXD6/SMOSI6/SSDA6 001011b: CTS11#/RTS11#/SS11# 001101b: MOSIA

Register	Bit	RX23T (n = 0 to 7)	RX66T (n = 0 to 7)
PB1PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0C 01010b: RXD5/SMISO5/SSCL5 01111b: SDA0	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0C 000011b: MTIOC0C# 000101b: TMCI0 001001b: ADSM1 001010b: RXD6/SMISO6/SSCL6 001111b: SCL0 010100b: GTADSM1
PB2PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0B 01001b: ADSM0 01010b: TXD5/SMOSI5/SSDA5 01111b: SDA0	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0B 000011b: MTIOC0B# 000101b: TMRI0 001001b: ADSM0 001010b: TXD6/SMOSI6/SSDA6 001111b: SDA0 010100b: GTADSM0
PB3PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0A 00111b: CACREF 01010b: SCK5 01101b: RSPCKA	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0A 000011b: MTIOC0A# 000111b: CACREF 001010b: SCK6 001101b: RSPCKA
PB4PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00111b: POE8#	Pin function select bits b5 b0 000000b: Hi-Z 000111b: POE8# 001010b: CTS5#/RTS5#/SS5# 001011b: SCK11 001100b: CTS11#/RTS11#/SS11# 010001b: USB0_OVRCURB 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD

Register	Bit	RX23T (n = 0 to 7)	RX66T (n = 0 to 7)
PB5PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 01010b: TXD5/SMOSI5/SSDA5	Pin function select bits b5 b0 000000b: Hi-Z 001010b: TXD5/SMOSI5/SSDA5 001011b: TXD11/SMOSI11/ SSDA11 001100b: TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12 010000b: CTX0 010001b: USB0_VBUSEN 010100b: GTIOC2B 010110b: GTIOC2B#
PB6PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 01010b: RXD5/SMISO5/SSCL5	Pin function select bits b5 b0 000000b: Hi-Z 001010b: RXD5/SMISO5/SSCL5 001011b: RXD11/SMISO11/ SSCL11 001100b: RXD12/SMISO12/ SSCL12/RXDX12 010000b: CRX0 010001b: USB0_OVRCURA 010100b: GTIOC2A 010110b: GTIOC2A#
PB7PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 01010b: SCK5	Pin function select bits b5 b0 000000b: Hi-Z 001010b: SCK5 001011b: SCK11 001100b: SCK12 010001b: USB0_OVRCURB 010100b: GTIOC1B 010110b: GTIOC1B#
PBnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB1: IRQ2 (64/52/48-pin) PB4: IRQ3 (64/52/48-pin) PB6: IRQ5 (64/52/48-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB0: IRQ8 (64/80/100/112/144-pin) PB1: IRQ4 (64/80/100/112/144-pin) PB3: IRQ9 (64/80/100/112/144-pin) PB4: IRQ3-DS (64/80/100/112/144-pin) PB6: IRQ2 (64/80/100/112/144-pin)

Table 2.45 Comparison of PCn Pin Function Control Register (PCnPFS)

Register	Bit	RX23T	RX66T
PCnPFS	—	—	PCn pin function control register (n = 0 to 6)

Table 2.46 Comparison of PDn Pin Function Control Register (PDnPFS)

Register	Bit	RX23T (n = 3 to 7)	RX66T (n = 0 to 7)
PD0PFS	—	—	PD0 pin function control register
PD1PFS	—	—	PD1 pin function control register
PD2PFS		—	PD2 pin function control register
PD3PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMO0 01010b: TXD1/SMOSI1/SSDA1	Pin function select bits b5 b0 000000b: Hi-Z 000101b: TMO0 001010b: TXD1/SMOSI1/SSDA1 001011b: TXD11/SMOSI11/ SSDA11 010100b: GTIOC2A 010101b: GTETRGC 010110b: GTIOC2A#
PD4PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMCI0 01010b: SCK1	Pin function select bits b5 b0 000000b: Hi-Z 000101b: TMCI0 000110b: TMCI6 001010b: SCK1 001011b: SCK11 010100b: GTIOC1B 010101b: GTETRGB 010110b: GTIOC1B#
PD5PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMRI0 01010b: RXD1/SMISO1/SSCL1	Pin function select bits b5 b0 000000b: Hi-Z 000101b: TMRI0 000110b: TMRI6 001010b: RXD1/SMISO1/SSCL1 001011b: RXD11/SMISO11/ SSCL11 010100b: GTIOC1A 010101b: GTETRGA 010110b: GTIOC1A#

Register	Bit	RX23T (n = 3 to 7)	RX66T (n = 0 to 7)
PD6PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMO1 01001b: ADST0 01010b: CTS1#/RTS1#/SS1# 01101b: SSLA0	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9C 000011b: MTIOC9C# 000101b: TMO1 001001b: ADST0 001010b: CTS1#/RTS1#/SS1# 001011b: CTS11#/RTS11#/SS11# 001101b: SSLA0 010100b: GTIOC0B 010101b: GTIOC3B 010110b: GTIOC0B# 010111b: GTIOC3B#
PD7PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMRI1 01101b: SSLA1	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9A 000011b: MTIOC9A# 000101b: TMRI1 000110b: TMRI5 001010b: TXD5/SMOSI5/SSDA5 001101b: SSLA1 010000b: CTX0 010100b: GTIOC0A 010101b: GTIOC3A 010110b: GTIOC0A# 010111b: GTIOC3A#
PDnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PD4: IRQ2 (64/52/48-pin) PD5: IRQ3 (64/52/48-pin) PD6: IRQ5 (64/52/48-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PD4: IRQ2 (64/80/100/112/144-pin) PD5: IRQ6 (64/80/100/112/144-pin) PD6: IRQ5 (64/80/100/112/144-pin) PD7: IRQ8 (64/80/100/112/144-pin)

Table 2.47 Comparison of PEn Pin Function Control Register (PEnPFS)

Register	Bit	RX23T (n = 2)	RX66T (n = 0 to 6)
PE0PFS	—	—	PE0 pin function control register
PE1PFS	—	—	PE1 pin function control register
PE2PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX66T)	Pin function select bits b4 b0 00000b: Hi-Z 00111b: POE10#	Pin function select bits b5 b0 000000b: Hi-Z 000111b: POE10#
PE3PFS	—	—	PE3 pin function control register
PE4PFS	—	—	PE4 pin function control register
PE5PFS	—	—	PE5 pin function control register
PE6PFS	—	—	PE6 pin function control register
PEnPFS	ISEL	—	Interrupt input function select bit

Table 2.48 Comparison of PFn Pin Function Control Register (PFnPFS)

Register	Bit	RX23T	RX66T
PFnPFS	—	—	PFn pin function control register (n = 0 to 3)

Table 2.49 Comparison of PGn Pin Function Control Register (PGnPFS)

Register	Bit	RX23T	RX66T
PGnPFS	—	—	PGn pin function control register (n = 0 to 2)

Table 2.50 Comparison of PHn Pin Function Control Register (PHnPFS)

Register	Bit	RX23T	RX66T
PHnPFS	—	—	PHn pin function control register (n = 0 to 7)

Table 2.51 Comparison of PKn Pin Function Control Register (PKnPFS)

Register	Bit	RX23T	RX66T
PKnPFS	—	—	PKn pin function control register (n = 0 to 2)

Table 2.52 Comparison of Multi-Function Pin Controller Registers

Register	Bit	RX23T (MPC)	RX66T (MPC)
PFCSE	—	—	CS output enable register
PFCSS0	—	—	CS output pin select register 0
PFAOE0	—	—	Address output enable register 0
PFAOE1	—	—	Address output enable register 1
PFBCR0	—	—	External bus control register 0
PFBCR1	—	—	External bus control register 1
PFBCR2	—	—	External bus control register 2
PFBCR3	—	—	External bus control register 3
PFBCR4	—	—	External bus control register 4

2.15 Multi-Function Timer Pulse Unit 3

Table 2.53 is a comparative overview of multi-function timer pulse unit 3, and Table 2.54 is a comparison of multi-function timer pulse unit 3 registers.

Table 2.53 Comparative Overview of Multi-Function Timer Pulse Unit 3

Item	RX23T (MTU3c)	RX66T (MTU3d)
Pulse input/output	Max. 16 lines	Max. 28 lines
Pulse input	3 lines	3 lines
Count clocks	11 clocks for each channel (14 clocks for MTU0, 12 clocks for MTU2, 10 clocks for MTU5, and four clocks for MTU1 and MTU2 (LWA = 1))	11 clocks for each channel (14 clocks for MTU0 and MTU9, 12 clocks for MTU2, 10 clocks for MTU5, and four clocks for MTU1 and MTU2 (LWA = 1))
Operating frequency	Up to 40 MHz	Up to 160 MHz
Available operations	[MTU0 to MTU4] • Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Simultaneous register input/output by synchronous counter operation • Up to 12-phase PWM output in combination with synchronous operation	[MTU0 to MTU4, MTU6, MTU7, MTU9] • Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Simultaneous register input/output by synchronous counter operation • Up to 14-phase PWM output in combination with synchronous operation
	[MTU0, MTU3, MTU4] Ability to specify buffer operation	[MTU0, MTU3, MTU4, MTU6, MTU7, MTU9] Ability to specify buffer operation
	[MTU1, MTU2] • Independent specification of phase counting mode • Ability to specify 32-bit phase counting mode for interlocked operation of MTU1 and MTU2 (when TMDR3.LWA = 1) • Cascade connection operation available	[MTU1, MTU2] • Independent specification of phase counting mode • Ability to specify 32-bit phase counting mode for interlocked operation of MTU1 and MTU2 (when TMDR3.LWA = 1) • Cascade connection operation available

Item	RX23T (MTU3c)	RX66T (MTU3d)
Available operations	[MTU3, MTU4] • Ability to output positive and negative signals in six phases in complementary PWM and reset PWM operation through interlocked operation of MTU3 and MTU4 • Ability to transfer values from buffer registers to temporary registers at peaks and troughs of the timer counter or at writes to the buffer registers (MTU4.TGRD) in complementary PWM mode • Ability to select double-buffering in complementary PWM mode	[MTU3, MTU4, MTU6, MTU7] • Ability to output positive and negative signals in six phases (12 phases total) in complementary PWM and reset-synchronized PWM operation through interlocked operation of MTU3 and MTU4 or MTU6 and MTU7. • Ability to transfer values from buffer registers to temporary registers at peaks and troughs of the timer counter or at writes to the buffer registers (MTU4.TGRD, MTU7.TGRD) in complementary PWM mode • Ability to select double-buffering in complementary PWM mode
	[MTU3, MTU4] Ability to select between two types of waveform output (chopping or level) by specifying a mode for driving AC synchronous motors (brushless DC motors) that uses complementary PWM output or reset PWM output and interlocking with MTU0	[MTU3, MTU4] Ability to select between two types of waveform output (chopping or level) by specifying a mode for driving AC synchronous motors (brushless DC motors) that uses complementary PWM output or reset PWM output and interlocking with MTU0
	[MTU5] Ability to use the MTU5 as a dead-time compensation counter	[MTU5] Ability to use the MTU5 as a dead-time compensation counter
	—	[MTU6, MTU7] Ability to select between two types of waveform output (chopping or level) by specifying a mode for driving AC synchronous motors (brushless DC motors) that uses complementary PWM output or reset PWM output and interlocking with MTU9
Interrupt skipping function	Ability to skip interrupts at counter peaks and troughs and A/D conversion start triggers in complementary PWM mode	Ability to skip interrupts at counter peaks and troughs and A/D conversion start triggers in complementary PWM mode
Interrupt sources	28 sources	45 sources
Buffer operation	Automatic transfer of register data (transfer from buffer register to timer register)	Automatic transfer of register data (transfer from buffer register to timer register)
Trigger generation	• Ability to generate A/D converter start trigger • Ability to start A/D conversion at any desired timing and in synchronization with PWM output using A/D conversion start request delaying function	• Ability to generate A/D converter start trigger • Ability to start A/D conversion at any desired timing and in synchronization with PWM output using A/D conversion start request delaying function
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Table 2.54 Comparison of Multi-Function Timer Pulse Unit 3 Registers

Register	Bit	RX23T (MTU3c)	RX66T (MTU3d)
TMDR2B	—	—	Timer mode register 2
TSYCR	—	—	Timer synchronous clear register
TSTRA	CST9	—	Counter start 9 bit
TSTRB	—	—	Timer start register
TSYRA	SYNC9	—	Timer synchronous operation 9 bit
TSYRB	—	—	Timer synchronous register
TCSYSTR	SCH7	—	Synchronous start 7 bit
	SCH6	—	Synchronous start 6 bit
	SCH9	—	Synchronous start 9 bit
TRWERB	—	—	Timer read/write enable register
TOERB	—	—	Timer output master enable register
TOCR1B	—	—	Timer output control register 1
TOCR2B	—	—	Timer output control register 2
TGCRB	—	—	Timer gate control register
TCNTSB	—	—	Timer subcounter
TCDRB	—	—	Timer period data register
TCBRB	—	—	Timer period buffer register
TDDRB	—	—	Timer dead time data register
TDERB	—	—	Timer dead time enable register
TBTERB	—	—	Timer buffer transfer set register
TWCRB	—	—	Timer waveform control register
NFCRn	—	Noise filter control register n (n = 0 to 4, C)	Noise filter control register n (n = 0 to 4, 6, 7, 9, and C)
TITMRB	—	—	Timer interrupt skipping mode register
TITCR1B	—	—	Timer interrupt skipping set register 1
TITCNT1B	—	—	Timer interrupt skipping counter 1
TITCR2B	—	—	Timer interrupt skipping set register 2
TITCNT2B	—	—	Timer interrupt skipping counter 2

Register	Bit	RX23T (MTU3c)	RX66T (MTU3d)
TADSTRGR0	TADSTRS0 [4:0]	A/D conversion start request select bits for ADSM0 pin output frame synchronization signal generation b4 b0 0 0 0 0 0: Source not selected. 0 0 0 0 1: TRGA0N 0 0 0 1 0: TRGA1N 0 0 0 1 1: TRGA2N 0 0 1 0 0: TRGA3N 0 0 1 0 1: TRGA4N 0 1 0 0 0: TRG0N 0 1 0 0 1: TRG4AN 0 1 0 1 0: TRG4BN 0 1 0 1 1: TRG4AN or TRG4BN 0 1 1 0 0: TRG4ABN	A/D conversion start request select bits for ADSM0 pin output frame synchronization signal generation b4 b0 0 0 0 0 0: Source not selected. 0 0 0 0 1: TRGA0N 0 0 0 1 0: TRGA1N 0 0 0 1 1: TRGA2N 0 0 1 0 0: TRGA3N 0 0 1 0 1: TRGA4N 0 0 1 1 0: TRGA6N 0 0 1 1 1: TRGA7N 0 1 0 0 0: TRG0N 0 1 0 0 1: TRG4AN 0 1 0 1 0: TRG4BN 0 1 1 0 0: TRG4ABN 0 1 1 0 1: TRG7AN 0 1 1 1 0: TRG7BN 1 0 0 0 0: TRG7ABN 1 0 0 0 1: TRGA9N 1 0 0 1 0: TRG9N 1 0 0 1 1: TRG9AEN 1 0 1 0 0: TRG0AEN 1 0 1 0 1: TRGA09N 1 0 1 1 0: TRG09N
	TADSMEN0	—	ADSM0 pin output enable bit
TADSTRGR1	—	—	A/D conversion start request select register 1

2.16 Port Output Enable 3

Table 2.55 is a comparative overview of port output enable 3, and Table 2.56 is a comparison of port output enable 3 registers.

Table 2.55 Comparative Overview of Port Output Enable 3

Item	RX23T (POE3b)	RX66T (POE3B)
Pin status while output is disabled	• High-impedance	• High-impedance • General I/O ports
Output disable control target pins	• MTU output pins — MTU0 pin (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) — MTU3 pin (MTIOC3B, MTIOC3D) — MTU4 pin (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D)	• MTU output pins — MTU0 pin (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) — MTU3 pin (MTIOC3B, MTIOC3D) — MTU4 pin (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) — MTU6 pin (MTIOC6B, MTIOC6D) — MTU7 pin (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D) — MTU9 pin (MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D) • GPTW output pins — GPTW0 pin (GTIOC0A, GTIOC0B) — GPTW1 pin (GTIOC1A, GTIOC1B) — GPTW2 pin (GTIOC2A, GTIOC2B) — GPTW3 pin (GTIOC3A, GTIOC3B) — GPTW4 pin (GTIOC4A, GTIOC4B) — GPTW5 pin (GTIOC5A, GTIOC5B) — GPTW6 pin (GTIOC6A, GTIOC6B) — GPTW7 pin (GTIOC7A, GTIOC7B) — GPTW8 pin (GTIOC8A, GTIOC8B) — GPTW9 pin (GTIOC9A, GTIOC9B)

Item	RX23T (POE3b)	RX66T (POE3B)
Conditions for generating output disable request	• Input pin change: Input received on POE0#, POE8#, or POE10# pin • Short circuit between output pins: A match (short circuit) between the output signal levels (active level) over one or more cycles on any of the following combinations of pins [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D • Register setting • Detection of oscillation stop by clock oscillator • Detection of output from comparator (CMPC)	• Input pin change: Detection of signal input on POE0#, POE4#, POE8#, POE9#, POE10#, POE11#, POE12#, POE13#, or POE14# • Short circuit between output pins: A match (short circuit) between the output signal levels (active level) over one or more cycles on any of the following combinations of pins [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D — MTIOC6B and MTIOC6D — MTIOC7A and MTIOC7C — MTIOC7B and MTIOC7D [GPTWPWM output pins] — GTIOC0A and GTIOC0B — GTIOC1A and GTIOC1B — GTIOC2A and GTIOC2B — GTIOC4A and GTIOC4B — GTIOC5A and GTIOC5B — GTIOC6A and GTIOC6B — GTIOC7A and GTIOC7B — GTIOC8A and GTIOC8B — GTIOC9A and GTIOC9B • SPOER register setting • Detection of oscillation stop by main clock oscillator • Detection of output from comparator C (CMPC)
Functions	• The POE0#, POE8#, and POE10# input pins can each be set for falling-edge, PCLK/8 × 16, PCLK/16 × 16, or PCLK/128 × 16 low-level sampling. • MTU complementary PWM output pins and MTU0 pins can be placed in the high-impedance state by falling-edge or low-level sampling on the POE0#, POE8#, or POE10# pin.	• The POE0#, POE4#, POE8#, POE9#, POE10#, POE11#, POE12#, POE13#, and POE14# pins can each be set for falling-edge or low-level detection. When using low-level detection, PCLK/1, PCLK/2, PCLK/4, PCLK/8, PCLK/16, or PCLK/128 can be selected as the a sampling clock, and the number of samples can be selected from four, eight, or 16. • The outputs of all target pins can be disabled by detecting falling-edge or low-level input on the POE0#, POE4#, POE8#, POE9#, POE10#, POE11#, POE12#, POE13#, or POE14# pin.

Item	RX23T (POE3b)	RX66T (POE3B)
Functions	• MTU complementary PWM output pins and MTU0 pins can be placed in the high-impedance state when oscillation stop is detected by the oscillation stop detection function of the clock generator.	• The outputs of all target pins can be disabled when oscillation stop is detected by the oscillation stop detection function of the clock generator.
	• MTU complementary PWM output pins can be placed in the high-impedance state when output levels of MTU complementary PWM output pins are compared and simultaneous active-level output continues for one cycle or more.	• Output on the MTU complementary PWM output pins can be disabled when output levels of MTU complementary PWM output pins are compared and simultaneous active-level output continues for one cycle or more.
		• The output on the GPTW output pins can be disabled when output levels of the GPTW output pins (GPTW0 to GPTW2, GPTW4 to GPTW6, and GPTW7 to GPTW9 pins) are compared and simultaneous active-level output continues for one cycle or more.
	• MTU complementary PWM output pins and MTU0 pins can be placed in the high-impedance state in response to comparator detection by the comparator (CMPC).	• The outputs of all target pins can be disabled in response to comparator C (CMPC) output detection.
	• MTU complementary PWM output pins and MTU0 pins can be placed in the high-impedance state by modifying the settings of the POE registers.	• The outputs of all target pins can be disabled by modifying the settings of the POE registers.
	• Interrupts can be generated by input-level sampling or output-level comparison results.	• Interrupts can be generated by input-level sampling or output-level comparison results.

Table 2.56 Comparison of Port Output Enable 3 Registers

Register	Bit	RX23T (POE3b)	RX66T (POE3B)
ICSR1	POE0M[1:0] (RX23T) POE0M[3:0] (RX66T)	POE0 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE0# pin input. 0 1: Accepts a request when POE0# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE0# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE0# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	POE0 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge of POE0# pin input. 0 0 0 1: Samples the level of the POE0# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 0: Samples the level of the POE0# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 1: Samples the level of the POE0# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 0: Samples the level of the POE0# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 1: Samples the level of the POE0# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 1 0: Samples the level of the POE0# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified times. Settings other than the above are prohibited.
	POE0M2[3:0]	—	POE0 sampling count select bits
ICSR2	—	—	Input level control/status register 2

Register	Bit	RX23T (POE3b)	RX66T (POE3B)
ICSR3	POE8M[1:0] (RX23T) POE8M[3:0] (RX66T)	POE8 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE8# pin input. 0 1: Accepts a request when POE8# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE8# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE8# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	POE8 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge of POE8# pin input. 0 0 0 1: Samples the level of the POE8# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 0: Samples the level of the POE8# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 1: Samples the level of the POE8# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 0: Samples the level of the POE8# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 1: Samples the level of the POE8# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 1 0: Samples the level of the POE8# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified times. Settings other than the above are prohibited.
	POE8M2[3:0]	—	POE8 sampling count select bits

Register	Bit	RX23T (POE3b)	RX66T (POE3B)
ICSR4	POE10M[1:0] (RX23T) POE10M[3:0] (RX66T)	POE10 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE10# pin input. 0 1: Accepts a request when POE10# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE10# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE10# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	POE10 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge of POE10# pin input. 0 0 0 1: Samples the level of the POE10# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 0: Samples the level of the POE10# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 1: Samples the level of the POE10# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 0: Samples the level of the POE10# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 1: Samples the level of the POE10# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 1 0: Samples the level of the POE10# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified times. Settings other than the above are prohibited.
	POE10M2[3:0]	—	POE10 sampling count select bits
ICSR5	—	—	Input level control/status register 5

Register	Bit	RX23T (POE3b)	RX66T (POE3B)
ICSR7	—	—	Input level control/status register 7
ICSR8	—	—	Input level control/status register 8
ICSR9	—	—	Input level control/status register 9
ICSR10	—	—	Input level control/status register 10
OCSR2	—	—	Output level control/status register 2
OCSR3	—	—	Output level control/status register 3
OCSR4	—	—	Output level control/status register 4
OCSR5	—	—	Output level control/status register 5
ALR2	—	—	Active level setting register 2
ALR3	—	—	Active level setting register 3
ALR4	—	—	Active level setting register 4
ALR5	—	—	Active level setting register 5
SPOER	MTUCH67HIZ	—	MTU6 and MTU7 pin output disable bit
	GPT01HIZ	—	GPTW0 and GPTW1 pin output disable bit
	GPT23HIZ	—	GPTW2 and GPTW3 pin output disable bit
	MTUCH9HIZ	—	MTU9 pin output disable bit
	GPT02HIZ	—	GPTW0 to GPTW2 pin output disable bit
	GPT46HIZ	—	GPTW4 to GPTW6 pin output disable bit
	GPT79HIZ	—	GPTW7 to GPTW9 pin output disable bit
POECR1	MTU0A1ZE	MTIOC0A P31 pin high-impedance enable bit	—
	MTU0B1ZE	MTIOC0B P30 pin high-impedance enable bit	—
	MTU0B2ZE	MTIOC0B P93 pin high-impedance enable bit	—
	MTU0C1ZE	MTIOC0C P94 pin high-impedance enable bit	—
POECR2	MTU7BDZE	—	MTIOC7B/MTIOC7D pin high-impedance enable bit
	MTU7ACZE	—	MTIOC7A/MTIOC7C pin high-impedance enable bit
	MTU6BDZE	—	MTIOC6B/MTIOC6D pin high-impedance enable bit
POECR3	—	—	Port output enable control register 3

Register	Bit	RX23T (POE3b)	RX66T (POE3B)
POECR4	IC1ADDMT34ZE	—	MTU3 and MTU4 output disabling condition POE0F add bit
	IC2ADDMT34ZE	—	MTU3 and MTU4 output disabling condition POE4F add bit
	IC5ADDMT34ZE	—	MTU3 and MTU4 output disabling condition POE11F add bit
	IC6ADDMT34ZE	—	MTU3 and MTU4 output disabling condition POE12F add bit
	IC8ADDMT34ZE	—	MTU3 and MTU4 output disabling condition POE9F add bit
	IC9ADDMT34ZE	—	MTU3 and MTU4 output disabling condition POE13F add bit
	IC10ADDMT34ZE	—	MTU3 and MTU4 output disabling condition POE14F add bit
POECR4B	—	—	Port output enable control register 4B
POECR5	IC2ADDMT0ZE	—	MTU0 output disabling condition POE4F add bit
POECR5	IC3ADDMT0ZE	—	MTU0 output disabling condition POE8F add bit
	IC5ADDMT0ZE	—	MTU0 output disabling condition POE11F add bit
	IC6ADDMT0ZE	—	MTU0 output disabling condition POE12F add bit
	IC8ADDMT0ZE	—	MTU0 output disabling condition POE9F add bit
	IC9ADDMT0ZE	—	MTU0 output disabling condition POE13F add bit
	IC10ADDMT0ZE	—	MTU0 output disabling condition POE14F add bit
POECR6	—	—	Port output enable control register 6
POECR6B	—	—	Port output enable control register 6B
POECR7	—	—	Port output enable control register 7
POECR8	—	—	Port output enable control register 8
POECR9	—	—	Port output enable control register 9
POECR10	—	—	Port output enable control register 10
POECR11	—	—	Port output enable control register 11
PMMCR0	—	—	Port mode mask control register 0

Register	Bit	RX23T (POE3b)	RX66T (POE3B)
PMMCR1	—	—	Port mode mask control register 1
PMMCR2	—	—	Port mode mask control register 2
PMMCR3	—	—	Port mode mask control register 3
POECMPFR	C3FLAG	—	Comparator channel 3 output detection flag
	C4FLAG	—	Comparator channel 4 output detection flag
	C5FLAG	—	Comparator channel 5 output detection flag
POECMPSEL	POEREQ3	—	Comparator channel 3 output disabling request enable bit
	POEREQ4	—	Comparator channel 4 output disabling request enable bit
	POEREQ5	—	Comparator channel 5 output disabling request enable bit
POECMPEXm	—	—	Port output enable comparator request extended selection register m (m = 0 to 8)
M0SELR1	—	—	MTU0 pin select register 1
M0SELR2	—	—	MTU0 pin select register 2
M3SELR	—	—	MTU3 pin select register
M4SELR1	—	—	MTU4 pin select register 1
M4SELR2	—	—	MTU4 pin select register 2
M6SELR	—	—	MTU6 pin select register
M7SELR1	—	—	MTU7 pin select register 1
M7SELR2	—	—	MTU7 pin select register 2
M9SELR1	—	—	MTU9 pin select register 1
M9SELR2	—	—	MTU9 pin select register 2
G0SELR	—	—	GPTW0 pin select register
G1SELR	—	—	GPTW1 pin select register
G2SELR	—	—	GPTW2 pin select register
G3SELR	—	—	GPTW3 pin select register
G4SELR	—	—	GPTW4 pin select register
G5SELR	—	—	GPTW5 pin select register
G6SELR	—	—	GPTW6 pin select register
G7SELR	—	—	GPTW7 pin select register
G8SELR	—	—	GPTW8 pin select register
G9SELR	—	—	GPTW9 pin select register

2.17 8-Bit Timer

Table 2.57 is a comparative overview of 8-bit timer, and Table 2.58 is a comparison of 8-bit timer registers.

Table 2.57 Comparative Overview of 8-Bit Timer

Item	RX23T (TMR)	RX66T (TMR)
Count clock	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192 • External clock: external count clock	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192 • External clock: external count clock
Number of channels	(8 bits × 2 channels) × 2 units	(8 bits × 2 channels) × 4 units
Compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selected by compare match A or B, or an external counter reset signal.	Selected by compare match A or B, or an external counter reset signal.
Timer output	Output pulses with a desired duty cycle or PWM output	Output pulses with a desired duty cycle or PWM output
Cascading of two channels	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits, TMR4 for the upper 8 bits and TMR5 for the lower 8 bits, TMR6 for the upper 8 bits and TMR7 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches, TMR5 can be used to count TMR4 compare matches, TMR7 can be used to count TMR6 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
Event linking function (output)	—	Compare match A, compare match B, and overflow (TMR0 to TMR3)
Event linking function (input)	—	One of the following three operations proceeds in response to an event reception: (1) Counting start operation (TMR0 to TMR3) (2) Event counting operation (TMR0 to TMR3) (3) Counting restart operation (TMR0 to TMR3)
DTC activation	DTC can be activated by compare match A interrupts or compare match B interrupts.	DTC can be activated by compare match A interrupts or compare match B interrupts.
A/D conversion start trigger of the A/D converter	Compare match A of TMR0 and TMR2	Compare match A of TMR0, TMR2, TMR4, and TMR6

Item	RX23T (TMR)	RX66T (TMR)
Capable of generating baud rate clock for SCI	Generates baud rate clock for SCI.	Generates baud rate clock for SCI.
Low power consumption function	Each unit can be placed in a module stop state	Each unit can be placed in a module stop state

Table 2.58 Comparison of 8-Bit Timer Registers

Register	Bit	RX23T (TMR)	RX66T (TMR)
TCSTR	—	—	Timer counter start register

2.18 Compare Match Timer

Table 2.59 is a comparative overview of compare match timer.

Table 2.59 Comparative Overview of Compare Match Timer

Item	RX23T (CMT)	RX66T (CMT)
Count clocks	Four frequency dividing clocks: One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.	Four frequency dividing clocks: One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.
Interrupt	A compare match interrupt can be requested for each channel.	A compare match interrupt can be requested for each channel.
Event linking function (output)	—	An event signal is output upon a CMT1 compare match.
Event linking function (input)	—	• Linking to the specified module is possible. • CMT1 count start, event counter, or count restart operation is possible.
Low power consumption function	Each unit can be placed in a module stop state.	Each unit can be placed in a module stop state.

2.19 Independent Watchdog Timer

Table 2.60 is a comparative overview of independent watchdog timer, and Table 2.61 is a comparison of independent watchdog timer registers.

Table 2.60 Comparative Overview of Independent Watchdog Timer

Item	RX23T (IWDTa)	RX66T (IWDTa)
Count source	IWDT-dedicated clock (IWDTCLK)	IWDT-dedicated clock (IWDTCLK)
Clock divide ratio	Divide by 1, 16, 32, 64, 128, or 256	Divide by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Counting automatically starts after a reset (auto-start mode) • Counting is started (register start mode) by refreshing the counter (writing 00h and then FFh to the IWDTRR register).	• Auto-start mode: Counting automatically starts after a reset is released • Register start mode: Counting is started by refresh operation (writing 00h and then FFh to the IWDTRR register).
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • In low power consumption states (depends on the register setting) • A counter underflows or a refresh error occurs Counting restarts (In auto-start mode, counting automatically restarts after a reset or after a non-maskable interrupt request is output. In register start mode, counting restarts after refreshing.)	• Reset (the down-counter and other registers return to their initial values) • In low power consumption states (depends on the register setting) • A counter underflows or a refresh error occurs (only in register start mode)
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)	• Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Reset output sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt/ interrupt sources	• Down-counter underflows. • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows. • Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read by the IWDTSR register.	The down-counter value can be read by the IWDTSR register.
Event linking function (output)	—	• Down-counter underflow event output • Refresh error event output
Output signal (internal signal)	• Reset output • Interrupt request output • Sleep mode count stop control output	• Reset output • Interrupt request output • Sleep mode count stop control output

Item	RX23T (IWDTa)	RX66T (IWDTa)
Auto-start mode (controlled by option function select register 0 (OFS0))	• Selecting the clock frequency divide ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (OFS0.IWDTSLCSTP bit)	• Selecting the clock frequency divide ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)
Register start mode (controlled by the IWDT registers)	• Selecting the clock frequency divide ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (IWDTCSTPR.SLCSTP bit)	• Selecting the clock frequency divide ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)

Table 2.61 Comparison of Independent Watchdog Timer Registers

Register	Bit	RX23T (IWDTa)	RX66T (IWDTa)
IWDTCR	TOPS[1:0]	Timeout period select bits b1 b0 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1,024 cycles (03FFh) 1 1: 2,048 cycles (07FFh)	Timeout period select bits b1 b0 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh)
IWDTRCR	RSTIRQS	Reset interrupt request select bit 0: Non-maskable interrupt request output is enabled. 1: Reset output is enabled.	Reset interrupt request select bit 0: Non-maskable interrupt request or interrupt request output is enabled.*1 1: Reset output is enabled.
IWDTCSTPR	SLCSTP	Sleep mode count stop control bit 0: Count stop is disabled. 1: Count is stopped at a transition to sleep mode, software standby mode, or deep sleep mode.	Sleep mode count stop control bit 0: Count stop is disabled. 1: Count is stopped at a transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode.

Note: 1. When the value of the NMIER.IWDTEN bit is 1 non-maskable interrupts, and when it is 0 maskable interrupts, are generated.

2.20 Serial Communications Interface

Table 2.62 is a comparative overview of the serial communications interfaces, Table 2.63 is a comparative listing of serial communications interface channels, and Table 2.64 is a comparison of serial communications interface registers.

Table 2.62 Comparative Overview of Serial Communications Interfaces

Item		RX23T (SCIg)	RX66T (SCIj, SCIi, SCIh)
Serial communications mode		• Asynchronous • Clock synchronous • Smart card interface • Simple I²C-bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C-bus • Simple SPI bus
Transfer speed		Bit rate specifiable with the on-chip baud rate generator.	Bit rate specifiable with the on-chip baud rate generator.
Full-duplex communications		• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable as LSB first or MSB first transfer	Selectable as LSB first or MSB first transfer
Interrupt sources		• Transmit end, transmit data empty, receive data full, and receive error • Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)	• Transmit end, transmit data empty, receive data full, receive error, receive data ready (SCI11), and data match (SCI1, SCI5, SCI6, SCI8, SCI9, SCI11) • Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)
Low power consumption function		Module stop state can be set for each channel.	Module stop state can be set for each channel.
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bit	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/ reception
	Transmit/ receive FIFO	—	16-stage FIFOs for transmit and receive buffers (SCI11)
	Data match detection	—	Compares receive data and comparison data, and generates interrupt when they are matched (SCI1, SCI5, SCI6, SCI8, SCI9, SCI11)
	Start-bit detection	Low level or falling edge is selectable.	Low level or falling edge is selectable.

Item		RX23T (SCIg)	RX66T (SCIj, SCIi, SCIh)
Asynchronous mode	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly or reading the SPTR.RXDMON flag.
	Clock source	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used. (SCI5, SCI6)	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used. (SCI5, SCI6, SCI12)
	Double-speed mode	Baud rate generator double-speed mode is selectable.	Baud rate generator double-speed mode is selectable.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Transmit/ receive FIFO	—	16-stage FIFOs for transmit and receive buffers (SCI11)
Smart card interface mode	Error processing	• An error signal can be automatically transmitted when detecting a parity error during reception • Data can be automatically retransmitted when receiving an error signal during transmission	• An error signal can be automatically transmitted when detecting a parity error during reception • Data can be automatically retransmitted when receiving an error signal during transmission
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Transfer format	I^2C-bus format	I^2C-bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer rate	Fast mode is supported.	Fast mode is supported.
	Noise cancellation	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.
Simple SPI bus	Data length	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.

Item		RX23T (SCIg)	RX66T (SCIj, SCIi, SCIh)
Extended serial mode (supported by SCI 12 only)	Start Frame transmission	—	• Output of a low level as the Break Field over a specified width and generation of interrupts on completion • Detection of bus collisions and the generation of interrupts on detection
	Start Frame reception	—	• Detection of the Break Field low width and generation of an interrupt on detection • Comparison of Control Fields 0 and 1 and generation of an interrupt when the two match • Two kinds of data for comparison (primary and secondary) can be set in Control Field 1. • A priority interrupt bit can be set in Control Field 1. • Handling of Start Frames that do not include a Break Field • Handling of Start Frames that do not include a Control Field 0 • Function for measuring bit rates
	I/O control function	—	• Selectable polarity for TXDX12 and RXDX12 signals • Selection of a digital filter for the RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Selectable timing for the sampling of data received through RXDX12
	Timer function	—	Usable as a reloading timer
Bit rate modulation function		Correction of outputs from the on-chip baud rate generator can reduce errors.	Correction of outputs from the on-chip baud rate generator can reduce errors.
Event linking function (supported by SCI5 only)		—	• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output

Table 2.63 Comparison of Serial Communications Interface Channel Specifications

Item	RX23T (SCIg)	RX66T (SCIj, SCIi, SCIh)
Asynchronous mode	SCI1, SCI5	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12
Clock synchronous mode	SCI1, SCI5	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12
Smart card interface mode	SCI1, SCI5	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12
Simple I²C mode	SCI1, SCI5	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12
Simple SPI mode	SCI1, SCI5	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12
FIFO mode	—	SCI11
Data match detection	—	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11
Extended serial mode	—	SCI12
TMR clock input	SCI5	SCI5, SCI6, SCI12
Event linking function	—	SCI5
Peripheral module clock	PCLKB: SCI1, SCI5	PCLKB: SCI1, SCI5, SCI6, SCI8, SCI9, SCI12 PCLKA: SCI11

Table 2.64 Comparison of Serial Communications Interface Registers

Register	Bit	RX23T (SCIg)	RX66T (SCIj, SCIi, SCIh)
FRDR	—	—	Receive FIFO data register
FTDR	—	—	Transmit FIFO data register
SMR	CM	Communications mode bit When SCMR.SMIF bit = 0 0: Asynchronous mode 1: Clock synchronous mode or simple SPI mode	Communications mode bit When SCMR.SMIF bit = 0 0: Asynchronous mode or simple I²C mode 1: Clock synchronous mode or simple SPI mode
SCR	CKE[1:0]	Clock enable bits When SCMR.SMIF = 0 • For SCI1 Asynchronous mode: b1 b0 0 0: On-chip baud rate generator The SCKn pin can be used as an I/O port by means of I/O port settings. 0 1: On-chip baud rate generator A clock with the same frequency as the bit rate is output on the SCKn pin. 1 x: External clock A clock with a frequency 16 times the bit rate should be input on the SCKn pin. Input a clock signal with a frequency eight times the bit rate when the SEMR.ABCS bit is set to 1.	Clock enable bits When SCMR.SMIF = 0 Asynchronous mode: b1 b0 0 0: On-chip baud rate generator The SCKn pin is placed in the high-impedance state 0 1: On-chip baud rate generator A clock with the same frequency as the bit rate is output on the SCKn pin. 1 x: External clock A clock with a frequency 16 times the bit rate should be input on the SCKn pin. Input a clock signal with a frequency eight times the bit rate when the SEMR.ABCS bit is set to 1.

Register	Bit	RX23T (SCIg)	RX66T (SCIj, SCIi, SCIh)
SCR	CKE[1:0]	Clock synchronous mode: b1 b0 0 x: Internal clock The SCKn pin functions as the clock output pin. 1 x: External clock The SCKn pin functions as the clock input pin. • For SCI5 Asynchronous mode: b1 b0 0 0: On-chip baud rate generator The SCKn pin can be used as an I/O port by means of I/O port settings. 0 1: On-chip baud rate generator A clock with the same frequency as the bit rate is output on the SCKn pin. 1 x: External clock or TMR clock A clock with a frequency 16 times the bit rate should be input on the SCKn pin. Input a clock signal with a frequency eight times the bit rate when the SEMR.ABCS bit is set to 1. The TMR clock can be used. The SCKn pin is available for use as an I/O port according to the I/O port settings when the TMR clock is used. Clock synchronous mode: b1 b0 0 x: Internal clock The SCKn pin functions as the clock output pin. 1 x: External clock The SCKn pin functions as the clock input pin.	Clock synchronous mode: b1 b0 0 x: Internal clock The SCKn pin functions as the clock output pin. 1 x: External clock The SCKn pin functions as the clock input pin. Asynchronous mode: b1 b0 0 0: On-chip baud rate generator The SCKn pin is placed in the high-impedance state 0 1: On-chip baud rate generator The clock with the same frequency as the bit rate is output from the SCKn pin. 1 x: External clock The clock with a frequency 16 times the bit rate should be input from the SCKn pin. Input a clock signal with a frequency eight times the bit rate when the SEMR.ABCS bit is 1. Clock synchronous mode: b1 b0 0 x: Internal clock The SCKn pin functions as the clock output pin. 1 x: External clock The SCKn pin functions as the clock input pin.

Register	Bit	RX23T (SCIg)	RX66T (SCIj, SCIi, SCIh)
SCR	CKE[1:0]	When SCMR.SMIF = 1 • When SMR.GM = 0 b1 b0 0 0: Output disabled The SCKn pin is available for use as an I/O port according to the I/O port settings. 0 1: Clock output 1 x: Setting prohibited • When SMR.GM = 1 b1 b0 0 0: Output fixed low x 1: Clock output 1 0: Output fixed high	When SCMR.SMIF = 1 • When SMR.GM = 0 b1 b0 0 0: Output disabled The SCKn pin becomes high-impedance. 0 1: Clock output 1 x: Setting prohibited • When SMR.GM = 1 b1 b0 0 0: Output fixed low x 1: Clock output 1 0: Output fixed high
SSRFIFO	—	—	Serial status register
SEMR	ACS0	Asynchronous mode clock source select bit (Valid only in asynchronous mode) 0: External clock input 1: Logical AND of two compare matches output from TMR (valid for SCI5 only) Available compare match output varies per SCI channel.	Asynchronous mode clock source select bit (Valid only in asynchronous mode) 0: External clock input 1: Logical AND of two compare matches output from TMR (valid for SCI5, SCI6, and SCI12 only) Available compare match output varies per SCI channel.
	ABCSE	—	Asynchronous mode base clock select extended bit This bit is reserved for SCI12. It is read as 0. The write value should be 0.
FCR	—	—	FIFO control register
FDR	—	—	FIFO data count register
LSR	—	—	Line status register
CDR	—	—	Comparison data register
DCCR	—	—	Data comparison control register
SPTR	—	—	Serial port register
ESMER	—	—	Extended serial module enable register
CR0	—	—	Control register 0
CR1	—	—	Control register 1
CR2	—	—	Control register 2
CR3	—	—	Control register 3
PCR	—	—	Port control register
ICR	—	—	Interrupt control register
STR	—	—	Status register
STCR	—	—	Status clear register
CF0DR	—	—	Control Field 0 data register
CF0CR	—	—	Control Field 0 compare enable register
CF0RR	—	—	Control Field 0 receive data register

Register	Bit	RX23T (SCIg)	RX66T (SCIj, SCIi, SCIh)
PCF1DR	—	—	Primary Control Field 1 data register
SCF1DR	—	—	Secondary Control Field 1 data register
CF1CR	—	—	Control Field 1 compare enable register
CF1RR	—	—	Control Field 1 receive data register
TCR	—	—	Timer control register
TMR	—	—	Timer mode register
TPRE	—	—	Timer prescaler register
TCNT	—	—	Timer count register

2.21 I²C Bus Interface

Table 2.65 is a comparative overview of I²C bus interface.

Table 2.65 Comparative Overview of I²C Bus Interface

Item	RX23T (RIICa)	RX66T (RIICa)
Communications format	• I²C-bus format or SMBus format • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate	• I²C-bus format or SMBus format • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate
Transfer rate	Fast-mode is supported (up to 400 kbps)	Fast-mode is supported (up to 400 kbps)
SCL clock	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%.	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%.
Issuing and detecting conditions	• Start, restart, and stop conditions are automatically generated. • Start conditions (including restart conditions) and stop conditions are detectable.	• Start, restart, and stop conditions are automatically generated. • Start conditions (including restart conditions) and stop conditions are detectable.
Slave address	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.
Acknowledgment	• For transmission, the acknowledge bit is automatically loaded. Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.	• For transmission, the acknowledge bit is automatically loaded. Transfer of the next data for transmission can be automatically aborted on detection of a not-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.
Wait function	• In reception, the following periods of waiting can be obtained by holding the SCL clock at the low level: • Waiting between the eighth and ninth clock cycles • Waiting between the ninth clock cycle and the first clock cycle of the next transfer	• In reception, the following periods of waiting can be obtained by holding the SCL clock at the low level: • Waiting between the eighth and ninth clock cycles • Waiting between the ninth clock cycle and the first clock cycle of the next transfer
SDA output delay function	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.

Item	RX23T (RIICa)	RX66T (RIICa)
Arbitration	• For multi-master operation — Operation to synchronize the SCL clock in cases of conflict with the SCL signal from another master is possible. — When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the internal signal for the SDA line and the level on the SDA line not matching is detectable. • Loss of arbitration due to non-matching of internal and line levels for data is detectable in slave transmission.	• For multi-master operation — Operation to synchronize the SCL clock in cases of conflict with the SCL signal from another master is possible. — When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the internal signal for the SDA line and the level on the SDA line not matching is detectable. • Loss of arbitration due to non-matching of internal and line levels for data is detectable in slave transmission.
Timeout detection function	The internal timeout function is capable of detecting long-interval stop of the SCL clock.	The internal timeout function is capable of detecting long-interval stop of the SCL clock.
Noise cancellation	The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable by software.	The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable by software.
Interrupt sources	Four sources: • Error in transfer or occurrence of events Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end	Four sources: • Error in transfer or occurrence of events Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end
Low power consumption function	Ability to transition to module stop state.	Ability to transition to module stop state.
RIIC operating modes	Four modes: • Master transmit mode • Master receive mode • Slave transmit mode • Slave receive mode	Four modes: • Master transmit mode • Master receive mode • Slave transmit mode • Slave receive mode

Item	RX23T (RIICa)	RX66T (RIICa)
Event linking function (output)	—	Four sources: • Error in transfer or occurrence of events Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end

2.22 Serial Peripheral Interface

Table 2.66 is a comparative overview of serial peripheral interface, and Table 2.67 is a comparison of serial peripheral interface registers.

Table 2.66 Comparative Overview of Serial Peripheral Interface

Item	RX23T (RSPIa)	RX66T (RSPIc)
Number of channels	1 channel	1 channel
RSPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communication through SPI operation (4-wire method) or clock synchronous operation (3-wire method), and interrupts can be generated in each case. • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communication through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK
Data format	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits).	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits). • Byte swapping of transmit and receive data is selectable
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4,096). • In slave mode, the minimum PCLK clock divided by 8 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 8). Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4,096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4). Width at high level: 2 cycles of PCLK; width at low level: 2 cycles of PCLK
Buffer configuration	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection

Item	RX23T (RSPIa)	RX66T (RSPIc)
SSL control function	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity
Control in master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function
Interrupt sources	Interrupt sources • Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, or parity error) • RSPI idle interrupt (RSPI idle)	Interrupt sources • Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, underrun, or parity error) • RSPI idle interrupt (RSPI idle)
Event linking function (output)	—	The following events can be output to the event link controller. (RSPI0) • Receive buffer full signal • Transmit buffer empty signal • Mode fault, overrun, underrun, or parity error signal • RSPI idle signal • Transmission-completed signal

Item	RX23T (RSPIa)	RX66T (RSPIc)
Others	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode
Low power consumption function	Ability to specify module stop state.	Ability to specify module stop state.

Table 2.67 Comparison of Serial Peripheral Interface Registers

Register	Bit	RX23T (RSPIa)	RX66T (RSPIc)
SPSR	UDRF	—	Underrun error flag When clearing the UDRF flag to 0, clear the MODF flag to 0 at the same time.
SPDR	—	RSPI data register Available access size: • Longwords (SPDCR.SPLW = 1) • Words (SPDCR.SPLW = 0)	RSPI data register Available access size: • Longwords (SPDCR.SPLW = 1, SPDCR.SPBYT = 0) • Words (SPDCR.SPLW=0, SPDCR.SPBYT = 0) • Bytes (SPDCR.SPBYT = 1)
SPDCR	SPBYT	—	RSPI byte access specification bit
SPCR2	SPPE	Parity enable bit 0: Transmit data parity bit is not added. Receive data parity check is disabled. 1: Transmit data parity bit is added and receive data parity check is enabled. (When SPCR.TXMD = 0) Transmit data parity bit is added, but receive data parity check is disabled. (When SPCR.TXMD = 1)	Parity enable bit 0: Transmit data parity bit is not added. Receive data parity check is disabled. 1: Transmit data parity bit is added and receive data parity check is enabled.
SPDCR2	—	—	RSPI data control register 2

2.23 CRC Calculator

Table 2.68 is a comparative overview of CRC calculator, and Table 2.69 is a comparison of CRC calculator registers.

Table 2.68 Comparative Overview of CRC Calculator

Item	RX23T (CRC)	RX66T (CRCA)	
Data size	8 bits	8 bits	32 bits
Data for CRC calculation	CRC codes are generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 32n-bit units (where n is a whole number)
CRC processor unit	8-bit parallel processing	8-bit parallel processing	32-bit parallel processing
CRC generating polynomial	One of three generating polynomials is selectable • 8-bit CRC: — $X^8 + X^2 + X + 1$ • 16-bit CRC: — $X^{16} + X^{15} + X^2 + 1$ — $X^{16} + X^{12} + X^5 + 1$	One of three generating polynomials is selectable • 8-bit CRC: — $X^8 + X^2 + X + 1$ • 16-bit CRC: — $X^{16} + X^{15} + X^2 + 1$ — $X^{16} + X^{12} + X^5 + 1$	One of two generating polynomials is selectable • 32-bit CRC: — $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ — $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$
CRC calculation switching	The bit order of CRC calculation results can be switched for LSB first or MSB first communication	The order of the bits produced by CRC calculation can be switched for LSB first or MSB first communication	
Low power consumption	Ability to specify module stop state.	Ability to transition to module stop state.	

Table 2.69 Comparison of CRC Calculator Registers

Register	Bit	RX23T (CRC)	RX66T (CRCA)
CRCCR	GPS[1:0]: RX23T GPS[2:0]: RX66T	CRC generating polynomial switching bits b1 b0 0 0: No calculation is executed. 0 1: 8-bit CRC ($X^8 + X^2 + X + 1$) 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$) 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$)	CRC generating polynomial switching bits b2 b0 0 0 0: No calculation is executed. 0 0 1: 8-bit CRC ($X^8 + X^2 + X + 1$) 0 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$) 0 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$) 1 0 0: 32-bit CRC ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1: 32-bit CRC ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) 1 1 0: No calculation is executed. 1 1 1: No calculation is executed.
	LMS	CRC calculation switching (b2)	CRC calculation switching (b6)
CRCDIR	—	CRC data input register Available access size: • Bytes	CRC data input register Available access size: • Longwords (When generating a 32-bit CRC) • Bytes (When generating a 16-bit/8-bit CRC)
CRCDOR	—	CRC data output register Available access size: • Words When generating 8-bit CRC, the valid CRC code is obtained from the lower-order byte (b7 to b0).	CRC data output register Available access size: • Longwords (When generating a 32-bit CRC) • Words (When generating a 16-bit CRC) • Bytes (When generating a 8-bit CRC)

2.24 12-Bit A/D Converter

Table 2.70 is a comparative overview of the 12-bit A/D converters, Table 2.71 is a comparison of 12-bit A/D converter registers, and Table 2.72 is a comparative listing of A/D conversion startup sources that can be set in the ADSTRGR register.

Table 2.70 Comparative Overview of 12-Bit A/D Converters

Item	RX23T (S12ADE)	RX66T (S12ADH)
Number of units	1 unit (S12AD)	3 units (S12AD, S12AD1, and S12AD2)
Input channels	S12AD: 10 channels	S12AD: 8 channels S12AD1: 8 channels S12AD2: 14 channels
Extended analog function	Internal reference voltage	Temperature sensor output, internal reference voltage (S12AD2 only)
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	1 µs per channel (when A/D conversion clock ADCLK = 40 MHz)	0.9 µs per channel (when A/D conversion clock ADCLK = 60 MHz)
A/D conversion clock	• Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. PCLK to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 • ADCLK is set using the clock generation circuit.	• Peripheral module clock PCLK and A/D conversion clock ADCLK can be set with one of the following frequency ratio: PCLK to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1 • ADCLK is set using the clock generation circuit. • A/D conversion clock (ADCLK) can operate between 8 MHz at a minimum and 60 MHz at a maximum.
Data registers	• 10 registers for analog input, 1 for A/D-converted data duplication in double trigger mode, and 2 for A/D-converted data duplication during extended operation in double trigger mode unit. • One register for internal reference • One register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • 12-bit accuracy output for the results of A/D conversion • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode.	• 30 registers for analog input (eight for S12AD, eight for S12AD1, and 14 for S12AD2), 1 for A/D-converted data duplication in double trigger mode per unit, and 2 for A/D-converted data duplication during extended operation in double trigger mode per unit. • One register for temperature sensor (S12AD2) • One register for internal reference (S12AD2) • One register for self-diagnosis per unit • The results of A/D conversion are stored in 12-bit A/D data registers. • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode.

Item	RX23T (S12ADE)	RX66T (S12ADH)
Data registers	• Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.	• Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.
Operating modes	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 10 arbitrarily selected channels. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs of up to 10 arbitrarily selected channels. • Group scan mode: — The analog inputs of up to 10 arbitrarily selected channels are divided into group A and group B, and A/D conversion is performed only once on analog inputs selected in group units. — The conditions for scanning start of groups A and B (synchronous trigger) can be independently selected, thus allowing A/D conversion of each group to be started independently.	Operating modes can be set independently for three units. • Single scan mode: — A/D conversion is performed only once on the analog inputs arbitrarily selected. — A/D conversion is performed only once on the temperature sensor output (S12AD2). — A/D conversion is performed only once on the internal reference voltage (S12AD2). • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs arbitrarily selected. • Group scan mode: — Two (groups A and B) or three (groups A, B, and C) can be selected as the number of the groups to be used. (Only the combination of groups A and B can be selected when the number of the groups is two.) — Analog inputs, temperature sensor output (S12AD2), and internal reference voltage (S12AD2) that are arbitrarily selected are divided into two groups (group A and B) or three groups (group A, B, and C), and A/D conversion of the analog input selected on a group basis is performed only once. — The conditions for scanning start of groups A, B, and C (synchronous trigger) can be independently selected, thus allowing A/D conversion of each group to be started independently.

Item	RX23T (S12ADE)	RX66T (S12ADH)
Operating modes	• Group scan mode (when group priority control selected): — If a group A trigger is input during A/D conversion of group B, A/D conversion of group B halts and A/D conversion of group A takes place. — It is possible to specify that A/D conversion of group B restarts (rescan) after A/D conversion of group A finishes.	• Group scan mode (when group priority control selected): — If a priority-group trigger is input during scanning of the low-priority group, scan of the low-priority group is stopped and scan of the priority group is started. The priority order is group A (highest) > group B > group C (lowest). — Whether or not to restart scanning of the low-priority group after processing for the high-priority group completes, is selectable. Rescan can also be set to start either from the beginning of the selected channel or the channel on which A/D conversion is not completed.
Conditions for A/D conversion start	• Software trigger • Synchronous trigger: Trigger by the multi-function timer pulse unit (MTU) or 8-bit timer (TMR). • Asynchronous trigger: A/D conversion can be triggered by the external trigger ADTRG0# pin.	• Software trigger • Synchronous trigger: Trigger by the multi-function timer pulse unit (MTU), 8-bit timer (TMR), or event link controller (ELC). • Asynchronous trigger: A/D conversion can be triggered by the external trigger ADTRG0# (S12AD), ADTRG1# (S12AD1), or ADTRG2# (S12AD2) pin (independently for three units).
Functions	• Channel-dedicated sample-and-hold function (three channels) • Variable sampling state count • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers	• Channel-dedicated sample-and-hold function (three channels for S12AD and three channels for S12AD1) (Constant sampling can be set) • Variable sampling time (can be set per channel) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection assist function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers • Comparison function (windows A and B) • Order of channel conversion in each unit can be set. • Input signal amplification function of the programmable gain amplifier (each unit has 3 channels; either single-ended input or pseudo-differential input can be selected)

Item	RX23T (S12ADE)	RX66T (S12ADH)
Interrupt sources	• In the modes except double trigger mode and group scan mode, a scan end interrupt request (S12ADI) can be generated on completion of single scan.	• In the modes except double trigger mode and group scan mode, a scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of single scan. (Independently for three units).
	• In double trigger mode, a scan end interrupt request (S12ADI) can be generated on completion of double scan.	• In double trigger mode, a scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of double scan. (Independently for three units).
	• In group scan mode, a scan end interrupt request (S12ADI) can be generated on completion of group A scan and whereas a scan end interrupt request (GBADI) for group B can be generated on completion of group B scan.	• In group scan mode, a scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of group A scan, whereas a group B scan end interrupt request (S12GBADI, S12GBADI1, or S12GBADI2) can be generated on completion of group B scan, and a group C scan end interrupt request (S12GCADI, S12GCADI1, or S12GCADI2) can be generated on completion of group C scan.
	• When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI) can be generated on completion of double scan of group A, and the corresponding scan end interrupt request (GBADI) can be generated on completion of group B and group C scan.	• When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of double scan of group A, and the corresponding scan end interrupt request (S12GBADI/S12GCADI, S12GBADI1/S12GCADI1, or S12GBADI2/S12GCADI2) can be generated on completion of group B and group C scan. • A compare interrupt request (S12CMPAI, S12CMPAI1, S12CMPAI2, S12CMPBI, S12CMPBI1, or S12CMPBI2) can be generated upon a match with the comparison condition for the digital compare function.
	• The S12ADI and GBADI interrupts can activate the data transfer controller (DTC).	• The S12ADI/S12ADI1/S12ADI2, S12GBADI/S12GBADI1/S12GBADI2, and S12GCADI/S12GCADI1/S12GCADI2 interrupts can trigger the DMA controller (DMAC) and data transfer controller (DTC).

Item	RX23T (S12ADE)	RX66T (S12ADH)
Event linking function	—	• The event signal is generated when all scans are finished. • The event signal is generated depending on conditions for comparison function window in single scan mode. • Able to start scanning by a trigger from the ELC.
Low power consumption function	Ability to specify module stop state.	Ability to transition to module stop state.

Table 2.71 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX23T (S12ADE)	RX66T (S12ADH)
ADDRy	—	A/D data registers y (y = 0 to 7, 16, 17)	A/D data registers y (S12AD: y = 0 to 7, S12AD1: y = 0 to 7, S12AD2: y = 0 to 11, 16, 17)
ADTSDR	—	—	A/D temperature sensor data register
S12AD1.ADANSA0	—	—	A/D channel select register A0
S12AD2.ADANSA0	—	—	A/D channel select register A0
ADANSA1	ANSA100 ANSA101	A/D conversion channel select bits 0: AN016 and AN017 not selected for conversion. 1: AN016 and AN017 selected for conversion.	A/D conversion channel select bits 0: AN216 and AN217 not selected for conversion. 1: AN216 and AN217 selected for conversion.
S12AD1.ADANSB0	—	—	A/D channel select register B0
S12AD2.ADANSB0	—	—	A/D channel select register B0
ADANSB1	ANSB100 ANSB101	A/D conversion channel select bits 0: AN016 and AN017 not selected for conversion. 1: AN016 and AN017 selected for conversion.	A/D conversion channel select bits 0: AN216 and AN217 not selected for conversion. 1: AN216 and AN217 selected for conversion.
ADANSC0	—	—	A/D channel select register C0
ADANSC1	—	—	A/D channel select register C1
ADSCSn	—	—	A/D channel conversion order setting register n (n = 0 to 13)
ADADS1	ADS100 ADS101	A/D-converted value addition/average channel select bits 0: A/D-converted value addition/average mode is not selected for AN016 and AN017. 1: A/D-converted value addition/average mode is selected for AN016 and AN017.	A/D-converted value addition/average channel select bits These bits set the A/D-converted value addition/average mode for AN216 and AN217. 0: A/D-converted value addition/average mode is disabled. 1: A/D-converted value addition/average mode is enabled.

Register	Bit	RX23T (S12ADE)	RX66T (S12ADH)
ADEXICR	TSSAD	—	Temperature sensor output A/D-converted value addition/average mode select bit
	TSSA	—	Temperature sensor output A/D conversion select bit
	TSSB	—	Group B temperature sensor output A/D conversion select bit
ADEXICR	OCSB	—	Group B internal reference voltage A/D conversion select bit
ADGCEXCR	—	—	A/D group C extended input control register
ADGCTRGR	—	—	A/D group C trigger select register
ADSSTRn	—	A/D sampling state register n (n = 0 to 7, L, O)	A/D sampling state register n (n = 0 to 11, L, T, and O)
		Initial value after a reset differs.	
ADSHCR	—	A/D sample-and-hold circuit control register	A/D sample-and-hold circuit control register
		Initial value after a reset differs.	
ADSHCR	SSTSH [7:0]	Channel-dedicated sample-and-hold circuit sampling time setting bits Set a sampling time between 4 and 255 states.	Channel-dedicated sample-and-hold circuit sampling time setting bits Set a sampling time between 12 and 252 clock cycles.
ADSHMSR	—	—	A/D sample-and-hold operating mode select register
ADDISCR	ADNDIS [3:0]	A/D disconnection detection assist setting bits These bits set the precharge or discharge period. The setting value corresponds to the number of states in the precharge or discharge period. The setting must be a value other than 0000b or 0001b.	A/D disconnection detection assist setting bits These bits specify the precharge or discharge period in ADCLK clock cycles. b3 b0 0000: No charging (disconnection detection assist function disabled) 0011: Charging period of 3 clock cycles 0110: Charging period of 6 clock cycles 1001: Charging period of 9 clock cycles 1100: Charging period of 12 clock cycles 1111: Charging period of 15 clock cycles Settings other than the above are prohibited.
ADELCCR	—	—	A/D event link control register
ADGSPCR	LGRRS	—	Restart channel select bit

Register	Bit	RX23T (S12ADE)	RX66T (S12ADH)
ADHVREFCNT		A/D high-potential/low-potential reference voltage control register	—
ADCMPCR	—	—	A/D comparison function control register
ADCMPANSR0	—	—	A/D comparison function window A channel select register 0
ADCMPANSR1	—	—	A/D comparison function window A channel select register 1
ADCMPANSER	—	—	A/D comparison function window A extended input select register
ADCMPLR0	—	—	A/D comparison function window A comparison condition setting register 0
ADCMPLR1	—	—	A/D comparison function window A comparison condition setting register 1
ADCMPLER	—	—	A/D comparison function window A extended input comparison condition setting register
ADCMPDR0	—	—	A/D comparison function window A lower level setting register
ADCMPDR1	—	—	A/D comparison function window A upper level setting register
ADCMPSR0	—	—	A/D comparison function window A channel status register 0
ADCMPSR1	—	—	A/D comparison function window A channel status register 1
ADCMPSER	—	—	A/D comparison function window A extended input channel status register
ADWINMON	—	—	A/D comparison function window A/B status monitoring register
ADCMPBNSR	—	—	A/D comparison function window B channel select register
ADWINLLB	—	—	A/D comparison function window B lower level setting register
ADWINULB	—	—	A/D comparison function window B upper level setting register
ADCMPBSR	—	—	A/D comparison function window B channel status register
ADPGACR	—	—	A/D programmable gain amplifier control register
ADPGAGS0	—	—	A/D programmable gain amplifier gain setting register 0
ADPGADCR0	—	—	A/D programmable gain amplifier differential input control register
ADVMONCR	—	—	A/D internal reference voltage monitoring circuit enable register
ADVMONO	—	—	A/D internal reference voltage monitoring circuit output enable register

Table 2.72 Comparative Listing of A/D Conversion Startup Sources that can be Set in ADSTRGR Register

Bit	RX23T (S12ADE)	RX66T (S12ADH)
TRSB[5:0]	A/D conversion start trigger select bits for Group B b5 b0 1 1 1 1 1 1: Trigger source deselection state 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1	Group B A/D conversion start trigger select bits b5 b0 1 1 1 1 1 1: Trigger source deselection state 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 0 1 1 0: TRGA6N 0 0 0 1 1 1: TRGA7N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 0 1 1 0 1: TRG7AN 0 0 1 1 1 0: TRG7BN 0 0 1 1 1 1: TRG7AN or TRG7BN 0 1 0 0 0 0: TRG7ABN 0 1 0 0 1 1: TRGA9N 0 1 0 1 0 0: TRG9N 0 1 1 0 0 1: TRGA0N or TRG0N 0 1 1 0 1 0: TRGA9N or TRG9N 0 1 1 0 1 1: TRGA0N or TRGA9N 0 1 1 1 0 0: TRG0N or TRG9N 1 0 0 0 0 1: TRG9AEN 1 0 0 0 1 0: TRG0AEN 1 0 0 0 1 1: TRGA09N 1 0 0 1 0 0: TRG09N 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1 0 1 1 1 1 1: TMTRG0AN_2 1 0 0 0 0 0: TMTRG0AN_3 1 1 0 0 1 0: ELCTRG00N*[1] ELCTRG10N*[2] ELCTRG20N*[3] 1 1 0 0 1 1: ELCTRG01N*[1] ELCTRG11N*[2] ELCTRG21N*[3] 1 1 1 0 1 0: ELCTRG00N or ELCTRG01N*[1] ELCTRG10N or ELCTRG11N*[2] ELCTRG20N or ELCTRG21N*[3]

Bit	RX23T (S12ADE)	RX66T (S12ADH)
TRSA[5:0]	A/D conversion start trigger select bits b13 b8 1 1 1 1 1 1: Trigger source deselection state 0 0 0 0 0 0: ADTRG0# 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1	A/D conversion start trigger select bits b13 b8 1 1 1 1 1 1: Trigger source deselection state 0 0 0 0 0 0: ADTRGn# 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 0 1 1 0: TRGA6N 0 0 0 1 1 1: TRGA7N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 0 1 1 0 1: TRG7AN 0 0 1 1 1 0: TRG7BN 0 0 1 1 1 1: TRG7AN or TRG7BN 0 1 0 0 0 0: TRG7ABN 0 1 0 0 1 1: TRGA9N 0 1 0 1 0 0: TRG9N 0 1 1 0 0 1: TRGA0N or TRG0N 0 1 1 0 1 0: TRGA9N or TRG9N 0 1 1 0 1 1: TRGA0N or TRGA9N 0 1 1 1 0 0: TRG0N or TRG9N 1 0 0 0 0 1: TRG9AEN 1 0 0 0 1 0: TRG0AEN 1 0 0 0 1 1: TRGA09N 1 0 0 1 0 0: TRG09N 0 1 1 1 0 1: TMTRG0AN_0/ 0 1 1 1 1 0: TMTRG0AN_1 0 1 1 1 1 1: TMTRG0AN_2 1 0 0 0 0 0: TMTRG0AN_3 1 1 0 0 1 0: ELCTRG00N*1 ELCTRG10N*2 ELCTRG20N*3 1 1 0 0 1 1: ELCTRG01N*1 ELCTRG11N*2 ELCTRG21N*3 1 1 1 0 1 0: ELCTRG00N or ELCTRG01N*1 ELCTRG10N or ELCTRG11N*2 ELCTRG20N or ELCTRG21N*3

Notes: 1. Unit 0
2. Unit 1
3. Unit 2

2.25 D/A Converter for Generating Comparator C Reference Voltage and 12-Bit D/A Converter

Table 2.73 is a comparative overview of the D/A converters, and Table 2.74 is a comparison of D/A converter registers.

Table 2.73 Comparative Overview of D/A Converters

Item	RX23T (DA)	RX66T (R12DAb)
Resolution	8 bits	12 bits
Output channels	1 channel	2 channels
Measure against mutual interference between analog modules	—	Measure against interference between D/A and A/D conversion D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable signal from the 12-bit A/D converter (unit 2). Therefore, the degradation of A/D conversion accuracy due to interference is reduced by controlling the timing in which the 12-bit D/A converter inrush current occurs, with the enable signal.
Low power consumption function	Ability to specify module stop state.	Ability to transition to module stop state.
Event linking function (input)	—	DA0 conversion can be started when an event signal is input.
Destination selection	—	Outputs to the external pin and to the comparator C are separately controllable.

Table 2.74 Comparison of D/A Converter Registers

Register	Bit	RX23T (DA)	RX66T (R12DAb)
DADRm	—	D/A data register m (m = 0)	D/A data register m (m = 0, 1)
DACR	DAE	—	D/A enable bit
	DAOE1	—	D/A output enable 1
DAADSCR	—	—	D/A A/D synchronous start control register
DADSELR	—	—	D/A destination select register

2.26 Comparator C

Table 2.75 is a comparative overview of the comparator C modules, and Table 2.76 is a comparison of comparator C registers.

Table 2.75 Comparative Overview of Comparator C Modules

Item	RX23T (CMPC)	RX66T (CMPC)
Number of channels	3 channels (comparator C0 to comparator C2)	6 channels (comparator C0 to comparator C5)
Analog input voltages	• Input voltage to the CMPCnm pin (n = channel number; m = 0 to 2) • Internal reference voltage	• Input voltage from the CMPCnm pin (n = channel number; m = 0 to 3)
Reference input voltage	Input voltage to the CVREFC0/CVREFC1 pin or on-chip D/A converter output voltage	Input voltage from the CVREFC0/CVREFC1 pin or on-chip D/A converter 0 output voltage or on-chip D/A converter 1 output voltage
Comparison result	The comparison result can be output externally.	The comparison result can be output externally.
Digital filter function	• One of three sampling periods can be selected. • The filter function can also be disabled. • A noise-filtered signal can be used to generate the interrupt request output, POE source output, and the signal can be used to read the comparison result via registers.	• One of three sampling periods can be selected. • The filter function can also be disabled. • A noise-filtered signal can be used to generate the interrupt request output, event output to the ELC, and POE source output*1, and the signal can be used to read the comparison result via registers.
Interrupt request	• An interrupt request is generated upon detecting a valid edge of the comparison result. • Rising edge, falling edge, or both edges of the comparison result can be selected.	• An interrupt request is generated upon detecting a valid edge of the comparison result. • A valid edge can be selected from a rising or a falling edge or both edges.
Low power consumption function	Ability to transition to module stop state.	Ability to transition to module stop state.

Note: 1. The POE only uses the level detection signal, and the POEG uses the level detection and edge detection signals.

Table 2.76 Comparison of Comparator C Registers

Register	Bit	RX23T (CMPC)	RX66T (CMPC)
CMPSEL0	CMPSEL [3:0]	Comparator input select bits • Comparator C0 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC00 selected 0 0 1 0: CMPC01 selected 0 1 0 0: CMPC02 selected 1 0 0 0: CMPC03 selected Settings other than the above are prohibited. • Comparator C1 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC10 selected 0 0 1 0: CMPC11 selected 0 1 0 0: CMPC12 selected 1 0 0 0: CMPC13 selected Settings other than the above are prohibited. • Comparator C2 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC20 selected 0 0 1 0: CMPC21 selected 0 1 0 0: CMPC22 selected 1 0 0 0: CMPC23 selected Settings other than the above are prohibited. • Comparator C3 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC30 selected 0 0 1 0: CMPC31 selected 0 1 0 0: CMPC32 selected 1 0 0 0: CMPC33 selected Settings other than the above are prohibited.	Comparator input select bits • Comparator C0 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC00 selected 0 0 1 0: CMPC01 selected 0 1 0 0: CMPC02 selected 1 0 0 0: CMPC03 selected Settings other than the above are prohibited. • Comparator C1 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC10 selected 0 0 1 0: CMPC11 selected 0 1 0 0: CMPC12 selected 1 0 0 0: CMPC13 selected Settings other than the above are prohibited. • Comparator C2 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC20 selected 0 0 1 0: CMPC21 selected 0 1 0 0: CMPC22 selected 1 0 0 0: CMPC23 selected Settings other than the above are prohibited. • Comparator C3 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC30 selected 0 0 1 0: CMPC31 selected 0 1 0 0: CMPC32 selected 1 0 0 0: CMPC33 selected Settings other than the above are prohibited. • Comparator C4 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC40 selected 0 0 1 0: CMPC41 selected 0 1 0 0: CMPC42 selected 1 0 0 0: CMPC43 selected Settings other than the above are prohibited.

Register	Bit	RX23T (CMPC)	RX66T (CMPC)
CMPSEL0	CMPSEL [3:0]		• Comparator C5 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC50 selected 0 0 1 0: CMPC51 selected 0 1 0 0: CMPC52 selected 1 0 0 0: CMPC53 selected Settings other than the above are prohibited.
CMPSEL1	CVRS[1:0] (RX23T) CVRS[3:0] (RX66T)	Reference input voltage select bits • Comparator C0, Comparator C1 b1 b0 0 0: No input 0 1: Input voltage to the CVREFC1 pin selected as reference input voltage 1 0: On-chip D/A converter output voltage selected as reference input voltage Settings other than the above are prohibited. • Comparator C2 b1 b0 0 0: No input 0 1: Input voltage to the CVREFC0 pin selected as reference input voltage 1 0: On-chip D/A converter output voltage selected as reference input voltage Settings other than the above are prohibited.	Reference input voltage select bits b3 b0 0 0 0 0: No input 0 0 0 1: On-chip D/A converter 1 output voltage selected as reference input voltage 0 0 1 0: On-chip D/A converter 0 output voltage selected as reference input voltage 0 1 0 0: Input voltage to the CVREFC1 pin selected as reference input voltage 1 0 0 0: Input voltage to the CVREFC0 pin selected as reference input voltage Settings other than the above are prohibited.
CMPC0.CMPIOC	VREFEN	Internal reference voltage on/off control bit	—

2.27 Data Operation Circuit

Table 2.77 is a comparative overview of data operation circuit.

Table 2.77 Comparative Overview of Data Operation Circuit

Item	RX23T (DOC)	RX66T (DOC)
Data operation functions	16-bit data comparison, addition, and subtraction	16-bit data comparison, addition, and subtraction
Lower power consumption function	Module stop state can be set.	Module stop state can be set.
Interrupts	• The compared values either match or mismatch • The result of data addition is greater than FFFFh • The result of data subtraction is less than 0000h	• The compared values either match or mismatch • The result of data addition is greater than FFFFh • The result of data subtraction is less than 0000h
Event linking function (output)	—	• The compared values either match or mismatch • The result of data addition is greater than FFFFh • The result of data subtraction is less than 0000h

2.28 RAM

Table 2.78 is a comparative overview of RAM, and Table 2.79 is a comparison of RAM registers.

Table 2.78 Comparative Overview of RAM

Item	RX23T (RAM)	RX66T Without ECC Error Correction (RAM)	RX66T With ECC Error Correction (ECCRAM)
Capacity	12 KB (RAM0: 12 KB)	• 64 KB • 128 KB	16 KB
Address	RAM0: 0000 0000h to 0000 27FFh 0000 4000h to 0000 4A7Fh	• RAM capacity: 64 KB 0000 0000h to 0000 FFFFh • RAM capacity: 128 KB 0000 0000h to 0001 FFFFh	00FF C000h to 00FF FFFFh
Memory bus	Memory bus 1	Memory bus 1	Memory bus 3
Access	• Single-cycle access is possible for both reading and writing. • On-chip RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. • Enabling or disabling of the RAM is selectable.	• Enabling or disabling of the ECC function is selectable. [When MEMWAIT is set to 0] • The ECC function is disabled: Access takes two cycles whether for reading or writing. • The ECC function is enabled (when no error has occurred): Access takes two cycles whether for reading or writing. • The ECC function is enabled (when an error has occurred): Access takes three cycles whether for reading or writing. [When MEMWAIT is set to 1] • The ECC function is disabled: Access takes three cycles whether for reading or writing. • The ECC function is enabled (when no error has occurred): Reading takes three cycles and writing takes four cycles. • The ECC function is enabled (when an error has occurred): Access takes five cycles whether for reading or writing.

Item	RX23T (RAM)	RX66T	
		Without ECC Error Correction (RAM)	With ECC Error Correction (ECCRAM)
Data retention function	—	Not available in deep software standby mode	
Low power consumption function	The module stop state is selectable for RAM0.	Transition to the module stop state is separately possible for the RAM and ECCRAM.	
Error checking	—	• Detection of 1-bit errors • A non-maskable interrupt or interrupt is generated in response to an error.	• ECC error correction: Correction of 1-bit errors and detection of 2-bit errors • A non-maskable interrupt or interrupt is generated in response to an error.

Table 2.79 Comparison of RAM Registers

Register	Bit	RX23T (RAM)	RX66T (RAM, ECCRAM)
ECCRAMMODE	—	—	ECCRAM operating mode control register
ECCRAM2STS	—	—	ECCRAM 2-bit error status register
ECCRAM1STSEN	—	—	ECCRAM 1-bit error information update enable register
ECCRAM1STS	—	—	ECCRAM 1-bit error status register
ECCRAMPRCR	—	—	ECCRAM protection register
ECCRAM2ECAD	—	—	ECCRAM 2-bit error address capture register
ECCRAM1ECAD	—	—	ECCRAM 1-bit error address capture register
ECCRAMPRCR2	—	—	ECCRAM protection register 2
ECCRAMETST	—	—	ECCRAM test control register
RAMMODE	—	—	RAM operating mode control register
RAMSTS	—	—	RAM error status register
RAMECAD	—	—	RAM error address capture register
RAMPRCR	—	—	RAM protection register

2.29 Flash Memory

Table 2.80 is a comparative overview of flash memory, and Table 2.81 is a comparison of flash memory registers.

Table 2.80 Comparative Overview of Flash Memory

	RX23T	**RX66T**	
Item	**ROM**	**Code Flash Memory**	**Data Flash Memory**
Memory capacity	• User area: Max. 128 KB • Extra area: Stores the start-up area information, access window information, and unique ID	• User area: Max. 1 MB • User boot area: 32 KB	• Data area: 32 KB
Address	• Products with capacity of 128 KB: FFFE 0000h to FFFF FFFFh • Products with capacity of 64 KB: FFFF 0000h to FFFF FFFFh	User area • Products with capacity of 1 MB: FFF0 0000h to FFFF FFFFh • Products with capacity of 512 KB: FFF8 0000h to FFFF FFFFh • Products with capacity of 256 KB: FFFC 0000h to FFFF FFFFh User boot area FF7F 8000h to FF7F FFFFh	0010 0000h to 0010 7FFFh
ROM cache	—	• Capacity: 8 KB • Mapping method: direct mapping • Line size: 16 bytes	—

Item	RX23T	RX66T	
	ROM	Code Flash Memory	Data Flash Memory
Read cycle	No ROM wait cycles when ICLK ≤ 32 MHz, ROM wait cycle when ICLK > 32 MHz	• While ROM cache operation is enabled: When the cache is hit, one cycle; When the cache is missed, — One to two cycles if ICLK ≤ 120 MHz — Two to three cycles if ICLK > 120 MHz • When ROM cache operation is disabled: — One cycle if ICLK ≤ 120 MHz — Two cycles if ICLK > 120 MHz	A read operation takes eight cycles of FCLK for 16-bit or 8-bit access.
Value after erasure	ROM: FFh	FFh	Undfined
Programming/ erasing method	Programming and erasing using software commands • The following commands are implemented: Program, blank check, block erase, all-block erase • The following commands are implemented for programming the extra area: Start-up area information program, access window information program	• Programming and erasing the code flash memory/data flash memory is handled by the FACI commands specified in the FACI command issuing area (007E 0000h). • Programming/erasure through transfer by a flash-memory programmer via a serial interface (serial programming) • Programming/erasure of flash memory by a user program (self-programming)	
Security function	Protects against illicit tampering with or reading out of data in flash memory	Protects against illicit tampering with or reading out of data in flash memory	
Protection function	Protects against erroneous rewriting of the flash memory	Protects against erroneous rewriting of the flash memory	
Trusted memory (TM) function	—	Protects against illicit reading of blocks 8 and 9 in the code flash memory	
Background operation (BGO)	—	The user area can be read while the data area is being programmed or erased.	
Units of programming and erasure	• Units of programming for the user area: 8 bytes • Units of erasure for the user area: Block units	• Units of programming for the user area or user boot area: 256 bytes • Units of erasure for the user area: Block units	• Unit of programming for the data area: 4 bytes • Unit of erasure for the data area: Block units
Other functions	—	Interrupts can be accepted during self-programming.	

Item	RX23T	RX66T	
	ROM	Code Flash Memory	Data Flash Memory
On-board programming (Serial programming/ Self-programming)	• Boot mode (SCI interface) — Channel 1 of the serial communications interface (SCI1) is used for asynchronous serial communication. — The user area is rewritable.	• Programming/erasure in boot mode (for the SCI interface) — The asynchronous serial interface (SCI1) is used. — The transfer rate is adjusted automatically. — The user boot area can also be programmed or erased.	
		• Programming/erasure in boot mode (for the USB interface) — USBb is used. — Dedicated hardware is not required, so direct connection to a PC is possible.	
	• Boot mode (FINE interface) — The FINE is used. — The user area is rewritable.	• Programming/erasure in boot mode (for the FINE interface) — FINE is used.	
		• Programming/erasure in user boot mode — Able to create original boot programs of the user's making.	
	• Self-programming (single-chip mode): — The user area is rewritable using the flash rewrite routine in the user program.	• Programming/erasure by self-programming — This allows user area/data area programming and erasure without resetting the system.	
Off-board programming (Programming and Erasure by Parallel Programmer)	The user area is rewritable using a flash programmer compatible with this MCU.	Programming and erasure of the user area and user boot area by using a parallel programmer is possible.	Programming or erasure of the data area by a parallel programmer is not possible.
Unique ID	A 16-byte ID code provided for each MCU	A 12-byte ID code provided for each MCU	

Table 2.81 Comparison of Flash Memory Registers

Register	Bit	RX23T	RX66T
ROMCE	—	—	ROM cache enable register
ROMCIV	—	—	ROM cache invalidate register
NCRGn	—	—	Non-cacheable area n address register (n = 0, 1)
NCRCn	—	—	Non-cacheable area n setting register (n = 0, 1)
FWEPROR	—	—	Flash P/E protect register
FASTAT	—	—	Flash access status register
FAEINT	—	—	Flash access error interrupt enable register
FRDYIE	—	—	Flash ready interrupt enable register
FSADDR	—	—	FACI command processing start address register
FEADDR	—	—	FACI command processing end address register
FSTATR0 (RX23T) FSTATR (RX66T)	—	Flash status register 0 FSTATR0 is an 8-bit register.	Flash status register FSTATR is a 32-bit register.
	ERERR (RX23T) ERSERR (RX66T)	Erase error flag (b0)	Erasure error flag (b13)
	PRGERR	Program error flag (b1)	Programming error flag (b12)
	BCERR	Blank check error flag	—
	ILGLERR	Illegal command error flag (b4)	Illegal error command flag (b14)
	EILGLERR	Extra area illegal command error flag	—
	FLWEERR	—	Flash write/erase protect error flag
	PRGSPD	—	Programming suspend status flag
	ERSSPD	—	Erasure suspend status flag
	DBFULL	—	Data buffer full flag
	SUSRDY	—	Suspend ready flag
	FRDY	—	Flash ready flag
FENTRYR	FENTRY0 (RX23T) FENTRYC (RX66T)	ROM P/E mode entry 0 bits	Code flash memory P/E mode entry bit
	FENTRYD	—	Data flash memory P/E mode entry bit
	FEKEY[7:0] (RX23T) KEY[7:0] (RX66T)	Key code bits	Key code bits
FPROTR	—	—	Flash protection register
FSUINITR	—	—	Flash sequencer set-up initialization register
FLKSTAT	—	—	Lock bit status register
FCMDR	—	—	FACI command register
FPESTAT	—	—	Flash P/E status register

Register	Bit	RX23T	RX66T
FBCCNT	—	—	Data flash blank check control register
FBCSTAT	—	—	Data flash blank check status register
FPSADDR	—	—	Data flash programming start address register
FCPSR	—	—	Flash sequencer processing switching register
FPCKAR	—	—	Flash sequencer processing clock frequency notification register
UIDRn	—	Unique ID register n (n = 0 to 3)	Unique ID register n (n = 0 to 2)
FPR	—	Protection unlock register	—
FPSR	—	Protection unlock status register	—
FPMCR	—	Flash P/E mode control register	—
FISR	—	Flash initial setting register	—
FRESETR	—	Flash reset register	—
FASR	—	Flash area select register	—
FCR	—	Flash control register	—
FEXCR	—	Flash extra area control register	—
FSARH	—	Flash processing start address register H	—
FSARL	—	Flash processing start address register L	—
FEARH	—	Flash processing end address register H	—
FEARL	—	Flash processing end address register L	—
FWBn	—	Flash write buffer n register (n = 0 to 3)	—
FSTATR1	—	Flash status register 1	—
FEAMH	—	Flash error address monitor register H	—
FEAML	—	Flash error address monitor register L	—
FSCMR	—	Flash start-up setting monitor register	—
FAWSMR	—	Flash access window start address monitor register	—
FAWEMR	—	Flash access window end address monitor register	—

2.30 Packages

As indicated in Table 2.82, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage.

Table 2.82 Packages

Package Type	Renesas Code	
	RX23T	**RX66t**
144-pin LFQFP	✕	○
112-pin LQFP	✕	○
100-pin LFQFP	✕	○
80-pin LQFP	✕	○
80-pin LFQFP	✕	○
52-pin LQFP	○	✕

○: Package available (Renesas code omitted); ✕: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by **blue text**. Items that exists on both groups with different specifications are indicated by **red text**. **Black text** indicates there is no differences in the item's specifications between groups.

3.1 64-Pin Package

Table 3.1 is comparative listing of the pin functions of 64-pin package products.

Table 3.1 Comparative Listing of 64-Pin Package Pin Functions

64-Pin	RX23T (64-Pin LFQFP)	RX66T (64-Pin LFQFP)
1	P02/CTS1#/RTS1#/SS1#/ADST0/IRQ5	EMLE
2	P00/IRQ2	UB/P00/MTIOC9A/MTIOC9A#/CACREF/RXD9/SMISO9/SSCL9/RXD12/SMISO12/SSCL12/RXDX12/IRQ2/ADST1/COMP0
3	VCL	VCL
4	P01/CACREF/IRQ4	MD/FINED
5	MD/FINED	P01/MTIOC9C/MTIOC9C#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE12#/TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/IRQ4/ADST2/COMP1
6	RES#	RES#
7	XTAL/P37	XTAL/P37
8	VSS	VSS
9	EXTAL/P36	EXTAL/P36
10	VCC	VCC
11	PE2/POE10#/NMI	PE2/POE10#/NMI
12	PD7/TMRI1/SSLA1	TRST#/PD7/MTIOC9A/MTIOC9A#/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/SSDA5/SSLA1/CTX0/IRQ8
13	PD6/TMO1/SSLA0/CTS1#/RTS1#/SS1#/ADST0/IRQ5	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/CTS1#/RTS1#/SS1#/CTS11#/RTS11#/SS11#/SSLA0/IRQ5/ADST0
14	PD5/TMRI0/RXD1/SMISO1/SSCL1/IRQ3	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/TMRI0/TMRI6/RXD1/SMISO1/SSCL1/RXD11/SMISO11/SSCL11/IRQ6
15	PD4/TMCI0/SCK1/IRQ2	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/TMCI0/TMCI6/SCK1/SCK11/IRQ2
16	PD3/TMO0/TXD1/SMOSI1/SSDA1	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/TMO0/TXD1/SMOSI1/SSDA1/TXD11/SMOSI11/SSDA11
17	PB7/SCK5	PB6/GTIOC2A/GTIOC2A#/RXD5/SMISO5/SSCL5/RXD11/SMISO11/SSCL11/RXD12/SMISO12/SSCL12/RXDX12/CRX0/IRQ2
18	PB6/RXD5/SMISO5/SSCL5/IRQ5	PB5/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/SSDA11/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/CTX0

64-Pin	RX23T (64-Pin LFQFP)	RX66T (64-Pin LFQFP)
19	PB5/TXD5/SMOSI5/SSDA5	PB4/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE8#/CTS5#/RTS5#/SS5#/SCK11/CTS11#/RTS11#/SS11#/IRQ3-DS
20	VCC	PB3/MTIOC0A/MTIOC0A#/CACREF/SCK6/RSPCKA/IRQ9
21	PB4/POE8#/IRQ3	PB2/MTIOC0B/MTIOC0B#/GTADSM0/TMRI0/TXD6/SMOSI6/SSDA6/SDA0/ADSM0
22	VSS	PB1/MTIOC0C/MTIOC0C#/GTADSM1/TMCI0/RXD6/SMISO6/SSCL6/SCL0/IRQ4/ADSM1
23	PB3/MTIOC0A/CACREF/SCK5/RSPCKA	PB0/MTIOC0D/MTIOC0D#/TMO0/TXD6/SMOSI6/SSDA6/CTS11#/RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
24	PB2/MTIOC0B/ADSM0/TXD5/SMOSI5/SSDA5/SDA0	VCC
25	PB1/MTIOC0C/RXD5/SMISO5/SSCL5/SCL0/IRQ2	P96/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE4#/CTS8#/RTS8#/SS8#/IRQ4-DS
26	PB0/MTIOC0D/MOSIA	VSS
27	PA3/MTIOC2A/SSLA0	P95/MTIOC6B/MTIOC6B#/GTIOC4A/GTIOC7A/GTIOC4A#/GTIOC7A#
28	PA2/MTIOC2B/CTS5#/RTS5#/SS5#/SSLA1/IRQ4	P94/MTIOC7A/MTIOC7A#/GTIOC5A/GTIOC8A/GTIOC5A#/GTIOC8A#
29	P94/MTIOC0C/TMO1/MISOA/IRQ1	P93/MTIOC7B/MTIOC7B#/GTIOC6A/GTIOC9A/GTIOC6A#/GTIOC9A#
30	P93/MTIOC0B/TMRI1/SCK5/RSPCKA/IRQ0	P92/MTIOC6D/MTIOC6D#/GTIOC4B/GTIOC7B/GTIOC4B#/GTIOC7B#
31	P92/TMCI1/SSLA2	P91/MTIOC7C/MTIOC7C#/GTIOC5B/GTIOC8B/GTIOC5B#/GTIOC8B#
32	P91/SSLA3	P90/MTIOC7D/MTIOC7D#/GTIOC6B/GTIOC9B/GTIOC6B#/GTIOC9B#
33	P76/MTIOC4D	P76/MTIOC4D/MTIOC4D#/GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#
34	P75/MTIOC4C	P75/MTIOC4C/MTIOC4C#/GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#
35	P74/MTIOC3D	P74/MTIOC3D/MTIOC3D#/GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#
36	P73/MTIOC4B	P73/MTIOC4B/MTIOC4B#/GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#
37	P72/MTIOC4A	P72/MTIOC4A/MTIOC4A#/GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#
38	P71/MTIOC3B	P71/MTIOC3B/MTIOC3B#/GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#
39	P70/POE0#/IRQ5	P70/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE0#/CTS9#/RTS9#/SS9#/IRQ5-DS
40	P33/MTIOC3A/MTCLKA/SSLA3	VCC
41	P32/MTIOC3C/MTCLKB/SSLA2	VSS
42	VCC	P22/MTIC5W/MTCLKD/MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/TMO4/RXD8/SMISO8/SSCL8/RXD12/SMISO12/SSCL12/RXDX12/MISOA/CRX0/IRQ10/ADTRG2#/COMP2

64-Pin	RX23T (64-Pin LFQFP)	RX66T (64-Pin LFQFP)
43	P31/MTIOC0A/MTCLKC/SSLA1	P21/MTIOC9A/MTCLKA/MTIOC9A#/ MTCLKA#/TMCI4/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ MOSIA/IRQ6-DS/AN217/ADTRG1#/COMP5
44	VSS	P20/MTIOC9C/MTCLKB/MTIOC9C#/ MTCLKB#/TMRI4/CTS8#/RTS8#/SS8#/ SCK8/RSPCKA/IRQ7-DS/AN216/ADTRG0#/ COMP4
45	P30/MTIOC0B/MTCLKD/SSLA0	P65/IRQ9/AN211/CMPC53/DA1
46	P24/MTIC5U/TMCI2/RSPCKA/COMP0/IRQ3	P64/IRQ8/AN210/CMPC33/DA0
47	P23/MTIC5V/CACREF/TMO2/MOSIA/ COMP1/IRQ4	AVCC2
48	P22/MTIC5W/TMRI2/MISOA/COMP2/IRQ2	AVSS2
49	P47/AN007/CMPC12/CMPC22	P54/IRQ2/AN202/CMPC22
50	P46/AN006/CMPC02	P53/IRQ1/AN201/CMPC12
51	P45/AN005/CMPC21	P52/IRQ0/AN200/CMPC02
52	P44/AN004/CMPC11	P46/AN102/CMPC50/CMPC51
53	P43/AN003/CMPC01	P45/AN101/CMPC40/CMPC41
54	P42/AN002/CMPC20	P44/AN100/CMPC30/CMPC31
55	P41/AN001/CMPC10	PH4/AN107/PGAVSS1
56	P40/AN000/CMPC00	P42/AN002/CMPC20/CMPC21
57	AVCC0	P41/AN001/CMPC10/CMPC11
58	VREFH0	P40/AN000/CMPC00/CMPC01
59	VREFL0	PH0/AN007/PGAVSS0
60	AVSS0	AVCC1
61	P11/MTIOC3A/MTCLKC/TMO3/IRQ1/AN016/ CVREFC0	AVCC0
62	P10/MTCLKD/TMRI3/IRQ0/AN017/CVREFC1	AVSS0
63	PA5/MTIOC1A/TMCI3/MISOA	AVSS1
64	PA4/MTIOC1B/RSPCKA/ADTRG0#	P11/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/MTIOC9D/GTIOC3B/GTETRGA/ GTIOC3B#/GTETRGC/TMO3/POE9#/ IRQ1-DS

3.2 48-Pin Package

Table 3.2 is comparative listing of the pin functions of 48-pin package products.

Table 3.2 Comparative Listing of 48-Pin Package Pin Functions

48-Pin	RX23T (48-Pin LFQFP)	RX66T (48-Pin LFQFP)
1	VCL	UB/P00/MTIOC9A/MTIOC9A#/CACREF/RXD9/SMISO9/SSCL9/RXD12/SMISO12/SSCL12/RXDX12/IRQ2/ADST1/COMP0
2	MD/FINED	VCL
3	RES#	MD/FINED
4	XTAL/P37	RES#
5	VSS	XTAL/P37
6	EXTAL/P36	VSS
7	VCC	EXTAL/P36
8	PE2/POE10#/NMI	VCC
9	PD6/TMO1/SSLA0/CTS1#/RTS1#/SS1#/ADST0/IRQ5	PE2/POE10#/NMI
10	PD5/TMRI0/RXD1/SMISO1/SSCL1/IRQ3	PD7/MTIOC9A/MTIOC9A#/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/SSDA5/SSLA1/CTX0/IRQ8
11	PD4/TMCI0/SCK1/IRQ2	PD5/GTIOC1A/GTETRGA/GTIOC1A#/TMRI0/TMRI6/RXD1/SMISO1/SSCL1/RXD11/SMISO11/SSCL11/IRQ6
12	PD3/TMO0/TXD1/SMOSI1/SSDA1	PD3/GTIOC2A/GTETRGC/GTIOC2A#/TMO0/TXD1/SMOSI1/SSDA1/TXD11/SMOSI11/SSDA11
13	PB6/RXD5/SMISO5/SSCL5/IRQ5	PB6/GTIOC2A/GTIOC2A#/RXD5/SMISO5/SSCL5/RXD11/SMISO11/SSCL11/RXD12/SMISO12/SSCL12/RXDX12/CRX0/IRQ2
14	PB5/TXD5/SMOSI5/SSDA5	PB5/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/SSDA11/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/CTX0
15	VCC	PB4/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE8#/CTS5#/RTS5#/SS5#/SCK11/CTS11#/RTS11#/SS11#/IRQ3-DS
16	PB4/POE8#/IRQ3	PB3/MTIOC0A/MTIOC0A#/CACREF/SCK6/RSPCKA/IRQ9
17	PB3/MTIOC0A/CACREF/SCK5/RSPCKA	PB2/MTIOC0B/MTIOC0B#/GTADSM0/TMRI0/TXD6/SMOSI6/SSDA6/SDA0/ADSM0
18	PB2/MTIOC0B/ADSM0/TXD5/SMOSI5/SSDA5/SDA0	PB1/MTIOC0C/MTIOC0C#/GTADSM1/TMCI0/RXD6/SMISO6/SSCL6/SCL0/IRQ4/ADSM1
19	PB1/MTIOC0C/RXD5/SMISO5/SSCL5/SCL0/IRQ2	PB0/MTIOC0D/MTIOC0D#/TMO0/TXD6/SMOSI6/SSDA6/CTS11#/RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
20	PB0/MTIOC0D/MOSIA	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/SMISO6/SSCL6/MISOA/IRQ1/ADTRG1#
21	PA3/MTIOC2A/SSLA0	PA3/MTIOC2A/MTIOC2A#/GTADSM0/TMRI7/TXD9/SMOSI9/SSDA9/SSLA0
22	PA2/MTIOC2B/CTS5#/RTS5#/SS5#/SSLA1/IRQ4	VCC
23	P94/MTIOC0C/TMO1/MISOA/IRQ1	VSS

48-Pin	RX23T (48-Pin LFQFP)	RX66T (48-Pin LFQFP)
24	P93/MTIOC0B/TMRI1/SCK5/RSPCKA/IRQ0	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#
25	P76/MTIOC4D	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC6B/GTIOC2B#/GTIOC6B#
26	P75/MTIOC4C	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC5B/GTIOC1B#/GTIOC5B#
27	P74/MTIOC3D	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC4B/GTIOC0B#/GTIOC4B#
28	P73/MTIOC4B	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC6A/GTIOC2A#/GTIOC6A#
29	P72/MTIOC4A	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC5A/GTIOC1A#/GTIOC5A#
30	P71/MTIOC3B	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC4A/GTIOC0A#/GTIOC4A#
31	P70/POE0#/IRQ5	VCC
32	VCC	VSS
33	VSS	P65/IRQ9/AN211/CMPC53/DA1
34	P24/MTIC5U/TMCI2/RSPCKA/COMP0/IRQ3	P64/IRQ8/AN210/CMPC33/DA0
35	P23/MTIC5V/CACREF/TMO2/MOSIA/COMP1/ IRQ4	AVCC2
36	P22/MTIC5W/TMRI2/MISOA/COMP2/IRQ2	AVSS2
37	P47/AN007/CMPC12/CMPC22	P62/IRQ6/AN208/CMPC43
38	P46/AN006/CMPC02	P44/AN100/CMPC30/CMPC31
39	P45/AN005/CMPC21	P43/AN003
40	P44/AN004/CMPC11	P42/AN002/CMPC20/CMPC21
41	P43/AN003/CMPC01	P41/AN001/CMPC10/CMPC11
42	P42/AN002/CMPC20	P40/AN000/CMPC00/CMPC01
43	P41/AN001/CMPC10	AVCC1
44	P40/AN000/CMPC00	AVCC0
45	AVCC0	AVSS0
46	AVSS0	AVSS1
47	P11/MTIOC3A/MTCLKC/TMO3/IRQ1/AN016/ CVREFC0	P11/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/MTIOC9D/GTIOC3B/GTETRGA/ GTIOC3B#/GTETRGC/TMO3/POE9#/ IRQ1-DS
48	P10/MTCLKD/TMRI3/IRQ0/AN017/CVREFC1	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0-DS

4. Important Information when Migrating Between MCUs

This section presents important information on differences between the RX23T Group and the RX66T Group. 4.1, Notes on Pin Design, presents information regarding the hardware, and 4.2, Notes on Functional Design, presents information regarding the software.

4.1 Notes on Pin Design

4.1.1 VCL Pin (External Capacitor)

Connect a smoothing capacitor with a capacitance rating of 4.7 µF to the VCL pin to stabilize the internal power supply, for the RX23T Group, or 0.47 µF, for the RX66T Group.

4.1.2 Mode Setting Pins

The mode setting pins after reset cancellation are the MD pin only on the RX23T Group and the MD pin and UB pin (multiplexed with P00) on the RX66T Group.

4.1.3 General I/O Ports

If you do not plan to use port 4 on the RX23T Group, set the pins to input and connect each pin via a resistor to VCC (pulled up) or to VSS (pulled down). If port 4 will not be used on the RX66T Group, set the pins to input and connect each pin via a resistor to AVCC (pulled up) or to AVSS (pulled down). Alternatively, the pins can be set to output and left open.

Note that even when the pins are set to output and left open they revert to the input setting immediately following cancellation of a reset, and that the pin voltage levels are unstable during the period they are set to input. This could cause an increase in the power supply current in some cases.

4.1.4 PGA Pseudo-Differential Input Pins (P40 to P42, P44 to P46, PH0, and PH4)

On the RX66T Group input of negative voltage to the PGA pseudo-differential input pins is possible from the reset state. Therefore, in order to make use of the functions of the P40 to P42, P44 to P46, PH0, and PH4 pins after cancellation of a reset, it is necessary to modify the settings of the PGA-related registers, regardless of whether or not the PGA is actually being used.

For details, refer to the descriptions of the VOLSR.PGAVLS bit, the initial setting sequence of the A/D converter, and the PIDR register in RX66T Group User's Manual: Hardware. Note that there is no need to change the above settings on products without PGA pseudo-differential input.

4.1.5 Inserting Decoupling Capacitor between AVCC and AVSS Pins

To prevent destruction of the analog input pins (AN000 to AN007, AN100 to AN107, AN200 to AN211, AN216, and AN117) by abnormal voltage such as an excessive surge, insert capacitors between AVCCn and AVSSn, and connect a protective circuit to protect the analog input pins (AN000 to AN007, AN100 to AN107, AN200 to AN211, AN216, and AN117).

For details, refer to "Notes on Noise Prevention" in the 12-Bit A/D Converter section of RX66T Group User's Manual: Hardware, listed in 5, Reference Documents.

4.1.6 Capacitors Connected to Analog Power Supply Pins

If you plan to use an A/D conversion clock frequency higher than 40 MHz on the RX66T Group, add a capacitor with the capacitance indicated below between the 0.1 µF capacitor and the power supply pin.

- Products with RAM capacity of 64 KB: 1,000 pF
- Products with RAM capacity of 128 KB: 0.01 µF

4.2 Notes on Functional Design

Some software that runs on the RX23T Group is compatible with the RX66T Group. Nevertheless, appropriate caution must be exercised due to differences in aspects such as operation timing and electrical characteristics.

Software-related considerations regarding function settings that differ between the RX66T Group and RX23T Group are as follows:

For differences between modules and functions, refer to 2, Comparative Overview of Specifications. For further information, refer to the User's Manual: Hardware of each MCU group, listed in 5, Reference Documents.

4.2.1 RIIC Operating Voltage Setting

When using the RIIC on the RX66T Group, it is necessary to specify the power supply voltage range in order to maintain the desired slope characteristics.

The default value for VCC is 4.5 V or greater. If you plan to use a VCC voltage lower than 4.5 V, change the voltage range before starting RIIC operation. For details, refer to the description of the VOLSR.RICVLS bit in RX66T Group User's Manual: Hardware.

4.2.2 USB Operating Voltage Setting

To use the USB module on the RX66T Group, set the USB power supply control bit to 1 before starting USB operation. For details, refer to the description of the VOLSR.USBVON bit in RX66T Group User's Manual: Hardware.

4.2.3 Voltage Level Settings

On the RX66T Group it is necessary to make appropriate settings to the voltage level setting register (VOLSR), voltage detection level select register (LVDLVLR), and option function select register 1 (OFS1) to match the operating voltage. Do not fail to make these settings in your software programs.

4.2.4 Clock Frequency Settings

On the RX23T Group there is a restriction on the clock frequency settings requiring that ICLK ≥ PCLK, but on the RX66T Group the settings should be made as indicated below. In addition, on the RX66T Group it is necessary to modify the setting of the MEMWAIT register if the ICLK frequency is higher than 120 MHz.

Clock frequency setting restrictions: ICLK ≥ BCLK, PCLKC ≥ PCLKA ≥ PCLKB
Clock frequency ratio restrictions: (N is an integer value):
ICLK:FCLK = N:1 or 1:N
ICLK:PCLKA = N:1 or 1:N
ICLK:PCLKB = N:1 or 1:N
ICLK:PCLKC = N:1 or 1:N
ICLK:PCLKD = N:1 or 1:N
PCLKA:PCLKC = 1:1 or 1:2
PCLKB:PCLKD = 1:1 or 2:1 or 4:1 or 1:2

4.2.5 Operation of Main Clock Oscillation Stop Detection Function

When the oscillation stop detection function detects that the main clock oscillator has stopped, it outputs a LOCO clock from the low-speed on-chip oscillator as the clock source of the system clock in place of the main clock and PLL clock.

Note that on the RX66T Group, if the HOCO clock is selected as the PLL clock source and the PLL clock is selected as the clock source of the system clock, the system clock does not switch to the LOCO clock even if oscillation stop of the main clock is detected.

4.2.6 PLL Circuit

The frequency multiplication factor of the PLL circuit can be set to ×4 to ×10 (in ×0.5 increments) on the RX23T Group and to ×10 to ×30 (in ×0.5 increments) on the RX66T Group. To use the PLL circuit, first change the setting of the PLLCR.STC[5:0] bits to an appropriate value. In addition, PLL clock switching can be implemented in software on the RX66T Group.

4.2.7 MTU3d/GPTW Operating Frequency

On the RX66T Group PCLKC is used as the count clock for the MTU3d and GPTW, and PCLKA is used as the bus clock. There are some restrictions on the allowable frequency combinations, so select frequency settings with care.

4.2.8 All-Module Clock Stop Mode

The RX23T Group does not have an all-module clock stop mode. In order to transition to all-module clock stop mode on the RX66T Group, it is necessary to write 1 to bits MSTPA24, MSTPA27, MSTPA29, and MSTPD0 to MSTPD7.

4.2.9 Input Buffer Control Using DIRQnE Bit (n = 0 to 15)

On the RX66T Group, the input buffers of pins IRQ0-DS to IRQ15-DS can be enabled by writing 1 to the corresponding low power consumption function DPSIERy.DIRQnE (y = 0 or 1, n = 0 to 15) bits. This causes input on these pins to be conveyed to the corresponding DPSIERy.DIRQnE (y = 0 or 1, n = 0 to 15) bits but not to the interrupt controller, peripheral modules, or I/O ports.

4.2.10 Software Configurable Interrupts

Interrupt sources have fixed vector numbers on the RX23T Group, but on the RX66T Group MTU and GPTW interrupt sources are associated with software configurable interrupt A, and these interrupt sources can be assigned to interrupt vector tables 208 to 255 by making settings in software configurable interrupt A source select register n (SLIARn).

4.2.11 Watchdog Timer and Independent Watchdog Timer

On the RX66T Group it is possible to select whether the WDT underflow and refresh error interrupts, and the IWDT underflow and refresh error interrupts, are maskable or non-maskable interrupts.

4.2.12 Initializing the Port Direction Register (PDR)

The method of initializing the PDR differs, even on products with the same pin count.

4.2.13 Note on Controlling General I/O Port Switching by POE3

On the RX66T Group, pins for which the corresponding bits in the PMMCRn register (n = 0 to 3) are set to 1 are switched to general I/O port pins when generation of an output disable request is specified by the POE3. Make sure to clear the corresponding bits in the POECRn register (n = 0 to 3) to 0 beforehand.

4.2.14 Buffer Register Setting Values in Complementary PWM Mode

When using the double buffering function in complementary PWM mode of multi-function timer pulse unit 3, the PWM output to the buffer registers (MTU3.TGRE, MTU4.TGRE, MTU4.TGRF, MTU6.TGRE, MTU7.TGRE, and MTU7.TGRF) should be set to “duty value − 1” on the RX23T Group, but on the RX66T Group a duty value should be specified for PWM output.

4.2.15 DMAC Activation by MTU

When the DMAC is activated by the MTU on the RX66T Group, the activation source is cleared when the DMAC requests ownership of the internal bus. Accordingly, depending on the state of the internal bus, there may be a period during which the DMAC is waiting to start the transfer even through the source has been cleared.

4.2.16 Count Clock Restrictions

On the RX66T Group the pulse width of the MTU's count clock source must be at least 1.5 PCLKC cycles, when counting single edges, or at least 2.5 PCLKC cycles, when counting both edges. A smaller pulse width may cause a malfunction.

In phase counting mode the phase difference and overlap of the two input clocks must be at least 1.5 PCLKC cycles and at least 2.5 PCLKC cycles, respectively.

4.2.17 Note on Timer Mode Register Settings when Using ELC Event Input

On the RX66T Group, when a setting is made in the MTU to specify an action in response to ELC event input, make sure that the timer mode register (TMDR) of the channel in question is set to the default value (00h).

4.2.18 Port Output Enable

The RX66T Group incorporates significant changes to the port output enable registers, compared to the RX23T Group. This results in a reduction in software compatibility.

4.2.19 Control of Output Disabling Request Issuance by Port Output Enable 3

When an output disabling request is generated on the RX66T Group, the pins for which the corresponding bits in the POECR1 to POECR3 and POECR7 registers have been set to 1 enter the high-impedance state and the pins for which the corresponding bits in the PMMCR0 to PMMCR3 registers have been set to 1 are switched to general I/O port operation.

If bits in both sets of registers corresponding to the same pins have been set to 1, the POECR1 to POECR3 and POECR7 registers take priority and the pins enter the high-impedance state.

After a switch to general I/O port operation, the pin state is determined by the settings of the PDR and PODR registers.

4.2.20 Active Level Setting with Inverted Output Enabled on MTU or GPTW

On the RX66T Group output from the MTU and GPTW can be set to either normal output or inverted output by making settings to the MPC.PmnPFS register.

When inverted MTU output is selected, the active level specified in the MTU.TOCR1j and MTU.TOCR2j (j = A and B) registers, and the active level of the signals output to the pins, are inverted. To use detection of simultaneous conduction in this case, specify the active level in the ALR1 and ALR2 registers, with reference to the signals output on the pins.

When inverted output is selected for the GPTW, the active level of the signals output to the pins is inverted. To use detection of simultaneous conduction in this case, specify the active level in registers ALR3 to ALR5, with reference to the signals output on the pins.

4.2.21 Reading Pins in High-Impedance State

When pins are placed in the high-impedance state by the POE on the RX66T Group, their level cannot be read. The value when read is undefined. To read the level of the pins, release them from the high-impedance state. This restriction does not apply when port switching control is selected instead of high-impedance control.

4.2.22 Note on Using POE and POEG Together

When using the POE and POEG together on the RX66T Group, do not apply control from both the POE and POEG to disable output on the same GPTW output pin.

4.2.23 I²C Bus Interface Noise Cancellation

The RX23T Group incorporates analog noise filters for the SCL and SDA lines, but the RX66T Group does not have analog noise filters.

4.2.24 12-Bit A/D Converter

The RX66T Group incorporates significant changes to the 12-bit A/D converter registers, compared to the RX23T Group. This results in a reduction in software compatibility.

4.2.25 Restrictions on Compare Function

The 12-bit A/D converter's compare function has the following restrictions on the RX66T Group:

1. Use of the self-diagnostic function and double trigger mode are not supported. (ADRD, ADDBLDR, ADDBLDRA, and ADDBLDRB are not covered by for the compare function.)
2. Single scan mode must be used for matching or unmatching event output.
3. Operation of window B is not supported when temperature sensor or internal reference voltage is selected for window A.
4. Operation of window A is not supported when temperature sensor or internal reference voltage is selected for window B.
5. The same channel cannot be set as both window A and window B.
6. It is necessary to make settings such that the high side reference value is greater than or equal to the low side reference value.

4.2.26 A/D Conversion Start Bit

When the 12-bit A/D converter's group priority operation mode is enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1) and the single-scan continuous function is used (ADGSPCR.GBRP bit = 1) on the RX66T Group, the value of the ADCSR.ADST remains 1.

4.2.27 PGA Output with 12-Bit A/D Converter in Module Stop State

On the RX66T Group the programmable gain amplifier (PGA) and 12-bit A/D converter are controlled by the same module stop signal, so comparison of the following PGA outputs cannot be performed when the 12-bit A/D converter is in the module stop state:

- AN000 pin PGA output
- AN001 pin PGA output
- AN002 pin PGA output
- AN100 pin PGA output
- AN101 pin PGA output
- AN102 pin PGA output

Comparison of the following analog pins cannot be performed when the 12-bit A/D converter is in the module stop state:

- AN000 pin
- AN001 pin
- AN002 pin
- AN100 pin
- AN101 pin
- AN102 pin

4.2.28 Generation of A/D Scan End Interrupt

When a scan is started by a software trigger on the RX66T Group, an A/D scan end interrupt is generated when the scan ends if the ADCSR.ADIE bit has been set to 1, even when double trigger mode is selected.

4.2.29 ROM Cache

The RX66T Group has an 8 KB ROM cache, but after reset cancellation the ROM cache is disabled. To use the ROM cache, set the ROMCE.ROMCEN bit to 1.

4.2.30 Using Flash Memory Commands

On the RX23T Group programming and erasing of the ROM is accomplished by first transitioning to the dedicated sequencer mode for ROM programming and erasing and then issuing software commands. On the RX66T Group programming and erasing of the ROM is accomplished by setting FACI commands in the FACI command-issuing area to control the FCU.

Table 4.1 is a comparative listing of software commands and FACI commands.

Table 4.1 Comparison of Software Commands and FACI Commands

Item	Software Command (RX23T)	FACI Command (RX66T)
Command-issuing area	—	FACI Command-issuing area (007E 0000h)
Usable commands	• Program • Block erase • All-block erase • Blank check • Start-up area information program • Access window information program	• Programming • Block erase • P/E suspend • P/E resume • Status clear • Forced stop • Configuration setting • Lock-bit programming • Lock-bit read

4.2.31 Option-Setting Memory

On the RX23T Group the codes used for ID code protection and on-chip debugger ID code protection are located in the ROM, but on the RX66T Group they are located in the option-setting memory. Note that the setting procedures therefore differ.

5. Reference Documents

User's Manual: Hardware

RX23T Group User's Manual: Hardware Rev.1.10 (R01UH0520EJ0110)
(The latest version can be downloaded from the Renesas Electronics website.)

RX66T Group User's Manual: Hardware Rev.1.21 (R01UH0749EJ0121)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This module reflects the content of the following technical updates:

TN-RX*-A0147B/E

TN-RX*-A200A/E

TN-RX*-A193A/E

TN-RX*-A194A/E

TN-RX*-A175A/E

TN-RX*-A173A/E

TN-RX*-A163A/E

TN-RX*-A151A/E

TN-RX*-A260A/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jun. 5, 2020	—	First edition issued
1.10	Mar. 1, 2022	43	Table 2.29 Comparative Overview of I/O Ports of 48-Pin Products added
		98	Table 2.66 Comparison of Serial Peripheral Interface Registers revised
		100	Table 2.67 SPCR2 register added
		113	Table 2.75 Comparative Overview of Comparator C Modules revised
		124	2.30 Packages revised
		128, 129	3.2 48-pin package added
		133	4.2.16 Count Clock Restrictions revised

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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