RX66N Group, RX72M/RX72N Group

Differences Between the RX66N Group and the RX72M/RX72N Group

Summary

This application note is a reference document that lists differences in peripheral modules, I/O registers, and pin functions between the RX66N Group and the RX72M/RX72N Group. This document also provides important information that needs to be taken into account when replacing the MCU. Unless otherwise indicated the maximum MCU specifications of RX66N Group products with 224 pins, RX72M Group products with 224 pins, and RX72N Group products with 224 pins are described. Refer to the User's Manual: Hardware of each MCU for details of differences in electrical characteristics, usage notes, and setting procedures.

Target Devices

RX66N Group

RX72M Group

RX72N Group

Contents

1. Comparison of Built-In Functions of RX66N Group and RX72M/RX72N Group 3

2. Comparative Overview of Specifications 5
2.1 CPU 5
2.2 Clock Generation Circuit 7
2.3 Low Power Consumption 11
2.4 Interrupt Controller 12
2.5 Buses 13
2.6 Event Link Controller 16
2.7 I/O Ports 25
2.8 Multi-Function Pin Controller 26
2.9 Ethernet Controller 106
2.10 DMA Controller for the Ethernet Controller 107
2.11 PHY Management Interface 109
2.12 RAM 110
2.13 Flash Memory 112
2.14 Packages 115

3. Comparison of Pin Functions 116
3.1 224-Pin LFBGA Package 116
3.2 176-Pin LFBGA Package 131
3.3 176-Pin LFQFP Package 143
3.4 145-Pin TFLGA Package 155
3.5 144-Pin LFQFP Package 162
3.6 100-Pin LFQFP Package 174

4. Important Information when Migrating Between MCUs 182
4.1 Important Information Regarding Function Settings 182
4.1.1 Port Direction Register (PDR) Initialization 182

5. Reference Documents 183

Revision History 185

1. Comparison of Built-In Functions of RX66N Group and RX72M/RX72N Group

A comparison of the built-in functions of the RX66N Group and RX72M/RX72N Group is provided below. For details of the functions, see section 2, Comparative Overview of Specifications and section 5, Reference Documents.

Table 1.1 is a comparison of built-in functions of RX66N Group and RX72M/RX72N Group.

Table 1.1 Comparison of Built-In Functions of RX66N Group and RX72M/RX72N Group

Function	RX72M	RX72N	RX66N
CPU	■		
Operating modes	○		
Address space	○		
Resets	○		
Option-setting memory (OFSM)	○		
Voltage detection circuit (LVDA)	○		
Clock generation circuit	■		
Clock frequency accuracy measurement circuit (CAC)	○		
Low power consumption	■		
Battery backup function	○		
Register write protection function	○		
Exception handling	○		
Interrupt controller (ICUD)	■		
Buses	■		
Memory-protection unit (MPU)	○		
DMA controller (DMACAa)	○		
EXDMA controller (EXDMACa)	○		
Data transfer controller (DTCb)	○		
Event link controller (ELC)	■		
I/O ports	●/■		
Multi-function pin controller (MPC)	■		
Multi-function timer pulse unit 3 (MTU3a)	○		
Port output enable 3 (POE3a)	○		
General PWM timer (GPTW)	○		
GPTW port output enable (POEG)	○		
16-bit timer pulse unit (TPUa)	○		
Programmable pulse generator (PPG)	○		
8-bit timer (TMR)	○		
Compare match timer (CMT)	○		
Compare match timer W (CMTW)	○		
Realtime clock (RTCd)	○		
Watchdog timer (WDTA)	○		
Independent watchdog timer (IWDTa)	○		
Ethernet controller (ETHERC)	■		
PTP module for the Ethernet controller (EPTPCb)	○		×
DMA controller for the Ethernet controller (EDMACa)	■		
PHY management interface (PMGI)	■		
EtherCAT slave controller (ESC)	○	×	
USB 2.0 FS Host/Function module (USBb)	○		
Serial communications interface (SCIj, SCIi, SCIh)	○		
I^2C bus interface (RIICa)	○		
CAN module (CAN)	○		

Function	RX72M	RX72N	RX66N
Serial peripheral interface (RSPIc)	○		
Quad serial peripheral interface (QSPI)	○		
CRC calculator (CRCA)	○		
Enhanced serial sound interface (SSIE)	○		
SD host interface (SDHI)	○		
MultiMediaCard interface (MMCIF)	○		
Parallel data capture unit (PDC)	○		
Graphic LCD controller (GLCDC)	○		
2D drawing engine (DRW2D)	○		
Boundary scan	○		
Arithmetic unit for trigonometric functions (TFU)	○		×
Trusted Secure IP (TSIP)	○		
Delta-sigma modulator interface (DSMIF)	○	×	
12-bit A/D converter (S12ADFa)	○		
12-bit D/A converter (R12DAa)	○		
Temperature sensor (TEMPS)	○		
Data operation circuit (DOC)	○		
RAM	▲		
Standby RAM	○		
Flash memory (FLASH)	●/▲/■		
Packages	●		

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Differences in register specifications are not listed.

2.1 CPU

Table 2.1 is a comparative overview of CPU.

Table 2.1 Comparative Overview of CPU

Item	RX72M/RX72N	RX66N
CPU	• Maximum operating frequency: 240 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per state (system clock cycle) • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • Basic instructions: 77 • Single-precision floating point instructions: 11 • DSP instructions: 23 • Instructions for register bank save function: 2 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits	• Maximum operating frequency: 120 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per state (system clock cycle) • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • Basic instructions: 77 • Single-precision floating point instructions: 11 • DSP instructions: 23 • Instructions for register bank save function: 2 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits
FPU	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard	• Single-precision floating point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard

Item	RX72M/RX72N	RX66N
Double-precision floating point coprocessor	• Double-precision floating-point register set — Double-precision floating-point data registers: 64-bit × 16 — Double-precision floating-point control registers: 32-bit × 4 • Double-precision floating-point processing instructions: 21 • Function for notifying the interrupt controller of double-precision floating-point exceptions	• Double-precision floating-point register set — Double-precision floating-point data registers: 64-bit × 16 — Double-precision floating-point control registers: 32-bit × 4 • Double-precision floating-point processing instructions: 21 • Function for notifying the interrupt controller of double-precision floating-point exceptions
Register bank save function	• Fast collective saving and restoration of the values of CPU registers • 16 save register banks	• Fast collective saving and restoration of the values of CPU registers • 16 save register banks

2.2 Clock Generation Circuit

Table 2.2 is a comparative overview of the clock generation circuits, and Table 2.3 is a comparison of clock generation circuit registers.

Table 2.2 Comparative Overview of Clock Generation Circuits

Item	RX72M	RX72N	RX66N
Use	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the ETHERC, EDMAC, EPTPC, RSPI, SCIi, MTU, GLCDC, DRW2D, PMGI, GPTW, and ESC. • Generates the peripheral module clock (PCLKB) to be supplied to the peripheral modules. • Generates the peripheral module clocks (for analog conversion) (PCLKC: unit 0; PCLKD: unit 1) to be supplied to the S12ADFa. • Generates the flash-IF clock (FCLK) to be supplied to the flash interface. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the SDRAM clock (SDCLK) to be supplied to the SDRAM. • Generates the USB clock (UCLK) to be supplied to the USB. • Generates the ESC clock (ESCCLK) to be supplied to the ESC. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the RTC sub-clock (RTCSCLK) to be supplied to the RTC.	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the ETHERC, EDMAC, EPTPC, RSPI, SCIi, MTU, GLCDC, DRW2D, PMGI, and GPTW. • Generates the peripheral module clock (PCLKB) to be supplied to the peripheral modules. • Generates the peripheral module clocks (for analog conversion) (PCLKC: unit 0; PCLKD: unit 1) to be supplied to the S12ADFa. • Generates the flash-IF clock (FCLK) to be supplied to the flash interface. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the SDRAM clock (SDCLK) to be supplied to the SDRAM. • Generates the USB clock (UCLK) to be supplied to the USB. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the RTC sub-clock (RTCSCLK) to be supplied to the RTC.	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the ETHERC, EDMAC, RSPI, SCIi, MTU, GLCDC, DRW2D, PMGI, and GPTW. • Generates the peripheral module clock (PCLKB) to be supplied to the peripheral modules. • Generates the peripheral module clocks (for analog conversion) (PCLKC: unit 0; PCLKD: unit 1) to be supplied to the S12ADFa. • Generates the flash-IF clock (FCLK) to be supplied to the flash interface. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the SDRAM clock (SDCLK) to be supplied to the SDRAM. • Generates the USB clock (UCLK) to be supplied to the USB. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the RTC sub-clock (RTCSCLK) to be supplied to the RTC.

Item	RX72M	RX72N	RX66N
Use	• Generates the RTC main clock (RTCMCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the JTAG clock (JTAGTCK) to be supplied to the JTAG.	• Generates the RTC main clock (RTCMCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the JTAG clock (JTAGTCK) to be supplied to the JTAG.	• Generates the RTC main clock (RTCMCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the JTAG clock (JTAGTCK) to be supplied to the JTAG.
Operating frequency	• ICLK: 240 MHz (max.) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKC: 60 MHz (max.) • PCLKD: 60 MHz (max.) • FCLK: — 4 MHz to 60 MHz (for programming and erasing the code flash memory and data flash memory) — 60 MHz (max.) (for reading from the data flash memory) • BCLK: 120 MHz (max.) • BCLK pin output: 80-MHz (max.) • SDCLK pin output: 80-MHz (max.) • UCLK: 48 MHz (max.) • ESCCLK: 100 MHz (max.) • CLKOUT25M pin output: 25 MHz (max.) • CLKOUT pin output: 40 MHz (max.) • CACCLK: Same as the clocks from the respective oscillators. • CANMCLK: 24 MHz (max.) • RTCSCLK: 32.768 kHz • RTCMCLK: 8 MHz to 16 MHz • IWDTCLK: 120 kHz • JTAGTCK: 10 MHz (max.)	• ICLK: 240 MHz (max.) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKC: 60 MHz (max.) • PCLKD: 60 MHz (max.) • FCLK: — 4 MHz to 60 MHz (for programming and erasing the code flash memory and data flash memory) — 60 MHz (max.) (for reading from the data flash memory) • BCLK: 120 MHz (max.) • BCLK pin output: 80-MHz (max.) • SDCLK pin output: 80-MHz (max.) • UCLK: 48 MHz (max.) • CLKOUT25M pin output: 25 MHz (max.) • CLKOUT pin output: 40 MHz (max.) • CACCLK: Same as the clocks from the respective oscillators. • CANMCLK: 24 MHz (max.) • RTCSCLK: 32.768 kHz • RTCMCLK: 8 MHz to 16 MHz • IWDTCLK: 120 kHz • JTAGTCK: 10 MHz (max.)	• ICLK: 120 MHz (max.) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKC: 60 MHz (max.) • PCLKD: 60 MHz (max.) • FCLK: — 4 MHz to 60 MHz (for programming and erasing the code flash memory and data flash memory) — 60 MHz (max.) (for reading from the data flash memory) • BCLK: 120 MHz (max.) • BCLK pin output: 80-MHz (max.) • SDCLK pin output: 80-MHz (max.) • UCLK: 48 MHz (max.) • CLKOUT25M pin output: 25 MHz (max.) • CLKOUT pin output: 40 MHz (max.) • CACCLK: Same as the clocks from the respective oscillators. • CANMCLK: 24 MHz (max.) • RTCSCLK: 32.768 kHz • RTCMCLK: 8 MHz to 16 MHz • IWDTCLK: 120 kHz • JTAGTCK: 10 MHz (max.)

Item	RX72M	RX72N	RX66N
Main clock oscillator	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 30 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop is detected on the main clock, the system clock source is switched to LOCO, and the MTU and GPTW pins can be forcedly driven high-impedance.	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 30 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop is detected on the main clock, the system clock source is switched to LOCO, and the MTU and GPTW pins can be forcedly driven high-impedance.	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 30 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop is detected on the main clock, the system clock source is switched to LOCO, and the MTU3 and GPT pins can be forcedly driven high-impedance.
Sub-clock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pins: XCIN, XCOUT	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pins: XCIN, XCOUT	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pins: XCIN, XCOUT
PLL frequency synthesizer	• Input clock sources: Main clock, HOCO • Input pulse frequency division ratio: Selectable from ×1/1, ×1/2, and ×1/3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication factor: Selectable from 10 to 30 • Output clock frequency of PLL frequency synthesizer: 120 MHz to 240 MHz	• Input clock sources: Main clock, HOCO • Input pulse frequency division ratio: Selectable from ×1/1, ×1/2, and ×1/3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication factor: Selectable from 10 to 30 • Output clock frequency of PLL frequency synthesizer: 120 MHz to 240 MHz	• Input clock sources: Main clock, HOCO • Input pulse frequency division ratio: Selectable from ×1/1, ×1/2, and ×1/3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication factor: Selectable from 10 to 30 • Output clock frequency of PLL frequency synthesizer: 120 MHz to 240 MHz

Item	RX72M	RX72N	RX66N
PLL frequency synthesizer for specific purposes (PPLL)	• Input clock sources: Main clock, HOCO • Input pulse frequency division ratio: Selectable from ×1/1, ×1/2, and ×1/3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication factor: Selectable from 10 to 30 • Output clock frequency of PLL frequency synthesizer: 120 MHz to 240 MHz	• Input clock sources: Main clock, HOCO • Input pulse frequency division ratio: Selectable from ×1/1, ×1/2, and ×1/3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication factor: Selectable from 10 to 30 • Output clock frequency of PLL frequency synthesizer: 120 MHz to 240 MHz	• Input clock sources: Main clock, HOCO • Input pulse frequency division ratio: Selectable from ×1/1, ×1/2, and ×1/3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication factor: Selectable from 10 to 30 • Output clock frequency of PLL frequency synthesizer: 120 MHz to 240 MHz
High-speed on-chip oscillator (HOCO)	• Oscillation frequency: Selectable among 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control	• Oscillation frequency: Selectable among 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control	• Oscillation frequency: Selectable among 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 240 kHz	Oscillation frequency: 240 kHz	Oscillation frequency: 240 kHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 120 kHz	Oscillation frequency: 120 kHz	Oscillation frequency: 120 kHz
JTAG external clock input (TCK)	Input clock frequency: 10 MHz (max.)	Input clock frequency: 10 MHz (max.)	Input clock frequency: 10 MHz (max.)
Control of output on BCLK pin	• Selectable between BCLK clock output and high output • Selectable between BCLK and BCLK ×1/2	• Selectable between BCLK clock output and high output • Selectable between BCLK and BCLK ×1/2	• Selectable between BCLK clock output and high output • Selectable between BCLK and BCLK ×1/2
Control of output on SDCLK pin	Selectable between SDCLK clock output and high output SDCLK	Selectable between SDCLK clock output and high output SDCLK	Selectable between SDCLK clock output and high output SDCLK
Event link function (output)	Detection of stopping of the main clock oscillator	Detection of stopping of the main clock oscillator	Detection of stopping of the main clock oscillator
Event link function (input)	Switching of the clock source to the low-speed on-chip oscillator	Switching of the clock source to the low-speed on-chip oscillator	Switching of the clock source to the low-speed on-chip oscillator

Table 2.3 Comparison of Clock Generation Circuit Registers

Register	Bit	RX72M	RX72N	RX66N
MEMWAIT	—	Memory wait cycle setting register	Memory wait cycle setting register	—
PACKCR	EPLLSEL	ESC clock (ESCCLK) source select bit	—	—

2.3 Low Power Consumption

Table 2.4 is a comparison of low power consumption registers.

Table 2.4 Comparison of Low Power Consumption Registers

Register	Bit	RX72M	RX72N	RX66N
MSTPCRB	MSTPB11	Delta-sigma interface module stop bit	—	—
	MSTPB13	Ethernet-controller PTP controller and Ethernet-controller DMA controller module stop setting bit	Ethernet-controller PTP controller and Ethernet-controller DMA controller module stop setting bit	—
	MSTPB14	Ethernet controller, Ethernet controller DMA controller, and PHY management interface (channel 1) modules stop bit	Ethernet controller, Ethernet controller DMA controller, and PHY management interface (channel 1) modules stop bit	—
MSTPCRD	MSTPD11	EtherCAT slave controller module stop bit*1	—	—

Note: 1. When transitioning to software standby mode after changing the value of the MSTPD11 bit, execute the WAIT instruction after two cycles of the ESC clock (ESCCLK) have elapsed after writing to the MSTPD11 bit.

2.4 Interrupt Controller

Table 2.5 is a comparison of interrupt controller registers.

Table 2.5 Comparison of Interrupt Controller Registers

Register	Bit	RX72M (ICUD)	RX72N (ICUD)	RX66N (ICUD)
PIARk	—	Software configurable interrupt A request register k (k = 0h to Ch)	Software configurable interrupt A request register k (k = 0h to Ah, Ch)	Software configurable interrupt A request register k (k = 0h to Ah, Ch)

2.5 Buses

Table 2.6 is a comparative overview of the buses.

Table 2.6 Comparative Overview of Buses

Item		RX72M	RX72N	RX66N
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, expansion RAM, ECCRAM, code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, expansion RAM, ECCRAM, code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, expansion RAM, ECCRAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, expansion RAM, ECCRAM, code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, expansion RAM, ECCRAM, code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, expansion RAM, ECCRAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	Connected to RAM	Connected to RAM	Connected to RAM
	Memory bus 2	Connected to code flash memory	Connected to code flash memory	Connected to code flash memory
	Memory bus 3	Connected to expansion RAM and ECCRAM	Connected to expansion RAM and ECCRAM	Connected to expansion RAM and ECCRAM
Internal main buses	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DMAC, DTC, and extended bus master • Connected to on-chip memory (RAM, expansion RAM, ECCRAM, code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the DMAC, DTC, and extended bus master • Connected to on-chip memory (RAM, expansion RAM, ECCRAM, code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the DMAC, DTC, and extended bus master • Connected to on-chip memory (RAM, expansion RAM, ECCRAM, code flash memory) • Operates in synchronization with the system clock (ICLK)

Item		RX72M	RX72N	RX66N
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, DMAC, EXDMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK) (EXDMAC operates in synchronization with the BCLK)	• Connected to peripheral modules (DTC, DMAC, EXDMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK) (EXDMAC operates in synchronization with the BCLK)	• Connected to peripheral modules (DTC, DMAC, EXDMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK) (EXDMAC operates in synchronization with the BCLK)
	Internal peripheral bus 2	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1 and 3 to 5) • Operates in synchronization with the peripheral module clock (PCLKB)	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1 and 3 to 5) • Operates in synchronization with the peripheral module clock (PCLKB)	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1 and 3 to 5) • Operates in synchronization with the peripheral module clock (PCLKB)
	Internal peripheral bus 3	• Connected to peripheral modules (USB, DSMIF, PDC, and standby RAM) • Operates in synchronization with the peripheral module clock (PCLKB)	• Connected to peripheral modules (USB, PDC, and standby RAM) • Operates in synchronization with the peripheral module clock (PCLKB)	• Connected to peripheral modules (USB, PDC, and standby RAM) • Operates in synchronization with the peripheral module clock (PCLKB)
	Internal peripheral bus 4	• Connected to peripheral modules (EDMAC, ETHERC, PMGI, EPTPC, GPTW, MTU, SCIi, and RSPI) • Operates in synchronization with the peripheral module clock (PCLKA)	• Connected to peripheral modules (EDMAC, ETHERC, PMGI, EPTPC, GPTW, MTU, SCIi, and RSPI) • Operates in synchronization with the peripheral module clock (PCLKA)	• Connected to peripheral modules (EDMAC, ETHERC, PMGI, GPTW, MTU, SCIi, and RSPI) • Operates in synchronization with the peripheral module clock (PCLKA)
	Internal peripheral bus 5	• Connected to peripheral modules (GLCDC, DRW2D, and ESC) • Operates in synchronization with the peripheral module clock (PCLKA)	• Connected to peripheral modules (GLCDC and DRW2D) • Operates in synchronization with the peripheral module clock (PCLKA)	• Connected to peripheral modules (GLCDC and DRW2D) • Operates in synchronization with the peripheral module clock (PCLKA)

Item		RX72M	RX72N	RX66N
Internal peripheral buses	Internal peripheral bus 6	• Connected to code flash (in P/E) and data flash memory • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to code flash (in P/E) and data flash memory • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to code flash (in P/E) and data flash memory • Operates in synchronization with the FlashIF clock (FCLK)
External bus	CS area	• Connected to external devices • Operates in synchronization with the external-bus clock (BCLK)	• Connected to external devices • Operates in synchronization with the external-bus clock (BCLK)	• Connected to external devices • Operates in synchronization with the external-bus clock (BCLK)
	SDRAM area	• Connected to SDRAM • Operates in synchronization with the SDRAM clock (SDCLK)	• Connected to SDRAM • Operates in synchronization with the SDRAM clock (SDCLK)	• Connected to SDRAM • Operates in synchronization with the SDRAM clock (SDCLK)

2.6 Event Link Controller

Table 2.7 is a comparative overview of the event link controllers, Table 2.8 is a comparison of event link controller registers, Table 2.9 lists correspondences between ELSRn registers and peripheral modules, and Table 2.10 shows correspondences between values set in ELSRn.ELS[7:0] and event signal names and numbers.

Table 2.7 Comparative Overview of Event Link Controllers

Item	RX72M (ELC)	RX72N (ELC)	RX66N (ELC)
Event link function	• 137 event signals can be directly interconnected to modules. • Operation of timer modules while inputting an event signal can be selected. • Event linkage operation is possible on ports B and E. — Single port*1: Event link operation can be specified on a single port. — Port group*1: Event linkage operation can be specified by grouping multiple designated ports among up to eight ports.	• 135 event signals can be directly interconnected to modules. • Operation of timer modules while inputting an event signal can be selected. • Event linkage operation is possible on ports B and E. — Single port*1: Event link operation can be specified on a single port. — Port group*1: Event linkage operation can be specified by grouping multiple designated ports among up to eight ports.	• 123 event signals can be directly interconnected to modules. • Operation of timer modules while inputting an event signal can be selected. • Event linkage operation is possible on ports B and E. — Single port*1: Event link operation can be specified on a single port. — Port group*1: Event linkage operation can be specified by grouping multiple designated ports among up to eight ports.
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state	Ability to transition to module stop state

Note: 1. An event is generated when the corresponding input signal on a single port or port group set to input changes.

Table 2.8 Comparison of Event Link Controller Registers

Register	Bit	RX72M (ELC)	RX72N (ELC)	RX66N (ELC)
ELSRn	—	Event Link Setting Register n (n = 0, 3, 4, 7, 10 to 13, 15, 16, 18 to 28, 33, 35 to 38, 41 to 45, and 48 to 57)	Event Link Setting Register n (n = 0, 3, 4, 7, 10 to 13, 15, 16, 18 to 28, 33, 35 to 38, 45, and 48 to 57)	Event Link Setting Register n (n = 0, 3, 4, 7, 10 to 13, 15, 16, 18 to 28, 33, 35 to 38, 45, and 48 to 57)
	ELS[7:0]	Event link select bits 00h: Event signal output to the corresponding peripheral module is disabled. 01h to CFh: Specifies the number of the event signal to be linked. Settings other than the above are prohibited.	Event link select bits 00h: Event signal output to the corresponding peripheral module is disabled. 01h to CFh: Specifies the number of the event signal to be linked. Settings other than the above are prohibited.	Event link select bits 00h: Event signal output to the corresponding peripheral module is disabled. 01h to CDh: Specifies the number of the event signal to be linked. Settings other than the above are prohibited.

Table 2.9 Correspondence between ELSRn Registers and Peripheral Modules

Register	RX72M (ELC)	RX72N (ELC)	RX66N (ELC)
ELSR0	MTU0	MTU0	MTU0
ELSR3	MTU3	MTU3	MTU3
ELSR4	MTU4	MTU4	MTU4
ELSR7	CMT1	CMT1	CMT1
ELSR10	TMR0	TMR0	TMR0
ELSR11	TMR1	TMR1	TMR1
ELSR12	TMR2	TMR2	TMR2
ELSR13	TMR3	TMR3	TMR3
ELSR15	S12AD (ELCTRG00N)	S12AD (ELCTRG00N)	S12AD (ELCTRG00N)
ELSR16	DA0	DA0	DA0
ELSR18	ICU (interrupt 1)	ICU (interrupt 1)	ICU (interrupt 1)
ELSR19	ICU (interrupt 2)	ICU (interrupt 2)	ICU (interrupt 2)
ELSR20	Output port group 1	Output port group 1	Output port group 1
ELSR21	Output port group 2	Output port group 2	Output port group 2
ELSR22	Input port group 1	Input port group 1	Input port group 1
ELSR23	Input port group 2	Input port group 2	Input port group 2
ELSR24	Single port 0	Single port 0	Single port 0
ELSR25	Single port 1	Single port 1	Single port 1
ELSR26	Single port 2	Single port 2	Single port 2
ELSR27	Single port 3	Single port 3	Single port 3
ELSR28	Clock source switching to LOCO	Clock source switching to LOCO	Clock source switching to LOCO
ELSR33	CMTW0	CMTW0	CMTW0
ELSR35	TPU0	TPU0	TPU0
ELSR36	TPU1	TPU1	TPU1
ELSR37	TPU2	TPU2	TPU2
ELSR38	TPU3	TPU3	TPU3
ELSR41	DSMIF0 trigger 0	—	—
ELSR42	DSMIF0 trigger 1	—	—
ELSR43	DSMIF1 trigger 0	—	—
ELSR44	DSMIF1 trigger 1	—	—
ELSR45	S12AD1 (ELCTRG10N)	S12AD1 (ELCTRG10N)	S12AD1 (ELCTRG10N)
ELSR48	GPTW event source A (common to all channels)	GPTW event source A (common to all channels)	GPTW event source A (common to all channels)
ELSR49	GPTW event source B (common to all channels)	GPTW event source B (common to all channels)	GPTW event source B (common to all channels)
ELSR50	GPTW event source C (common to all channels)	GPTW event source C (common to all channels)	GPTW event source C (common to all channels)
ELSR51	GPTW event source D (common to all channels)	GPTW event source D (common to all channels)	GPTW event source D (common to all channels)
ELSR52	GPTW event source E (common to all channels)	GPTW event source E (common to all channels)	GPTW event source E (common to all channels)
ELSR53	GPTW event source F (common to all channels)	GPTW event source F (common to all channels)	GPTW event source F (common to all channels)
ELSR54	GPTW event source G (common to all channels)	GPTW event source G (common to all channels)	GPTW event source G (common to all channels)
ELSR55	GPTW event source H (common to all channels)	GPTW event source H (common to all channels)	GPTW event source H (common to all channels)
ELSR56	S12AD (ELCTRG01N)	S12AD (ELCTRG01N)	S12AD (ELCTRG01N)
ELSR57	S12AD1 (ELCTRG11N)	S12AD1 (ELCTRG11N)	S12AD1 (ELCTRG11N)

Table 2.10 Correspondence between Values Set in ELSRn.ELS[7:0] Bits and Event Signal Names and Numbers

Value of ELS[7:0] Bits	Peripheral Module	RX72M (ELC)	RX72N (ELC)	RX66N (ELC)
01h	Multifunction timer pulse unit 3	MTU0 compare match 0A	MTU0 compare match 0A	MTU0 compare match 0A
02h		MTU0 compare match 0B	MTU0 compare match 0B	MTU0 compare match 0B
03h		MTU0 compare match 0C	MTU0 compare match 0C	MTU0 compare match 0C
04h		MTU0 compare match 0D	MTU0 compare match 0D	MTU0 compare match 0D
05h		MTU0 compare match 0E	MTU0 compare match 0E	MTU0 compare match 0E
06h		MTU0 compare match 0F	MTU0 compare match 0F	MTU0 compare match 0F
07h		MTU0 overflow	MTU0 overflow	MTU0 overflow
10h		MTU3 compare match 3A	MTU3 compare match 3A	MTU3 compare match 3A
11h		MTU3 compare match 3B	MTU3 compare match 3B	MTU3 compare match 3B
12h		MTU3 compare match 3C	MTU3 compare match 3C	MTU3 compare match 3C
13h		MTU3 compare match 3D	MTU3 compare match 3D	MTU3 compare match 3D
14h		MTU3 overflow	MTU3 overflow	MTU3 overflow
15h		MTU4 compare match 4A	MTU4 compare match 4A	MTU4 compare match 4A
16h		MTU4 compare match 4B	MTU4 compare match 4B	MTU4 compare match 4B
17h		MTU4 compare match 4C	MTU4 compare match 4C	MTU4 compare match 4C
18h		MTU4 compare match 4D	MTU4 compare match 4D	MTU4 compare match 4D
19h		MTU4 overflow	MTU4 overflow	MTU4 overflow
1Ah		MTU4 underflow	MTU4 underflow	MTU4 underflow
1Fh	Compare match timer	CMT1 compare match 1	CMT1 compare match 1	CMT1 compare match 1
22h	8-bit timer	TMR0 compare match A0	TMR0 compare match A0	TMR0 compare match A0
23h		TMR0 compare match B0	TMR0 compare match B0	TMR0 compare match B0
24h		TMR0 overflow	TMR0 overflow	TMR0 overflow
25h		TMR1 compare match A1	TMR1 compare match A1	TMR1 compare match A1
26h		TMR1 compare match B1	TMR1 compare match B1	TMR1 compare match B1
27h		TMR1 overflow	TMR1 overflow	TMR1 overflow
28h		TMR2 compare match A2	TMR2 compare match A2	TMR2 compare match A2
29h		TMR2 compare match B2	TMR2 compare match B2	TMR2 compare match B2
2Ah		TMR2 overflow	TMR2 overflow	TMR2 overflow

Value of ELS[7:0] Bits	Peripheral Module	RX72M (ELC)	RX72N (ELC)	RX66N (ELC)
2Bh	8-bit timer	TMR3 compare match A3	TMR3 compare match A3	TMR3 compare match A3
2Ch		TMR3 compare match B3	TMR3 compare match B3	TMR3 compare match B3
2Dh		TMR3 overflow	TMR3 overflow	TMR3 overflow
2Eh	Realtime clock	RTC periodic event (select 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, 1, or 2 seconds)	RTC periodic event (select 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, 1, or 2 seconds)	RTC periodic event (select 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, 1, or 2 seconds)
31h	Independent watchdog timer	IWDT underflow or refresh error	IWDT underflow or refresh error	IWDT underflow or refresh error
3Ah	Serial communications interface	SCI5 error (receive error or error signal detection)	SCI5 error (receive error or error signal detection)	SCI5 error (receive error or error signal detection)
3Bh		SCI5 receive data full	SCI5 receive data full	SCI5 receive data full
3Ch		SCI5 transmit data empty	SCI5 transmit data empty	SCI5 transmit data empty
3Dh		SCI5 transmit end	SCI5 transmit end	SCI5 transmit end
4Eh	I^2C bus interface	RIIC0 communication error or event generation	RIIC0 communication error or event generation	RIIC0 communication error or event generation
4Fh		RIIC0 receive data full	RIIC0 receive data full	RIIC0 receive data full
50h		RIIC0 transmit data empty	RIIC0 transmit data empty	RIIC0 transmit data empty
51h		RIIC0 transmit end	RIIC0 transmit end	RIIC0 transmit end
52h	Serial peripheral interface	RSPI0 error (mode fault, overrun, underrun, or parity error)	RSPI0 error (mode fault, overrun, underrun, or parity error)	RSPI0 error (mode fault, overrun, underrun, or parity error)
53h		RSPI0 idle	RSPI0 idle	RSPI0 idle
54h		RSPI0 receive data full	RSPI0 receive data full	RSPI0 receive data full
55h		RSPI0 transmit data empty	RSPI0 transmit data empty	RSPI0 transmit data empty
56h		RSPI0 transmit end	RSPI0 transmit end	RSPI0 transmit end
58h	12-bit A/D converter	S12AD A/D conversion end	S12AD A/D conversion end	S12AD A/D conversion end
5Bh	Voltage detection circuit	LVD1 voltage detection	LVD1 voltage detection	LVD1 voltage detection
5Ch		LVD2 voltage detection	LVD2 voltage detection	LVD2 voltage detection
5Dh	DMA controller	DMAC0 transfer end	DMAC0 transfer end	DMAC0 transfer end
5Eh		DMAC1 transfer end	DMAC1 transfer end	DMAC1 transfer end
5Fh		DMAC2 transfer end	DMAC2 transfer end	DMAC2 transfer end
60h		DMAC3 transfer end	DMAC3 transfer end	DMAC3 transfer end
61h	Data transfer controller	DTC transfer end	DTC transfer end	DTC transfer end
62h	Clock generation circuit	Oscillation stop detection of clock generation circuit	Oscillation stop detection of clock generation circuit	Oscillation stop detection of clock generation circuit

Value of ELS[7:0] Bits	Peripheral Module	RX72M (ELC)	RX72N (ELC)	RX66N (ELC)
63h	I/O ports	Input edge detection of input port group 1	Input edge detection of input port group 1	Input edge detection of input port group 1
64h		Input edge detection of input port group 2	Input edge detection of input port group 2	Input edge detection of input port group 2
65h		Input edge detection of single input port 0	Input edge detection of single input port 0	Input edge detection of single input port 0
66h		Input edge detection of single input port 1	Input edge detection of single input port 1	Input edge detection of single input port 1
67h		Input edge detection of single input port 2	Input edge detection of single input port 2	Input edge detection of single input port 2
68h		Input edge detection of single input port 3	Input edge detection of single input port 3	Input edge detection of single input port 3
69h	Event link controller	Software event	Software event	Software event
6Ah	Data operation circuit	DOC data operation condition met	DOC data operation condition met	DOC data operation condition met
6Ch	12-bit A/D converter	S12AD1 A/D conversion end	S12AD1 A/D conversion end	S12AD1 A/D conversion end
7Eh	Compare match timer W	CMTW channel 0 compare match	CMTW channel 0 compare match	CMTW channel 0 compare match
80h	General PWM timer	GPTW0 compare match A	GPTW0 compare match A	GPTW0 compare match A
81h		GPTW0 compare match B	GPTW0 compare match B	GPTW0 compare match B
82h		GPTW0 compare match C	GPTW0 compare match C	GPTW0 compare match C
83h		GPTW0 compare match D	GPTW0 compare match D	GPTW0 compare match D
84h		GPTW0 compare match E	GPTW0 compare match E	GPTW0 compare match E
85h		GPTW0 compare match F	GPTW0 compare match F	GPTW0 compare match F
86h		GPTW0 overflow	GPTW0 overflow	GPTW0 overflow
87h		GPTW0 underflow	GPTW0 underflow	GPTW0 underflow
88h		GPTW1 compare match A	GPTW1 compare match A	GPTW1 compare match A
89h		GPTW1 compare match B	GPTW1 compare match B	GPTW1 compare match B
8Ah		GPTW1 compare match C	GPTW1 compare match C	GPTW1 compare match C
8Bh		GPTW1 compare match D	GPTW1 compare match D	GPTW1 compare match D
8Ah		GPTW1 compare match E	GPTW1 compare match E	GPTW1 compare match E
8Bh		GPTW1 compare match F	GPTW1 compare match F	GPTW1 compare match F
8Eh		GPTW1 overflow	GPTW1 overflow	GPTW1 overflow
8Fh		GPTW1 underflow	GPTW1 underflow	GPTW1 underflow
90h		GPTW2 compare match A	GPTW2 compare match A	GPTW2 compare match A
91h		GPTW2 compare match B	GPTW2 compare match B	GPTW2 compare match B

Value of ELS[7:0] Bits	Peripheral Module	RX72M (ELC)	RX72N (ELC)	RX66N (ELC)
92h	General PWM timer	GPTW2 compare match C	GPTW2 compare match C	GPTW2 compare match C
93h		GPTW2 compare match D	GPTW2 compare match D	GPTW2 compare match D
94h		GPTW2 compare match E	GPTW2 compare match E	GPTW2 compare match E
95h		GPTW2 compare match F	GPTW2 compare match F	GPTW2 compare match F
96h		GPTW2 overflow	GPTW2 overflow	GPTW2 overflow
97h		GPTW2 underflow	GPTW2 underflow	GPTW2 underflow
98h		GPTW3 compare match A	GPTW3 compare match A	GPTW3 compare match A
99h		GPTW3 compare match B	GPTW3 compare match B	GPTW3 compare match B
9Ah		GPTW3 compare match C	GPTW3 compare match C	GPTW3 compare match C
9Bh		GPTW3 compare match D	GPTW3 compare match D	GPTW3 compare match D
9Ah		GPTW3 compare match E	GPTW3 compare match E	GPTW3 compare match E
9Bh		GPTW3 compare match F	GPTW3 compare match F	GPTW3 compare match F
9Eh		GPT3 overflow	GPTW3 overflow	GPTW3 overflow
9Fh		GPT3 underflow	GPTW3 underflow	GPTW3 underflow
A0h	Ethernet controller	EPTPC STCA timer 0 rising edge detection	EPTPC STCA timer 0 rising edge detection	—
A1h		EPTPC STCA timer 1 rising edge detection	EPTPC STCA timer 1 rising edge detection	—
A2h		EPTPC STCA timer 2 rising edge detection	EPTPC STCA timer 2 rising edge detection	—
A3h		EPTPC STCA timer 3 rising edge detection	EPTPC STCA timer 3 rising edge detection	—
A4h		EPTPC STCA timer 4 rising edge detection	EPTPC STCA timer 4 rising edge detection	—
A5h		EPTPC STCA timer 5 rising edge detection	EPTPC STCA timer 5 rising edge detection	—
A6h		EPTPC STCA timer 0 falling edge detection	EPTPC STCA timer 0 falling edge detection	—
A7h		EPTPC STCA timer 1 falling edge detection	EPTPC STCA timer 1 falling edge detection	—
A8h		EPTPC STCA timer 2 falling edge detection	EPTPC STCA timer 2 falling edge detection	—
A9h		EPTPC STCA timer 3 falling edge detection	EPTPC STCA timer 3 falling edge detection	—
AAh		EPTPC STCA timer 4 falling edge detection	EPTPC STCA timer 4 falling edge detection	—
ABh		EPTPC STCA timer 5 falling edge detection	EPTPC STCA timer 5 falling edge detection	—

Value of ELS[7:0] Bits	Peripheral Module	RX72M (ELC)	RX72N (ELC)	RX66N (ELC)
ACh	16-bit timer pulse unit	TPU0 compare match A	TPU0 compare match A	TPU0 compare match A
ADh		TPU0 compare match B	TPU0 compare match B	TPU0 compare match B
AEh		TPU0 compare match C	TPU0 compare match C	TPU0 compare match C
AFh		TPU0 compare match D	TPU0 compare match D	TPU0 compare match D
B0h		TPU0 overflow	TPU0 overflow	TPU0 overflow
B1h		TPU1 compare match A	TPU1 compare match A	TPU1 compare match A
B2h		TPU1 compare match B	TPU1 compare match B	TPU1 compare match B
B3h		TPU1 overflow	TPU1 overflow	TPU1 overflow
B4h		TPU1 underflow	TPU1 underflow	TPU1 underflow
B5h		TPU2 compare match A	TPU2 compare match A	TPU2 compare match A
B6h		TPU2 compare match B	TPU2 compare match B	TPU2 compare match B
B7h		TPU2 overflow	TPU2 overflow	TPU2 overflow
B8h		TPU2 underflow	TPU2 underflow	TPU2 underflow
B9h		TPU3 compare match A	TPU3 compare match A	TPU3 compare match A
BAh		TPU3 compare match B	TPU3 compare match B	TPU3 compare match B
BBh		TPU3 compare match C	TPU3 compare match C	TPU3 compare match C
BCh		TPU3 compare match D	TPU3 compare match D	TPU3 compare match D
BDh		TPU3 overflow	TPU3 overflow	TPU3 overflow
C6h	General PWM timer	GPTW0 A/D converter start request A	GPTW0 A/D converter start request A	GPTW0 A/D converter start request A
C7h		GPTW0 A/D converter start request B	GPTW0 A/D converter start request B	GPTW0 A/D converter start request B
C8h		GPTW1 A/D converter start request A	GPTW1 A/D converter start request A	GPTW1 A/D converter start request A
C9h		GPTW1 A/D converter start request B	GPTW1 A/D converter start request B	GPTW1 A/D converter start request B
CAh		GPTW2 A/D converter start request A	GPTW2 A/D converter start request A	GPTW2 A/D converter start request A
CBh		GPTW2 A/D converter start request B	GPTW2 A/D converter start request B	GPTW2 A/D converter start request B
CCh		GPTW3 A/D converter start request A	GPTW3 A/D converter start request A	GPTW3 A/D converter start request A

Value of ELS[7:0] Bits	Peripheral Module	RX72M (ELC)	RX72N (ELC)	RX66N (ELC)
CDh	General PWM timer	GPTW3 A/D converter start request B	GPTW3 A/D converter start request B	GPTW3 A/D converter start request B
CEh	EtherCAT slave controller	ESC SYNC0	—	—
CFh		ESC SYNC1	—	—
Settings other than the above are prohibited.				

2.7 I/O Ports

Table 2.11 is a comparative overview of the I/O ports of 145-pin and 144-pin products, Table 2.12 is a comparative overview of the I/O ports of 100-pin products.

Table 2.11 Comparative Overview of I/O Ports of 145- and 144-Pin Products

Item	RX72M (144-Pin)	RX72N (145-Pin, 144-Pin)	RX66N (145-Pin, 144-Pin)
PORT0	P00 to P03, P05	P00 to P03, P05, P07	P00 to P03, P05, P07
PORT1	P12 to P17	P12 to P17	P12 to P17
PORT2	P20 to P27	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37	P30 to P37
PORT4	P40 to P44	P40 to P47	P40 to P47
PORT5	P50 to P56	P50 to P56	P50 to P56
PORT6	P60 to P67	P60 to P67	P60 to P67
PORT7	P73 to P77	P70 to P77	P70 to P77
PORT8	P80 to P83, P86, P87	P80 to P83, P86, P87	P80 to P83, P86, P87
PORT9	P90 to P93, P96, P97	P90 to P93	P90 to P93
PORTA	PA0 to PA7	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7	PE0 to PE7
PORTF	—	PF5	PF5
PORTG	PG0 to PG2, PG5 to PG7	—	—
PORTJ	PJ2, PJ3	PJ3, PJ5	PJ3, PJ5

Table 2.12 Comparative Overview of I/O Ports of 100-Pin Products

Item	RX72M (100-Pin)	RX72N (100-Pin)	RX66N (100-Pin)
PORT0	P00	P05, P07	P05, P07
PORT1	P14 to P17	P12 to P17	P12 to P17
PORT2	P20, P21, P23 to P27	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37	P30 to P37
PORT4	P40 to P42	P40 to P47	P40 to P47
PORT5	P50 to P52, P56	P50 to P55	P50 to P55
PORT6	P60 to P64, P66, P67	—	—
PORT8	P80 to P82, P86, P87	—	—
PORT9	P90 to P93, P96, P97	—	—
PORTA	PA0 to PA4, PA6	PA0 to PA7	PA0 to PA7
PORTB	PB0, PB1, PB3 to PB7	PB0 to PB7	PB0 to PB7
PORTC	PC2, PC4 to PC7	PC0 to PC7	PC0 to PC7
PORTD	PD1, PD2, PD6, PD7	PD0 to PD7	PD0 to PD7
PORTE	PE3 to PE5	PE0 to PE7	PE0 to PE7
PORTJ	—	PJ3	PJ3
PORTG	PG2, PG5, PG6	—	—

2.8 Multi-Function Pin Controller

Table 2.13 and Table 2.14 are comparison of the assignments of multiplexed pins, and Table 2.15 to Table 2.38 are comparisons of multi-function pin controller registers.

In the following comparison of the assignments of multiplexed pins, **orange text** designates pins that exist on the RX72M/RX72N Group only, **purple text** pins that exist on the RX72N Group or RX66N Group only, and **green text** pins that exist on the RX72M Group only. A circle (○) indicates that a function is assigned, a cross (×) that the pin does not exist or that no function is assigned, and grayed out items mean that the function is not implemented.

Table 2.13 Comparison of Multiplexed Pin Assignments (224-Pin/176-Pin)

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			224-Pin	176-Pin	224-Pin	176-Pin	224-Pin	176-Pin
Interrupt	NMI (input)	P35	○	○	○	○	○	○
EXDMA controller	EDREQ0 (input)	P22	○	○	○	○	○	○
		P55	○	○	○	○	○	○
		P80	○	○	○	○	○	○
	EDACK0 (output)	P54	○	○	○	○	○	○
		P23	○	○	○	○	○	○
		P81	○	○	○	○	○	○
	EDREQ1 (input)	P24	○	○	○	○	○	○
		P33	○	○	○	○	○	○
		P82	○	○	○	○	○	○
	EDACK1 (output)	P25	○	○	○	○	○	○
		P56	○	○	○	○	○	○
		P83	○	○	○	○	○	○
		PJ3	○	○	○	○	○	○
Interrupt	IRQ0-DS (input)	P30	○	○	○	○	○	○
	IRQ0 (input)	P10	○	○	○	○	○	○
		PD0	○	○	○	○	○	○
	IRQ1-DS (input)	P31	○	○	○	○	○	○
	IRQ1 (input)	P11	○	○	○	○	○	○
		PD1	○	○	○	○	○	○
	IRQ2-DS (input)	P32	○	○	○	○	○	○
	IRQ2 (input)	P12	○	○	○	○	○	○
		PD2	○	○	○	○	○	○
	IRQ3-DS (input)	P33	○	○	○	○	○	○
	IRQ3 (input)	P13	○	○	○	○	○	○
		PD3	○	○	○	○	○	○
	IRQ4-DS (input)	PB1	○	○	○	○	○	○
	IRQ4 (input)	P14	○	○	○	○	○	○
		P34	○	○	○	○	○	○
		PD4	○	○	○	○	○	○
		PF5	○	○	○	○	○	○
	IRQ5-DS (input)	PA4	○	○	○	○	○	○
	IRQ5 (input)	P15	○	○	○	○	○	○
		PD5	○	○	○	○	○	○
		PE5	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			224-Pin	176-Pin	224-Pin	176-Pin	224-Pin	176-Pin
Interrupt	IRQ6-DS (input)	PA3	○	○	○	○	○	○
	IRQ6 (input)	P16	○	○	○	○	○	○
		PD6	○	○	○	○	○	○
		PE6	○	○	○	○	○	○
	IRQ7-DS (input)	PE2	○	○	○	○	○	○
	IRQ7 (input)	P17	○	○	○	○	○	○
		PD7	○	○	○	○	○	○
		PE7	○	○	○	○	○	○
	IRQ8-DS (input)	P40	○	○	○	○	○	○
	IRQ8 (input)	P00	○	○	○	○	○	○
		P20	○	○	○	○	○	○
	IRQ9-DS (input)	P41	○	○	○	○	○	○
	IRQ9 (input)	P01	○	○	○	○	○	○
		P21	○	○	○	○	○	○
	IRQ10-DS (input)	P42	○	○	○	○	○	○
	IRQ10 (input)	P02	○	○	○	○	○	○
		P55	○	○	○	○	○	○
	IRQ11-DS (input)	P43	○	○	○	○	○	○
	IRQ11 (input)	P03	○	○	○	○	○	○
		PA1	○	○	○	○	○	○
	IRQ12-DS (input)	P44	○	○	○	○	○	○
	IRQ12 (input)	PB0	○	○	○	○	○	○
		PC1	○	○	○	○	○	○
	IRQ13-DS (input)	P45	○	○	○	○	○	○
	IRQ13 (input)	P05	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	IRQ14-DS (input)	P46	○	○	○	○	○	○
	IRQ14 (input)	PC0	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	IRQ15-DS (input)	P47	○	○	○	○	○	○
	IRQ15 (input)	P07	○	○	○	○	○	○
		P67	○	○	○	○	○	○
Multi-function timer pulse unit 3	MTIOC0A (input/output)	P34	○	○	○	○	○	○
		PB3	○	○	○	○	○	○
	MTIOC0B (input/output)	P13	○	○	○	○	○	○
		P15	○	○	○	○	○	○
		PA1	○	○	○	○	○	○
	MTIOC0C (input/output)	P32	○	○	○	○	○	○
		PB1	○	○	○	○	○	○
	MTIOC0D (input/output)	P33	○	○	○	○	○	○
		PA3	○	○	○	○	○	○
	MTIOC1A (input/output)	P20	○	○	○	○	○	○
		PE4	○	○	○	○	○	○
	MTIOC1B (input/output)	P21	○	○	○	○	○	○
		PB5	○	○	○	○	○	○
	MTIOC2A (input/output)	P26	○	○	○	○	○	○
		PB5	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			224-Pin	176-Pin	224-Pin	176-Pin	224-Pin	176-Pin
Multi-function timer pulse unit 3	MTIOC2B (input/output)	P27	○	○	○	○	○	○
		PE5	○	○	○	○	○	○
	MTIOC3A (input/output)	P14	○	○	○	○	○	○
		P17	○	○	○	○	○	○
		PC1	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	MTIOC3B (input/output)	P17	○	○	○	○	○	○
		P22	○	○	○	○	○	○
		P80	○	○	○	○	○	○
		PB7	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
		PE1	○	○	○	○	○	○
	MTIOC3C (input/output)	P16	○	○	○	○	○	○
		P56	○	○	○	○	○	○
		PC0	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
		PJ3	○	○	○	○	○	○
	MTIOC3D (input/output)	P16	○	○	○	○	○	○
		P23	○	○	○	○	○	○
		P81	○	○	○	○	○	○
		PB6	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
		PE0	○	○	○	○	○	○
	MTIOC4A (input/output)	P21	○	○	○	○	○	○
		P24	○	○	○	○	○	○
		P82	○	○	○	○	○	○
		PA0	○	○	○	○	○	○
		PB3	○	○	○	○	○	○
		PE2	○	○	○	○	○	○
	MTIOC4B (input/output)	P17	○	○	○	○	○	○
		P30	○	○	○	○	○	○
		P54	○	○	○	○	○	○
		PC2	○	○	○	○	○	○
		PD1	○	○	○	○	○	○
		PE3	○	○	○	○	○	○
	MTIOC4C (input/output)	P25	○	○	○	○	○	○
		P83	○	○	○	○	○	○
		P87	○	○	○	○	○	○
		PB1	○	○	○	○	○	○
		PE1	○	○	○	○	○	○
		PE5	○	○	○	○	○	○
	MTIOC4D (input/output)	P31	○	○	○	○	○	○
		P55	○	○	○	○	○	○
		P86	○	○	○	○	○	○
		PC3	○	○	○	○	○	○
		PD2	○	○	○	○	○	○
		PE4	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			224-Pin	176-Pin	224-Pin	176-Pin	224-Pin	176-Pin
Multi-function timer pulse unit 3	MTIC5U (input)	P12	○	○	○	○	○	○
		PA4	○	○	○	○	○	○
		PD7	○	○	○	○	○	○
	MTIC5V (input)	P11	○	○	○	○	○	○
		PA6	○	○	○	○	○	○
		PD6	○	○	○	○	○	○
	MTIC5W (input)	P10	○	○	○	○	○	○
		PB0	○	○	○	○	○	○
		PD5	○	○	○	○	○	○
	MTIOC6A (input/output)	PE7	○	○	○	○	○	○
		PJ1	○	○	○	○	○	○
	MTIOC6B (input/output)	PA5	○	○	○	○	○	○
		PJ0	○	○	○	○	○	○
	MTIOC6C (input/output)	P85	○	○	○	○	○	○
		PE6	○	○	○	○	○	○
	MTIOC6D (input/output)	P84	○	○	○	○	○	○
		PA0	○	○	○	○	○	○
	MTIOC7A (input/output)	PA2	○	○	○	○	○	○
	MTIOC7B (input/output)	PA1	○	○	○	○	○	○
	MTIOC7C (input/output)	P67	○	○	○	○	○	○
	MTIOC7D (input/output)	P66	○	○	○	○	○	○
	MTIOC8A (input/output)	PD6	○	○	○	○	○	○
	MTIOC8B (input/output)	PD4	○	○	○	○	○	○
	MTIOC8C (input/output)	PD5	○	○	○	○	○	○
	MTIOC8D (input/output)	PD3	○	○	○	○	○	○
	MTCLKA (input)	P14	○	○	○	○	○	○
		P24	○	○	○	○	○	○
		PA4	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
		PD5	○	○	○	○	○	○
	MTCLKB (input)	P15	○	○	○	○	○	○
		P25	○	○	○	○	○	○
		PA6	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	MTCLKC (input)	P22	○	○	○	○	○	○
		PA1	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	MTCLKD (input)	P23	○	○	○	○	○	○
		PA3	○	○	○	○	○	○
		PC5	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			224-Pin	176-Pin	224-Pin	176-Pin	224-Pin	176-Pin
Port output enable 3	POE0# (input)	P32	○	○	○	○	○	○
		P93	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
		PD1	○	○	○	○	○	○
		PD7	○	○	○	○	○	○
	POE4# (input)	P33	○	○	○	○	○	○
		P92	○	○	○	○	○	○
		PB5	○	○	○	○	○	○
		PD0	○	○	○	○	○	○
		PD6	○	○	○	○	○	○
	POE8# (input)	P17	○	○	○	○	○	○
		P30	○	○	○	○	○	○
		PD3	○	○	○	○	○	○
		PE3	○	○	○	○	○	○
		PJ5	○	○	○	○	○	○
	POE10# (input)	P32	○	○	○	○	○	○
		P34	○	○	○	○	○	○
		PA6	○	○	○	○	○	○
		PD5	○	○	○	○	○	○
	POE11# (input)	P33	○	○	○	○	○	○
		PB3	○	○	○	○	○	○
		PD4	○	○	○	○	○	○
General PWM timer W	GTADSM0 (output)	P12	○	○	○	○	○	○
		PH4	○	×	○	×	○	×
		PK4	○	×	○	×	○	×
		PL4	○	×	○	×	○	×
		PM4	○	×	○	×	○	×
	GTADSM1 (output)	P13	○	○	○	○	○	○
		PH5	○	×	○	×	○	×
		PK5	○	×	○	×	○	×
		PL5	○	×	○	×	○	×
		PM5	○	×	○	×	○	×
	GTETRGA (input)	P15	○	○	○	○	○	○
		PH0	○	×	○	×	○	×
		PK0	○	×	○	×	○	×
		PL0	○	×	○	×	○	×
		PM0	○	×	○	×	○	×
	GTETRGB (input)	PA6	○	○	○	○	○	○
		PH1	○	×	○	×	○	×
		PK1	○	×	○	×	○	×
		PL1	○	×	○	×	○	×
		PM1	○	×	○	×	○	×
	GTETRGC (input)	PC4	○	○	○	○	○	○
		PH2	○	×	○	×	○	×
		PK2	○	×	○	×	○	×
		PL2	○	×	○	×	○	×
		PM2	○	×	○	×	○	×

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			224-Pin	176-Pin	224-Pin	176-Pin	224-Pin	176-Pin
General PWM timer W	GTETRGD (input)	P14	○	○	○	○	○	○
		PH3	○	×	○	×	○	×
		PK3	○	×	○	×	○	×
		PL3	○	×	○	×	○	×
		PM3	○	×	○	×	○	×
	GTIOC0A (input/output)	P23	○	○	○	○	○	○
		P83	○	○	○	○	○	○
		PA5	○	○	○	○	○	○
		PD3	○	○	○	○	○	○
		PE5	○	○	○	○	○	○
		PH6	○	×	○	×	○	×
	GTIOC0B (input/output)	P17	○	○	○	○	○	○
		P81	○	○	○	○	○	○
		PA0	○	○	○	○	○	○
		PD2	○	○	○	○	○	○
		PE2	○	○	○	○	○	○
		PH7	○	×	○	×	○	×
	GTIOC1A (input/output)	P22	○	○	○	○	○	○
		PA2	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
		PD1	○	○	○	○	○	○
		PE4	○	○	○	○	○	○
		PK6	○	×	○	×	○	×
	GTIOC1B (input/output)	P67	○	○	○	○	○	○
		P87	○	○	○	○	○	○
		PC3	○	○	○	○	○	○
		PD0	○	○	○	○	○	○
		PE1	○	○	○	○	○	○
		PK7	○	×	○	×	○	×
	GTIOC2A (input/output)	P21	○	○	○	○	○	○
		P82	○	○	○	○	○	○
		PA1	○	○	○	○	○	○
		PE3	○	○	○	○	○	○
		PL6	○	×	○	×	○	×
	GTIOC2B (input/output)	P66	○	○	○	○	○	○
		P86	○	○	○	○	○	○
		PC2	○	○	○	○	○	○
		PE0	○	○	○	○	○	○
		PL7	○	×	○	×	○	×
	GTIOC3A (input/output)	PC7	○	○	○	○	○	○
		PE7	○	○	○	○	○	○
		PM6	○	×	○	×	○	×
	GTIOC3B (input/output)	PC6	○	○	○	○	○	○
		PE6	○	○	○	○	○	○
		PM7	○	×	○	×	○	×

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			224-Pin	176-Pin	224-Pin	176-Pin	224-Pin	176-Pin
16-bit timer pulse unit	TIOCA0 (input/output)	P86	○	○	○	○	○	○
		PA0	○	○	○	○	○	○
	TIOCB0 (input/output)	P17	○	○	○	○	○	○
		PA1	○	○	○	○	○	○
	TIOCC0 (input/output)	P32	○	○	○	○	○	○
		P85	○	○	○	○	○	○
	TIOCD0 (input/output)	P33	○	○	○	○	○	○
		PA3	○	○	○	○	○	○
	TIOCA1 (input/output)	P56	○	○	○	○	○	○
		PA4	○	○	○	○	○	○
	TIOCB1 (input/output)	P16	○	○	○	○	○	○
		PA5	○	○	○	○	○	○
	TIOCA2 (input/output)	P87	○	○	○	○	○	○
		PA6	○	○	○	○	○	○
	TIOCB2 (input/output)	P15	○	○	○	○	○	○
		PA7	○	○	○	○	○	○
	TIOCA3 (input/output)	P21	○	○	○	○	○	○
		PB0	○	○	○	○	○	○
	TIOCB3 (input/output)	P20	○	○	○	○	○	○
		PB1	○	○	○	○	○	○
	TIOCC3 (input/output)	P22	○	○	○	○	○	○
		PB2	○	○	○	○	○	○
	TIOCD3 (input/output)	P23	○	○	○	○	○	○
		PB3	○	○	○	○	○	○
	TIOCA4 (input/output)	P25	○	○	○	○	○	○
		PB4	○	○	○	○	○	○
	TIOCB4 (input/output)	P24	○	○	○	○	○	○
		PB5	○	○	○	○	○	○
	TIOCA5 (input/output)	P13	○	○	○	○	○	○
		PB6	○	○	○	○	○	○
	TIOCB5 (input/output)	P14	○	○	○	○	○	○
		PB7	○	○	○	○	○	○
	TCLKA (input)	P14	○	○	○	○	○	○
		PC2	○	○	○	○	○	○
	TCLKB (input)	P15	○	○	○	○	○	○
		PA3	○	○	○	○	○	○
		PC3	○	○	○	○	○	○
	TCLKC (input)	P16	○	○	○	○	○	○
		PB2	○	○	○	○	○	○
		PC0	○	○	○	○	○	○
	TCLKD (input)	P17	○	○	○	○	○	○
		PB3	○	○	○	○	○	○
		PC1	○	○	○	○	○	○
Programmable pulse generator	PO0 (output)	P20	○	○	○	○	○	○
	PO1 (output)	P21	○	○	○	○	○	○
	PO2 (output)	P22	○	○	○	○	○	○
	PO3 (output)	P23	○	○	○	○	○	○
	PO4 (output)	P24	○	○	○	○	○	○
	PO5 (output)	P25	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			224-Pin	176-Pin	224-Pin	176-Pin	224-Pin	176-Pin
Programmable pulse generator	PO6 (output)	P26	○	○	○	○	○	○
	PO7 (output)	P27	○	○	○	○	○	○
	PO8 (output)	P30	○	○	○	○	○	○
	PO9 (output)	P31	○	○	○	○	○	○
	PO10 (output)	P32	○	○	○	○	○	○
	PO11 (output)	P33	○	○	○	○	○	○
	PO12 (output)	P34	○	○	○	○	○	○
	PO13 (output)	P13	○	○	○	○	○	○
		P15	○	○	○	○	○	○
	PO14 (output)	P16	○	○	○	○	○	○
	PO15 (output)	P14	○	○	○	○	○	○
		P17	○	○	○	○	○	○
	PO16 (output)	P73	○	○	○	○	○	○
		PA0	○	○	○	○	○	○
	PO17 (output)	PA1	○	○	○	○	○	○
		PC0	○	○	○	○	○	○
	PO18 (output)	PA2	○	○	○	○	○	○
		PC1	○	○	○	○	○	○
		PE1	○	○	○	○	○	○
	PO19 (output)	P74	○	○	○	○	○	○
		PA3	○	○	○	○	○	○
	PO20 (output)	P75	○	○	○	○	○	○
		PA4	○	○	○	○	○	○
	PO21 (output)	PA5	○	○	○	○	○	○
		PC2	○	○	○	○	○	○
	PO22 (output)	P76	○	○	○	○	○	○
		PA6	○	○	○	○	○	○
	PO23 (output)	P77	○	○	○	○	○	○
		PA7	○	○	○	○	○	○
		PE2	○	○	○	○	○	○
	PO24 (output)	PB0	○	○	○	○	○	○
		PC3	○	○	○	○	○	○
	PO25 (output)	PB1	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	PO26 (output)	P80	○	○	○	○	○	○
		PB2	○	○	○	○	○	○
		PE3	○	○	○	○	○	○
	PO27 (output)	P81	○	○	○	○	○	○
		PB3	○	○	○	○	○	○
	PO28 (output)	P82	○	○	○	○	○	○
		PB4	○	○	○	○	○	○
		PE4	○	○	○	○	○	○
	PO29 (output)	PB5	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
	PO30 (output)	PB6	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	PO31 (output)	PB7	○	○	○	○	○	○
		PC7	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			224-Pin	176-Pin	224-Pin	176-Pin	224-Pin	176-Pin
8-bit timer	TMO0 (output)	P22	○	○	○	○	○	○
		PB3	○	○	○	○	○	○
	TMCI0 (input)	P01	○	○	○	○	○	○
		P21	○	○	○	○	○	○
		PB1	○	○	○	○	○	○
	TMRI0 (input)	P00	○	○	○	○	○	○
		P20	○	○	○	○	○	○
		PA4	○	○	○	○	○	○
	TMO1 (output)	P17	○	○	○	○	○	○
		P26	○	○	○	○	○	○
	TMCI1 (input)	P02	○	○	○	○	○	○
		P12	○	○	○	○	○	○
		P54	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	TMRI1 (input)	P24	○	○	○	○	○	○
		PB5	○	○	○	○	○	○
	TMO2 (output)	P16	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	TMCI2 (input)	P15	○	○	○	○	○	○
		P31	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	TMRI2 (input)	P14	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
	TMO3 (output)	P13	○	○	○	○	○	○
		P32	○	○	○	○	○	○
		P55	○	○	○	○	○	○
	TMCI3 (input)	P11	○	○	○	○	○	○
		P27	○	○	○	○	○	○
		P34	○	○	○	○	○	○
		PA6	○	○	○	○	○	○
	TMRI3 (input)	P10	○	○	○	○	○	○
		P30	○	○	○	○	○	○
		P33	○	○	○	○	○	○
Compare match timer W	TOC0 (output)	PC7	○	○	○	○	○	○
		PH1	○	×	○	×	○	×
	TIC0 (input)	PC6	○	○	○	○	○	○
		PH0	○	×	○	×	○	×
	TOC1 (output)	PE7	○	○	○	○	○	○
		PK1	○	×	○	×	○	×
	TIC1 (input)	PE6	○	○	○	○	○	○
		PK0	○	×	○	×	○	×
	TOC2 (output)	PD3	○	○	○	○	○	○
		PL1	○	×	○	×	○	×
	TIC2 (input)	PD2	○	○	○	○	○	○
		PL0	○	×	○	×	○	×
	TOC3 (output)	PE3	○	○	○	○	○	○
		PM1	○	×	○	×	○	×
	TIC3 (input)	PE2	○	○	○	○	○	○
		PM0	○	×	○	×	○	×

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			224-Pin	176-Pin	224-Pin	176-Pin	224-Pin	176-Pin
Realtime clock	RTCOUT (output)	P16	○	○	○	○	○	○
		P32	○	○	○	○	○	○
	RTCIC0 (input)*1	P30	○	○	○	○	○	○
	RTCIC1 (input)*1	P31	○	○	○	○	○	○
	RTCIC2 (input)*1	P32	○	○	○	○	○	○
PTP module for the Ethernet controller	EPLSOUT0 (output)	P17	○	○	○	○		
		PJ0	○	○	○	○		
		PJ5	○	○	○	○		
	EPLSOUT1 (output)	P11	○	○	○	○		
		P67	○	○	○	○		
		P87	○	○	○	○		
		PJ1	○	○	○	○		
Ethernet controller	REF50CK0 (input)	P76	○	○	○	○	○	○
		PB2	○	○	○	○	○	○
		PE5	○	○	○	○	○	○
		PL3	○	×	○	×	○	×
	RMII0_CRS_DV (input)	P83	○	○	○	○	○	○
		PB7	○	○	○	○	○	○
		PM7	○	×	○	×	○	×
	RMII0_TXD0 (output)	P81	○	○	○	○	○	○
		PB5	○	○	○	○	○	○
		PL4	○	×	○	×	○	×
	RMII0_TXD1 (output)	P82	○	○	○	○	○	○
		PB6	○	○	○	○	○	○
		PL5	○	×	○	×	○	×
	RMII0_RXD0 (input)	P75	○	○	○	○	○	○
		PB1	○	○	○	○	○	○
		PL0	○	×	○	×	○	×
	RMII0_RXD1 (input)	P74	○	○	○	○	○	○
		PB0	○	○	○	○	○	○
		PL1	○	×	○	×	○	×
	RMII0_TXD_EN (output)	P80	○	○	○	○	○	○
		PA0	○	○	○	○	○	○
		PB4	○	○	○	○	○	○
		PL6	○	×	○	×	○	×
	RMII0_RX_ER (input)	P77	○	○	○	○	○	○
		PB3	○	○	○	○	○	○
		PL2	○	×	○	×	○	×
	REF50CK1 (input)	PD6	○	○	○	○		
		PG0	○	○	○	○		
		PQ4	○	×	○	×		
	RMII1_CRS_DV (input)	P92	○	○	○	○		
		PQ0	○	×	○	×		
	RMII1_TXD0 (output)	P64	○	○	○	○		
		PG3	○	○	○	○		
		PQ5	○	×	○	×		
	RMII1_TXD1 (output)	P63	○	○	○	○		
		PG4	○	○	○	○		
		PQ6	○	×	○	×		

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			224-Pin	176-Pin	224-Pin	176-Pin	224-Pin	176-Pin
Ethernet controller	RMII1_RXD0 (input)	P62	○	○	○	○		
		P94	○	○	○	○		
		PM0	○	×	○	×		
	RMII1_RXD1 (input)	P61	○	○	○	○		
		P95	○	○	○	○		
		PM1	○	×	○	×		
	RMII1_TXD_EN (output)	P60	○	○	○	○		
		PQ7	○	×	○	×		
	RMII1_RX_ER (input)	PD7	○	○	○	○		
		PG1	○	○	○	○		
		PN3	○	×	○	×		
	ET0_CRS (input)	P83	○	○	○	○	○	○
		PB7	○	○	○	○	○	○
		PM7	○	×	○	×	○	×
	ET0_RX_DV (input)	PC2	○	○	○	○	○	○
		PK2	○	×	○	×	○	×
	ET0_EXOUT (output)	P55	○	○	○	○	○	○
		PA6	○	○	○	○	○	○
		PJ3	○	○	○	○	○	○
	ET0_LINKSTA (input)	P34	○	○	○	○	○	○
		P54	○	○	○	○	○	○
		PA5	○	○	○	○	○	○
	ET0_ETXD0 (output)	P81	○	○	○	○	○	○
		PB5	○	○	○	○	○	○
		PL4	○	×	○	×	○	×
	ET0_ETXD1 (output)	P82	○	○	○	○	○	○
		PB6	○	○	○	○	○	○
		PL5	○	×	○	×	○	×
	ET0_ETXD2 (output)	PC5	○	○	○	○	○	○
		PM4	○	×	○	×	○	×
	ET0_ETXD3 (output)	PC6	○	○	○	○	○	○
		PM5	○	×	○	×	○	×
	ET0_ERXD0 (input)	P75	○	○	○	○	○	○
		PB1	○	○	○	○	○	○
		PL0	○	×	○	×	○	×
	ET0_ERXD1 (input)	P74	○	○	○	○	○	○
		PB0	○	○	○	○	○	○
		PL1	○	×	○	×	○	×
	ET0_ERXD2 (input)	PC1	○	○	○	○	○	○
		PE4	○	○	○	○	○	○
		PK4	○	×	○	×	○	×
	ET0_ERXD3 (input)	PC0	○	○	○	○	○	○
		PE3	○	○	○	○	○	○
		PK5	○	×	○	×	○	×
	ET0_TX_EN (output)	P80	○	○	○	○	○	○
		PA0	○	○	○	○	○	○
		PB4	○	○	○	○	○	○
		PL6	○	×	○	×	○	×

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			224-Pin	176-Pin	224-Pin	176-Pin	224-Pin	176-Pin
Ethernet controller	ET0_TX_ER (output)	PC3	○	○	○	○	○	○
		PK3	○	×	○	×	○	×
	ET0_RX_ER (input)	P77	○	○	○	○	○	○
		PB3	○	○	○	○	○	○
		PL2	○	×	○	×	○	×
	ET0_TX_CLK (input)	PC4	○	○	○	○	○	○
		PM6	○	×	○	×	○	×
	ET0_RX_CLK (input)	P76	○	○	○	○	○	○
		PB2	○	○	○	○	○	○
		PE5	○	○	○	○	○	○
		PL3	○	×	○	×	○	×
	ET0_COL (input)	PC7	○	○	○	○	○	○
		PK1	○	×	○	×	○	×
	ET0_WOL (output)	P73	○	○	○	○	○	○
		PA1	○	○	○	○	○	○
		PA7	○	○	○	○	○	○
	ET0_MDC (output)	P72	○	○	○	○	○	○
		PA4	○	○	○	○	○	○
		PK0	○	×	○	×	○	×
	ET0_MDIO (input/output)	P71	○	○	○	○	○	○
		PA3	○	○	○	○	○	○
		PL7	○	×	○	×	○	×
	ET1_CRS (input)	P92	○	○	○	○		
		PQ0	○	×	○	×		
	ET1_RX_DV (input)	P90	○	○	○	○		
		PQ2	○	×	○	×		
	ET1_EXOUT (output)	P26	○	○	○	○		
		PD2	○	○	○	○		
	ET1_LINKSTA (input)	P84	○	○	○	○		
		P93	○	○	○	○		
	ET1_ETXD0 (output)	P64	○	○	○	○		
		PG3	○	○	○	○		
		PQ5	○	×	○	×		
	ET1_ETXD1 (output)	P63	○	○	○	○		
		PG4	○	○	○	○		
		PQ6	○	×	○	×		
	ET1_ETXD2 (output)	PG5	○	○	○	○		
		PN0	○	×	○	×		
	ET1_ETXD3 (output)	PG6	○	○	○	○		
		PN1	○	×	○	×		
	ET1_ERXD0 (input)	P62	○	○	○	○		
		P94	○	○	○	○		
		PM0	○	×	○	×		
	ET1_ERXD1 (input)	P61	○	○	○	○		
		P95	○	○	○	○		
		PM1	○	×	○	×		
	ET1_ERXD2 (input)	P96	○	○	○	○		
		PM2	○	×	○	×		

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			224-Pin	176-Pin	224-Pin	176-Pin	224-Pin	176-Pin
Ethernet controller	ET1_ERXD3 (input)	P97	○	○	○	○		
		PM3	○	×	○	×		
	ET1_TX_EN (output)	P60	○	○	○	○		
		PQ7	○	×	○	×		
	ET1_TX_ER (output)	PG7	○	○	○	○		
		PQ3	○	×	○	×		
	ET1_RX_ER (input)	PD7	○	○	○	○		
		PG1	○	○	○	○		
		PN3	○	×	○	×		
	ET1_TX_CLK (input)	PG2	○	○	○	○		
		PN2	○	×	○	×		
	ET1_RX_CLK (input)	PD6	○	○	○	○		
		PG0	○	○	○	○		
		PQ4	○	×	○	×		
	ET1_COL (input)	P91	○	○	○	○		
		PQ1	○	×	○	×		
	ET1_WOL (output)	P27	○	○	○	○		
		PD3	○	○	○	○		
	ET1_MDC (output)	P31	○	○	○	○		
		PD5	○	○	○	○		
		PN5	○	×	○	×		
	ET1_MDIO (input/output)	P30	○	○	○	○		
		PD4	○	○	○	○		
		PN4	○	×	○	×		
Ethernet PHY management interface	PMGI0_MDC (output)	P72	○	○	○	○	○	○
		PA4	○	○	○	○	○	○
		PK0	○	×	○	×	○	×
	PMGI0_MDIO (input/output)	P71	○	○	○	○	○	○
		PA3	○	○	○	○	○	○
		PL7	○	×	○	×	○	×
	PMGI1_MDC (output)	P31	○	○	○	○		
		PD5	○	○	○	○		
		PN5	○	×	○	×		
	PMGI1_MDIO (input/output)	P30	○	○	○	○		
		PD4	○	○	○	○		
		PN4	○	×	○	×		
EtherCAT slave controller	CAT0_LINKSTA (input)	P34	○	○				
		P54	○	○				
		PA5	○	○				
	CAT0_RX_CLK (input)	P76	○	○				
		PB2	○	○				
		PE5	○	○				
		PL3	○	×				
	CAT0_RX_DV (input)	P83	○	○				
		PB7	○	○				
		PC2	○	○				
		PK2	○	×				
		PM7	○	×				

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			224-Pin	176-Pin	224-Pin	176-Pin	224-Pin	176-Pin
EtherCAT slave controller	CAT0_ERXD0 (input)	P75	○	○				
		PB1	○	○				
		PL0	○	×				
	CAT0_ERXD1 (input)	P74	○	○				
		PB0	○	○				
		PL1	○	×				
	CAT0_ERXD2 (input)	PC1	○	○				
		PE4	○	○				
		PK4	○	×				
	CAT0_ERXD3 (input)	PC0	○	○				
		PE3	○	○				
		PK5	○	×				
	CAT0_RX_ER (input)	P77	○	○				
		PB3	○	○				
		PL2	○	×				
	CAT0_TX_CLK (input)	PC4	○	○				
		PM6	○	×				
	CAT0_TX_EN (output)	P80	○	○				
		PA0	○	○				
		PB4	○	○				
		PL6	○	×				
	CAT0_ETXD0 (output)	P81	○	○				
		PB5	○	○				
		PL4	○	×				
	CAT0_ETXD1 (output)	P82	○	○				
		PB6	○	○				
		PL5	○	×				
	CAT0_ETXD2 (output)	PC5	○	○				
		PM4	○	×				
	CAT0_ETXD3 (output)	PC6	○	○				
		PM5	○	×				
	CAT0_MDC (output)	P72	○	○				
		PA4	○	○				
		PK0	○	×				
	CAT0_MDIO (input/output)	P71	○	○				
		PA3	○	○				
		PL7	○	×				
	CAT1_LINKSTA (input)	P84	○	○				
		P93	○	○				
	CAT1_RX_CLK (input)	PD6	○	○				
		PG0	○	○				
		PQ4	○	×				
	CAT1_RX_DV (input)	P90	○	○				
		P92	○	○				
		PQ0	○	×				
		PQ2	○	×				
	CAT1_ERXD0 (input)	P62	○	○				
		P94	○	○				
		PM0	○	×				

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			224-Pin	176-Pin	224-Pin	176-Pin	224-Pin	176-Pin
EtherCAT slave controller	CAT1_ERXD1 (input)	P61	○	○				
		P95	○	○				
		PM1	○	×				
	CAT1_ERXD2 (input)	P96	○	○				
		PM2	○	×				
	CAT1_ERXD3 (input)	P97	○	○				
		PM3	○	×				
	CAT1_RX_ER (input)	PD7	○	○				
		PG1	○	○				
		PN3	○	×				
	CAT1_TX_CLK (input)	PG2	○	○				
		PN2	○	×				
	CAT1_TX_EN (output)	P60	○	○				
		PQ7	○	×				
	CAT1_ETXD0 (output)	P64	○	○				
		PG3	○	○				
		PQ5	○	×				
	CAT1_ETXD1 (output)	P63	○	○				
		PG4	○	○				
		PQ6	○	×				
	CAT1_ETXD2 (output)	PG5	○	○				
		PN0	○	×				
	CAT1_ETXD3 (output)	PG6	○	○				
		PN1	○	×				
	CATRESTOUT (output)	PA6	○	○				
		PJ3	○	○				
	CATLEDRUN (output)	P15	○	○				
		PA0	○	○				
		PH0	○	×				
	CATIRQ (output)	P27	○	○				
		PA4	○	○				
	CATLEDSTER (output)	P02	○	○				
		P52	○	○				
		PH4	○	×				
	CATLEDERR (output)	P01	○	○				
		P50	○	○				
		PH3	○	×				
	CATLINKACT0 (output)	P70	○	○				
		P86	○	○				
		PK6	○	×				
	CATLINKACT1 (output)	P26	○	○				
		PA2	○	○				
		PK7	○	×				
	CATSYNC0 (output)	P17	○	○				
		PC4	○	○				
		PJ0	○	○				
		PJ5	○	○				

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			224-Pin	176-Pin	224-Pin	176-Pin	224-Pin	176-Pin
EtherCAT slave controller	CATSYNC1 (output)	P11	○	○				
		P67	○	○				
		P87	○	○				
		PJ1	○	○				
	CATLATCH0 (input)	P80	○	○				
		PF5	○	○				
		PH5	○	×				
	CATLATCH1 (input)	P00	○	○				
		PC6	○	○				
		PH6	○	×				
	CATI2CCLK (output)	P81	○	○				
		PF2	○	○				
		PH1	○	×				
	CATI2CDATA (input/output)	P82	○	○				
		PF0	○	○				
		PH2	○	×				
Serial communications interface	CTS0# (input)/ RTS0# (output)/ SS0# (input)	P23	○	○	○	○	○	○
		PJ3	○	○	○	○	○	○
	RXD0 (input)/ SMISO0 (input/output)/ SSCL0 (input/output)	P21	○	○	○	○	○	○
		P33	○	○	○	○	○	○
	SCK0 (input/output)	P22	○	○	○	○	○	○
		P34	○	○	○	○	○	○
	SMOSI0 (input/output)/ SSDA0 (input/output)/ TXD0 (output)	P20	○	○	○	○	○	○
		P32	○	○	○	○	○	○
	CTS1# (input)/ RTS1# (output)/ SS1# (input)	P14	○	○	○	○	○	○
		P31	○	○	○	○	○	○
	RXD1 (input)/ SMISO1 (input/output)/ SSCL1 (input/output)	P15	○	○	○	○	○	○
		P30	○	○	○	○	○	○
		PF2	○	○	○	○	○	○
	SCK1 (input/output)	P17	○	○	○	○	○	○
		P27	○	○	○	○	○	○
		PF1	○	○	○	○	○	○
	SMOSI1 (input/output)/ SSDA1 (input/output)/ TXD1 (output)	P16	○	○	○	○	○	○
		P26	○	○	○	○	○	○
		PF0	○	○	○	○	○	○
	CTS2# (input)/ RTS2# (output)/ SS2# (input)	P54	○	○	○	○	○	○
		PJ5	○	○	○	○	○	○
	RXD2 (input)/ SMISO2 (input/output)/ SSCL2 (input/output)	P12	○	○	○	○	○	○
		P52	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			224-Pin	176-Pin	224-Pin	176-Pin	224-Pin	176-Pin
Serial communications interface	SCK2 (input/output)	P11	○	○	○	○	○	○
		P51	○	○	○	○	○	○
	SMOSI2 (input/output)/ SSDA2 (input/output)/ TXD2 (output)	P13	○	○	○	○	○	○
		P50	○	○	○	○	○	○
	CTS3# (input)/ RTS3# (output)/ SS3# (input)	P26	○	○	○	○	○	○
	RXD3 (input)/ SMISO3 (input/output)/ SSCL3 (input/output)	P16	○	○	○	○	○	○
		P25	○	○	○	○	○	○
	SCK3 (input/output)	P15	○	○	○	○	○	○
		P24	○	○	○	○	○	○
	SMOSI3 (input/output)/ SSDA3 (input/output)/ TXD3 (output)	P17	○	○	○	○	○	○
		P23	○	○	○	○	○	○
	CTS4# (input)/ RTS4# (output)/ SS4# (input)	PB2	○	○	○	○	○	○
	RXD4 (input)/ SMISO4 (input/output)/ SSCL4 (input/output)	PB0	○	○	○	○	○	○
	SCK4 (input/output)	PB3	○	○	○	○	○	○
	SMOSI4 (input/output)/ SSDA4 (input/output)/ TXD4 (output)	PB1	○	○	○	○	○	○
	CTS5# (input)/ RTS5# (output)/ SS5# (input)	PA6	○	○	○	○	○	○
		PC0	○	○	○	○	○	○
	RXD5 (input)/ SMISO5 (input/output)/ SSCL5 (input/output)	PA2	○	○	○	○	○	○
		PA3	○	○	○	○	○	○
		PC2	○	○	○	○	○	○
	SCK5 (input/output)	PA1	○	○	○	○	○	○
		PC1	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	SMOSI5 (input/output)/ SSDA5 (input/output)/ TXD5 (output)	PA4	○	○	○	○	○	○
		PC3	○	○	○	○	○	○
	CTS6# (input)/ RTS6# (output)/ SS6# (input)	PB2	○	○	○	○	○	○
		PJ3	○	○	○	○	○	○
	RXD6 (input)/ SMISO6 (input/output)/ SSCL6 (input/output)	P01	○	○	○	○	○	○
		P33	○	○	○	○	○	○
		PB0	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			224-Pin	176-Pin	224-Pin	176-Pin	224-Pin	176-Pin
Serial communications interface	SCK6 (input/output)	P02	○	○	○	○	○	○
		P34	○	○	○	○	○	○
		PB3	○	○	○	○	○	○
	SMOSI6 (input/output)/ SSDA6 (input/output)/ TXD6 (output)	P00	○	○	○	○	○	○
		P32	○	○	○	○	○	○
		PB1	○	○	○	○	○	○
	CTS7# (input)/ RTS7# (output)/ SS7# (input)	P93	○	○	○	○	○	○
		PH3	○	×	○	×	○	×
	RXD7 (input)/ SMISO7 (input/output)/ SSCL7 (input/output)	P57	○	○	○	○	○	○
		P92	○	○	○	○	○	○
		PH1	○	×	○	×	○	×
	SCK7 (input/output)	P56	○	○	○	○	○	○
		P91	○	○	○	○	○	○
		PH0	○	×	○	×	○	×
	SMOSI7 (input/output)/ SSDA7 (input/output)/ TXD7 (output)	P55	○	○	○	○	○	○
		P90	○	○	○	○	○	○
		PH2	○	×	○	×	○	×
	CTS8# (input)/ SS8# (input)	PC4	○	○	○	○	○	○
	RTS8# (output)/ CTS8# (input)/ SS8# (input)	PK3	○	×	○	×	○	×
	RTS8# (output)/ SCK8 (input/output)	PC5	○	○	○	○	○	○
	RXD8 (input)/ SMISO8 (input/output)/ SSCL8 (input/output)	PC6	○	○	○	○	○	○
		PJ1	○	○	○	○	○	○
		PK1	○	×	○	×	○	×
	SCK8 (input/output)	PJ0	○	○	○	○	○	○
		PK0	○	×	○	×	○	×
	SMOSI8 (input/output)/ SSDA8 (input/output)/ TXD8 (output)	PC7	○	○	○	○	○	○
		PJ2	○	○	○	○	○	○
		PK2	○	×	○	×	○	×
	CTS9# (input)/ SS9# (input)	PB4	○	○	○	○	○	○
	RTS9# (output)/ CTS9# (input)/ SS9# (input)	PL3	○	×	○	×	○	×
	RTS9# (output)/ SCK9 (input/output)	PB5	○	○	○	○	○	○
	RXD9 (input)/ SMISO9 (input/output)/ SSCL9 (input/output)	PB6	○	○	○	○	○	○
		PL1	○	×	○	×	○	×
	SCK9 (input/output)	PL0	○	×	○	×	○	×

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			224-Pin	176-Pin	224-Pin	176-Pin	224-Pin	176-Pin
Serial communications interface	SMOSI9 (input/output)/ SSDA9 (input/output)/ TXD9 (output)	PB7	○	○	○	○	○	○
		PL2	○	×	○	×	○	×
	CTS10# (input)/ RTS10# (output)/ SS10# (input)	PC4	○	○	○	○	○	○
	CTS10# (input)/ SCK10 (input/output)/ SS10# (input)	P83	○	○	○	○	○	○
	RTS10# (output)/ CTS10# (input)/ SS10# (input)	PM3	○	×	○	×	○	×
	RTS10# (output)/ SCK10 (input/output)	P80	○	○	○	○	○	○
	RXD10 (input)/ SMISO10 (input/output)/ SSCL10 (input/output)	P81	○	○	○	○	○	○
		P86	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
		PM1	○	×	○	×	○	×
	SCK10 (input/output)	PC5	○	○	○	○	○	○
		PM0	○	×	○	×	○	×
	SMOSI10 (input/output)/ SSDA10 (input/output)/ TXD10 (output)	P82	○	○	○	○	○	○
		P87	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
		PM2	○	×	○	×	○	×
	CTS11# (input)/ RTS11# (output)/ SS11# (input)	PB4	○	○	○	○	○	○
	CTS11# (input)/ SS11# (input)	P74	○	○	○	○	○	○
	RTS11# (output)/ CTS11# (input)/ SS11# (input)	PQ3	○	×	○	×	○	×
	RTS11# (output)/ SCK11 (input/output)	P75	○	○	○	○	○	○
	RXD11 (input)/ SMISO11 (input/output)/ SSCL11 (input/output)	P76	○	○	○	○	○	○
		PB6	○	○	○	○	○	○
		PQ1	○	×	○	×	○	×
	SCK11 (input/output)	PB5	○	○	○	○	○	○
		PQ0	○	×	○	×	○	×
	SMOSI11 (input/output)/ SSDA11 (input/output)/ TXD11 (output)	P77	○	○	○	○	○	○
		PB7	○	○	○	○	○	○
		PQ2	○	×	○	×	○	×
	CTS12# (input)/ RTS12# (output)/ SS12# (input)	PE3	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			224-Pin	176-Pin	224-Pin	176-Pin	224-Pin	176-Pin
Serial communications interface	RXD12 (input)/ RXDX12 (input)/ SMISO12 (input/output)/ SSCL12 (input/output)	PE2	○	○	○	○	○	○
	SCK12 (input/output)	PE0	○	○	○	○	○	○
	SMOSI12 (input/output)/ SSDA12 (input/output)/ TXD12 (output)/ TXDX12 (output)/ SIOX12 (input/output)	PE1	○	○	○	○	○	○
I^2C bus interface	SCL0[FM+] (input/output)	P12	○	○	○	○	○	○
	SDA0[FM+] (input/output)	P13	○	○	○	○	○	○
	SCL1 (input/output)	P21	○	○	○	○	○	○
	SDA1 (input/output)	P20	○	○	○	○	○	○
	SCL2-DS (input/output)	P16	○	○	○	○	○	○
	SDA2-DS (input/output)	P17	○	○	○	○	○	○
USB 2.0 FS Host/Function module	USB0_VBUS (input)	P16	○	○	○	○	○	○
	USB0_EXICEN (output)	P21	○	○	○	○	○	○
	USB0_VBUSEN (output)	P16	○	○	○	○	○	○
		P24	○	○	○	○	○	○
		P32	○	○	○	○	○	○
	USB0_OVRCURA (input)/ USB0_OVRCURA-DS (input)	P14	○	○	○	○	○	○
	USB0_OVRCURB (input)	P16	○	○	○	○	○	○
		P22	○	○	○	○	○	○
	USB0_ID (input)	P20	○	○	○	○	○	○
CAN module	CRX0 (input)	P33	○	○	○	○	○	○
		PD2	○	○	○	○	○	○
	CTX0 (output)	P32	○	○	○	○	○	○
		PD1	○	○	○	○	○	○
	CRX1-DS (input)	P15	○	○	○	○	○	○
	CRX1 (input)	P55	○	○	○	○	○	○
	CTX1 (output)	P14	○	○	○	○	○	○
		P23	○	○	○	○	○	○
		P54	○	○	○	○	○	○
	CRX2 (input)	P67	○	○	○	○	○	○
	CTX2 (output)	P66	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			224-Pin	176-Pin	224-Pin	176-Pin	224-Pin	176-Pin
Serial peripheral interface	RSPCKA (input/output)	PA5	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
		PH0	○	×	○	×	○	×
	MOSIA (input/output)	PA6	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
		PH1	○	×	○	×	○	×
	MISOA (input/output)	PA7	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
		PH2	○	×	○	×	○	×
	SSLA0 (output)	PA4	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
		PH3	○	×	○	×	○	×
	SSLA1 (output)	PA0	○	○	○	○	○	○
		PC0	○	○	○	○	○	○
		PH4	○	×	○	×	○	×
	SSLA2 (output)	PA1	○	○	○	○	○	○
		PC1	○	○	○	○	○	○
		PH5	○	×	○	×	○	×
	SSLA3 (output)	PA2	○	○	○	○	○	○
		PC2	○	○	○	○	○	○
		PH6	○	×	○	×	○	×
	RSPCKB (input/output)	P27	○	○	○	○	○	○
		PE5	○	○	○	○	○	○
		PK0	○	×	○	×	○	×
	MOSIB (input/output)	P26	○	○	○	○	○	○
		PE6	○	○	○	○	○	○
		PK1	○	×	○	×	○	×
	MISOB (input/output)	P30	○	○	○	○	○	○
		PE7	○	○	○	○	○	○
		PK2	○	×	○	×	○	×
	SSLB0 (output)	P31	○	○	○	○	○	○
		PE4	○	○	○	○	○	○
		PK3	○	×	○	×	○	×
	SSLB1 (output)	P50	○	○	○	○	○	○
		PE0	○	○	○	○	○	○
		PK4	○	×	○	×	○	×
	SSLB2 (output)	P51	○	○	○	○	○	○
		PE1	○	○	○	○	○	○
		PK5	○	×	○	×	○	×
	SSLB3 (output)	P52	○	○	○	○	○	○
		PE2	○	○	○	○	○	○
		PK6	○	×	○	×	○	×
	RSPCKC (input/output)	P56	○	○	○	○	○	○
		PD3	○	○	○	○	○	○
		PL0	○	×	○	×	○	×
	MOSIC (input/output)	P54	○	○	○	○	○	○
		PD1	○	○	○	○	○	○
		PL1	○	×	○	×	○	×

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			224-Pin	176-Pin	224-Pin	176-Pin	224-Pin	176-Pin
Serial peripheral interface	MISOC (input/output)	P55	○	○	○	○	○	○
		PD2	○	○	○	○	○	○
		PL2	○	×	○	×	○	×
	SSLC0 (output)	P57	○	○	○	○	○	○
		PD4	○	○	○	○	○	○
		PL3	○	×	○	×	○	×
	SSLC1 (output)	PD5	○	○	○	○	○	○
		PJ0	○	○	○	○	○	○
		PL4	○	×	○	×	○	×
	SSLC2 (output)	PD6	○	○	○	○	○	○
		PJ1	○	○	○	○	○	○
		PL5	○	×	○	×	○	×
	SSLC3 (output)	PD7	○	○	○	○	○	○
		PJ2	○	○	○	○	○	○
		PL6	○	×	○	×	○	×
Quad serial peripheral interface	QSPCLK (output)	P77	○	○	○	○	○	○
		PD5	○	○	○	○	○	○
		PM0	○	×	○	×	○	×
		PN4	○	×	○	×	○	×
	QSSL (output)	P76	○	○	○	○	○	○
		PD4	○	○	○	○	○	○
		PM1	○	×	○	×	○	×
		PN5	○	×	○	×	○	×
	QMO/QIO0 (input/output)	PC3	○	○	○	○	○	○
		PD6	○	○	○	○	○	○
		PJ3	○	×	○	×	○	×
		PM2	○	×	○	×	○	×
	QMI/QIO1 (input/output)	PC4	○	○	○	○	○	○
		PD7	○	○	○	○	○	○
		PJ5	○	×	○	×	○	×
		PM3	○	×	○	×	○	×
	QIO2 (input/output)	P00	○	×	○	×	○	×
		P80	○	○	○	○	○	○
		PD2	○	○	○	○	○	○
		PM4	○	×	○	×	○	×
	QIO3 (input/output)	P01	○	×	○	×	○	×
		P81	○	○	○	○	○	○
		PD3	○	○	○	○	○	○
		PM5	○	×	○	×	○	×
Enhanced serial sound interface	AUDIO_CLK (input)	P00	○	○	○	○	○	○
		P22	○	○	○	○	○	○
	SSIBCK0 (input/output)	P01	○	○	○	○	○	○
		P23	○	○	○	○	○	○
	SSILRCK0 (input/output)	P21	○	○	○	○	○	○
		PF5	○	○	○	○	○	○
	SSIRXD0 (input)	P20	○	○	○	○	○	○
		PJ5	○	○	○	○	○	○
	SSITXD0 (output)	P17	○	○	○	○	○	○
		PJ3	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			224-Pin	176-Pin	224-Pin	176-Pin	224-Pin	176-Pin
Enhanced serial sound interface	SSIBCK1 (input/output)	P02	○	○	○	○	○	○
		P24	○	○	○	○	○	○
	SSILRCK1 (input/output)	P05	○	○	○	○	○	○
		P15	○	○	○	○	○	○
	SSIDATA1 (input/output)	P03	○	○	○	○	○	○
		P25	○	○	○	○	○	○
SD host interface	SDHI_CLK (output)	P21	○	○	○	○	○	○
		P77	○	○	○	○	○	○
		PD5	○	○	○	○	○	○
		PM0	○	×	○	×	○	×
	SDHI_CMD (input/output)	P20	○	○	○	○	○	○
		P76	○	○	○	○	○	○
		PD4	○	○	○	○	○	○
		PM1	○	×	○	×	○	×
	SDHI_CD (input)	P25	○	○	○	○	○	○
		P81	○	○	○	○	○	○
		PE6	○	○	○	○	○	○
		PM6	○	×	○	×	○	×
	SDHI_WP (input)	P24	○	○	○	○	○	○
		P80	○	○	○	○	○	○
		PE7	○	○	○	○	○	○
		PM7	○	×	○	×	○	×
	SDHI_D0 (input/output)	P22	○	○	○	○	○	○
		PC3	○	○	○	○	○	○
		PD6	○	○	○	○	○	○
		PM2	○	×	○	×	○	×
	SDHI_D1 (input/output)	P23	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
		PD7	○	○	○	○	○	○
		PM3	○	×	○	×	○	×
	SDHI_D2 (input/output)	P75	○	○	○	○	○	○
		P87	○	○	○	○	○	○
		PD2	○	○	○	○	○	○
		PM4	○	×	○	×	○	×
	SDHI_D3 (input/output)	P17	○	○	○	○	○	○
		PC2	○	○	○	○	○	○
		PD3	○	○	○	○	○	○
		PM5	○	×	○	×	○	×
MultiMediaCard interface	MMC_RES# (output)	P75	○	○	○	○	○	○
		PE7	○	○	○	○	○	○
	MMC_CLK (output)	P77	○	○	○	○	○	○
		PD5	○	○	○	○	○	○
	MMC_CD (input)	PC2	○	○	○	○	○	○
		PE6	○	○	○	○	○	○
	MMC_CMD (input/output)	P76	○	○	○	○	○	○
		PD4	○	○	○	○	○	○
	MMC_D0 (input/output)	PC3	○	○	○	○	○	○
		PD6	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			224-Pin	176-Pin	224-Pin	176-Pin	224-Pin	176-Pin
MultiMediaCard interface	MMC_D1 (input/output)	PC4	○	○	○	○	○	○
		PD7	○	○	○	○	○	○
	MMC_D2 (input/output)	P80	○	○	○	○	○	○
		PD2	○	○	○	○	○	○
	MMC_D3 (input/output)	P81	○	○	○	○	○	○
		PD3	○	○	○	○	○	○
	MMC_D4 (input/output)	P82	○	○	○	○	○	○
		PE0	○	○	○	○	○	○
	MMC_D5 (input/output)	PC5	○	○	○	○	○	○
		PE1	○	○	○	○	○	○
	MMC_D6 (input/output)	PC6	○	○	○	○	○	○
		PE2	○	○	○	○	○	○
	MMC_D7 (input/output)	PC7	○	○	○	○	○	○
		PE3	○	○	○	○	○	○
Delta-sigma modulator interface	DSMCLK0 (input/output)	P33	○	○				
	DSMDAT0 (input)	P34	○	○				
	DSMCLK1 (input/output)	P83	○	○				
	DSMDAT1 (input)	P56	○	○				
	DSMCLK2 (input/output)	P74	○	○				
	DSMDAT2 (input)	P75	○	○				
	DSMCLK3 (input/output)	P71	○	○				
	DSMDAT3 (input)	P72	○	○				
	DSMCLK4 (input/output)	P92	○	○				
	DSMDAT4 (input)	P93	○	○				
	DSMCLK5 (input/output)	P90	○	○				
	DSMDAT5 (input)	P91	○	○				
12-bit A/D converter	AN000 (input)*1	P40	○	○	○	○	○	○
	AN001 (input)*1	P41	○	○	○	○	○	○
	AN002 (input)*1	P42	○	○	○	○	○	○
	AN003 (input)*1	P43	○	○	○	○	○	○
	AN004 (input)*1	P44	○	○	○	○	○	○
	AN005 (input)*1	P45	○	○	○	○	○	○
	AN006 (input)*1	P46	○	○	○	○	○	○
	AN007 (input)*1	P47	○	○	○	○	○	○
	ADTRG0# (input)	P07	○	○	○	○	○	○
		P16	○	○	○	○	○	○
		P25	○	○	○	○	○	○
	AN100 (input)*1	PE2	○	○	○	○	○	○
	AN101 (input)*1	PE3	○	○	○	○	○	○
	AN102 (input)*1	PE4	○	○	○	○	○	○
	AN103 (input)*1	PE5	○	○	○	○	○	○
	AN104 (input)*1	PE6	○	○	○	○	○	○
	AN105 (input)*1	PE7	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			224-Pin	176-Pin	224-Pin	176-Pin	224-Pin	176-Pin
12-bit A/D converter	AN106 (input)*1	PD6	○	○	○	○	○	○
	AN107 (input)*1	PD7	○	○	○	○	○	○
	AN108 (input)*1	PD0	○	○	○	○	○	○
	AN109 (input)*1	PD1	○	○	○	○	○	○
	AN110 (input)*1	PD2	○	○	○	○	○	○
	AN111 (input)*1	PD3	○	○	○	○	○	○
	AN112 (input)*1	PD4	○	○	○	○	○	○
	AN113 (input)*1	PD5	○	○	○	○	○	○
	AN114 (input)*1	P90	○	○	○	○	○	○
	AN115 (input)*1	P91	○	○	○	○	○	○
	AN116 (input)*1	P92	○	○	○	○	○	○
	AN117 (input)*1	P93	○	○	○	○	○	○
	AN118 (input)*1	P00	○	○	○	○	○	○
	AN119 (input)*1	P01	○	○	○	○	○	○
	AN120 (input)*1	P02	○	○	○	○	○	○
	ANEX0 (output)*1	PE0	○	○	○	○	○	○
	ANEX1 (input)*1	PE1	○	○	○	○	○	○
	ADTRG1# (input)	P13	○	○	○	○	○	○
		P17	○	○	○	○	○	○
12-bit D/A converter	DA0 (output)*1	P03	○	○	○	○	○	○
	DA1 (output)*1	P05	○	○	○	○	○	○
Parallel data capture unit	PIXCLK (input)	P24	○	○	○	○	○	○
	VSYNC (input)	P32	○	○	○	○	○	○
	HSYNC (input)	P25	○	○	○	○	○	○
	PIXD0 (input)	P15	○	○	○	○	○	○
	PIXD1 (input)	P86	○	○	○	○	○	○
	PIXD2 (input)	P87	○	○	○	○	○	○
	PIXD3 (input)	P17	○	○	○	○	○	○
	PIXD4 (input)	P20	○	○	○	○	○	○
	PIXD5 (input)	P21	○	○	○	○	○	○
	PIXD6 (input)	P22	○	○	○	○	○	○
	PIXD7 (input)	P23	○	○	○	○	○	○
	PCKO (output)	P33	○	○	○	○	○	○
Clock generation circuit	CLKOUT (output)	P25	○	○	○	○	○	○
		PH6	○	×	○	×	○	×
	CLKOUT25M (output)	P56	○	○	○	○	○	○
		PH7	○	×	○	×	○	×
		PJ2	○	○	○	○	○	○
Clock frequency accuracy measurement circuit	CACREF (input)	PA0	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
Graphic LCD controller	LCD_EXTCLK (input)	P73	○	○	○	○	○	○
		PD0	○	○	○	○	○	○
	LCD_CLK (output)	P14	○	○	○	○	○	○
		PB5	○	○	○	○	○	○
	LCD_TCON0 (output)	P13	○	○	○	○	○	○
		PB4	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			224-Pin	176-Pin	224-Pin	176-Pin	224-Pin	176-Pin
Graphic LCD controller	LCD_TCON1 (output)	PB3	○	○	○	○	○	○
		P12	○	○	○	○	○	○
	LCD_TCON2 (output)	PB2	○	○	○	○	○	○
		PJ2	○	○	○	○	○	○
	LCD_TCON3 (output)	PB1	○	○	○	○	○	○
		PJ1	○	○	○	○	○	○
	LCD_DATA0 (output)	PB0	○	○	○	○	○	○
		PJ0	○	○	○	○	○	○
	LCD_DATA1 (output)	P85	○	○	○	○	○	○
		PA7	○	○	○	○	○	○
	LCD_DATA2 (output)	P84	○	○	○	○	○	○
		PA6	○	○	○	○	○	○
	LCD_DATA3 (output)	P57	○	○	○	○	○	○
		PA5	○	○	○	○	○	○
	LCD_DATA4 (output)	P56	○	○	○	○	○	○
		PA4	○	○	○	○	○	○
	LCD_DATA5 (output)	P55	○	○	○	○	○	○
		PA3	○	○	○	○	○	○
	LCD_DATA6 (output)	P54	○	○	○	○	○	○
		PA2	○	○	○	○	○	○
	LCD_DATA7 (output)	P11	○	○	○	○	○	○
		PA1	○	○	○	○	○	○
	LCD_DATA8 (output)	P83	○	○	○	○	○	○
		PA0	○	○	○	○	○	○
	LCD_DATA9 (output)	PC7	○	○	○	○	○	○
		PE7	○	○	○	○	○	○
	LCD_DATA10 (output)	PC6	○	○	○	○	○	○
		PE6	○	○	○	○	○	○
	LCD_DATA11 (output)	PC5	○	○	○	○	○	○
		PE5	○	○	○	○	○	○
	LCD_DATA12 (output)	P82	○	○	○	○	○	○
		PE4	○	○	○	○	○	○
	LCD_DATA13 (output)	P81	○	○	○	○	○	○
		PE3	○	○	○	○	○	○
	LCD_DATA14 (output)	P80	○	○	○	○	○	○
		PE2	○	○	○	○	○	○
	LCD_DATA15 (output)	PC4	○	○	○	○	○	○
		PE1	○	○	○	○	○	○
	LCD_DATA16 (output)	PC3	○	○	○	○	○	○
		PE0	○	○	○	○	○	○
	LCD_DATA17 (output)	P77	○	○	○	○	○	○
		PD7	○	○	○	○	○	○
	LCD_DATA18 (output)	P76	○	○	○	○	○	○
		PD6	○	○	○	○	○	○
	LCD_DATA19 (output)	PC2	○	○	○	○	○	○
		PD5	○	○	○	○	○	○
	LCD_DATA20 (output)	P75	○	○	○	○	○	○
		PD4	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			224-Pin	176-Pin	224-Pin	176-Pin	224-Pin	176-Pin
Graphic LCD controller	LCD_DATA21 (output)	P74	○	○	○	○	○	○
		PD3	○	○	○	○	○	○
	LCD_DATA22 (output)	PC1	○	○	○	○	○	○
		PD2	○	○	○	○	○	○
	LCD_DATA23 (output)	P72	○	○	○	○	○	○
		PD1	○	○	○	○	○	○

Note: 1. For these pin functions, ensure that the corresponding pin is set as general input (PORTm.PDR.Bn and PORTm.PMR.Bn bits cleared to 0).

Table 2.14 Comparison of Multiplexed Pin Assignments (145-Pin/144-Pin/100-Pin)

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			144-Pin	100-Pin	145-/144-Pin	100-Pin	145-/144-Pin	100-Pin
Interrupt	NMI (input)	P35	○	○	○	○	○	○
EXDMA controller	EDREQ0 (input)	P22	○	×	○	○	○	○
		P55	○	×	○	○	○	○
		P80	○	×	○	×	○	×
	EDACK0 (output)	P54	○	×	○	○	○	○
		P23	○	×	○	○	○	○
		P81	○	×	○	×	○	×
	EDREQ1 (input)	P24	○	×	○	○	○	○
		P33	○	×	○	○	○	○
		P82	○	×	○	×	○	×
	EDACK1 (output)	P25	○	×	○	○	○	○
		P56	○	×	○	×	○	×
		P83	○	×	○	×	○	×
		PJ3	○	×	○	○	○	○
Interrupt	IRQ0-DS (input)	P30	○	○	○	○	○	○
	IRQ0 (input)	PD0	○	×	○	○	○	○
	IRQ1-DS (input)	P31	○	○	○	○	○	○
	IRQ1 (input)	PD1	○	○	○	○	○	○
	IRQ2-DS (input)	P32	○	○	○	○	○	○
	IRQ2 (input)	P12	○	×	○	○	○	○
		PD2	○	○	○	○	○	○
	IRQ3-DS (input)	P33	○	○	○	○	○	○
	IRQ3 (input)	P13	○	×	○	○	○	○
		PD3	○	×	○	○	○	○
	IRQ4-DS (input)	PB1	○	○	○	○	○	○
	IRQ4 (input)	P14	○	○	○	○	○	○
		P34	○	○	○	○	○	○
		PD4	○	×	○	○	○	○
		PF5	×	×	○	×	○	×
	IRQ5-DS (input)	PA4	○	○	○	○	○	○
	IRQ5 (input)	P15	○	○	○	○	○	○
		PD5	○	×	○	○	○	○
		PE5	○	○	○	○	○	○
	IRQ6-DS (input)	PA3	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			144-Pin	100-Pin	145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
Interrupt	IRQ6 (input)	P16	○	○	○	○	○	○
		PD6	○	○	○	○	○	○
		PE6	○	×	○	○	○	○
	IRQ7-DS (input)	PE2	○	×	○	○	○	○
	IRQ7 (input)	P17	○	○	○	○	○	○
		PD7	○	○	○	○	○	○
		PE7	○	×	○	○	○	○
	IRQ8-DS (input)	P40	○	○	○	○	○	○
	IRQ8 (input)	P00	○	○	○	×	○	×
		P20	○	○	○	○	○	○
	IRQ9-DS (input)	P41	○	○	○	○	○	○
	IRQ9 (input)	P01	○	×	○	×	○	×
		P21	○	○	○	○	○	○
	IRQ10-DS (input)	P42	○	○	○	○	○	○
	IRQ10 (input)	P02	○	×	○	×	○	×
		P55	○	×	○	○	○	○
	IRQ11-DS (input)	P43	○	×	○	○	○	○
	IRQ11 (input)	P03	○	×	○	×	○	×
		PA1	○	○	○	○	○	○
	IRQ12-DS (input)	P44	○	×	○	○	○	○
	IRQ12 (input)	PB0	○	○	○	○	○	○
		PC1	○	×	○	○	○	○
	IRQ13-DS (input)	P45	×	×	○	○	○	○
	IRQ13 (input)	P05	○	×	○	○	○	○
		PC6	○	○	○	○	○	○
	IRQ14-DS (input)	P46	×	×	○	○	○	○
	IRQ14 (input)	PC0	○	×	○	○	○	○
		PC7	○	○	○	○	○	○
	IRQ15-DS (input)	P47	×	×	○	○	○	○
	IRQ15 (input)	P07	×	×	○	○	○	○
		P67	○	○	○	×	○	×
Multi-function timer pulse unit 3	MTIOC0A (input/output)	P34	○	○	○	○	○	○
		PB3	○	○	○	○	○	○
	MTIOC0B (input/output)	P13	○	×	○	○	○	○
		P15	○	○	○	○	○	○
		PA1	○	○	○	○	○	○
	MTIOC0C (input/output)	P32	○	○	○	○	○	○
		PB1	○	○	○	○	○	○
	MTIOC0D (input/output)	P33	○	○	○	○	○	○
		PA3	○	○	○	○	○	○
	MTIOC1A (input/output)	P20	○	○	○	○	○	○
		PE4	○	○	○	○	○	○
	MTIOC1B (input/output)	P21	○	○	○	○	○	○
		PB5	○	○	○	○	○	○
	MTIOC2A (input/output)	P26	○	○	○	○	○	○
		PB5	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			144-Pin	100-Pin	145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
Multi-function timer pulse unit 3	MTIOC2B (input/output)	P27	○	○	○	○	○	○
		PE5	○	○	○	○	○	○
	MTIOC3A (input/output)	P14	○	○	○	○	○	○
		P17	○	○	○	○	○	○
		PC1	○	×	○	○	○	○
		PC7	○	○	○	○	○	○
	MTIOC3B (input/output)	P17	○	○	○	○	○	○
		P22	○	×	○	○	○	○
		P80	○	○	○	×	○	×
		PB7	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
		PE1	○	×	○	○	○	○
	MTIOC3C (input/output)	P16	○	○	○	○	○	○
		P56	○	○	○	×	○	×
		PC0	○	×	○	○	○	○
		PC6	○	○	○	○	○	○
		PJ3	○	×	○	○	○	○
	MTIOC3D (input/output)	P16	○	○	○	○	○	○
		P23	○	○	○	○	○	○
		P81	○	○	○	×	○	×
		PB6	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
		PE0	○	×	○	○	○	○
	MTIOC4A (input/output)	P21	○	○	○	○	○	○
		P24	○	○	○	○	○	○
		P82	○	○	○	×	○	×
		PA0	○	○	○	○	○	○
		PB3	○	○	○	○	○	○
		PE2	○	×	○	○	○	○
	MTIOC4B (input/output)	P17	○	○	○	○	○	○
		P30	○	○	○	○	○	○
		P54	○	×	○	○	○	○
		PC2	○	○	○	○	○	○
		PD1	○	○	○	○	○	○
		PE3	○	○	○	○	○	○
	MTIOC4C (input/output)	P25	○	○	○	○	○	○
		P83	○	×	○	×	○	×
		P87	○	○	○	×	○	×
		PB1	○	○	○	○	○	○
		PE1	○	×	○	○	○	○
		PE5	○	○	○	○	○	○
	MTIOC4D (input/output)	P31	○	○	○	○	○	○
		P55	○	×	○	○	○	○
		P86	○	○	○	×	○	×
		PC3	○	×	○	○	○	○
		PD2	○	○	○	○	○	○
		PE4	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			144-Pin	100-Pin	145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
Multi-function timer pulse unit 3	MTIC5U (input)	PA4	○	○	○	○	○	○
		PD7	○	○	○	○	○	○
	MTIC5V (input)	PA6	○	○	○	○	○	○
		PD6	○	○	○	○	○	○
	MTIC5W (input)	PB0	○	○	○	○	○	○
		PD5	○	×	○	○	○	○
	MTIOC6A (input/output)	PE7	○	×	○	○	○	○
	MTIOC6B (input/output)	PA5	○	×	○	○	○	○
	MTIOC6C (input/output)	PE6	○	×	○	○	○	○
	MTIOC6D (input/output)	PA0	○	○	○	○	○	○
	MTIOC7A (input/output)	PA2	○	○	○	○	○	○
	MTIOC7B (input/output)	PA1	○	○	○	○	○	○
	MTIOC7C (input/output)	P67	○	○	○	×	○	×
	MTIOC7D (input/output)	P66	○	○	○	×	○	×
	MTIOC8A (input/output)	PD6	○	○	○	○	○	○
	MTIOC8B (input/output)	PD4	○	×	○	○	○	○
	MTIOC8C (input/output)	PD5	○	×	○	○	○	○
	MTIOC8D (input/output)	PD3	○	×	○	○	○	○
	MTCLKA (input)	P14	○	○	○	○	○	○
		P24	○	○	○	○	○	○
		PA4	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
		PD5	○	×	○	○	○	○
	MTCLKB (input)	P15	○	○	○	○	○	○
		P25	○	○	○	○	○	○
		PA6	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	MTCLKC (input)	P22	○	×	○	○	○	○
		PA1	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	MTCLKD (input)	P23	○	○	○	○	○	○
		PA3	○	○	○	○	○	○
		PC5	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			144-Pin	100-Pin	145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
Port output enable 3	POE0# (input)	P32	○	○	○	○	○	○
		P93	○	○	○	×	○	×
		PC4	○	○	○	○	○	○
		PD1	○	○	○	○	○	○
		PD7	○	○	○	○	○	○
	POE4# (input)	P33	○	○	○	○	○	○
		P92	○	○	○	×	○	×
		PB5	○	○	○	○	○	○
		PD0	○	×	○	○	○	○
		PD6	○	○	○	○	○	○
	POE8# (input)	P17	○	○	○	○	○	○
		P30	○	○	○	○	○	○
		PD3	○	×	○	○	○	○
		PE3	○	○	○	○	○	○
		PJ5	×	×	○	×	○	×
	POE10# (input)	P32	○	○	○	○	○	○
		P34	○	○	○	○	○	○
		PA6	○	○	○	○	○	○
		PD5	○	×	○	○	○	○
	POE11# (input)	P33	○	○	○	○	○	○
		PB3	○	○	○	○	○	○
		PD4	○	×	○	○	○	○
General PWM timer W	GTADSM0 (output)	P12	○	×	○	○	○	○
	GTADSM1 (output)	P13	○	×	○	○	○	○
	GTETRGA (input)	P15	○	○	○	○	○	○
	GTETRGB (input)	PA6	○	○	○	○	○	○
	GTETRGC (input)	PC4	○	○	○	○	○	○
	GTETRGD (input)	P14	○	○	○	○	○	○
	GTIOC0A (input/output)	P23	○	○	○	○	○	○
		P83	○	×	○	×	○	×
		PA5	○	×	○	○	○	○
		PD3	○	×	○	○	○	○
		PE5	○	○	○	○	○	○
	GTIOC0B (input/output)	P17	○	○	○	○	○	○
		P81	○	○	○	×	○	×
		PA0	○	○	○	○	○	○
		PD2	○	○	○	○	○	○
		PE2	○	×	○	○	○	○
	GTIOC1A (input/output)	P22	○	×	○	○	○	○
		PA2	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
		PD1	○	○	○	○	○	○
		PE4	○	○	○	○	○	○
	GTIOC1B (input/output)	P67	○	○	○	×	○	×
		P87	○	○	○	×	○	×
		PC3	○	×	○	○	○	○
		PD0	○	×	○	○	○	○
		PE1	○	×	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			144-Pin	100-Pin	145-/144-Pin	100-Pin	145-/144-Pin	100-Pin
General PWM timer W	GTIOC2A (input/output)	P21	○	○	○	○	○	○
		P82	○	○	○	×	○	×
		PA1	○	○	○	○	○	○
		PE3	○	○	○	○	○	○
	GTIOC2B (input/output)	P66	○	○	○	×	○	×
		P86	○	○	○	×	○	×
		PC2	○	○	○	○	○	○
		PE0	○	×	○	○	○	○
	GTIOC3A (input/output)	PC7	○	○	○	○	○	○
		PE7	○	×	○	○	○	○
	GTIOC3B (input/output)	PC6	○	○	○	○	○	○
		PE6	○	×	○	○	○	○
16-bit timer pulse unit	TIOCA0 (input/output)	P86	○	○	○	×	○	×
		PA0	○	○	○	○	○	○
	TIOCB0 (input/output)	P17	○	○	○	○	○	○
		PA1	○	○	○	○	○	○
	TIOCC0 (input/output)	P32	○	○	○	○	○	○
	TIOCD0 (input/output)	P33	○	○	○	○	○	○
		PA3	○	○	○	○	○	○
	TIOCA1 (input/output)	P56	○	○	○	×	○	×
		PA4	○	○	○	○	○	○
	TIOCB1 (input/output)	P16	○	○	○	○	○	○
		PA5	○	×	○	○	○	○
	TIOCA2 (input/output)	P87	○	○	○	×	○	×
		PA6	○	○	○	○	○	○
	TIOCB2 (input/output)	P15	○	○	○	○	○	○
		PA7	○	×	○	○	○	○
	TIOCA3 (input/output)	P21	○	○	○	○	○	○
		PB0	○	○	○	○	○	○
	TIOCB3 (input/output)	P20	○	○	○	○	○	○
		PB1	○	○	○	○	○	○
	TIOCC3 (input/output)	P22	○	×	○	○	○	○
		PB2	○	×	○	○	○	○
	TIOCD3 (input/output)	P23	○	○	○	○	○	○
		PB3	○	○	○	○	○	○
	TIOCA4 (input/output)	P25	○	○	○	○	○	○
		PB4	○	○	○	○	○	○
	TIOCB4 (input/output)	P24	○	○	○	○	○	○
		PB5	○	○	○	○	○	○
	TIOCA5 (input/output)	P13	○	×	○	○	○	○
		PB6	○	○	○	○	○	○
	TIOCB5 (input/output)	P14	○	○	○	○	○	○
		PB7	○	○	○	○	○	○
	TCLKA (input)	P14	○	○	○	○	○	○
		PC2	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			144-Pin	100-Pin	145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
16-bit timer pulse unit	TCLKB (input)	P15	○	○	○	○	○	○
		PA3	○	○	○	○	○	○
		PC3	○	×	○	○	○	○
	TCLKC (input)	P16	○	○	○	○	○	○
		PB2	○	×	○	○	○	○
		PC0	○	×	○	○	○	○
	TCLKD (input)	P17	○	○	○	○	○	○
		PB3	○	○	○	○	○	○
		PC1	○	×	○	○	○	○
Programmable pulse generator	PO0 (output)	P20	○	○	○	○	○	○
	PO1 (output)	P21	○	○	○	○	○	○
	PO2 (output)	P22	○	×	○	○	○	○
	PO3 (output)	P23	○	○	○	○	○	○
	PO4 (output)	P24	○	○	○	○	○	○
	PO5 (output)	P25	○	○	○	○	○	○
	PO6 (output)	P26	○	○	○	○	○	○
	PO7 (output)	P27	○	○	○	○	○	○
	PO8 (output)	P30	○	○	○	○	○	○
	PO9 (output)	P31	○	○	○	○	○	○
	PO10 (output)	P32	○	○	○	○	○	○
	PO11 (output)	P33	○	○	○	○	○	○
	PO12 (output)	P34	○	○	○	○	○	○
	PO13 (output)	P13	○	×	○	○	○	○
		P15	○	○	○	○	○	○
	PO14 (output)	P16	○	○	○	○	○	○
	PO15 (output)	P14	○	○	○	○	○	○
		P17	○	○	○	○	○	○
	PO16 (output)	P73	○	×	○	×	○	×
		PA0	○	○	○	○	○	○
	PO17 (output)	PA1	○	○	○	○	○	○
		PC0	○	×	○	○	○	○
	PO18 (output)	PA2	○	○	○	○	○	○
		PC1	○	×	○	○	○	○
		PE1	○	×	○	○	○	○
	PO19 (output)	P74	○	×	○	×	○	×
		PA3	○	○	○	○	○	○
	PO20 (output)	P75	○	×	○	×	○	×
		PA4	○	○	○	○	○	○
	PO21 (output)	PA5	○	×	○	○	○	○
		PC2	○	○	○	○	○	○
	PO22 (output)	P76	○	×	○	×	○	×
		PA6	○	○	○	○	○	○
	PO23 (output)	P77	○	×	○	×	○	×
		PA7	○	×	○	○	○	○
		PE2	○	×	○	○	○	○
	PO24 (output)	PB0	○	○	○	○	○	○
		PC3	○	×	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			144-Pin	100-Pin	145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
Programmable pulse generator	PO25 (output)	PB1	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	PO26 (output)	P80	○	○	○	×	○	×
		PB2	○	×	○	○	○	○
		PE3	○	○	○	○	○	○
	PO27 (output)	P81	○	○	○	×	○	×
		PB3	○	○	○	○	○	○
	PO28 (output)	P82	○	○	○	×	○	×
		PB4	○	○	○	○	○	○
		PE4	○	○	○	○	○	○
	PO29 (output)	PB5	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
	PO30 (output)	PB6	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	PO31 (output)	PB7	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
8-bit timer	TMO0 (output)	P22	○	×	○	○	○	○
		PB3	○	○	○	○	○	○
	TMCI0 (input)	P01	○	×	○	×	○	×
		P21	○	○	○	○	○	○
		PB1	○	○	○	○	○	○
	TMRI0 (input)	P00	○	○	○	×	○	×
		P20	○	○	○	○	○	○
		PA4	○	○	○	○	○	○
	TMO1 (output)	P17	○	○	○	○	○	○
		P26	○	○	○	○	○	○
	TMCI1 (input)	P02	○	×	○	×	○	×
		P12	○	×	○	○	○	○
		P54	○	×	○	○	○	○
		PC4	○	○	○	○	○	○
	TMRI1 (input)	P24	○	○	○	○	○	○
		PB5	○	○	○	○	○	○
	TMO2 (output)	P16	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	TMCI2 (input)	P15	○	○	○	○	○	○
		P31	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	TMRI2 (input)	P14	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
	TMO3 (output)	P13	○	×	○	○	○	○
		P32	○	○	○	○	○	○
		P55	○	×	○	○	○	○
	TMCI3 (input)	P27	○	○	○	○	○	○
		P34	○	○	○	○	○	○
		PA6	○	○	○	○	○	○
	TMRI3 (input)	P30	○	○	○	○	○	○
		P33	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			144-Pin	100-Pin	145-/144-Pin	100-Pin	145-/144-Pin	100-Pin
Compare match timer W	TOC0 (output)	PC7	○	×	○	○	○	○
	TIC0 (input)	PC6	○	×	○	○	○	○
	TOC1 (output)	PE7	○	×	○	○	○	○
	TIC1 (input)	PE6	○	×	○	○	○	○
	TOC2 (output)	PD3	○	×	○	○	○	○
	TIC2 (input)	PD2	○	×	○	○	○	○
	TOC3 (output)	PE3	○	×	○	○	○	○
	TIC3 (input)	PE2	○	×	○	○	○	○
Realtime clock	RTCOUT (output)	P16	○	○	○	○	○	○
		P32	○	○	○	○	○	○
	RTCIC0 (input)*1	P30	○	○	○	○	○	○
	RTCIC1 (input)*1	P31	○	○	○	○	○	○
	RTCIC2 (input)*1	P32	○	○	○	○	○	○
PTP module for the Ethernet controller	EPLSOUT0 (output)	P17	○	○	○	○		
		PJ5	×	×	○	×		
	EPLSOUT1 (output)	P67	○	○	○	×		
		P87	○	○	○	×		
Ethernet controller	REF50CK0 (input)	P76	○	×	○	×	○	×
		PB2	○	×	○	○	○	○
		PE5	○	○	○	○	○	○
	RMII0_CRS_DV (input)	P83	○	×	○	×	○	×
		PB7	○	○	○	○	○	○
	RMII0_TXD0 (output)	P81	○	○	○	×	○	×
		PB5	○	○	○	○	○	○
	RMII0_TXD1 (output)	P82	○	○	○	×	○	×
		PB6	○	○	○	○	○	○
	RMII0_RXD0 (input)	P75	○	×	○	×	○	×
		PB1	○	○	○	○	○	○
	RMII0_RXD1 (input)	P74	○	×	○	×	○	×
		PB0	○	○	○	○	○	○
	RMII0_TXD_EN (output)	P80	○	○	○	×	○	×
		PA0	○	○	○	○	○	○
		PB4	○	○	○	○	○	○
	RMII0_RX_ER (input)	P77	○	×	○	×	○	×
		PB3	○	○	○	○	○	○
	REF50CK1 (input)	PD6	○	○	○	×		
		PG0	○	×	×	×		
	RMII1_CRS_DV (input)	P92	○	○	○	×		
	RMII1_TXD0 (output)	P64	○	○	○	×		
	RMII1_TXD1 (output)	P63	○	○	○	×		
	RMII1_RXD0 (input)	P62	○	○	○	×		
	RMII1_RXD1 (input)	P61	○	○	○	×		
	RMII1_TXD_EN (output)	P60	○	○	○	×		
	RMII1_RX_ER (input)	PD7	○	○	○	×		
		PG1	○	×	×	×		

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			144-Pin	100-Pin	145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
Ethernet controller	ET0_CRS (input)	P83	○	×	○	×	○	×
		PB7	○	○	○	○	○	○
	ET0_RX_DV (input)	PC2	○	○	○	○	○	○
	ET0_EXOUT (output)	P55	○	×	○	○	○	○
		PA6	○	○	○	○	○	○
		PJ3	○	×	○	○	○	○
	ET0_LINKSTA (input)	P34	○	○	○	○	○	○
		P54	○	×	○	○	○	○
		PA5	○	×	○	○	○	○
	ET0_ETXD0 (output)	P81	○	○	○	×	○	×
		PB5	○	○	○	○	○	○
	ET0_ETXD1 (output)	P82	○	○	○	×	○	×
		PB6	○	○	○	○	○	○
	ET0_ETXD2 (output)	PC5	○	○	○	○	○	○
	ET0_ETXD3 (output)	PC6	○	○	○	○	○	○
	ET0_ERXD0 (input)	P75	○	×	○	×	○	×
		PB1	○	○	○	○	○	○
	ET0_ERXD1 (input)	P74	○	×	○	×	○	×
		PB0	○	○	○	○	○	○
	ET0_ERXD2 (input)	PC1	○	×	○	○	○	○
		PE4	○	○	○	○	○	○
	ET0_ERXD3 (input)	PC0	○	×	○	○	○	○
		PE3	○	○	○	○	○	○
	ET0_TX_EN (output)	P80	○	○	○	×	○	×
		PA0	○	○	○	○	○	○
		PB4	○	○	○	○	○	○
	ET0_TX_ER (output)	PC3	○	×	○	○	○	○
	ET0_RX_ER (input)	P77	○	×	○	×	○	×
		PB3	○	○	○	○	○	○
	ET0_TX_CLK (input)	PC4	○	○	○	○	○	○
	ET0_RX_CLK (input)	P76	○	×	○	×	○	×
		PB2	○	×	○	○	○	○
		PE5	○	○	○	○	○	○
	ET0_COL (input)	PC7	○	○	○	○	○	○
	ET0_WOL (output)	P73	○	×	○	×	○	×
		PA1	○	○	○	○	○	○
		PA7	○	×	○	○	○	○
	ET0_MDC (output)	P72	×	×	○	×	○	×
		PA4	○	○	○	○	○	○
	ET0_MDIO (input/output)	P71	×	×	○	×	○	×
		PA3	○	○	○	○	○	○
	ET1_CRS (input)	P92	○	○	×	×		
	ET1_RX_DV (input)	P90	○	○	×	×		
	ET1_EXOUT (output)	P26	○	○	○	×		
		PD2	○	○	○	×		
	ET1_LINKSTA (input)	P93	○	○	○	×		
	ET1_ETXD0 (output)	P64	○	○	×	×		
	ET1_ETXD1 (output)	P63	○	○	×	×		

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			144-Pin	100-Pin	145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
Ethernet controller	ET1_ETXD2 (output)	PG5	○	○	×	×		
	ET1_ETXD3 (output)	PG6	○	○	×	×		
	ET1_ERXD0 (input)	P62	○	○	×	×		
	ET1_ERXD1 (input)	P61	○	○	×	×		
	ET1_ERXD2 (input)	P96	○	○	×	×		
	ET1_ERXD3 (input)	P97	○	○	×	×		
	ET1_TX_EN (output)	P60	○	○	×	×		
	ET1_TX_ER (output)	PG7	○	×	×	×		
	ET1_RX_ER (input)	PD7	○	○	×	×		
		PG1	○	×	×	×		
	ET1_TX_CLK (input)	PG2	○	○	×	×		
	ET1_RX_CLK (input)	PD6	○	○	×	×		
		PG0	○	×	×	×		
	ET1_COL (input)	P91	○	○	×	×		
	ET1_WOL (output)	P27	○	○	○	×		
		PD3	○	×	○	×		
	ET1_MDC (output)	P31	○	○	○	×		
		PD5	○	×	○	×		
	ET1_MDIO (input/output)	P30	○	○	○	×		
		PD4	○	×	○	×		
Ethernet PHY management interface	PMGI0_MDC (output)	P72	×	×	○	×	○	×
		PA4	○	○	○	○	○	○
	PMGI0_MDIO (input/output)	P71	×	×	○	×	○	×
		PA3	○	○	○	○	○	○
	PMGI1_MDC (output)	P31	○	○	○	×		
		PD5	○	×	○	×		
	PMGI1_MDIO (input/output)	P30	○	○	○	×		
		PD4	○	×	○	×		
EtherCAT slave controller	CAT0_LINKSTA (input)	P34	○	○				
		P54	○	×				
		PA5	○	×				
	CAT0_RX_CLK (input)	P76	○	×				
		PB2	○	×				
		PE5	○	○				
	CAT0_RX_DV (input)	P83	○	×				
		PB7	○	○				
		PC2	○	○				
	CAT0_ERXD0 (input)	P75	○	×				
		PB1	○	○				
	CAT0_ERXD1 (input)	P74	○	×				
		PB0	○	○				
	CAT0_ERXD2 (input)	PC1	○	×				
		PE4	○	○				
	CAT0_ERXD3 (input)	PC0	○	×				
		PE3	○	○				
	CAT0_RX_ER (input)	P77	○	×				
		PB3	○	○				

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			144-Pin	100-Pin	145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
EtherCAT slave controller	CAT0_TX_CLK (input)	PC4	○	○				
	CAT0_TX_EN (output)	P80	○	○				
		PA0	○	○				
		PB4	○	○				
	CAT0_ETXD0 (output)	P81	○	○				
		PB5	○	○				
	CAT0_ETXD1 (output)	P82	○	○				
		PB6	○	○				
	CAT0_ETXD2 (output)	PC5	○	○				
	CAT0_ETXD3 (output)	PC6	○	○				
	CAT0_MDC (output)	PA4	○	○				
	CAT0_MDIO (input/output)	PA3	○	○				
	CAT1_LINKSTA (input)	P93	○	○				
	CAT1_RX_CLK (input)	PD6	○	○				
		PG0	○	×				
	CAT1_RX_DV (input)	P90	○	○				
		P92	○	○				
	CAT1_ERXD0 (input)	P62	○	○				
	CAT1_ERXD1 (input)	P61	○	○				
	CAT1_ERXD2 (input)	P96	○	○				
	CAT1_ERXD3 (input)	P97	○	○				
	CAT1_RX_ER (input)	PD7	○	○				
		PG1	○	×				
	CAT1_TX_CLK (input)	PG2	○	○				
	CAT1_TX_EN (output)	P60	○	○				
	CAT1_ETXD0 (output)	P64	○	○				
	CAT1_ETXD1 (output)	P63	○	○				
	CAT1_ETXD2 (output)	PG5	○	○				
	CAT1_ETXD3 (output)	PG6	○	○				
	CATRESTOUT (output)	PA6	○	○				
		PJ3	○	×				
	CATLEDRUN (output)	P15	○	○				
		PA0	○	○				
	CATIRQ (output)	P27	○	○				
		PA4	○	○				
	CATLEDSTER (output)	P02	○	×				
		P52	○	○				
	CATLEDERR (output)	P01	○	×				
		P50	○	○				
	CATLINKACT0 (output)	P86	○	○				
	CATLINKACT1 (output)	P26	○	○				
		PA2	○	○				
	CATSYNC0 (output)	P17	○	○				
		PC4	○	○				

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			144-Pin	100-Pin	145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
EtherCAT slave controller	CATSYNC1 (output)	P67	○	○				
		P87	○	○				
	CATLATCH0 (input)	P80	○	○				
	CATLATCH1 (input)	P00	○	○				
		PC6	○	○				
	CATI2CCLK (output)	P81	○	○				
	CATI2CDATA (input/output)	P82	○	○				
Serial communications interface	CTS0# (input)/ RTS0# (output)/ SS0# (input)	P23	○	○	○	○	○	○
		PJ3	○	×	○	○	○	○
	RXD0 (input)/ SMISO0 (input/output)/ SSCL0 (input/output)	P21	○	○	○	○	○	○
		P33	○	○	○	○	○	○
	SCK0 (input/output)	P22	○	×	○	○	○	○
		P34	○	○	○	○	○	○
	SMOSI0 (input/output)/ SSDA0 (input/output)/ TXD0 (output)	P20	○	○	○	○	○	○
		P32	○	○	○	○	○	○
	CTS1# (input)/ RTS1# (output)/ SS1# (input)	P14	○	○	○	○	○	○
		P31	○	○	○	○	○	○
	RXD1 (input)/ SMISO1 (input/output)/ SSCL1 (input/output)	P15	○	○	○	○	○	○
		P30	○	○	○	○	○	○
	SCK1 (input/output)	P17	○	○	○	○	○	○
		P27	○	○	○	○	○	○
	SMOSI1 (input/output)/ SSDA1 (input/output)/ TXD1 (output)	P16	○	○	○	○	○	○
		P26	○	○	○	○	○	○
	CTS2# (input)/ RTS2# (output)/ SS2# (input)	P54	○	×	○	○	○	○
		PJ5	×	×	○	×	○	×
	RXD2 (input)/ SMISO2 (input/output)/ SSCL2 (input/output)	P12	○	×	○	○	○	○
		P52	○	○	○	○	○	○
	SCK2 (input/output)	P51	○	○	○	○	○	○
	SMOSI2 (input/output)/ SSDA2 (input/output)/ TXD2 (output)	P13	○	×	○	○	○	○
		P50	○	○	○	○	○	○
	CTS3# (input)/ RTS3# (output)/ SS3# (input)	P26	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			144-Pin	100-Pin	145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
Serial communications interface	RXD3 (input)/ SMISO3 (input/output)/ SSCL3 (input/output)	P16	○	○	○	○	○	○
		P25	○	○	○	○	○	○
	SCK3 (input/output)	P15	○	○	○	○	○	○
		P24	○	○	○	○	○	○
	SMOSI3 (input/output)/ SSDA3 (input/output)/ TXD3 (output)	P17	○	○	○	○	○	○
		P23	○	○	○	○	○	○
	CTS4# (input)/ RTS4# (output)/ SS4# (input)	PB2	○	×	○	×	○	×
	RXD4 (input)/ SMISO4 (input/output)/ SSCL4 (input/output)	PB0	○	○	○	×	○	×
	SCK4 (input/output)	PB3	○	○	○	×	○	×
	SMOSI4 (input/output)/ SSDA4 (input/output)/ TXD4 (output)	PB1	○	○	○	×	○	×
	CTS5# (input)/ RTS5# (output)/ SS5# (input)	PA6	○	○	○	○	○	○
		PC0	○	×	○	○	○	○
	RXD5 (input)/ SMISO5 (input/output)/ SSCL5 (input/output)	PA2	○	○	○	○	○	○
		PA3	○	○	○	○	○	○
		PC2	○	○	○	○	○	○
	SCK5 (input/output)	PA1	○	○	○	○	○	○
		PC1	○	×	○	○	○	○
		PC4	○	○	○	○	○	○
	SMOSI5 (input/output)/ SSDA5 (input/output)/ TXD5 (output)	PA4	○	○	○	○	○	○
		PC3	○	×	○	○	○	○
	CTS6# (input)/ RTS6# (output)/ SS6# (input)	PB2	○	×	○	○	○	○
		PJ3	○	×	○	○	○	○
	RXD6 (input)/ SMISO6 (input/output)/ SSCL6 (input/output)	P01	○	×	○	×	○	×
		P33	○	○	○	○	○	○
		PB0	○	○	○	○	○	○
	SCK6 (input/output)	P02	○	×	○	×	○	×
		P34	○	○	○	○	○	○
		PB3	○	○	○	○	○	○
	SMOSI6 (input/output)/ SSDA6 (input/output)/ TXD6 (output)	P00	○	○	○	×	○	×
		P32	○	○	○	○	○	○
		PB1	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			144-Pin	100-Pin	145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
Serial communications interface	CTS7# (input)/ RTS7# (output)/ SS7# (input)	P93	○	○	○	×	○	×
	RXD7 (input)/ SMISO7 (input/output)/ SSCL7 (input/output)	P92	○	○	○	×	○	×
	SCK7 (input/output)	P56	○	○	○	×	○	×
		P91	○	○	○	×	○	×
	SMOSI7 (input/output)/ SSDA7 (input/output)/ TXD7 (output)	P55	○	×	○	×	○	×
		P90	○	○	○	×	○	×
	CTS8# (input)/SS8# (input)	PC4	○	○	○	○	○	○
	RTS8# (output)/ SCK8 (input/output)	PC5	○	○	○	○	○	○
	RXD8 (input)/ SMISO8 (input/output)/ SSCL8 (input/output)	PC6	○	○	○	○	○	○
	SMOSI8 (input/output)/ SSDA8 (input/output)/ TXD8 (output)	PC7	○	○	○	○	○	○
		PJ2	○	×	×	×	×	×
	CTS9# (input)/SS9# (input)	PB4	○	○	○	○	○	○
	RTS9# (output)/ SCK9 (input/output)	PB5	○	○	○	○	○	○
	RXD9 (input)/ SMISO9 (input/output)/ SSCL9 (input/output)	PB6	○	○	○	○	○	○
	SMOSI9 (input/output)/ SSDA9 (input/output)/ TXD9 (output)	PB7	○	○	○	○	○	○
	CTS10# (input)/ RTS10# (output)/ SS10# (input)	PC4	○	○	○	○	○	○
	CTS10# (input)/ SCK10 (input/output)/ SS10# (input)	P83	○	×	○	×	○	×
	RTS10# (output)/ SCK10 (input/output)	P80	○	○	○	×	○	×
	RXD10 (input)/ SMISO10 (input/output)/ SSCL10 (input/output)	P81	○	○	○	×	○	×
		P86	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	SCK10 (input/output)	PC5	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			144-Pin	100-Pin	145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
Serial communications interface	SMOSI10 (input/output)/ SSDA10 (input/output)/ TXD10 (output)	P82	○	○	○	×	○	×
		P87	○	○	○	×	○	×
		PC7	○	○	○	○	○	○
	CTS11# (input)/ RTS11# (output)/ SS11# (input)	PB4	○	○	○	○	○	○
	CTS11# (input)/ SS11# (input)	P74	○	×	○	×	○	×
	RTS11# (output)/ SCK11 (input/output)	P75	○	×	○	×	○	×
	RXD11 (input)/ SMISO11 (input/output)/ SSCL11 (input/output)	P76	○	×	○	×	○	×
		PB6	○	○	○	○	○	○
	SCK11 (input/output)	PB5	○	○	○	○	○	○
	SMOSI11 (input/output)/ SSDA11 (input/output)/ TXD11 (output)	P77	○	×	○	×	○	×
		PB7	○	○	○	○	○	○
	CTS12# (input)/ RTS12# (output)/ SS12# (input)	PE3	○	×	○	○	○	○
	RXD12 (input)/ RXDX12 (input)/ SMISO12 (input/output)/ SSCL12 (input/output)	PE2	○	×	○	○	○	○
	SCK12 (input/output)	PE0	○	×	○	○	○	○
	SMOSI12 (input/output)/ SSDA12 (input/output)/ TXD12 (output)/ TXDX12 (output)/ SIOX12 (input/output)	PE1	○	×	○	○	○	○
I^2C bus interface	SCL0[FM+] (input/output)	P12	○	×	○	○	○	○
	SDA0[FM+] (input/output)	P13	○	×	○	○	○	○
	SCL1 (input/output)	P21	○	○	○	○	○	○
	SDA1 (input/output)	P20	○	○	○	○	○	○
	SCL2-DS (input/output)	P16	○	○	○	○	○	○
	SDA2-DS (input/output)	P17	○	○	○	○	○	○
USB 2.0 FS Host/Function module	USB0_VBUS (input)	P16	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			144-Pin	100-Pin	145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
USB 2.0 FS Host/Function module	USB0_EXICEN (output)	P21	○	○	○	○	○	○
	USB0_VBUSEN (output)	P16	○	○	○	○	○	○
		P24	○	○	○	○	○	○
		P32	○	○	○	○	○	○
	USB0_OVRCURA (input)/ USB0_OVRCURA-DS (input)	P14	○	○	○	○	○	○
	USB0_OVRCURB (input)	P16	○	○	○	○	○	○
		P22	○	×	○	○	○	○
	USB0_ID (input)	P20	○	○	○	○	○	○
CAN module	CRX0 (input)	P33	○	○	○	○	○	○
		PD2	○	○	○	○	○	○
	CTX0 (output)	P32	○	○	○	○	○	○
		PD1	○	○	○	○	○	○
	CRX1-DS (input)	P15	○	○	○	○	○	○
	CRX1 (input)	P55	○	×	○	○	○	○
	CTX1 (output)	P14	○	○	○	○	○	○
		P23	○	○	○	○	○	○
		P54	○	×	○	○	○	○
	CRX2 (input)	P67	○	○	○	×	○	×
	CTX2 (output)	P66	○	○	○	×	○	×
Serial peripheral interface	RSPCKA (input/output)	PA5	○	×	○	○	○	○
		PC5	○	×	○	○	○	○
	MOSIA (input/output)	PA6	○	×	○	○	○	○
		PC6	○	×	○	○	○	○
	MISOA (input/output)	PA7	○	×	○	○	○	○
		PC7	○	×	○	○	○	○
	SSLA0 (input/output)	PA4	○	×	○	○	○	○
		PC4	○	×	○	○	○	○
	SSLA1 (output)	PA0	○	×	○	○	○	○
		PC0	○	×	○	○	○	○
	SSLA2 (output)	PA1	○	×	○	○	○	○
		PC1	○	×	○	○	○	○
	SSLA3 (output)	PA2	○	×	○	○	○	○
		PC2	○	×	○	○	○	○
	RSPCKB (input/output)	P27	○	○	○	○	○	○
		PE5	○	○	○	○	○	○
	MOSIB (input/output)	P26	○	○	○	○	○	○
		PE6	○	×	○	○	○	○
	MISOB (input/output)	P30	○	○	○	○	○	○
		PE7	○	×	○	○	○	○
	SSLB0 (input/output)	P31	○	○	○	○	○	○
		PE4	○	○	○	○	○	○
	SSLB1 (output)	P50	○	○	○	○	○	○
		PE0	○	×	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			144-Pin	100-Pin	145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
Serial peripheral interface	SSLB2 (output)	P51	○	○	○	○	○	○
		PE1	○	×	○	○	○	○
	SSLB3 (output)	P52	○	○	○	○	○	○
		PE2	○	×	○	○	○	○
	RSPCKC (input/output)	PD3	○	×	○	○	○	○
	MOSIC (input/output)	PD1	○	×	○	○	○	○
	MISOC (input/output)	PD2	○	×	○	○	○	○
	SSLC0 (input/output)	PD4	○	×	○	○	○	○
	SSLC1 (output)	PD5	○	×	○	○	○	○
	SSLC2 (output)	PD6	○	×	○	○	○	○
	SSLC3 (output)	PD7	○	×	○	○	○	○
Quad serial peripheral interface	QSPCLK (output)	P77	○	×	○	×	○	×
		PD5	○	×	○	○	○	○
	QSSL (output)	P76	○	×	○	×	○	×
		PD4	○	×	○	○	○	○
	QMO /QIO0 (input/output)	PC3	○	×	○	×	○	×
		PD6	○	×	○	○	○	○
	QMI /QIO1 (input/output)	PC4	○	×	○	×	○	×
		PD7	○	×	○	○	○	○
	QIO2 (input/output)	P80	○	×	○	×	○	×
		PD2	○	×	○	○	○	○
	QIO3 (input/output)	P81	○	×	○	×	○	×
		PD3	○	×	○	○	○	○
Enhanced serial sound interface	AUDIO_CLK (input)	P00	○	○	○	×	○	×
		P22	○	×	○	○	○	○
	SSIBCK0 (input/output)	P01	○	×	○	×	○	×
		P23	○	○	○	○	○	○
	SSILRCK0 (input/output)	P21	○	○	○	○	○	○
		PF5	×	×	○	×	○	×
	SSIRXD0 (input)	P20	○	○	○	○	○	○
		PJ5	×	×	○	×	○	×
	SSITXD0 (output)	P17	○	○	○	○	○	○
		PJ3	○	×	○	○	○	○
	SSIBCK1 (input/output)	P02	○	×	○	×	○	×
		P24	○	○	○	○	○	○
	SSILRCK1 (input/output)	P05	○	×	○	○	○	○
		P15	○	○	○	○	○	○
	SSIDATA1 (input/output)	P03	○	×	○	×	○	×
		P25	○	○	○	○	○	○
SD host interface	SDHI_CLK (output)	P21	○	×	○	×	○	×
		P77	○	×	○	×	○	×
		PD5	○	×	○	○	○	○
	SDHI_CMD (input/output)	P20	○	×	○	×	○	×
		P76	○	×	○	×	○	×
		PD4	○	×	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			144-Pin	100-Pin	145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
SD host interface	SDHI_CD (input)	P25	○	×	○	×	○	×
		P81	○	×	○	×	○	×
		PE6	○	×	○	○	○	○
	SDHI_WP (input)	P24	○	×	○	×	○	×
		P80	○	×	○	×	○	×
		PE7	○	×	○	○	○	○
	SDHI_D0 (input/output)	P22	○	×	○	×	○	×
		PC3	○	×	○	×	○	×
		PD6	○	×	○	○	○	○
	SDHI_D1 (input/output)	P23	○	×	○	×	○	×
		PC4	○	×	○	×	○	×
		PD7	○	×	○	○	○	○
	SDHI_D2 (input/output)	P75	○	×	○	×	○	×
		P87	○	×	○	×	○	×
		PD2	○	×	○	○	○	○
	SDHI_D3 (input/output)	P17	○	×	○	×	○	×
		PC2	○	×	○	×	○	×
		PD3	○	×	○	○	○	○
MultiMediaCard interface	MMC_RES# (output)	P75	○	×	○	×	○	×
		PE7	○	×	○	○	○	○
	MMC_CLK (output)	P77	○	×	○	×	○	×
		PD5	○	×	○	○	○	○
	MMC_CD (input)	PC2	○	×	○	×	○	×
		PE6	○	×	○	○	○	○
	MMC_CMD (input/output)	P76	○	×	○	×	○	×
		PD4	○	×	○	○	○	○
	MMC_D0 (input/output)	PC3	○	×	○	×	○	×
		PD6	○	×	○	○	○	○
	MMC_D1 (input/output)	PC4	○	×	○	×	○	×
		PD7	○	×	○	○	○	○
	MMC_D2 (input/output)	P80	○	×	○	×	○	×
		PD2	○	×	○	○	○	○
	MMC_D3 (input/output)	P81	○	×	○	×	○	×
		PD3	○	×	○	○	○	○
	MMC_D4 (input/output)	P82	○	×	○	×	○	×
		PE0	○	×	○	○	○	○
	MMC_D5 (input/output)	PC5	○	×	○	×	○	×
		PE1	○	×	○	○	○	○
	MMC_D6 (input/output)	PC6	○	×	○	×	○	×
		PE2	○	×	○	○	○	○
	MMC_D7 (input/output)	PC7	○	×	○	×	○	×
		PE3	○	×	○	○	○	○
Delta-sigma modulator interface	DSMCLK0 (input/output)	P33	○	×				
	DSMDAT0 (input)	P34	○	×				
	DSMCLK1 (input/output)	P83	○	×				
	DSMDAT1 (input)	P56	○	×				

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			144-Pin	100-Pin	145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
Delta-sigma modulator interface	DSMCLK2 (input/output)	P74	○	×				
	DSMDAT2 (input)	P75	○	×				
12-bit A/D converter	AN000 (input)*1	P40	○	○	○	○	○	○
	AN001 (input)*1	P41	○	○	○	○	○	○
	AN002 (input)*1	P42	○	○	○	○	○	○
	AN003 (input)*1	P43	○	×	○	○	○	○
	AN004 (input)*1	P44	○	×	○	○	○	○
	AN005 (input)*1	P45	×	×	○	○	○	○
	AN006 (input)*1	P46	×	×	○	○	○	○
	AN007 (input)*1	P47	×	×	○	○	○	○
	ADTRG0# (input)	P07	×	×	○	○	○	○
		P16	○	○	○	○	○	○
		P25	○	○	○	○	○	○
	AN100 (input)*1	PE2	○	×	○	○	○	○
	AN101 (input)*1	PE3	○	○	○	○	○	○
	AN102 (input)*1	PE4	○	○	○	○	○	○
	AN103 (input)*1	PE5	○	○	○	○	○	○
	AN104 (input)*1	PE6	○	×	○	○	○	○
	AN105 (input)*1	PE7	○	×	○	○	○	○
	AN106 (input)*1	PD6	○	○	○	○	○	○
	AN107 (input)*1	PD7	○	○	○	○	○	○
	AN108 (input)*1	PD0	○	×	○	○	○	○
	AN109 (input)*1	PD1	○	○	○	○	○	○
	AN110 (input)*1	PD2	○	○	○	○	○	○
	AN111 (input)*1	PD3	○	×	○	○	○	○
	AN112 (input)*1	PD4	○	×	○	○	○	○
	AN113 (input)*1	PD5	○	×	○	○	○	○
	AN114 (input)*1	P90	○	○	○	×	○	×
	AN115 (input)*1	P91	○	○	○	×	○	×
	AN116 (input)*1	P92	○	○	○	×	○	×
	AN117 (input)*1	P93	○	○	○	×	○	×
	AN118 (input)*1	P00	○	○	○	×	○	×
	AN119 (input)*1	P01	○	×	○	×	○	×
	AN120 (input)*1	P02	○	×	○	×	○	×
	ANEX0 (output)*1	PE0	○	×	○	○	○	○
	ANEX1 (input)*1	PE1	○	×	○	○	○	○
	ADTRG1# (input)	P13	○	×	○	○	○	○
		P17	○	○	○	○	○	○
12-bit D/A converter	DA0 (output)*1	P03	○	×	○	×	○	○
	DA1 (output)*1	P05	○	×	○	○	○	○
Parallel data capture unit	PIXCLK (input)	P24	○	×	○	×	○	×
	VSYNC (input)	P32	○	×	○	×	○	×
	HSYNC (input)	P25	○	×	○	×	○	×
	PIXD0 (input)	P15	○	×	○	×	○	×
	PIXD1 (input)	P86	○	×	○	×	○	×
	PIXD2 (input)	P87	○	×	○	×	○	×
	PIXD3 (input)	P17	○	×	○	×	○	×

Module/ Function	Pin Function	Port Allocation	RX72M		RX72N		RX66N	
			144-Pin	100-Pin	145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
Parallel data capture unit	PIXD4 (input)	P20	○	×	○	×	○	×
	PIXD5 (input)	P21	○	×	○	×	○	×
	PIXD6 (input)	P22	○	×	○	×	○	×
	PIXD7 (input)	P23	○	×	○	×	○	×
	PCKO (output)	P33	○	×	○	×	○	×
Clock generation circuit	CLKOUT (output)	P25	○	○	○	○	○	○
	CLKOUT25M (output)	P56	○	○	○	×	○	×
		PJ2	○	×	×	×	×	×
Clock frequency accuracy measurement circuit	CACREF (input)	PA0	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
Graphic LCD controller	LCD_EXTCLK (input)	PD0	○	×	○	○	○	○
	LCD_CLK (output)	PB5	○	×	○	○	○	○
	LCD_TCON0 (output)	PB4	○	×	○	○	○	○
	LCD_TCON1 (output)	PB3	○	×	○	○	○	○
	LCD_TCON2 (output)	PB2	○	×	○	○	○	○
	LCD_TCON3 (output)	PB1	○	×	○	○	○	○
	LCD_DATA0 (output)	PB0	○	×	○	○	○	○
	LCD_DATA1 (output)	PA7	○	×	○	○	○	○
	LCD_DATA2 (output)	PA6	○	×	○	○	○	○
	LCD_DATA3 (output)	PA5	○	×	○	○	○	○
	LCD_DATA4 (output)	PA4	○	×	○	○	○	○
	LCD_DATA5 (output)	PA3	○	×	○	○	○	○
	LCD_DATA6 (output)	PA2	○	×	○	○	○	○
	LCD_DATA7 (output)	PA1	○	×	○	○	○	○
	LCD_DATA8 (output)	PA0	○	×	○	○	○	○
	LCD_DATA9 (output)	PE7	○	×	○	○	○	○
	LCD_DATA10 (output)	PE6	○	×	○	○	○	○
	LCD_DATA11 (output)	PE5	○	×	○	○	○	○
	LCD_DATA12 (output)	PE4	○	×	○	○	○	○
	LCD_DATA13 (output)	PE3	○	×	○	○	○	○
	LCD_DATA14 (output)	PE2	○	×	○	○	○	○
	LCD_DATA15 (output)	PE1	○	×	○	○	○	○
	LCD_DATA16 (output)	PE0	○	×	○	○	○	○
	LCD_DATA17 (output)	PD7	○	×	○	○	○	○
	LCD_DATA18 (output)	PD6	○	×	○	○	○	○
	LCD_DATA19 (output)	PD5	○	×	○	○	○	○
	LCD_DATA20 (output)	PD4	○	×	○	○	○	○
	LCD_DATA21 (output)	PD3	○	×	○	○	○	○
	LCD_DATA22 (output)	PD2	○	×	○	○	○	○
	LCD_DATA23 (output)	PD1	○	×	○	○	○	○

Note: 1. For these pin functions, ensure that the corresponding pin is set as general input (PORTm.PDR.Bn and PORTm.PMR.Bn bits cleared to 0).

Table 2.15 Comparison of P0n Pin Function Control Register (P0nPFS)

Register	Bit	RX72M (n = 0 to 3, 5, 7)	RX72N (n = 0 to 3, 5, 7)	RX66N (n = 0 to 3, 5, 7)
P00PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000101b: TMRI0 001010b: TXD6/SMOSI6/ SSDA6 010111b: AUDIO_CLK 011011b: QIO2-C 100111b: CATLATCH1	Pin function select bits 000000b: Hi-Z 000101b: MRI0 001010b: TXD6/SMOSI6/ SSDA6 010111b: AUDIO_CLK 011011b: QIO2-C	Pin function select bits 000000b: Hi-Z 000101b: TMRI0 001010b: TXD6/SMOSI6/ SSDA6 010111b: AUDIO_CLK 011011b: QIO2-C
P01PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000101b: TMCI0 001010b: RXD6/SMISO6/ SSCL6 010111b: SSIBCK0 011011b: QIO3-C 100111b: CATLEDERR	Pin function select bits 000000b: Hi-Z 000101b: TMCI0 001010b: RXD6/SMISO6/ SSCL6 010111b: SSIBCK0 011011b: QIO3-C	Pin function select bits 000000b: Hi-Z 000101b: TMCI0 001010b: RXD6/SMISO6/ SSCL6 010111b: SSIBCK0 011011b: QIO3-C
P02PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000101b: TMCI1 001010b: SCK6 010111b: SSIBCK1 100111b: CATLEDSTER	Pin function select bits 000000b: Hi-Z 000101b: TMCI1 001010b: SCK6 010111b: SSIBCK1	Pin function select bits 000000b: Hi-Z 000101b: TMCI1 001010b: SCK6 010111b: SSIBCK1

Table 2.16 Comparison of P1n Pin Function Control Register (P1nPFS)

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 7)
P11PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000101b: TMCI3 001010b: SCK2 010001b: EPLSOUT1 100101b: LCD_DATA7-A 100111b: CATSYNC1	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000101b: TMCI3 001010b: SCK2 010001b: EPLSOUT1 100101b: LCD_DATA7-A	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000101b: TMCI3 001010b: SCK2 100101b: LCD_DATA7-A
P14PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKA 000011b: TIOCB5 000100b: TCLKA 000101b: TMRI2 000110b: PO15 001011b: CTS1#/RTS1#/SS1# 010000b: CTX1 010010b: USB0_OVRCURA 011110b: GTETRGD 100101b: LCD_CLK-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKA 000011b: TIOCB5 000100b: TCLKA 000101b: TMRI2 000110b: PO15 001011b: CTS1#/RTS1#/SS1# 010000b: CTX1 010010b: USB0_OVRCURA-DS 011110b: GTETRGD 100101b: LCD_CLK-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKA 000011b: TIOCB5 000100b: TCLKA 000101b: TMRI2 000110b: PO15 001011b: CTS1#/RTS1#/SS1# 010000b: CTX1 010010b: USB0_OVRCURA-DS 011110b: GTETRGD 100101b: LCD_CLK-A
P15PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKB 000011b: TIOCB2 000100b: TCLKB 000101b: TMCI2 000110b: PO13 001010b: RXD1/SMISO1/SSCL1 001011b: SCK3 010000b: CRX1-DS 010111b: SSILRCK1 011100b: PIXD0 011110b: GTETRGA 100111b: CATLEDRUN	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKB 000011b: TIOCB2 000100b: TCLKB 000101b: TMCI2 000110b: PO13 001010b: RXD1/SMISO1/SSCL1 001011b: SCK3 010000b: CRX1-DS 010111b: SSILRCK1 011100b: PIXD0 011110b: GTETRGA	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKB 000011b: TIOCB2 000100b: TCLKB 000101b: TMCI2 000110b: PO13 001010b: RXD1/SMISO1/SSCL1 001011b: SCK3 010000b: CRX1-DS 010111b: SSILRCK1 011100b: PIXD0 011110b: GTETRGA

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 7)
P17PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTIOC3B 000011b: TIOCB0 000100b: TCLKD 000101b: TMO1 000110b: PO15 000111b: POE8# 001000b: MTIOC4B 001001b: ADTRG1# 001010b: SCK1 001011b: TXD3/SMOSI3/ SSDA3 001111b: SDA2-DS 010001b: EPLSOUT0 010111b: SSITXD0 011010b: SDHI_D3-C 011100b: PIXD3 011110b: GTIOC0B 100111b: CATSYNC0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTIOC3B 000011b: TIOCB0 000100b: TCLKD 000101b: TMO1 000110b: PO15 000111b: POE8# 001000b: MTIOC4B 001001b: ADTRG1# 001010b: SCK1 001011b: TXD3/SMOSI3/ SSDA3 001111b: SDA2-DS 010001b: EPLSOUT0 010111b: SSITXD0 011010b: SDHI_D3-C 011100b: PIXD3 011110b: GTIOC0B	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTIOC3B 000011b: TIOCB0 000100b: TCLKD 000101b: TMO1 000110b: PO15 000111b: POE8# 001000b: MTIOC4B 001001b: ADTRG1# 001010b: SCK1 001011b: TXD3/SMOSI3/ SSDA3 001111b: SDA2-DS 010111b: SSITXD0 011010b: SDHI_D3-C 011100b: PIXD3 011110b: GTIOC0B

Table 2.17 Comparison of P2n Pin Function Control Register (P2nPFS)

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 7)
P24PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000010b: MTCLKA 000011b: TIOCB4 000101b: TMRI1 000110b: PO4 001010b: SCK3 010011b: USB0_VBUS EN 010111b: SSIBCK1 011000b: EDREQ1 011010b: SDHI_WP 011100b: PIXCLK	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000010b: MTCLKA 000011b: TIOCB4 000101b: TMRI1 000110b: PO4 001010b: SCK3 010011b: USB0_VBUS EN 010111b: SSIBCK1 011000b: EDREQ1 011010b: SDHI_WP-C 011100b: PIXCLK	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000010b: MTCLKA 000011b: TIOCB4 000101b: TMRI1 000110b: PO4 001010b: SCK3 010011b: USB0_VBUS EN 010111b: SSIBCK1 011000b: EDREQ1 011010b: SDHI_WP-C 011100b: PIXCLK

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 7)
P25PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000010b: MTCLKB 000011b: TIOCA4 000110b: PO5 001001b: ADTRG0# 001010b: RXD3/SMISO3/ SSCL3 010111b: SSIDATA1 011000b: EDACK1 011010b: SDHI_CD 011100b: HSYNC 101010b: CLKOUT	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000010b: MTCLKB 000011b: TIOCA4 000110b: PO5 001001b: ADTRG0# 001010b: RXD3/SMISO3/ SSCL3 010111b: SSIDATA1 011000b: EDACK1 011010b: SDHI_CD-C 011100b: HSYNC 101010b: CLKOUT	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000010b: MTCLKB 000011b: TIOCA4 000110b: PO5 001001b: ADTRG0# 001010b: RXD3/SMISO3/ SSCL3 010111b: SSIDATA1 011000b: EDACK1 011010b: SDHI_CD-C 011100b: HSYNC 101010b: CLKOUT
P26PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2A 000101b: TMO1 000110b: PO6 001010b: TXD1/SMOSI1/ SSDA1 001011b: CTS3#/ RTS3#/SS3# 001101b: MOSIB-A 010100b: ET1_EXOUT 100111b: CATLINKACT1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2A 000101b: TMO1 000110b: PO6 001010b: TXD1/SMOSI1/ SSDA1 001011b: TS3#/ RTS3#/SS3# 001101b: MOSIB-A 010100b: ET1_EXOUT 100111b: CATLINKACT1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2A 000101b: TMO1 000110b: PO6 001010b: TXD1/SMOSI1/ SSDA1 001011b: CTS3#/ RTS3#/SS3# 001101b: MOSIB-A
P27PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2B 000101b: TMCI3 000110b: PO7 001010b: SCK1 001101b: RSPCKB-A 010100b: ET1_WOL 100111b: CATIRQ	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2B 000101b: TMCI3 000110b: PO7 001010b: SCK1 001101b: RSPCKB-A 010100b: ET1_WOL 100111b: CATIRQ	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2B 000101b: TMCI3 000110b: PO7 001010b: SCK1 001101b: RSPCKB-A

Table 2.18 Comparison of P3n Pin Function Control Register (P3nPFS)

Register	Bit	RX72M (n = 0 to 4)	RX72N (n = 0 to 4)	RX66N (n = 0 to 4)
P30PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000101b: TMRI3 000110b: PO8 000111b: POE8# 001010b: RXD1/SMISO1/SSCL1 001101b: MISOB-A 010100b: ET1_MDIO 101000b: PMGI1_MDIO	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000101b: TMRI3 000110b: PO8 000111b: POE8# 001010b: RXD1/SMISO1/SSCL1 001101b: MISOB-A 010100b: ET1_MDIO 101000b: PMGI1_MDIO	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000101b: TMRI3 000110b: PO8 000111b: POE8# 001010b: RXD1/SMISO1/SSCL1 001101b: MISOB-A
P31PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000101b: TMCI2 000110b: PO9 001011b: CTS1#/RTS1#/SS1# 001101b: SSLB0-A 010100b: ET1_MDC 101000b: PMGI1_MDC	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000101b: TMCI2 000110b: PO9 001011b: CTS1#/RTS1#/SS1# 001101b: SSLB0-A 010100b: ET1_MDC 101000b: PMGI1_MDC	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000101b: TMCI2 000110b: PO9 001011b: CTS1#/RTS1#/SS1# 001101b: SSLB0-A
P33PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0D 000011b: TIOCD0 000101b: TMRI3 000110b: PO11 001000b: POE4# 001010b: RXD6/SMISO6/SSCL6 001011b: RXD0/SMISO0/SSCL0 010000b: CRX0 011000b: EDREQ1 011100b: PCKO 100001b: POE11# 101001b: DSMCLK0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0D 000011b: TIOCD0 000101b: TMRI3 000110b: PO11 001000b: POE4# 001010b: RXD6/SMISO6/SSCL6 001011b: RXD0/SMISO0/SSCL0 010000b: CRX0 011000b: EDREQ1 011100b: PCKO 100001b: POE11#	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0D 000011b: TIOCD0 000101b: TMRI3 000110b: PO11 001000b: POE4# 001010b: RXD6/SMISO6/SSCL6 001011b: RXD0/SMISO0/SSCL0 010000b: CRX0 011000b: EDREQ1 011100b: PCKO 100001b: POE11#

Register	Bit	RX72M (n = 0 to 4)	RX72N (n = 0 to 4)	RX66N (n = 0 to 4)
P34PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0A 000101b: TMCI3 000110b: PO12 000111b: POE10# 001010b: SCK6 001011b: SCK0 010001b: ET0_LINKSTA 100110b: CAT0_LINKSTA 101001b: DSMDAT0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0A 000101b: TMCI3 000110b: PO12 000111b: POE10# 001010b: SCK6 001011b: SCK0 010001b: ET0_LINKSTA	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0A 000101b: TMCI3 000110b: PO12 000111b: POE10# 001010b: SCK6 001011b: SCK0 010001b: ET0_LINKSTA

Table 2.19 Comparison of P5n Pin Function Control Register (P5nPFS)

Register	Bit	RX72M (n = 0 to 2, 4 to 7)	RX72N (n = 0 to 2, 4 to 7)	RX66N (n = 0 to 2, 4 to 7)
P50PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001010b: TXD2/SMOSI2/SSDA2 001101b: SSLB1-A 100111b: CATLEDERR	Pin function select bits 000000b: Hi-Z 001010b: TXD2/SMOSI2/SSDA2 001101b: SSLB1-A	Pin function select bits 000000b: Hi-Z 001010b: TXD2/SMOSI2/SSDA2 001101b: SSLB1-A
P52PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001010b: RXD2/SMISO2/SSCL2 001101b: SSLB3-A 100111b: CATLEDSTER	Pin function select bits 000000b: Hi-Z 001010b: RXD2/SMISO2/SSCL2 001101b: SSLB3-A	Pin function select bits 000000b: Hi-Z 001010b: RXD2/SMISO2/SSCL2 001101b: SSLB3-A
P54PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000101b: TMCI1 001011b: CTS2#/RTS2#/SS2# 001101b: MOSIC-B 010000b: CTX1 010001b: ET0_LINKSTA 011000b: EDACK0 100101b: LCD_DATA6-A 100110b: CAT0_LINKSTA	Pin function select bits 000000b: Hi-Z 000101b: TMCI1 001011b: CTS2#/RTS2#/SS2# 001101b: MOSIC-B 010000b: CTX1 010001b: ET0_LINKSTA 011000b: EDACK0 100101b: LCD_DATA6-A	Pin function select bits 000000b: Hi-Z 000101b: TMCI1 001011b: CTS2#/RTS2#/SS2# 001101b: MOSIC-B 010000b: CTX1 010001b: ET0_LINKSTA 011000b: EDACK0 100101b: LCD_DATA6-A

Register	Bit	RX72M (n = 0 to 2, 4 to 7)	RX72N (n = 0 to 2, 4 to 7)	RX66N (n = 0 to 2, 4 to 7)
P56PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000011b: TIOCA1 001010b: SCK7 001101b: RSPCKC-B 011000b: EDACK1 100101b: LCD_DATA4-A 101001b: DSMDAT1 101010b: CLKOUT25M	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000011b: TIOCA1 001010b: SCK7 001101b: RSPCKC-B 011000b: EDACK1 100101b: LCD_DATA4-A 101010b: CLKOUT25M	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000011b: TIOCA1 001010b: SCK7 001101b: RSPCKC-B 011000b: EDACK1 100101b: LCD_DATA4-A 101010b: CLKOUT25M

Table 2.20 Comparison of P6n Pin Function Control Register (P6nPFS)

Register	Bit	RX72M (n = 0 to 4, 6, 7)	RX72N (n = 0 to 4, 6, 7)	RX66N (n = 6, 7)
P60PFS	PSEL[5:0]	Pin function select bits	Pin function select bits	—
P61PFS	PSEL[5:0]	Pin function select bits	Pin function select bits	—
P62PFS	PSEL[5:0]	Pin function select bits	Pin function select bits	—
P63PFS	PSEL[5:0]	Pin function select bits	Pin function select bits	—
P64PFS	PSEL[5:0]	Pin function select bits	Pin function select bits	—
P67PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001000b: MTIOC7C 010000b: CRX2 010001b: EPLSOUT1 011110b: GTIOC1B 100111b: CATSYNC1	Pin function select bits 000000b: Hi-Z 001000b: MTIOC7C 010000b: CRX2 010001b: EPLSOUT1 011110b: GTIOC1B	Pin function select bits 000000b: Hi-Z 001000b: MTIOC7C 010000b: CRX2 011110b: GTIOC1B

Table 2.21 Comparison of P7n Pin Function Control Register (P7nPFS)

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 1 to 7)	RX66N (n = 1 to 7)
P70PFS	PSEL[5:0]	Pin function select bits	—	—
P71PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 010001b: ET0_MDIO 100110b: CAT0_MDIO 101000b: PMGI0_MDIO 101001b: DSMCLK3	Pin function select bits 000000b: Hi-Z 010001b: ET0_MDIO 101000b: PMGI0_MDIO	Pin function select bits 000000b: Hi-Z 010001b: ET0_MDIO 101000b: PMGI0_MDIO
P72PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 010001b: ET0_MDC 100101b: LCD_DATA23-A 100110b: CAT0_MDC 101000b: PMGI0_MDC 101001b: DSMDAT3	Pin function select bits 000000b: Hi-Z 010001b: ET0_MDC 100101b: LCD_DATA23-A 101000b: PMGI0_MDC	Pin function select bits 000000b: Hi-Z 010001b: ET0_MDC 100101b: LCD_DATA23-A 101000b: PMGI0_MDC

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 1 to 7)	RX66N (n = 1 to 7)
P74PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000110b: PO19 001011b: SS11#/CTS11# 010001b: ET0_ERXD1 010010b: RMII0_RXD1 100101b: LCD_DATA21-A 100110b: CAT0_ERXD1 101001b: DSMCLK2	Pin function select bits 000000b: Hi-Z 000110b: PO19 001011b: SS11#/CTS11# 010001b: ET0_ERXD1 010010b: RMII0_RXD1 100101b: LCD_DATA21-A	Pin function select bits 000000b: Hi-Z 000110b: PO19 001011b: SS11#/CTS11# 010001b: ET0_ERXD1 010010b: RMII0_RXD1 100101b: LCD_DATA21-A
P75PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000110b: PO20 001010b: SCK11 001011b: RTS11# 010001b: ET0_ERXD0 010010b: RMII0_RXD0 011001b: MMC_RES#-A 011010b: SDHI_D2-A 100101b: LCD_DATA20-A 100110b: CAT0_ERXD0 101001b: DSMDAT2	Pin function select bits 000000b: Hi-Z 000110b: PO20 001010b: SCK11 001011b: RTS11# 010001b: ET0_ERXD0 010010b: RMII0_RXD0 011001b: MMC_RES#-A 011010b: SDHI_D2-A 100101b: LCD_DATA20-A	Pin function select bits 000000b: Hi-Z 000110b: PO20 001010b: SCK11 001011b: RTS11# 010001b: ET0_ERXD0 010010b: RMII0_RXD0 011001b: MMC_RES#-A 011010b: SDHI_D2-A 100101b: LCD_DATA20-A
P76PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000110b: PO22 001010b: SMISO11/ SSCL11/ RXD11 010001b: ET0_RX_CLK 010010b: REF50CK0 011001b: MMC_CMD-A 011010b: SDHI_CMD-A 011011b: QSSL-A 100101b: LCD_DATA18-A 100110b: CAT0_RX_CLK	Pin function select bits 000000b: Hi-Z 000110b: PO22 001010b: SMISO11/ SSCL11/ RXD11 010001b: ET0_RX_CLK 010010b: REF50CK0 011001b: MMC_CMD-A 011010b: SDHI_CMD-A 011011b: QSSL-A 100101b: LCD_DATA18-A	Pin function select bits 000000b: Hi-Z 000110b: PO22 001010b: SMISO11/ SSCL11/ RXD11 010001b: ET0_RX_CLK 010010b: REF50CK0 011001b: MMC_CMD-A 011010b: SDHI_CMD-A 011011b: QSSL-A 100101b: LCD_DATA18-A

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 1 to 7)	RX66N (n = 1 to 7)
P77PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000110b: PO23 001010b: SMOSI11/ SSDA11/ TXD11 010001b: ET0_RX_ER 010010b: RMII0_RX_ER 011001b: MMC_CLK-A 011010b: SDHI_CLK-A 011011b: QSPCLK-A 100101b: LCD_DATA17-A 100110b: CAT0_RX_ER	Pin function select bits 000000b: Hi-Z 000110b: PO23 001010b: SMOSI11/ SSDA11/ TXD11 010001b: ET0_RX_ER 010010b: RMII0_RX_ER 011001b: MMC_CLK-A 011010b: SDHI_CLK-A 011011b: QSPCLK-A 100101b: LCD_DATA17-A	Pin function select bits 000000b: Hi-Z 000110b: PO23 001010b: SMOSI11/ SSDA11/ TXD11 010001b: ET0_RX_ER 010010b: RMII0_RX_ER 011001b: MMC_CLK-A 011010b: SDHI_CLK-A 011011b: QSPCLK-A 100101b: LCD_DATA17-A

Table 2.22 Comparison of P8n Pin Function Control Register (P8nPFS)

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 7)
P80PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000110b: PO26 001010b: SCK10 001011b: RTS10# 010001b: ET0_TX_EN 010010b: RMII0_TXD_EN 011000b: EDREQ0 011001b: MMC_D2-A 011010b: SDHI_WP 011011b: QIO2-A 100101b: LCD_DATA14-A 100110b: CAT0_TX_EN 100111b: CATLATCH0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000110b: PO26 001010b: SCK10 001011b: RTS10# 010001b: ET0_TX_EN 010010b: RMII0_TXD_EN 011000b: EDREQ0 011001b: MMC_D2-A 011010b: SDHI_WP-A 011011b: QIO2-A 100101b: LCD_DATA14-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000110b: PO26 001010b: SCK10 001011b: RTS10# 010001b: ET0_TX_EN 010010b: RMII0_TXD_EN 011000b: EDREQ0 011001b: MMC_D2-A 011010b: SDHI_WP-A 011011b: QIO2-A 100101b: LCD_DATA14-A

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 7)
P81PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000110b: PO27 001010b: SMISO10/ SSCL10/ RXD10 010001b: ET0_ETXD0 010010b: RMII0_TXD0 011000b: EDACK0 011001b: MMC_D3-A 011010b: SDHI_CD 011011b: QIO3-A 011110b: GTIOC0B 100101b: LCD_DATA13-A 100110b: CAT0_ETXD0 100111b: CATI2CCLK	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000110b: PO27 001010b: SMISO10/ SSCL10/ RXD10 010001b: ET0_ETXD0 010010b: RMII0_TXD0 011000b: EDACK0 011001b: MMC_D3-A 011010b: SDHI_CD-A 011011b: QIO3-A 011110b: GTIOC0B 100101b: LCD_DATA13-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000110b: PO27 001010b: SMISO10/ SSCL10/ RXD10 010001b: ET0_ETXD0 010010b: RMII0_TXD0 011000b: EDACK0 011001b: MMC_D3-A 011010b: SDHI_CD-A 011011b: QIO3-A 011110b: GTIOC0B 100101b: LCD_DATA13-A
P82PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000110b: PO28 001010b: SMOSI10/ SSDA10/ TXD10 010001b: ET0_ETXD1 010010b: RMII0_TXD1 011000b: EDREQ1 011001b: MMC_D4-A 011110b: GTIOC2A 100101b: LCD_DATA12-A 100110b: CAT0_ETXD1 100111b: CATI2CDATA	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000110b: PO28 001010b: SMOSI10/ SSDA10/ TXD10 010001b: ET0_ETXD1 010010b: RMII0_TXD1 011000b: EDREQ1 011001b: MMC_D4-A 011110b: GTIOC2A 100101b: LCD_DATA12-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000110b: PO28 001010b: SMOSI10/ SSDA10/ TXD10 010001b: ET0_ETXD1 010010b: RMII0_TXD1 011000b: EDREQ1 011001b: MMC_D4-A 011110b: GTIOC2A 100101b: LCD_DATA12-A
P83PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 001010b: SCK10 001011b: SS10#/CTS10# 010001b: ET0_CRS 010010b: RMII0_CRS_ DV 011000b: EDACK1 011110b: GTIOC0A 100101b: LCD_DATA8-A 100110b: CAT0_RX_DV 101001b: DSMCLK1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 001010b: SCK10 001011b: SS10#/CTS10# 010001b: ET0_CRS 010010b: RMII0_CRS_ DV 011000b: EDACK1 011110b: GTIOC0A 100101b: LCD_DATA8-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 001010b: SCK10 001011b: SS10#/CTS10# 010001b: ET0_CRS 010010b: RMII0_CRS_ DV 011000b: EDACK1 011110b: GTIOC0A 100101b: LCD_DATA8-A

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 7)
P84PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC6D 010100b: ET1_LINKSTA 100101b: LCD_DATA2-A 100110b: CAT1_LINKSTA	Pin function select bits 000000b: Hi-Z 000001b: MTIOC6D 010100b: ET1_LINKSTA 100101b: LCD_DATA2-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC6D 100101b: LCD_DATA2-A
P86PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000011b: TIOCA0 001000b: MTIOC4D 001010b: SMISO10/ SSCL10/ RXD10 011100b: PIXD1 011110b: GTIOC2B 100111b: CATLINKACT0	Pin function select bits 000000b: Hi-Z 000011b: TIOCA0 001000b: MTIOC4D 001010b: SMISO10/ SSCL10/ RXD10 011100b: PIXD1 011110b: GTIOC2B	Pin function select bits 000000b: Hi-Z 000011b: TIOCA0 001000b: MTIOC4D 001010b: SMISO10/ SSCL10/ RXD10 011100b: PIXD1 011110b: GTIOC2B
P87PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000011b: TIOCA2 001000b: MTIOC4C 001010b: SMOSI10/ SSDA10/ TXD10 010001b: EPLSOUT1 011010b: SDHI_D2-C 011100b: PIXD2 011110b: GTIOC1B 100111b: CATSYNC1	Pin function select bits 000000b: Hi-Z 000011b: TIOCA2 001000b: MTIOC4C 001010b: SMOSI10/ SSDA10/ TXD10 010001b: EPLSOUT1 011010b: SDHI_D2-C 011100b: PIXD2 011110b: GTIOC1B	Pin function select bits 000000b: Hi-Z 000011b: TIOCA2 001000b: MTIOC4C 001010b: SMOSI10/ SSDA10/ TXD10 011010b: SDHI_D2-C 011100b: PIXD2 011110b: GTIOC1B

Table 2.23 Comparison of P9n Pin Function Control Register (P9nPFS)

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 3)
P90PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001010b: TXD7/SMOSI7/ SSDA7 010100b: ET1_RX_DV 100110b: CAT1_RX_DV 101001b: DSMCLK5	Pin function select bits 000000b: Hi-Z 001010b: TXD7/SMOSI7/ SSDA7 010100b: ET1_RX_DV	Pin function select bits 000000b: Hi-Z 001010b: TXD7/SMOSI7/ SSDA7
P91PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001010b: SCK7 010100b: ET1_COL 101001b: DSMDAT5	Pin function select bits 000000b: Hi-Z 001010b: SCK7 010100b: ET1_COL	Pin function select bits 000000b: Hi-Z 001010b: SCK7
P92PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001000b: POE4# 001010b: RXD7/SMISO7/ SSCL7 010100b: ET1_CRS 010101b: RMII1_CRS_ DV 100110b: CAT1_RX_DV 101001b: DSMCLK4	Pin function select bits 000000b: Hi-Z 001000b: POE4# 001010b: RXD7/SMISO7/ SSCL7 010100b: ET1_CRS 010101b: RMII1_CRS_ DV	Pin function select bits 000000b: Hi-Z 001000b: POE4# 001010b: RXD7/SMISO7/ SSCL7
P93PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001000b: POE0# 001011b: CTS7#/RTS7#/ SS7# 010100b: ET1_LINKSTA 100110b: CAT1_LINKS TA 101001b: DSMDAT4	Pin function select bits 000000b: Hi-Z 001000b: POE0# 001011b: CTS7#/RTS7#/ SS7# 010100b: ET1_LINKSTA	Pin function select bits 000000b: Hi-Z 001000b: POE0# 001011b: CTS7#/RTS7#/ SS7#
P94PFS	PSEL[5:0]	Pin function select bits	Pin function select bits	—
P95PFS	PSEL[5:0]	Pin function select bits	Pin function select bits	—
P96PFS	PSEL[5:0]	Pin function select bits	Pin function select bits	—
P97PFS	PSEL[5:0]	Pin function select bits	Pin function select bits	—

Table 2.24 Comparison of PAn Pin Function Control Register (PAnPFS)

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 7)
PA0PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000011b: TIOCA0 000110b: PO16 000111b: CACREF 001000b: MTIOC6D 001101b: SSLA1-B 010001b: ET0_TX_EN 010010b: RMII0_TXD_EN 011110b: GTIOC0B 100101b: LCD_DATA8-B 100110b: CAT0_TX_EN 100111b: CATLEDRUN	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000011b: TIOCA0 000110b: PO16 000111b: CACREF 001000b: MTIOC6D 001101b: SSLA1-B 010001b: ET0_TX_EN 010010b: RMII0_TXD_EN 011110b: GTIOC0B 100101b: LCD_DATA8-B	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000011b: TIOCA0 000110b: PO16 000111b: CACREF 001000b: MTIOC6D 001101b: SSLA1-B 010001b: ET0_TX_EN 010010b: RMII0_TXD_EN 011110b: GTIOC0B 100101b: LCD_DATA8-B
PA2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000110b: PO18 001000b: MTIOC7A 001010b: RXD5/SMISO5/SSCL5 001101b: SSLA3-B 011110b: GTIOC1A 100101b: LCD_DATA6-B 100111b: CATLINKACT1	Pin function select bits 000000b: Hi-Z 000110b: PO18 001000b: MTIOC7A 001010b: RXD5/SMISO5/SSCL5 001101b: SSLA3-B 011110b: GTIOC1A 100101b: LCD_DATA6-B	Pin function select bits 000000b: Hi-Z 000110b: PO18 001000b: MTIOC7A 001010b: RXD5/SMISO5/SSCL5 001101b: SSLA3-B 011110b: GTIOC1A 100101b: LCD_DATA6-B
PA3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0D 000010b: MTCLKD 000011b: TIOCD0 000100b: TCLKB 000110b: PO19 001010b: RXD5/SMISO5/SSCL5 010001b: ET0_MDIO 100101b: LCD_DATA5-B 100110b: CAT0_MDIO 101000b: PMGI0_MDIO	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0D 000010b: MTCLKD 000011b: TIOCD0 000100b: TCLKB 000110b: PO19 001010b: RXD5/SMISO5/SSCL5 010001b: ET0_MDIO 100101b: LCD_DATA5-B 101000b: PMGI0_MDIO	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0D 000010b: MTCLKD 000011b: TIOCD0 000100b: TCLKB 000110b: PO19 001010b: RXD5/SMISO5/SSCL5 010001b: ET0_MDIO 100101b: LCD_DATA5-B 101000b: PMGI0_MDIO

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 7)
PA4PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000010b: MTCLKA 000011b: TIOCA1 000101b: TMRI0 000110b: PO20 001010b: TXD5/SMOSI5/SSDA5 001101b: SSLA0-B 010001b: ET0_MDC 100101b: LCD_DATA4-B 100110b: CAT0_MDC 100111b: CATIRQ 101000b: PMGI0_MDC	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000010b: MTCLKA 000011b: TIOCA1 000101b: TMRI0 000110b: PO20 001010b: TXD5/SMOSI5/SSDA5 001101b: SSLA0-B 010001b: ET0_MDC 100101b: LCD_DATA4-B 101000b: PMGI0_MDC	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000010b: MTCLKA 000011b: TIOCA1 000101b: TMRI0 000110b: PO20 001010b: TXD5/SMOSI5/SSDA5 001101b: SSLA0-B 010001b: ET0_MDC 100101b: LCD_DATA4-B 101000b: PMGI0_MDC
PA5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000011b: TIOCB1 000110b: PO21 001000b: MTIOC6B 001101b: RSPCKA-B 010001b: ET0_LINKSTA 011110b: GTIOC0A 100101b: LCD_DATA3-B 100110b: CAT0_LINKSTA	Pin function select bits 000000b: Hi-Z 000011b: TIOCB1 000110b: PO21 001000b: MTIOC6B 001101b: RSPCKA-B 010001b: ET0_LINKSTA 011110b: GTIOC0A 100101b: LCD_DATA3-B	Pin function select bits 000000b: Hi-Z 000011b: TIOCB1 000110b: PO21 001000b: MTIOC6B 001101b: RSPCKA-B 010001b: ET0_LINKSTA 011110b: GTIOC0A 100101b: LCD_DATA3-B
PA6PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000010b: MTCLKB 000011b: TIOCA2 000101b: TMCI3 000110b: PO22 000111b: POE10# 001011b: CTS5#/RTS5#/SS5# 001101b: MOSIA-B 010001b: ET0_EXOUT 011110b: GTETRGB 100101b: LCD_DATA2-B 100111b: CATRESTOUT	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000010b: MTCLKB 000011b: TIOCA2 000101b: TMCI3 000110b: PO22 000111b: POE10# 001011b: CTS5#/RTS5#/SS5# 001101b: MOSIA-B 010001b: ET0_EXOUT 011110b: GTETRGB 100101b: LCD_DATA2-B	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000010b: MTCLKB 000011b: TIOCA2 000101b: TMCI3 000110b: PO22 000111b: POE10# 001011b: CTS5#/RTS5#/SS5# 001101b: MOSIA-B 010001b: ET0_EXOUT 011110b: GTETRGB 100101b: LCD_DATA2-B

Table 2.25 Comparison of PBn Pin Function Control Register (PBnPFS)

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 7)
PB0PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5W 000011b: TIOCA3 000110b: PO24 001010b: RXD4/SMISO4/SSCL4 001011b: RXD6/SMISO6/SSCL6 010001b: ET0_ERXD1 010010b: RMII0_RXD1 100101b: LCD_DATA0-B 100110b: CAT0_ERXD1	Pin function select bits 000000b: Hi-Z 000001b: MTIC5W 000011b: TIOCA3 000110b: PO24 001010b: RXD4/SMISO4/SSCL4 001011b: RXD6/SMISO6/SSCL6 010001b: ET0_ERXD1 010010b: RMII0_RXD1 100101b: LCD_DATA0-B	Pin function select bits 000000b: Hi-Z 000001b: MTIC5W 000011b: TIOCA3 000110b: PO24 001010b: RXD4/SMISO4/SSCL4 001011b: RXD6/SMISO6/SSCL6 010001b: ET0_ERXD1 010010b: RMII0_RXD1 100101b: LCD_DATA0-B
PB1PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0C 000010b: MTIOC4C 000011b: TIOCB3 000101b: TMCI0 000110b: PO25 001010b: TXD4/SMOSI4/SSDA4 001011b: TXD6/SMOSI6/SSDA6 010001b: ET0_ERXD0 010010b: RMII0_RXD0 100101b: LCD_TCON3-B 100110b: CAT0_ERXD0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0C 000010b: MTIOC4C 000011b: TIOCB3 000101b: TMCI0 000110b: PO25 001010b: TXD4/SMOSI4/SSDA4 001011b: TXD6/SMOSI6/SSDA6 010001b: ET0_ERXD0 010010b: RMII0_RXD0 100101b: LCD_TCON3-B	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0C 000010b: MTIOC4C 000011b: TIOCB3 000101b: TMCI0 000110b: PO25 001010b: TXD4/SMOSI4/SSDA4 001011b: TXD6/SMOSI6/SSDA6 010001b: ET0_ERXD0 010010b: RMII0_RXD0 100101b: LCD_TCON3-B
PB2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000011b: TIOCC3 000100b: TCLKC 000110b: PO26 001010b: CTS4#/RTS4#/SS4# 001011b: CTS6#/RTS6#/SS6# 010001b: ET0_RX_CLK 010010b: REF50CK0 100101b: LCD_TCON2-B 100110b: CAT0_RX_CLK	Pin function select bits 000000b: Hi-Z 000011b: TIOCC3 000100b: TCLKC 000110b: PO26 001010b: CTS4#/RTS4#/SS4# 001011b: CTS6#/RTS6#/SS6# 010001b: ET0_RX_CLK 010010b: REF50CK0 100101b: LCD_TCON2-B	Pin function select bits 000000b: Hi-Z 000011b: TIOCC3 000100b: TCLKC 000110b: PO26 001010b: CTS4#/RTS4#/SS4# 001011b: CTS6#/RTS6#/SS6# 010001b: ET0_RX_CLK 010010b: REF50CK0 100101b: LCD_TCON2-B

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 7)
PB3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0A 000010b: MTIOC4A 000011b: TIOCD3 000100b: TCLKD 000101b: TMO0 000110b: PO27 000111b: POE11# 001010b: SCK4 001011b: SCK6 010001b: ET0_RX_ER 010010b: RMII0_RX_ER 100101b: LCD_TCON1-B 100110b: CAT0_RX_ER	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0A 000010b: MTIOC4A 000011b: TIOCD3 000100b: TCLKD 000101b: TMO0 000110b: PO27 000111b: POE11# 001010b: SCK4 001011b: SCK6 010001b: ET0_RX_ER 010010b: RMII0_RX_ER 100101b: LCD_TCON1-B	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0A 000010b: MTIOC4A 000011b: TIOCD3 000100b: TCLKD 000101b: TMO0 000110b: PO27 000111b: POE11# 001010b: SCK4 001011b: SCK6 010001b: ET0_RX_ER 010010b: RMII0_RX_ER 100101b: LCD_TCON1-B
PB4PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000011b: TIOCA4 000110b: PO28 001011b: SS9#/CTS9# 010001b: ET0_TX_EN 010010b: RMII0_TXD_EN 100100b: SS11#/CTS11#/RTS11# 100101b: LCD_TCON0-B 100110b: CAT0_TX_EN	Pin function select bits 000000b: Hi-Z 000011b: TIOCA4 000110b: PO28 001011b: SS9#/CTS9# 010001b: ET0_TX_EN 010010b: RMII0_TXD_EN 100100b: SS11#/CTS11#/RTS11# 100101b: LCD_TCON0-B	Pin function select bits 000000b: Hi-Z 000011b: TIOCA4 000110b: PO28 001011b: SS9#/CTS9# 010001b: ET0_TX_EN 010010b: RMII0_TXD_EN 100100b: SS11#/CTS11#/RTS11# 100101b: LCD_TCON0-B
PB5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2A 000010b: MTIOC1B 000011b: TIOCB4 000101b: TMRI1 000110b: PO29 000111b: POE4# 001010b: SCK9 001011b: RTS9# 010001b: ET0_ETXD0 010010b: RMII0_TXD0 100100b: SCK11 100101b: LCD_CLK-B 100110b: CAT0_ETXD0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2A 000010b: MTIOC1B 000011b: TIOCB4 000101b: TMRI1 000110b: PO29 000111b: POE4# 001010b: SCK9 001011b: RTS9# 010001b: ET0_ETXD0 010010b: RMII0_TXD0 100100b: SCK11 100101b: LCD_CLK-B	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2A 000010b: MTIOC1B 000011b: TIOCB4 000101b: TMRI1 000110b: PO29 000111b: POE4# 001010b: SCK9 001011b: RTS9# 010001b: ET0_ETXD0 010010b: RMII0_TXD0 100100b: SCK11 100101b: LCD_CLK-B

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 7)
PB6PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000011b: TIOCA5 000110b: PO30 001010b: RXD9/SMISO9/ SSCL9 010001b: ET0_ETXD1 010010b: RMII0_TXD1 100100b: SMISO11/ SSCL11/ RXD11 100110b: CAT0_ETXD1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000011b: TIOCA5 000110b: PO30 001010b: RXD9/SMISO9/ SSCL9 010001b: ET0_ETXD1 010010b: RMII0_TXD1 100100b: SMISO11/ SSCL11/ RXD11	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000011b: TIOCA5 000110b: PO30 001010b: RXD9/SMISO9/ SSCL9 010001b: ET0_ETXD1 010010b: RMII0_TXD1 100100b: SMISO11/ SSCL11/ RXD11
PB7PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000011b: TIOCB5 000110b: PO31 001010b: TXD9/SMOSI9/ SSDA9 010001b: ET0_CRS 010010b: RMII0_CRS_ DV 100100b: SMOSI11/ SSDA11/ TXD11 100110b: CAT0_RX_DV	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000011b: TIOCB5 000110b: PO31 001010b: TXD9/SMOSI9/ SSDA9 010001b: ET0_CRS 010010b: RMII0_CRS_ DV 100100b: SMOSI11/ SSDA11/ TXD11	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000011b: TIOCB5 000110b: PO31 001010b: TXD9/SMOSI9/ SSDA9 010001b: ET0_CRS 010010b: RMII0_CRS_ DV 100100b: SMOSI11/ SSDA11/ TXD11

Table 2.26 Comparison of PCn Pin Function Control Register (PCnPFS)

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 7)
PC0PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000011b: TCLKC 000110b: PO17 001011b: CTS5#/RTS5#/ SS5# 001101b: SSLA1-A 010001b: ET0_ERXD3 100110b: CAT0_ERXD3	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000011b: TCLKC 000110b: PO17 001011b: CTS5#/RTS5#/ SS5# 001101b: SSLA1-A 010001b: ET0_ERXD3	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000011b: TCLKC 000110b: PO17 001011b: CTS5#/RTS5#/ SS5# 001101b: SSLA1-A 010001b: ET0_ERXD3

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 7)
PC1PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000011b: TCLKD 000110b: PO18 001010b: SCK5 001101b: SSLA2-A 010001b: ET0_ERXD2 100101b: LCD_DATA22-A 100110b: CAT0_ERXD2	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000011b: TCLKD 000110b: PO18 001010b: SCK5 001101b: SSLA2-A 010001b: ET0_ERXD2 100101b: LCD_DATA22-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000011b: TCLKD 000110b: PO18 001010b: SCK5 001101b: SSLA2-A 010001b: ET0_ERXD2 100101b: LCD_DATA22-A
PC2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000011b: TCLKA 000110b: PO21 001010b: RXD5/SMISO5/SSCL5 001101b: SSLA3-A 010001b: ET0_RX_DV 011001b: MMC_CD-A 011010b: SDHI_D3-A 011110b: GTIOC2B 100101b: LCD_DATA19-A 100110b: CAT0_RX_DV	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000011b: TCLKA 000110b: PO21 001010b: RXD5/SMISO5/SSCL5 001101b: SSLA3-A 010001b: ET0_RX_DV 011001b: MMC_CD-A 011010b: SDHI_D3-A 011110b: GTIOC2B 100101b: LCD_DATA19-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000011b: TCLKA 000110b: PO21 001010b: RXD5/SMISO5/SSCL5 001101b: SSLA3-A 010001b: ET0_RX_DV 011001b: MMC_CD-A 011010b: SDHI_D3-A 011110b: GTIOC2B 100101b: LCD_DATA19-A
PC3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000011b: TCLKB 000110b: PO24 001010b: TXD5/SMOSI5/SSDA5 010001b: ET0_TX_ER 011001b: MMC_D0-A 011010b: SDHI_D0-A 011011b: QMO-A/QIO0-A 011110b: GTIOC1B 100101b: LCD_DATA16-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000011b: TCLKB 000110b: PO24 001010b: TXD5/SMOSI5/SSDA5 010001b: ET0_TX_ER 011001b: MMC_D0-A 011010b: SDHI_D0-A 011011b: QMO/QIO0 011110b: GTIOC1B 100101b: LCD_DATA16-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000011b: TCLKB 000110b: PO24 001010b: TXD5/SMOSI5/SSDA5 010001b: ET0_TX_ER 011001b: MMC_D0-A 011010b: SDHI_D0-A 011011b: QMO/QIO0 011110b: GTIOC1B 100101b: LCD_DATA16-A

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 7)
PC4PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKC 000101b: TMCI1 000110b: PO25 000111b: POE0# 001010b: SCK5 001011b: SS8#/CTS8# 001101b: SSLA0-A 010001b: ET0_TX_CLK 011001b: MMC_D1-A 011010b: SDHI_D1-A 011011b: QMI-A/QIO1-A 011110b: GTETRGC 100100b: SS10#/ CTS10#/ RTS10# 100101b: LCD_DATA15- A 100110b: CAT0_TX_CLK 100111b: CATSYNC0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKC 000101b: TMCI1 000110b: PO25 000111b: POE0# 001010b: SCK5 001011b: SS8#/CTS8# 001101b: SSLA0-A 010001b: ET0_TX_CLK 011001b: MMC_D1-A 011010b: SDHI_D1-A 011011b: QMI/QIO1 011110b: GTETRGC 100100b: SS10#/ CTS10#/ RTS10# 100101b: LCD_DATA15- A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKC 000101b: TMCI1 000110b: PO25 000111b: POE0# 001010b: SCK5 001011b: SS8#/CTS8# 001101b: SSLA0-A 010001b: ET0_TX_CLK 011001b: MMC_D1-A 011010b: SDHI_D1-A 011011b: QMI/QIO1 011110b: GTETRGC 100100b: SS10#/ CTS10#/ RTS10# 100101b: LCD_DATA15- A
PC5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKD 000101b: TMRI2 000110b: PO29 001010b: SCK8 001011b: RTS8# 001101b: RSPCKA-A 010001b: ET0_ETXD2 011001b: MMC_D5-A 011110b: GTIOC1A 100100b: SCK10 100101b: LCD_DATA11- A 100110b: CAT0_ETXD2	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKD 000101b: TMRI2 000110b: PO29 001010b: SCK8 001011b: RTS8# 001101b: RSPCKA-A 010001b: ET0_ETXD2 011001b: MMC_D5-A 011110b: GTIOC1A 100100b: SCK10 100101b: LCD_DATA11- A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKD 000101b: TMRI2 000110b: PO29 001010b: SCK8 001011b: RTS8# 001101b: RSPCKA-A 010001b: ET0_ETXD2 011001b: MMC_D5-A 011110b: GTIOC1A 100100b: SCK10 100101b: LCD_DATA11- A

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 7)
PC6PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTCLKA 000101b: TMCI2 000110b: PO30 001010b: RXD8/SMISO8/ SSCL8 001101b: MOSIA-A 010001b: ET0_ETXD3 011001b: MMC_D6-A 011101b: TIC0 011110b: GTIOC3B 100100b: SMISO10/ SSCL10/ RXD10 100101b: LCD_DATA10-A 100110b: CAT0_ETXD3 100111b: CATLATCH1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTCLKA 000101b: TMCI2 000110b: PO30 001010b: RXD8/SMISO8/ SSCL8 001101b: MOSIA-A 010001b: ET0_ETXD3 011001b: MMC_D6-A 011101b: TIC0 011110b: GTIOC3B 100100b: SMISO10/ SSCL10/ RXD10 100101b: LCD_DATA10-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTCLKA 000101b: TMCI2 000110b: PO30 001010b: RXD8/SMISO8/ SSCL8 001101b: MOSIA-A 010001b: ET0_ETXD3 011001b: MMC_D6-A 011101b: TIC0 011110b: GTIOC3B 100100b: SMISO10/ SSCL10/ RXD10 100101b: LCD_DATA10-A

Table 2.27 Comparison of PDn Pin Function Control Register (PDnPFS)

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 7)
PD2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 001101b: MISOC-A 010000b: CRX0 010100b: ET1_EXOUT 011001b: MMC_D2-B 011010b: SDHI_D2-B 011011b: QIO2-B 011101b: TIC2 011110b: GTIOC0B 100101b: LCD_DATA22-B	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 001101b: MISOC-A 010000b: CRX0 010100b: ET1_EXOUT 011001b: MMC_D2-B 011010b: SDHI_D2-B 011011b: QIO2-B 011101b: TIC2 011110b: GTIOC0B 100101b: LCD_DATA22-B	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 001101b: MISOC-A 010000b: CRX0 011001b: MMC_D2-B 011010b: SDHI_D2-B 011011b: QIO2-B 011101b: TIC2 011110b: GTIOC0B 100101b: LCD_DATA22-B

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 7)
PD3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000111b: POE8# 001000b: MTIOC8D 001101b: RSPCKC-A 010100b: ET1_WOL 011001b: MMC_D3-B 011010b: SDHI_D3-B 011011b: QIO3-B 011101b: TOC2 011110b: GTIOC0A 100101b: LCD_DATA21-B	Pin function select bits 000000b: Hi-Z 000111b: POE8# 001000b: MTIOC8D 001101b: RSPCKC-A 010100b: ET1_WOL 011001b: MMC_D3-B 011010b: SDHI_D3-B 011011b: QIO3-B 011101b: TOC2 011110b: GTIOC0A 100101b: LCD_DATA21-B	Pin function select bits 000000b: Hi-Z 000111b: POE8# 001000b: MTIOC8D 001101b: RSPCKC-A 011001b: MMC_D3-B 011010b: SDHI_D3-B 011011b: QIO3-B 011101b: TOC2 011110b: GTIOC0A 100101b: LCD_DATA21-B
PD4PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000111b: POE11# 001000b: MTIOC8B 001101b: SSLC0-A 010100b: ET1_MDIO 011001b: MMC_CMD-B 011010b: SDHI_CMD-B 011011b: QSSL-B 100101b: LCD_DATA20-B 101000b: PMGI1_MDIO	Pin function select bits 000000b: Hi-Z 000111b: POE11# 001000b: MTIOC8B 001101b: SSLC0-A 010100b: ET1_MDIO 011001b: MMC_CMD-B 011010b: SDHI_CMD-B 011011b: QSSL-B 100101b: LCD_DATA20-B 101000b: PMGI1_MDIO	Pin function select bits 000000b: Hi-Z 000111b: POE11# 001000b: MTIOC8B 001101b: SSLC0-A 011001b: MMC_CMD-B 011010b: SDHI_CMD-B 011011b: QSSL-B 100101b: LCD_DATA20-B
PD5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5W 000010b: MTCLKA 000111b: POE10# 001000b: MTIOC8C 001101b: SSLC1-A 010100b: ET1_MDC 011001b: MMC_CLK-B 011010b: SDHI_CLK-B 011011b: QSPCLK-B 100101b: LCD_DATA19-B 101000b: PMGI1_MDC	Pin function select bits 000000b: Hi-Z 000001b: MTIC5W 000010b: MTCLKA 000111b: POE10# 001000b: MTIOC8C 001101b: SSLC1-A 010100b: ET1_MDC 011001b: MMC_CLK-B 011010b: SDHI_CLK-B 011011b: QSPCLK-B 100101b: LCD_DATA19-B 101000b: PMGI1_MDC	Pin function select bits 000000b: Hi-Z 000001b: MTIC5W 000010b: MTCLKA 000111b: POE10# 001000b: MTIOC8C 001101b: SSLC1-A 011001b: MMC_CLK-B 011010b: SDHI_CLK-B 011011b: QSPCLK-B 100101b: LCD_DATA19-B

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 7)
PD6PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000111b: POE4# 001000b: MTIOC8A 001101b: SSLC2-A 010100b: ET1_RX_CLK 010101b: REF50CK1 011001b: MMC_D0-B 011010b: SDHI_D0-B 011011b: QMO-B/QIO0-B 100101b: LCD_DATA18-B 100110b: CAT1_RX_CLK	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000111b: POE4# 001000b: MTIOC8A 001101b: SSLC2-A 010100b: ET1_RX_CLK 010101b: REF50CK1 011001b: MMC_D0-B 011010b: SDHI_D0-B 011011b: QMO/QIO0 100101b: LCD_DATA18-B	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000111b: POE4# 001000b: MTIOC8A 001101b: SSLC2-A 011001b: MMC_D0-B 011010b: SDHI_D0-B 011011b: QMO/QIO0 100101b: LCD_DATA18-B
PD7PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000111b: POE0# 001101b: SSLC3-A 010100b: ET1_RX_ER 010101b: RMII1_RX_ER 011001b: MMC_D1-B 011010b: SDHI_D1-B 011011b: QMI-B/QIO1-B 100101b: LCD_DATA17-B 100110b: CAT1_RX_ER	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000111b: POE0# 001101b: SSLC3-A 010100b: ET1_RX_ER 010101b: RMII1_RX_ER 011001b: MMC_D1-B 011010b: SDHI_D1-B 011011b: QMI/QIO1 100101b: LCD_DATA17-B	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000111b: POE0# 001101b: SSLC3-A 011001b: MMC_D1-B 011010b: SDHI_D1-B 011011b: QMI/QIO1 100101b: LCD_DATA17-B

Table 2.28 Comparison of PEn Pin Function Control Register (PEnPFS)

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 7)
PE3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000110b: PO26 000111b: POE8# 001100b: CTS12#/RTS12#/SS12# 010001b: ET0_ERXD3 011001b: MMC_D7-B 011101b: TOC3 011110b: GTIOC2A 100101b: LCD_DATA13-B 100110b: CAT0_ERXD3	Pin function select bits 000000b: Hi-Z 000110b: PO26 000111b: POE8# 001100b: CTS12#/RTS12#/SS12# 010001b: ET0_ERXD3 011001b: MMC_D7-B 011101b: TOC3 011110b: GTIOC2A 100101b: LCD_DATA13-B	Pin function select bits 000000b: Hi-Z 000110b: PO26 000111b: POE8# 001100b: CTS12#/RTS12#/SS12# 010001b: ET0_ERXD3 011001b: MMC_D7-B 011101b: TOC3 011110b: GTIOC2A 100101b: LCD_DATA13-B

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 7)
PE4PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000010b: MTIOC1A 000110b: PO28 001101b: SSLB0-B 010001b: ET0_ERXD2 011110b: GTIOC1A 100101b: LCD_DATA12-B 100110b: CAT0_ERXD2	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000010b: MTIOC1A 000110b: PO28 001101b: SSLB0-B 010001b: ET0_ERXD2 011110b: GTIOC1A 100101b: LCD_DATA12-B	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000010b: MTIOC1A 000110b: PO28 001101b: SSLB0-B 010001b: ET0_ERXD2 011110b: GTIOC1A 100101b: LCD_DATA12-B
PE5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000010b: MTIOC2B 001101b: RSPCKB-B 010001b: ET0_RX_CLK 010010b: REF50CK0 011110b: GTIOC0A 100101b: LCD_DATA11-B 100110b: CAT0_RX_CLK	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000010b: MTIOC2B 001101b: RSPCKB-B 010001b: ET0_RX_CLK 010010b: REF50CK0 011110b: GTIOC0A 100101b: LCD_DATA11-B	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000010b: MTIOC2B 001101b: RSPCKB-B 010001b: ET0_RX_CLK 010010b: REF50CK0 011110b: GTIOC0A 100101b: LCD_DATA11-B
PE6PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001000b: MTIOC6C 001101b: MOSIB-B 011001b: MMC_CD-B 011010b: SDHI_CD 011101b: TIC1 011110b: GTIOC3B 100101b: LCD_DATA10-B	Pin function select bits 000000b: Hi-Z 001000b: MTIOC6C 001101b: MOSIB-B 011001b: MMC_CD-B 011010b: SDHI_CD-B 011101b: TIC1 011110b: GTIOC3B 100101b: LCD_DATA10-B	Pin function select bits 000000b: Hi-Z 001000b: MTIOC6C 001101b: MOSIB-B 011001b: MMC_CD-B 011010b: SDHI_CD-B 011101b: TIC1 011110b: GTIOC3B 100101b: LCD_DATA10-B
PE7PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001000b: MTIOC6A 001101b: MISOB-B 011001b: MMC_RES#-B 011010b: SDHI_WP 011101b: TOC1 011110b: GTIOC3A 100101b: LCD_DATA9-B	Pin function select bits 000000b: Hi-Z 001000b: MTIOC6A 001101b: MISOB-B 011001b: MMC_RES#-B 011010b: SDHI_WP-B 011101b: TOC1 011110b: GTIOC3A 100101b: LCD_DATA9-B	Pin function select bits 000000b: Hi-Z 001000b: MTIOC6A 001101b: MISOB-B 011001b: MMC_RES#-B 011010b: SDHI_WP-B 011101b: TOC1 011110b: GTIOC3A 100101b: LCD_DATA9-B

Table 2.29 Comparison of PFn Pin Function Control Register (PFnPFS)

Register	Bit	RX72M (n = 0 to 2, 5)	RX72N (n = 0 to 2, 5)	RX66N (n = 0 to 2, 5)
PF0PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001010b: TXD1/SMOSI1/ SSDA1 100111b: CATI2CDATA	Pin function select bits 000000b: Hi-Z 001010b: TXD1/SMOSI1/ SSDA1	Pin function select bits 000000b: Hi-Z 001010b: TXD1/SMOSI1/ SSDA1
PF2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001010b: RXD1/SMISO1/ SSCL1 100111b: CATI2CCLK	Pin function select bits 000000b: Hi-Z 001010b: RXD1/SMISO1/ SSCL1	Pin function select bits 000000b: Hi-Z 001010b: RXD1/SMISO1/ SSCL1
PF5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 010111b: SSILRCK0 100111b: CATLATCH0	Pin function select bits 000000b: Hi-Z 010111b: SSILRCK0	Pin function select bits 000000b: Hi-Z 010111b: SSILRCK0

Table 2.30 Comparison of PGn Pin Function Control Register (PGnPFS)

Register	Bit	RX72M/RX72N	RX66N
PGnPFS	—	PGn pin function control register (n = 0 to 7)	—

Table 2.31 Comparison of PHn Pin Function Control Register (PHnPFS)

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 7)
PH0PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001010b: SCK7 001101b: RSPCKA 011101b: TIC0 011110b: GTETRGA 100111b: CATLEDRUN	Pin function select bits 000000b: Hi-Z 001010b: SCK7 001101b: RSPCKA 011101b: TIC0 011110b: GTETRGA	Pin function select bits 000000b: Hi-Z 001010b: SCK7 001101b: RSPCKA 011101b: TIC0 011110b: GTETRGA
PH1PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001010b: SMISO7/ SSCL7/ RXD7 001101b: MOSIA 011101b: TOC0 011110b: GTETRGB 100111b: CATI2CCLK	Pin function select bits 000000b: Hi-Z 001010b: SMISO7/ SSCL7/ RXD7 001101b: MOSIA 011101b: TOC0 011110b: GTETRGB	Pin function select bits 000000b: Hi-Z 001010b: SMISO7/ SSCL7/ RXD7 001101b: MOSIA 011101b: TOC0 011110b: GTETRGB

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 7)
PH2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001010b: SMOSI7/ SSDA7/ TXD7 001101b: MISOA 011110b: GTETRGC 100111b: CATI2CDATA	Pin function select bits 000000b: Hi-Z 001010b: SMOSI7/ SSDA7/ TXD7 001101b: MISOA 011110b: GTETRGC	Pin function select bits 000000b: Hi-Z 001010b: SMOSI7/ SSDA7/ TXD7 001101b: MISOA 011110b: GTETRGC
PH3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001011b: RTS7#/CTS7#/ SS7# 001101b: SSLA0 011110b: GTETRGD 100111b: CATLEDERR	Pin function select bits 000000b: Hi-Z 001011b: RTS7#/CTS7#/ SS7# 001101b: SSLA0 011110b: GTETRGD	Pin function select bits 000000b: Hi-Z 001011b: RTS7#/CTS7#/ SS7# 001101b: SSLA0 011110b: GTETRGD
PH4PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001101b: SSLA1 011110b: GTADSM0 100111b: CATLEDSTER	Pin function select bits 000000b: Hi-Z 001101b: SSLA1 011110b: GTADSM0	Pin function select bits 000000b: Hi-Z 001101b: SSLA1 011110b: GTADSM0
PH5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001101b: SSLA2 011110b: GTADSM1 100111b: CATLATCH0	Pin function select bits 000000b: Hi-Z 001101b: SSLA2 011110b: GTADSM1	Pin function select bits 000000b: Hi-Z 001101b: SSLA2 011110b: GTADSM1
PH6PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001101b: SSLA3 011110b: GTIOC0A 101010b: CLKOUT 100111b: CATLATCH1	Pin function select bits 000000b: Hi-Z 001101b: SSLA3 011110b: GTIOC0A 101010b: CLKOUT	Pin function select bits 000000b: Hi-Z 001101b: SSLA3 011110b: GTIOC0A 101010b: CLKOUT

Table 2.32 Comparison of PJn Pin Function Control Register (PJnPFS)

Register	Bit	RX72M (n = 0 to 3, 5)	RX72N (n = 0 to 3, 5)	RX66N (n = 0 to 3, 5)
PJ0PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC6B 001010b: SCK8 001101b: SSLC1-B 010001b: EPLSOUT0 100101b: LCD_DATA0-A 100111b: CATSYNC0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC6B 001010b: SCK8 001101b: SSLC1-B 010001b: EPLSOUT0 100101b: LCD_DATA0-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC6B 001010b: SCK8 001101b: SSLC1-B 100101b: LCD_DATA0-A
PJ1PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC6A 001010b: RXD8/SMISO8/SSCL8 001101b: SSLC2-B 010001b: EPLSOUT1 100101b: LCD_TCON3-A 100111b: CATSYNC1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC6A 001010b: RXD8/SMISO8/SSCL8 001101b: SSLC2-B 010001b: EPLSOUT1 100101b: LCD_TCON3-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC6A 001010b: RXD8/SMISO8/SSCL8 001101b: SSLC2-B 100101b: LCD_TCON3-A
PJ3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 001010b: CTS6#/RTS6#/SS6# 001011b: CTS0#/RTS0#/SS0# 010001b: ET0_EXOUT 010111b: SSITXD0 011000b: EDACK1 011011b: QMO-C/QIO0-C 100111b: CATRESTOUT	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 001010b: CTS6#/RTS6#/SS6# 001011b: CTS0#/RTS0#/SS0# 010001b: ET0_EXOUT 010111b: SSITXD0 011000b: EDACK1 011011b: QMO-C/QIO0-C	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 001010b: CTS6#/RTS6#/SS6# 001011b: CTS0#/RTS0#/SS0# 010001b: ET0_EXOUT 010111b: SSITXD0 011000b: EDACK1 011011b: QMO-C/QIO0-C
PJ5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001011b: CTS2#/RTS2#/SS2# 010001b: EPLSOUT0 010111b: SSIRXD0 011011b: QMI-C/QIO1-C 100001b: POE8# 100111b: CATSYNC0	Pin function select bits 000000b: Hi-Z 001011b: CTS2#/RTS2#/SS2# 010001b: EPLSOUT0 010111b: SSIRXD0 011011b: QMI-C/QIO1-C 100001b: POE8#	Pin function select bits 000000b: Hi-Z 001011b: CTS2#/RTS2#/SS2# 010111b: SSIRXD0 011011b: QMI-C/QIO1-C 100001b: POE8#

Table 2.33 Comparison of PKn Pin Function Control Register (PKnPFS)

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 7)
PK0PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001010b: SCK8 001101b: RSPCKB 010001b: ET0_MDC 011101b: TIC1 011110b: GTETRGA 100110b: CAT0_MDC 101000b: PMGI0_MDC	Pin function select bits 000000b: Hi-Z 001010b: SCK8 001101b: RSPCKB 010001b: ET0_MDC 011101b: TIC1 011110b: GTETRGA 101000b: PMGI0_MDC	Pin function select bits 000000b: Hi-Z 001010b: SCK8 001101b: RSPCKB 010001b: ET0_MDC 011101b: TIC1 011110b: GTETRGA 101000b: PMGI0_MDC
PK2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001010b: SMOSI8/ SSDA8/TXD8 001101b: MISOB 010001b: ET0_RX_DV 011110b: GTETRGC 100110b: CAT0_RX_DV	Pin function select bits 000000b: Hi-Z 001010b: SMOSI8/ SSDA8/TXD8 001101b: MISOB 010001b: ET0_RX_DV 011110b: GTETRGC	Pin function select bits 000000b: Hi-Z 001010b: SMOSI8/ SSDA8/TXD8 001101b: MISOB 010001b: ET0_RX_DV 011110b: GTETRGC
PK4PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001101b: SSLB1 010001b: ET0_ERXD2 011110b: GTADSM0 100110b: CAT0_ERXD2	Pin function select bits 000000b: Hi-Z 001101b: SSLB1 010001b: ET0_ERXD2 011110b: GTADSM0	Pin function select bits 000000b: Hi-Z 001101b: SSLB1 010001b: ET0_ERXD2 011110b: GTADSM0
PK5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001101b: SSLB2 010001b: ET0_ERXD3 011110b: GTADSM1 100110b: CAT0_ERXD3	Pin function select bits 000000b: Hi-Z 001101b: SSLB2 010001b: ET0_ERXD3 011110b: GTADSM1	Pin function select bits 000000b: Hi-Z 001101b: SSLB2 010001b: ET0_ERXD3 011110b: GTADSM1
PK6PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001101b: SSLB3 011110b: GTIOC1A 100111b: CATLINKACT0	Pin function select bits 000000b: Hi-Z 001101b: SSLB3 011110b: GTIOC1A	Pin function select bits 000000b: Hi-Z 001101b: SSLB3 011110b: GTIOC1A
PK7PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 011110b: GTIOC1B 100111b: CATLINKACT1	Pin function select bits 000000b: Hi-Z 011110b: GTIOC1B	Pin function select bits 000000b: Hi-Z 011110b: GTIOC1B

Table 2.34 Comparison of PLn Pin Function Control Register (PLnPFS)

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 7)
PL0PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001010b: SCK9 001101b: RSPCKC 010001b: ET0_ERXD0 010010b: RMII0_RXD0 011101b: TIC2 011110b: GTETRGA 100110b: CAT0_ERXD0	Pin function select bits 000000b: Hi-Z 001010b: SCK9 001101b: RSPCKC 010001b: ET0_ERXD0 010010b: RMII0_RXD0 011101b: TIC2 011110b: GTETRGA	Pin function select bits 000000b: Hi-Z 001010b: SCK9 001101b: RSPCKC 010001b: ET0_ERXD0 010010b: RMII0_RXD0 011101b: TIC2 011110b: GTETRGA
PL1PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001010b: SMISO9/ SSCL9/RXD9 001101b: MOSIC 010001b: ET0_ERXD1 010010b: RMII0_RXD1 011101b: TOC2 011110b: GTETRGB 100110b: CAT0_ERXD1	Pin function select bits 000000b: Hi-Z 001010b: SMISO9/ SSCL9/RXD9 001101b: MOSIC 010001b: ET0_ERXD1 010010b: RMII0_RXD1 011101b: TOC2 011110b: GTETRGB	Pin function select bits 000000b: Hi-Z 001010b: SMISO9/ SSCL9/RXD9 001101b: MOSIC 010001b: ET0_ERXD1 010010b: RMII0_RXD1 011101b: TOC2 011110b: GTETRGB
PL2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001010b: SMOSI9/ SSDA9/TXD9 001101b: MISOC 010001b: ET0_RX_ER 010010b: RMII0_RX_ER 011110b: GTETRGC 100110b: CAT0_RX_ER	Pin function select bits 000000b: Hi-Z 001010b: SMOSI9/ SSDA9/TXD9 001101b: MISOC 010001b: ET0_RX_ER 010010b: RMII0_RX_ER 011110b: GTETRGC	Pin function select bits 000000b: Hi-Z 001010b: SMOSI9/ SSDA9/TXD9 001101b: MISOC 010001b: ET0_RX_ER 010010b: RMII0_RX_ER 011110b: GTETRGC
PL3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001011b: RTS9#/ CTS9#/SS9# 001101b: SSLC0 010001b: ET0_RX_CLK 010010b: REF50CK0 011110b: GTETRGD 100110b: CAT0_RX_CLK	Pin function select bits 000000b: Hi-Z 001011b: RTS9#/ CTS9#/SS9# 001101b: SSLC0 010001b: ET0_RX_CLK 010010b: REF50CK0 011110b: GTETRGD	Pin function select bits 000000b: Hi-Z 001011b: RTS9#/ CTS9#/SS9# 001101b: SSLC0 010001b: ET0_RX_CLK 010010b: REF50CK0 011110b: GTETRGD
PL4PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001101b: SSLC1 010001b: ET0_ETXD0 010010b: RMII0_TXD0 011110b: GTADSM0 100110b: CAT0_ETXD0	Pin function select bits 000000b: Hi-Z 001101b: SSLC1 010001b: ET0_ETXD0 010010b: RMII0_TXD0 011110b: GTADSM0	Pin function select bits 000000b: Hi-Z 001101b: SSLC1 010001b: ET0_ETXD0 010010b: RMII0_TXD0 011110b: GTADSM0

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 7)
PL5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001101b: SSLC2 010001b: ET0_ETXD1 010010b: RMII0_TXD1 011110b: GTADSM1 100110b: CAT0_ETXD1	Pin function select bits 000000b: Hi-Z 001101b: SSLC2 010001b: ET0_ETXD1 010010b: RMII0_TXD1 011110b: GTADSM1	Pin function select bits 000000b: Hi-Z 001101b: SSLC2 010001b: ET0_ETXD1 010010b: RMII0_TXD1 011110b: GTADSM1
PL6PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001101b: SSLC3 010001b: ET0_TX_EN 010010b: RMII0_TXD_EN 011110b: GTIOC2A 100110b: CAT0_TX_EN	Pin function select bits 000000b: Hi-Z 001101b: SSLC3 010001b: ET0_TX_EN 010010b: RMII0_TXD_EN 011110b: GTIOC2A	Pin function select bits 000000b: Hi-Z 001101b: SSLC3 010001b: ET0_TX_EN 010010b: RMII0_TXD_EN 011110b: GTIOC2A
PL7PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 010001b: ET0_MDIO 011110b: GTIOC2B 100110b: CAT0_MDIO 101000b: PMGI0_MDIO	Pin function select bits 000000b: Hi-Z 010001b: ET0_MDIO 011110b: GTIOC2B 101000b: PMGI0_MDIO	Pin function select bits 000000b: Hi-Z 010001b: ET0_MDIO 011110b: GTIOC2B 101000b: PMGI0_MDIO

Table 2.35 Comparison of PMn Pin Function Control Register (PMnPFS)

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 7)
PM0PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001010b: SCK10 010100b: ET1_ERXD0 010101b: RMII1_RXD0 011010b: SDHI_CLK 011011b: QSPCLK-A 011101b: TIC3 011110b: GTETRGA 100110b: CAT1_ERXD0	Pin function select bits 000000b: Hi-Z 001010b: SCK10 010100b: ET1_ERXD0 010101b: RMII1_RXD0 011010b: SDHI_CLK 011011b: QSPCLK-A 011101b: TIC3 011110b: GTETRGA	Pin function select bits 000000b: Hi-Z 001010b: SCK10 011010b: SDHI_CLK 011011b: QSPCLK-A 011101b: TIC3 011110b: GTETRGA
PM1PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001010b: SMISO10/ SSCL10/ XD10 010100b: ET1_ERXD1 010101b: RMII1_RXD1 011010b: SDHI_CMD 011011b: QSSL-A 011101b: TOC3 011110b: GTETRGB 100110b: CAT1_ERXD1	Pin function select bits 000000b: Hi-Z 001010b: SMISO10/ SSCL10/ RXD10 010100b: ET1_ERXD1 010101b: RMII1_RXD1 011010b: SDHI_CMD 011011b: QSSL-A 011101b: TOC3 011110b: GTETRGB	Pin function select bits 000000b: Hi-Z 001010b: SMISO10/ SSCL10/ RXD10 011010b: SDHI_CMD 011011b: QSSL-A 011101b: TOC3 011110b: GTETRGB
PM2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001010b: SMOSI10/ SSDA10/ TXD10 010100b: ET1_ERXD2 011010b: SDHI_D0 011011b: QMO/QIO0 011110b: GTETRGC 100110b: CAT1_ERXD2	Pin function select bits 000000b: Hi-Z 001010b: SMOSI10/ SSDA10/ TXD10 010100b: ET1_ERXD2 011010b: SDHI_D0 011011b: QMO/QIO0 011110b: GTETRGC	Pin function select bits 000000b: Hi-Z 001010b: SMOSI10/ SSDA10/ TXD10 011010b: SDHI_D0 011011b: QMO/QIO0 011110b: GTETRGC
PM3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001011b: RTS10#/ CTS10#/SS10# 010100b: ET1_ERXD3 011010b: SDHI_D1 011011b: QMI/QIO1 011110b: GTETRGD 100110b: CAT1_ERXD3	Pin function select bits 000000b: Hi-Z 001011b: RTS10#/ CTS10#/SS10# 010100b: ET1_ERXD3 011010b: SDHI_D1 011011b: QMI/QIO1 011110b: GTETRGD	Pin function select bits 000000b: Hi-Z 001011b: RTS10#/ CTS10#/SS10# 011010b: SDHI_D1 011011b: QMI/QIO1 011110b: GTETRGD

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 7)
PM4PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 010001b: ET0_ETXD2 011010b: SDHI_D2 011011b: QIO2-A 011110b: GTADSM0 100110b: CAT0_ETXD2	Pin function select bits 000000b: Hi-Z 010001b: ET0_ETXD2 011010b: SDHI_D2 011011b: QIO2-A 011110b: GTADSM0	Pin function select bits 000000b: Hi-Z 010001b: ET0_ETXD2 011010b: SDHI_D2 011011b: QIO2-A 011110b: GTADSM0
PM5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 010001b: ET0_ETXD3 011010b: SDHI_D3 011011b: QIO3-A 011110b: GTADSM1 100110b: CAT0_ETXD3	Pin function select bits 000000b: Hi-Z 010001b: ET0_ETXD3 011010b: SDHI_D3 011011b: QIO3-A 011110b: GTADSM1	Pin function select bits 000000b: Hi-Z 010001b: ET0_ETXD3 011010b: SDHI_D3 011011b: QIO3-A 011110b: GTADSM1
PM6PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 010001b: ET0_TX_CLK 011010b: SDHI_CD 011110b: GTIOC3A 100110b: CAT0_TX_CLK	Pin function select bits 000000b: Hi-Z 010001b: ET0_TX_CLK 011010b: SDHI_CD 011110b: GTIOC3A	Pin function select bits 000000b: Hi-Z 010001b: ET0_TX_CLK 011010b: SDHI_CD 011110b: GTIOC3A
PM7PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 010001b: ET0_CRS 010010b: RMII0_CRS_DV 011010b: SDHI_WP 011110b: GTIOC3B 100110b: CAT0_RX_DV	Pin function select bits 000000b: Hi-Z 010001b: ET0_CRS 010010b: RMII0_CRS_DV 011010b: SDHI_WP 011110b: GTIOC3B	Pin function select bits 000000b: Hi-Z 010001b: ET0_CRS 010010b: RMII0_CRS_DV 011010b: SDHI_WP 011110b: GTIOC3B

Table 2.36 Comparison of PNn Pin Function Control Register (PNnPFS)

Register	Bit	RX72M/RX72N (n = 0 to 5)	RX66N (n = 4, 5)
PN0PFS	PSEL[5:0]	Pin function select bits	—
PN1PFS	PSEL[5:0]	Pin function select bits	—
PN2PFS	PSEL[5:0]	Pin function select bits	—
PN3PFS	PSEL[5:0]	Pin function select bits	—
PN4PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 010100b: ET1_MDIO 011011b: QSPCLK-C 101000b: PMGI1_MDIO	Pin function select bits 000000b: Hi-Z 011011b: QSPCLK-C
PN5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 010100b: ET1_MDC 011011b: QSSL-C 101000b: PMGI1_MDC	Pin function select bits 000000b: Hi-Z 011011b: QSSL-C

Table 2.37 Comparison of PQn Pin Function Control Register (PQnPFS)

Register	Bit	RX72M (n = 0 to 7)	RX72N (n = 0 to 7)	RX66N (n = 0 to 3)
PQ0PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001010b: SCK11 010100b: ET1_CRS 010101b: RMII1_CRS_DV 100110b: CAT1_RX_DV	Pin function select bits 000000b: Hi-Z 001010b: SCK11 010100b: ET1_CRS 010101b: RMII1_CRS_DV	Pin function select bits 000000b: Hi-Z 001010b: SCK11
PQ1PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001010b: SMISO11/SSCL11/RXD11 010100b: ET1_COL	Pin function select bits 000000b: Hi-Z 001010b: SMISO11/SSCL11/RXD11 010100b: ET1_COL	Pin function select bits 000000b: Hi-Z 001010b: SMISO11/SSCL11/RXD11
PQ2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001010b: SMOSI11/SSDA11/TXD11 010100b: ET1_RX_DV 100110b: CAT1_RX_DV	Pin function select bits 000000b: Hi-Z 001010b: SMOSI11/SSDA11/TXD11 010100b: ET1_RX_DV	Pin function select bits 000000b: Hi-Z 001010b: SMOSI11/SSDA11/TXD11
PQ3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001011b: RTS11#/CTS11#/SS11# 010100b: ET1_TX_ER	Pin function select bits 000000b: Hi-Z 001011b: RTS11#/CTS11#/SS11# 010100b: ET1_TX_ER	Pin function select bits 000000b: Hi-Z 001011b: RTS11#/CTS11#/SS11#
PQ4PFS	PSEL[5:0]	Pin function select bits	Pin function select bits	—
PQ5PFS	PSEL[5:0]	Pin function select bits	Pin function select bits	—
PQ6PFS	PSEL[5:0]	Pin function select bits	Pin function select bits	—
PQ7PFS	PSEL[5:0]	Pin function select bits	Pin function select bits	—

Table 2.38 Comparison of Multi-Function Pin Controller Registers

Register	Bit	RX72M (MPC)	RX72N (MPC)	RX66N (MPC)
PFENET	PHYMODE1	Ethernet channel 1 mode set bit	Ethernet channel 1 mode set bit	—

2.9 Ethernet Controller

Table 2.39 is a comparative overview of the Ethernet controllers.

Table 2.39 Comparative Overview of Ethernet Controllers

Item	RX72M (ETHERC)/RX72N (ETHERC)	RX66N (ETHERC)
Channels	2 channels	1 channel
Protocol	Flow control compliant with IEEE 802.3x	Flow control compliant with IEEE 802.3x
Data transmission and reception	Transmission and reception of frames compliant with Ethernet/IEEE 802.3 standard	Transmission and reception of frames compliant with Ethernet/IEEE 802.3 standard
Bit rate	10 Mbps and 100 Mbps	10 Mbps and 100 Mbps
Operation modes	Full-duplex and half-duplex	Full-duplex and half-duplex
Interfaces	Media Independent Interface (MII) and Reduced Media Independent Interface (RMII) compliant with IEEE 802.3u standard	Media Independent Interface (MII) and Reduced Media Independent Interface (RMII) compliant with IEEE 802.3u standard
Functions	Magic Packet™*1 detection, Wake-On-LAN (WOL) signal output	Magic Packet™*1 detection, Wake-On-LAN (WOL) signal output

Note: 1. Magic Packet is a trademark of Advanced Micro Devices, Inc.

2.10 DMA Controller for the Ethernet Controller

Table 2.40 is a comparative overview of the DMA controller for the Ethernet controller, and Table 2.41 is a comparison of DMA controller for the Ethernet controller registers.

Table 2.40 Comparative Overview of DMA Controller for the Ethernet Controller

Item	RX72M (EDMACa)/RX72N (EDMACa)	RX66N (EDMACa)
Channels	ETHERC: 2 channels EPTPC: 1 channel	ETHERC: 1 channel
Data transmission and reception	• Control of data transmission and reception by means of descriptors • Support for single-buffer frame transmission and reception (one buffer per frame) and multi-buffer frame transmission and reception (multiple buffers per frame)	• Control of data transmission and reception by means of descriptors • Support for single-buffer frame transmission and reception (one buffer per frame) and multi-buffer frame transmission and reception (multiple buffers per frame)
Functions	• Minimizing of system bus occupation time using block transfer (32-byte units) • Writeback of transmit and receive frame status to descriptors • Insertion of padding in receive data	• Minimizing of system bus occupation time using block transfer (32-byte units) • Writeback of transmit and receive frame status to descriptors • Insertion of padding in receive data
Low power consumption function	Ability to reduce power consumption by transitioning to the module-stop state	Ability to reduce power consumption by transitioning to the module-stop state

Table 2.41 Comparison of DMA Controller for the Ethernet Controller Registers

Register	Bit	RX72M (EDMACa)/ RX72N (EDMACa)	RX66N (EDMACa)
PTPEDMAC.EESR	—	PTP/EDMAC status register	—
PTPEDMAC.EESIPR	—	PTP/EDMAC status interrupt enable register	—
FDR	RFD[4:0]	Receive FIFO depth bits b4 b0 01111: 4,096 bytes Settings other than the above are prohibited.	Receive FIFO depth bits b4 b0 00111: 1,968 bytes Settings other than the above are prohibited.
FCFTR	RFDO[2:0]	Receive FIFO data PAUSE output threshold bits b2 b0 0 0 0: When 224 (256 − 32) bytes of data is stored in the receive FIFO. 0 0 1: When 480 (512 − 32) bytes of data is stored in the receive FIFO. : 1 1 0: When 1,760 (1,792 − 32) bytes of data is stored in the receive FIFO. 1 1 1: When 2,016 (2,048 − 32) bytes of data is stored in the receive FIFO.	Receive FIFO data PAUSE output threshold bits b2 b0 0 0 0: When 224 (256 − 32) bytes of data is stored in the receive FIFO. 0 0 1: When 480 (512 − 32) bytes of data is stored in the receive FIFO. : 1 1 0: When 1,760 (1,792 − 32) bytes of data is stored in the receive FIFO. 1 1 1: When 1,952 (2,048 − 96) bytes of data is stored in the receive FIFO.

2.11 PHY Management Interface

Table 2.42 is a comparative overview of the PHY management interface.

Table 2.42 Comparative Overview of PHY Management Interface

Item	RX72M (PMGI)/RX72N (PMGI)	RX66N (PMGI)
Number of channels	2 channels	1 channel
Communication format	MII Management Interface compliant with IEEE 802.3	MII Management Interface compliant with IEEE 802.3
I/O pins	MDC (clock output) and MDIO (data input and output)	MDC (clock output) and MDIO (data input and output)
Transfer rate	MDC is generated by frequency division of PCLKA. The range of division ratios is from 1/4 to 1/128.	MDC is generated by frequency division of PCLKA. The range of division ratios is from 1/4 to 1/128.
PHY register addressing	5-bit address format	5-bit address format
PHY device addressing	5-bit address format	5-bit address format
Preamble inclusion/ non-inclusion	Ability to select between preamble inclusion or non-inclusion	Ability to select between preamble inclusion or non-inclusion
MDIO output delay function	Ability to adjust timing of output on MDIO pins	Ability to adjust timing of output on MDIO pins
Adjustment of MDIO input capture timing	Ability to adjust timing of MDIO input capture	Ability to adjust timing of MDIO input capture
Interrupt sources	Write data transmit end, read data receive end	Write data transmit end, read data receive end

2.12 RAM

Table 2.43 is a comparative overview of RAM.

Table 2.43 Comparative Overview of RAM

Item		RX72M/RX72N	RX66N
RAM	Capacity	512 KB	512 KB
	Address	0000 0000h to 0007 FFFFh	0000 0000h to 0007 FFFFh
	Memory bus	Memory bus 1	Memory bus 1
	Access	• RAM can be enabled or disabled. • Access takes one cycle for both reading and writing.	• RAM can be enabled or disabled. • Access takes one cycle for both reading and writing.
	Data retention function	Not available in deep software standby mode	Not available in deep software standby mode
	Low power consumption function	Ability to transition RAM, expansion RAM, and ECCRAM to the module stop state independently	Ability to transition RAM, expansion RAM, and ECCRAM to the module stop state independently
	Error checking	• Parity checking: 1-bit error detection • When an error is found, a non-maskable interrupt or an interrupt is generated.	• Parity checking: 1-bit error detection • When an error is found, a non-maskable interrupt or an interrupt is generated.
Expansion RAM	Capacity	512 KB	512 KB
	Address	0080 0000h to 0087 FFFFh	0080 0000h to 0087 FFFFh
	Memory bus	Memory bus 3	Memory bus 3
	Access	• Ability to enable or disable expansion RAM [When MEMWAIT = 0] • Access takes one cycle for both reading and writing. [When MEMWAIT = 1] • Access takes two cycles for both reading and writing.	• Ability to enable or disable expansion RAM • Access takes one cycle for both reading and writing.
	Data retention function	Not available in deep software standby mode	Not available in deep software standby mode
	Low power consumption function	Ability to transition RAM, expansion RAM, and ECCRAM to the module stop state independently	Ability to transition RAM, expansion RAM, and ECCRAM to the module stop state independently
	Error checking	• Parity checking: 1-bit error detection • When an error is found, a non-maskable interrupt or an interrupt is generated.	• Parity checking: 1-bit error detection • When an error is found, a non-maskable interrupt or an interrupt is generated.

Item		RX72M/RX72N	RX66N
ECCRAM	Capacity	32 KB	32 KB
	Address	00FF 8000h to 00FF FFFFh	00FF 8000h to 00FF FFFFh
	Memory bus	Memory bus 3	Memory bus 3
	Access	Ability to enable or disable ECCRAM [When MEMWAIT = 0] • When ECC function is disabled Access takes two cycles for both reading and writing. • When ECC function is enabled (when no error has occurred) Access takes two cycles for both reading and writing. • When ECC function is enabled (when an error has occurred) Access takes three cycles for both reading and writing. [When MEMWAIT = 1] • When ECC function is disabled Access takes three cycles for both reading and writing. • When ECC function is enabled (when no error has occurred) Access takes three cycles for reading and four cycles for writing. • When ECC function is enabled (when an error has occurred) Access takes five cycles for both reading and writing.	Ability to enable or disable ECCRAM • When ECC function is disabled Access takes two cycles for both reading and writing. • When ECC function is enabled (when no error has occurred) Access takes two cycles for both reading and writing. • When ECC function is enabled (when an error has occurred) Access takes three cycles for both reading and writing.
	Data retention function	Not available in deep software standby mode	Not available in deep software standby mode
	Low power consumption function	Ability to transition RAM, expansion RAM, and ECCRAM to the module stop state independently	Ability to transition RAM, expansion RAM, and ECCRAM to the module stop state independently
	Error checking	• ECC error correction 1-bit error correction and 2-bit error detection • When an error is found, a non-maskable interrupt or an interrupt is generated.	• ECC error correction 1-bit error correction and 2-bit error detection • When an error is found, a non-maskable interrupt or an interrupt is generated.

2.13 Flash Memory

Table 2.44 is a comparative overview of flash memory.

Table 2.44 Comparative Overview of Flash Memory

Item		RX72M (FLASH)/RX72N (FLASH)	RX66N (FLASH)
Both code flash memory and data flash memory	Programming/ erasing method	• Programming and erasing of code flash memory and data flash memory, and programming of option-setting memory, by FACI commands specified in FACI command issuing area (007E 0000h) (self-programming) • Programming and erasing through transfer by serial programmer via serial interface (serial programming)	• Programming and erasing of code flash memory and data flash memory, and programming of option-setting memory, by FACI commands specified in FACI command issuing area (007E 0000h) (self-programming) • Programming and erasing through transfer by serial programmer via serial interface (serial programming)
	Security function	Protection against illicit tampering or reading of data in flash memory	Protection against illicit tampering or reading of data in flash memory
	Protection function	Protection against erroneous overwriting of flash memory	Protection against erroneous overwriting of flash memory
	Background operation (BGO) function	• The code flash memory can be read while the code flash memory is being programmed or erased. • The data flash memory can be read while the code flash memory is being programmed or erased. • The code flash memory can be read while the data flash memory is being programmed or erased.	• The code flash memory can be read while the code flash memory is being programmed or erased. • The data flash memory can be read while the code flash memory is being programmed or erased. • The code flash memory can be read while the data flash memory is being programmed or erased.
	Other functions	• Interrupts can be accepted during self-programming. • Option-setting memory can be specified in the initial settings of the MCU	• Interrupts can be accepted during self-programming. • Option-setting memory can be specified in the initial settings of the MCU
	On-board programming (serial programming and self-programming)	• Programming/erasure in boot mode (SCI interface) — The asynchronous serial interface (SCI1) is used. — The transfer rate is adjusted automatically. • Programming/erasure in boot mode (USB interface) — USB is used. — Dedicated hardware is not required, so direct connection to a PC is possible. • Programming/erasure in boot mode (FINE interface) — FINE is used.	• Programming/erasure in boot mode (SCI interface) — The asynchronous serial interface (SCI1) is used. — The transfer rate is adjusted automatically. • Programming/erasure in boot mode (USB interface) — USB is used. — Dedicated hardware is not required, so direct connection to a PC is possible. • Programming/erasure in boot mode (FINE interface) — FINE is used.

Item		RX72M (FLASH)/RX72N (FLASH)	RX66N (FLASH)
Both code flash memory and data flash memory	On-board programming (serial programming and self-programming)	• Programming/erasure by self-programming — Allows programming/erasure of flash memory without resetting the system.	• Programming/erasure by self-programming — Allows programming/erasure of flash memory without resetting the system.
	Unique ID	A 16-byte unique ID code provided for each MCU.	A 16-byte unique ID code provided for each MCU.
Code flash memory	Memory capacity	User area: Up to 4 MB	User area: Up to 4 MB
	Address	• When capacity is 4 MB FFC0 0000h to FFFF FFFFh • When capacity is 2 MB FFE0 0000h to FFFF FFFFh	• When capacity is 4 MB FFC0 0000h to FFFF FFFFh • When capacity is 2 MB FFE0 0000h to FFFF FFFFh
	ROM cache	• Capacity: 8 KB • Mapping method: direct mapping • Line size: 16 bytes	• Capacity: 8 KB • Mapping method: direct mapping • Line size: 16 bytes
	Read cycle	• While ROM cache operation is enabled: — When the cache is hit: One cycle — when the cache is missed: One to two cycles if ICLK ≤ 120 MHz Two to three cycles if ICLK > 120 MHz • When ROM cache operation is disabled: One cycle if ICLK ≤ 120 MHz Two cycles if ICLK > 120 MHz	• While ROM cache operation is enabled: — When the cache is hit: One cycle — when the cache is missed: One to two cycles • When ROM cache operation is disabled: One cycle
	Value after erasure	FFh	FFh
	Dual bank function	The dual-bank configuration enables safe updating in cases where programming is suspended. • Linear mode: the code flash memory is used as one area. • Dual mode: the code flash memory is divided into two areas.	The dual-bank configuration enables safe updating in cases where programming is suspended. • Linear mode: the code flash memory is used as one area. • Dual mode: the code flash memory is divided into two areas.
	Trusted memory (TM) function	Protects against unauthorized reading of the code flash memory. • Linear mode: blocks 8 and 9 • Dual mode: blocks 8, 9, 78, and 79	Protects against unauthorized reading of the code flash memory. • Linear mode: blocks 8 and 9 • Dual mode: blocks 8, 9, 78, and 79
	Units of programming and erasure	• Unit of programming for the user area: 128 bytes • Unit of erasure for the user area: Block	• Unit of programming for the user area: 128 bytes • Unit of erasure for the user area: Block
	Off-board programming	Programming or erasure of the code flash memory or option-setting memory are possible by using a parallel programmer.	Programming or erasure of the code flash memory or option-setting memory are possible by using a parallel programmer.

Item		RX72M (FLASH)/RX72N (FLASH)	RX66N (FLASH)
Data flash memory	Memory capacity	Data area: 32 KB	Data area: 32 KB
	Address	0010 0000h to 0010 7FFFh	0010 0000h to 0010 7FFFh
	Read cycle	Reading proceeds in every cycle of FCLK.	Reading proceeds in every cycle of FCLK.
	Value after erasure	Undefined	Undefined
	Units of programming and erasure	• Unit of programming for data area: 4 bytes • Unit of erasure for data area: 64, 128, or 256 bytes	• Unit of programming for data area: 4 bytes • Unit of erasure for data area: 64, 128, or 256 bytes
	Off-board programming	Programming or erasure of the data flash memory by using a parallel programmer is not possible.	Programming or erasure of the data flash memory by using a parallel programmer is not possible.

2.14 Packages

As indicated in Table 2.45, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage.

Table 2.45 Packages

Package Type	Renesas Code		
	RX72M	RX72N	RX66N
145-pin TFLGA	×	○	○

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by **blue text**. Items that exists on both groups with different specifications are indicated by **red text**. **Black text** indicates there is no differences in the item's specifications between groups.

3.1 224-Pin LFBGA Package

Table 3.1 is a comparative listing of the pin functions of 224-pin LFBGA package products.

Table 3.1 Comparative Listing of 224-Pin LFBGA Package Pin Functions

224-Pin LFBGA	RX72M	RX72N	RX66N
A1	NC	NC	NC
A2	VREFH0	VREFH0	VREFH0
A3	VREFL0	VREFL0	VREFL0
A4	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
A5	P92/D18/A18/POE4#/RXD7/ SMISO7/SSCL7/ET1_CRS/ RMII1_CRS_DV/ CAT1_RX_DV/AN116/ DSMCLK4	P92/D18/A18/POE4#/RXD7/ SMISO7/SSCL7/ET1_CRS/ RMII1_CRS_DV/AN116	P92/D18/A18/POE4#/RXD7/ SMISO7/SSCL7/AN116
A6	PD0/D0[A0/D0]/POE4#/ GTIOC1B/LCD_EXTCLK-B/ IRQ0/AN108	PD0/D0[A0/D0]/POE4#/ GTIOC1B/LCD_EXTCLK-B/ IRQ0/AN108	PD0/D0[A0/D0]/POE4#/ GTIOC1B/LCD_EXTCLK-B/ IRQ0/AN108
A7	PD2/D2[A2/D2]/MTIOC4D/ TIC2/GTIOC0B/MISOC-A/ CRX0/ET1_EXOUT/QIO2-B/ SDHI_D2-B/MMC_D2-B/ LCD_DATA22-B/IRQ2/AN110	PD2/D2[A2/D2]/MTIOC4D/ TIC2/GTIOC0B/MISOC-A/ CRX0/ET1_EXOUT/QIO2-B/ SDHI_D2-B/MMC_D2-B/ LCD_DATA22-B/IRQ2/AN110	PD2/D2[A2/D2]/MTIOC4D/ TIC2/GTIOC0B/MISOC-A/ CRX0/QIO2-B/SDHI_D2-B/ MMC_D2-B/LCD_DATA22-B/ IRQ2/AN110
A8	TRDATA5/P96/D22/A22/ ET1_ERXD2/CAT1_ERXD2	TRDATA5/P96/D22/A22/ ET1_ERXD2	TRDATA5/P96/D22/A22
A9	PD3/D3[A3/D3]/MTIOC8D/ TOC2/POE8#/GTIOC0A/ RSPCKC-A/ET1_WOL/ QIO3-B/SDHI_D3-B/ MMC_D3-B/LCD_DATA21-B/ IRQ3/AN111	PD3/D3[A3/D3]/MTIOC8D/ TOC2/POE8#/GTIOC0A/ RSPCKC-A/ET1_WOL/ QIO3-B/SDHI_D3-B/ MMC_D3-B/LCD_DATA21-B/ IRQ3/AN111	PD3/D3[A3/D3]/MTIOC8D/ TOC2/POE8#/GTIOC0A/ RSPCKC-A/QIO3-B/ SDHI_D3-B/MMC_D3-B/ LCD_DATA21-B/IRQ3/AN111
A10	TRDATA6/PG0/D24/ ET1_RX_CLK/REF50CK1/ CAT1_RX_CLK	TRDATA6/PG0/D24/ ET1_RX_CLK/REF50CK1	TRDATA6/PG0/D24
A11	PD7/D7[A7/D7]/MTIC5U/ POE0#/SSLC3-A/ ET1_RX_ER/RMII1_RX_ER/ CAT1_RX_ER/QMI-B/ QIO1-B/SDHI_D1-B/ MMC_D1-B/LCD_DATA17-B/ IRQ7/AN107	PD7/D7[A7/D7]/MTIC5U/ POE0#/SSLC3-A/ ET1_RX_ER/RMII1_RX_ER/ QMI-B/QIO1-B/SDHI_D1-B/ MMC_D1-B/LCD_DATA17-B/ IRQ7/AN107	PD7/D7[A7/D7]/MTIC5U/ POE0#/SSLC3-A/QMI-B/ QIO1-B/SDHI_D1-B/ MMC_D1-B/LCD_DATA17-B/ IRQ7/AN107
A12	P61/SDCS#/D0[A0/D0]/ CS1#/ET1_ERXD1/ RMII1_RXD1/CAT1_ERXD1	P61/SDCS#/D0[A0/D0]/ CS1#/ET1_ERXD1/ RMII1_RXD1	P61/SDCS#/D0[A0/D0]/CS1#
A13	P62/RAS#/D1[A1/D1]/CS2#/ ET1_ERXD0/RMII1_RXD0/ CAT1_ERXD0	P62/RAS#/D1[A1/D1]/CS2#/ ET1_ERXD0/RMII1_RXD0	P62/RAS#/D1[A1/D1]/CS2#

224-Pin LFBGA	RX72M	RX72N	RX66N
A14	PE1/D9[A9/D9]/D1[A1/D1]/ MTIOC4C/MTIOC3B/PO18/ GTIOC1B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/ SSLB2-B/MMC_D5-B/ LCD_DATA15-B/ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/ MTIOC4C/MTIOC3B/PO18/ GTIOC1B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/ SSLB2-B/MMC_D5-B/ LCD_DATA15-B/ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/ MTIOC4C/MTIOC3B/PO18/ GTIOC1B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/ SSLB2-B/MMC_D5-B/ LCD_DATA15-B/ANEX1
A15	P70/SDCLK/CATLINKACT0	P70/SDCLK	P70/SDCLK
B1	AVSS0	AVSS0	AVSS0
B2	AVCC0	AVCC0	AVCC0
B3	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
B4	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
B5	P91/D17/A17/SCK7/ ET1_COL/AN115/DSMDAT5	P91/D17/A17/SCK7/ ET1_COL/AN115	P91/D17/A17/SCK7/AN115
B6	VCC	VCC	VCC
B7	P94/D20/A20/ET1_ERXD0/ RMII1_RXD0/CAT1_ERXD0	P94/D20/A20/ET1_ERXD0/ RMII1_RXD0	P94/D20/A20
B8	TRDATA4/P95/D21/A21/ ET1_ERXD1/RMII1_RXD1/ CAT1_ERXD1	TRDATA4/P95/D21/A21/ ET1_ERXD1/RMII1_RXD1	TRDATA4/P95/D21/A21
B9	PD4/D4[A4/D4]/MTIOC8B/ POE11#/SSLC0-A/ ET1_MDIO/PMGI1_MDIO/ QSSL-B/SDHI_CMD-B/ MMC_CMD-B/ LCD_DATA20-B/IRQ4/AN112	PD4/D4[A4/D4]/MTIOC8B/ POE11#/SSLC0-A/ ET1_MDIO/PMGI1_MDIO/ QSSL-B/SDHI_CMD-B/ MMC_CMD-B/ LCD_DATA20-B/IRQ4/AN112	PD4/D4[A4/D4]/MTIOC8B/ POE11#/SSLC0-A/QSSL-B/ SDHI_CMD-B/MMC_CMD-B/ LCD_DATA20-B/IRQ4/AN112
B10	PD6/D6[A6/D6]/MTIC5V/MTI OC8A/POE4#/SSLC2-A/ ET1_RX_CLK/REF50CK1/ CAT1_RX_CLK/QMO-B/ QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/ IRQ6/AN106	PD6/D6[A6/D6]/MTIC5V/MTI OC8A/POE4#/SSLC2-A/ ET1_RX_CLK/REF50CK1/ QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/ IRQ6/AN106	PD6/D6[A6/D6]/MTIC5V/ MTIOC8A/POE4#/SSLC2-A/ QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/ IRQ6/AN106
B11	VCC	VCC	VCC
B12	P63/CAS#/D2[A2/D2]/CS3#/ ET1_ETXD1/RMII1_TXD1/ CAT1_ETXD1	P63/CAS#/D2[A2/D2]/CS3#/ ET1_ETXD1/RMII1_TXD1	P63/CAS#/D2[A2/D2]/CS3#
B13	PE2/D10[A10/D10]/ D2[A2/D2]/MTIOC4A/PO23/ TIC3/GTIOC0B/RXD12/ SMISO12/SSCL12/RXDX12/ SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/ AN100	PE2/D10[A10/D10]/ D2[A2/D2]/MTIOC4A/PO23/ TIC3/GTIOC0B/RXD12/ SMISO12/SSCL12/RXDX12/ SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/ AN100	PE2/D10[A10/D10]/ D2[A2/D2]/MTIOC4A/PO23/ TIC3/GTIOC0B/RXD12/ SMISO12/SSCL12/RXDX12/ SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/ AN100
B14	PE4/D12[A12/D12]/ D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/ SSLB0-B/ET0_ERXD2/ CAT0_ERXD2/ LCD_DATA12-B/AN102	PE4/D12[A12/D12]/ D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/ SSLB0-B/ET0_ERXD2/ LCD_DATA12-B/AN102	PE4/D12[A12/D12]/ D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/ SSLB0-B/ET0_ERXD2/ LCD_DATA12-B/AN102
B15	PE7/D15[A15/D15]/ D7[A7/D7]/MTIOC6A/TOC1/ GTIOC3A/MISOB-B/ SDHI_WP/MMC_RES#-B/ LCD_DATA9-B/IRQ7/AN105	PE7/D15[A15/D15]/ D7[A7/D7]/MTIOC6A/TOC1/ GTIOC3A/MISOB-B/ SDHI_WP/MMC_RES#-B/ LCD_DATA9-B/IRQ7/AN105	PE7/D15[A15/D15]/ D7[A7/D7]/MTIOC6A/TOC1/ GTIOC3A/MISOB-B/ SDHI_WP/MMC_RES#-B/ LCD_DATA9-B/IRQ7/AN105

224-Pin LFBGA	RX72M	RX72N	RX66N
C1	AVSS1	AVSS1	AVSS1
C2	AVCC1	AVCC1	AVCC1
C3	P05/SSILRCK1/IRQ13/DA1	P05/SSILRCK1/IRQ13/DA1	P05/SSILRCK1/IRQ13/DA1
C4	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
C5	VSS	VSS	VSS
C6	P90/D16/A16/TXD7/SMOSI7/ SSDA7/ET1_RX_DV/ CAT1_RX_DV/AN114/ DSMCLK5	P90/D16/A16/TXD7/SMOSI7/ SSDA7/ET1_RX_DV/AN114	P90/D16/A16/TXD7/SMOSI7/ SSDA7/AN114
C7	PD1/D1[A1/D1]/MTIOC4B/ POE0#/GTIOC1A/MOSIC-A/ CTX0/LCD_DATA23-B/IRQ1/ AN109	PD1/D1[A1/D1]/MTIOC4B/ POE0#/GTIOC1A/MOSIC-A/ CTX0/LCD_DATA23-B/IRQ1/ AN109	PD1/D1[A1/D1]/MTIOC4B/ POE0#/GTIOC1A/MOSIC-A/ CTX0/LCD_DATA23-B/IRQ1/ AN109
C8	VCC	VCC	VCC
C9	TRSYNC1/P97/D23/A23/ ET1_ERXD3/CAT1_ERXD3	TRSYNC1/P97/D23/A23/ ET1_ERXD3	TRSYNC1/P97/D23/A23
C10	P60/CS0#/ET1_TX_EN/ RMII1_TXD_EN/ CAT1_TX_EN	P60/CS0#/ET1_TX_EN/ RMII1_TXD_EN	P60/CS0#
C11	P64/WE#/D3[A3/D3]/CS4#/ ET1_ETXD0/RMII1_TXD0/ CAT1_ETXD0	P64/WE#/D3[A3/D3]/CS4#/ ET1_ETXD0/RMII1_TXD0	P64/WE#/D3[A3/D3]/CS4#
C12	VSS	VSS	VSS
C13	PE5/D13[A13/D13]/ D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/ RSPCKB-B/ET0_RX_CLK/ REF50CK0/CAT0_RX_CLK/ LCD_DATA11-B/IRQ5/AN103	PE5/D13[A13/D13]/ D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/ RSPCKB-B/ET0_RX_CLK/ REF50CK0/LCD_DATA11-B/ IRQ5/AN103	PE5/D13[A13/D13]/ D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/ RSPCKB-B/ET0_RX_CLK/ REF50CK0/LCD_DATA11-B/ IRQ5/AN103
C14	P65/CKE/CS5#	P65/CKE/CS5#	P65/CKE/CS5#
C15	P66/DQM0/CS6#/MTIOC7D/ GTIOC2B/CTX2	P66/DQM0/CS6#/MTIOC7D/ GTIOC2B/CTX2	P66/DQM0/CS6#/MTIOC7D/ GTIOC2B/CTX2
D1	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
D2	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
D3	P03/SSIDATA1/IRQ11/DA0	P03/SSIDATA1/IRQ11/DA0	P03/SSIDATA1/IRQ11/DA0
D4	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
D5	P01/TMCI0/RXD6/SMISO6/ SSCL6/SSIBCK0/ CATLEDERR/QIO3-C/IRQ9/ AN119	P01/TMCI0/RXD6/SMISO6/ SSCL6/SSIBCK0/QIO3-C/ IRQ9/AN119	P01/TMCI0/RXD6/SMISO6/ SSCL6/SSIBCK0/QIO3-C/ IRQ9/AN119
D6	P02/TMCI1/SCK6/SSIBCK1/ CATLEDSTER/IRQ10/AN120	P02/TMCI1/SCK6/SSIBCK1/ IRQ10/AN120	P02/TMCI1/SCK6/SSIBCK1/ IRQ10/AN120
D7	P93/D19/A19/POE0#/CTS7#/ RTS7#/SS7#/ET1_LINKSTA/ CAT1_LINKSTA/AN117/ DSMDAT4	P93/D19/A19/POE0#/CTS7#/ RTS7#/SS7#/ET1_LINKSTA/ AN117	P93/D19/A19/POE0#/CTS7#/ RTS7#/SS7#/AN117
D8	VSS	VSS	VSS
D9	PD5/D5[A5/D5]/MTIC5W/ MTIOC8C/MTCLKA/POE10#/ SSLC1-A/ET1_MDC/ PMGI1_MDC/QSPCLK-B/ SDHI_CLK-B/MMC_CLK-B/ LCD_DATA19-B/IRQ5/AN113	PD5/D5[A5/D5]/MTIC5W/ MTIOC8C/MTCLKA/POE10#/ SSLC1-A/ET1_MDC/ PMGI1_MDC/QSPCLK-B/ SDHI_CLK-B/MMC_CLK-B/ LCD_DATA19-B/IRQ5/AN113	PD5/D5[A5/D5]/MTIC5W/ MTIOC8C/MTCLKA/POE10#/ SSLC1-A/QSPCLK-B/ SDHI_CLK-B/MMC_CLK-B/ LCD_DATA19-B/IRQ5/AN113

224-Pin LFBGA	RX72M	RX72N	RX66N
D10	TRDATA7/PG1/D25/ ET1_RX_ER/RMII1_RX_ER/ CAT1_RX_ER	TRDATA7/PG1/D25/ ET1_RX_ER/RMII1_RX_ER	TRDATA7/PG1/D25
D11	PE0/D8[A8/D8]/D0[A0/D0]/ MTIOC3D/GTIOC2B/SCK12/ SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/ MTIOC3D/GTIOC2B/SCK12/ SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/ MTIOC3D/GTIOC2B/SCK12/ SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0
D12	PE3/D11[A11/D11]/ D3[A3/D3]/MTIOC4B/PO26/ TOC3/POE8#/GTIOC2A/ CTS12#/RTS12#/SS12#/ ET0_ERXD3/CAT0_ERXD3/ MMC_D7-B/LCD_DATA13-B/ AN101	PE3/D11[A11/D11]/ D3[A3/D3]/MTIOC4B/PO26/ TOC3/POE8#/GTIOC2A/ CTS12#/RTS12#/SS12#/ ET0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101	PE3/D11[A11/D11]/ D3[A3/D3]/MTIOC4B/PO26/ TOC3/POE8#/GTIOC2A/ CTS12#/RTS12#/SS12#/ ET0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101
D13	VSS	VSS	VSS
D14	TRDATA0/PG2/D26/ ET1_TX_CLK/ CAT1_TX_CLK	TRDATA0/PG2/D26/ ET1_TX_CLK	TRDATA0/PG2/D26
D15	P67/DQM1/CS7#/MTIOC7C/ GTIOC1B/CRX2/EPLSOUT1/ CATSYNC1/IRQ15	P67/DQM1/CS7#/MTIOC7C/ GTIOC1B/CRX2/EPLSOUT1/ IRQ15	P67/DQM1/CS7#/MTIOC7C/ GTIOC1B/CRX2/IRQ15
E1	VCL	VCL	VCL
E2	VSS	VSS	VSS
E3	P00/TMRI0/TXD6/SMOSI6/ SSDA6/AUDIO_CLK/ CATLATCH1/QIO2-C/IRQ8/ AN118	P00/TMRI0/TXD6/SMOSI6/ SSDA6/AUDIO_CLK/QIO2-C/ IRQ8/AN118	P00/TMRI0/TXD6/SMOSI6/ SSDA6/AUDIO_CLK/QIO2-C/ IRQ8/AN118
E4	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
E5	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
E6	PN0/ET1_ETXD2/ CAT1_ETXD2	PN0/ET1_ETXD2	PN0
E7	PQ0/SCK11/ET1_CRS/ RMII1_CRS_DV/ CAT1_RX_DV	PQ0/SCK11/ET1_CRS/ RMII1_CRS_DV	PQ0/SCK11
E8	PQ1/SMISO11/SSCL11/ RXD11/ET1_COL	PQ1/SMISO11/SSCL11/ RXD11/ET1_COL	PQ1/SMISO11/SSCL11/ RXD11
E9	PQ3/RTS11#/CTS11#/ SS11#/ET1_TX_ER	PQ3/RTS11#/CTS11#/ SS11#/ET1_TX_ER	PQ3/RTS11#/CTS11#/ SS11#
E10	PQ5/ET1_ETXD0/ RMII1_TXD0/CAT1_ETXD0	PQ5/ET1_ETXD0/ RMII1_TXD0	PQ5
E11	PQ4/ET1_RX_CLK/ REF50CK1/CAT1_RX_CLK	PQ4/ET1_RX_CLK/ REF50CK1	PQ4
E12	VCC	VCC	VCC
E13	PE6/D14[A14/D14]/ D6[A6/D6]/MTIOC6C/TIC1/ GTIOC3B/MOSIB-B/ SDHI_CD/MMC_CD-B/ LCD_DATA10-B/IRQ6/AN104	PE6/D14[A14/D14]/ D6[A6/D6]/MTIOC6C/TIC1/ GTIOC3B/MOSIB-B/ SDHI_CD/MMC_CD-B/ LCD_DATA10-B/IRQ6/AN104	PE6/D14[A14/D14]/ D6[A6/D6]/MTIOC6C/TIC1/ GTIOC3B/MOSIB-B/ SDHI_CD/MMC_CD-B/ LCD_DATA10-B/IRQ6/AN104
E14	TRCLK/PG5/D29/ ET1_ETXD2/CAT1_ETXD2	TRCLK/PG5/D29/ ET1_ETXD2	TRCLK/PG5/D29
E15	TRSYNC/PG4/D28/ ET1_ETXD1/RMII1_TXD1/ CAT1_ETXD1	TRSYNC/PG4/D28/ ET1_ETXD1/RMII1_TXD1	TRSYNC/PG4/D28

224-Pin LFBGA	RX72M	RX72N	RX66N
F1	XCIN	XCIN	XCIN
F2	VBATT	VBATT	VBATT
F3	TRST#/PF4	TRST#/PF4	TRST#/PF4
F4	PK4/GTADSM0/SSLB1/ ET0_ERXD2/CAT0_ERXD2	PK4/GTADSM0/SSLB1/ ET0_ERXD2	PK4/GTADSM0/SSLB1/ ET0_ERXD2
F5	PK5/GTADSM1/SSLB2/ ET0_ERXD3/CAT0_ERXD3	PK5/GTADSM1/SSLB2/ ET0_ERXD3	PK5/GTADSM1/SSLB2/ ET0_ERXD3
F6	EMLE	EMLE	EMLE
F7	PK6/GTIOC1A/SSLB3/ CATLINKACT0	PK6/GTIOC1A/SSLB3	PK6/GTIOC1A/SSLB3
F8	PN1/ET1_ETXD3/ CAT1_ETXD3	PN1/ET1_ETXD3	PN1
F9	PQ6/ET1_ETXD1/ RMII1_TXD1/CAT1_ETXD1	PQ6/ET1_ETXD1/ RMII1_TXD1	PQ6
F10	VSS	VSS	VSS
F11	PM1/TOC3/GTETRGB/ SMISO10/SSCL10/RXD10/ ET1_ERXD1/RMII1_RXD1/ CAT1_ERXD1/ SDHI_CMD-D/QSSL-A	PM1/TOC3/GTETRGB/ SMISO10/SSCL10/RXD10/ ET1_ERXD1/RMII1_RXD1/ SDHI_CMD-D/QSSL-A	PM1/TOC3/GTETRGB/ SMISO10/SSCL10/RXD10/ SDHI_CMD-D/QSSL-A
F12	PA0/DQM2/BC0#/A0/ MTIOC4A/MTIOC6D/ TIOCA0/PO16/CACREF/ GTIOC0B/SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN/ CAT0_TX_EN/CATLEDRUN/ LCD_DATA8-B	PA0/DQM2/BC0#/A0/ MTIOC4A/MTIOC6D/ TIOCA0/PO16/CACREF/ GTIOC0B/SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN/ LCD_DATA8-B	PA0/DQM2/BC0#/A0/ MTIOC4A/MTIOC6D/ TIOCA0/PO16/CACREF/ GTIOC0B/SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN/ LCD_DATA8-B
F13	TRDATA1/PG3/D27/ ET1_ETXD0/RMII1_TXD0/ CAT1_ETXD0	TRDATA1/PG3/D27/ ET1_ETXD0/RMII1_TXD0	TRDATA1/PG3/D27
F14	TRDATA2/PG6/D30/ ET1_ETXD3/CAT1_ETXD3	TRDATA2/PG6/D30/ ET1_ETXD3	TRDATA2/PG6/D30
F15	TRDATA3/PG7/D31/ ET1_TX_ER	TRDATA3/PG7/D31/ ET1_TX_ER	TRDATA3/PG7/D31
G1	XCOUT	XCOUT	XCOUT
G2	VSS	VSS	VSS
G3	VCC	VCC	VCC
G4	MD/FINED	MD/FINED	MD/FINED
G5	PJ5/POE8#/CTS2#/RTS2#/ SS2#/SSIRXD0/EPLSOUT0/ CATSYNC0/QMI-C/QIO1-C	PJ5/POE8#/CTS2#/RTS2#/ SS2#/SSIRXD0/EPLSOUT0/ QMI-C/QIO1-C	PJ5/POE8#/CTS2#/RTS2#/ SS2#/SSIRXD0/QMI-C/ QIO1-C
G6	PF5/WAIT#/SSILRCK0/ CATLATCH0/IRQ4	PF5/WAIT#/SSILRCK0/IRQ4	PF5/WAIT#/SSILRCK0/IRQ4
G7	RES#	RES#	RES#
G8	PQ2/SMOSI11/SSDA11/ TXD11/ET1_RX_DV/ CAT1_RX_DV	PQ2/SMOSI11/SSDA11/ TXD11/ET1_RX_DV	PQ2/SMOSI11/SSDA11/ TXD11
G9	PN2/ET1_TX_CLK/ CAT1_TX_CLK	PN2/ET1_TX_CLK	PN2
G10	VCC	VCC	VCC

224-Pin LFBGA	RX72M	RX72N	RX66N
G11	PM0/TIC3/GTETRGA/ SCK10/ET1_ERXD0/ RMII1_RXD0/CAT1_ERXD0/ SDHI_CLK-D/QSPCLK-A	PM0/TIC3/GTETRGA/ SCK10/ET1_ERXD0/ RMII1_RXD0/SDHI_CLK-D/ QSPCLK-A	PM0/TIC3/GTETRGA/ SCK10/SDHI_CLK-D/ QSPCLK-A
G12	PA1/DQM3/A1/MTIOC0B/ MTCLKC/MTIOC7B/TIOCB0/ PO17/GTIOC2A/SCK5/ SSLA2-B/ET0_WOL/ LCD_DATA7-B/IRQ11	PA1/DQM3/A1/MTIOC0B/ MTCLKC/MTIOC7B/TIOCB0/ PO17/GTIOC2A/SCK5/ SSLA2-B/ET0_WOL/ LCD_DATA7-B/IRQ11	PA1/DQM3/A1/MTIOC0B/ MTCLKC/MTIOC7B/TIOCB0/ PO17/GTIOC2A/SCK5/ SSLA2-B/ET0_WOL/ LCD_DATA7-B/IRQ11
G13	PA2/A2/MTIOC7A/PO18/ GTIOC1A/RXD5/SMISO5/ SSCL5/SSLA3-B/ CATLINKACT1/ LCD_DATA6-B	PA2/A2/MTIOC7A/PO18/ GTIOC1A/RXD5/SMISO5/ SSCL5/SSLA3-B/ LCD_DATA6-B	PA2/A2/MTIOC7A/PO18/ GTIOC1A/RXD5/SMISO5/ SSCL5/SSLA3-B/ LCD_DATA6-B
G14	PA3/A3/MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19/ RXD5/SMISO5/SSCL5/ ET0_MDIO/CAT0_MDIO/ PMGI0_MDIO/ LCD_DATA5-B/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19/ RXD5/SMISO5/SSCL5/ ET0_MDIO/PMGI0_MDIO/ LCD_DATA5-B/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19/ RXD5/SMISO5/SSCL5/ ET0_MDIO/PMGI0_MDIO/ LCD_DATA5-B/IRQ6-DS
G15	PA4/A4/MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20/TXD5/ SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/CAT0_MDC/ CATIRQ/PMGI0_MDC/ LCD_DATA4-B/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20/TXD5/ SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/PMGI0_MDC/ LCD_DATA4-B/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20/TXD5/ SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/PMGI0_MDC/ LCD_DATA4-B/IRQ5-DS
H1	XTAL/P37	XTAL/P37	XTAL/P37
H2	P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/ ET0_LINKSTA/ CAT0_LINKSTA/IRQ4/ DSMDAT0	P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/ ET0_LINKSTA/IRQ4	P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/ ET0_LINKSTA/IRQ4
H3	UPSEL/P35/NMI	UPSEL/P35/NMI	UPSEL/P35/NMI
H4	P33/EDREQ1/MTIOC0D/ TIOCD0/TMRI3/PO11/ POE4#/POE11#/RXD6/ SMISO6/SSCL6/RXD0/ SMISO0/SSCL0/CRX0/ PCKO/IRQ3-DS/DSMCLK0	P33/EDREQ1/MTIOC0D/ TIOCD0/TMRI3/PO11/ POE4#/POE11#/RXD6/ SMISO6/SSCL6/RXD0/ SMISO0/SSCL0/CRX0/ PCKO/IRQ3-DS	P33/EDREQ1/MTIOC0D/ TIOCD0/TMRI3/PO11/ POE4#/POE11#/RXD6/ SMISO6/SSCL6/RXD0/ SMISO0/SSCL0/CRX0/ PCKO/IRQ3-DS
H5	P32/MTIOC0C/TIOCC0/ TMO3/PO10/RTCIC2/ RTCOUT/POE0#/POE10#/ TXD6/SMOSI6/SSDA6/ TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/ VSYNC/IRQ2-DS	P32/MTIOC0C/TIOCC0/ TMO3/PO10/RTCIC2/ RTCOUT/POE0#/POE10#/ TXD6/SMOSI6/SSDA6/ TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/ VSYNC/IRQ2-DS	P32/MTIOC0C/TIOCC0/ TMO3/PO10/RTCIC2/ RTCOUT/POE0#/POE10#/ TXD6/SMOSI6/SSDA6/ TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/ VSYNC/IRQ2-DS
H6	BSCANP	BSCANP	BSCANP
H7	PJ3/EDACK1/MTIOC3C/ CTS6#/RTS6#/SS6#/CTS0#/ RTS0#/SS0#/SSITXD0/ ET0_EXOUT/CATRESTOUT/ QMO-C/QIO0-C	PJ3/EDACK1/MTIOC3C/ CTS6#/RTS6#/SS6#/CTS0#/ RTS0#/SS0#/SSITXD0/ ET0_EXOUT/QMO-C/QIO0-C	PJ3/EDACK1/MTIOC3C/ CTS6#/RTS6#/SS6#/CTS0#/ RTS0#/SS0#/SSITXD0/ ET0_EXOUT/QMO-C/QIO0-C

224-Pin LFBGA	RX72M	RX72N	RX66N
H8	PQ7/ET1_TX_EN/ RMII1_TXD_EN/ CAT1_TX_EN	PQ7/ET1_TX_EN/ RMII1_TXD_EN	PQ7
H9	PN3/ET1_RX_ER/ RMII1_RX_ER/CAT1_RX_ER	PN3/ET1_RX_ER/ RMII1_RX_ER	PN3
H10	P73/CS3#/PO16/ET0_WOL/ LCD_EXTCLK-A	P73/CS3#/PO16/ET0_WOL/ LCD_EXTCLK-A	P73/CS3#/PO16/ET0_WOL/ LCD_EXTCLK-A
H11	PL0/TIC2/GTETRGA/SCK9/ RSPCKC/ET0_ERXD0/ RMII0_RXD0/CAT0_ERXD0	PL0/TIC2/GTETRGA/SCK9/ RSPCKC/ET0_ERXD0/ RMII0_RXD0	PL0/TIC2/GTETRGA/SCK9/ RSPCKC/ET0_ERXD0/ RMII0_RXD0
H12	VCC	VCC	VCC
H13	VSS	VSS	VSS
H14	PA6/A6/MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE10#/GTETRGB/CTS5#/ RTS5#/SS5#/MOSIA-B/ ET0_EXOUT/CATRESTOUT/ LCD_DATA2-B	PA6/A6/MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE10#/GTETRGB/CTS5#/ RTS5#/SS5#/MOSIA-B/ ET0_EXOUT/LCD_DATA2-B	PA6/A6/MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE10#/GTETRGB/CTS5#/ RTS5#/SS5#/MOSIA-B/ ET0_EXOUT/LCD_DATA2-B
H15	PA5/A5/MTIOC6B/TIOCB1/ PO21/GTIOC0A/RSPCKA-B/ ET0_LINKSTA/ CAT0_LINKSTA/ LCD_DATA3-B	PA5/A5/MTIOC6B/TIOCB1/ PO21/GTIOC0A/RSPCKA-B/ ET0_LINKSTA/ LCD_DATA3-B	PA5/A5/MTIOC6B/TIOCB1/ PO21/GTIOC0A/RSPCKA-B/ ET0_LINKSTA/ LCD_DATA3-B
J1	EXTAL/P36	EXTAL/P36	EXTAL/P36
J2	TDI/PF2/RXD1/SMISO1/ SSCL1/CATI2CCLK	TDI/PF2/RXD1/SMISO1/ SSCL1	TDI/PF2/RXD1/SMISO1/ SSCL1
J3	TMS/PF3	TMS/PF3	TMS/PF3
J4	P31/MTIOC4D/TMCI2/PO9/ RTCIC1/CTS1#/RTS1#/ SS1#/SSLB0-A/ET1_MDC/ PMGI1_MDC/IRQ1-DS	P31/MTIOC4D/TMCI2/PO9/ RTCIC1/CTS1#/RTS1#/ SS1#/SSLB0-A/ET1_MDC/ PMGI1_MDC/IRQ1-DS	P31/MTIOC4D/TMCI2/PO9/ RTCIC1/CTS1#/RTS1#/ SS1#/SSLB0-A/IRQ1-DS
J5	P30/MTIOC4B/TMRI3/PO8/ RTCIC0/POE8#/RXD1/ SMISO1/SSCL1/MISOB-A/ ET1_MDIO/PMGI1_MDIO/ IRQ0-DS	P30/MTIOC4B/TMRI3/PO8/ RTCIC0/POE8#/RXD1/ SMISO1/SSCL1/MISOB-A/ ET1_MDIO/PMGI1_MDIO/ IRQ0-DS	P30/MTIOC4B/TMRI3/PO8/ RTCIC0/POE8#/RXD1/ SMISO1/SSCL1/MISOB-A/ IRQ0-DS
J6	PH2/GTETRGC/SMOSI7/ SSDA7/TXD7/MISOA/ CATI2CDATA	PH2/GTETRGC/SMOSI7/ SSDA7/TXD7/MISOA	PH2/GTETRGC/SMOSI7/ SSDA7/TXD7/MISOA
J7	P15/MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCI2/ PO13/GTETRGA/RXD1/ SMISO1/SSCL1/SCK3/ CRX1-DS/SSILRCK1/ CATLEDRUN/PIXD0/IRQ5	P15/MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCI2/ PO13/GTETRGA/RXD1/ SMISO1/SSCL1/SCK3/ CRX1-DS/SSILRCK1/ PIXD0/IRQ5	P15/MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCI2/ PO13/GTETRGA/RXD1/ SMISO1/SSCL1/SCK3/ CRX1-DS/SSILRCK1/ PIXD0/IRQ5
J8	P53*[1]/BCLK	P53*[1]/BCLK	P53*[1]/BCLK
J9	PK3/GTETRGD/RTS8#/ CTS8#/SS8#/SSLB0/ ET0_TX_ER	PK3/GTETRGD/RTS8#/ CTS8#/SS8#/SSLB0/ ET0_TX_ER	PK3/GTETRGD/RTS8#/ CTS8#/SS8#/SSLB0/ ET0_TX_ER
J10	PL1/TOC2/GTETRGB/ SMISO9/SSCL9/RXD9/ MOSIC/ET0_ERXD1/ RMII0_RXD1/CAT0_ERXD1	PL1/TOC2/GTETRGB/ SMISO9/SSCL9/RXD9/ MOSIC/ET0_ERXD1/ RMII0_RXD1	PL1/TOC2/GTETRGB/ SMISO9/SSCL9/RXD9/ MOSIC/ET0_ERXD1/ RMII0_RXD1

224-Pin LFBGA	RX72M	RX72N	RX66N
J11	PN5/ET1_MDC/ PMGI1_MDC/QSSL-C	PN5/ET1_MDC/ PMGI1_MDC/QSSL-C	PN5/QSSL-C
J12	PB1/A9/MTIOC0C/ MTIOC4C/TIOCB3/TMCI0/ PO25/TXD4/SMOSI4/SSDA4/ TXD6/SMOSI6/SSDA6/ ET0_ERXD0/RMII0_RXD0/ CAT0_ERXD0/ LCD_TCON3-B/IRQ4-DS	PB1/A9/MTIOC0C/ MTIOC4C/TIOCB3/TMCI0/ PO25/TXD4/SMOSI4/SSDA4/ TXD6/SMOSI6/SSDA6/ ET0_ERXD0/RMII0_RXD0/ LCD_TCON3-B/IRQ4-DS	PB1/A9/MTIOC0C/ MTIOC4C/TIOCB3/TMCI0/ PO25/TXD4/SMOSI4/SSDA4/ TXD6/SMOSI6/SSDA6/ ET0_ERXD0/RMII0_RXD0/ LCD_TCON3-B/IRQ4-DS
J13	P71/A18/CS1#/ET0_MDIO/ CAT0_MDIO/PMGI0_MDIO/ DSMCLK3	P71/A18/CS1#/ET0_MDIO/ PMGI0_MDIO	P71/A18/CS1#/ET0_MDIO/ PMGI0_MDIO
J14	PB0/A8/MTIC5W/TIOCA3/ PO24/RXD4/SMISO4/SSCL4/ RXD6/SMISO6/SSCL6/ ET0_ERXD1/RMII0_RXD1/ CAT0_ERXD1/ LCD_DATA0-B/IRQ12	PB0/A8/MTIC5W/TIOCA3/ PO24/RXD4/SMISO4/SSCL4/ RXD6/SMISO6/SSCL6/ ET0_ERXD1/RMII0_RXD1/ LCD_DATA0-B/IRQ12	PB0/A8/MTIC5W/TIOCA3/ PO24/RXD4/SMISO4/SSCL4/ RXD6/SMISO6/SSCL6/ ET0_ERXD1/RMII0_RXD1/ LCD_DATA0-B/IRQ12
J15	PA7/A7/TIOCB2/PO23/ MISOA-B/ET0_WOL/ LCD_DATA1-B	PA7/A7/TIOCB2/PO23/ MISOA-B/ET0_WOL/ LCD_DATA1-B	PA7/A7/TIOCB2/PO23/ MISOA-B/ET0_WOL/ LCD_DATA1-B
K1	CLKOUT25M/PH7/GTIOC0B	CLKOUT25M/PH7/GTIOC0B	CLKOUT25M/PH7/GTIOC0B
K2	CLKOUT/PH6/GTIOC0A/ SSLA3/CATLATCH1	CLKOUT/PH6/GTIOC0A/ SSLA3	CLKOUT/PH6/GTIOC0A/ SSLA3
K3	PH4/GTADSM0/SSLA1/ CATLEDSTER	PH4/GTADSM0/SSLA1	PH4/GTADSM0/SSLA1
K4	PH5/GTADSM1/SSLA2/ CATLATCH0	PH5/GTADSM1/SSLA2	PH5/GTADSM1/SSLA2
K5	TDO/PF0/TXD1/SMOSI1/ SSDA1/CATI2CDATA	TDO/PF0/TXD1/SMOSI1/ SSDA1	TDO/PF0/TXD1/SMOSI1/ SSDA1
K6	PH1/TOC0/GTETRGB/ SMISO7/SSCL7/RXD7/ MOSIA/CATI2CCLK	PH1/TOC0/GTETRGB/ SMISO7/SSCL7/RXD7/ MOSIA	PH1/TOC0/GTETRGB/ SMISO7/SSCL7/RXD7/ MOSIA
K7	P10/ALE/MTIC5W/TMRI3/ IRQ0	P10/ALE/MTIC5W/TMRI3/ IRQ0	P10/ALE/MTIC5W/TMRI3/ IRQ0
K8	P50/WR0#/WR#/TXD2/ SMOSI2/SSDA2/ SSLB1-A/CATLEDERR	P50/WR0#/WR#/TXD2/ SMOSI2/SSDA2/SSLB1-A	P50/WR0#/WR#/TXD2/ SMOSI2/SSDA2/SSLB1-A
K9	PK1/TOC1/GTETRGB/ SMISO8/SSCL8/RXD8/ MOSIB/ET0_COL	PK1/TOC1/GTETRGB/ SMISO8/SSCL8/RXD8/ MOSIB/ET0_COL	PK1/TOC1/GTETRGB/ SMISO8/SSCL8/RXD8/ MOSIB/ET0_COL
K10	PL3/GTETRGD/RTS9#/ CTS9#/SS9#/SSLC0/ ET0_RX_CLK/REF50CK0/ CAT0_RX_CLK	PL3/GTETRGD/RTS9#/ CTS9#/SS9#/SSLC0/ ET0_RX_CLK/REF50CK0	PL3/GTETRGD/RTS9#/ CTS9#/SS9#/SSLC0/ ET0_RX_CLK/REF50CK0
K11	PM2/GTETRGC/SMOSI10/ SSDA10/TXD10/ ET1_ERXD2/CAT1_ERXD2/ SDHI_D0-D/QMO-A/QIO0-A	PM2/GTETRGC/SMOSI10/ SSDA10/TXD10/ ET1_ERXD2/SDHI_D0-D/ QMO-A/QIO0-A	PM2/GTETRGC/SMOSI10/ SSDA10/TXD10/ SDHI_D0-D/QMO-A/QIO0-A
K12	VSS	VSS	VSS

224-Pin LFBGA	RX72M	RX72N	RX66N
K13	PB5/A13/MTIOC2A/ MTIOC1B/TIOCB4/TMRI1/ PO29/POE4#/SCK9/RTS9#/ SCK11/ET0_ETXD0/ RMII0_TXD0/CAT0_ETXD0/ LCD_CLK-B	PB5/A13/MTIOC2A/ MTIOC1B/TIOCB4/TMRI1/ PO29/POE4#/SCK9/RTS9#/ SCK11/ET0_ETXD0/ RMII0_TXD0/LCD_CLK-B	PB5/A13/MTIOC2A/ MTIOC1B/TIOCB4/TMRI1/ PO29/POE4#/SCK9/RTS9#/ SCK11/ET0_ETXD0/ RMII0_TXD0/LCD_CLK-B
K14	PB3/A11/MTIOC0A/ MTIOC4A/TIOCD3/TCLKD/ TMO0/PO27/POE11#/SCK4/ SCK6/ET0_RX_ER/ RMII0_RX_ER/ CAT0_RX_ER/ LCD_TCON1-B	PB3/A11/MTIOC0A/ MTIOC4A/TIOCD3/TCLKD/ TMO0/PO27/POE11#/SCK4/ SCK6/ET0_RX_ER/ RMII0_RX_ER/ LCD_TCON1-B	PB3/A11/MTIOC0A/ MTIOC4A/TIOCD3/TCLKD/ TMO0/PO27/POE11#/SCK4/ SCK6/ET0_RX_ER/ RMII0_RX_ER/ LCD_TCON1-B
K15	P72/A19/CS2#/ET0_MDC/ CAT0_MDC/PMGI0_MDC/ LCD_DATA23-A/DSMDAT3	P72/A19/CS2#/ET0_MDC/ PMGI0_MDC/ LCD_DATA23-A	P72/A19/CS2#/ET0_MDC/ PMGI0_MDC/ LCD_DATA23-A
L1	PH3/GTETRGD/RTS7#/ CTS7#/SS7#/SSLA0/ CATLEDERR	PH3/GTETRGD/RTS7#/ CTS7#/SS7#/SSLA0	PH3/GTETRGD/RTS7#/ CTS7#/SS7#/SSLA0
L2	P27/CS7#/MTIOC2B/TMCI3/ PO7/SCK1/RSPCKB-A/ ET1_WOL/CATIRQ	P27/CS7#/MTIOC2B/TMCI3/ PO7/SCK1/RSPCKB-A/ ET1_WOL	P27/CS7#/MTIOC2B/TMCI3/ PO7/SCK1/RSPCKB-A
L3	TCK/PF1/SCK1	TCK/PF1/SCK1	TCK/PF1/SCK1
L4	P24/CS4#/EDREQ1/ MTIOC4A/MTCLKA/TIOCB4/ TMRI1/PO4/SCK3/ USB0_VBUSEN/SSIBCK1/ SDHI_WP/PIXCLK	P24/CS4#/EDREQ1/ MTIOC4A/MTCLKA/TIOCB4/ TMRI1/PO4/SCK3/ USB0_VBUSEN/SSIBCK1/ SDHI_WP/PIXCLK	P24/CS4#/EDREQ1/ MTIOC4A/MTCLKA/TIOCB4/ TMRI1/PO4/SCK3/ USB0_VBUSEN/SSIBCK1/ SDHI_WP/PIXCLK
L5	VCC	VCC	VCC
L6	CLKOUT25M/PJ2/TXD8/ SMOSI8/SSDA8/SSLC3-B/ LCD_TCON2-A	CLKOUT25M/PJ2/TXD8/ SMOSI8/SSDA8/SSLC3-B/ LCD_TCON2-A	CLKOUT25M/PJ2/TXD8/ SMOSI8/SSDA8/SSLC3-B/ LCD_TCON2-A
L7	VCC	VCC	VCC
L8	P52/RD#/RXD2/SMISO2/ SSCL2/SSLB3-A/ CATLEDSTER	P52/RD#/RXD2/SMISO2/ SSCL2/SSLB3-A	P52/RD#/RXD2/SMISO2/ SSCL2/SSLB3-A
L9	P81/EDACK0/MTIOC3D/ PO27/GTIOC0B/SMISO10/ SSCL10/RXD10/ ET0_ETXD0/RMII0_TXD0/ CAT0_ETXD0/CATI2CCLK/ QIO3-A/SDHI_CD/ MMC_D3-A/LCD_DATA13-A	P81/EDACK0/MTIOC3D/ PO27/GTIOC0B/SMISO10/ SSCL10/RXD10/ ET0_ETXD0/RMII0_TXD0/ QIO3-A/SDHI_CD/ MMC_D3-A/LCD_DATA13-A	P81/EDACK0/MTIOC3D/ PO27/GTIOC0B/SMISO10/ SSCL10/RXD10/ ET0_ETXD0/RMII0_TXD0/ QIO3-A/SDHI_CD/ MMC_D3-A/LCD_DATA13-A
L10	PL7/GTIOC2B/ET0_MDIO/ CAT0_MDIO/PMGI0_MDIO	PL7/GTIOC2B/ET0_MDIO/ PMGI0_MDIO	PL7/GTIOC2B/ET0_MDIO/ PMGI0_MDIO
L11	P77/CS7#/PO23/SMOSI11/ SSDA11/TXD11/ ET0_RX_ER/RMII0_RX_ER/ CAT0_RX_ER/QSPCLK-A/ SDHI_CLK-A/MMC_CLK-A/ LCD_DATA17-A	P77/CS7#/PO23/SMOSI11/ SSDA11/TXD11/ ET0_RX_ER/RMII0_RX_ER/ QSPCLK-A/SDHI_CLK-A/ MMC_CLK-A/ LCD_DATA17-A	P77/CS7#/PO23/SMOSI11/ SSDA11/TXD11/ ET0_RX_ER/RMII0_RX_ER/ QSPCLK-A/SDHI_CLK-A/ MMC_CLK-A/ LCD_DATA17-A
L12	PN4/ET1_MDIO/ PMGI1_MDIO/QSPCLK-C	PN4/ET1_MDIO/ PMGI1_MDIO/QSPCLK-C	PN4/QSPCLK-C
L13	VCC	VCC	VCC

224-Pin LFBGA	RX72M	RX72N	RX66N
L14	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/RTS4#/SS4#/CTS6#/RTS6#/SS6#/ET0_RX_CLK/REF50CK0/CAT0_RX_CLK/LCD_TCON2-B	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/RTS4#/SS4#/CTS6#/RTS6#/SS6#/ET0_RX_CLK/REF50CK0/LCD_TCON2-B	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/RTS4#/SS4#/CTS6#/RTS6#/SS6#/ET0_RX_CLK/REF50CK0/LCD_TCON2-B
L15	PB4/A12/TIOCA4/PO28/CTS9#/SS9#/SS11#/CTS11#/RTS11#/ET0_TX_EN/RMII0_TXD_EN/CAT0_TX_EN/LCD_TCON0-B	PB4/A12/TIOCA4/PO28/CTS9#/SS9#/SS11#/CTS11#/RTS11#/ET0_TX_EN/RMII0_TXD_EN/LCD_TCON0-B	PB4/A12/TIOCA4/PO28/CTS9#/SS9#/SS11#/CTS11#/RTS11#/ET0_TX_EN/RMII0_TXD_EN/LCD_TCON0-B
M1	P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/MOSIB-A/ET1_EXOUT/CATLINKACT1	P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/MOSIB-A/ET1_EXOUT	P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/MOSIB-A
M2	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/GTIOC0A/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/SS0#/CTX1/SSIBCK0/SDHI_D1-C/PIXD7	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/GTIOC0A/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/SS0#/CTX1/SSIBCK0/SDHI_D1-C/PIXD7	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/GTIOC0A/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/SS0#/CTX1/SSIBCK0/SDHI_D1-C/PIXD7
M3	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/SSIDATA1/SDHI_CD/HSYNC/ADTRG0#	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/SSIDATA1/SDHI_CD/HSYNC/ADTRG0#	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/SSIDATA1/SDHI_CD/HSYNC/ADTRG0#
M4	VSS	VSS	VSS
M5	PJ0/MTIOC6B/SCK8/SSLC1-B/EPLSOUT0/CATSYNC0/LCD_DATA0-A	PJ0/MTIOC6B/SCK8/SSLC1-B/EPLSOUT0/LCD_DATA0-A	PJ0/MTIOC6B/SCK8/SSLC1-B/LCD_DATA0-A
M6	P84/MTIOC6D/ET1_LINKSTA/CAT1_LINKSTA/LCD_DATA2-A	P84/MTIOC6D/ET1_LINKSTA/LCD_DATA2-A	P84/MTIOC6D/LCD_DATA2-A
M7	VSS	VSS	VSS
M8	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A
M9	P83/EDACK1/MTIOC4C/GTIOC0A/SCK10/SS10#/CTS10#/ET0_CRS/RMII0_CRS_DV/CAT0_RX_DV/LCD_DATA8-A/DSMCLK1	P83/EDACK1/MTIOC4C/GTIOC0A/SCK10/SS10#/CTS10#/ET0_CRS/RMII0_CRS_DV/LCD_DATA8-A	P83/EDACK1/MTIOC4C/GTIOC0A/SCK10/SS10#/CTS10#/ET0_CRS/RMII0_CRS_DV/LCD_DATA8-A
M10	PK0/TIC1/GTETRGA/SCK8/RSPCKB/ET0_MDC/CAT0_MDC/PMGI0_MDC	PK0/TIC1/GTETRGA/SCK8/RSPCKB/ET0_MDC/PMGI0_MDC	PK0/TIC1/GTETRGA/SCK8/RSPCKB/ET0_MDC/PMGI0_MDC
M11	PL5/GTADSM1/SSLC2/ET0_ETXD1/RMII0_TXD1/CAT0_ETXD1	PL5/GTADSM1/SSLC2/ET0_ETXD1/RMII0_TXD1	PL5/GTADSM1/SSLC2/ET0_ETXD1/RMII0_TXD1

224-Pin LFBGA	RX72M	RX72N	RX66N
M12	PL6/GTIOC2A/SSLC3/ ET0_TX_EN/ RMII0_TXD_EN/ CAT0_TX_EN	PL6/GTIOC2A/SSLC3/ ET0_TX_EN/RMII0_TXD_EN	PL6/GTIOC2A/SSLC3/ ET0_TX_EN/RMII0_TXD_EN
M13	PM7/GTIOC3B/ET0_CRS/ RMII0_CRS_DV/ CAT0_RX_DV/SDHI_WP	PM7/GTIOC3B/ET0_CRS/ RMII0_CRS_DV/SDHI_WP	PM7/GTIOC3B/ET0_CRS/ RMII0_CRS_DV/SDHI_WP
M14	PC0/A16/MTIOC3C/TCLKC/ PO17/CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3/ CAT0_ERXD3/IRQ14	PC0/A16/MTIOC3C/TCLKC/ PO17/CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3/IRQ14	PC0/A16/MTIOC3C/TCLKC/ PO17/CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3/IRQ14
M15	PB6/A14/MTIOC3D/TIOCA5/ PO30/RXD9/SMISO9/ SSCL9/SMISO11/SSCL11/ RXD11/ET0_ETXD1/ RMII0_TXD1/CAT0_ETXD1	PB6/A14/MTIOC3D/TIOCA5/ PO30/RXD9/SMISO9/ SSCL9/SMISO11/SSCL11/ RXD11/ET0_ETXD1/ RMII0_TXD1	PB6/A14/MTIOC3D/TIOCA5/ PO30/RXD9/SMISO9/ SSCL9/SMISO11/SSCL11/ RXD11/ET0_ETXD1/ RMII0_TXD1
N1	P22/EDREQ0/MTIOC3B/ MTCLKC/TIOCC3/TMO0/ PO2/GTIOC1A/SCK0/ USB0_OVRCURB/ AUDIO_CLK/SDHI_D0-C/ PIXD6	P22/EDREQ0/MTIOC3B/ MTCLKC/TIOCC3/TMO0/ PO2/GTIOC1A/SCK0/ USB0_OVRCURB/ AUDIO_CLK/SDHI_D0-C/ PIXD6	P22/EDREQ0/MTIOC3B/ MTCLKC/TIOCC3/TMO0/ PO2/GTIOC1A/SCK0/ USB0_OVRCURB/ AUDIO_CLK/SDHI_D0-C/ PIXD6
N2	PH0/TIC0/GTETRGA/SCK7/ RSPCKA/CATLEDRUN	PH0/TIC0/GTETRGA/SCK7/ RSPCKA	PH0/TIC0/GTETRGA/SCK7/ RSPCKA
N3	P86/MTIOC4D/TIOCA0/ GTIOC2B/SMISO10/ SSCL10/RXD10/ CATLINKACT0/PIXD1	P86/MTIOC4D/TIOCA0/ GTIOC2B/SMISO10/ SSCL10/RXD10/PIXD1	P86/MTIOC4D/TIOCA0/ GTIOC2B/SMISO10/ SSCL10/RXD10/PIXD1
N4	P85/MTIOC6C/TIOCC0/ LCD_DATA1-A	P85/MTIOC6C/TIOCC0/ LCD_DATA1-A	P85/MTIOC6C/TIOCC0/ LCD_DATA1-A
N5	P13/WR2#/BC2#/MTIOC0B/ TIOCA5/TMO3/PO13/ GTADSM1/TXD2/SMOSI2/ SSDA2/SDA0[FM+]/ LCD_TCON0-A/IRQ3/ ADTRG1#	P13/WR2#/BC2#/MTIOC0B/ TIOCA5/TMO3/PO13/ GTADSM1/TXD2/SMOSI2/ SSDA2/SDA0[FM+]/ LCD_TCON0-A/IRQ3/ ADTRG1#	P13/WR2#/BC2#/MTIOC0B/ TIOCA5/TMO3/PO13/ GTADSM1/TXD2/SMOSI2/ SSDA2/SDA0[FM+]/ LCD_TCON0-A/IRQ3/ ADTRG1#
N6	PJ1/MTIOC6A/RXD8/ SMISO8/SSCL8/SSLC2-B/ EPLSOUT1/CATSYNC1/ LCD_TCON3-A	PJ1/MTIOC6A/RXD8/ SMISO8/SSCL8/SSLC2-B/ EPLSOUT1/LCD_TCON3-A	PJ1/MTIOC6A/RXD8/ SMISO8/SSCL8/SSLC2-B/ LCD_TCON3-A
N7	CLKOUT25M/P56/EDACK1/ MTIOC3C/TIOCA1/SCK7/ RSPCKC-B/LCD_DATA4-A/ DSMDAT1	CLKOUT25M/P56/EDACK1/ MTIOC3C/TIOCA1/SCK7/ RSPCKC-B/LCD_DATA4-A	CLKOUT25M/P56/EDACK1/ MTIOC3C/TIOCA1/SCK7/ RSPCKC-B/LCD_DATA4-A
N8	VCC	VCC	VCC
N9	UB/PC7/A23/CS0#/ MTIOC3A/MTCLKB/TMO2/ PO31/TOC0/CACREF/ GTIOC3A/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/ ET0_COL/MMC_D7-A/ LCD_DATA9-A/IRQ14	UB/PC7/A23/CS0#/ MTIOC3A/MTCLKB/TMO2/ PO31/TOC0/CACREF/ GTIOC3A/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/ET0_COL/ MMC_D7-A/LCD_DATA9-A/ IRQ14	UB/PC7/A23/CS0#/ MTIOC3A/MTCLKB/TMO2/ PO31/TOC0/CACREF/ GTIOC3A/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/ET0_COL/ MMC_D7-A/LCD_DATA9-A/ IRQ14

224-Pin LFBGA	RX72M	RX72N	RX66N
N10	P80/EDREQ0/MTIOC3B/ PO26/SCK10/RTS10#/ ET0_TX_EN/ RMII0_TXD_EN/ CAT0_TX_EN/CATLATCH0/ QIO2-A/SDHI_WP/ MMC_D2-A/LCD_DATA14-A	P80/EDREQ0/MTIOC3B/ PO26/SCK10/RTS10#/ ET0_TX_EN/ RMII0_TXD_EN/QIO2-A/ SDHI_WP/MMC_D2-A/ LCD_DATA14-A	P80/EDREQ0/MTIOC3B/ PO26/SCK10/RTS10#/ ET0_TX_EN/ RMII0_TXD_EN/QIO2-A/ SDHI_WP/MMC_D2-A/ LCD_DATA14-A
N11	PK2/GTETRGC/SMOSI8/ SSDA8/TXD8/MISOB/ ET0_RX_DV/CAT0_RX_DV	PK2/GTETRGC/SMOSI8/ SSDA8/TXD8/MISOB/ ET0_RX_DV	PK2/GTETRGC/SMOSI8/ SSDA8/TXD8/MISOB/ ET0_RX_DV
N12	P76/CS6#/PO22/SMISO11/ SSCL11/RXD11/ ET0_RX_CLK/REF50CK0/ CAT0_RX_CLK/QSSL-A/ SDHI_CMD-A/MMC_CMD-A/ LCD_DATA18-A	P76/CS6#/PO22/SMISO11/ SSCL11/RXD11/ ET0_RX_CLK/REF50CK0/ QSSL-A/SDHI_CMD-A/ MMC_CMD-A/ LCD_DATA18-A	P76/CS6#/PO22/SMISO11/ SSCL11/RXD11/ ET0_RX_CLK/REF50CK0/ QSSL-A/SDHI_CMD-A/ MMC_CMD-A/ LCD_DATA18-A
N13	PM6/GTIOC3A/ ET0_TX_CLK/ CAT0_TX_CLK/SDHI_CD	PM6/GTIOC3A/ ET0_TX_CLK/SDHI_CD	PM6/GTIOC3A/ ET0_TX_CLK/SDHI_CD
N14	PC1/A17/MTIOC3A/TCLKD/ PO18/SCK5/SSLA2-A/ ET0_ERXD2/CAT0_ERXD2/ LCD_DATA22-A/IRQ12	PC1/A17/MTIOC3A/TCLKD/ PO18/SCK5/SSLA2-A/ ET0_ERXD2/ LCD_DATA22-A/IRQ12	PC1/A17/MTIOC3A/TCLKD/ PO18/SCK5/SSLA2-A/ ET0_ERXD2/ LCD_DATA22-A/IRQ12
N15	PB7/A15/MTIOC3B/TIOCB5/ PO31/TXD9/SMOSI9/ SSDA9/SMOSI11/SSDA11/ TXD11/ET0_CRS/ RMII0_CRS_DV/ CAT0_RX_DV	PB7/A15/MTIOC3B/TIOCB5/ PO31/TXD9/SMOSI9/ SSDA9/SMOSI11/SSDA11/ TXD11/ET0_CRS/ RMII0_CRS_DV	PB7/A15/MTIOC3B/TIOCB5/ PO31/TXD9/SMOSI9/ SSDA9/SMOSI11/SSDA11/ TXD11/ET0_CRS/ RMII0_CRS_DV
P1	PK7/GTIOC1B/ CATLINKACT1	PK7/GTIOC1B	PK7/GTIOC1B
P2	P17/MTIOC3A/MTIOC3B/ MTIOC4B/TIOCB0/TCLKD/ TMO1/PO15/POE8#/ GTIOC0B/SCK1/TXD3/ SMOSI3/SSDA3/SDA2-DS/ SSITXD0/EPLSOUT0/ CATSYNC0/SDHI_D3-C/ PIXD3/IRQ7/ADTRG1#	P17/MTIOC3A/MTIOC3B/ MTIOC4B/TIOCB0/TCLKD/ TMO1/PO15/POE8#/ GTIOC0B/SCK1/TXD3/ SMOSI3/SSDA3/SDA2-DS/ SSITXD0/EPLSOUT0/ SDHI_D3-C/PIXD3/IRQ7/ ADTRG1#	P17/MTIOC3A/MTIOC3B/ MTIOC4B/TIOCB0/TCLKD/ TMO1/PO15/POE8#/ GTIOC0B/SCK1/TXD3/ SMOSI3/SSDA3/SDA2-DS/ SSITXD0/SDHI_D3-C/ PIXD3/IRQ7/ADTRG1#
P3	P20/MTIOC1A/TIOCB3/ TMRI0/PO0/TXD0/SMOSI0/ SSDA0/SDA1/USB0_ID/ SSIRXD0/SDHI_CMD-C/ PIXD4/IRQ8	P20/MTIOC1A/TIOCB3/ TMRI0/PO0/TXD0/SMOSI0/ SSDA0/SDA1/USB0_ID/ SSIRXD0/SDHI_CMD-C/ PIXD4/IRQ8	P20/MTIOC1A/TIOCB3/ TMRI0/PO0/TXD0/SMOSI0/ SSDA0/SDA1/USB0_ID/ SSIRXD0/SDHI_CMD-C/ PIXD4/IRQ8
P4	P14/MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15/GTETRGD/CTS1#/ RTS1#/SS1#/CTX1/ USB0_OVRCURA/ LCD_CLK-A/IRQ4	P14/MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15/GTETRGD/CTS1#/ RTS1#/SS1#/CTX1/ USB0_OVRCURA/ LCD_CLK-A/IRQ4	P14/MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15/GTETRGD/CTS1#/ RTS1#/SS1#/CTX1/ USB0_OVRCURA/ LCD_CLK-A/IRQ4
P5	VCC_USB	VCC_USB	VCC_USB
P6	VSS_USB	VSS_USB	VSS_USB
P7	P57/RXD7/SMISO7/SSCL7/ SSLC0-B/LCD_DATA3-A	P57/RXD7/SMISO7/SSCL7/ SSLC0-B/LCD_DATA3-A	P57/RXD7/SMISO7/SSCL7/ SSLC0-B/LCD_DATA3-A

224-Pin LFBGA	RX72M	RX72N	RX66N
P8	P11/MTIC5V/TMCI3/SCK2/ EPLSOUT1/CATSYNC1/ LCD_DATA7-A/IRQ1	P11/MTIC5V/TMCI3/SCK2/ EPLSOUT1/LCD_DATA7-A/ IRQ1	P11/MTIC5V/TMCI3/SCK2/ LCD_DATA7-A/IRQ1
P9	VSS	VSS	VSS
P10	P82/EDREQ1/MTIOC4A/ PO28/GTIOC2A/SMOSI10/ SSDA10/TXD10/ ET0_ETXD1/RMII0_TXD1/ CAT0_ETXD1/CATI2CDATA/ MMC_D4-A/LCD_DATA12-A	P82/EDREQ1/MTIOC4A/ PO28/GTIOC2A/SMOSI10/ SSDA10/TXD10/ ET0_ETXD1/RMII0_TXD1/ MMC_D4-A/LCD_DATA12-A	P82/EDREQ1/MTIOC4A/ PO28/GTIOC2A/SMOSI10/ SSDA10/TXD10/ ET0_ETXD1/RMII0_TXD1/ MMC_D4-A/LCD_DATA12-A
P11	PC4/A20/CS3#/MTIOC3D/ MTCLKC/TMCI1/PO25/ POE0#/GTETRGC/SCK5/ CTS8#/SS8#/SS10#/ CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK/ CAT0_TX_CLK/CATSYNC0/ QMI-A/QIO1-A/SDHI_D1-A/ MMC_D1-A/LCD_DATA15-A	PC4/A20/CS3#/MTIOC3D/ MTCLKC/TMCI1/PO25/ POE0#/GTETRGC/SCK5/ CTS8#/SS8#/SS10#/ CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK/QMI-A/ QIO1-A/SDHI_D1-A/ MMC_D1-A/LCD_DATA15-A	PC4/A20/CS3#/MTIOC3D/ MTCLKC/TMCI1/PO25/ POE0#/GTETRGC/SCK5/ CTS8#/SS8#/SS10#/ CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK/QMI-A/ QIO1-A/SDHI_D1-A /MMC_D1-A/LCD_DATA15-A
P12	PL2/GTETRGC/SMOSI9/ SSDA9/TXD9/MISOC/ ET0_RX_ER/RMII0_RX_ER/ CAT0_RX_ER	PL2/GTETRGC/SMOSI9/ SSDA9/TXD9/MISOC/ ET0_RX_ER/RMII0_RX_ER	PL2/GTETRGC/SMOSI9/ SSDA9/TXD9/MISOC/ ET0_RX_ER/RMII0_RX_ER
P13	PC2/A18/MTIOC4B/TCLKA/ PO21/GTIOC2B/RXD5/ SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV/CAT0_RX_DV/ SDHI_D3-A/MMC_CD-A/ LCD_DATA19-A	PC2/A18/MTIOC4B/TCLKA/ PO21/GTIOC2B/RXD5/ SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV/SDHI_D3-A/ MMC_CD-A/LCD_DATA19-A	PC2/A18/MTIOC4B/TCLKA/ PO21/GTIOC2B/RXD5/ SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV/SDHI_D3-A/ MMC_CD-A/LCD_DATA19-A
P14	PM4/GTADSM0/ ET0_ETXD2/CAT0_ETXD2/ SDHI_D2-D/QIO2-A	PM4/GTADSM0/ ET0_ETXD2/SDHI_D2-D/ QIO2-A	PM4/GTADSM0/ ET0_ETXD2/SDHI_D2-D/ QIO2-A
P15	PM3/GTETRGD/RTS10#/ CTS10#/SS10#/ET1_ERXD3/ CAT1_ERXD3/SDHI_D1-D/ QMI-A/QIO1-A	PM3/GTETRGD/RTS10#/ CTS10#/SS10#/ET1_ERXD3/ SDHI_D1-D/QMI-A/QIO1-A	PM3/GTETRGD/RTS10#/ CTS10#/SS10#/SDHI_D1-D/ QMI-A/QIO1-A
R1	P21/MTIOC1B/MTIOC4A/ TIOCA3/TMCI0/PO1/ GTIOC2A/RXD0/SMISO0/ SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/ SDHI_CLK-C/PIXD5/IRQ9	P21/MTIOC1B/MTIOC4A/ TIOCA3/TMCI0/PO1/ GTIOC2A/RXD0/SMISO0/ SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/ SDHI_CLK-C/PIXD5/IRQ9	P21/MTIOC1B/MTIOC4A/ TIOCA3/TMCI0/PO1/ GTIOC2A/RXD0/SMISO0/ SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/ SDHI_CLK-C/PIXD5/IRQ9
R2	P87/MTIOC4C/TIOCA2/ GTIOC1B/SMOSI10/ SSDA10/TXD10/EPLSOUT1/ CATSYNC1/SDHI_D2-C/ PIXD2	P87/MTIOC4C/TIOCA2/ GTIOC1B/SMOSI10/ SSDA10/TXD10/EPLSOUT1/ SDHI_D2-C/PIXD2	P87/MTIOC4C/TIOCA2/ GTIOC1B/SMOSI10/ SSDA10/TXD10/SDHI_D2-C/ PIXD2

224-Pin LFBGA	RX72M	RX72N	RX66N
R3	P16/MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOUT/TXD1/ SMOSI1/SSDA1/RXD3/ SMISO3/SSCL3/SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB/IRQ6/ ADTRG0#	P16/MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOUT/TXD1/ SMOSI1/SSDA1/RXD3/ SMISO3/SSCL3/SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB/IRQ6/ ADTRG0#	P16/MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOUT/TXD1/ SMOSI1/SSDA1/RXD3/ SMISO3/SSCL3/SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB/IRQ6/ ADTRG0#
R4	P12/WR3#/BC3#/MTIC5U/ TMCI1/GTADSM0/RXD2/ SMISO2/SSCL2/SCL0[FM+]/ LCD_TCON1-A/IRQ2	P12/WR3#/BC3#/MTIC5U/ TMCI1/GTADSM0/RXD2/ SMISO2/SSCL2/SCL0[FM+]/ LCD_TCON1-A/IRQ2	P12/WR3#/BC3#/MTIC5U/ TMCI1/GTADSM0/RXD2/ SMISO2/SSCL2/SCL0[FM+]/ LCD_TCON1-A/IRQ2
R5	USB0_DM	USB0_DM	USB0_DM
R6	USB0_DP	USB0_DP	USB0_DP
R7	P54/D1[A1/D1]/EDACK0/ ALE/MTIOC4B/TMCI1/ CTS2#/RTS2#/SS2#/ MOSIC-B/CTX1/ ET0_LINKSTA/ CAT0_LINKSTA/ LCD_DATA6-A	P54/D1[A1/D1]/EDACK0/ ALE/MTIOC4B/TMCI1/ CTS2#/RTS2#/SS2#/ MOSIC-B/CTX1/ ET0_LINKSTA/ LCD_DATA6-A	P54/D1[A1/D1]/EDACK0/ ALE/MTIOC4B/TMCI1/ CTS2#/RTS2#/SS2#/ MOSIC-B/CTX1/ ET0_LINKSTA/ LCD_DATA6-A
R8	P55/D0[A0/D0]/EDREQ0/ WAIT#/MTIOC4D/TMO3/ TXD7/SMOSI7/SSDA7/ MISOC-B/CRX1/ ET0_EXOUT/ LCD_DATA5-A/IRQ10	P55/D0[A0/D0]/EDREQ0/ WAIT#/MTIOC4D/TMO3/ TXD7/SMOSI7/SSDA7/ MISOC-B/CRX1/ ET0_EXOUT/ LCD_DATA5-A/IRQ10	P55/D0[A0/D0]/EDREQ0/ WAIT#/MTIOC4D/TMO3/ TXD7/SMOSI7/SSDA7/ MISOC-B/CRX1/ ET0_EXOUT/ LCD_DATA5-A/IRQ10
R9	PC6/D2[A2/D2]/A22/CS1#/ MTIOC3C/MTCLKA/TMCI2/ PO30/TIC0/GTIOC3B/RXD8/ SMISO8/SSCL8/SMISO10/ SSCL10/RXD10/MOSIA-A/ ET0_ETXD3/CAT0_ETXD3/ CATLATCH1/MMC_D6-A/ LCD_DATA10-A/IRQ13	PC6/D2[A2/D2]/A22/CS1#/ MTIOC3C/MTCLKA/TMCI2/ PO30/TIC0/GTIOC3B/RXD8/ SMISO8/SSCL8/SMISO10/ SSCL10/RXD10/MOSIA-A/ ET0_ETXD3/MMC_D6-A/ LCD_DATA10-A/IRQ13	PC6/D2[A2/D2]/A22/CS1#/ MTIOC3C/MTCLKA/TMCI2/ PO30/TIC0/GTIOC3B/RXD8/ SMISO8/SSCL8/SMISO10/ SSCL10/RXD10/MOSIA-A/ ET0_ETXD3/MMC_D6-A/ LCD_DATA10-A/IRQ13
R10	PC5/D3[A3/D3]/A21/CS2#/ WAIT#/MTIOC3B/MTCLKD/ TMRI2/PO29/GTIOC1A/ SCK8/RTS8#/SCK10/ RSPCKA-A/ET0_ETXD2/ CAT0_ETXD2/MMC_D5-A/ LCD_DATA11-A	PC5/D3[A3/D3]/A21/CS2#/ WAIT#/MTIOC3B/MTCLKD/ TMRI2/PO29/GTIOC1A/ SCK8/RTS8#/SCK10/ RSPCKA-A/ET0_ETXD2/ MMC_D5-A/LCD_DATA11-A	PC5/D3[A3/D3]/A21/CS2#/ WAIT#/MTIOC3B/MTCLKD/ TMRI2/PO29/GTIOC1A/ SCK8/RTS8#/SCK10/ RSPCKA-A/ET0_ETXD2/ MMC_D5-A/LCD_DATA11-A
R11	PC3/A19/MTIOC4D/TCLKB/ PO24/GTIOC1B/TXD5/ SMOSI5/SSDA5/ ET0_TX_ER/QMO-A/QIO0-A/ SDHI_D0-A/MMC_D0-A/ LCD_DATA16-A	PC3/A19/MTIOC4D/TCLKB/ PO24/GTIOC1B/TXD5/ SMOSI5/SSDA5/ ET0_TX_ER/QMO-A/QIO0-A/ SDHI_D0-A/MMC_D0-A/ LCD_DATA16-A	PC3/A19/MTIOC4D/TCLKB/ PO24/GTIOC1B/TXD5/ SMOSI5/SSDA5/ ET0_TX_ER/QMO-A/QIO0-A/ SDHI_D0-A/MMC_D0-A/ LCD_DATA16-A
R12	PL4/GTADSM0/SSLC1/ ET0_ETXD0/RMII0_TXD0/ CAT0_ETXD0	PL4/GTADSM0/SSLC1/ ET0_ETXD0/RMII0_TXD0	PL4/GTADSM0/SSLC1/ ET0_ETXD0/RMII0_TXD0

224-Pin LFBGA	RX72M	RX72N	RX66N
R13	P75/CS5#/PO20/SCK11/ RTS11#/ET0_ERXD0/ RMII0_RXD0/CAT0_ERXD0/ SDHI_D2-A/MMC_RES#-A/ LCD_DATA20-A/DSMDAT2	P75/CS5#/PO20/SCK11/ RTS11#/ET0_ERXD0/ RMII0_RXD0/SDHI_D2-A/ MMC_RES#-A/ LCD_DATA20-A	P75/CS5#/PO20/SCK11/ RTS11#/ET0_ERXD0/ RMII0_RXD0/SDHI_D2-A/ MMC_RES#-A/ LCD_DATA20-A
R14	P74/A20/CS4#/PO19/SS11#/ CTS11#/ET0_ERXD1/ RMII0_RXD1/CAT0_ERXD1/ LCD_DATA21-A/DSMCLK2	P74/A20/CS4#/PO19/SS11#/ CTS11#/ET0_ERXD1/ RMII0_RXD1/ LCD_DATA21-A	P74/A20/CS4#/PO19/SS11#/ CTS11#/ET0_ERXD1/ RMII0_RXD1/ LCD_DATA21-A
R15	PM5/GTADSM1/ ET0_ETXD3/CAT0_ETXD3/ SDHI_D3-D/QIO3-A	PM5/GTADSM1/ ET0_ETXD3/SDHI_D3-D/ QIO3-A	PM5/GTADSM1/ ET0_ETXD3/SDHI_D3-D/ QIO3-A

Note: 1. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.

3.2 176-Pin LFBGA Package

Table 3.2 is a comparative listing of the pin functions of 176-pin LFBGA package products.

Table 3.2 Comparative Listing of 176-Pin LFBGA Package Pin Functions

176-Pin LFBGA	RX72M	RX72N	RX66N
A1	AVSS0	AVSS0	AVSS0
A2	AVCC0	AVCC0	AVCC0
A3	VREFL0	VREFL0	VREFL0
A4	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
A5	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
A6	VCC	VCC	VCC
A7	VSS	VSS	VSS
A8	P94/D20/A20/ET1_ERXD0/ RMII1_RXD0/CAT1_ERXD0	P94/D20/A20/ET1_ERXD0/ RMII1_RXD0	P94/D20/A20
A9	VCC	VCC	VCC
A10	TRSYNC1/P97/D23/A23/ ET1_ERXD3/CAT1_ERXD3	TRSYNC1/P97/D23/A23/ ET1_ERXD3	TRSYNC1/P97/D23/A23
A11	PD6/D6[A6/D6]/MTIC5V/ MTIOC8A/POE4#/SSLC2-A/ ET1_RX_CLK/REF50CK1/ CAT1_RX_CLK/QMO-B/ QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/ IRQ6/AN106	PD6/D6[A6/D6]/MTIC5V/ MTIOC8A/POE4#/SSLC2-A/ ET1_RX_CLK/REF50CK1/ QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/ IRQ6/AN106	PD6/D6[A6/D6]/MTIC5V/ MTIOC8A/POE4#/SSLC2-A/ QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/ IRQ6/AN106
A12	P60/CS0#/ET1_TX_EN/ RMII1_TXD_EN/ CAT1_TX_EN	P60/CS0#/ET1_TX_EN/ RMII1_TXD_EN	P60/CS0#
A13	P63/CAS#/D2[A2/D2]/CS3#/ ET1_ETXD1/RMII1_TXD1/ CAT1_ETXD1	P63/CAS#/D2[A2/D2]/CS3#/ ET1_ETXD1/RMII1_TXD1	P63/CAS#/D2[A2/D2]/CS3#
A14	PE1/D9[A9/D9]/D1[A1/D1]/ MTIOC4C/MTIOC3B/PO18/ GTIOC1B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/ SSLB2-B/MMC_D5-B/ LCD_DATA15-B/ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/ MTIOC4C/MTIOC3B/PO18/ GTIOC1B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/ SSLB2-B/MMC_D5-B/ LCD_DATA15-B/ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/ MTIOC4C/MTIOC3B/PO18/ GTIOC1B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/ SSLB2-B/MMC_D5-B/ LCD_DATA15-B/ANEX1
A15	PE2/D10[A10/D10]/ D2[A2/D2]/MTIOC4A/PO23/ TIC3/GTIOC0B/RXD12/ SMISO12/SSCL12/RXDX12/ SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/ AN100	PE2/D10[A10/D10]/ D2[A2/D2]/MTIOC4A/PO23/ TIC3/GTIOC0B/RXD12/ SMISO12/SSCL12/RXDX12/ SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/ AN100	PE2/D10[A10/D10]/ D2[A2/D2]/MTIOC4A/PO23/ TIC3/GTIOC0B/RXD12/ SMISO12/SSCL12/RXDX12/ SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/ AN100
B1	P05/SSILRCK1/IRQ13/DA1	P05/SSILRCK1/IRQ13/DA1	P05/SSILRCK1/IRQ13/DA1
B2	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
B3	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
B4	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
B5	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
B6	P91/D17/A17/SCK7/ ET1_COL/AN115/DSMDAT5	P91/D17/A17/SCK7/ ET1_COL/AN115	P91/D17/A17/SCK7/AN115

176-Pin LFBGA	RX72M	RX72N	RX66N
B7	P92/D18/A18/POE4#/RXD7/ SMISO7/SSCL7/ET1_CRS/ RMII1_CRS_DV/ CAT1_RX_DV/AN116/ DSMCLK4	P92/D18/A18/POE4#/RXD7/ SMISO7/SSCL7/ET1_CRS/ RMII1_CRS_DV/AN116	P92/D18/A18/POE4#/RXD7/ SMISO7/SSCL7/AN116
B8	PD1/D1[A1/D1]/MTIOC4B/ POE0#/GTIOC1A/MOSIC-A/ CTX0/LCD_DATA23-B/IRQ1/ AN109	PD1/D1[A1/D1]/MTIOC4B/ POE0#/GTIOC1A/MOSIC-A/ CTX0/LCD_DATA23-B/IRQ1/ AN109	PD1/D1[A1/D1]/MTIOC4B/ POE0#/GTIOC1A/MOSIC-A/ CTX0/LCD_DATA23-B/IRQ1/ AN109
B9	TRDATA5/P96/D22/A22/ ET1_ERXD2/CAT1_ERXD2	TRDATA5/P96/D22/A22/ ET1_ERXD2	TRDATA5/P96/D22/A22
B10	PD4/D4[A4/D4]/MTIOC8B/ POE11#/SSLC0-A/ ET1_MDIO/PMGI1_MDIO/ QSSL-B/SDHI_CMD-B/ MMC_CMD-B/ LCD_DATA20-B/IRQ4/AN112	PD4/D4[A4/D4]/MTIOC8B/ POE11#/SSLC0-A/ ET1_MDIO/PMGI1_MDIO/ QSSL-B/SDHI_CMD-B/ MMC_CMD-B/ LCD_DATA20-B/IRQ4/AN112	PD4/D4[A4/D4]/MTIOC8B/ POE11#/SSLC0-A/QSSL-B/ SDHI_CMD-B/MMC_CMD-B/ LCD_DATA20-B/IRQ4/ AN112
B11	TRDATA7/PG1/D25/ ET1_RX_ER/RMII1_RX_ER/ CAT1_RX_ER	TRDATA7/PG1/D25/ ET1_RX_ER/RMII1_RX_ER	TRDATA7/PG1/D25
B12	VSS	VSS	VSS
B13	P64/WE#/D3[A3/D3]/CS4#/ ET1_ETXD0/RMII1_TXD0/ CAT1_ETXD0	P64/WE#/D3[A3/D3]/CS4#/ ET1_ETXD0/RMII1_TXD0	P64/WE#/D3[A3/D3]/CS4#
B14	PE0/D8[A8/D8]/D0[A0/D0]/ MTIOC3D/GTIOC2B/SCK12/ SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/ MTIOC3D/GTIOC2B/SCK12/ SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/ MTIOC3D/GTIOC2B/SCK12/ SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0
B15	PE3/D11[A11/D11]/ D3[A3/D3]/MTIOC4B/PO26/ TOC3/POE8#/GTIOC2A/ CTS12#/RTS12#/SS12#/ ET0_ERXD3/CAT0_ERXD3/ MMC_D7-B/LCD_DATA13-B/ AN101	PE3/D11[A11/D11]/ D3[A3/D3]/MTIOC4B/PO26/ TOC3/POE8#/GTIOC2A/ CTS12#/RTS12#/SS12#/ ET0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101	PE3/D11[A11/D11]/ D3[A3/D3]/MTIOC4B/PO26/ TOC3/POE8#/GTIOC2A/ CTS12#/RTS12#/SS12#/ ET0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101
C1	AVSS1	AVSS1	AVSS1
C2	AVCC1	AVCC1	AVCC1
C3	VREFH0	VREFH0	VREFH0
C4	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
C5	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
C6	P90/D16/A16/TXD7/SMOSI7/ SSDA7/ET1_RX_DV/ CAT1_RX_DV/AN114/ DSMCLK5	P90/D16/A16/TXD7/SMOSI7/ SSDA7/ET1_RX_DV/AN114	P90/D16/A16/TXD7/SMOSI7/ SSDA7/AN114
C7	PD0/D0[A0/D0]/POE4#/ GTIOC1B/LCD_EXTCLK-B/ IRQ0/AN108	PD0/D0[A0/D0]/POE4#/ GTIOC1B/LCD_EXTCLK-B/ IRQ0/AN108	PD0/D0[A0/D0]/POE4#/ GTIOC1B/LCD_EXTCLK-B/ IRQ0/AN108
C8	PD2/D2[A2/D2]/MTIOC4D/ TIC2/GTIOC0B/MISOC-A/ CRX0/ET1_EXOUT/QIO2-B/ SDHI_D2-B/MMC_D2-B/ LCD_DATA22-B/IRQ2/AN110	PD2/D2[A2/D2]/MTIOC4D/ TIC2/GTIOC0B/MISOC-A/ CRX0/ET1_EXOUT/QIO2-B/ SDHI_D2-B/MMC_D2-B/ LCD_DATA22-B/IRQ2/AN110	PD2/D2[A2/D2]/MTIOC4D/ TIC2/GTIOC0B/MISOC-A/ CRX0/QIO2-B/SDHI_D2-B/ MMC_D2-B/LCD_DATA22-B/ IRQ2/AN110

176-Pin LFBGA	RX72M	RX72N	RX66N
C9	PD3/D3[A3/D3]/MTIOC8D/ TOC2/POE8#/GTIOC0A/ RSPCKC-A/ET1_WOL/ QIO3-B/SDHI_D3-B/ MMC_D3-B/LCD_DATA21-B/ IRQ3/AN111	PD3/D3[A3/D3]/MTIOC8D/ TOC2/POE8#/GTIOC0A/ RSPCKC-A/ET1_WOL/ QIO3-B/SDHI_D3-B/ MMC_D3-B/LCD_DATA21-B/ IRQ3/AN111	PD3/D3[A3/D3]/MTIOC8D/ TOC2/POE8#/GTIOC0A/ RSPCKC-A/QIO3-B/ SDHI_D3-B/MMC_D3-B/ LCD_DATA21-B/IRQ3/AN111
C10	TRDATA6/PG0/D24/ ET1_RX_CLK/REF50CK1/ CAT1_RX_CLK	TRDATA6/PG0/D24/ ET1_RX_CLK/REF50CK1	TRDATA6/PG0/D24
C11	VCC	VCC	VCC
C12	P62/RAS#/D1[A1/D1]/CS2#/ ET1_ERXD0/RMII1_RXD0/ CAT1_ERXD0	P62/RAS#/D1[A1/D1]/CS2#/ ET1_ERXD0/RMII1_RXD0	P62/RAS#/D1[A1/D1]/CS2#
C13	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/MTIOC1A/PO28/ GTIOC1A/SSLB0-B/ ET0_ERXD2/CAT0_ERXD2/ LCD_DATA12-B/AN102	PE4/D12[A12/D12]/D4[A4/ D4]/MTIOC4D/MTIOC1A/ PO28/GTIOC1A/SSLB0-B/ ET0_ERXD2/ LCD_DATA12-B/AN102	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/MTIOC1A/PO28/ GTIOC1A/SSLB0-B/ ET0_ERXD2/ LCD_DATA12-B/AN102
C14	VSS	VSS	VSS
C15	P70/SDCLK/CATLINKACT0	P70/SDCLK	P70/SDCLK
D1	P01/TMCI0/RXD6/SMISO6/ SSCL6/SSIBCK0/ CATLEDERR/IRQ9/AN119	P01/TMCI0/RXD6/SMISO6/ SSCL6/SSIBCK0/IRQ9/ AN119	P01/TMCI0/RXD6/SMISO6/ SSCL6/SSIBCK0/IRQ9/ AN119
D2	P02/TMCI1/SCK6/SSIBCK1/ CATLEDSTER/IRQ10/AN120	P02/TMCI1/SCK6/SSIBCK1/ IRQ10/AN120	P02/TMCI1/SCK6/SSIBCK1/ IRQ10/AN120
D3	P03/SSIDATA1/IRQ11/DA0	P03/SSIDATA1/IRQ11/DA0	P03/SSIDATA1/IRQ11/DA0
D4	P00/TMRI0/TXD6/SMOSI6/ SSDA6/AUDIO_CLK/ CATLATCH1/IRQ8/AN118	P00/TMRI0/TXD6/SMOSI6/ SSDA6/AUDIO_CLK/IRQ8/ AN118	P00/TMRI0/TXD6/SMOSI6/ SSDA6/AUDIO_CLK/IRQ8/ AN118
D5	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
D6	P93/D19/A19/POE0#/CTS7#/ RTS7#/SS7#/ET1_LINKSTA/ CAT1_LINKSTA/AN117/ DSMDAT4	P93/D19/A19/POE0#/CTS7#/ RTS7#/SS7#/ET1_LINKSTA/ AN117	P93/D19/A19/POE0#/CTS7#/ RTS7#/SS7#/AN117
D7	TRDATA4/P95/D21/A21/ ET1_ERXD1/RMII1_RXD1/ CAT1_ERXD1	TRDATA4/P95/D21/A21/ ET1_ERXD1/RMII1_RXD1	TRDATA4/P95/D21/A21
D8	VSS	VSS	VSS
D9	PD5/D5[A5/D5]/MTIC5W/ MTIOC8C/MTCLKA/POE10#/ SSLC1-A/ET1_MDC/ PMGI1_MDC/QSPCLK-B/ SDHI_CLK-B/MMC_CLK-B/ LCD_DATA19-B/IRQ5/AN113	PD5/D5[A5/D5]/MTIC5W/ MTIOC8C/MTCLKA/POE10#/ SSLC1-A/ET1_MDC/ PMGI1_MDC/QSPCLK-B/ SDHI_CLK-B/MMC_CLK-B/ LCD_DATA19-B/IRQ5/AN113	PD5/D5[A5/D5]/MTIC5W/ MTIOC8C/MTCLKA/POE10#/ SSLC1-A/QSPCLK-B/ SDHI_CLK-B/MMC_CLK-B/ LCD_DATA19-B/IRQ5/AN113
D10	PD7/D7[A7/D7]/MTIC5U/ POE0#/SSLC3-A/ ET1_RX_ER/RMII1_RX_ER/ CAT1_RX_ER/QMI-B/ QIO1-B/SDHI_D1-B/ MMC_D1-B/LCD_DATA17-B/ IRQ7/AN107	PD7/D7[A7/D7]/MTIC5U/ POE0#/SSLC3-A/ ET1_RX_ER/RMII1_RX_ER/ QMI-B/QIO1-B/SDHI_D1-B/ MMC_D1-B/LCD_DATA17-B/ IRQ7/AN107	PD7/D7[A7/D7]/MTIC5U/ POE0#/SSLC3-A/QMI-B/ QIO1-B/SDHI_D1-B/ MMC_D1-B/LCD_DATA17-B/ IRQ7/AN107
D11	P61/SDCS#/D0[A0/D0]/ CS1#/ET1_ERXD1/ RMII1_RXD1/CAT1_ERXD1	P61/SDCS#/D0[A0/D0]/ CS1#/ET1_ERXD1/ RMII1_RXD1	P61/SDCS#/D0[A0/D0]/CS1#

176-Pin LFBGA	RX72M	RX72N	RX66N
D12	PE5/D13[A13/D13]/ D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/ RSPCKB-B/ET0_RX_CLK/ REF50CK0/CAT0_RX_CLK/ LCD_DATA11-B/IRQ5/AN103	PE5/D13[A13/D13]/ D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/ RSPCKB-B/ET0_RX_CLK/ REF50CK0/LCD_DATA11-B/ IRQ5/AN103	PE5/D13[A13/D13]/ D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/ RSPCKB-B/ET0_RX_CLK/ REF50CK0/LCD_DATA11-B/ IRQ5/AN103
D13	VCC	VCC	VCC
D14	PE7/D15[A15/D15]/ D7[A7/D7]/MTIOC6A/TOC1/ GTIOC3A/MISOB-B/ SDHI_WP/MMC_RES#-B/ LCD_DATA9-B/IRQ7/AN105	PE7/D15[A15/D15]/ D7[A7/D7]/MTIOC6A/TOC1/ GTIOC3A/MISOB-B/ SDHI_WP/MMC_RES#-B/ LCD_DATA9-B/IRQ7/AN105	PE7/D15[A15/D15]/ D7[A7/D7]/MTIOC6A/TOC1/ GTIOC3A/MISOB-B/ SDHI_WP/MMC_RES#-B/ LCD_DATA9-B/IRQ7/AN105
D15	P65/CKE/CS5#	P65/CKE/CS5#	P65/CKE/CS5#
E1	PJ5/POE8#/CTS2#/RTS2#/ SS2#/SSIRXD0/EPLSOUT0/ CATSYNC0	PJ5/POE8#/CTS2#/RTS2#/ SS2#/SSIRXD0/EPLSOUT0	PJ5/POE8#/CTS2#/RTS2#/ SS2#/SSIRXD0
E2	EMLE	EMLE	EMLE
E3	PF5/WAIT#/SSILRCK0/ CATLATCH0/IRQ4	PF5/WAIT#/SSILRCK0/IRQ4	PF5/WAIT#/SSILRCK0/IRQ4
E4	VSS	VSS	VSS
E12	PE6/D14[A14/D14]/ D6[A6/D6]/MTIOC6C/TIC1/ GTIOC3B/MOSIB-B/ SDHI_CD/MMC_CD-B/ LCD_DATA10-B/IRQ6/AN104	PE6/D14[A14/D14]/ D6[A6/D6]/MTIOC6C/TIC1/ GTIOC3B/MOSIB-B/ SDHI_CD/MMC_CD-B/ LCD_DATA10-B/IRQ6/AN104	PE6/D14[A14/D14]/ D6[A6/D6]/MTIOC6C/TIC1/ GTIOC3B/MOSIB-B/ SDHI_CD/MMC_CD-B/ LCD_DATA10-B/IRQ6/AN104
E13	TRDATA0/PG2/D26/ ET1_TX_CLK/ CAT1_TX_CLK	TRDATA0/PG2/D26/ ET1_TX_CLK	TRDATA0/PG2/D26
E14	TRDATA1/PG3/D27/ ET1_ETXD0/RMII1_TXD0/ CAT1_ETXD0	TRDATA1/PG3/D27/ ET1_ETXD0/RMII1_TXD0	TRDATA1/PG3/D27
E15	P67/DQM1/CS7#/MTIOC7C/ GTIOC1B/CRX2/EPLSOUT1/ CATSYNC1/IRQ15	P67/DQM1/CS7#/MTIOC7C/ GTIOC1B/CRX2/EPLSOUT1/ IRQ15	P67/DQM1/CS7#/MTIOC7C/ GTIOC1B/CRX2/IRQ15
F1	VBATT	VBATT	VBATT
F2	VCL	VCL	VCL
F3	PJ3/EDACK1/MTIOC3C/ CTS6#/RTS6#/SS6#/CTS0#/ RTS0#/SS0#/SSITXD0/ ET0_EXOUT/CATRESTOUT	PJ3/EDACK1/MTIOC3C/ CTS6#/RTS6#/SS6#/CTS0#/ RTS0#/SS0#/SSITXD0/ ET0_EXOUT	PJ3/EDACK1/MTIOC3C/ CTS6#/RTS6#/SS6#/CTS0#/ RTS0#/SS0#/SSITXD0/ ET0_EXOUT
F4	BSCANP	BSCANP	BSCANP
F12	P66/DQM0/CS6#/MTIOC7D/ GTIOC2B/CTX2	P66/DQM0/CS6#/MTIOC7D/ GTIOC2B/CTX2	P66/DQM0/CS6#/MTIOC7D/ GTIOC2B/CTX2
F13	TRSYNC/PG4/D28/ ET1_ETXD1/RMII1_TXD1/ CAT1_ETXD1	TRSYNC/PG4/D28/ ET1_ETXD1/RMII1_TXD1	TRSYNC/PG4/D28
F14	PA0/DQM2/BC0#/A0/ MTIOC4A/MTIOC6D/ TIOCA0/PO16/CACREF/ GTIOC0B/SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN/ CAT0_TX_EN/CATLEDRUN/ LCD_DATA8-B	PA0/DQM2/BC0#/A0/ MTIOC4A/MTIOC6D/ TIOCA0/PO16/CACREF/ GTIOC0B/SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN/ LCD_DATA8-B	PA0/DQM2/BC0#/A0/ MTIOC4A/MTIOC6D/ TIOCA0/PO16/CACREF/ GTIOC0B/SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN/ LCD_DATA8-B

176-Pin LFBGA	RX72M	RX72N	RX66N
F15	VSS	VSS	VSS
G1	XCIN	XCIN	XCIN
G2	XCOUT	XCOUT	XCOUT
G3	MD/FINED	MD/FINED	MD/FINED
G4	TRST#/PF4	TRST#/PF4	TRST#/PF4
G12	TRCLK/PG5/D29/ ET1_ETXD2/CAT1_ETXD2	TRCLK/PG5/D29/ ET1_ETXD2	TRCLK/PG5/D29
G13	TRDATA2/PG6/D30/ ET1_ETXD3/CAT1_ETXD3	TRDATA2/PG6/D30/ ET1_ETXD3	TRDATA2/PG6/D30
G14	PA1/DQM3/A1/MTIOC0B/ MTCLKC/MTIOC7B/TIOCB0/ PO17/GTIOC2A/SCK5/ SSLA2-B/ET0_WOL/ LCD_DATA7-B/IRQ11	PA1/DQM3/A1/MTIOC0B/ MTCLKC/MTIOC7B/TIOCB0/ PO17/GTIOC2A/SCK5/ SSLA2-B/ET0_WOL/ LCD_DATA7-B/IRQ11	PA1/DQM3/A1/MTIOC0B/ MTCLKC/MTIOC7B/TIOCB0/ PO17/GTIOC2A/SCK5/ SSLA2-B/ET0_WOL/ LCD_DATA7-B/IRQ11
G15	VCC	VCC	VCC
H1	XTAL/P37	XTAL/P37	XTAL/P37
H2	VSS	VSS	VSS
H3	RES#	RES#	RES#
H4	UPSEL/P35/NMI	UPSEL/P35/NMI	UPSEL/P35/NMI
H12	PA4/A4/MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20/TXD5/ SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/CAT0_MDC/ CATIRQ/PMGI0_MDC/ LCD_DATA4-B/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20/TXD5/ SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/PMGI0_MDC/ LCD_DATA4-B/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20/TXD5/ SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/PMGI0_MDC/ LCD_DATA4-B/IRQ5-DS
H13	PA3/A3/MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19/ RXD5/SMISO5/SSCL5/ ET0_MDIO/CAT0_MDIO/ PMGI0_MDIO/ LCD_DATA5-B/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19/ RXD5/SMISO5/SSCL5/ ET0_MDIO/PMGI0_MDIO/ LCD_DATA5-B/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19/ RXD5/SMISO5/SSCL5/ ET0_MDIO/PMGI0_MDIO/ LCD_DATA5-B/IRQ6-DS
H14	PA2/A2/MTIOC7A/PO18/ GTIOC1A/RXD5/SMISO5/ SSCL5/SSLA3-B/ CATLINKACT1/ LCD_DATA6-B	PA2/A2/MTIOC7A/PO18/ GTIOC1A/RXD5/SMISO5/ SSCL5/SSLA3-B/ LCD_DATA6-B	PA2/A2/MTIOC7A/PO18/ GTIOC1A/RXD5/SMISO5/ SSCL5/SSLA3-B/ LCD_DATA6-B
H15	TRDATA3/PG7/D31/ ET1_TX_ER	TRDATA3/PG7/D31/ ET1_TX_ER	TRDATA3/PG7/D31
J1	EXTAL/P36	EXTAL/P36	EXTAL/P36
J2	VCC	VCC	VCC
J3	P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/ ET0_LINKSTA/ CAT0_LINKSTA/IRQ4/ DSMDAT0	P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/ ET0_LINKSTA/IRQ4	P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/ ET0_LINKSTA/IRQ4
J4	TMS/PF3	TMS/PF3	TMS/PF3
J12	PA5/A5/MTIOC6B/TIOCB1/ PO21/GTIOC0A/RSPCKA-B/ ET0_LINKSTA/ CAT0_LINKSTA/ LCD_DATA3-B	PA5/A5/MTIOC6B/TIOCB1/ PO21/GTIOC0A/RSPCKA-B/ ET0_LINKSTA/ LCD_DATA3-B	PA5/A5/MTIOC6B/TIOCB1/ PO21/GTIOC0A/RSPCKA-B/ ET0_LINKSTA/ LCD_DATA3-B
J13	VSS	VSS	VSS

176-Pin LFBGA	RX72M	RX72N	RX66N
J14	PA7/A7/TIOCB2/PO23/ MISOA-B/ET0_WOL/ LCD_DATA1-B	PA7/A7/TIOCB2/PO23/ MISOA-B/ET0_WOL/ LCD_DATA1-B	PA7/A7/TIOCB2/PO23/ MISOA-B/ET0_WOL/ LCD_DATA1-B
J15	PA6/A6/MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE10#/GTETRGB/CTS5#/ RTS5#/SS5#/MOSIA-B/ ET0_EXOUT/CATRESTOUT/ LCD_DATA2-B	PA6/A6/MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE10#/GTETRGB/CTS5#/ RTS5#/SS5#/MOSIA-B/ ET0_EXOUT/LCD_DATA2-B	PA6/A6/MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE10#/GTETRGB/CTS5#/ RTS5#/SS5#/MOSIA-B/ ET0_EXOUT/LCD_DATA2-B
K1	P33/EDREQ1/MTIOC0D/ TIOCD0/TMRI3/PO11/ POE4#/POE11#/RXD6/ SMISO6/SSCL6/RXD0/ SMISO0/SSCL0/CRX0/ PCKO/IRQ3-DS/DSMCLK0	P33/EDREQ1/MTIOC0D/ TIOCD0/TMRI3/PO11/ POE4#/POE11#/RXD6/ SMISO6/SSCL6/RXD0/ SMISO0/SSCL0/CRX0/ PCKO/IRQ3-DS	P33/EDREQ1/MTIOC0D/ TIOCD0/TMRI3/PO11/ POE4#/POE11#/RXD6/ SMISO6/SSCL6/RXD0/ SMISO0/SSCL0/CRX0/ PCKO/IRQ3-DS
K2	P32/MTIOC0C/TIOCC0/ TMO3/PO10/RTCIC2/ RTCOUT/POE0#/POE10#/ TXD6/SMOSI6/SSDA6/TXD0/ SMOSI0/SSDA0/CTX0/ USB0_VBUSEN/VSYNC/ IRQ2-DS	P32/MTIOC0C/TIOCC0/ TMO3/PO10/RTCIC2/ RTCOUT/POE0#/POE10#/ TXD6/SMOSI6/SSDA6/TXD0/ SMOSI0/SSDA0/CTX0/ USB0_VBUSEN/VSYNC/ IRQ2-DS	P32/MTIOC0C/TIOCC0/ TMO3/PO10/RTCIC2/ RTCOUT/POE0#/POE10#/ TXD6/SMOSI6/SSDA6/TXD0/ SMOSI0/SSDA0/CTX0/ USB0_VBUSEN/VSYNC/ IRQ2-DS
K3	TDI/PF2/RXD1/SMISO1/ SSCL1/CATI2CCLK	TDI/PF2/RXD1/SMISO1/ SSCL1	TDI/PF2/RXD1/SMISO1/ SSCL1
K4	TCK/PF1/SCK1	TCK/PF1/SCK1	TCK/PF1/SCK1
K12	PB2/A10/TIOCC3/TCLKC/ PO26/CTS4#/RTS4#/SS4#/ CTS6#/RTS6#/SS6#/ ET0_RX_CLK/REF50CK0/ CAT0_RX_CLK/ LCD_TCON2-B	PB2/A10/TIOCC3/TCLKC/ PO26/CTS4#/RTS4#/SS4#/ CTS6#/RTS6#/SS6#/ ET0_RX_CLK/REF50CK0/ LCD_TCON2-B	PB2/A10/TIOCC3/TCLKC/ PO26/CTS4#/RTS4#/SS4#/ CTS6#/RTS6#/SS6#/ ET0_RX_CLK/REF50CK0/ LCD_TCON2-B
K13	P71/A18/CS1#/ET0_MDIO/ CAT0_MDIO/PMGI0_MDIO/ DSMCLK3	P71/A18/CS1#/ET0_MDIO/ PMGI0_MDIO	P71/A18/CS1#/ET0_MDIO/ PMGI0_MDIO
K14	VCC	VCC	VCC
K15	PB0/A8/MTIC5W/TIOCA3/ PO24/RXD4/SMISO4/SSCL4/ RXD6/SMISO6/SSCL6/ ET0_ERXD1/RMII0_RXD1/ CAT0_ERXD1/ LCD_DATA0-B/IRQ12	PB0/A8/MTIC5W/TIOCA3/ PO24/RXD4/SMISO4/SSCL4/ RXD6/SMISO6/SSCL6/ ET0_ERXD1/RMII0_RXD1/ LCD_DATA0-B/IRQ12	PB0/A8/MTIC5W/TIOCA3/ PO24/RXD4/SMISO4/SSCL4/ RXD6/SMISO6/SSCL6/ ET0_ERXD1/RMII0_RXD1/ LCD_DATA0-B/IRQ12
L1	P31/MTIOC4D/TMCI2/PO9/ RTCIC1/CTS1#/RTS1#/ SS1#/SSLB0-A/ET1_MDC/ PMGI1_MDC/IRQ1-DS	P31/MTIOC4D/TMCI2/PO9/ RTCIC1/CTS1#/RTS1#/ SS1#/SSLB0-A/ET1_MDC/ PMGI1_MDC/IRQ1-DS	P31/MTIOC4D/TMCI2/PO9/ RTCIC1/CTS1#/RTS1#/ SS1#/SSLB0-A/IRQ1-DS
L2	P30/MTIOC4B/TMRI3/PO8/ RTCIC0/POE8#/RXD1/ SMISO1/SSCL1/MISOB-A/ ET1_MDIO/PMGI1_MDIO/ IRQ0-DS	P30/MTIOC4B/TMRI3/PO8/ RTCIC0/POE8#/RXD1/ SMISO1/SSCL1/MISOB-A/ ET1_MDIO/PMGI1_MDIO/ IRQ0-DS	P30/MTIOC4B/TMRI3/PO8/ RTCIC0/POE8#/RXD1/ SMISO1/SSCL1/MISOB-A/ IRQ0-DS
L3	TDO/PF0/TXD1/SMOSI1/ SSDA1/CATI2CDATA	TDO/PF0/TXD1/SMOSI1/ SSDA1	TDO/PF0/TXD1/SMOSI1/ SSDA1

176-Pin LFBGA	RX72M	RX72N	RX66N
L4	CLKOUT/P25/CS5#/ EDACK1/MTIOC4C/ MTCLKB/TIOCA4/PO5/ RXD3/SMISO3/SSCL3/ SSIDATA1/SDHI_CD/ HSYNC/ADTRG0#	CLKOUT/P25/CS5#/ EDACK1/MTIOC4C/ MTCLKB/TIOCA4/PO5/ RXD3/SMISO3/SSCL3/ SSIDATA1/SDHI_CD/ HSYNC/ADTRG0#	CLKOUT/P25/CS5#/ EDACK1/MTIOC4C/ MTCLKB/TIOCA4/PO5/ RXD3/SMISO3/SSCL3/ SSIDATA1/SDHI_CD/ HSYNC/ADTRG0#
L12	PB6/A14/MTIOC3D/TIOCA5/ PO30/RXD9/SMISO9/SSCL9/ SMISO11/SSCL11/RXD11/ ET0_ETXD1/RMII0_TXD1/ CAT0_ETXD1	PB6/A14/MTIOC3D/TIOCA5/ PO30/RXD9/SMISO9/SSCL9/ SMISO11/SSCL11/RXD11/ ET0_ETXD1/RMII0_TXD1	PB6/A14/MTIOC3D/TIOCA5/ PO30/RXD9/SMISO9/SSCL9/ SMISO11/SSCL11/RXD11/ ET0_ETXD1/RMII0_TXD1
L13	PB3/A11/MTIOC0A/ MTIOC4A/TIOCD3/TCLKD/ TMO0/PO27/POE11#/SCK4/ SCK6/ET0_RX_ER/ RMII0_RX_ER/ CAT0_RX_ER/ LCD_TCON1-B	PB3/A11/MTIOC0A/ MTIOC4A/TIOCD3/TCLKD/ TMO0/PO27/POE11#/SCK4/ SCK6/ET0_RX_ER/ RMII0_RX_ER/ LCD_TCON1-B	PB3/A11/MTIOC0A/ MTIOC4A/TIOCD3/TCLKD/ TMO0/PO27/POE11#/SCK4/ SCK6/ET0_RX_ER/ RMII0_RX_ER/ LCD_TCON1-B
L14	PB1/A9/MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25/TXD4/ SMOSI4/SSDA4/TXD6/ SMOSI6/SSDA6/ ET0_ERXD0/RMII0_RXD0/ CAT0_ERXD0/ LCD_TCON3-B/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25/TXD4/ SMOSI4/SSDA4/TXD6/ SMOSI6/SSDA6/ ET0_ERXD0/RMII0_RXD0/ LCD_TCON3-B/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25/TXD4/ SMOSI4/SSDA4/TXD6/ SMOSI6/SSDA6/ ET0_ERXD0/RMII0_RXD0/ LCD_TCON3-B/IRQ4-DS
L15	P72/A19/CS2#/ET0_MDC/ CAT0_MDC/PMGI0_MDC/ LCD_DATA23-A/DSMDAT3	P72/A19/CS2#/ET0_MDC/ PMGI0_MDC/ LCD_DATA23-A	P72/A19/CS2#/ET0_MDC/ PMGI0_MDC/ LCD_DATA23-A
M1	P27/CS7#/MTIOC2B/TMCI3/ PO7/SCK1/RSPCKB-A/ ET1_WOL/CATIRQ	P27/CS7#/MTIOC2B/TMCI3/ PO7/SCK1/RSPCKB-A/ ET1_WOL	P27/CS7#/MTIOC2B/TMCI3/ PO7/SCK1/RSPCKB-A
M2	P26/CS6#/MTIOC2A/TMO1/ PO6/TXD1/SMOSI1/SSDA1/ CTS3#/RTS3#/SS3#/ MOSIB-A/ET1_EXOUT/ CATLINKACT1	P26/CS6#/MTIOC2A/TMO1/ PO6/TXD1/SMOSI1/SSDA1/ CTS3#/RTS3#/SS3#/ MOSIB-A/ET1_EXOUT	P26/CS6#/MTIOC2A/TMO1/ PO6/TXD1/SMOSI1/SSDA1/ CTS3#/RTS3#/SS3#/ MOSIB-A
M3	P24/CS4#/EDREQ1/ MTIOC4A/MTCLKA/TIOCB4/ TMRI1/PO4/SCK3/ USB0_VBUSEN/SSIBCK1/ SDHI_WP/PIXCLK	P24/CS4#/EDREQ1/ MTIOC4A/MTCLKA/TIOCB4/ TMRI1/PO4/SCK3/ USB0_VBUSEN/SSIBCK1/ SDHI_WP/PIXCLK	P24/CS4#/EDREQ1/ MTIOC4A/MTCLKA/TIOCB4/ TMRI1/PO4/SCK3/ USB0_VBUSEN/SSIBCK1/ SDHI_WP/PIXCLK
M4	P86/MTIOC4D/TIOCA0/ GTIOC2B/SMISO10/SSCL10/ RXD10/CATLINKACT0/ PIXD1	P86/MTIOC4D/TIOCA0/ GTIOC2B/SMISO10/SSCL10/ RXD10/PIXD1	P86/MTIOC4D/TIOCA0/ GTIOC2B/SMISO10/SSCL10/ RXD10/PIXD1
M5	CLKOUT25M/PJ2/TXD8/ SMOSI8/SSDA8/SSLC3-B/ LCD_TCON2-A	CLKOUT25M/PJ2/TXD8/ SMOSI8/SSDA8/SSLC3-B/ LCD_TCON2-A	CLKOUT25M/PJ2/TXD8/ SMOSI8/SSDA8/SSLC3-B/ LCD_TCON2-A
M6	PJ1/MTIOC6A/RXD8/ SMISO8/SSCL8/SSLC2-B/ EPLSOUT1/CATSYNC1/ LCD_TCON3-A	PJ1/MTIOC6A/RXD8/ SMISO8/SSCL8/SSLC2-B/ EPLSOUT1/LCD_TCON3-A	PJ1/MTIOC6A/RXD8/ SMISO8/SSCL8/SSLC2-B/ LCD_TCON3-A
M7	P85/MTIOC6C/TIOCC0/ LCD_DATA1-A	P85/MTIOC6C/TIOCC0/ LCD_DATA1-A	P85/MTIOC6C/TIOCC0/ LCD_DATA1-A

176-Pin LFBGA	RX72M	RX72N	RX66N
M8	P55/D0[A0/D0]/EDREQ0/ WAIT#/MTIOC4D/TMO3/ TXD7/SMOSI7/SSDA7/ MISOC-B/CRX1/ ET0_EXOUT/ LCD_DATA5-A/IRQ10	P55/D0[A0/D0]/EDREQ0/ WAIT#/MTIOC4D/TMO3/ TXD7/SMOSI7/SSDA7/ MISOC-B/CRX1/ ET0_EXOUT/ LCD_DATA5-A/IRQ10	P55/D0[A0/D0]/EDREQ0/ WAIT#/MTIOC4D/TMO3/ TXD7/SMOSI7/SSDA7/ MISOC-B/CRX1/ ET0_EXOUT/ LCD_DATA5-A/IRQ10
M9	P50/WR0#/WR#/TXD2/ SMOSI2/SSDA2/SSLB1-A/ CATLEDERR	P50/WR0#/WR#/TXD2/ SMOSI2/SSDA2/SSLB1-A	P50/WR0#/WR#/TXD2/ SMOSI2/SSDA2/SSLB1-A
M10	PC5/D3[A3/D3]/A21/CS2#/ WAIT#/MTIOC3B/MTCLKD/ TMRI2/PO29/GTIOC1A/ SCK8/RTS8#/SCK10/ RSPCKA-A/ET0_ETXD2/ CAT0_ETXD2/MMC_D5-A/ LCD_DATA11-A	PC5/D3[A3/D3]/A21/CS2#/ WAIT#/MTIOC3B/MTCLKD/ TMRI2/PO29/GTIOC1A/ SCK8/RTS8#/SCK10/ RSPCKA-A/ET0_ETXD2/ MMC_D5-A/LCD_DATA11-A	PC5/D3[A3/D3]/A21/CS2#/ WAIT#/MTIOC3B/MTCLKD/ TMRI2/PO29/GTIOC1A/ SCK8/RTS8#/SCK10/ RSPCKA-A/ET0_ETXD2/ MMC_D5-A/LCD_DATA11-A
M11	P81/EDACK0/MTIOC3D/ PO27/GTIOC0B/SMISO10/ SSCL10/RXD10/ ET0_ETXD0/RMII0_TXD0/ CAT0_ETXD0/CATI2CCLK/ QIO3-A/SDHI_CD/ MMC_D3-A/LCD_DATA13-A	P81/EDACK0/MTIOC3D/ PO27/GTIOC0B/SMISO10/ SSCL10/RXD10/ ET0_ETXD0/RMII0_TXD0/ QIO3-A/SDHI_CD/ MMC_D3-A/LCD_DATA13-A	P81/EDACK0/MTIOC3D/ PO27/GTIOC0B/SMISO10/ SSCL10/RXD10/ ET0_ETXD0/RMII0_TXD0/ QIO3-A/SDHI_CD/ MMC_D3-A/LCD_DATA13-A
M12	P77/CS7#/PO23/SMOSI11/ SSDA11/TXD11/ ET0_RX_ER/RMII0_RX_ER/ CAT0_RX_ER/QSPCLK-A/ SDHI_CLK-A/MMC_CLK-A/ LCD_DATA17-A	P77/CS7#/PO23/SMOSI11/ SSDA11/TXD11/ ET0_RX_ER/RMII0_RX_ER/ QSPCLK-A/SDHI_CLK-A/ MMC_CLK-A/ LCD_DATA17-A	P77/CS7#/PO23/SMOSI11/ SSDA11/TXD11/ ET0_RX_ER/RMII0_RX_ER/ QSPCLK-A/SDHI_CLK-A/ MMC_CLK-A/ LCD_DATA17-A
M13	PB7/A15/MTIOC3B/TIOCB5/ PO31/TXD9/SMOSI9/SSDA9/ SMOSI11/SSDA11/TXD11/ ET0_CRS/RMII0_CRS_DV/ CAT0_RX_DV	PB7/A15/MTIOC3B/TIOCB5/ PO31/TXD9/SMOSI9/SSDA9/ SMOSI11/SSDA11/TXD11/ ET0_CRS/RMII0_CRS_DV	PB7/A15/MTIOC3B/TIOCB5/ PO31/TXD9/SMOSI9/SSDA9/ SMOSI11/SSDA11/TXD11/ ET0_CRS/RMII0_CRS_DV
M14	PB5/A13/MTIOC2A/ MTIOC1B/TIOCB4/TMRI1/ PO29/POE4#/SCK9/RTS9#/ SCK11/ET0_ETXD0/ RMII0_TXD0/CAT0_ETXD0/ LCD_CLK-B	PB5/A13/MTIOC2A/ MTIOC1B/TIOCB4/TMRI1/ PO29/POE4#/SCK9/RTS9#/ SCK11/ET0_ETXD0/ RMII0_TXD0/LCD_CLK-B	PB5/A13/MTIOC2A/ MTIOC1B/TIOCB4/TMRI1/ PO29/POE4#/SCK9/RTS9#/ SCK11/ET0_ETXD0/ RMII0_TXD0/LCD_CLK-B
M15	PB4/A12/TIOCA4/PO28/ CTS9#/SS9#/SS11#/ CTS11#/RTS11#/ ET0_TX_EN/ RMII0_TXD_EN/ CAT0_TX_EN/ LCD_TCON0-B	PB4/A12/TIOCA4/PO28/ CTS9#/SS9#/SS11#/ CTS11#/RTS11#/ ET0_TX_EN/ RMII0_TXD_EN/ LCD_TCON0-B	PB4/A12/TIOCA4/PO28/ CTS9#/SS9#/SS11#/ CTS11#/RTS11#/ ET0_TX_EN/ RMII0_TXD_EN/ LCD_TCON0-B
N1	VCC	VCC	VCC
N2	P23/EDACK0/MTIOC3D/ MTCLKD/TIOCD3/PO3/ GTIOC0A/TXD3/SMOSI3/ SSDA3/CTS0#/RTS0#/SS0#/ CTX1/SSIBCK0/SDHI_D1-C/ PIXD7	P23/EDACK0/MTIOC3D/ MTCLKD/TIOCD3/PO3/ GTIOC0A/TXD3/SMOSI3/ SSDA3/CTS0#/RTS0#/SS0#/ CTX1/SSIBCK0/SDHI_D1-C/ PIXD7	P23/EDACK0/MTIOC3D/ MTCLKD/TIOCD3/PO3/ GTIOC0A/TXD3/SMOSI3/ SSDA3/CTS0#/RTS0#/SS0#/ CTX1/SSIBCK0/SDHI_D1-C/ PIXD7

176-Pin LFBGA	RX72M	RX72N	RX66N
N3	P22/EDREQ0/MTIOC3B/ MTCLKC/TIOCC3/TMO0/ PO2/GTIOC1A/SCK0/ USB0_OVRCURB/ AUDIO_CLK/SDHI_D0-C/ PIXD6	P22/EDREQ0/MTIOC3B/ MTCLKC/TIOCC3/TMO0/ PO2/GTIOC1A/SCK0/ USB0_OVRCURB/ AUDIO_CLK/SDHI_D0-C/ PIXD6	P22/EDREQ0/MTIOC3B/ MTCLKC/TIOCC3/TMO0/ PO2/GTIOC1A/SCK0/ USB0_OVRCURB/ AUDIO_CLK/SDHI_D0-C/ PIXD6
N4	P15/MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCI2/ PO13/GTETRGA/RXD1/ SMISO1/SSCL1/SCK3/ CRX1-DS/SSILRCK1/ CATLEDRUN/PIXD0/IRQ5	P15/MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCI2/ PO13/GTETRGA/RXD1/ SMISO1/SSCL1/SCK3/ CRX1-DS/SSILRCK1/PIXD0/ IRQ5	P15/MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCI2/ PO13/GTETRGA/RXD1/ SMISO1/SSCL1/SCK3/ CRX1-DS/SSILRCK1/PIXD0/ IRQ5
N5	P12/WR3#/BC3#/MTIC5U/ TMCI1/GTADSM0/RXD2/ SMISO2/SSCL2/SCL0[FM+]/ LCD_TCON1-A/IRQ2	P12/WR3#/BC3#/MTIC5U/ TMCI1/GTADSM0/RXD2/ SMISO2/SSCL2/SCL0[FM+]/ LCD_TCON1-A/IRQ2	P12/WR3#/BC3#/MTIC5U/ TMCI1/GTADSM0/RXD2/ SMISO2/SSCL2/SCL0[FM+]/ LCD_TCON1-A/IRQ2
N6	PJ0/MTIOC6B/SCK8/ SSLC1-B/EPLSOUT0/ CATSYNC0/LCD_DATA0-A	PJ0/MTIOC6B/SCK8/ SSLC1-B/EPLSOUT0/ LCD_DATA0-A	PJ0/MTIOC6B/SCK8/ SSLC1-B/LCD_DATA0-A
N7	P84/MTIOC6D/ ET1_LINKSTA/ CAT1_LINKSTA/ LCD_DATA2-A	P84/MTIOC6D/ ET1_LINKSTA/ LCD_DATA2-A	P84/MTIOC6D/ LCD_DATA2-A
N8	P54/D1[A1/D1]/EDACK0/ ALE/MTIOC4B/TMCI1/ CTS2#/RTS2#/SS2#/ MOSIC-B/CTX1/ ET0_LINKSTA/ CAT0_LINKSTA/ LCD_DATA6-A	P54/D1[A1/D1]/EDACK0/ ALE/MTIOC4B/TMCI1/ CTS2#/RTS2#/SS2#/ MOSIC-B/CTX1/ ET0_LINKSTA/ LCD_DATA6-A	P54/D1[A1/D1]/EDACK0/ ALE/MTIOC4B/TMCI1/ CTS2#/RTS2#/SS2#/ MOSIC-B/CTX1/ ET0_LINKSTA/ LCD_DATA6-A
N9	P51/WR1#/BC1#/WAIT#/ SCK2/SSLB2-A	P51/WR1#/BC1#/WAIT#/ SCK2/SSLB2-A	P51/WR1#/BC1#/WAIT#/ SCK2/SSLB2-A
N10	UB/PC7/A23/CS0#/ MTIOC3A/MTCLKB/TMO2/ PO31/TOC0/CACREF/ GTIOC3A/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/ET0_COL/ MMC_D7-A/LCD_DATA9-A/ IRQ14	UB/PC7/A23/CS0#/ MTIOC3A/MTCLKB/TMO2/ PO31/TOC0/CACREF/ GTIOC3A/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/ ET0_COL/MMC_D7-A/ LCD_DATA9-A/IRQ14	UB/PC7/A23/CS0#/ MTIOC3A/MTCLKB/TMO2/ PO31/TOC0/CACREF/ GTIOC3A/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/ ET0_COL/MMC_D7-A/ LCD_DATA9-A/IRQ14
N11	P82/EDREQ1/MTIOC4A/ PO28/GTIOC2A/SMOSI10/ SSDA10/TXD10/ ET0_ETXD1/RMII0_TXD1/ CAT0_ETXD1/CATI2CDATA/ MMC_D4-A/LCD_DATA12-A	P82/EDREQ1/MTIOC4A/ PO28/GTIOC2A/SMOSI10/ SSDA10/TXD10/ ET0_ETXD1/RMII0_TXD1/ MMC_D4-A/LCD_DATA12-A	P82/EDREQ1/MTIOC4A/ PO28/GTIOC2A/SMOSI10/ SSDA10/TXD10/ ET0_ETXD1/RMII0_TXD1/ MMC_D4-A/LCD_DATA12-A
N12	PC3/A19/MTIOC4D/TCLKB/ PO24/GTIOC1B/TXD5/ SMOSI5/SSDA5/ ET0_TX_ER/QMO-A/QIO0-A/ SDHI_D0-A/MMC_D0-A/ LCD_DATA16-A	PC3/A19/MTIOC4D/TCLKB/ PO24/GTIOC1B/TXD5/ SMOSI5/SSDA5/ ET0_TX_ER/QMO-A/QIO0-A/ SDHI_D0-A/MMC_D0-A/ LCD_DATA16-A	PC3/A19/MTIOC4D/TCLKB/ PO24/GTIOC1B/TXD5/ SMOSI5/SSDA5/ ET0_TX_ER/QMO-A/QIO0-A/ SDHI_D0-A/MMC_D0-A/ LCD_DATA16-A

176-Pin LFBGA	RX72M	RX72N	RX66N
N13	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1-A/ET0_ERXD3/CAT0_ERXD3/IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14
N14	P73/CS3#/PO16/ET0_WOL/LCD_EXTCLK-A	P73/CS3#/PO16/ET0_WOL/LCD_EXTCLK-A	P73/CS3#/PO16/ET0_WOL/LCD_EXTCLK-A
N15	VSS	VSS	VSS
P1	VSS	VSS	VSS
P2	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/GTIOC0B/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/SSITXD0/EPLSOUT0/CATSYNC0/SDHI_D3-C/PIXD3/IRQ7/ADTRG1#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/GTIOC0B/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/SSITXD0/EPLSOUT0/SDHI_D3-C/PIXD3/IRQ7/ADTRG1#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/GTIOC0B/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/SSITXD0/SDHI_D3-C/PIXD3/IRQ7/ADTRG1#
P3	P87/MTIOC4C/TIOCA2/GTIOC1B/SMOSI10/SSDA10/TXD10/EPLSOUT1/CATSYNC1/SDHI_D2-C/PIXD2	P87/MTIOC4C/TIOCA2/GTIOC1B/SMOSI10/SSDA10/TXD10/EPLSOUT1/SDHI_D2-C/PIXD2	P87/MTIOC4C/TIOCA2/GTIOC1B/SMOSI10/SSDA10/TXD10/SDHI_D2-C/PIXD2
P4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/GTETRGD/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/LCD_CLK-A/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/GTETRGD/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/LCD_CLK-A/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/GTETRGD/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/LCD_CLK-A/IRQ4
P5	VCC_USB	VCC_USB	VCC_USB
P6	VSS_USB	VSS_USB	VSS_USB
P7	P57/RXD7/SMISO7/SSCL7/SSLC0-B/LCD_DATA3-A	P57/RXD7/SMISO7/SSCL7/SSLC0-B/LCD_DATA3-A	P57/RXD7/SMISO7/SSCL7/SSLC0-B/LCD_DATA3-A
P8	P10/ALE/MTIC5W/TMRI3/IRQ0	P10/ALE/MTIC5W/TMRI3/IRQ0	P10/ALE/MTIC5W/TMRI3/IRQ0
P9	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A/CATLEDSTER	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A
P10	P83/EDACK1/MTIOC4C/GTIOC0A/SCK10/SS10#/CTS10#/ET0_CRS/RMII0_CRS_DV/CAT0_RX_DV/LCD_DATA8-A/DSMCLK1	P83/EDACK1/MTIOC4C/GTIOC0A/SCK10/SS10#/CTS10#/ET0_CRS/RMII0_CRS_DV/LCD_DATA8-A	P83/EDACK1/MTIOC4C/GTIOC0A/SCK10/SS10#/CTS10#/ET0_CRS/RMII0_CRS_DV/LCD_DATA8-A
P11	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/PO30/TIC0/GTIOC3B/RXD8/SMISO8/SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/ET0_ETXD3/CAT0_ETXD3/CATLATCH1/MMC_D6-A/LCD_DATA10-A/IRQ13	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/PO30/TIC0/GTIOC3B/RXD8/SMISO8/SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/ET0_ETXD3/MMC_D6-A/LCD_DATA10-A/IRQ13	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/PO30/TIC0/GTIOC3B/RXD8/SMISO8/SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/ET0_ETXD3/MMC_D6-A/LCD_DATA10-A/IRQ13

176-Pin LFBGA	RX72M	RX72N	RX66N
P12	PC4/A20/CS3#/MTIOC3D/ MTCLKC/TMCI1/PO25/ POE0#/GTETRGC/SCK5/ CTS8#/SS8#/SS10#/ CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK/ CAT0_TX_CLK/CATSYNC0/ QMI-A/QIO1-A/SDHI_D1-A/ MMC_D1-A/LCD_DATA15-A	PC4/A20/CS3#/MTIOC3D/ MTCLKC/TMCI1/PO25/ POE0#/GTETRGC/SCK5/ CTS8#/SS8#/SS10#/ CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK/QMI-A/QIO1-A/ SDHI_D1-A/MMC_D1-A/ LCD_DATA15-A	PC4/A20/CS3#/MTIOC3D/ MTCLKC/TMCI1/PO25/ POE0#/GTETRGC/SCK5/ CTS8#/SS8#/SS10#/ CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK/QMI-A/QIO1-A/ SDHI_D1-A/MMC_D1-A/ LCD_DATA15-A
P13	PC2/A18/MTIOC4B/TCLKA/ PO21/GTIOC2B/RXD5/ SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV/CAT0_RX_DV/ SDHI_D3-A/MMC_CD-A/ LCD_DATA19-A	PC2/A18/MTIOC4B/TCLKA/ PO21/GTIOC2B/RXD5/ SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV/SDHI_D3-A/ MMC_CD-A/LCD_DATA19-A	PC2/A18/MTIOC4B/TCLKA/ PO21/GTIOC2B/RXD5/ SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV/SDHI_D3-A/ MMC_CD-A/LCD_DATA19-A
P14	P75/CS5#/PO20/SCK11/ RTS11#/ET0_ERXD0/ RMII0_RXD0/CAT0_ERXD0/ SDHI_D2-A/MMC_RES#-A/ LCD_DATA20-A/DSMDAT2	P75/CS5#/PO20/SCK11/ RTS11#/ET0_ERXD0/ RMII0_RXD0/SDHI_D2-A/ MMC_RES#-A/ LCD_DATA20-A	P75/CS5#/PO20/SCK11/ RTS11#/ET0_ERXD0/ RMII0_RXD0/SDHI_D2-A/ MMC_RES#-A/ LCD_DATA20-A
P15	VCC	VCC	VCC
R1	P21/MTIOC1B/MTIOC4A/ TIOCA3/TMCI0/PO1/ GTIOC2A/RXD0/SMISO0/ SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/ SDHI_CLK-C/PIXD5/IRQ9	P21/MTIOC1B/MTIOC4A/ TIOCA3/TMCI0/PO1/ GTIOC2A/RXD0/SMISO0/ SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/ SDHI_CLK-C/PIXD5/IRQ9	P21/MTIOC1B/MTIOC4A/ TIOCA3/TMCI0/PO1/ GTIOC2A/RXD0/SMISO0/ SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/ SDHI_CLK-C/PIXD5/IRQ9
R2	P20/MTIOC1A/TIOCB3/ TMRI0/PO0/TXD0/SMOSI0/ SSDA0/SDA1/USB0_ID/ SSIRXD0/SDHI_CMD-C/ PIXD4/IRQ8	P20/MTIOC1A/TIOCB3/ TMRI0/PO0/TXD0/SMOSI0/ SSDA0/SDA1/USB0_ID/ SSIRXD0/SDHI_CMD-C/ PIXD4/IRQ8	P20/MTIOC1A/TIOCB3/ TMRI0/PO0/TXD0/SMOSI0/ SSDA0/SDA1/USB0_ID/ SSIRXD0/SDHI_CMD-C/ PIXD4/IRQ8
R3	P16/MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOUT/TXD1/ SMOSI1/SSDA1/RXD3/ SMISO3/SSCL3/SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB/IRQ6/ ADTRG0#	P16/MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOUT/TXD1/ SMOSI1/SSDA1/RXD3/ SMISO3/SSCL3/SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB/IRQ6/ ADTRG0#	P16/MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOUT/TXD1/ SMOSI1/SSDA1/RXD3/ SMISO3/SSCL3/SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB/IRQ6/ ADTRG0#
R4	P13/WR2#/BC2#/MTIOC0B/ TIOCA5/TMO3/PO13/ GTADSM1/TXD2/SMOSI2/ SSDA2/SDA0[FM+]/ LCD_TCON0-A/IRQ3/ ADTRG1#	P13/WR2#/BC2#/MTIOC0B/ TIOCA5/TMO3/PO13/ GTADSM1/TXD2/SMOSI2/ SSDA2/SDA0[FM+]/ LCD_TCON0-A/IRQ3/ ADTRG1#	P13/WR2#/BC2#/MTIOC0B/ TIOCA5/TMO3/PO13/ GTADSM1/TXD2/SMOSI2/ SSDA2/SDA0[FM+]/ LCD_TCON0-A/IRQ3/ ADTRG1#
R5	USB0_DM	USB0_DM	USB0_DM
R6	USB0_DP	USB0_DP	USB0_DP
R7	CLKOUT25M/P56/EDACK1/ MTIOC3C/TIOCA1/SCK7/ RSPCKC-B/LCD_DATA4-A/ DSMDAT1	CLKOUT25M/P56/EDACK1/ MTIOC3C/TIOCA1/SCK7/ RSPCKC-B/LCD_DATA4-A	CLKOUT25M/P56/EDACK1/ MTIOC3C/TIOCA1/SCK7/ RSPCKC-B/LCD_DATA4-A

176-Pin LFBGA	RX72M	RX72N	RX66N
R8	P11/MTIC5V/TMCI3/SCK2/ EPLSOUT1/CATSYNC1/ LCD_DATA7-A/IRQ1	P11/MTIC5V/TMCI3/SCK2/ EPLSOUT1/LCD_DATA7-A/ IRQ1	P11/MTIC5V/TMCI3/SCK2/ LCD_DATA7-A/IRQ1
R9	P53*1/BCLK	P53*1/BCLK	P53*1/BCLK
R10	VSS	VSS	VSS
R11	VCC	VCC	VCC
R12	P80/EDREQ0/MTIOC3B/ PO26/SCK10/RTS10#/ ET0_TX_EN/ RMII0_TXD_EN/ CAT0_TX_EN/CATLATCH0/ QIO2-A/SDHI_WP/ MMC_D2-A/LCD_DATA14-A	P80/EDREQ0/MTIOC3B/ PO26/SCK10/RTS10#/ ET0_TX_EN/ RMII0_TXD_EN/QIO2-A/ SDHI_WP/MMC_D2-A/ LCD_DATA14-A	P80/EDREQ0/MTIOC3B/ PO26/SCK10/RTS10#/ ET0_TX_EN/ RMII0_TXD_EN/QIO2-A/ SDHI_WP/MMC_D2-A/ LCD_DATA14-A
R13	P76/CS6#/PO22/SMISO11/ SSCL11/RXD11/ ET0_RX_CLK/REF50CK0/ CAT0_RX_CLK/QSSL-A/ SDHI_CMD-A/MMC_CMD-A/ LCD_DATA18-A	P76/CS6#/PO22/SMISO11/ SSCL11/RXD11/ ET0_RX_CLK/REF50CK0/ QSSL-A/SDHI_CMD-A/ MMC_CMD-A/ LCD_DATA18-A	P76/CS6#/PO22/SMISO11/ SSCL11/RXD11/ ET0_RX_CLK/REF50CK0/ QSSL-A/SDHI_CMD-A/ MMC_CMD-A/ LCD_DATA18-A
R14	P74/A20/CS4#/PO19/SS11#/ CTS11#/ET0_ERXD1/ RMII0_RXD1/CAT0_ERXD1/ LCD_DATA21-A/DSMCLK2	P74/A20/CS4#/PO19/SS11#/ CTS11#/ET0_ERXD1/ RMII0_RXD1/ LCD_DATA21-A	P74/A20/CS4#/PO19/SS11#/ CTS11#/ET0_ERXD1/ RMII0_RXD1/ LCD_DATA21-A
R15	PC1/A17/MTIOC3A/TCLKD/ PO18/SCK5/SSLA2-A/ ET0_ERXD2/CAT0_ERXD2/ LCD_DATA22-A/IRQ12	PC1/A17/MTIOC3A/TCLKD/ PO18/SCK5/SSLA2-A/ ET0_ERXD2/ LCD_DATA22-A/IRQ12	PC1/A17/MTIOC3A/TCLKD/ PO18/SCK5/SSLA2-A/ ET0_ERXD2/ LCD_DATA22-A/IRQ12

Note: 1. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.

3.3 176-Pin LFQFP Package

Table 3.3 is a comparative listing of the pin functions of 176-pin LFQFP package products.

Table 3.3 Comparative Listing of 176-Pin LFQFP Package Pin Functions

176-Pin LFQFP	RX72M	RX72N	RX66N
1	AVSS0	AVSS0	AVSS0
2	P05/SSILRCK1/IRQ13/DA1	P05/SSILRCK1/IRQ13/DA1	P05/SSILRCK1/IRQ13/DA1
3	AVCC1	AVCC1	AVCC1
4	P03/SSIDATA1/IRQ11/DA0	P03/SSIDATA1/IRQ11/DA0	P03/SSIDATA1/IRQ11/DA0
5	AVSS1	AVSS1	AVSS1
6	P02/TMCI1/SCK6/SSIBCK1/ CATLEDSTER/IRQ10/AN120	P02/TMCI1/SCK6/SSIBCK1/ IRQ10/AN120	P02/TMCI1/SCK6/SSIBCK1/ IRQ10/AN120
7	P01/TMCI0/RXD6/SMISO6/ SSCL6/SSIBCK0/ CATLEDERR/IRQ9/AN119	P01/TMCI0/RXD6/SMISO6/ SSCL6/SSIBCK0/IRQ9/ AN119	P01/TMCI0/RXD6/SMISO6/ SSCL6/SSIBCK0/IRQ9/ AN119
8	P00/TMRI0/TXD6/SMOSI6/ SSDA6/AUDIO_CLK/ CATLATCH1/IRQ8/AN118	P00/TMRI0/TXD6/SMOSI6/ SSDA6/AUDIO_CLK/IRQ8/ AN118	P00/TMRI0/TXD6/SMOSI6/ SSDA6/AUDIO_CLK/IRQ8/ AN118
9	PF5/WAIT#/SSILRCK0/ CATLATCH0/IRQ4	PF5/WAIT#/SSILRCK0/IRQ4	PF5/WAIT#/SSILRCK0/IRQ4
10	EMLE	EMLE	EMLE
11	PJ5/POE8#/CTS2#/RTS2#/ SS2#/SSIRXD0/EPLSOUT0/ CATSYNC0	PJ5/POE8#/CTS2#/RTS2#/ SS2#/SSIRXD0/EPLSOUT0	PJ5/POE8#/CTS2#/RTS2#/ SS2#/SSIRXD0
12	VSS	VSS	VSS
13	PJ3/EDACK1/MTIOC3C/ CTS6#/RTS6#/SS6#/CTS0#/ RTS0#/SS0#/SSITXD0/ ET0_EXOUT/CATRESTOUT	PJ3/EDACK1/MTIOC3C/ CTS6#/RTS6#/SS6#/CTS0#/ RTS0#/SS0#/SSITXD0/ ET0_EXOUT	PJ3/EDACK1/MTIOC3C/ CTS6#/RTS6#/SS6#/CTS0#/ RTS0#/SS0#/SSITXD0/ ET0_EXOUT
14	VCL	VCL	VCL
15	VBATT	VBATT	VBATT
16	NC	NC	NC
17	TRST#/PF4	TRST#/PF4	TRST#/PF4
18	MD/FINED	MD/FINED	MD/FINED
19	XCIN	XCIN	XCIN
20	XCOUT	XCOUT	XCOUT
21	RES#	RES#	RES#
22	XTAL/P37	XTAL/P37	XTAL/P37
23	VSS	VSS	VSS
24	EXTAL/P36	EXTAL/P36	EXTAL/P36
25	VCC	VCC	VCC
26	UPSEL/P35/NMI	UPSEL/P35/NMI	UPSEL/P35/NMI
27	P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/ ET0_LINKSTA/ CAT0_LINKSTA/IRQ4/ DSMDAT0	P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/ ET0_LINKSTA/IRQ4	P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/ ET0_LINKSTA/IRQ4

176-Pin LFQFP	RX72M	RX72N	RX66N
28	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/POE4#/POE11#/RXD6/SMISO6/SSCL6/RXD0/SMISO0/SSCL0/CRX0/PCKO/IRQ3-DS/DSMCLK0	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/POE4#/POE11#/RXD6/SMISO6/SSCL6/RXD0/SMISO0/SSCL0/CRX0/PCKO/IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/POE4#/POE11#/RXD6/SMISO6/SSCL6/RXD0/SMISO0/SSCL0/CRX0/PCKO/IRQ3-DS
29	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCIC2/RTCOUT/POE0#/POE10#/TXD6/SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCIC2/RTCOUT/POE0#/POE10#/TXD6/SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCIC2/RTCOUT/POE0#/POE10#/TXD6/SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS
30	TMS/PF3	TMS/PF3	TMS/PF3
31	TDI/PF2/RXD1/SMISO1/SSCL1/CATI2CCLK	TDI/PF2/RXD1/SMISO1/SSCL1	TDI/PF2/RXD1/SMISO1/SSCL1
32	P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/ET1_MDC/PMGI1_MDC/IRQ1-DS	P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/ET1_MDC/PMGI1_MDC/IRQ1-DS	P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS
33	P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ET1_MDIO/PMGI1_MDIO/IRQ0-DS	P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ET1_MDIO/PMGI1_MDIO/IRQ0-DS	P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS
34	TCK/PF1/SCK1	TCK/PF1/SCK1	TCK/PF1/SCK1
35	TDO/PF0/TXD1/SMOSI1/SSDA1/CATI2CDATA	TDO/PF0/TXD1/SMOSI1/SSDA1	TDO/PF0/TXD1/SMOSI1/SSDA1
36	P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB-A/ET1_WOL/CATIRQ	P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB-A/ET1_WOL	P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB-A
37	P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/MOSIB-A/ET1_EXOUT/CATLINKACT1	P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/MOSIB-A/ET1_EXOUT	P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/MOSIB-A
38	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/SSIDATA1/SDHI_CD/HSYNC/ADTRG0#	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/SSIDATA1/SDHI_CD/HSYNC/ADTRG0#	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/SSIDATA1/SDHI_CD/HSYNC/ADTRG0#
39	VCC	VCC	VCC
40	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/SSIBCK1/SDHI_WP/PIXCLK	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/SSIBCK1/SDHI_WP/PIXCLK	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/SSIBCK1/SDHI_WP/PIXCLK
41	VSS	VSS	VSS

176-Pin LFQFP	RX72M	RX72N	RX66N
42	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/GTIOC0A/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/SS0#/CTX1/SSIBCK0/SDHI_D1-C/PIXD7	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/GTIOC0A/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/SS0#/CTX1/SSIBCK0/SDHI_D1-C/PIXD7	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/GTIOC0A/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/SS0#/CTX1/SSIBCK0/SDHI_D1-C/PIXD7
43	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/GTIOC1A/SCK0/USB0_OVRCURB/AUDIO_CLK/SDHI_D0-C/PIXD6	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/GTIOC1A/SCK0/USB0_OVRCURB/AUDIO_CLK/SDHI_D0-C/PIXD6	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/GTIOC1A/SCK0/USB0_OVRCURB/AUDIO_CLK/SDHI_D0-C/PIXD6
44	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/GTIOC2A/RXD0/SMISO0/SSCL0/SCL1/USB0_EXICEN/SSILRCK0/SDHI_CLK-C/PIXD5/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/GTIOC2A/RXD0/SMISO0/SSCL0/SCL1/USB0_EXICEN/SSILRCK0/SDHI_CLK-C/PIXD5/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/GTIOC2A/RXD0/SMISO0/SSCL0/SCL1/USB0_EXICEN/SSILRCK0/SDHI_CLK-C/PIXD5/IRQ9
45	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/SDHI_CMD-C/PIXD4/IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/SDHI_CMD-C/PIXD4/IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/SDHI_CMD-C/PIXD4/IRQ8
46	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/GTIOC0B/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/SSITXD0/EPLSOUT0/CATSYNC0/SDHI_D3-C/PIXD3/IRQ7/ADTRG1#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/GTIOC0B/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/SSITXD0/EPLSOUT0/SDHI_D3-C/PIXD3/IRQ7/ADTRG1#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/GTIOC0B/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/SSITXD0/SDHI_D3-C/PIXD3/IRQ7/ADTRG1#
47	P87/MTIOC4C/TIOCA2/GTIOC1B/SMOSI10/SSDA10/TXD10/EPLSOUT1/CATSYNC1/SDHI_D2-C/PIXD2	P87/MTIOC4C/TIOCA2/GTIOC1B/SMOSI10/SSDA10/TXD10/EPLSOUT1/SDHI_D2-C/PIXD2	P87/MTIOC4C/TIOCA2/GTIOC1B/SMOSI10/SSDA10/TXD10/SDHI_D2-C/PIXD2
48	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/SMOSI1/SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/USB0_VBUSEN/USB0_VBUS/USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/SMOSI1/SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/USB0_VBUSEN/USB0_VBUS/USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/SMOSI1/SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/USB0_VBUSEN/USB0_VBUS/USB0_OVRCURB/IRQ6/ADTRG0#
49	P86/MTIOC4D/TIOCA0/GTIOC2B/SMISO10/SSCL10/RXD10/CATLINKACT0/PIXD1	P86/MTIOC4D/TIOCA0/GTIOC2B/SMISO10/SSCL10/RXD10/PIXD1	P86/MTIOC4D/TIOCA0/GTIOC2B/SMISO10/SSCL10/RXD10/PIXD1
50	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/GTETRGA/RXD1/SMISO1/SSCL1/SCK3/CRX1-DS/SSILRCK1/CATLEDRUN/PIXD0/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/GTETRGA/RXD1/SMISO1/SSCL1/SCK3/CRX1-DS/SSILRCK1/PIXD0/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/GTETRGA/RXD1/SMISO1/SSCL1/SCK3/CRX1-DS/SSILRCK1/PIXD0/IRQ5

176-Pin LFQFP	RX72M	RX72N	RX66N
51	P14/MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15/GTETRGD/CTS1#/ RTS1#/SS1#/CTX1/ USB0_OVRCURA/ LCD_CLK-A/IRQ4	P14/MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15/GTETRGD/CTS1#/ RTS1#/SS1#/CTX1/ USB0_OVRCURA/ LCD_CLK-A/IRQ4	P14/MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15/GTETRGD/CTS1#/ RTS1#/SS1#/CTX1/ USB0_OVRCURA/ LCD_CLK-A/IRQ4
52	P13/WR2#/BC2#/MTIOC0B/ TIOCA5/TMO3/PO13/ GTADSM1/TXD2/SMOSI2/ SSDA2/SDA0[FM+]/ LCD_TCON0-A/IRQ3/ ADTRG1#	P13/WR2#/BC2#/MTIOC0B/ TIOCA5/TMO3/PO13/ GTADSM1/TXD2/SMOSI2/ SSDA2/SDA0[FM+]/ LCD_TCON0-A/IRQ3/ ADTRG1#	P13/WR2#/BC2#/MTIOC0B/ TIOCA5/TMO3/PO13/ GTADSM1/TXD2/SMOSI2/ SSDA2/SDA0[FM+]/ LCD_TCON0-A/IRQ3/ ADTRG1#
53	P12/WR3#/BC3#/MTIC5U/ TMCI1/GTADSM0/RXD2/ SMISO2/SSCL2/SCL0[FM+]/ LCD_TCON1-A/IRQ2	P12/WR3#/BC3#/MTIC5U/ TMCI1/GTADSM0/RXD2/ SMISO2/SSCL2/SCL0[FM+]/ LCD_TCON1-A/IRQ2	P12/WR3#/BC3#/MTIC5U/ TMCI1/GTADSM0/RXD2/ SMISO2/SSCL2/SCL0[FM+]/ LCD_TCON1-A/IRQ2
54	VCC_USB	VCC_USB	VCC_USB
55	USB0_DM	USB0_DM	USB0_DM
56	USB0_DP	USB0_DP	USB0_DP
57	VSS_USB	VSS_USB	VSS_USB
58	CLKOUT25M/PJ2/TXD8/ SMOSI8/SSDA8/SSLC3-B/ LCD_TCON2-A	CLKOUT25M/PJ2/TXD8/ SMOSI8/SSDA8/SSLC3-B/ LCD_TCON2-A	CLKOUT25M/PJ2/TXD8/ SMOSI8/SSDA8/SSLC3-B/ LCD_TCON2-A
59	PJ1/MTIOC6A/RXD8/ SMISO8/SSCL8/SSLC2-B/ EPLSOUT1/CATSYNC1/ LCD_TCON3-A	PJ1/MTIOC6A/RXD8/ SMISO8/SSCL8/SSLC2-B/ EPLSOUT1/LCD_TCON3-A	PJ1/MTIOC6A/RXD8/ SMISO8/SSCL8/SSLC2-B/ LCD_TCON3-A
60	PJ0/MTIOC6B/SCK8/ SSLC1-B/EPLSOUT0/ CATSYNC0/LCD_DATA0-A	PJ0/MTIOC6B/SCK8/ SSLC1-B/EPLSOUT0/ LCD_DATA0-A	PJ0/MTIOC6B/SCK8/ SSLC1-B/LCD_DATA0-A
61	P85/MTIOC6C/TIOCC0/ LCD_DATA1-A	P85/MTIOC6C/TIOCC0/ LCD_DATA1-A	P85/MTIOC6C/TIOCC0/ LCD_DATA1-A
62	P84/MTIOC6D/ ET1_LINKSTA/ CAT1_LINKSTA/ LCD_DATA2-A	P84/MTIOC6D/ ET1_LINKSTA/ LCD_DATA2-A	P84/MTIOC6D/ LCD_DATA2-A
63	P57/RXD7/SMISO7/SSCL7/ SSLC0-B/LCD_DATA3-A	P57/RXD7/SMISO7/SSCL7/ SSLC0-B/LCD_DATA3-A	P57/RXD7/SMISO7/SSCL7/ SSLC0-B/LCD_DATA3-A
64	CLKOUT25M/P56/EDACK1/ MTIOC3C/TIOCA1/SCK7/ RSPCKC-B/LCD_DATA4-A/ DSMDAT1	CLKOUT25M/P56/EDACK1/ MTIOC3C/TIOCA1/SCK7/ RSPCKC-B/LCD_DATA4-A	CLKOUT25M/P56/EDACK1/ MTIOC3C/TIOCA1/SCK7/ RSPCKC-B/LCD_DATA4-A
65	P55/D0[A0/D0]/EDREQ0/ WAIT#/MTIOC4D/TMO3/ TXD7/SMOSI7/SSDA7/ MISOC-B/CRX1/ ET0_EXOUT/LCD_DATA5-A/ IRQ10	P55/D0[A0/D0]/EDREQ0/ WAIT#/MTIOC4D/TMO3/ TXD7/SMOSI7/SSDA7/ MISOC-B/CRX1/ ET0_EXOUT/LCD_DATA5-A/ IRQ10	P55/D0[A0/D0]/EDREQ0/ WAIT#/MTIOC4D/TMO3/ TXD7/SMOSI7/SSDA7/ MISOC-B/CRX1/ ET0_EXOUT/LCD_DATA5-A/ IRQ10

176-Pin LFQFP	RX72M	RX72N	RX66N
66	P54/D1[A1/D1]/EDACK0/ ALE/MTIOC4B/TMCI1/ CTS2#/RTS2#/SS2#/ MOSIC-B/CTX1/ ET0_LINKSTA/ CAT0_LINKSTA/ LCD_DATA6-A	P54/D1[A1/D1]/EDACK0/ ALE/MTIOC4B/TMCI1/ CTS2#/RTS2#/SS2#/ MOSIC-B/CTX1/ ET0_LINKSTA/ LCD_DATA6-A	P54/D1[A1/D1]/EDACK0/ ALE/MTIOC4B/TMCI1/ CTS2#/RTS2#/SS2#/ MOSIC-B/CTX1/ ET0_LINKSTA/ LCD_DATA6-A
67	P11/MTIC5V/TMCI3/SCK2/ EPLSOUT1/CATSYNC1/ LCD_DATA7-A/IRQ1	P11/MTIC5V/TMCI3/SCK2/ EPLSOUT1/LCD_DATA7-A/ IRQ1	P11/MTIC5V/TMCI3/SCK2/ LCD_DATA7-A/IRQ1
68	P10/ALE/MTIC5W/TMRI3/I RQ0	P10/ALE/MTIC5W/TMRI3/ IRQ0	P10/ALE/MTIC5W/TMRI3/ IRQ0
69	P53*[1]/BCLK	P53*[1]/BCLK	P53*[1]/BCLK
70	P52/RD#/RXD2/SMISO2/ SSCL2/SSLB3-A/ CATLEDSTER	P52/RD#/RXD2/SMISO2/ SSCL2/SSLB3-A	P52/RD#/RXD2/SMISO2/ SSCL2/SSLB3-A
71	P51/WR1#/BC1#/WAIT#/ SCK2/SSLB2-A	P51/WR1#/BC1#/WAIT#/ SCK2/SSLB2-A	P51/WR1#/BC1#/WAIT#/ SCK2/SSLB2-A
72	P50/WR0#/WR#/TXD2/ SMOSI2/SSDA2/SSLB1-A/ CATLEDERR	P50/WR0#/WR#/TXD2/ SMOSI2/SSDA2/SSLB1-A	P50/WR0#/WR#/TXD2/ SMOSI2/SSDA2/SSLB1-A
73	VSS	VSS	VSS
74	P83/EDACK1/MTIOC4C/ GTIOC0A/SCK10/SS10#/ CTS10#/ET0_CRS/ RMII0_CRS_DV/ CAT0_RX_DV/ LCD_DATA8-A/DSMCLK1	P83/EDACK1/MTIOC4C/ GTIOC0A/SCK10/SS10#/ CTS10#/ET0_CRS/ RMII0_CRS_DV/ LCD_DATA8-A	P83/EDACK1/MTIOC4C/ GTIOC0A/SCK10/SS10#/ CTS10#/ET0_CRS/ RMII0_CRS_DV/ LCD_DATA8-A
75	VCC	VCC	VCC
76	UB/PC7/A23/CS0#/ MTIOC3A/MTCLKB/TMO2/ PO31/TOC0/CACREF/ GTIOC3A/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/ET0_COL/ MMC_D7-A/LCD_DATA9-A/ IRQ14	UB/PC7/A23/CS0#/ MTIOC3A/MTCLKB/TMO2/ PO31/TOC0/CACREF/ GTIOC3A/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/ET0_COL/ MMC_D7-A/LCD_DATA9-A/ IRQ14	UB/PC7/A23/CS0#/ MTIOC3A/MTCLKB/TMO2/ PO31/TOC0/CACREF/ GTIOC3A/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/ET0_COL/ MMC_D7-A/LCD_DATA9-A/ IRQ14
77	PC6/D2[A2/D2]/A22/CS1#/ MTIOC3C/MTCLKA/TMCI2/ PO30/TIC0/GTIOC3B/RXD8/ SMISO8/SSCL8/SMISO10/ SSCL10/RXD10/MOSIA-A/ ET0_ETXD3/CAT0_ETXD3/ CATLATCH1/MMC_D6-A/ LCD_DATA10-A/IRQ13	PC6/D2[A2/D2]/A22/CS1#/ MTIOC3C/MTCLKA/TMCI2/ PO30/TIC0/GTIOC3B/RXD8/ SMISO8/SSCL8/SMISO10/ SSCL10/RXD10/MOSIA-A/ ET0_ETXD3/MMC_D6-A/ LCD_DATA10-A/IRQ13	PC6/D2[A2/D2]/A22/CS1#/ MTIOC3C/MTCLKA/TMCI2/ PO30/TIC0/GTIOC3B/RXD8/ SMISO8/SSCL8/SMISO10/ SSCL10/RXD10/MOSIA-A/ ET0_ETXD3/MMC_D6-A/ LCD_DATA10-A/IRQ13
78	PC5/D3[A3/D3]/A21/CS2#/ WAIT#/MTIOC3B/MTCLKD/ TMRI2/PO29/GTIOC1A/ SCK8/RTS8#/SCK10/ RSPCKA-A/ET0_ETXD2/ CAT0_ETXD2/MMC_D5-A/ LCD_DATA11-A	PC5/D3[A3/D3]/A21/CS2#/ WAIT#/MTIOC3B/MTCLKD/ TMRI2/PO29/GTIOC1A/ SCK8/RTS8#/SCK10/ RSPCKA-A/ET0_ETXD2/ MMC_D5-A/LCD_DATA11-A	PC5/D3[A3/D3]/A21/CS2#/ WAIT#/MTIOC3B/MTCLKD/ TMRI2/PO29/GTIOC1A/ SCK8/RTS8#/SCK10/ RSPCKA-A/ET0_ETXD2/ MMC_D5-A/LCD_DATA11-A

176-Pin LFQFP	RX72M	RX72N	RX66N
79	P82/EDREQ1/MTIOC4A/ PO28/GTIOC2A/SMOSI10/ SSDA10/TXD10/ ET0_ETXD1/RMII0_TXD1/ CAT0_ETXD1/CATI2CDATA/ MMC_D4-A/LCD_DATA12-A	P82/EDREQ1/MTIOC4A/ PO28/GTIOC2A/SMOSI10/ SSDA10/TXD10/ ET0_ETXD1/RMII0_TXD1/ MMC_D4-A/LCD_DATA12-A	P82/EDREQ1/MTIOC4A/ PO28/GTIOC2A/SMOSI10/ SSDA10/TXD10/ ET0_ETXD1/RMII0_TXD1/ MMC_D4-A/LCD_DATA12-A
80	P81/EDACK0/MTIOC3D/ PO27/GTIOC0B/SMISO10/ SSCL10/RXD10/ ET0_ETXD0/RMII0_TXD0/ CAT0_ETXD0/CATI2CCLK/ QIO3-A/SDHI_CD/ MMC_D3-A/LCD_DATA13-A	P81/EDACK0/MTIOC3D/ PO27/GTIOC0B/SMISO10/ SSCL10/RXD10/ ET0_ETXD0/RMII0_TXD0/ QIO3-A/SDHI_CD/ MMC_D3-A/LCD_DATA13-A	P81/EDACK0/MTIOC3D/ PO27/GTIOC0B/SMISO10/ SSCL10/RXD10/ ET0_ETXD0/RMII0_TXD0/ QIO3-A/SDHI_CD/ MMC_D3-A/LCD_DATA13-A
81	P80/EDREQ0/MTIOC3B/ PO26/SCK10/RTS10#/ ET0_TX_EN/ RMII0_TXD_EN/ CAT0_TX_EN/CATLATCH0/ QIO2-A/SDHI_WP/ MMC_D2-A/LCD_DATA14-A	P80/EDREQ0/MTIOC3B/ PO26/SCK10/RTS10#/ ET0_TX_EN/ RMII0_TXD_EN/QIO2-A/ SDHI_WP/MMC_D2-A/ LCD_DATA14-A	P80/EDREQ0/MTIOC3B/ PO26/SCK10/RTS10#/ ET0_TX_EN/ RMII0_TXD_EN/QIO2-A/ SDHI_WP/MMC_D2-A/ LCD_DATA14-A
82	PC4/A20/CS3#/MTIOC3D/ MTCLKC/TMCI1/PO25/ POE0#/GTETRGC/SCK5/ CTS8#/SS8#/SS10#/ CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK/ CAT0_TX_CLK/CATSYNC0/ QMI-A/QIO1-A/SDHI_D1-A/ MMC_D1-A/LCD_DATA15-A	PC4/A20/CS3#/MTIOC3D/ MTCLKC/TMCI1/PO25/ POE0#/GTETRGC/SCK5/ CTS8#/SS8#/SS10#/ CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK/QMI-A/ QIO1-A/SDHI_D1-A/ MMC_D1-A/LCD_DATA15-A	PC4/A20/CS3#/MTIOC3D/ MTCLKC/TMCI1/PO25/ POE0#/GTETRGC/SCK5/ CTS8#/SS8#/SS10#/ CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK/QMI-A/ QIO1-A/SDHI_D1-A/ MMC_D1-A/LCD_DATA15-A
83	PC3/A19/MTIOC4D/TCLKB/ PO24/GTIOC1B/TXD5/ SMOSI5/SSDA5/ ET0_TX_ER/QMO-A/ QIO0-A/SDHI_D0-A/ MMC_D0-A/LCD_DATA16-A	PC3/A19/MTIOC4D/TCLKB/ PO24/GTIOC1B/TXD5/ SMOSI5/SSDA5/ ET0_TX_ER/QMO-A/ QIO0-A/SDHI_D0-A/ MMC_D0-A/LCD_DATA16-A	PC3/A19/MTIOC4D/TCLKB/ PO24/GTIOC1B/TXD5/ SMOSI5/SSDA5/ ET0_TX_ER/QMO-A/ QIO0-A/SDHI_D0-A/ MMC_D0-A/LCD_DATA16-A
84	P77/CS7#/PO23/SMOSI11/ SSDA11/TXD11/ ET0_RX_ER/RMII0_RX_ER/ CAT0_RX_ER/QSPCLK-A/ SDHI_CLK-A/MMC_CLK-A/ LCD_DATA17-A	P77/CS7#/PO23/SMOSI11/ SSDA11/TXD11/ ET0_RX_ER/RMII0_RX_ER/ QSPCLK-A/SDHI_CLK-A/ MMC_CLK-A/ LCD_DATA17-A	P77/CS7#/PO23/SMOSI11/ SSDA11/TXD11/ ET0_RX_ER/RMII0_RX_ER/ QSPCLK-A/SDHI_CLK-A/ MMC_CLK-A/ LCD_DATA17-A
85	P76/CS6#/PO22/SMISO11/ SSCL11/RXD11/ ET0_RX_CLK/REF50CK0/ CAT0_RX_CLK/QSSL-A/ SDHI_CMD-A/MMC_CMD-A/ LCD_DATA18-A	P76/CS6#/PO22/SMISO11/ SSCL11/RXD11/ ET0_RX_CLK/REF50CK0/ QSSL-A/SDHI_CMD-A/ MMC_CMD-A/ LCD_DATA18-A	P76/CS6#/PO22/SMISO11/ SSCL11/RXD11/ ET0_RX_CLK/REF50CK0/ QSSL-A/SDHI_CMD-A/ MMC_CMD-A/ LCD_DATA18-A
86	PC2/A18/MTIOC4B/TCLKA/ PO21/GTIOC2B/RXD5/ SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV/CAT0_RX_DV/ SDHI_D3-A/MMC_CD-A/ LCD_DATA19-A	PC2/A18/MTIOC4B/TCLKA/ PO21/GTIOC2B/RXD5/ SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV/SDHI_D3-A/ MMC_CD-A/LCD_DATA19-A	PC2/A18/MTIOC4B/TCLKA/ PO21/GTIOC2B/RXD5/ SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV/SDHI_D3-A/ MMC_CD-A/LCD_DATA19-A

176-Pin LFQFP	RX72M	RX72N	RX66N
87	P75/CS5#/PO20/SCK11/ RTS11#/ET0_ERXD0/ RMII0_RXD0/CAT0_ERXD0/ SDHI_D2-A/MMC_RES#-A/ LCD_DATA20-A/DSMDAT2	P75/CS5#/PO20/SCK11/ RTS11#/ET0_ERXD0/ RMII0_RXD0/SDHI_D2-A/ MMC_RES#-A/ LCD_DATA20-A	P75/CS5#/PO20/SCK11/ RTS11#/ET0_ERXD0/ RMII0_RXD0/SDHI_D2-A/ MMC_RES#-A/ LCD_DATA20-A
88	P74/A20/CS4#/PO19/SS11#/ CTS11#/ET0_ERXD1/ RMII0_RXD1/CAT0_ERXD1/ LCD_DATA21-A/DSMCLK2	P74/A20/CS4#/PO19/SS11#/ CTS11#/ET0_ERXD1/ RMII0_RXD1/ LCD_DATA21-A	P74/A20/CS4#/PO19/SS11#/ CTS11#/ET0_ERXD1/ RMII0_RXD1/ LCD_DATA21-A
89	PC1/A17/MTIOC3A/TCLKD/ PO18/SCK5/SSLA2-A/ ET0_ERXD2/CAT0_ERXD2/ LCD_DATA22-A/IRQ12	PC1/A17/MTIOC3A/TCLKD/ PO18/SCK5/SSLA2-A/ ET0_ERXD2/ LCD_DATA22-A/IRQ12	PC1/A17/MTIOC3A/TCLKD/ PO18/SCK5/SSLA2-A/ ET0_ERXD2/ LCD_DATA22-A/IRQ12
90	VCC	VCC	VCC
91	PC0/A16/MTIOC3C/TCLKC/ PO17/CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3/ CAT0_ERXD3/IRQ14	PC0/A16/MTIOC3C/TCLKC/ PO17/CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3/IRQ14	PC0/A16/MTIOC3C/TCLKC/ PO17/CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3/IRQ14
92	VSS	VSS	VSS
93	P73/CS3#/PO16/ET0_WOL/ LCD_EXTCLK-A	P73/CS3#/PO16/ET0_WOL/ LCD_EXTCLK-A	P73/CS3#/PO16/ET0_WOL/ LCD_EXTCLK-A
94	PB7/A15/MTIOC3B/TIOCB5/ PO31/TXD9/SMOSI9/ SSDA9/SMOSI11/SSDA11/ TXD11/ET0_CRS/ RMII0_CRS_DV/ CAT0_RX_DV	PB7/A15/MTIOC3B/TIOCB5/ PO31/TXD9/SMOSI9/ SSDA9/SMOSI11/SSDA11/ TXD11/ET0_CRS/ RMII0_CRS_DV	PB7/A15/MTIOC3B/TIOCB5/ PO31/TXD9/SMOSI9/ SSDA9/SMOSI11/SSDA11/ TXD11/ET0_CRS/ RMII0_CRS_DV
95	PB6/A14/MTIOC3D/TIOCA5/ PO30/RXD9/SMISO9/SSCL9/ SMISO11/SSCL11/RXD11/ ET0_ETXD1/RMII0_TXD1/ CAT0_ETXD1	PB6/A14/MTIOC3D/TIOCA5/ PO30/RXD9/SMISO9/SSCL9/ SMISO11/SSCL11/RXD11/ ET0_ETXD1/RMII0_TXD1	PB6/A14/MTIOC3D/TIOCA5/ PO30/RXD9/SMISO9/SSCL9/ SMISO11/SSCL11/RXD11/ ET0_ETXD1/RMII0_TXD1
96	PB5/A13/MTIOC2A/ MTIOC1B/TIOCB4/TMRI1/ PO29/POE4#/SCK9/RTS9#/ SCK11/ET0_ETXD0/ RMII0_TXD0/CAT0_ETXD0/ LCD_CLK-B	PB5/A13/MTIOC2A/ MTIOC1B/TIOCB4/TMRI1/ PO29/POE4#/SCK9/RTS9#/ SCK11/ET0_ETXD0/ RMII0_TXD0/LCD_CLK-B	PB5/A13/MTIOC2A/ MTIOC1B/TIOCB4/TMRI1/ PO29/POE4#/SCK9/RTS9#/ SCK11/ET0_ETXD0/ RMII0_TXD0/LCD_CLK-B
97	PB4/A12/TIOCA4/PO28/ CTS9#/SS9#/SS11#/ CTS11#/RTS11#/ ET0_TX_EN/ RMII0_TXD_EN/ CAT0_TX_EN/ LCD_TCON0-B	PB4/A12/TIOCA4/PO28/ CTS9#/SS9#/SS11#/ CTS11#/RTS11#/ ET0_TX_EN/ RMII0_TXD_EN/ LCD_TCON0-B	PB4/A12/TIOCA4/PO28/ CTS9#/SS9#/SS11#/ CTS11#/RTS11#/ ET0_TX_EN/ RMII0_TXD_EN/ LCD_TCON0-B
98	PB3/A11/MTIOC0A/ MTIOC4A/TIOCD3/TCLKD/ TMO0/PO27/POE11#/SCK4/ SCK6/ET0_RX_ER/ RMII0_RX_ER/ CAT0_RX_ER/ LCD_TCON1-B	PB3/A11/MTIOC0A/ MTIOC4A/TIOCD3/TCLKD/ TMO0/PO27/POE11#/SCK4/ SCK6/ET0_RX_ER/ RMII0_RX_ER/ LCD_TCON1-B	PB3/A11/MTIOC0A/ MTIOC4A/TIOCD3/TCLKD/ TMO0/PO27/POE11#/SCK4/ SCK6/ET0_RX_ER/ RMII0_RX_ER/ LCD_TCON1-B

176-Pin LFQFP	RX72M	RX72N	RX66N
99	PB2/A10/TIOCC3/TCLKC/ PO26/CTS4#/RTS4#/SS4#/ CTS6#/RTS6#/SS6#/ ET0_RX_CLK/REF50CK0/ CAT0_RX_CLK/ LCD_TCON2-B	PB2/A10/TIOCC3/TCLKC/ PO26/CTS4#/RTS4#/SS4#/ CTS6#/RTS6#/SS6#/ ET0_RX_CLK/REF50CK0/ LCD_TCON2-B	PB2/A10/TIOCC3/TCLKC/ PO26/CTS4#/RTS4#/SS4#/ CTS6#/RTS6#/SS6#/ ET0_RX_CLK/REF50CK0/ LCD_TCON2-B
100	PB1/A9/MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25/TXD4/ SMOSI4/SSDA4/TXD6/ SMOSI6/SSDA6/ ET0_ERXD0/RMII0_RXD0/ CAT0_ERXD0/ LCD_TCON3-B/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25/TXD4/ SMOSI4/SSDA4/TXD6/ SMOSI6/SSDA6/ ET0_ERXD0/RMII0_RXD0/ LCD_TCON3-B/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25/TXD4/ SMOSI4/SSDA4/TXD6/ SMOSI6/SSDA6/ ET0_ERXD0/RMII0_RXD0/ LCD_TCON3-B/IRQ4-DS
101	P72/A19/CS2#/ET0_MDC/ CAT0_MDC/PMGI0_MDC/ LCD_DATA23-A/DSMDAT3	P72/A19/CS2#/ET0_MDC/ PMGI0_MDC/ LCD_DATA23-A	P72/A19/CS2#/ET0_MDC/ PMGI0_MDC/ LCD_DATA23-A
102	P71/A18/CS1#/ET0_MDIO/ CAT0_MDIO/PMGI0_MDIO/ DSMCLK3	P71/A18/CS1#/ET0_MDIO/ PMGI0_MDIO	P71/A18/CS1#/ET0_MDIO/ PMGI0_MDIO
103	VCC	VCC	VCC
104	PB0/A8/MTIC5W/TIOCA3/ PO24/RXD4/SMISO4/SSCL4/ RXD6/SMISO6/SSCL6/ ET0_ERXD1/RMII0_RXD1/ CAT0_ERXD1/ LCD_DATA0-B/IRQ12	PB0/A8/MTIC5W/TIOCA3/ PO24/RXD4/SMISO4/SSCL4/ RXD6/SMISO6/SSCL6/ ET0_ERXD1/RMII0_RXD1/ LCD_DATA0-B/IRQ12	PB0/A8/MTIC5W/TIOCA3/ PO24/RXD4/SMISO4/SSCL4/ RXD6/SMISO6/SSCL6/ ET0_ERXD1/RMII0_RXD1/ LCD_DATA0-B/IRQ12
105	VSS	VSS	VSS
106	PA7/A7/TIOCB2/PO23/ MISOA-B/ET0_WOL/ LCD_DATA1-B	PA7/A7/TIOCB2/PO23/ MISOA-B/ET0_WOL/ LCD_DATA1-B	PA7/A7/TIOCB2/PO23/ MISOA-B/ET0_WOL/ LCD_DATA1-B
107	PA6/A6/MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE10#/GTETRGB/CTS5#/ RTS5#/SS5#/MOSIA-B/ ET0_EXOUT/CATRESTOUT/ LCD_DATA2-B	PA6/A6/MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE10#/GTETRGB/CTS5#/ RTS5#/SS5#/MOSIA-B/ ET0_EXOUT/LCD_DATA2-B	PA6/A6/MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE10#/GTETRGB/CTS5#/ RTS5#/SS5#/MOSIA-B/ ET0_EXOUT/LCD_DATA2-B
108	PA5/A5/MTIOC6B/TIOCB1/ PO21/GTIOC0A/RSPCKA-B/ ET0_LINKSTA/ CAT0_LINKSTA/ LCD_DATA3-B	PA5/A5/MTIOC6B/TIOCB1/ PO21/GTIOC0A/RSPCKA-B/ ET0_LINKSTA/ LCD_DATA3-B	PA5/A5/MTIOC6B/TIOCB1/ PO21/GTIOC0A/RSPCKA-B/ ET0_LINKSTA/ LCD_DATA3-B
109	PA4/A4/MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20/TXD5/ SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/CAT0_MDC/ CATIRQ/PMGI0_MDC/ LCD_DATA4-B/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20/TXD5/ SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/PMGI0_MDC/ LCD_DATA4-B/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20/TXD5/ SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/PMGI0_MDC/ LCD_DATA4-B/IRQ5-DS
110	PA3/A3/MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19/ RXD5/SMISO5/SSCL5/ ET0_MDIO/CAT0_MDIO/ PMGI0_MDIO/ LCD_DATA5-B/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19/ RXD5/SMISO5/SSCL5/ ET0_MDIO/PMGI0_MDIO/ LCD_DATA5-B/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19/ RXD5/SMISO5/SSCL5/ ET0_MDIO/PMGI0_MDIO/ LCD_DATA5-B/IRQ6-DS

176-Pin LFQFP	RX72M	RX72N	RX66N
111	TRDATA3/PG7/D31/ ET1_TX_ER	TRDATA3/PG7/D31/ ET1_TX_ER	TRDATA3/PG7/D31
112	PA2/A2/MTIOC7A/PO18/ GTIOC1A/RXD5/SMISO5/ SSCL5/SSLA3-B/ CATLINKACT1/ LCD_DATA6-B	PA2/A2/MTIOC7A/PO18/ GTIOC1A/RXD5/SMISO5/ SSCL5/SSLA3-B/ LCD_DATA6-B	PA2/A2/MTIOC7A/PO18/ GTIOC1A/RXD5/SMISO5/ SSCL5/SSLA3-B/ LCD_DATA6-B
113	TRDATA2/PG6/D30/ ET1_ETXD3/CAT1_ETXD3	TRDATA2/PG6/D30/ ET1_ETXD3	TRDATA2/PG6/D30
114	PA1/DQM3/A1/MTIOC0B/ MTCLKC/MTIOC7B/TIOCB0/ PO17/GTIOC2A/SCK5/ SSLA2-B/ET0_WOL/ LCD_DATA7-B/IRQ11	PA1/DQM3/A1/MTIOC0B/ MTCLKC/MTIOC7B/TIOCB0/ PO17/GTIOC2A/SCK5/ SSLA2-B/ET0_WOL/ LCD_DATA7-B/IRQ11	PA1/DQM3/A1/MTIOC0B/ MTCLKC/MTIOC7B/TIOCB0/ PO17/GTIOC2A/SCK5/ SSLA2-B/ET0_WOL/ LCD_DATA7-B/IRQ11
115	VCC	VCC	VCC
116	TRCLK/PG5/D29/ ET1_ETXD2/CAT1_ETXD2	TRCLK/PG5/D29/ ET1_ETXD2	TRCLK/PG5/D29
117	VSS	VSS	VSS
118	PA0/DQM2/BC0#/A0/ MTIOC4A/MTIOC6D/ TIOCA0/PO16/CACREF/ GTIOC0B/SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN/ CAT0_TX_EN/CATLEDRUN/ LCD_DATA8-B	PA0/DQM2/BC0#/A0/ MTIOC4A/MTIOC6D/ TIOCA0/PO16/CACREF/ GTIOC0B/SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN/ LCD_DATA8-B	PA0/DQM2/BC0#/A0/ MTIOC4A/MTIOC6D/ TIOCA0/PO16/CACREF/ GTIOC0B/SSLA1-B/ET0_TX_EN/ RMII0_TXD_EN/ LCD_DATA8-B
119	TRSYNC/PG4/D28/ ET1_ETXD1/RMII1_TXD1/ CAT1_ETXD1	TRSYNC/PG4/D28/ ET1_ETXD1/RMII1_TXD1	TRSYNC/PG4/D28
120	P67/DQM1/CS7#/MTIOC7C/ GTIOC1B/CRX2/EPLSOUT1/ CATSYNC1/IRQ15	P67/DQM1/CS7#/MTIOC7C/ GTIOC1B/CRX2/EPLSOUT1/ IRQ15	P67/DQM1/CS7#/MTIOC7C/ GTIOC1B/CRX2/IRQ15
121	TRDATA1/PG3/D27/ ET1_ETXD0/RMII1_TXD0/ CAT1_ETXD0	TRDATA1/PG3/D27/ ET1_ETXD0/RMII1_TXD0	TRDATA1/PG3/D27
122	P66/DQM0/CS6#/MTIOC7D/ GTIOC2B/CTX2	P66/DQM0/CS6#/MTIOC7D/ GTIOC2B/CTX2	P66/DQM0/CS6#/MTIOC7D/ GTIOC2B/CTX2
123	TRDATA0/PG2/D26/ ET1_TX_CLK/ CAT1_TX_CLK	TRDATA0/PG2/D26/ ET1_TX_CLK	TRDATA0/PG2/D26
124	P65/CKE/CS5#	P65/CKE/CS5#	P65/CKE/CS5#
125	PE7/D15[A15/D15]/ D7[A7/D7]/MTIOC6A/TOC1/ GTIOC3A/MISOB-B/ SDHI_WP/MMC_RES#-B/ LCD_DATA9-B/IRQ7/AN105	PE7/D15[A15/D15]/ D7[A7/D7]/MTIOC6A/TOC1/ GTIOC3A/MISOB-B/ SDHI_WP/MMC_RES#-B/ LCD_DATA9-B/IRQ7/AN105	PE7/D15[A15/D15]/ D7[A7/D7]/MTIOC6A/TOC1/ GTIOC3A/MISOB-B/ SDHI_WP/MMC_RES#-B/ LCD_DATA9-B/IRQ7/AN105
126	PE6/D14[A14/D14]/ D6[A6/D6]/MTIOC6C/TIC1/ GTIOC3B/MOSIB-B/ SDHI_CD/MMC_CD-B/ LCD_DATA10-B/IRQ6/AN104	PE6/D14[A14/D14]/ D6[A6/D6]/MTIOC6C/TIC1/ GTIOC3B/MOSIB-B/ SDHI_CD/MMC_CD-B/ LCD_DATA10-B/IRQ6/AN104	PE6/D14[A14/D14]/ D6[A6/D6]/MTIOC6C/TIC1/ GTIOC3B/MOSIB-B/ SDHI_CD/MMC_CD-B/ LCD_DATA10-B/IRQ6/AN104
127	VCC	VCC	VCC
128	P70/SDCLK/CATLINKACT0	P70/SDCLK	P70/SDCLK
129	VSS	VSS	VSS

176-Pin LFQFP	RX72M	RX72N	RX66N
130	PE5/D13[A13/D13]/ D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/ RSPCKB-B/ET0_RX_CLK/ REF50CK0/CAT0_RX_CLK/ LCD_DATA11-B/IRQ5/AN103	PE5/D13[A13/D13]/ D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/ RSPCKB-B/ET0_RX_CLK/ REF50CK0/LCD_DATA11-B/ IRQ5/AN103	PE5/D13[A13/D13]/ D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/ RSPCKB-B/ET0_RX_CLK/ REF50CK0/LCD_DATA11-B/ IRQ5/AN103
131	PE4/D12[A12/D12]/ D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/ SSLB0-B/ET0_ERXD2/ CAT0_ERXD2/ LCD_DATA12-B/AN102	PE4/D12[A12/D12]/ D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/ SSLB0-B/ET0_ERXD2/ LCD_DATA12-B/AN102	PE4/D12[A12/D12]/ D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/ SSLB0-B/ET0_ERXD2/ LCD_DATA12-B/AN102
132	PE3/D11[A11/D11]/ D3[A3/D3]/MTIOC4B/PO26/ TOC3/POE8#/GTIOC2A/ CTS12#/RTS12#/SS12#/ ET0_ERXD3/CAT0_ERXD3/ MMC_D7-B/LCD_DATA13-B/ AN101	PE3/D11[A11/D11]/ D3[A3/D3]/MTIOC4B/PO26/ TOC3/POE8#/GTIOC2A/ CTS12#/RTS12#/SS12#/ ET0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101	PE3/D11[A11/D11]/ D3[A3/D3]/MTIOC4B/PO26/ TOC3/POE8#/GTIOC2A/ CTS12#/RTS12#/SS12#/ ET0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101
133	PE2/D10[A10/D10]/ D2[A2/D2]/MTIOC4A/PO23/ TIC3/GTIOC0B/RXD12/ SMISO12/SSCL12/RXDX12/ SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/ AN100	PE2/D10[A10/D10]/ D2[A2/D2]/MTIOC4A/PO23/ TIC3/GTIOC0B/RXD12/ SMISO12/SSCL12/RXDX12/ SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/ AN100	PE2/D10[A10/D10]/ D2[A2/D2]/MTIOC4A/PO23/ TIC3/GTIOC0B/RXD12/ SMISO12/SSCL12/RXDX12/ SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/ AN100
134	PE1/D9[A9/D9]/D1[A1/D1]/ MTIOC4C/MTIOC3B/PO18/ GTIOC1B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/ SSLB2-B/MMC_D5-B/ LCD_DATA15-B/ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/ MTIOC4C/MTIOC3B/PO18/ GTIOC1B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/ SSLB2-B/MMC_D5-B/ LCD_DATA15-B/ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/ MTIOC4C/MTIOC3B/PO18/ GTIOC1B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/ SSLB2-B/MMC_D5-B/ LCD_DATA15-B/ANEX1
135	PE0/D8[A8/D8]/D0[A0/D0]/ MTIOC3D/GTIOC2B/SCK12/ SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/ MTIOC3D/GTIOC2B/SCK12/ SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/ MTIOC3D/GTIOC2B/SCK12/ SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0
136	P64/WE#/D3[A3/D3]/CS4#/ ET1_ETXD0/RMII1_TXD0/ CAT1_ETXD0	P64/WE#/D3[A3/D3]/CS4#/ ET1_ETXD0/RMII1_TXD0	P64/WE#/D3[A3/D3]/CS4#
137	P63/CAS#/D2[A2/D2]/CS3#/ ET1_ETXD1/RMII1_TXD1/ CAT1_ETXD1	P63/CAS#/D2[A2/D2]/CS3#/ ET1_ETXD1/RMII1_TXD1	P63/CAS#/D2[A2/D2]/CS3#
138	P62/RAS#/D1[A1/D1]/CS2#/ ET1_ERXD0/RMII1_RXD0/ CAT1_ERXD0	P62/RAS#/D1[A1/D1]/CS2#/ ET1_ERXD0/RMII1_RXD0	P62/RAS#/D1[A1/D1]/CS2#
139	P61/SDCS#/D0[A0/D0]/ CS1#/ET1_ERXD1/ RMII1_RXD1/CAT1_ERXD1	P61/SDCS#/D0[A0/D0]/ CS1#/ET1_ERXD1/ RMII1_RXD1	P61/SDCS#/D0[A0/D0]/CS1#
140	VSS	VSS	VSS
141	P60/CS0#/ET1_TX_EN/ RMII1_TXD_EN/ CAT1_TX_EN	P60/CS0#/ET1_TX_EN/ RMII1_TXD_EN	P60/CS0#
142	VCC	VCC	VCC

176-Pin LFQFP	RX72M	RX72N	RX66N
143	PD7/D7[A7/D7]/MTIC5U/ POE0#/SSLC3-A/ ET1_RX_ER/RMII1_RX_ER/ CAT1_RX_ER/QMI-B/ QIO1-B/SDHI_D1-B/ MMC_D1-B/LCD_DATA17-B/ IRQ7/AN107	PD7/D7[A7/D7]/MTIC5U/ POE0#/SSLC3-A/ ET1_RX_ER/RMII1_RX_ER/ QMI-B/QIO1-B/SDHI_D1-B/ MMC_D1-B/LCD_DATA17-B/ IRQ7/AN107	PD7/D7[A7/D7]/MTIC5U/ POE0#/SSLC3-A/QMI-B/ QIO1-B/SDHI_D1-B/ MMC_D1-B/LCD_DATA17-B/ IRQ7/AN107
144	TRDATA7/PG1/D25/ ET1_RX_ER/RMII1_RX_ER/ CAT1_RX_ER	TRDATA7/PG1/D25/ ET1_RX_ER/RMII1_RX_ER	TRDATA7/PG1/D25
145	PD6/D6[A6/D6]/MTIC5V/ MTIOC8A/POE4#/SSLC2-A/ ET1_RX_CLK/REF50CK1/ CAT1_RX_CLK/QMO-B/ QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/ IRQ6/AN106	PD6/D6[A6/D6]/MTIC5V/ MTIOC8A/POE4#/SSLC2-A/ ET1_RX_CLK/REF50CK1/ QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/ IRQ6/AN106	PD6/D6[A6/D6]/MTIC5V/ MTIOC8A/POE4#/SSLC2-A/ QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/ IRQ6/AN106
146	TRDATA6/PG0/D24/ ET1_RX_CLK/REF50CK1/ CAT1_RX_CLK	TRDATA6/PG0/D24/ ET1_RX_CLK/REF50CK1	TRDATA6/PG0/D24
147	PD5/D5[A5/D5]/MTIC5W/ MTIOC8C/MTCLKA/POE10#/ SSLC1-A/ET1_MDC/ PMGI1_MDC/QSPCLK-B/ SDHI_CLK-B/MMC_CLK-B/ LCD_DATA19-B/IRQ5/AN113	PD5/D5[A5/D5]/MTIC5W/ MTIOC8C/MTCLKA/POE10#/ SSLC1-A/ET1_MDC/ PMGI1_MDC/QSPCLK-B/ SDHI_CLK-B/MMC_CLK-B/ LCD_DATA19-B/IRQ5/AN113	PD5/D5[A5/D5]/MTIC5W/ MTIOC8C/MTCLKA/POE10#/ SSLC1-A/QSPCLK-B/ SDHI_CLK-B/MMC_CLK-B/ LCD_DATA19-B/IRQ5/AN113
148	PD4/D4[A4/D4]/MTIOC8B/ POE11#/SSLC0-A/ ET1_MDIO/PMGI1_MDIO/ QSSL-B/SDHI_CMD-B/ MMC_CMD-B/ LCD_DATA20-B/IRQ4/AN112	PD4/D4[A4/D4]/MTIOC8B/ POE11#/SSLC0-A/ ET1_MDIO/PMGI1_MDIO/ QSSL-B/SDHI_CMD-B/ MMC_CMD-B/ LCD_DATA20-B/IRQ4/AN112	PD4/D4[A4/D4]/MTIOC8B/ POE11#/SSLC0-A/QSSL-B/ SDHI_CMD-B/MMC_CMD-B/ LCD_DATA20-B/IRQ4/AN112
149	TRSYNC1/P97/D23/A23/ ET1_ERXD3/CAT1_ERXD3	TRSYNC1/P97/D23/A23/ ET1_ERXD3	TRSYNC1/P97/D23/A23
150	PD3/D3[A3/D3]/MTIOC8D/ TOC2/POE8#/GTIOC0A/ RSPCKC-A/ET1_WOL/ QIO3-B/SDHI_D3-B/ MMC_D3-B/LCD_DATA21-B/ IRQ3/AN111	PD3/D3[A3/D3]/MTIOC8D/ TOC2/POE8#/GTIOC0A/ RSPCKC-A/ET1_WOL/ QIO3-B/SDHI_D3-B/ MMC_D3-B/LCD_DATA21-B/ IRQ3/AN111	PD3/D3[A3/D3]/MTIOC8D/ TOC2/POE8#/GTIOC0A/ RSPCKC-A/QIO3-B/ SDHI_D3-B/MMC_D3-B/ LCD_DATA21-B/IRQ3/AN111
151	VSS	VSS	VSS
152	TRDATA5/P96/D22/A22/ ET1_ERXD2/CAT1_ERXD2	TRDATA5/P96/D22/A22/ ET1_ERXD2	TRDATA5/P96/D22/A22
153	VCC	VCC	VCC
154	PD2/D2[A2/D2]/MTIOC4D/ TIC2/GTIOC0B/MISOC-A/ CRX0/ET1_EXOUT/QIO2-B/ SDHI_D2-B/MMC_D2-B/ LCD_DATA22-B/IRQ2/AN110	PD2/D2[A2/D2]/MTIOC4D/ TIC2/GTIOC0B/MISOC-A/ CRX0/ET1_EXOUT/QIO2-B/ SDHI_D2-B/MMC_D2-B/ LCD_DATA22-B/IRQ2/AN110	PD2/D2[A2/D2]/MTIOC4D/ TIC2/GTIOC0B/MISOC-A/ CRX0/QIO2-B/SDHI_D2-B/ MMC_D2-B/LCD_DATA22-B/ IRQ2/AN110
155	TRDATA4/P95/D21/A21/ ET1_ERXD1/RMII1_RXD1/ CAT1_ERXD1	TRDATA4/P95/D21/A21/ ET1_ERXD1/RMII1_RXD1	TRDATA4/P95/D21/A21

176-Pin LFQFP	RX72M	RX72N	RX66N
156	PD1/D1[A1/D1]/MTIOC4B/ POE0#/GTIOC1A/MOSIC-A/ CTX0/LCD_DATA23-B/IRQ1/ AN109	PD1/D1[A1/D1]/MTIOC4B/ POE0#/GTIOC1A/MOSIC-A/ CTX0/LCD_DATA23-B/IRQ1/ AN109	PD1/D1[A1/D1]/MTIOC4B/ POE0#/GTIOC1A/MOSIC-A/ CTX0/LCD_DATA23-B/IRQ1/ AN109
157	P94/D20/A20/ET1_ERXD0/ RMII1_RXD0/CAT1_ERXD0	P94/D20/A20/ET1_ERXD0/ RMII1_RXD0	P94/D20/A20
158	PD0/D0[A0/D0]/POE4#/ GTIOC1B/LCD_EXTCLK-B/ IRQ0/AN108	PD0/D0[A0/D0]/POE4#/ GTIOC1B/LCD_EXTCLK-B/ IRQ0/AN108	PD0/D0[A0/D0]/POE4#/ GTIOC1B/LCD_EXTCLK-B/ IRQ0/AN108
159	P93/D19/A19/POE0#/CTS7#/ RTS7#/SS7#/ET1_LINKSTA/ CAT1_LINKSTA/AN117/ DSMDAT4	P93/D19/A19/POE0#/CTS7#/ RTS7#/SS7#/ET1_LINKSTA/ AN117	P93/D19/A19/POE0#/CTS7#/ RTS7#/SS7#/AN117
160	P92/D18/A18/POE4#/RXD7/ SMISO7/SSCL7/ET1_CRS/ RMII1_CRS_DV/ CAT1_RX_DV/AN116/ DSMCLK4	P92/D18/A18/POE4#/RXD7/ SMISO7/SSCL7/ET1_CRS/ RMII1_CRS_DV/AN116	P92/D18/A18/POE4#/RXD7/ SMISO7/SSCL7/AN116
161	P91/D17/A17/SCK7/ ET1_COL/AN115/DSMDAT5	P91/D17/A17/SCK7/ ET1_COL/AN115	P91/D17/A17/SCK7/AN115
162	VSS	VSS	VSS
163	P90/D16/A16/TXD7/SMOSI7/ SSDA7/ET1_RX_DV/ CAT1_RX_DV/AN114/ DSMCLK5	P90/D16/A16/TXD7/SMOSI7/ SSDA7/ET1_RX_DV/AN114	P90/D16/A16/TXD7/SMOSI7/ SSDA7/AN114
164	VCC	VCC	VCC
165	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
166	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
167	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
168	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
169	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
170	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
171	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
172	VREFL0	VREFL0	VREFL0
173	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
174	VREFH0	VREFH0	VREFH0
175	AVCC0	AVCC0	AVCC0
176	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#

Note: 1. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.

3.4 145-Pin TFLGA Package

Table 3.4 is a comparative listing of the pin functions of 145-pin TFLGA package products. Note that the RX72M Group has no product versions with a 145-pin package.

Table 3.4 Comparative Listing of 145-Pin TFLGA Package Pin Functions

145-Pin TFLGA	RX72N	RX66N
A1	AVSS0	AVSS0
A2	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
A3	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
A4	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
A5	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
A6	P90/A16/TXD7/SMOSI7/SSDA7/AN114	P90/A16/TXD7/SMOSI7/SSDA7/AN114
A7	P92/A18/POE4#/RXD7/SMISO7/SSCL7/ RMII1_CRS_DV/AN116	P92/A18/POE4#/RXD7/SMISO7/SSCL7/ AN116
A8	PD2/D2[A2/D2]/MTIOC4D/TIC2/GTIOC0B/ MISOC-A/CRX0/ET1_EXOUT/QIO2-B/ SDHI_D2-B/MMC_D2-B/LCD_DATA22-B/ IRQ2/AN110	PD2/D2[A2/D2]/MTIOC4D/TIC2/GTIOC0B/ MISOC-A/CRX0/QIO2-B/SDHI_D2-B/ MMC_D2-B/LCD_DATA22-B/IRQ2/AN110
A9	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/REF50CK1/QMO-B/QIO0-B/ SDHI_D0-B/MMC_D0-B/LCD_DATA18-B/ IRQ6/AN106	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/IRQ6/AN106
A10	VSS	VSS
A11	P62/RAS#/D1[A1/D1]/CS2#/RMII1_RXD0	P62/RAS#/D1[A1/D1]/CS2#
A12	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/GTIOC1B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/SSLB2-B/ MMC_D5-B/LCD_DATA15-B/ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/GTIOC1B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/SSLB2-B/ MMC_D5-B/LCD_DATA15-B/ANEX1
A13	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/TOC3/POE8#/GTIOC2A/CTS12#/ RTS12#/SS12#/ET0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/TOC3/POE8#/GTIOC2A/CTS12#/ RTS12#/SS12#/ET0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101
B1	AVCC1	AVCC1
B2	AVCC0	AVCC0
B3	P05/SSILRCK1/IRQ13/DA1	P05/SSILRCK1/IRQ13/DA1
B4	VREFL0	VREFL0
B5	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
B6	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
B7	P91/A17/SCK7/AN115	P91/A17/SCK7/AN115
B8	PD0/D0[A0/D0]/POE4#/GTIOC1B/ LCD_EXTCLK-B/IRQ0/AN108	PD0/D0[A0/D0]/POE4#/GTIOC1B/ LCD_EXTCLK-B/IRQ0/AN108
B9	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/ET1_MDIO/PMGI1_MDIO/ QSSL-B/SDHI_CMD-B/MMC_CMD-B/ LCD_DATA20-B/IRQ4/AN112	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/QSSL-B/SDHI_CMD-B/ MMC_CMD-B/LCD_DATA20-B/IRQ4/AN112
B10	VCC	VCC
B11	P61/SDCS#/D0[A0/D0]/CS1#/RMII1_RXD1	P61/SDCS#/D0[A0/D0]/CS1#
B12	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/GTIOC0B/RXD12/SMISO12/ SSCL12/RXDX12/SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/AN100	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/GTIOC0B/RXD12/SMISO12/ SSCL12/RXDX12/SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/AN100

145-Pin TFLGA	RX72N	RX66N
B13	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/SSLB0-B/ ET0_ERXD2/LCD_DATA12-B/AN102	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/SSLB0-B/ ET0_ERXD2/LCD_DATA12-B/AN102
C1	AVSS1	AVSS1
C2	P02/TMCI1/SCK6/SSIBCK1/IRQ10/AN120	P02/TMCI1/SCK6/SSIBCK1/IRQ10/AN120
C3	VREFH0	VREFH0
C4	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
C5	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
C6	VSS	VSS
C7	PD1/D1[A1/D1]/MTIOC4B/POE0#/GTIOC1A/ MOSIC-A/CTX0/LCD_DATA23-B/IRQ1/ AN109	PD1/D1[A1/D1]/MTIOC4B/POE0#/GTIOC1A/ MOSIC-A/CTX0/LCD_DATA23-B/IRQ1/ AN109
C8	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ GTIOC0A/RSPCKC-A/ET1_WOL/QIO3-B/ SDHI_D3-B/MMC_D3-B/LCD_DATA21-B/ IRQ3/AN111	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ GTIOC0A/RSPCKC-A/QIO3-B/SDHI_D3-B/ MMC_D3-B/LCD_DATA21-B/IRQ3/AN111
C9	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ RMII1_RX_ER/QMI-B/QIO1-B/SDHI_D1-B/ MMC_D1-B/LCD_DATA17-B/IRQ7/AN107	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B/ LCD_DATA17-B/IRQ7/AN107
C10	P63/CAS#/D2[A2/D2]/CS3#/RMII1_TXD1	P63/CAS#/D2[A2/D2]/CS3#
C11	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/ GTIOC2B/SCK12/SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/ GTIOC2B/SCK12/SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0
C12	P70/SDCLK	P70/SDCLK
C13	VSS	VSS
D1	P00/TMRI0/TXD6/SMOSI6/SSDA6/ AUDIO_CLK/IRQ8/AN118	P00/TMRI0/TXD6/SMOSI6/SSDA6/ AUDIO_CLK/IRQ8/AN118
D2	PF5/WAIT#/SSILRCK0/IRQ4	PF5/WAIT#/SSILRCK0/IRQ4
D3	P03/SSIDATA1/IRQ11/DA0	P03/SSIDATA1/IRQ11/DA0
D4	P01/TMCI0/RXD6/SMISO6/SSCL6/SSIBCK0/ IRQ9/AN119	P01/TMCI0/RXD6/SMISO6/SSCL6/SSIBCK0/ IRQ9/AN119
D5	VCC	VCC
D6	P93/A19/POE0#/CTS7#/RTS7#/SS7#/ ET1_LINKSTA/AN117	P93/A19/POE0#/CTS7#/RTS7#/SS7#/ AN117
D7	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/ MTCLKA/POE10#/SSLC1-A/ET1_MDC/ PMGI1_MDC/QSPCLK-B/SDHI_CLK-B/ MMC_CLK-B/LCD_DATA19-B/IRQ5/AN113	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/ MTCLKA/POE10#/SSLC1-A/QSPCLK-B/ SDHI_CLK-B/MMC_CLK-B/LCD_DATA19-B/ IRQ5/AN113
D8	P60/CS0#/RMII1_TXD_EN	P60/CS0#
D9	P64/WE#/D3[A3/D3]/CS4#/RMII1_TXD0	P64/WE#/D3[A3/D3]/CS4#
D10	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/GTIOC3A/MISOB-B/SDHI_WP/ MMC_RES#-B/LCD_DATA9-B/IRQ7/AN105	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/GTIOC3A/MISOB-B/SDHI_WP/ MMC_RES#-B/LCD_DATA9-B/IRQ7/AN105
D11	VCC	VCC
D12	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/RSPCKB-B/ ET0_RX_CLK/REF50CK0/LCD_DATA11-B/ IRQ5/AN103	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/RSPCKB-B/ ET0_RX_CLK/REF50CK0/LCD_DATA11-B/ IRQ5/AN103
D13	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/GTIOC3B/MOSIB-B/SDHI_CD/ MMC_CD-B/LCD_DATA10-B/IRQ6/AN104	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/GTIOC3B/MOSIB-B/SDHI_CD/ MMC_CD-B/LCD_DATA10-B/IRQ6/AN104
E1	VSS	VSS

145-Pin TFLGA	RX72N	RX66N
E2	VCL	VCL
E3	PJ5/POE8#/CTS2#/RTS2#/SS2#/SSIRXD0/ EPLSOUT0	PJ5/POE8#/CTS2#/RTS2#/SS2#/SSIRXD0
E4	EMLE	EMLE
E5	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
E10	PA0/BC0#/A0/MTIOC4A/MTIOC6D/TIOCA0/ PO16/CACREF/GTIOC0B/SSLA1-B/ ET0_TX_EN/RMII0_TXD_EN/LCD_DATA8-B	PA0/BC0#/A0/MTIOC4A/MTIOC6D/TIOCA0/ PO16/CACREF/GTIOC0B/SSLA1-B/ ET0_TX_EN/RMII0_TXD_EN/LCD_DATA8-B
E11	P66/DQM0/CS6#/MTIOC7D/GTIOC2B/CTX2	P66/DQM0/CS6#/MTIOC7D/GTIOC2B/CTX2
E12	P65/CKE/CS5#	P65/CKE/CS5#
E13	P67/DQM1/CS7#/MTIOC7C/GTIOC1B/ CRX2/EPLSOUT1/IRQ15	P67/DQM1/CS7#/MTIOC7C/GTIOC1B/ CRX2/IRQ15
F1	XCIN	XCIN
F2	XCOUT	XCOUT
F3	PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/ SS6#/CTS0#/RTS0#/SS0#/SSITXD0/ ET0_EXOUT	PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/ SS6#/CTS0#/RTS0#/SS0#/SSITXD0/ ET0_EXOUT
F4	VBATT	VBATT
F10	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/ PO19/RXD5/SMISO5/SSCL5/ET0_MDIO/ PMGI0_MDIO/LCD_DATA5-B/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/ PO19/RXD5/SMISO5/SSCL5/ET0_MDIO/ PMGI0_MDIO/LCD_DATA5-B/IRQ6-DS
F11	VSS	VSS
F12	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/GTIOC2A/SCK5/SSLA2-B/ ET0_WOL/LCD_DATA7-B/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/GTIOC2A/SCK5/SSLA2-B/ ET0_WOL/LCD_DATA7-B/IRQ11
F13	PA2/A2/MTIOC7A/PO18/GTIOC1A/RXD5/ SMISO5/SSCL5/SSLA3-B/LCD_DATA6-B	PA2/A2/MTIOC7A/PO18/GTIOC1A/RXD5/ SMISO5/SSCL5/SSLA3-B/LCD_DATA6-B
G1	XTAL/P37	XTAL/P37
G2	RES#	RES#
G3	MD/FINED	MD/FINED
G4	BSCANP	BSCANP
G10	PA5/A5/MTIOC6B/TIOCB1/PO21/GTIOC0A/ RSPCKA-B/ET0_LINKSTA/LCD_DATA3-B	PA5/A5/MTIOC6B/TIOCB1/PO21/GTIOC0A/ RSPCKA-B/ET0_LINKSTA/LCD_DATA3-B
G11	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/GTETRGB/CTS5#/RTS5#/ SS5#/MOSIA-B/ET0_EXOUT/LCD_DATA2-B	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/GTETRGB/CTS5#/RTS5#/ SS5#/MOSIA-B/ET0_EXOUT/LCD_DATA2-B
G12	VCC	VCC
G13	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/PMGI0_MDC/LCD_DATA4-B/ IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/PMGI0_MDC/LCD_DATA4-B/ IRQ5-DS
H1	EXTAL/P36	EXTAL/P36
H2	VCC	VCC
H3	VSS	VSS
H4	UPSEL/P35/NMI	UPSEL/P35/NMI
H10	P72/A19/CS2#/ET0_MDC/PMGI0_MDC	P72/A19/CS2#/ET0_MDC/PMGI0_MDC
H11	P71/A18/CS1#/ET0_MDIO/PMGI0_MDIO	P71/A18/CS1#/ET0_MDIO/PMGI0_MDIO
H12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/ SMISO4/SSCL4/RXD6/SMISO6/SSCL6/ ET0_ERXD1/RMII0_RXD1/LCD_DATA0-B/ IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/ SMISO4/SSCL4/RXD6/SMISO6/SSCL6/ ET0_ERXD1/RMII0_RXD1/LCD_DATA0-B/ IRQ12

145-Pin TFLGA	RX72N	RX66N
H13	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/ LCD_DATA1-B	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/ LCD_DATA1-B
J1	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/ET0_LINKSTA/IRQ4	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/ET0_LINKSTA/IRQ4
J2	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/SMISO6/ SSCL6/RXD0/SMISO0/SSCL0/CRX0/PCKO/ IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/SMISO6/ SSCL6/RXD0/SMISO0/SSCL0/CRX0/PCKO/ IRQ3-DS
J3	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCIC2/RTCOUT/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCIC2/RTCOUT/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS
J4	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ ET1_MDIO/PMGI1_MDIO/IRQ0-DS	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS
J10	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ ET0_RX_ER/RMII0_RX_ER/LCD_TCON1-B	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ ET0_RX_ER/RMII0_RX_ER/LCD_TCON1-B
J11	PB4/A12/TIOCA4/PO28/CTS9#/SS9#/ SS11#/CTS11#/RTS11#/ET0_TX_EN/ RMII0_TXD_EN/LCD_TCON0-B	PB4/A12/TIOCA4/PO28/CTS9#/SS9#/ SS11#/CTS11#/RTS11#/ET0_TX_EN/ RMII0_TXD_EN/LCD_TCON0-B
J12	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/ RTS4#/SS4#/CTS6#/RTS6#/SS6#/ ET0_RX_CLK/REF50CK0/LCD_TCON2-B	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/ RTS4#/SS4#/CTS6#/RTS6#/SS6#/ ET0_RX_CLK/REF50CK0/LCD_TCON2-B
J13	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD4/SMOSI4/SSDA4/TXD6/ SMOSI6/SSDA6/ET0_ERXD0/RMII0_RXD0/ LCD_TCON3-B/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD4/SMOSI4/SSDA4/TXD6/ SMOSI6/SSDA6/ET0_ERXD0/RMII0_RXD0/ LCD_TCON3-B/IRQ4-DS
K1	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/ RSPCKB-A/ET1_WOL	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/ RSPCKB-A
K2	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A/ET1_EXOUT	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A
K3	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/ET1_MDC/ PMGI1_MDC/IRQ1-DS	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS
K4	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/GTETRGA/RXD1/SMISO1/ SSCL1/SCK3/CRX1-DS/SSILRCK1/PIXD0/ IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/GTETRGA/RXD1/SMISO1/ SSCL1/SCK3/CRX1-DS/SSILRCK1/PIXD0/ IRQ5
K5	TRDATA2/P54/ALE/D1[A1/D1]/EDACK0/ MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/ CTX1/ET0_LINKSTA	TRDATA2/P54/ALE/D1[A1/D1]/EDACK0/ MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/ CTX1/ET0_LINKSTA
K6	P53*[1]/BCLK	P53*[1]/BCLK
K7	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A
K8	VCC	VCC
K9	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/ SCK10/RTS10#/ET0_TX_EN/ RMII0_TXD_EN/QIO2-A/SDHI_WP/ MMC_D2-A	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/ SCK10/RTS10#/ET0_TX_EN/ RMII0_TXD_EN/QIO2-A/SDHI_WP/ MMC_D2-A
K10	TRDATA6/P76/CS6#/PO22/SMISO11/ SSCL11/RXD11/ET0_RX_CLK/REF50CK0/ QSSL-A/SDHI_CMD-A/MMC_CMD-A	TRDATA6/P76/CS6#/PO22/SMISO11/ SSCL11/RXD11/ET0_RX_CLK/REF50CK0/ QSSL-A/SDHI_CMD-A/MMC_CMD-A

145-Pin TFLGA	RX72N	RX66N
K11	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ ET0_CRS/RMII0_CRS_DV	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ ET0_CRS/RMII0_CRS_DV
K12	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ ET0_ETXD1/RMII0_TXD1	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ ET0_ETXD1/RMII0_TXD1
K13	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9/RTS9#/SCK11/ ET0_ETXD0/RMII0_TXD0/LCD_CLK-B	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9/RTS9#/SCK11/ ET0_ETXD0/RMII0_TXD0/LCD_CLK-B
L1	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/ MTCLKB/TIOCA4/PO5/RXD3/SMISO3/ SSCL3/SSIDATA1/SDHI_CD/HSYNC/ ADTRG0#	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/ MTCLKB/TIOCA4/PO5/RXD3/SMISO3/ SSCL3/SSIDATA1/SDHI_CD/HSYNC/ ADTRG0#
L2	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/GTIOC0A/TXD3/SMOSI3/SSDA3/ CTS0#/RTS0#/SS0#/CTX1/SSIBCK0/ SDHI_D1-C/PIXD7	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/GTIOC0A/TXD3/SMOSI3/SSDA3/ CTS0#/RTS0#/SS0#/CTX1/SSIBCK0/ SDHI_D1-C/PIXD7
L3	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/SMOSI1/ SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/ USB0_VBUSEN/USB0_VBUS/ USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/SMOSI1/ SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/ USB0_VBUSEN/USB0_VBUS/ USB0_OVRCURB/IRQ6/ADTRG0#
L4	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SSIBCK1/SDHI_WP/PIXCLK	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SSIBCK1/SDHI_WP/PIXCLK
L5	P13/MTIOC0B/TIOCA5/TMO3/PO13/ GTADSM1/TXD2/SMOSI2/SSDA2/ SDA0[FM+]/IRQ3/ADTRG1#	P13/MTIOC0B/TIOCA5/TMO3/PO13/ GTADSM1/TXD2/SMOSI2/SSDA2/ SDA0[FM+]/IRQ3/ADTRG1#
L6	CLKOUT25M/P56/EDACK1/MTIOC3C/ TIOCA1/SCK7	CLKOUT25M/P56/EDACK1/MTIOC3C/ TIOCA1/SCK7
L7	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A
L8	TRCLK/P83/EDACK1/MTIOC4C/GTIOC0A/ SCK10/SS10#/CTS10#/ET0_CRS/ RMII0_CRS_DV	TRCLK/P83/EDACK1/MTIOC4C/GTIOC0A/ SCK10/SS10#/CTS10#/ET0_CRS/ RMII0_CRS_DV
L9	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/GTIOC1A/SCK8/ RTS8#/SCK10/RSPCKA-A/ET0_ETXD2/ MMC_D5-A	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/GTIOC1A/SCK8/ RTS8#/SCK10/RSPCKA-A/ET0_ETXD2/ MMC_D5-A
L10	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/GTETRGC/SCK5/CTS8#/ SS8#/SS10#/CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK/QMI-A/QIO1-A/SDHI_D1-A/ MMC_D1-A	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/GTETRGC/SCK5/CTS8#/ SS8#/SS10#/CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK/QMI-A/QIO1-A/SDHI_D1-A/ MMC_D1-A
L11	PC2/A18/MTIOC4B/TCLKA/PO21/GTIOC2B/ RXD5/SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV/SDHI_D3-A/MMC_CD-A	PC2/A18/MTIOC4B/TCLKA/PO21/GTIOC2B/ RXD5/SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV/SDHI_D3-A/MMC_CD-A
L12	TRDATA4/P73/CS3#/PO16/ET0_WOL	TRDATA4/P73/CS3#/PO16/ET0_WOL
L13	VSS	VSS
M1	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/GTIOC1A/SCK0/ USB0_OVRCURB/AUDIO_CLK/SDHI_D0-C/ PIXD6	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/GTIOC1A/SCK0/ USB0_OVRCURB/AUDIO_CLK/SDHI_D0-C/ PIXD6

145-Pin TFLGA	RX72N	RX66N
M2	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/GTIOC0B/ SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/ SSITXD0/EPLSOUT0/SDHI_D3-C/PIXD3/ IRQ7/ADTRG1#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/GTIOC0B/ SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/ SSITXD0/SDHI_D3-C/PIXD3/IRQ7/ ADTRG1#
M3	P86/MTIOC4D/TIOCA0/GTIOC2B/SMISO10/ SSCL10/RXD10/PIXD1	P86/MTIOC4D/TIOCA0/GTIOC2B/SMISO10/ SSCL10/RXD10/PIXD1
M4	P12/TMCI1/GTADSM0/RXD2/SMISO2/ SSCL2/SCL0[FM+]/IRQ2	P12/TMCI1/GTADSM0/RXD2/SMISO2/ SSCL2/SCL0[FM+]/IRQ2
M5	VCC_USB	VCC_USB
M6	VSS_USB	VSS_USB
M7	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A
M8	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/PO30/TIC0/GTIOC3B/ RXD8/SMISO8/SSCL8/SMISO10/SSCL10/ RXD10/MOSIA-A/ET0_ETXD3/MMC_D6-A/ IRQ13	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/PO30/TIC0/GTIOC3B/ RXD8/SMISO8/SSCL8/SMISO10/SSCL10/ RXD10/MOSIA-A/ET0_ETXD3/MMC_D6-A/ IRQ13
M9	TRDATA1/P81/EDACK0/MTIOC3D/PO27/ GTIOC0B/SMISO10/SSCL10/RXD10/ ET0_ETXD0/RMII0_TXD0/QIO3-A/ SDHI_CD/MMC_D3-A	TRDATA1/P81/EDACK0/MTIOC3D/PO27/ GTIOC0B/SMISO10/SSCL10/RXD10/ ET0_ETXD0/RMII0_TXD0/QIO3-A/ SDHI_CD/MMC_D3-A
M10	TRDATA7/P77/CS7#/PO23/SMOSI11/ SSDA11/TXD11/ET0_RX_ER/ RMII0_RX_ER/QSPCLK-A/SDHI_CLK-A/ MMC_CLK-A	TRDATA7/P77/CS7#/PO23/SMOSI11/ SSDA11/TXD11/ET0_RX_ER/ RMII0_RX_ER/QSPCLK-A/SDHI_CLK-A/ MMC_CLK-A
M11	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14
M12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/IRQ12
M13	VCC	VCC
N1	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/GTIOC2A/RXD0/SMISO0/SSCL0/ SCL1/USB0_EXICEN/SSILRCK0/ SDHI_CLK-C/PIXD5/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/GTIOC2A/RXD0/SMISO0/SSCL0/ SCL1/USB0_EXICEN/SSILRCK0/ SDHI_CLK-C/PIXD5/IRQ9
N2	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMD-C/PIXD4/IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMD-C/PIXD4/IRQ8
N3	P87/MTIOC4C/TIOCA2/GTIOC1B/SMOSI10/ SSDA10/TXD10/EPLSOUT1/SDHI_D2-C/ PIXD2	P87/MTIOC4C/TIOCA2/GTIOC1B/SMOSI10/ SSDA10/TXD10/SDHI_D2-C/PIXD2
N4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/GTETRGD/CTS1#/RTS1#/ SS1#/CTX1/USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/GTETRGD/CTS1#/RTS1#/ SS1#/CTX1/USB0_OVRCURA/IRQ4
N5	USB0_DM	USB0_DM
N6	USB0_DP	USB0_DP
N7	TRDATA3/P55/D0[A0/D0]/WAIT#/EDREQ0/ MTIOC4D/TMO3/TXD7/SMOSI7/SSDA7/ CRX1/ET0_EXOUT/IRQ10	TRDATA3/P55/D0[A0/D0]/WAIT#/EDREQ0/ MTIOC4D/TMO3/TXD7/SMOSI7/SSDA7/ CRX1/ET0_EXOUT/IRQ10
N8	VSS	VSS

145-Pin TFLGA	RX72N	RX66N
N9	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/PO31/TOC0/CACREF/GTIOC3A/ TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/ET0_COL/MMC_D7-A/ IRQ14	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/PO31/TOC0/CACREF/GTIOC3A/ TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/ET0_COL/MMC_D7-A/ IRQ14
N10	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/ GTIOC2A/SMOSI10/SSDA10/TXD10/ ET0_ETXD1/RMII0_TXD1/MMC_D4-A	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/ GTIOC2A/SMOSI10/SSDA10/TXD10/ ET0_ETXD1/RMII0_TXD1/MMC_D4-A
N11	PC3/A19/MTIOC4D/TCLKB/PO24/GTIOC1B/ TXD5/SMOSI5/SSDA5/ET0_TX_ER/QMO-A/ QIO0-A/SDHI_D0-A/MMC_D0-A	PC3/A19/MTIOC4D/TCLKB/PO24/GTIOC1B/ TXD5/SMOSI5/SSDA5/ET0_TX_ER/QMO-A/ QIO0-A/SDHI_D0-A/MMC_D0-A
N12	TRSYNC1/P75/CS5#/PO20/SCK11/RTS11#/ ET0_ERXD0/RMII0_RXD0/SDHI_D2-A/ MMC_RES#-A	TRSYNC1/P75/CS5#/PO20/SCK11/RTS11#/ ET0_ERXD0/RMII0_RXD0/SDHI_D2-A/ MMC_RES#-A
N13	TRDATA5/P74/A20/CS4#/PO19/SS11#/ CTS11#/ET0_ERXD1/RMII0_RXD1	TRDATA5/P74/A20/CS4#/PO19/SS11#/ CTS11#/ET0_ERXD1/RMII0_RXD1

Note: 1. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.

3.5 144-Pin LFQFP Package

Table 3.5 is a comparative listing of the pin functions of 144-pin LFQFP package products.

Table 3.5 Comparative Listing of 144-Pin LFQFP Package Pin Functions

144-Pin LFQFP	RX72M	RX72N	RX66N
1	AVSS0	AVSS0	AVSS0
2	P05/SSILRCK1/IRQ13/DA1	P05/SSILRCK1/IRQ13/DA1	P05/SSILRCK1/IRQ13/DA1
3	AVCC1	AVCC1	AVCC1
4	P03/SSIDATA1/IRQ11/DA0	P03/SSIDATA1/IRQ11/DA0	P03/SSIDATA1/IRQ11/DA0
5	AVSS1	AVSS1	AVSS1
6	P02/TMCI1/SCK6/SSIBCK1/ CATLEDSTER/IRQ10/ AN120	P02/TMCI1/SCK6/SSIBCK1/ IRQ10/AN120	P02/TMCI1/SCK6/SSIBCK1/ IRQ10/AN120
7	P01/TMCI0/RXD6/SMISO6/ SSCL6/SSIBCK0/ CATLEDERR/IRQ9/AN119	P01/TMCI0/RXD6/SMISO6/ SSCL6/SSIBCK0/IRQ9/ AN119	P01/TMCI0/RXD6/SMISO6/ SSCL6/SSIBCK0/IRQ9/ AN119
8	P00/TMRI0/TXD6/SMOSI6/ SSDA6/AUDIO_CLK/ CATLATCH1/IRQ8/AN118	P00/TMRI0/TXD6/SMOSI6/ SSDA6/AUDIO_CLK/IRQ8/ AN118	P00/TMRI0/TXD6/SMOSI6/ SSDA6/AUDIO_CLK/IRQ8/ AN118
9	EMLE	PF5/WAIT#/SSILRCK0/IRQ4	PF5/WAIT#/SSILRCK0/IRQ4
10	VSS	EMLE	EMLE
11	PJ3/EDACK1/MTIOC3C/ CTS6#/RTS6#/SS6#/CTS0#/ RTS0#/SS0#/SSITXD0/ ET0_EXOUT/CATRESTOUT	PJ5/POE8#/CTS2#/RTS2#/ SS2#/SSIRXD0/EPLSOUT0	PJ5/POE8#/CTS2#/RTS2#/ SS2#/SSIRXD0
12	VCL	VSS	VSS
13	VBATT	PJ3/EDACK1/MTIOC3C/ CTS6#/RTS6#/SS6#/CTS0#/ RTS0#/SS0#/SSITXD0/ ET0_EXOUT	PJ3/EDACK1/MTIOC3C/ CTS6#/RTS6#/SS6#/CTS0#/ RTS0#/SS0#/SSITXD0/ ET0_EXOUT
14	MD/FINED	VCL	VCL
15	XCIN	VBATT	VBATT
16	XCOUT	MD/FINED	MD/FINED
17	RES#	XCIN	XCIN
18	XTAL/P37	XCOUT	XCOUT
19	VSS	RES#	RES#
20	EXTAL/P36	XTAL/P37	XTAL/P37
21	VCC	VSS	VSS
22	UPSEL/P35/NMI	EXTAL/P36	EXTAL/P36
23	TRST#/P34/MTIOC0A/ TMCI3/PO12/POE10#/SCK6/ SCK0/ET0_LINKSTA/ CAT0_LINKSTA/IRQ4/ DSMDAT0	VCC	VCC
24	P33/EDREQ1/MTIOC0D/ TIOCD0/TMRI3/PO11/ POE4#/POE11#/RXD6/ SMISO6/SSCL6/RXD0/ SMISO0/SSCL0/CRX0/ PCKO/IRQ3_DS/DSMCLK0	UPSEL/P35/NMI	UPSEL/P35/NMI

144-Pin LFQFP	RX72M	RX72N	RX66N
25	P32/MTIOC0C/TIOCC0/ TMO3/PO10/RTCIC2/ RTCOUT/POE0#/POE10#/ TXD6/SMOSI6/SSDA6/ TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/ VSYNC/IRQ2_DS	TRST#/P34/MTIOC0A/ TMCI3/PO12/POE10#/SCK6/ SCK0/ET0_LINKSTA/IRQ4	TRST#/P34/MTIOC0A/ TMCI3/PO12/POE10#/SCK6/ SCK0/ET0_LINKSTA/IRQ4
26	TMS/P31/MTIOC4D/TMCI2/ PO9/RTCIC1/CTS1#/RTS1#/ SS1#/SSLB0-A/ET1_MDC/ PMGI1_MDC/IRQ1_DS	P33/EDREQ1/MTIOC0D/ TIOCD0/TMRI3/PO11/ POE4#/POE11#/RXD6/ SMISO6/SSCL6/RXD0/ SMISO0/SSCL0/CRX0/ PCKO/IRQ3-DS	P33/EDREQ1/MTIOC0D/ TIOCD0/TMRI3/PO11/ POE4#/POE11#/RXD6/ SMISO6/SSCL6/RXD0/ SMISO0/SSCL0/CRX0/ PCKO/IRQ3-DS
27	TDI/P30/MTIOC4B/TMRI3/ PO8/RTCIC0/POE8#/RXD1/ SMISO1/SSCL1/MISOB-A/ ET1_MDIO/PMGI1_MDIO/ IRQ0_DS	P32/MTIOC0C/TIOCC0/ TMO3/PO10/RTCIC2/ RTCOUT/POE0#/POE10#/ TXD6/SMOSI6/SSDA6/ TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/ VSYNC/IRQ2-DS	P32/MTIOC0C/TIOCC0/ TMO3/PO10/RTCIC2/ RTCOUT/POE0#/POE10#/ TXD6/SMOSI6/SSDA6/ TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/ VSYNC/IRQ2-DS
28	TCK/P27/CS7#/MTIOC2B/ TMCI3/PO7/SCK1/ RSPCKBA/ET1_WOL/ CATIRQ	TMS/P31/MTIOC4D/TMCI2/ PO9/RTCIC1/CTS1#/RTS1#/ SS1#/SSLB0-A/ET1_MDC/ PMGI1_MDC/IRQ1-DS	TMS/P31/MTIOC4D/TMCI2/ PO9/RTCIC1/CTS1#/RTS1#/ SS1#/SSLB0-A/IRQ1-DS
29	TDO/P26/CS6#/MTIOC2A/ TMO1/PO6/TXD1/SMOSI1/ SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A/ET1_EXOUT/ CATLINKACT1	TDI/P30/MTIOC4B/TMRI3/ PO8/RTCIC0/POE8#/RXD1/ SMISO1/SSCL1/MISOB-A/ ET1_MDIO/PMGI1_MDIO/ IRQ0-DS	TDI/P30/MTIOC4B/TMRI3/ PO8/RTCIC0/POE8#/RXD1/ SMISO1/SSCL1/MISOB-A/ IRQ0-DS
30	CLKOUT/P25/CS5#/ EDACK1/MTIOC4C/ MTCLKB/TIOCA4/PO5/ RXD3/SMISO3/SSCL3/ SSIDATA1/SDHI_CD/ HSYNC/ADTRG0#	TCK/P27/CS7#/MTIOC2B/ TMCI3/PO7/SCK1/ RSPCKB-A/ET1_WOL	TCK/P27/CS7#/MTIOC2B/ TMCI3/PO7/SCK1/ RSPCKB-A
31	P24/CS4#/EDREQ1/ MTIOC4A/MTCLKA/TIOCB4/ TMRI1/PO4/SCK3/ USB0_VBUSEN/SSIBCK1/ SDHI_WP/PIXCLK	TDO/P26/CS6#/MTIOC2A/ TMO1/PO6/TXD1/SMOSI1/ SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A/ET1_EXOUT	TDO/P26/CS6#/MTIOC2A/ TMO1/PO6/TXD1/SMOSI1/ SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A
32	P23/EDACK0/MTIOC3D/ MTCLKD/TIOCD3/PO3/ GTIOC0A/TXD3/SMOSI3/ SSDA3/CTS0#/RTS0#/SS0#/ CTX1/SSIBCK0/SDHI_D1C/ PIXD7	CLKOUT/P25/CS5#/ EDACK1/MTIOC4C/ MTCLKB/TIOCA4/PO5/ RXD3/SMISO3/SSCL3/ SSIDATA1/SDHI_CD/ HSYNC/ADTRG0#	CLKOUT/P25/CS5#/ EDACK1/MTIOC4C/ MTCLKB/TIOCA4/PO5/ RXD3/SMISO3/SSCL3/ SSIDATA1/SDHI_CD/ HSYNC/ADTRG0#
33	P22/EDREQ0/MTIOC3B/ MTCLKC/TIOCC3/TMO0/ PO2/GTIOC1A/SCK0/ USB0_OVRCURB/ AUDIO_CLK/SDHI_D0C/ PIXD6	P24/CS4#/EDREQ1/ MTIOC4A/MTCLKA/TIOCB4/ TMRI1/PO4/SCK3/ USB0_VBUSEN/SSIBCK1/ SDHI_WP/PIXCLK	P24/CS4#/EDREQ1/ MTIOC4A/MTCLKA/TIOCB4/ TMRI1/PO4/SCK3/ USB0_VBUSEN/SSIBCK1/ SDHI_WP/PIXCLK

144-Pin LFQFP	RX72M	RX72N	RX66N
34	P21/MTIOC1B/MTIOC4A/ TIOCA3/TMCI0/PO1/ GTIOC2A/RXD0/SMISO0/ SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/ SDHI_CLK-C/PIXD5/IRQ9	P23/EDACK0/MTIOC3D/ MTCLKD/TIOCD3/PO3/ GTIOC0A/TXD3/SMOSI3/ SSDA3/CTS0#/RTS0#/SS0#/ CTX1/SSIBCK0/SDHI_D1-C/ PIXD7	P23/EDACK0/MTIOC3D/ MTCLKD/TIOCD3/PO3/ GTIOC0A/TXD3/SMOSI3/ SSDA3/CTS0#/RTS0#/SS0#/ CTX1/SSIBCK0/SDHI_D1-C/ PIXD7
35	P20/MTIOC1A/TIOCB3/ TMRI0/PO0/TXD0/SMOSI0/ SSDA0/SDA1/USB0_ID/ SSIRXD0/SDHI_CMD-C/ PIXD4/IRQ8	P22/EDREQ0/MTIOC3B/ MTCLKC/TIOCC3/TMO0/ PO2/GTIOC1A/SCK0/ USB0_OVRCURB/ AUDIO_CLK/SDHI_D0-C/ PIXD6	P22/EDREQ0/MTIOC3B/ MTCLKC/TIOCC3/TMO0/ PO2/GTIOC1A/SCK0/ USB0_OVRCURB/ AUDIO_CLK/SDHI_D0-C/ PIXD6
36	P17/MTIOC3A/MTIOC3B/ MTIOC4B/TIOCB0/TCLKD/ TMO1/PO15/POE8#/ GTIOC0B/SCK1/TXD3/ SMOSI3/SSDA3/SDA2_DS/ SSITXD0/EPLSOUT0/ CATSYNC0/SDHI_D3C/ PIXD3/IRQ7/ADTRG1#	P21/MTIOC1B/MTIOC4A/ TIOCA3/TMCI0/PO1/ GTIOC2A/RXD0/SMISO0/ SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/ SDHI_CLK-C/ PIXD5/IRQ9	P21/MTIOC1B/MTIOC4A/ TIOCA3/TMCI0/PO1/ GTIOC2A/RXD0/SMISO0/ SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/ SDHI_CLK-C/ PIXD5/IRQ9
37	P87/MTIOC4C/TIOCA2/ GTIOC1B/SMOSI10/ SSDA10/TXD10/EPLSOUT1/ CATSYNC1/SDHI_D2C/ PIXD2	P20/MTIOC1A/TIOCB3/ TMRI0/PO0/TXD0/SMOSI0/ SSDA0/SDA1/USB0_ID/ SSIRXD0/SDHI_CMD-C/ PIXD4/IRQ8	P20/MTIOC1A/TIOCB3/ TMRI0/PO0/TXD0/SMOSI0/ SSDA0/SDA1/USB0_ID/ SSIRXD0/SDHI_CMD-C/ PIXD4/IRQ8
38	P16/MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOUT/TXD1/ SMOSI1/SSDA1/RXD3/ SMISO3/SSCL3/SCL2_DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB/IRQ6/ ADTRG0#	P17/MTIOC3A/MTIOC3B/ MTIOC4B/TIOCB0/TCLKD/ TMO1/PO15/POE8#/ GTIOC0B/SCK1/TXD3/ SMOSI3/SSDA3/SDA2-DS/ SSITXD0/EPLSOUT0/ SDHI_D3-C/PIXD3/IRQ7/ ADTRG1#	P17/MTIOC3A/MTIOC3B/ MTIOC4B/TIOCB0/TCLKD/ TMO1/PO15/POE8#/ GTIOC0B/SCK1/TXD3/ SMOSI3/SSDA3/SDA2-DS/ SSITXD0/SDHI_D3-C/PIXD3/ IRQ7/ ADTRG1#
39	P86/MTIOC4D/TIOCA0/ GTIOC2B/SMISO10/ SSCL10/RXD10/ CATLINKACT0/PIXD1	P87/MTIOC4C/TIOCA2/ GTIOC1B/SMOSI10/ SSDA10/TXD10/EPLSOUT1/ SDHI_D2-C/PIXD2	P87/MTIOC4C/TIOCA2/ GTIOC1B/SMOSI10/ SSDA10/TXD10/ SDHI_D2-C/PIXD2
40	P15/MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCI2/ PO13/GTETRGA/RXD1/ SMISO1/SSCL1/SCK3/ CRX1_DS/SSILRCK1/ CATLEDRUN/PIXD0/IRQ5	P16/MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOUT/TXD1/ SMOSI1/ SSDA1/RXD3/ SMISO3/ SSCL3/SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB/IRQ6/ ADTRG0#	P16/MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOUT/TXD1/ SMOSI1/ SSDA1/RXD3/ SMISO3/ SSCL3/SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB/IRQ6/ ADTRG0#
41	P13/MTIOC0B/TIOCA5/ TMO3/PO13/GTADSM1/ TXD2/SMOSI2/SSDA2/ SDA0[FM+]/IRQ3/ADTRG1#	P86/MTIOC4D/TIOCA0/ GTIOC2B/SMISO10/ SSCL10/RXD10/PIXD1	P86/MTIOC4D/TIOCA0/ GTIOC2B/SMISO10/ SSCL10/ RXD10/PIXD1

144-Pin LFQFP	RX72M	RX72N	RX66N
42	P14/MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15/GTETRGD/CTS1#/ RTS1#/SS1#/CTX1/ USB0_OVRCURA/IRQ4	P15/MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCI2/ PO13/GTETRGA/RXD1/ SMISO1/ SSCL1/SCK3/ CRX1-DS/ SSILRCK1/ PIXD0/IRQ5	P15/MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCI2/ PO13/GTETRGA/RXD1/ SMISO1/ SSCL1/SCK3/ CRX1-DS/ SSILRCK1/ PIXD0/IRQ5
43	P12/TMCI1/GTADSM0/ RXD2/SMISO2/SSCL2/ SCL0[FM+]/IRQ2	P14/MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15/GTETRGD/CTS1#/ RTS1#/ SS1#/CTX1/ USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15/GTETRGD/CTS1#/ RTS1#/ SS1#/CTX1/ USB0_OVRCURA/IRQ4
44	VCC_USB	P13/MTIOC0B/TIOCA5/ TMO3/PO13/GTADSM1/ TXD2/SMOSI2/SSDA2/ SDA0[FM+]/IRQ3/ADTRG1#	P13/MTIOC0B/TIOCA5/ TMO3/PO13/GTADSM1/ TXD2/SMOSI2/SSDA2/ SDA0[FM+]/IRQ3/ADTRG1#
45	USB0_DM	P12/TMCI1/GTADSM0/ RXD2/SMISO2/SSCL2/ SCL0[FM+]/IRQ2	P12/TMCI1/GTADSM0/ RXD2/SMISO2/SSCL2/ SCL0[FM+]/IRQ2
46	USB0_DP	VCC_USB	VCC_USB
47	VSS_USB	USB0_DM	USB0_DM
48	CLKOUT25M/PJ2/TXD8/ SMOSI8/SSDA8	USB0_DP	USB0_DP
49	CLKOUT25M/P56/EDACK1/ MTIOC3C/TIOCA1/SCK7/ DSMDAT1	VSS_USB	VSS_USB
50	TRDATA3/P55/D0[A0/D0]/ WAIT#/EDREQ0/MTIOC4D/ TMO3/TXD7/SMOSI7/ SSDA7/CRX1/ET0_EXOUT/ IRQ10	CLKOUT25M/P56/EDACK1/ MTIOC3C/TIOCA1/SCK7	CLKOUT25M/P56/EDACK1/ MTIOC3C/TIOCA1/SCK7
51	TRDATA2/P54/ALE/ D1[A1/D1]/EDACK0/ MTIOC4B/TMCI1/CTS2#/ RTS2#/SS2#/CTX1/ ET0_LINKSTA/ CAT0_LINKSTA	TRDATA3/P55/D0[A0/D0]/ WAIT#/EDREQ0/MTIOC4D/ TMO3/TXD7/SMOSI7/ SSDA7/CRX1/ET0_EXOUT/ IRQ10	TRDATA3/P55/D0[A0/D0]/ WAIT#/EDREQ0/MTIOC4D/ TMO3/TXD7/SMOSI7/ SSDA7/CRX1/ET0_EXOUT/ IRQ10
52	P53*1/BCLK	TRDATA2/P54/ALE/ D1[A1/D1]/EDACK0/ MTIOC4B/TMCI1/CTS2#/ RTS2#/SS2#/CTX1/ ET0_LINKSTA	TRDATA2/P54/ALE/ D1[A1/D1]/EDACK0/ MTIOC4B/TMCI1/CTS2#/ RTS2#/SS2#/CTX1/ ET0_LINKSTA
53	P52/RD#/RXD2/SMISO2/ SSCL2/SSLB3-A/ CATLEDSTER	P53*1/BCLK	P53*1/BCLK
54	P51/WR1#/BC1#/WAIT#/ SCK2/SSLB2-A	P52/RD#/RXD2/SMISO2/ SSCL2/SSLB3-A	P52/RD#/RXD2/SMISO2/ SSCL2/SSLB3-A
55	P50/WR0#/WR#/TXD2/ SMOSI2/SSDA2/SSLB1-A/ CATLEDERR	P51/WR1#/BC1#/WAIT#/ SCK2/SSLB2-A	P51/WR1#/BC1#/WAIT#/ SCK2/SSLB2-A
56	VSS	P50/WR0#/WR#/TXD2/ SMOSI2/SSDA2/SSLB1-A	P50/WR0#/WR#/TXD2/ SMOSI2/SSDA2/SSLB1-A

144-Pin LFQFP	RX72M	RX72N	RX66N
57	TRCLK/P83/EDACK1/ MTIOC4C/GTIOC0A/SCK10/ SS10#/CTS10#/ET0_CRS/ RMII0_CRS_DV/ CAT0_RX_DV/DSMCLK1	VSS	VSS
58	VCC	TRCLK/P83/EDACK1/ MTIOC4C/GTIOC0A/SCK10/ SS10#/CTS10#/ET0_CRS/ RMII0_CRS_DV	TRCLK/P83/EDACK1/ MTIOC4C/GTIOC0A/SCK10/ SS10#/CTS10#/ET0_CRS/ RMII0_CRS_DV
59	UB/PC7/A23/CS0#/ MTIOC3A/MTCLKB/TMO2/ PO31/TOC0/CACREF/ GTIOC3A/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/ ET0_COL/MMC_D7-A/ IRQ14	VCC	VCC
60	PC6/D2[A2/D2]/A22/CS1#/ MTIOC3C/MTCLKA/TMCI2/ PO30/TIC0/GTIOC3B/RXD8/ SMISO8/SSCL8/SMISO10/ SSCL10/RXD10/MOSIA-A/ ET0_ETXD3/CAT0_ETXD3/ CATLATCH1/MMC_D6-A/ IRQ13	UB/PC7/A23/CS0#/ MTIOC3A/MTCLKB/TMO2/ PO31/TOC0/CACREF/ GTIOC3A/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/ET0_COL/ MMC_D7-A/IRQ14	UB/PC7/A23/CS0#/ MTIOC3A/MTCLKB/TMO2/ PO31/TOC0/CACREF/ GTIOC3A/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/ET0_COL/ MMC_D7-A/IRQ14
61	PC5/D3[A3/D3]/A21/CS2#/ WAIT#/MTIOC3B/MTCLKD/ TMRI2/PO29/GTIOC1A/ SCK8/RTS8#/SCK10/ RSPCKAA/ET0_ETXD2/ CAT0_ETXD2/MMC_D5-A	PC6/D2[A2/D2]/A22/CS1#/ MTIOC3C/MTCLKA/TMCI2/ PO30/TIC0/GTIOC3B/RXD8/ SMISO8/SSCL8/SMISO10/ SSCL10/RXD10/MOSIA-A/ ET0_ETXD3/MMC_D6-A/ IRQ13	PC6/D2[A2/D2]/A22/CS1#/ MTIOC3C/MTCLKA/TMCI2/ PO30/TIC0/GTIOC3B/RXD8/ SMISO8/SSCL8/SMISO10/ SSCL10/RXD10/MOSIA-A/ ET0_ETXD3/MMC_D6-A/ IRQ13
62	TRSYNC/P82/EDREQ1/ MTIOC4A/PO28/GTIOC2A/ SMOSI10/SSDA10/TXD10/ ET0_ETXD1/RMII0_TXD1/ CAT0_ETXD1/ CATI2CDATA/MMC_D4-A	PC5/D3[A3/D3]/A21/CS2#/ WAIT#/MTIOC3B/MTCLKD/ TMRI2/PO29/GTIOC1A/ SCK8/RTS8#/SCK10/ RSPCKA-A/ET0_ETXD2/ MMC_D5-A	PC5/D3[A3/D3]/A21/CS2#/ WAIT#/MTIOC3B/MTCLKD/ TMRI2/PO29/GTIOC1A/ SCK8/RTS8#/SCK10/ RSPCKA-A/ET0_ETXD2/ MMC_D5-A
63	TRDATA1/P81/EDACK0/ MTIOC3D/PO27/GTIOC0B/ SMISO10/SSCL10/RXD10/ ET0_ETXD0/RMII0_TXD0/ CAT0_ETXD0/CATI2CCLK/ QIO3-A/SDHI_CD/ MMC_D3-A	TRSYNC/P82/EDREQ1/ MTIOC4A/PO28/GTIOC2A/ SMOSI10/SSDA10/TXD10/ ET0_ETXD1/RMII0_TXD1/ MMC_D4-A	TRSYNC/P82/EDREQ1/ MTIOC4A/PO28/GTIOC2A/ SMOSI10/SSDA10/TXD10/ ET0_ETXD1/RMII0_TXD1/ MMC_D4-A
64	TRDATA0/P80/EDREQ0/ MTIOC3B/PO26/SCK10/ RTS10#/ET0_TX_EN/ RMII0_TXD_EN/ CAT0_TX_EN/CATLATCH0/ QIO2-A/SDHI_WP/ MMC_D2-A	TRDATA1/P81/EDACK0/ MTIOC3D/PO27/GTIOC0B/ SMISO10/SSCL10/RXD10/ ET0_ETXD0/RMII0_TXD0/ QIO3-A/SDHI_CD/ MMC_D3-A	TRDATA1/P81/EDACK0/ MTIOC3D/PO27/GTIOC0B/ SMISO10/SSCL10/RXD10/ ET0_ETXD0/RMII0_TXD0/ QIO3-A/SDHI_CD/ MMC_D3-A

144-Pin LFQFP	RX72M	RX72N	RX66N
65	PC4/A20/CS3#/MTIOC3D/ MTCLKC/TMCI1/PO25/ POE0#/GTETRGC/SCK5/ SS8#/CTS8#/SS10#/ CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK/ CAT0_TX_CLK/CATSYNC0/ QMI-A/QIO1-A/SDHI_D1A/ MMC_D1-A	TRDATA0/P80/EDREQ0/ MTIOC3B/PO26/SCK10/ RTS10#/ET0_TX_EN/ RMII0_TXD_EN/QIO2-A/ SDHI_WP/MMC_D2-A	TRDATA0/P80/EDREQ0/ MTIOC3B/PO26/SCK10/ RTS10#/ET0_TX_EN/ RMII0_TXD_EN/QIO2-A/ SDHI_WP/MMC_D2-A
66	PC3/A19/MTIOC4D/TCLKB/ PO24/GTIOC1B/TXD5/ SMOSI5/SSDA5/ ET0_TX_ER/QMO-A/ QIO0-A/SDHI_D0A/ MMC_D0-A	PC4/A20/CS3#/MTIOC3D/ MTCLKC/TMCI1/PO25/ POE0#/GTETRGC/SCK5/ CTS8#/SS8#/SS10#/ CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK/QMI-A/ QIO1-A/SDHI_D1-A/ MMC_D1-A	PC4/A20/CS3#/MTIOC3D/ MTCLKC/TMCI1/PO25/ POE0#/GTETRGC/SCK5/ CTS8#/SS8#/SS10#/ CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK/QMI-A/ QIO1-A/SDHI_D1-A/ MMC_D1-A
67	TRDATA7/P77/CS7#/PO23/ SMOSI11/SSDA11/TXD11/ ET0_RX_ER/RMII0_RX_ER/ CAT0_RX_ER/QSPCLK-A/ SDHI_CLK-A/MMC_CLK-A	PC3/A19/MTIOC4D/TCLKB/ PO24/GTIOC1B/TXD5/ SMOSI5/SSDA5/ ET0_TX_ER/QMO-A/ QIO0-A/SDHI_D0-A/ MMC_D0-A	PC3/A19/MTIOC4D/TCLKB/ PO24/GTIOC1B/TXD5/ SMOSI5/SSDA5/ ET0_TX_ER/QMO-A/ QIO0-A/SDHI_D0-A/ MMC_D0-A
68	TRDATA6/P76/CS6#/PO22/ SMISO11/SSCL11/RXD11/ ET0_RX_CLK/REF50CK0/ CAT0_RX_CLK/QSSL-A/ SDHI_CMD-A/MMC_CMD-A	TRDATA7/P77/CS7#/PO23/ SMOSI11/SSDA11/TXD11/ ET0_RX_ER/RMII0_RX_ER/ QSPCLK-A/SDHI_CLK-A/ MMC_CLK-A	TRDATA7/P77/CS7#/PO23/ SMOSI11/SSDA11/TXD11/ ET0_RX_ER/RMII0_RX_ER/ QSPCLK-A/SDHI_CLK-A/ MMC_CLK-A
69	PC2/A18/MTIOC4B/TCLKA/ PO21/GTIOC2B/RXD5/ SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV/CAT0_RX_DV/ SDHI_D3-A/MMC_CD-A	TRDATA6/P76/CS6#/PO22/ SMISO11/SSCL11/RXD11/ ET0_RX_CLK/REF50CK0/ QSSL-A/SDHI_CMD-A/ MMC_CMD-A	TRDATA6/P76/CS6#/PO22/ SMISO11/SSCL11/RXD11/ ET0_RX_CLK/REF50CK0/ QSSL-A/SDHI_CMD-A/ MMC_CMD-A
70	TRSYNC1/P75/CS5#/PO20/ SCK11/RTS11#/ ET0_ERXD0/RMII0_RXD0/ CAT0_ERXD0/SDHI_D2-A/ MMC_RES#-A/DSMDAT2	PC2/A18/MTIOC4B/TCLKA/ PO21/GTIOC2B/RXD5/ SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV/SDHI_D3-A/ MMC_CD-A	PC2/A18/MTIOC4B/TCLKA/ PO21/GTIOC2B/RXD5/ SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV/SDHI_D3-A/ MMC_CD-A
71	TRDATA5/P74/A20/CS4#/ PO19/SS11#/CTS11#/ ET0_ERXD1/RMII0_RXD1/ CAT0_ERXD1/DSMCLK2	TRSYNC1/P75/CS5#/PO20/ SCK11/RTS11#/ ET0_ERXD0/RMII0_RXD0/ SDHI_D2-A/MMC_RES#-A	TRSYNC1/P75/CS5#/PO20/ SCK11/RTS11#/ ET0_ERXD0/RMII0_RXD0/ SDHI_D2-A/MMC_RES#-A
72	PC1/A17/MTIOC3A/TCLKD/ PO18/SCK5/SSLA2-A/ ET0_ERXD2/CAT0_ERXD2/ IRQ12	TRDATA5/P74/A20/CS4#/ PO19/SS11#/CTS11#/ ET0_ERXD1/RMII0_RXD1	TRDATA5/P74/A20/CS4#/ PO19/SS11#/CTS11#/ ET0_ERXD1/RMII0_RXD1
73	VCC	PC1/A17/MTIOC3A/TCLKD/ PO18/SCK5/SSLA2-A/ ET0_ERXD2/IRQ12	PC1/A17/MTIOC3A/TCLKD/ PO18/SCK5/SSLA2-A/ ET0_ERXD2/IRQ12
74	PC0/A16/MTIOC3C/TCLKC/ PO17/CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3/ CAT0_ERXD3/IRQ14	VCC	VCC

144-Pin LFQFP	RX72M	RX72N	RX66N
75	VSS	PC0/A16/MTIOC3C/TCLKC/ PO17/CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3/ IRQ14	PC0/A16/MTIOC3C/TCLKC/ PO17/CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3/ IRQ14
76	TRDATA4/P73/CS3#/PO16/ ET0_WOL	VSS	VSS
77	PB7/A15/MTIOC3B/TIOCB5/ PO31/TXD9/SMOSI9/ SSDA9/SMOSI11/ SSDA11/TXD11/ET0_CRS/ RMII0_CRS_DV/ CAT0_RX_DV	TRDATA4/P73/CS3#/PO16/ ET0_WOL	TRDATA4/P73/CS3#/PO16/ ET0_WOL
78	PB6/A14/MTIOC3D/TIOCA5/ PO30/RXD9/SMISO9/ SSCL9/SMISO11/SSCL11/ RXD11/ET0_ETXD1/ RMII0_TXD1/CAT0_ETXD1	PB7/A15/MTIOC3B/TIOCB5/ PO31/TXD9/SMOSI9/ SSDA9/SMOSI11/SSDA11/ TXD11/ET0_CRS/ RMII0_CRS_DV	PB7/A15/MTIOC3B/TIOCB5/ PO31/TXD9/SMOSI9/ SSDA9/SMOSI11/SSDA11/ TXD11/ET0_CRS/ RMII0_CRS_DV
79	PB5/A13/MTIOC2A/ MTIOC1B/TIOCB4/TMRI1/ PO29/POE4#/SCK9/RTS9#/ SCK11/ET0_ETXD0/ RMII0_TXD0/CAT0_ETXD0/ LCD_CLK-B	PB6/A14/MTIOC3D/TIOCA5/ PO30/RXD9/SMISO9/ SSCL9/SMISO11/SSCL11/ RXD11/ET0_ETXD1/ RMII0_TXD1	PB6/A14/MTIOC3D/TIOCA5/ PO30/RXD9/SMISO9/ SSCL9/SMISO11/SSCL11/ RXD11/ET0_ETXD1/ RMII0_TXD1
80	PB4/A12/TIOCA4/PO28/ SS9#/CTS9#/SS11#/ CTS11#/RTS11#/ ET0_TX_EN/ RMII0_TXD_EN/ CAT0_TXEN/LCD_TCON0-B	PB5/A13/MTIOC2A/ MTIOC1B/TIOCB4/TMRI1/ PO29/POE4#/SCK9/RTS9#/ SCK11/ET0_ETXD0/ RMII0_TXD0/LCD_CLK-B	PB5/A13/MTIOC2A/ MTIOC1B/TIOCB4/TMRI1/ PO29/POE4#/SCK9/RTS9#/ SCK11/ET0_ETXD0/ RMII0_TXD0/LCD_CLK-B
81	PB3/A11/MTIOC0A/ MTIOC4A/TIOCD3/TCLKD/ TMO0/PO27/POE11#/SCK4/ SCK6/ET0_RX_ER/ RMII0_RX_ER/ CAT0_RX_ER/ LCD_TCON1-B	PB4/A12/TIOCA4/PO28/ CTS9#/SS9#/SS11#/ CTS11#/RTS11#/ ET0_TX_EN/ RMII0_TXD_EN/ LCD_TCON0-B	PB4/A12/TIOCA4/PO28/ CTS9#/SS9#/SS11#/ CTS11#/RTS11#/ ET0_TX_EN/ RMII0_TXD_EN/ LCD_TCON0-B
82	PB2/A10/TIOCC3/TCLKC/ PO26/CTS4#/RTS4#/SS4#/ CTS6#/RTS6#/SS6#/ ET0_RX_CLK/REF50CK0/ CAT0_RX_CLK/ LCD_TCON2-B	PB3/A11/MTIOC0A/ MTIOC4A/TIOCD3/TCLKD/ TMO0/PO27/POE11#/SCK4/ SCK6/ET0_RX_ER/ RMII0_RX_ER/ LCD_TCON1-B	PB3/A11/MTIOC0A/ MTIOC4A/TIOCD3/TCLKD/ TMO0/PO27/POE11#/SCK4/ SCK6/ET0_RX_ER/ RMII0_RX_ER/ LCD_TCON1-B
83	PB1/A9/MTIOC0C/ MTIOC4C/TIOCB3/TMCI0/ PO25/TXD4/SMOSI4/ SSDA4/TXD6/SMOSI6/ SSDA6/ET0_ERXD0/ RMII0_RXD0/CAT0_ERXD0/ LCD_TCON3-B/IRQ4_DS	PB2/A10/TIOCC3/TCLKC/ PO26/CTS4#/RTS4#/SS4#/ CTS6#/RTS6#/SS6#/ ET0_RX_CLK/REF50CK0/ LCD_TCON2-B	PB2/A10/TIOCC3/TCLKC/ PO26/CTS4#/RTS4#/SS4#/ CTS6#/RTS6#/SS6#/ ET0_RX_CLK/REF50CK0/ LCD_TCON2-B

144-Pin LFQFP	RX72M	RX72N	RX66N
84	PB0/A8/MTIC5W/TIOCA3/ PO24/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/ SSCL6/ET0_ERXD1/ RMII0_RXD1/CAT0_ERXD1/ LCD_DATA0-B/IRQ12	PB1/A9/MTIOC0C/ MTIOC4C/TIOCB3/TMCI0/ PO25/TXD4/SMOSI4/ SSDA4/TXD6/SMOSI6/ SSDA6/ET0_ERXD0/ RMII0_RXD0/ LCD_TCON3-B/IRQ4-DS	PB1/A9/MTIOC0C/ MTIOC4C/TIOCB3/TMCI0/ PO25/TXD4/SMOSI4/ SSDA4/TXD6/SMOSI6/ SSDA6/ET0_ERXD0/ RMII0_RXD0/ LCD_TCON3-B/IRQ4-DS
85	PA7/A7/TIOCB2/PO23/ MISOA-B/ET0_WOL/ LCD_DATA1-B	P72/A19/CS2#/ET0_MDC/ PMGI0_MDC	P72/A19/CS2#/ET0_MDC/ PMGI0_MDC
86	PA6/A6/MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE10#/GTETRGB/CTS5#/ RTS5#/SS5#/MOSIA-B/ ET0_EXOUT/ CATRESTOUT/ LCD_DATA2-B	P71/A18/CS1#/ET0_MDIO/ PMGI0_MDIO	P71/A18/CS1#/ET0_MDIO/ PMGI0_MDIO
87	PA5/A5/MTIOC6B/TIOCB1/ PO21/GTIOC0A/RSPCKAB/ ET0_LINKSTA/ CAT0_LINKSTA/ LCD_DATA3-B	PB0/A8/MTIC5W/TIOCA3/ PO24/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/ SSCL6/ET0_ERXD1/ RMII0_RXD1/ LCD_DATA0-B/IRQ12	PB0/A8/MTIC5W/TIOCA3/ PO24/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/ SSCL6/ET0_ERXD1/ RMII0_RXD1/ LCD_DATA0-B/IRQ12
88	VCC	PA7/A7/TIOCB2/PO23/ MISOA-B/ET0_WOL/ LCD_DATA1-B	PA7/A7/TIOCB2/PO23/ MISOA-B/ET0_WOL/ LCD_DATA1-B
89	PA4/A4/MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20/TXD5/ SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/CAT0_MDC/ CATIRQ/PMGI0_MDC/ LCD_DATA4-B/IRQ5_DS	PA6/A6/MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE10#/GTETRGB/CTS5#/ RTS5#/SS5#/MOSIA-B/ ET0_EXOUT/LCD_DATA2-B	PA6/A6/MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE10#/GTETRGB/CTS5#/ RTS5#/SS5#/MOSIA-B/ ET0_EXOUT/LCD_DATA2-B
90	VSS	PA5/A5/MTIOC6B/TIOCB1/ PO21/GTIOC0A/RSPCKA-B/ ET0_LINKSTA/ LCD_DATA3-B	PA5/A5/MTIOC6B/TIOCB1/ PO21/GTIOC0A/RSPCKA-B/ ET0_LINKSTA/ LCD_DATA3-B
91	PA3/A3/MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19/ RXD5/SMISO5/SSCL5/ ET0_MDIO/CAT0_MDIO/ PMGI0_MDIO/ LCD_DATA5-B/IRQ6_DS	VCC	VCC
92	PG7/ET1_TX_ER	PA4/A4/MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20/TXD5/ SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/PMGI0_MDC/ LCD_DATA4-B/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20/TXD5/ SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/PMGI0_MDC/ LCD_DATA4-B/IRQ5-DS
93	PA2/A2/MTIOC7A/PO18/ GTIOC1A/RXD5/SMISO5/ SSCL5/SSLA3-B/ CATLINKACT1/ LCD_DATA6-B	VSS	VSS

144-Pin LFQFP	RX72M	RX72N	RX66N
94	PG6/ET1_ETXD3/ CAT1_ETXD3	PA3/A3/MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19/ RXD5/SMISO5/SSCL5/ ET0_MDIO/PMGI0_MDIO/ LCD_DATA5-B/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19/ RXD5/SMISO5/SSCL5/ ET0_MDIO/PMGI0_MDIO/ LCD_DATA5-B/IRQ6-DS
95	PA1/A1/MTIOC0B/MTCLKC/ MTIOC7B/TIOCB0/PO17/ GTIOC2A/SCK5/SSLA2-B/ ET0_WOL/LCD_DATA7-B/ IRQ11	PA2/A2/MTIOC7A/PO18/ GTIOC1A/RXD5/SMISO5/ SSCL5/SSLA3-B/ LCD_DATA6-B	PA2/A2/MTIOC7A/PO18/ GTIOC1A/RXD5/SMISO5/ SSCL5/SSLA3-B/ LCD_DATA6-B
96	PG5/ET1_ETXD2/ CAT1_ETXD2	PA1/A1/MTIOC0B/MTCLKC/ MTIOC7B/TIOCB0/PO17/ GTIOC2A/SCK5/SSLA2-B/ ET0_WOL/LCD_DATA7-B/ IRQ11	PA1/A1/MTIOC0B/MTCLKC/ MTIOC7B/TIOCB0/PO17/ GTIOC2A/SCK5/SSLA2-B/ ET0_WOL/LCD_DATA7-B/ IRQ11
97	PA0/BC0#/A0/MTIOC4A/ MTIOC6D/TIOCA0/PO16/ CACREF/GTIOC0B/ SSLA1-B/ET0_TX_EN/ RMII0_TXD_EN/ CAT0_TX_EN/CATLEDRUN/ LCD_DATA8-B	PA0/BC0#/A0/MTIOC4A/ MTIOC6D/TIOCA0/PO16/ CACREF/GTIOC0B/ SSLA1-B/ET0_TX_EN/ RMII0_TXD_EN/ LCD_DATA8-B	PA0/BC0#/A0/MTIOC4A/ MTIOC6D/TIOCA0/PO16/ CACREF/GTIOC0B/ SSLA1-B/ET0_TX_EN/ RMII0_TXD_EN/ LCD_DATA8-B
98	P67/CS7#/MTIOC7C/ GTIOC1B/CRX2/ EPLSOUT1/CATSYNC1/ IRQ15	P67/DQM1/CS7#/MTIOC7C/ GTIOC1B/CRX2/ EPLSOUT1/IRQ15	P67/DQM1/CS7#/MTIOC7C/ GTIOC1B/CRX2/IRQ15
99	P66/CS6#/MTIOC7D/ GTIOC2B/CTX2	P66/DQM0/CS6#/MTIOC7D/ GTIOC2B/CTX2	P66/DQM0/CS6#/MTIOC7D/ GTIOC2B/CTX2
100	PG2/ET1_TX_CLK/ CAT1_TX_CLK	P65/CKE/CS5#	P65/CKE/CS5#
101	P65/CS5#	PE7/D15[A15/D15]/ D7[A7/D7]/MTIOC6A/TOC1/ GTIOC3A/MISOB-B/ SDHI_WP/MMC_RES#-B/ LCD_DATA9-B/IRQ7/AN105	PE7/D15[A15/D15]/ D7[A7/D7]/MTIOC6A/TOC1/ GTIOC3A/MISOB-B/ SDHI_WP/MMC_RES#-B/ LCD_DATA9-B/IRQ7/AN105
102	PE7/D15[A15/D15]/ D7[A7/D7]/MTIOC6A/TOC1/ GTIOC3A/MISOB-B/ SDHI_WP/MMC_RES#-B/ LCD_DATA9-B/IRQ7/AN105	PE6/D14[A14/D14]/ D6[A6/D6]/MTIOC6C/TIC1/ GTIOC3B/MOSIB-B/ SDHI_CD/MMC_CD-B/ LCD_DATA10-B/IRQ6/ AN104	PE6/D14[A14/D14]/ D6[A6/D6]/MTIOC6C/TIC1/ GTIOC3B/MOSIB-B/ SDHI_CD/MMC_CD-B/ LCD_DATA10-B/IRQ6/ AN104
103	PE6/D14[A14/D14]/ D6[A6/D6]/MTIOC6C/TIC1/ GTIOC3B/MOSIB-B/ SDHI_CD/MMC_CD-B/ LCD_DATA10-B/IRQ6/ AN104	VCC	VCC
104	VCC	P70/SDCLK	P70/SDCLK
105	VSS	VSS	VSS

144-Pin LFQFP	RX72M	RX72N	RX66N
106	PE5/D13[A13/D13]/ D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/ RSPCKBB/ET0_RX_CLK/ REF50CK0/CAT0_RX_CLK/ LCD_DATA11-B/IRQ5/ AN103	PE5/D13[A13/D13]/ D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/ RSPCKB-B/ET0_RX_CLK/ REF50CK0/LCD_DATA11-B/ IRQ5/AN103	PE5/D13[A13/D13]/ D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/ RSPCKB-B/ET0_RX_CLK/ REF50CK0/LCD_DATA11-B/ IRQ5/AN103
107	PE4/D12[A12/D12]/ D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/ SSLB0-B/ET0_ERXD2/ CAT0_ERXD2/ LCD_DATA12-B/AN102	PE4/D12[A12/D12]/ D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/ SSLB0-B/ET0_ERXD2/ LCD_DATA12-B/AN102	PE4/D12[A12/D12]/ D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/ SSLB0-B/ET0_ERXD2/ LCD_DATA12-B/AN102
108	PE3/D11[A11/D11]/ D3[A3/D3]/MTIOC4B/PO26/ TOC3/POE8#/GTIOC2A/ CTS12#/RTS12#/SS12#/ ET0_ERXD3/CAT0_ERXD3/ MMC_D7-B/ LCD_DATA13-B/AN101	PE3/D11[A11/D11]/ D3[A3/D3]/MTIOC4B/PO26/ TOC3/POE8#/GTIOC2A/ CTS12#/RTS12#/SS12#/ ET0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101	PE3/D11[A11/D11]/ D3[A3/D3]/MTIOC4B/PO26/ TOC3/POE8#/GTIOC2A/ CTS12#/RTS12#/SS12#/ ET0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101
109	PE2/D10[A10/D10]/ D2[A2/D2]/MTIOC4A/PO23/ TIC3/GTIOC0B/RXD12/ SMISO12/SSCL12/RXDX12/ SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7_DS/ AN100	PE2/D10[A10/D10]/ D2[A2/D2]/MTIOC4A/PO23/ TIC3/GTIOC0B/RXD12/ SMISO12/SSCL12/RXDX12/ SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/ AN100	PE2/D10[A10/D10]/ D2[A2/D2]/MTIOC4A/PO23/ TIC3/GTIOC0B/RXD12/ SMISO12/SSCL12/RXDX12/ SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/ AN100
110	PE1/D9[A9/D9]/D1[A1/D1]/ MTIOC4C/MTIOC3B/PO18/ GTIOC1B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/ SSLB2-B/MMC_D5-B/ LCD_DATA15-B/ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/ MTIOC4C/MTIOC3B/PO18/ GTIOC1B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/ SSLB2-B/MMC_D5-B/ LCD_DATA15-B/ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/ MTIOC4C/MTIOC3B/PO18/ GTIOC1B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/ SSLB2-B/MMC_D5-B/ LCD_DATA15-B/ANEX1
111	PE0/D8[A8/D8]/D0[A0/D0]/ MTIOC3D/GTIOC2B/SCK12/ SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/ MTIOC3D/GTIOC2B/SCK12/ SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/ MTIOC3D/GTIOC2B/SCK12/ SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0
112	P64/D3[A3/D3]/CS4#/ ET1_ETXD0/RMII1_TXD0/ CAT1_ETXD0	P64/WE#/D3[A3/D3]/CS4#/ RMII1_TXD0	P64/WE#/D3[A3/D3]/CS4#
113	P63/D2[A2/D2]/CS3#/ ET1_ETXD1/RMII1_TXD1/ CAT1_ETXD1	P63/CAS#/D2[A2/D2]/CS3#/ RMII1_TXD1	P63/CAS#/D2[A2/D2]/CS3#
114	P62/D1[A1/D1]/CS2#/ ET1_ERXD0/RMII1_RXD0/ CAT1_ERXD0	P62/RAS#/D1[A1/D1]/CS2#/ RMII1_RXD0	P62/RAS#/D1[A1/D1]/CS2#
115	P61/D0[A0/D0]/CS1#/ ET1_ERXD1/RMII1_RXD1/ CAT1_ERXD1	P61/SDCS#/D0[A0/D0]/ CS1#/RMII1_RXD1	P61/SDCS#/D0[A0/D0]/ CS1#
116	VSS	VSS	VSS
117	P60/CS0#/ET1_TX_EN/ RMII1_TXD_EN/ CAT1_TX_EN	P60/CS0#/RMII1_TXD_EN	P60/CS0#
118	VCC	VCC	VCC

144-Pin LFQFP	RX72M	RX72N	RX66N
119	PD7/D7[A7/D7]/MTIC5U/ POE0#/SSLC3-A/ ET1_RX_ER/RMII1_RX_ER/ CAT1_RX_ER/QMI-B/ QIO1-B/SDHI_D1-B/ MMC_D1-B/ LCD_DATA17-B/IRQ7/ AN107	PD7/D7[A7/D7]/MTIC5U/ POE0#/SSLC3-A/ RMII1_RX_ER/QMI-B/ QIO1-B/SDHI_D1-B/ MMC_D1-B/ LCD_DATA17-B/IRQ7/ AN107	PD7/D7[A7/D7]/MTIC5U/ POE0#/SSLC3-A/QMI-B/ QIO1-B/SDHI_D1-B/ MMC_D1-B/ LCD_DATA17-B/IRQ7/ AN107
120	PG1/ET1_RX_ER/ RMII1_RX_ER/ CAT1_RX_ER	PD6/D6[A6/D6]/MTIC5V/ MTIOC8A/POE4#/SSLC2-A/ REF50CK1/QMO-B/QIO0-B/ SDHI_D0-B/MMC_D0-B/ LCD_DATA18-B/IRQ6/ AN106	PD6/D6[A6/D6]/MTIC5V/ MTIOC8A/POE4#/SSLC2-A/ QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/ LCD_DATA18-B/IRQ6/ AN106
121	PD6/D6[A6/D6]/MTIC5V/ MTIOC8A/POE4#/SSLC2-A/ ET1_RX_CLK/REF50CK1/ CAT1_RX_CLK/QMO-B/ QIO0-B/SDHI_D0B/ MMC_D0-B/ LCD_DATA18-B/IRQ6/ AN106	PD5/D5[A5/D5]/MTIC5W/ MTIOC8C/MTCLKA/ POE10#/SSLC1-A/ ET1_MDC/PMGI1_MDC/ QSPCLK-B/SDHI_CLK-B/ MMC_CLK-B/ LCD_DATA19-B/IRQ5/ AN113	PD5/D5[A5/D5]/MTIC5W/ MTIOC8C/MTCLKA/ POE10#/SSLC1-A/ QSPCLK-B/SDHI_CLK-B/ MMC_CLK-B/ LCD_DATA19-B/IRQ5/ AN113
122	PG0/ET1_RX_CLK/ REF50CK1/CAT1_RX_CLK	PD4/D4[A4/D4]/MTIOC8B/ POE11#/SSLC0-A/ ET1_MDIO/PMGI1_MDIO/ QSSL-B/SDHI_CMD-B/ MMC_CMD-B/ LCD_DATA20-B/IRQ4/ AN112	PD4/D4[A4/D4]/MTIOC8B/ POE11#/SSLC0-A/QSSL-B/ SDHI_CMD-B/MMC_CMD-B/ LCD_DATA20-B/IRQ4/ AN112
123	PD5/D5[A5/D5]/MTIC5W/ MTCLKA/MTIOC8C/ POE10#/SSLC1-A/ ET1_MDC/PMGI1_MDC/ QSPCLK-B/SDHI_CLK-B/ MMC_CLK-B/ LCD_DATA19-B/IRQ5/ AN113	PD3/D3[A3/D3]/MTIOC8D/ TOC2/POE8#/GTIOC0A/ RSPCKC-A/ET1_WOL/ QIO3-B/SDHI_D3-B/ MMC_D3-B/ LCD_DATA21-B/IRQ3/ AN111	PD3/D3[A3/D3]/MTIOC8D/ TOC2/POE8#/GTIOC0A/ RSPCKC-A/QIO3-B/ SDHI_D3-B/ MMC_D3-B/ LCD_DATA21-B/IRQ3/ AN111
124	PD4/D4[A4/D4]/MTIOC8B/ POE11#/SSLC0-A/ ET1_MDIO/PMGI1_MDIO/ QSSL-B/SDHI_CMD-B/ MMC_CMD-B/ LCD_DATA20-B/IRQ4/ AN112	PD2/D2[A2/D2]/MTIOC4D/ TIC2/GTIOC0B/MISOC-A/ CRX0/ET1_EXOUT/QIO2-B/ SDHI_D2-B/MMC_D2-B/ LCD_DATA22-B/IRQ2/ AN110	PD2/D2[A2/D2]/MTIOC4D/ TIC2/GTIOC0B/MISOC-A/ CRX0/QIO2-B/SDHI_D2-B/ MMC_D2-B/ LCD_DATA22-B/IRQ2/ AN110
125	P97/A23/ET1_ERXD3/ CAT1_ERXD3	PD1/D1[A1/D1]/MTIOC4B/ POE0#/GTIOC1A/MOSIC-A/ CTX0/LCD_DATA23-B/IRQ1/ AN109	PD1/D1[A1/D1]/MTIOC4B/ POE0#/GTIOC1A/MOSIC-A/ CTX0/LCD_DATA23-B/IRQ1/ AN109
126	PD3/D3[A3/D3]/MTIOC8D/ TOC2/POE8#/GTIOC0A/ RSPCKCA/ET1_WOL/ QIO3-B/SDHI_D3B/ MMC_D3-B/ LCD_DATA21-B/IRQ3/ AN111	PD0/D0[A0/D0]/POE4#/ GTIOC1B/LCD_EXTCLK-B/ IRQ0/AN108	PD0/D0[A0/D0]/POE4#/ GTIOC1B/LCD_EXTCLK-B/ IRQ0/AN108

144-Pin LFQFP	RX72M	RX72N	RX66N
127	P96/A22/ET1_ERXD2/ CAT1_ERXD2	P93/A19/POE0#/CTS7#/ RTS7#/SS7#/ET1_LINKSTA/ AN117	P93/A19/POE0#/CTS7#/ RTS7#/SS7#/AN117
128	PD2/D2[A2/D2]/MTIOC4D/ TIC2/GTIOC0B/MISOC-A/ CRX0/ET1_EXOUT/QIO2-B/ SDHI_D2B/MMC_D2-B/ LCD_DATA22-B/IRQ2/ AN110	P92/A18/POE4#/RXD7/ SMISO7/SSCL7/ RMII1_CRS_DV/AN116	P92/A18/POE4#/RXD7/ SMISO7/SSCL7/AN116
129	PD1/D1[A1/D1]/MTIOC4B/ POE0#/GTIOC1A/MOSIC-A/ CTX0/LCD_DATA23-B/IRQ1/ AN109	P91/A17/SCK7/AN115	P91/A17/SCK7/AN115
130	PD0/D0[A0/D0]/POE4#/ GTIOC1B/LCD_EXTCLK-B/ IRQ0/AN108	VSS	VSS
131	P93/A19/POE0#/CTS7#/ RTS7#/SS7#/ET1_LINKSTA/ CAT1_LINKSTA/AN117	P90/A16/TXD7/SMOSI7/ SSDA7/AN114	P90/A16/TXD7/SMOSI7/ SSDA7/AN114
132	P92/A18/POE4#/RXD7/ SMISO7/SSCL7/ET1_CRS/ RMII1_CRS_DV/ CAT1_RX_DV/AN116	VCC	VCC
133	P91/A17/SCK7/ET1_COL/ AN115	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
134	VSS	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
135	P90/A16/TXD7/SMOSI7/ SSDA7/ET1_RX_DV/ CAT1_RX_DV/AN114	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
136	VCC	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
137	P44/IRQ12_DS/AN004	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
138	P43/IRQ11_DS/AN003	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
139	P42/IRQ10_DS/AN002	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
140	P41/IRQ9_DS/AN001	VREFL0	VREFL0
141	VREFL0	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
142	P40/IRQ8_DS/AN000	VREFH0	VREFH0
143	VREFH0	AVCC0	AVCC0
144	AVCC0	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#

Note: 1. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.

3.6 100-Pin LFQFP Package

Table 3.6 is a comparative listing of the pin functions of 100-pin LFQFP package products.

Table 3.6 Comparative Listing of 100-Pin LFQFP Package Pin Functions

100-Pin LFQFP	RX72M	RX72N	RX66N
1	AVSS0	AVCC1	AVCC1
2	AVCC1	EMLE	EMLE
3	AVSS1	AVSS1	AVSS1
4	P00/TMRI0/TXD6/SMOSI6/ SSDA6/AUDIO_CLK/ CATLATCH1/IRQ8/AN118	PJ3/EDACK1/MTIOC3C/ CTS6#/RTS6#/SS6#/CTS0#/ RTS0#/SS0#/SSITXD0/ ET0_EXOUT	PJ3/EDACK1/MTIOC3C/ CTS6#/RTS6#/SS6#/CTS0#/ RTS0#/SS0#/SSITXD0/ ET0_EXOUT
5	EMLE	VCL	VCL
6	VCL	VBATT	VBATT
7	VBATT	MD/FINED	MD/FINED
8	MD/FINED	XCIN	XCIN
9	XCIN	XCOUT	XCOUT
10	XCOUT	RES#	RES#
11	RES#	XTAL/P37	XTAL/P37
12	XTAL/P37	VSS	VSS
13	VSS	EXTAL/P36	EXTAL/P36
14	EXTAL/P36	VCC	VCC
15	VCC	UPSEL/P35/NMI	UPSEL/P35/NMI
16	UPSEL/P35/NMI	TRST#/P34/MTIOC0A/ TMCI3/PO12/POE10#/SCK6/ SCK0/ET0_LINKSTA/IRQ4	TRST#/P34/MTIOC0A/ TMCI3/PO12/POE10#/SCK6/ SCK0/ET0_LINKSTA/IRQ4
17	TRST#/P34/MTIOC0A/ TMCI3/PO12/POE10#/SCK6/ SCK0/ET0_LINKSTA/ CAT0_LINKSTA/IRQ4	P33/EDREQ1/MTIOC0D/ TIOCD0/TMRI3/PO11/ POE4#/POE11#/RXD6/ SMISO6/SSCL6/RXD0/ SMISO0/SSCL0/CRX0/ IRQ3-DS	P33/EDREQ1/MTIOC0D/ TIOCD0/TMRI3/PO11/ POE4#/POE11#/RXD6/ SMISO6/SSCL6/RXD0/ SMISO0/SSCL0/CRX0/ IRQ3-DS
18	P33/MTIOC0D/TIOCD0/ TMRI3/PO11/POE4#/ POE11#/RXD6/SMISO6/ SSCL6/RXD0/SMISO0/ SSCL0/CRX0/IRQ3_DS	P32/MTIOC0C/TIOCC0/ TMO3/PO10/RTCIC2/ RTCOUT/POE0#/POE10#/ TXD6/SMOSI6/SSDA6/ TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/ IRQ2-DS	P32/MTIOC0C/TIOCC0/ TMO3/PO10/RTCIC2/ RTCOUT/POE0#/POE10#/ TXD6/SMOSI6/SSDA6/ TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/ IRQ2-DS
19	P32/MTIOC0C/TIOCC0/ TMO3/PO10/RTCIC2/ RTCOUT/POE0#/POE10#/ TXD6/SMOSI6/SSDA6/ TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/ IRQ2_DS	TMS/P31/MTIOC4D/TMCI2/ PO9/RTCIC1/CTS1#/RTS1#/ SS1#/SSLB0-A/IRQ1-DS	TMS/P31/MTIOC4D/TMCI2/ PO9/RTCIC1/CTS1#/RTS1#/ SS1#/SSLB0-A/IRQ1-DS
20	TMS/P31/MTIOC4D/TMCI2/ PO9/RTCIC1/CTS1#/RTS1#/ SS1#/SSLB0-A/ET1_MDC/ PMGI1_MDC/IRQ1_DS	TDI/P30/MTIOC4B/TMRI3/ PO8/RTCIC0/POE8#/RXD1/ SMISO1/SSCL1/MISOB-A/ IRQ0-DS	TDI/P30/MTIOC4B/TMRI3/ PO8/RTCIC0/POE8#/RXD1/ SMISO1/SSCL1/MISOB-A/ IRQ0-DS

100-Pin LFQFP	RX72M	RX72N	RX66N
21	TDI/P30/MTIOC4B/TMRI3/ PO8/RTCIC0/POE8#/RXD1/ SMISO1/SSCL1/MISOB-A/ ET1_MDIO/PMGI1_MDIO/ IRQ0_DS	TCK/P27/CS7#/MTIOC2B/ TMCI3/PO7/SCK1/ RSPCKB-A	TCK/P27/CS7#/MTIOC2B/ TMCI3/PO7/SCK1/ RSPCKB-A
22	TCK/P27/MTIOC2B/TMCI3/ PO7/SCK1/RSPCKB-A/ ET1_WOL/CATIRQ	TDO/P26/CS6#/MTIOC2A/ TMO1/PO6/TXD1/SMOSI1/ SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A	TDO/P26/CS6#/MTIOC2A/ TMO1/PO6/TXD1/SMOSI1/ SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A
23	TDO/P26/MTIOC2A/TMO1/ PO6/TXD1/SMOSI1/SSDA1/ CTS3#/RTS3#/SS3#/ MOSIB-A/ET1_EXOUT/ CATLINKACT1	CLKOUT/P25/CS5#/ EDACK1/MTIOC4C/ MTCLKB/TIOCA4/PO5/ RXD3/SMISO3/SSCL3/ SSIDATA1/ADTRG0#	CLKOUT/P25/CS5#/ EDACK1/MTIOC4C/ MTCLKB/TIOCA4/PO5/ RXD3/SMISO3/SSCL3/ SSIDATA1/ADTRG0#
24	CLKOUT/P25/MTIOC4C/ MTCLKB/TIOCA4/PO5/ RXD3/SMISO3/SSCL3/ SSIDATA1/ADTRG0#	P24/CS4#/EDREQ1/ MTIOC4A/MTCLKA/TIOCB4/ TMRI1/PO4/SCK3/ USB0_VBUSEN/SSIBCK1	P24/CS4#/EDREQ1/ MTIOC4A/MTCLKA/TIOCB4/ TMRI1/PO4/SCK3/ USB0_VBUSEN/SSIBCK1
25	P24/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/ USB0_VBUSEN/SSIBCK1	P23/EDACK0/MTIOC3D/ MTCLKD/TIOCD3/PO3/ GTIOC0A/TXD3/SMOSI3/ SSDA3/CTS0#/RTS0#/SS0#/ CTX1/SSIBCK0	P23/EDACK0/MTIOC3D/ MTCLKD/TIOCD3/PO3/ GTIOC0A/TXD3/SMOSI3/ SSDA3/CTS0#/RTS0#/SS0#/ CTX1/SSIBCK0
26	P23/MTIOC3D/MTCLKD/ TIOCD3/PO3/GTIOC0A/ TXD3/SMOSI3/SSDA3/ CTS0#/RTS0#/SS0#/CTX1/ SSIBCK0	P22/EDREQ0/MTIOC3B/ MTCLKC/TIOCC3/TMO0/ PO2/GTIOC1A/SCK0/ USB0_OVRCURB/ AUDIO_CLK	P22/EDREQ0/MTIOC3B/ MTCLKC/TIOCC3/TMO0/ PO2/GTIOC1A/SCK0/ USB0_OVRCURB/ AUDIO_CLK
27	P21/MTIOC1B/MTIOC4A/ TIOCA3/TMCI0/PO1/ GTIOC2A/RXD0/SMISO0/ SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/ IRQ9	P21/MTIOC1B/MTIOC4A/ TIOCA3/TMCI0/PO1/ GTIOC2A/RXD0/SMISO0/ SSCL0/USB0_EXICEN/ SSILRCK0/SCL1/IRQ9	P21/MTIOC1B/MTIOC4A/ TIOCA3/TMCI0/PO1/ GTIOC2A/RXD0/SMISO0/ SSCL0/USB0_EXICEN/ SSILRCK0/SCL1/IRQ9
28	P20/MTIOC1A/TIOCB3/ TMRI0/PO0/TXD0/SMOSI0/ SSDA0/SDA1/USB0_ID/ SSIRXD0/IRQ8	P20/MTIOC1A/TIOCB3/ TMRI0/PO0/TXD0/SMOSI0/ SSDA0/USB0_ID/SSIRXD0/ SDA1/IRQ8	P20/MTIOC1A/TIOCB3/ TMRI0/PO0/TXD0/SMOSI0/ SSDA0/USB0_ID/SSIRXD0/ SDA1/IRQ8
29	P17/MTIOC3A/MTIOC3B/ MTIOC4B/TIOCB0/TCLKD/ TMO1/PO15/POE8#/ GTIOC0B/SCK1/TXD3/ SMOSI3/SSDA3/SDA2_DS/ SSITXD0/EPLSOUT0/ CATSYNC0/IRQ7/ADTRG1#	P17/MTIOC3A/MTIOC3B/ MTIOC4B/TIOCB0/TCLKD/ TMO1/PO15/POE8#/ GTIOC0B/SCK1/TXD3/ SMOSI3/SSDA3/SDA2-DS/ SSITXD0/EPLSOUT0/IRQ7/ ADTRG1#	P17/MTIOC3A/MTIOC3B/ MTIOC4B/TIOCB0/TCLKD/ TMO1/PO15/POE8#/ GTIOC0B/SCK1/TXD3/ SMOSI3/SSDA3/SDA2-DS/ SSITXD0/IRQ7/ADTRG1#
30	P87/MTIOC4C/TIOCA2/ GTIOC1B/SMOSI10/ SSDA10/TXD10/EPLSOUT1/ CATSYNC1	P16/MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOUT/TXD1/ SMOSI1/SSDA1/RXD3/ SMISO3/SSCL3/SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB/IRQ6/ ADTRG0#	P16/MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOUT/TXD1/ SMOSI1/SSDA1/RXD3/ SMISO3/SSCL3/SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB/IRQ6/ ADTRG0#

100-Pin LFQFP	RX72M	RX72N	RX66N
31	P16/MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOUT/TXD1/ SMOSI1/SSDA1/RXD3/ SMISO3/SSCL3/SCL2_DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB/IRQ6/ ADTRG0#	P15/MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCI2/ PO13/GTETRGA/RXD1/ SMISO1/SSCL1/SCK3/ CRX1-DS/SSILRCK1/IRQ5	P15/MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCI2/ PO13/GTETRGA/RXD1/ SMISO1/SSCL1/SCK3/ CRX1-DS/SSILRCK1/IRQ5
32	P86/MTIOC4D/TIOCA0/ GTIOC2B/SMISO10/ SSCL10/RXD10/ CATLINKACT0	P14/MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15/GTETRGD/CTS1#/ RTS1#/ SS1#/CTX1/ USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15/GTETRGD/CTS1#/ RTS1#/ SS1#/CTX1/ USB0_OVRCURA/IRQ4
33	P15/MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCI2/ PO13/GTETRGA/RXD1/ SMISO1/SSCL1/SCK3/ CRX1_DS/SSILRCK1/ CATLEDRUN/IRQ5	P13/MTIOC0B/TIOCA5/ TMO3/PO13/GTADSM1/ TXD2/SMOSI2/SSDA2/ SDA0[FM+]/IRQ3/ADTRG1#	P13/MTIOC0B/TIOCA5/ TMO3/PO13/GTADSM1/ TXD2/SMOSI2/SSDA2/ SDA0[FM+]/IRQ3/ADTRG1#
34	P14/MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15/GTETRGD/CTS1#/ RTS1#/SS1#/CTX1/ USB0_OVRCURA/IRQ4	P12/TMCI1/GTADSM0/ RXD2/SMISO2/SSCL2/ SCL0[FM+]/ IRQ2	P12/TMCI1/GTADSM0/ RXD2/SMISO2/SSCL2/ SCL0[FM+]/ IRQ2
35	VCC_USB	VCC_USB	VCC_USB
36	USB0_DM	USB0_DM	USB0_DM
37	USB0_DP	USB0_DP	USB0_DP
38	VSS_USB	VSS_USB	VSS_USB
39	CLKOUT25M/P56/ MTIOC3C/TIOCA1/SCK7	P55/D0[A0/D0]/WAIT#/ EDREQ0/MTIOC4D/TMO3/ CRX1/ET0_EXOUT/IRQ10	P55/D0[A0/D0]/WAIT#/ EDREQ0/MTIOC4D/TMO3/ CRX1/ET0_EXOUT/IRQ10
40	P51/SCK2/SSLB2-A	P54/ALE/D1[A1/D1]/ EDACK0/MTIOC4B/TMCI1/ CTS2#/ RTS2#/SS2#/CTX1/ ET0_LINKSTA	P54/ALE/D1[A1/D1]/ EDACK0/MTIOC4B/TMCI1/ CTS2#/ RTS2#/SS2#/CTX1/ ET0_LINKSTA
41	P52/RXD2/SMISO2/SSCL2/ SSLB3-A/CATLEDSTER	P53*1/BCLK	P53*1/BCLK
42	P50/TXD2/SMOSI2/SSDA2/ SSLB1-A/CATLEDERR	P52/RD#/RXD2/SMISO2/ SSCL2/SSLB3-A	P52/RD#/RXD2/SMISO2/ SSCL2/SSLB3-A
43	VSS	P51/WR1#/BC1#/WAIT#/ SCK2/SSLB2-A	P51/WR1#/BC1#/WAIT#/ SCK2/SSLB2-A
44	VCC	P50/WR0#/WR#/TXD2/ SMOSI2/SSDA2/SSLB1-A	P50/WR0#/WR#/TXD2/ SMOSI2/SSDA2/SSLB1-A
45	UB/PC7/MTIOC3A/MTCLKB/ TMO2/PO31/CACREF/ GTIOC3A/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/ TXD10/ET0_COL/IRQ14	UB/PC7/A23/CS0#/ MTIOC3A/MTCLKB/TMO2/ PO31/TOC0/CACREF/ GTIOC3A/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/ ET0_COL/IRQ14	UB/PC7/A23/CS0#/ MTIOC3A/MTCLKB/TMO2/ PO31/TOC0/CACREF/ GTIOC3A/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/ ET0_COL/IRQ14

100-Pin LFQFP	RX72M	RX72N	RX66N
46	PC6/MTIOC3C/MTCLKA/ TMCI2/PO30/GTIOC3B/ RXD8/SMISO8/SSCL8/ SMISO10/SSCL10/RXD10/ ET0_ETXD3/CAT0_ETXD3/ CATLATCH1/IRQ13	PC6/D2[A2/D2]/A22/CS1#/ MTIOC3C/MTCLKA/TMCI2/ PO30/TIC0/GTIOC3B/RXD8/ SMISO8/SSCL8/SMISO10/ SSCL10/RXD10/MOSIA-A/ ET0_ETXD3/IRQ13	PC6/D2[A2/D2]/A22/CS1#/ MTIOC3C/MTCLKA/TMCI2/ PO30/TIC0/GTIOC3B/RXD8/ SMISO8/SSCL8/SMISO10/ SSCL10/RXD10/MOSIA-A/ ET0_ETXD3/IRQ13
47	PC5/MTIOC3B/MTCLKD/ TMRI2/PO29/GTIOC1A/ SCK8/RTS8#/SCK10/ ET0_ETXD2/CAT0_ETXD2	PC5/D3[A3/D3]/A21/CS2#/ WAIT#/MTIOC3B/MTCLKD/ TMRI2/PO29/GTIOC1A/ SCK8/RTS8#/SCK10/ RSPCKA-A/ET0_ETXD2	PC5/D3[A3/D3]/A21/CS2#/ WAIT#/MTIOC3B/MTCLKD/ TMRI2/PO29/GTIOC1A/ SCK8/RTS8#/SCK10/ RSPCKA-A/ET0_ETXD2
48	P82/MTIOC4A/PO28/ GTIOC2A/SMOSI10/ SSDA10/TXD10/ ET0_ETXD1/RMII0_TXD1/ CAT0_ETXD1/CATI2CDATA	PC4/A20/CS3#/MTIOC3D/ MTCLKC/TMCI1/PO25/ POE0#/GTETRGC/SCK5/ CTS8#/SS8#/SS10#/ CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK	PC4/A20/CS3#/MTIOC3D/ MTCLKC/TMCI1/PO25/ POE0#/GTETRGC/SCK5/ CTS8#/SS8#/SS10#/ CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK
49	P81/MTIOC3D/PO27/ GTIOC0B/SMISO10/ SSCL10/RXD10/ ET0_ETXD0/RMII0_TXD0/ CAT0_ETXD0/CATI2CCLK	PC3/A19/MTIOC4D/TCLKB/ PO24/GTIOC1B/TXD5/ SMOSI5/SSDA5/ ET0_TX_ER	PC3/A19/MTIOC4D/TCLKB/ PO24/GTIOC1B/TXD5/ SMOSI5/SSDA5/ ET0_TX_ER
50	P80/MTIOC3B/PO26/SCK10/ RTS10#/ET0_TX_EN/ RMII0_TXD_EN/ CAT0_TX_EN/CATLATCH0	PC2/A18/MTIOC4B/TCLKA/ PO21/GTIOC2B/RXD5/ SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV	PC2/A18/MTIOC4B/TCLKA/ PO21/GTIOC2B/RXD5/ SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV
51	PC4/MTIOC3D/MTCLKC/ TMCI1/PO25/POE0#/ GTETRGC/SCK5/SS8#/ CTS8#/SS10#/CTS10#/ RTS10#/ET0_TX_CLK/ CAT0_TX_CLK/CATSYNC0	PC1/A17/MTIOC3A/TCLKD/ PO18/SCK5/SSLA2-A/ ET0_ERXD2/IRQ12	PC1/A17/MTIOC3A/TCLKD/ PO18/SCK5/SSLA2-A/ ET0_ERXD2/IRQ12
52	PC2/MTIOC4B/TCLKA/ PO21/GTIOC2B/RXD5/ SMISO5/SSCL5/ ET0_RX_DV/CAT0_RX_DV	PC0/A16/MTIOC3C/TCLKC/ PO17/CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3/ IRQ14	PC0/A16/MTIOC3C/TCLKC/ PO17/CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3/ IRQ14
53	PB7/MTIOC3B/TIOCB5/ PO31/TXD9/SMOSI9/ SSDA9/SMOSI11/SSDA11/ TXD11/ET0_CRS/ RMII0_CRS_DV/ CAT0_RX_DV	PB7/A15/MTIOC3B/TIOCB5/ PO31/TXD9/SMOSI9/ SSDA9/SMOSI11/SSDA11/ TXD11/ET0_CRS/ RMII0_CRS_DV	PB7/A15/MTIOC3B/TIOCB5/ PO31/TXD9/SMOSI9/ SSDA9/SMOSI11/SSDA11/ TXD11/ET0_CRS/ RMII0_CRS_DV
54	PB6/MTIOC3D/TIOCA5/ PO30/RXD9/SMISO9/ SSCL9/SMISO11/SSCL11/ RXD11/ET0_ETXD1/ RMII0_TXD1/CAT0_ETXD1	PB6/A14/MTIOC3D/TIOCA5/ PO30/RXD9/SMISO9/ SSCL9/SMISO11/SSCL11/ RXD11/ET0_ETXD1/ RMII0_TXD1	PB6/A14/MTIOC3D/TIOCA5/ PO30/RXD9/SMISO9/ SSCL9/SMISO11/SSCL11/ RXD11/ET0_ETXD1/ RMII0_TXD1
55	PB5/MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE4#/SCK9/RTS9#/ SCK11/ET0_ETXD0/ RMII0_TXD0/CAT0_ETXD0	PB5/A13/MTIOC2A/ MTIOC1B/TIOCB4/TMRI1/ PO29/POE4#/SCK9/RTS9#/ SCK11/ET0_ETXD0/ RMII0_TXD0/LCD_CLK-B	PB5/A13/MTIOC2A/ MTIOC1B/TIOCB4/TMRI1/ PO29/POE4#/SCK9/RTS9#/ SCK11/ET0_ETXD0/ RMII0_TXD0/LCD_CLK-B

100-Pin LFQFP	RX72M	RX72N	RX66N
56	PB4/TIOCA4/PO28/SS9#/ CTS9#/SS11#/CTS11#/ RTS11#/ET0_TX_EN/ RMII0_TXD_EN/ CAT0_TX_EN	PB4/A12/TIOCA4/PO28/ CTS9#/SS9#/SS11#/ CTS11#/RTS11#/ ET0_TX_EN/ RMII0_TXD_EN/ LCD_TCON0-B	PB4/A12/TIOCA4/PO28/ CTS9#/SS9#/SS11#/ CTS11#/RTS11#/ ET0_TX_EN/ RMII0_TXD_EN/ LCD_TCON0-B
57	PB3/MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/TMO0/ PO27/POE11#/SCK4/SCK6/ ET0_RX_ER/RMII0_RX_ER/ CAT0_RX_ER	PB3/A11/MTIOC0A/ MTIOC4A/TIOCD3/TCLKD/ TMO0/PO27/POE11#/SCK6/ ET0_RX_ER/RMII0_RX_ER/ LCD_TCON1-B	PB3/A11/MTIOC0A/ MTIOC4A/TIOCD3/TCLKD/ TMO0/PO27/POE11#/SCK6/ ET0_RX_ER/RMII0_RX_ER/ LCD_TCON1-B
58	PB1/MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25/TXD4/ SMOSI4/SSDA4/TXD6/ SMOSI6/SSDA6/ ET0_ERXD0/RMII0_RXD0/ CAT0_ERXD0/IRQ4_DS	PB2/A10/TIOCC3/TCLKC/ PO26/CTS6#/RTS6#/SS6#/ ET0_RX_CLK/REF50CK0/ LCD_TCON2-B	PB2/A10/TIOCC3/TCLKC/ PO26/CTS6#/RTS6#/SS6#/ ET0_RX_CLK/REF50CK0/ LCD_TCON2-B
59	PB0/MTIC5W/TIOCA3/ PO24/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/ SSCL6/ET0_ERXD1/ RMII0_RXD1/CAT0_ERXD1/ IRQ12	PB1/A9/MTIOC0C/ MTIOC4C/TIOCB3/TMCI0/ PO25/TXD6/SMOSI6/ SSDA6/ET0_ERXD0/ RMII0_RXD0/ LCD_TCON3-B/IRQ4-DS	PB1/A9/MTIOC0C/ MTIOC4C/TIOCB3/TMCI0/ PO25/TXD6/SMOSI6/ SSDA6/ET0_ERXD0/ RMII0_RXD0/ LCD_TCON3-B/IRQ4-DS
60	PA6/MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE10#/GTETRGB/CTS5#/ RTS5#/SS5#/ET0_EXOUT/ CATRESTOUT	VCC	VCC
61	VCC	PB0/A8/MTIC5W/TIOCA3/ PO24/RXD6/SMISO6/ SSCL6/ET0_ERXD1/ RMII0_RXD1/ LCD_DATA0-B/IRQ12	PB0/A8/MTIC5W/TIOCA3/ PO24/RXD6/SMISO6/ SSCL6/ET0_ERXD1/ RMII0_RXD1/ LCD_DATA0-B/IRQ12
62	PA4/MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20/TXD5/ SMOSI5/SSDA5/ET0_MDC/ CAT0_MDC/CATIRQ/ PMGI0_MDC/IRQ5_DS	VSS	VSS
63	VSS	PA7/A7/TIOCB2/PO23/ MISOA-B/ET0_WOL/ LCD_DATA1-B	PA7/A7/TIOCB2/PO23/ MISOA-B/ET0_WOL/ LCD_DATA1-B
64	PA3/MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19/ RXD5/SMISO5/SSCL5/ ET0_MDIO/CAT0_MDIO/ PMGI0_MDIO/IRQ6_DS	PA6/A6/MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE10#/GTETRGB/CTS5#/ RTS5#/SS5#/MOSIA-B/ ET0_EXOUT/LCD_DATA2-B	PA6/A6/MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE10#/GTETRGB/CTS5#/ RTS5#/SS5#/MOSIA-B/ ET0_EXOUT/LCD_DATA2-B
65	PA2/MTIOC7A/PO18/ GTIOC1A/RXD5/SMISO5/ SSCL5/CATLINKACT1	PA5/A5/MTIOC6B/TIOCB1/ PO21/GTIOC0A/RSPCKA-B/ ET0_LINKSTA/ LCD_DATA3-B	PA5/A5/MTIOC6B/TIOCB1/ PO21/GTIOC0A/RSPCKA-B/ ET0_LINKSTA/ LCD_DATA3-B
66	PG6/ET1_ETXD3/ CAT1_ETXD3	PA4/A4/MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20/TXD5/ SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/PMGI0_MDC/ LCD_DATA4-B/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20/TXD5/ SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/PMGI0_MDC/ LCD_DATA4-B/IRQ5-DS

100-Pin LFQFP	RX72M	RX72N	RX66N
67	PA1/MTIOC0B/MTCLKC/ MTIOC7B/TIOCB0/PO17/ GTIOC2A/SCK5/ET0_WOL/ IRQ11	PA3/A3/MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19/ RXD5/SMISO5/SSCL5/ ET0_MDIO/PMGI0_MDIO/ LCD_DATA5-B/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19/ RXD5/SMISO5/SSCL5/ ET0_MDIO/PMGI0_MDIO/ LCD_DATA5-B/IRQ6-DS
68	PG5/ET1_ETXD2/ CAT1_ETXD2	PA2/A2/MTIOC7A/PO18/ GTIOC1A/RXD5/SMISO5/ SSCL5/SSLA3-B/ LCD_DATA6-B	PA2/A2/MTIOC7A/PO18/ GTIOC1A/RXD5/SMISO5/ SSCL5/SSLA3-B/ LCD_DATA6-B
69	PA0/MTIOC4A/MTIOC6D/ TIOCA0/PO16/CACREF/ GTIOC0B/ET0_TX_EN/ RMII0_TXD_EN/ CAT0_TX_EN/CATLEDRUN	PA1/A1/MTIOC0B/MTCLKC/ MTIOC7B/TIOCB0/PO17/ GTIOC2A/SCK5/SSLA2-B/ ET0_WOL/LCD_DATA7-B/ IRQ11	PA1/A1/MTIOC0B/MTCLKC/ MTIOC7B/TIOCB0/PO17/ GTIOC2A/SCK5/SSLA2-B/ ET0_WOL/LCD_DATA7-B/ IRQ11
70	P67/MTIOC7C/GTIOC1B/ CRX2/EPLSOUT1/ CATSYNC1/IRQ15	PA0/BC0#/A0/MTIOC4A/ MTIOC6D/TIOCA0/PO16/ CACREF/GTIOC0B/ SSLA1-B/ET0_TX_EN/ RMII0_TXD_EN/ LCD_DATA8-B	PA0/BC0#/A0/MTIOC4A/ MTIOC6D/TIOCA0/PO16/ CACREF/GTIOC0B/ SSLA1-B/ET0_TX_EN/ RMII0_TXD_EN/ LCD_DATA8-B
71	P66/MTIOC7D/GTIOC2B/ CTX2	PE7/D15[A15/D15]/ D7[A7/D7]/MTIOC6A/TOC1/ GTIOC3A/MISOB-B/ SDHI_WP/MMC_RES#-B/ LCD_DATA9-B/IRQ7/AN105	PE7/D15[A15/D15]/ D7[A7/D7]/MTIOC6A/TOC1/ GTIOC3A/MISOB-B/ SDHI_WP/MMC_RES#-B/ LCD_DATA9-B/IRQ7/AN105
72	PG2/ET1_TX_CLK/ CAT1_TX_CLK	PE6/D14[A14/D14]/ D6[A6/D6]/MTIOC6C/TIC1/ GTIOC3B/MOSIB-B/ SDHI_CD/MMC_CD-B/ LCD_DATA10-B/IRQ6/ AN104	PE6/D14[A14/D14]/ D6[A6/D6]/MTIOC6C/TIC1/ GTIOC3B/MOSIB-B/ SDHI_CD/MMC_CD-B/ LCD_DATA10-B/IRQ6/ AN104
73	PE5/MTIOC4C/MTIOC2B/ GTIOC0A/ET0_RX_CLK/ REF50CK0/CAT0_RX_CLK/ IRQ5/AN103	PE5/D13[A13/D13]/ D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/ RSPCKB-B/ET0_RX_CLK/ REF50CK0/LCD_DATA11-B/ IRQ5/AN103	PE5/D13[A13/D13]/ D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/ RSPCKB-B/ET0_RX_CLK/ REF50CK0/LCD_DATA11-B/ IRQ5/AN103
74	PE4/MTIOC4D/MTIOC1A/ PO28/GTIOC1A/ ET0_ERXD2/CAT0_ERXD2/ AN102	PE4/D12[A12/D12]/ D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/ SSLB0-B/ET0_ERXD2/ LCD_DATA12-B/AN102	PE4/D12[A12/D12]/ D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/ SSLB0-B/ET0_ERXD2/ LCD_DATA12-B/AN102
75	PE3/MTIOC4B/PO26/ POE8#/GTIOC2A/ ET0_ERXD3/CAT0_ERXD3/ AN101	PE3/D11[A11/D11]/ D3[A3/D3]/MTIOC4B/PO26/ TOC3/POE8#/GTIOC2A/ CTS12#/RTS12#/SS12#/ ET0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101	PE3/D11[A11/D11]/ D3[A3/D3]/MTIOC4B/PO26/ TOC3/POE8#/GTIOC2A/ CTS12#/RTS12#/SS12#/ ET0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101
76	P64/ET1_ETXD0/ RMII1_TXD0/CAT1_ETXD0	PE2/D10[A10/D10]/ D2[A2/D2]/MTIOC4A/PO23/ TIC3/GTIOC0B/RXD12/ SMISO12/SSCL12/RXDX12/ SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/ AN100	PE2/D10[A10/D10]/ D2[A2/D2]/MTIOC4A/PO23/ TIC3/GTIOC0B/RXD12/ SMISO12/SSCL12/RXDX12/ SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/ AN100

100-Pin LFQFP	RX72M	RX72N	RX66N
77	P63/ET1_ETXD1/ RMII1_TXD1/CAT1_ETXD1	PE1/D9[A9/D9]/D1[A1/D1]/ MTIOC4C/MTIOC3B/PO18/ GTIOC1B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/ SSLB2-B/MMC_D5-B/ LCD_DATA15-B/ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/ MTIOC4C/MTIOC3B/PO18/ GTIOC1B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/ SSLB2-B/MMC_D5-B/ LCD_DATA15-B/ANEX1
78	P62/ET1_ERXD0/ RMII1_RXD0/CAT1_ERXD0	PE0/D8[A8/D8]/D0[A0/D0]/ MTIOC3D/GTIOC2B/SCK12/ SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/ MTIOC3D/GTIOC2B/SCK12/ SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0
79	P61/ET1_ERXD1/ RMII1_RXD1/CAT1_ERXD1	PD7/D7[A7/D7]/MTIC5U/ POE0#/SSLC3-A/QMI-B/ QIO1-B/SDHI_D1-B/ MMC_D1-B/LCD_DATA17-B/ IRQ7/AN107	PD7/D7[A7/D7]/MTIC5U/ POE0#/SSLC3-A/QMI-B/ QIO1-B/SDHI_D1-B/ MMC_D1-B/LCD_DATA17-B/ IRQ7/AN107
80	VSS	PD6/D6[A6/D6]/MTIC5V/ MTIOC8A/POE4#/SSLC2-A/ QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/ IRQ6/AN106	PD6/D6[A6/D6]/MTIC5V/ MTIOC8A/POE4#/SSLC2-A/ QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/ IRQ6/AN106
81	P60/ET1_TX_EN/ RMII1_TXD_EN/ CAT1_TX_EN	PD5/D5[A5/D5]/MTIC5W/ MTIOC8C/MTCLKA/ POE10#/SSLC1-A/ QSPCLK-B/SDHI_CLK-B/ MMC_CLK-B/ LCD_DATA19-B/IRQ5/ AN113	PD5/D5[A5/D5]/MTIC5W/ MTIOC8C/MTCLKA/ POE10#/SSLC1-A/ QSPCLK-B/SDHI_CLK-B/ MMC_CLK-B/ LCD_DATA19-B/IRQ5/ AN113
82	VCC	PD4/D4[A4/D4]/MTIOC8B/ POE11#/SSLC0-A/QSSL-B/ SDHI_CMD-B/MMC_CMD-B/ LCD_DATA20-B/IRQ4/ AN112	PD4/D4[A4/D4]/MTIOC8B/ POE11#/SSLC0-A/QSSL-B/ SDHI_CMD-B/MMC_CMD-B/ LCD_DATA20-B/IRQ4/ AN112
83	PD7/MTIC5U/POE0#/ ET1_RX_ER/RMII1_RX_ER/ CAT1_RX_ER/IRQ7/AN107	PD3/D3[A3/D3]/MTIOC8D/ TOC2/POE8#/GTIOC0A/ RSPCKC-A/QIO3-B/ SDHI_D3-B/MMC_D3-B/ LCD_DATA21-B/IRQ3/ AN111	PD3/D3[A3/D3]/MTIOC8D/ TOC2/POE8#/GTIOC0A/ RSPCKC-A/QIO3-B/ SDHI_D3-B/MMC_D3-B/ LCD_DATA21-B/IRQ3/ AN111
84	PD6/MTIC5V/MTIOC8A/ POE4#/ET1_RX_CLK/ REF50CK1/CAT1_RX_CLK/ IRQ6/AN106	PD2/D2[A2/D2]/MTIOC4D/ TIC2/GTIOC0B/MISOC-A/ CRX0/QIO2-B/SDHI_D2-B/ MMC_D2-B/LCD_DATA22-B/ IRQ2/AN110	PD2/D2[A2/D2]/MTIOC4D/ TIC2/GTIOC0B/MISOC-A/ CRX0/QIO2-B/SDHI_D2-B/ MMC_D2-B/LCD_DATA22-B/ IRQ2/AN110
85	P97/ET1_ERXD3/ CAT1_ERXD3	PD1/D1[A1/D1]/MTIOC4B/ POE0#/GTIOC1A/MOSIC-A/ CTX0/LCD_DATA23-B/IRQ1/ AN109	PD1/D1[A1/D1]/MTIOC4B/ POE0#/GTIOC1A/MOSIC-A/ CTX0/LCD_DATA23-B/IRQ1/ AN109
86	P96/ET1_ERXD2/ CAT1_ERXD2	PD0/D0[A0/D0]/POE4#/ TIOC1B/LCD_EXTCLK-B/ IRQ0/AN108	PD0/D0[A0/D0]/POE4#/ TIOC1B/LCD_EXTCLK-B/ IRQ0/AN108
87	PD2/MTIOC4D/GTIOC0B/ CRX0/ET1_EXOUT/IRQ2/ AN110	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007

100-Pin LFQFP	RX72M	RX72N	RX66N
88	PD1/MTIOC4B/POE0#/ GTIOC1A/CTX0/IRQ1/ AN109	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
89	P93/POE0#/CTS7#/RTS7#/ SS7#/ET1_LINKSTA/ CAT1_LINKSTA/AN117	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
90	P92/POE4#/RXD7/SMISO7/ SSCL7/ET1_CRS/ RMII1_CRS_DV/ CAT1_RX_DV/AN116	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
91	P91/SCK7/ET1_COL/AN115	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
92	VSS	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
93	P90/TXD7/SMOSI7/SSDA7/ ET1_RX_DV/CAT1_RX_DV/ AN114	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
94	VCC	VREFL0	VREFL0
95	P42/IRQ10_DS/AN002	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
96	P41/IRQ9_DS/AN001	VREFH0	VREFH0
97	VREFL0	AVCC0	AVCC0
98	P40/IRQ8_DS/AN000	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
99	VREFH0	AVSS0	AVSS0
100	AVCC0	P05/SSILRCK1/IRQ13/DA1	P05/SSILRCK1/IRQ13/DA1

Note: 1. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.

4. Important Information when Migrating Between MCUs

There are important points that must be borne in mind regarding differences between the RX72M/RX72N Group and RX66N Group.

Important points regarding software are described in 4.1, Important Information Regarding Function Settings.

4.1 Important Information Regarding Function Settings

Software that runs on the RX72M/RX72N Group is largely compatible with the RX66N Group. Nevertheless, appropriate caution must be exercised because there are differences in the maximum operating frequencies and some functions, as well as in aspects such as operation timing and electrical characteristics.

Important points regarding differences in function settings on the RX72M/RX72N Group and RX66N Group that must be borne in mind when writing software are listed below.

For differences between modules and functions, refer to section 2, Comparative Overview of Specifications. For details, refer to the User's Manual: Hardware of each group, listed in section 5, Reference Documents.

4.1.1 Port Direction Register (PDR) Initialization

The PDR register initialization procedure differs even on products with the same pin count.

5. Reference Documents

User's Manual: Hardware

RX72M Group User's Manual: Hardware, Rev. 1.11 (R01UH0804EJ0111)
(The latest version can be downloaded from the Renesas Electronics website.)

RX72N Group User's Manual: Hardware, Rev. 1.11 (R01UH0824EJ0111)
(The latest version can be downloaded from the Renesas Electronics website.)

RX66N Group User's Manual: Hardware, Rev. 1.11 (R01UH0825EJ0111)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This application note reflects the content of the following technical updates:

- TN-RX*-A0227A/E
- TN-RX*-A0233A/E
- TN-RX*-A0235B/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Dec. 25, 2019	—	First edition issued
1.10	Mar. 4, 2021	3	1 Table 1.1 Comparison of Built-In Functions of RX66N Group and RX72M/RX72N Group revised
		25	2.7 Table 2.11 Comparative Overview of I/O Ports of 145- and 144-Pin Products and Table 2.12 Comparative Overview of I/O Ports of 100-Pin Products added
		52	2.8 Table 2.14 Comparison of Multiplexed Pin Assignments (145-Pin/144-Pin/100-Pin) revised
		74	2.8 Table 2.16 Comparison of P1n Pin Function Control Register (P1nPFS) revised
		75	2.8 Table 2.17 Comparison of P2n Pin Function Control Register (P2nPFS) revised
		81	2.8 Table 2.22 Comparison of P8n Pin Function Control Register (P8nPFS) revised
		89	2.8 Table 2.26 Comparison of PCn Pin Function Control Register (PCnPFS) revised
		92	2.8 Table 2.27 Comparison of PDn Pin Function Control Register (PDnPFS) revised
		94	2.8 Table 2.28 Comparison of PEn Pin Function Control Register (PEnPFS) revised
		115	2.14 Table 2.45 Packages revised
		162	3.5 Table 3.5 Comparative Listing of 144-Pin LFQFP Package Pin Functions revised
		174	3.6 Table 3.6 Comparative Listing of 100-Pin LFQFP Package Pin Functions revised
		182	4.1.1 Port Direction Register (PDR) Initialization added
		183	5. Reference Documents revised
		184	Related Technical Updates revised

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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