RX66N Group, RX64M Group

Differences Between the RX66N Group and the RX64M Group

Summary

This application note is a reference document that lists differences in peripheral modules, I/O registers, and pin functions between the RX66N Group and the RX64M Group. This document also provides important information that needs to be taken into account when replacing the MCU.

Unless otherwise indicated the MCU specifications of RX66N Group products with 224 pins and RX64M Group products with 177 pins are described. Refer to the User's Manual: Hardware of each MCU for details of differences in electrical characteristics, usage notes, and setting procedures.

Target Devices

RX66N Group

RX64M Group

Contents

1. Comparison of Built-In Functions of RX66N Group and RX64M Group

Table 1.1 is a comparative listing of the built-in functions of RX66N Group and RX64M Group. For details of each function, refer to section 2, Comparative Overview of Specifications, as well as the documents listed in section 5, Reference Documents.

Table 1.1 Comparison of Built-In Functions of RX66N Group and RX64M Group

Function	RX64M	RX66N
CPU	●	
Operating modes	●/■	
Address space	▲	
Resets	○	
Option-setting memory (OFSM)	●/■	
Voltage detection circuit (LVDA)	○	
Clock generation circuit	●/▲/■	
Clock frequency accuracy measurement circuit (CAC)	●	
Low power consumption	●/▲/■	
Battery backup function	○	
Register write protection function	●	
Exception handling	●	
Interrupt controller (ICUA): RX64M, (ICUD): RX66N	●/■	
Buses	●/■	
Memory-protection unit (MPU)	○	
DMA controller (DMACAa)	○	
EXDMA controller (EXDMACa)	○	
Data transfer controller (DTCa): RX64M, (DTCb): RX66N	●	
Event link controller (ELC)	●	
I/O ports	●	
Multi-function pin controller (MPC)	●/▲	
Multi-function timer pulse unit 3 (MTU3a)	○	
Port output enable 3 (POE3a)	■	
General PWM timer (GPTA): RX64M, (GPTW): RX66N	●	
GPTW port output enable (POEG)	×	○
16-bit timer pulse unit (TPUa)	○	
Programmable pulse generator (PPG)	○	
8-bit timer (TMR)	○	
Compare match timer (CMT)	○	
Compare match timer W (CMTW)	○	
Realtime clock (RTCd)	○	
Watchdog timer (WDTA)	○	
Independent watchdog timer (IWDTa)	○	
Ethernet controller (ETHERC)	■	
PTP module for the Ethernet controller (EPTPC)	○	×
DMA controller for the Ethernet controller (EDMACa)	■	
PHY management interface (PMGI)	×	○
USB 2.0 FS Host/Function module (USBb)	▲	
USB 2.0 Full-Speed Host/Function module (USBA)	○	×
Serial communications interface (SCIg, SCIh): RX64M, (SCIj, SCIi, SCIh): RX66N	●	
FIFO-embedded serial communications interface (SCIFA)	○	×
I²C bus interface (RIICa)	●	

Function	RX64M	RX66N
CAN module (CAN)	○	
Serial peripheral interface (RSPIa): RX64M, (RSPIc): RX66N	●/▲	
Quad serial peripheral interface (QSPI)	○	
CRC calculator (CRC): RX64M, (CRCA): RX66N	●	
Serial sound interface (SSI): RX64M, enhanced serial sound interface (SSIE): RX66N	●/▲	
Sample rate converter (SRC)	○	×
SD host interface (SDHI)	●	
MultiMediaCard interface (MMCIF)	○	
Parallel data capture unit (PDC)	○	
Graphic LCD controller (GLCDC)	×	○
2D drawing engine (DRW2D)	×	○
Boundary scan	▲	
AES	○	×
DES	○	×
SHA	○	×
RNG	○	×
Trusted Secure IP (TSIP)	×	○
12-bit A/D converter (S12ADC): RX64M, (S12ADFa): RX66N	●/▲	
12-bit D/A converter (R12DA): RX64M, (R12DAa): RX66N	●	
Temperature sensor (TEMPS)	○	
Data operation circuit (DOC)	○	
RAM	●	
Standby RAM	▲	
Flash memory (FLASH)	●/▲/■	
Packages	●/▲/■	

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Differences in register specifications are not listed.

2.1 CPU

Table 2.1 is a comparative overview of CPU, and Table 2.2 is a comparison of CPU registers.

Table 2.1 Comparative Overview of CPU

Item	RX64M	RX66N
CPU	• Maximum operating frequency: 120 MHz • 32-bit RX CPU (RXv2) • Minimum instruction execution time: One instruction per state (system clock cycle) • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit register • Basic instructions: 75 • Floating-point instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits	• Maximum operating frequency: 120 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per state (system clock cycle) • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • Basic instructions: 77 • Single-precision floating point instructions: 11 • DSP instructions: 23 • Instructions for register bank save function: 2 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits
FPU	• Single-precision floating point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard

Item	RX64M	RX66N
Double-precision floating point coprocessor	—	• Double-precision floating-point data registers: 64-bit × 16 • Double-precision floating-point control registers: 32-bit × 4 • Double-precision floating-point processing instructions: 21 • Function for notifying the interrupt controller of double-precision floating-point exceptions
Register bank save function	—	• Fast collective saving and restoration of the values of CPU registers • 16 save register banks

Table 2.2 Comparison of CPU Registers

Register	Bit	RX64M	RX66N
DR0 to DR15	—	—	Double-precision floating-point data registers
DPSW	—	—	Double-precision floating-point status word
DCMR	—	—	Double-precision floating-point comparison result register
DECNT	—	—	Double-precision floating-point exception handling control register
DEPC	—	—	Double-precision floating-point exception program counter

2.2 Operating Modes

Table 2.3 is a comparative overview of operating modes, and Table 2.4 is a comparison of operating mode registers.

Table 2.3 Comparative Overview of Operating Modes

Item	RX64M	RX66N
Operating modes selected by mode-setting pins	Single-chip mode	Single-chip mode
	Boot mode (SCI interface)	Boot mode (SCI interface)
	Boot mode (USB interface)	Boot mode (USB interface)
	User boot mode	—
	—	Boot mode (FINE interface)
Operating modes selected by register settings	Single-chip mode	Single-chip mode
	User boot mode	—
	On-chip ROM disabled extended mode	On-chip ROM disabled extended mode
	On-chip ROM enabled extended mode	On-chip ROM enabled extended mode

Table 2.4 Comparison of Operating Mode Registers

Register	Bit	RX64M	RX66N
MDSR	—	Mode status register	—

2.3 Address Space

Table 2.5 is a comparative memory map of single-chip mode, Table 2.6 a comparative memory map of on-chip ROM enabled extended mode, and Table 2.7 a comparative memory map of on-chip ROM disabled extended mode.

Table 2.5 Comparative Memory Map of Single-Chip Mode

Start Address	RX64M	RX66N
0000 0000h	On-chip RAM	On-chip RAM
0008 0000h	Peripheral I/O registers	Peripheral I/O registers
000A 4000h	Standby RAM	Standby RAM
000A 6000h	Peripheral I/O registers	Peripheral I/O registers
0010 0000h	On-chip ROM (data flash memory)	On-chip ROM (data flash memory)
0010 8000h		Reserved area
0011 0000h	Reserved area	
0012 0040h	On-chip ROM (option-setting memory)	
0012 0070h	Reserved area	
007E 0000h	On-chip ROM (write only)	FACI command issuing area
007F 0000h	Reserved area	
007F 0004h		Reserved area
007F 8000h	FCU-RAM area	
007F 9000h	Reserved area	
007F C000h		Peripheral I/O registers
007F E000h	Peripheral I/O registers	
0080 0000h	Reserved area	On-chip expansion RAM
0088 0000h		Reserved area
00FF 8000h	ECC-RAM area	ECCRAM
0100 0000h	Reserved area	Reserved area
FE7F 5D00h		On-chip ROM (option-setting memory)
FE7F 5D80h		Reserved area
FE7F 7D70h		On-chip ROM (read only)
FE7F 7DA0h		Reserved area
FEFF F000h	On-chip ROM (FCU firmware) (read only)	
FF00 0000h	Reserved area	
FF7F 8000h	On-chip ROM (user boot) (read only)	
FF80 0000h	Reserved area	
FFC0 0000h	On-chip ROM (program ROM) (read only)	On-chip ROM (code flash memory)

Table 2.6 Comparative Memory Map of On-Chip ROM Enabled Extended Mode

Start Address	RX64M	RX66N
0000 0000h	On-chip RAM	On-chip RAM
0008 0000h	Peripheral I/O registers	Peripheral I/O registers
000A 4000h	Standby RAM	Standby RAM
000A 6000h	Peripheral I/O registers	Peripheral I/O registers
0010 0000h	On-chip ROM (data flash memory)	On-chip ROM (data flash memory)
0010 8000h		Reserved area
0011 0000h	Reserved area	
0012 0040h	On-chip ROM (option-setting memory)	
0012 0070h	Reserved area	
007E 0000h	On-chip ROM (write only)	FACI command issuing area
007F 0000h	Reserved area	
007F 0004h		Reserved area
007F 8000h	FCU-RAM area	
007F 9000h	Reserved area	
007F C000h		Peripheral I/O registers
007F E000h	Peripheral I/O registers	
0080 0000h	Reserved area	On-chip expansion RAM
0088 0000h		Reserved area
00FF 8000h	ECC-RAM area	ECCRAM
0100 0000h	CS7 (16 MB)	CS7 (16 MB)
0200 0000h	CS6 (16 MB)	CS6 (16 MB)
0300 0000h	CS5 (16 MB)	CS5 (16 MB)
0400 0000h	CS4 (16 MB)	CS4 (16 MB)
0500 0000h	CS3 (16 MB)	CS3 (16 MB)
0600 0000h	CS2 (16 MB)	CS2 (16 MB)
0700 0000h	CS1 (16 MB)	CS1 (16 MB)
0800 0000h	SDCS (128 MB)	SDCS (128 MB)
1000 0000h	Reserved area	Reserved area
FE7F 5D00h		On-chip ROM (option-setting memory)
FE7F 5D80h		Reserved area
FE7F 7D70h		On-chip ROM (read only)
FE7F 7DA0h		Reserved area
FEFF F000h	On-chip ROM (FCU firmware) (read only)	
FF00 0000h	Reserved area	
FF7F 8000h	On-chip ROM (user boot) (read only)	
FF80 0000h	Reserved area	
FFC0 0000h	On-chip ROM (program ROM) (read only)	On-chip ROM (code flash memory)

Note: The areas enclosed in thick borders are in external address spaces (CS and SDRAM areas).

Table 2.7 Comparative Memory Map of On-Chip ROM Disabled Extended Mode

Start Address	RX64M	RX66N
0000 0000h	On-chip RAM	On-chip RAM
0008 0000h	Peripheral I/O registers	Peripheral I/O registers
000A 4000h	Standby RAM	Standby RAM
000A 6000h	Peripheral I/O registers	Peripheral I/O registers
0010 0000h	Reserved area	Reserved area
0080 0000h		On-chip expansion RAM
0088 0000h		Reserved area
00FF 8000h	ECC-RAM area	ECCRAM
0100 0000h	CS7 (16 MB)	CS7 (16 MB)
0200 0000h	CS6 (16 MB)	CS6 (16 MB)
0300 0000h	CS5 (16 MB)	CS5 (16 MB)
0400 0000h	CS4 (16 MB)	CS4 (16 MB)
0500 0000h	CS3 (16 MB)	CS3 (16 MB)
0600 0000h	CS2 (16 MB)	CS2 (16 MB)
0700 0000h	CS1 (16 MB)	CS1 (16 MB)
0800 0000h	SDCS (128 MB)	SDCS (128 MB)
1000 0000h	Reserved area	Reserved area
FF00 0000h	CS0 (16 MB)	CS0 (16 MB)

Note: The areas enclosed in thick borders are in external address spaces (CS and SDRAM areas).

2.4 Option-Setting Memory

Table 2.8 is a comparison of option-setting memory registers.

Table 2.8 Comparison of Option-Setting Memory Registers

Register	Bit	RX64M (OFSM)	RX66N (OFSM)
SPCC	IDE	ID code protection enable bit	—
	SEPR	Block erasure command protect bit	—
	WRPR	Programming command protect bit	—
	RDPR	Read command protect bit	—
OSIS	—	OCD/serial programmer ID setting register This register is used to store the ID code for ID code protection of the OCD/serial programmer. Refer to RX64M Group User's Manual: Hardware for details.	OCD/serial programmer ID setting register This register is used to store the control code or ID code for ID code protection of the OCD/serial programmer. Refer to RX66N Group User's Manual: Hardware for details.
MDE	BANKMD[2:0]	—	Bank mode select bits
TMEF	TMEFDB[2:0]	—	Dual-bank TM enable bits
BANKSEL	—	—	Bank select register
FAW	—	—	Flash access window setting register
ROMCODE	—	—	ROM code protection register

2.5 Clock Generation Circuit

Table 2.9 is a comparative overview of the clock generation circuits, and Table 2.10 is a comparison of clock generation circuit registers.

Table 2.9 Comparative Overview of Clock Generation Circuits

Item	RX64M	RX66N
Use	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the ETHERC, EDMAC, EPTPC, USBA, RSPI, SCIF, MTU3, GPT, and AES. • Generates the peripheral module clock (PCLKB) to be supplied to the peripheral modules. • Generates the peripheral module clocks (for analog conversion) (PCLKC: unit 0; PCLKD: unit 1) to be supplied to the S12ADC. • Generates the flash-IF clock (FCLK) to be supplied to the flash interface. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the SDRAM clock (SDCLK) to be supplied to the SDRAM. • Generates the USB clock (UCLK) to be supplied to the USBb and the PHY in the USBA. • Generates the USBA clock (USBMCLK) to be supplied to the PHY in the USBA. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the RTC sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the RTC main clock (RTCMCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the JTAG clock (JTAGTCK) to be supplied to the JTAG.	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the ETHERC, EDMAC, RSPI, SCIi, MTU, GLCDC, DRW2D, PMGI, and GPTW. • Generates the peripheral module clock (PCLKB) to be supplied to the peripheral modules. • Generates the peripheral module clocks (for analog conversion) (PCLKC: unit 0; PCLKD: unit 1) to be supplied to the S12AD. • Generates the flash-IF clock (FCLK) to be supplied to the flash interface. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the SDRAM clock (SDCLK) to be supplied to the SDRAM. • Generates the USB clock (UCLK) to be supplied to the USB. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the RTC sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the RTC main clock (RTCMCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the JTAG clock (JTAGTCK) to be supplied to the JTAG.

Item	RX64M	RX66N
Operating frequency	• ICLK: 120 MHz (max.) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKC: 60 MHz (max.) • PCLKD: 60 MHz (max.) • FCLK: — 4 MHz to 60 MHz (for programming and erasing the code flash memory and data flash memory) — 60 MHz (max.) (for reading from the data flash memory) • BCLK: 120 MHz (max.) • BCLK pin output: 60 MHz (max.) • SDCLK pin output: 60 MHz (max.) • UCLK: 48 MHz (max.) • USBMCLK: 20 MHz, 24 MHz • CACCLK: Same as the clocks from the respective oscillators. • CANMCLK: 24 MHz (max.) • RTCSCLK: 32.768 kHz • RTCMCLK: 8 MHz to 16 MHz • IWDTCLK: 120 kHz • JTAGTCK: 10 MHz (max.)	• ICLK: 120 MHz (max.) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKC: 60 MHz (max.) • PCLKD: 60 MHz • FCLK: — 4 MHz to 60 MHz (for programming and erasing the code flash memory and data flash memory) — 60 MHz (max.) (for reading from the data flash memory) • BCLK: 120 MHz (max.) • BCLK pin output: 80 MHz (max.) • SDCLK pin output: 80 MHz (max.) • UCLK: 48 MHz (max.) • CLKOUT25M pin output: 25 MHz (max.) • CLKOUT pin output: 40 MHz (max.) • CACCLK: Same as the clocks from the respective oscillators. • CANMCLK: 24 MHz (max.) • RTCSCLK: 32.768 kHz • RTCMCLK: 8 MHz to 16 MHz • IWDTCLK: 120 kHz • JTAGTCK: 10 MHz (max.)
Main clock oscillator	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop is detected on the main clock, the system clock source is switched to LOCO, and the MTU3 and GPT pins can be forcedly driven high-impedance.	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 30 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop is detected on the main clock, the system clock source is switched to LOCO, and the MTU and GPTW pins can be forcedly driven high-impedance.
Sub-clock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pins: XCIN, XCOUT	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pins: XCIN, XCOUT

Item	RX64M	RX66N
PLL frequency synthesizer	• Input clock sources: Main clock, HOCO • Input pulse frequency division ratio: Selectable from ×1/1, ×1/2, and ×1/3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication factor: Selectable from 10 to 30 • Output clock frequency of PLL frequency synthesizer: 120 MHz to 240 MHz	• Input clock sources: Main clock, HOCO • Input pulse frequency division ratio: Selectable from ×1/1, ×1/2, and ×1/3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication factor: Selectable from 10 to 30 • Output clock frequency of PLL frequency synthesizer: 120 MHz to 240 MHz
PLL frequency synthesizer for specific purposes (PPLL)	—	• Input clock sources: Main clock, HOCO • Input pulse frequency division ratio: Selectable from ×1/1, ×1/2, and ×1/3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication factor: Selectable from 10 to 30 • Output clock frequency of PLL frequency synthesizer: 120 MHz to 240 MHz
High-speed on-chip oscillator (HOCO)	• Oscillation frequency: Selectable among 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control	• Oscillation frequency: Selectable among 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 240 kHz	Oscillation frequency: 240 kHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 120 kHz	Oscillation frequency: 120 kHz
JTAG external clock input (TCK)	Input clock frequency: 10 MHz (max.)	Input clock frequency: 10 MHz (max.)
Control of output on BCLK pin	• Selectable between BCLK clock output and high output • Selectable between BCLK and BCLK ×1/2	• Selectable between BCLK clock output and high output • Selectable between BCLK and BCLK ×1/2
Control of output on SDCLK pin	Selectable between SDCLK clock output and high output SDCLK	Selectable between SDCLK clock output and high output SDCLK
Event link function (output)	Detection of stopping of the main clock oscillator	Detection of stopping of the main clock oscillator
Event link function (input)	Switching of the clock source to the low-speed on-chip oscillator	Switching of the clock source to the low-speed on-chip oscillator

Table 2.10 Comparison of Clock Generation Circuit Registers

Register	Bit	RX64M	RX66N
SCKCR	BCK[3:0]	External bus clock (BCLK) select bits b19 b16 0 0 0 0: 1/1 0 0 0 1: 1/2 0 0 1 0: 1/4 0 0 1 1: 1/8 0 1 0 0: 1/16 0 1 0 1: 1/32 0 1 1 0: 1/64 Settings other than the above are prohibited.	External bus clock (BCLK) select bits b19 b16 0 0 0 0: 1/1 0 0 0 1: 1/2 0 0 1 0: 1/4 0 0 1 1: 1/8 0 1 0 0: 1/16 0 1 0 1: 1/32 0 1 1 0: 1/64 1 0 0 1: 1/3 Settings other than the above are prohibited.
OSCOVFSR	PPLOVF	—	PPLL clock oscillation stabilization flag
CKOCR	—	—	CLKOUT output control register
PACKCR	—	—	Specific-use clock control register
PPLLCR	—	—	PPLL control register
PPLLCR2	—	—	PPLL control register 2
PPLLCR3	—	—	PPLL control register 3

2.6 Clock Frequency Accuracy Measurement Circuit

Table 2.11 is a comparative overview of clock frequency accuracy measurement circuits, and Table 2.12 is a comparison of clock frequency accuracy measurement circuit registers.

Table 2.11 Comparative Overview of Clock Frequency Accuracy Measurement Circuits

Item	RX64M (CAC)	RX66N (CAC)
Measurement target clocks	• Main clock • Sub-clock • HOCO clock • LOCO clock • IWDTCLK clock • Peripheral module clock B (PCLKB)	• Main clock • Sub-clock • HOCO clock • LOCO clock • IWDT-dedicated clock (IWDTCLK) • Peripheral module clock B (PCLKB) • USB clock (UCLK) • External clock for the Ethernet-PHY (CLKOUT25M)
Measurement reference clocks	• External clock input on CACREF pin • Main clock • Sub-clock • HOCO clock • LOCO clock • IWDTCLK clock • Peripheral module clock B (PCLKB)	• External clock input on CACREF pin • Main clock • Sub-clock • HOCO clock • LOCO clock • IWDT-dedicated clock (IWDTCLK) • Peripheral module clock B (PCLKB) • USB clock (UCLK) • External clock for the Ethernet-PHY (CLKOUT25M)
Selectable function	Digital filter function	Digital filter function
Interrupt sources	• Measurement end interrupt • Frequency error interrupt • Overflow interrupt	• Measurement end interrupt • Frequency error interrupt • Overflow interrupt
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Table 2.12 Comparison of Clock Frequency Accuracy Measurement Circuit Registers

Register	Bit	RX64M (CAC)	RX66N (CAC)
CACR1	FMCS[2:0]	Measurement target clock select bits b3 b1 0 0 0: Main clock 0 0 1: Sub-clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDTCLK clock 1 0 1: Peripheral module clock B (PCLKB) Settings other than the above are prohibited.	Measurement target clock select bits b3 b1 0 0 0: Main clock 0 0 1: Sub-clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock B (PCLKB) 1 1 0: USB clock (UCLK) 1 1 1: External clock for the Ethernet-PHY (CLKOUT25M) Settings other than the above are prohibited.
CACR2	RSCS[2:0]	Measurement reference clock select bits b3 b1 0 0 0: Main clock 0 0 1: Sub-clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDTCLK clock 1 0 1: Peripheral module clock B (PCLKB) Settings other than the above are prohibited.	Measurement reference clock select bits b3 b1 0 0 0: Main clock 0 0 1: Sub-clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock B (PCLKB) 1 1 0: USB clock (UCLK) 1 1 1: External clock for the Ethernet-PHY (CLKOUT25M) Settings other than the above are prohibited.

2.7 Low Power Consumption

Table 2.13 is a comparative overview of the low power consumption functions, Table 2.14 is a comparison of procedures for entering and exiting low power consumption modes and operating states in each mode, and Table 2.15 is a comparison of low power consumption registers.

Table 2.13 Comparative Overview of Low Power Consumption Functions

Item	RX64M	RX66N
Reduced power consumption by switching clocks	The frequency division ratio is settable independently for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, and PCLKD), external bus clock (BCLK), and flash interface clock (FCLK).	The frequency division ratio is settable independently for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, and PCLKD), external bus clock (BCLK), and flash interface clock (FCLK).
BCLK output control function	It is possible to select between BCLK output and high output.	It is possible to select between BCLK output and high output.
SDCLK output control function	It is possible to select between SDCLK output and high output.	It is possible to select between SDCLK output and high output.
Module stop function	Functions can be stopped independently for each peripheral module.	Functions can be stopped independently for each peripheral module.
Function for transition to low power consumption mode	It is possible to transition to low power consumption modes that stop the CPU, peripheral modules, and oscillator.	It is possible to transition to low power consumption modes that stop the CPU, peripheral modules, and oscillator.
Low power consumption function	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode
Function for lower operating power consumption	• Power consumption can be reduced in normal operation, sleep mode, and all-module clock stop mode by selecting an appropriate operating power consumption control mode according to the operating frequency and operating voltage range. • Operating power control modes: 3 — High-speed operating mode — Low-speed operating mode 1 — Low-speed operating mode 2	• Power consumption can be reduced in normal operation, sleep mode, and all-module clock stop mode by selecting an appropriate operating power consumption control mode according to the operating frequency and operating voltage range. • Operating power control modes: 3 — High-speed operating mode — Low-speed operating mode 1 — Low-speed operating mode 2 There is no difference in power consumption when the same conditions (frequency and voltage) are set in low-speed operating modes 1 and 2.

Table 2.14 Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX64M	RX66N
Sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	PPLL	—	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM and ECCRAM: RX64M RAM, expansion RAM, and ECCRAM: RX66N	Operation possible (retained)	Operation possible (retained)
	Standby RAM	Operation possible (retained)	Operation possible (retained)
	Flash memory	Operation	Operation
	USBFS Host/Function module (USB)	Operation possible	Operation possible
	USBFS Host/Function module (USBA)	Operation possible	—
	Watchdog timer (WDT)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	8-bit timer (unit 0, unit 1) (TMR)	Operation possible	Operation possible
	Port output enable (POE)	—	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Operation possible	Operation possible
	I/O ports	Operation	Operation
All-module clock stop mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	PPLL	—	Operation possible
	CPU	Stopped (retained)	Stopped (retained)

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX64M	RX66N
All-module clock stop mode	RAM, ECCRAM: RX64M RAM, expansion RAM, ECCRAM: RX66N	Stopped (retained)	Stopped (retained)
	Standby RAM	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	USBFS Host/Function module (USB)	Stopped	Stopped
	USBFS Host/Function module (USBA)	Stopped	—
	Watchdog timer (WDT)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	8-bit timer (unit 0, unit 1) (TMR)	Operation possible	Operation possible
	Port output enable (POE)	—	Operation possible*1
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained
Software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Stopped
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Stopped	Stopped
	PPLL	—	Stopped
	CPU	Stopped (retained)	Stopped (retained)
	RAM, ECCRAM: RX64M RAM, expansion RAM, ECCRAM: RX66N	Stopped (retained)	Stopped (retained)
	Standby RAM	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	USBFS Host/Function module (USB)	Stopped	Stopped
	USBFS Host/Function module (USBA)	Stopped	—
	Watchdog timer (WDT)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	8-bit timer (unit 0, unit 1) (TMR)	Stopped (retained)	Stopped (retained)
	Port output enable (POE)	—	Stopped (retained)
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX64M	RX66N
Deep software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (reset processing)	Program execution state (reset processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Stopped
	IWDT-dedicated on-chip oscillator	Stopped (undefined)	Stopped (undefined)
	PLL	Stopped	Stopped
	PPLL	—	Stopped
	CPU	Stopped (undefined)	Stopped (undefined)
	RAM, ECCRAM: RX64M RAM, expansion RAM, ECCRAM: RX66N	Stopped (undefined)	Stopped (undefined)
	Standby RAM	Stopped (retained/undefined)	Stopped (retained/undefined)
	Flash memory	Stopped (retained)	Stopped (retained)
	USBFS Host/Function module (USB)	Stopped (retained/undefined)	Stopped (retained/undefined)
	USBFS Host/Function module (USBA)	Stopped (retained/undefined)	—
	Watchdog timer (WDT)	Stopped (undefined)	Stopped (undefined)
	Independent watchdog timer (IWDT)	Stopped (undefined)	Stopped (undefined)
	Realtime clock (RTC)	Operation possible	Operation possible
	8-bit timer (unit 0, unit 1) (TMR)	Stopped (undefined)	Stopped (undefined)
	Port output enable (POE)	—	Stopped (undefined)
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (undefined)	Stopped (undefined)
	I/O ports	Retained	Retained

Notes: “Operation possible” means that whether the state is operating or stopped is controlled by the control register setting.

“Stopped (retained)” means that internal register values are retained and internal operations are suspended.

“Stopped (undefined)” means that internal register values are undefined and power is not supplied to the internal circuit.

1. If POE interrupts are enabled and a POE interrupt source occurs while the chip is in all-module clock stop mode, return from all-module clock stop mode does not occur but the state of the interrupt source flag is retained. If a different source initiates return from all-module clock stop mode in this state, the POE interrupt is generated after the return.

Table 2.15 Comparison of Low Power Consumption Registers

Register	Bit	RX64M	RX66N
MSTPCRA	MSTPA7	General PWM timer bit Target module: GPTA	General PWM timer/GPTW dedicated port output enable module stop bit Target modules: GPTW and POEG
MSTPCRB	MSTPB12	Universal serial bus 2.0 HS interface module stop bit	—
	MSTPB14	Ethernet Controller and Ethernet controller DMA controller (channel 1) modules stop bit	—
	MSTPB15	Ethernet Controller and Ethernet controller DMA controller (channel 0) modules stop bit Target modules: ETHER and EDMAC (channel 0)	Ethernet controller, Ethernet controller DMA controller, and PHY management interface (channel 0) modules stop bit Target modules: ETHERC, EDMAC, and PMGI (channel 0)
	MSTPB16	—	Serial peripheral interface 1 module stop bit
	MSTPB20	—	I^2C bus interface 1 module stop bit
MSTPCRC	MSTPC2	Expansion RAM module stop bit	—
	MSTPC22	—	Serial peripheral interface 2 module stop bit
	MSTPC28	—	2D drawing engine module stop bit
	MSTPC29	—	Graphic-LCD controller module stop bit
MSTPCRD	MSTPD14	Serial sound interface 1 module stop bit Target module: SSI1	Extended serial sound interface 1 module stop bit Target module: SSIE1
	MSTPD15	Serial sound interface 0 module stop bit Target module: SSI0	Extended serial sound interface 0 module stop bit Target module: SSIE0
	MSTPD23	Sampling rate converter module stop bit	—
	MSTPD27	—	Trusted secure IP module stop bit

2.8 Register Write Protection Function

Table 2.16 is a comparative overview of the register write protection functions.

Table 2.16 Comparative Overview of Register Write Protection Functions

Item	RX64M	RX66N
PRC0 bit	Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, OSTDCR, OSTDSR	Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PACKCR, PLLCR, PLLCR2, PPLLCR, PPLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, OSTDCR, OSTDSR, CKOCR
PRC1 bit	• Registers related to the operating modes: SYSCR0, SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, DPSIEGR0 to DPSIEGR3 • Registers related to the clock generation circuit: MOSCWTCR, SOSCWTCR, MOFCR, HOCOPCR • Software reset register: SWRR	• Registers related to the operating modes: SYSCR0, SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, DPSIEGR0 to DPSIEGR3 • Registers related to the clock generation circuit: MOSCWTCR, SOSCWTCR, MOFCR, HOCOPCR • Software reset register: SWRR
PRC3 bit	Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

2.9 Exception Handling

Table 2.17 is a comparative overview of exception handling.

Table 2.17 Comparative Overview of Exception Handling

Item	RX64M	RX66N
Exception events	• Undefined instruction exception • Privileged instruction exception • Access exception • Floating-point exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap	• Undefined instruction exception • Privileged instruction exception • Access exception • Address exception • Single-precision floating-point exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap

2.10 Interrupt Controller

Table 2.18 is a comparative overview of the interrupt controllers, and Table 2.19 is a comparison of interrupt controller registers.

Table 2.18 Comparative Overview of Interrupt Controllers

Item		RX64M (ICUA)	RX66N (ICUD)
Interrupts	Peripheral function interrupts	Interrupts from peripheral modules • Interrupt detection method: Edge detection/level detection (fixed for each interrupt source) • Group interrupts: Multiple interrupt sources are grouped together and treated as a single interrupt source. — Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) — Group BL0/BL1 interrupts: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) — Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt B: Any of the interrupt sources for peripheral modules that use PCLKB as the operating clock can be assigned to interrupt vector numbers 128 to 207. • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.	Interrupts from peripheral modules • Interrupt detection method: Edge detection/level detection (fixed for each interrupt source) • Group interrupts: Multiple interrupt sources are grouped together and treated as a single interrupt source. — Group IE0 interrupt: Interrupt sources of coprocessors that use ICLK as the operating clock (edge detection) — Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) — Group BL0/BL1/BL2 interrupts: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) — Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt B: Any of the interrupt sources for peripheral modules that use PCLKB as the operating clock can be assigned to interrupt vector numbers 128 to 207. • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.

Item		RX64M (ICUA)	RX66N (ICUD)
Interrupts	External pin interrupts	Interrupts by input signals on IRQi pins (i = 0 to 15) • Interrupt detection: Ability to set as source detection of low level, falling edge, rising edge, or rising and falling edges • A digital filter can be used to remove noise.	Interrupts by input signals on IRQi pins (i = 0 to 15) • Interrupt detection: Ability to set as source detection of low level, falling edge, rising edge, or rising and falling edges • A digital filter can be used to remove noise.
	Software interrupts	• An interrupt request can be generated by writing to a register. • Number of sources: 2	• An interrupt request can be generated by writing to a register. • Number of sources: 2
	Interrupt priority	The priority level is set by writing to interrupt source priority register r (IPRr).	The priority level is set by writing to interrupt source priority register r (IPRr) (r = 000 to 255).
	Fast interrupt function	The CPU's interrupt response time can be reduced. This setting can be used for one interrupt source only.	The CPU's interrupt response time can be reduced. This setting can be used for one interrupt source only.
	DTC/DMAC control	Interrupt sources can be used to start the DTC and DMAC.	Interrupt sources can be used to start the DTC and DMAC.
	EXDMAC control	• An interrupt selected by software configurable interrupt B source select register 144 or software configurable interrupt A source select register 208 can be used to start EXDMAC0. • An interrupt selected by software configurable interrupt B source select register 145 or software configurable interrupt A source select register 209 can be used to start EXDMAC1.	• An interrupt selected by software configurable interrupt B source select register 144 or software configurable interrupt A source select register 208 can be used to start EXDMAC0. • An interrupt selected by software configurable interrupt B source select register 145 or software configurable interrupt A source select register 209 can be used to start EXDMAC1.
Non-maskable interrupts	NMI pin interrupt	Interrupt by the input signal on the NMI pin • Interrupt detection: Falling edge or rising edge • Digital filter can be used to remove noise.	Interrupt by the input signal on the NMI pin • Interrupt detection: Falling edge or rising edge • Digital filter can be used to remove noise.
	Oscillation stop detection interrupt	Interrupt occurs at detection of main clock oscillation having stopped.	Interrupt occurs at detection of main clock oscillation having stopped.
	WDT underflow/ refresh error interrupt	Interrupt occurs when the watchdog timer underflows or a refresh error occurs.	Interrupt occurs when the watchdog timer underflows or a refresh error occurs.
	IWDT underflow/ refresh error interrupt	Interrupt occurs when the independent watchdog timer underflows or a refresh error occurs.	Interrupt occurs when the independent watchdog timer underflows or a refresh error occurs.

Item		RX64M (ICUA)	RX66N (ICUD)
Non-maskable interrupts	Voltage monitoring 1 interrupt	Interrupt from voltage detection circuit 1 (LVD1)	Interrupt from voltage detection circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Interrupt from voltage detection circuit 2 (LVD2)	Interrupt from voltage detection circuit 2 (LVD2)
	RAM error interrupt	Interrupt occurs when a parity check error is detected in the RAM or an ECC error is detected in the ECCRAM.	Interrupt occurs when a parity check error is detected in the RAM (including the expansion RAM) or an ECC error is detected in the ECCRAM.
	Double-precision floating-point exceptions	—	Exceptions from double-precision floating-point coprocessor
Return from low power consumption state	Sleep mode	Exit sleep mode by any interrupt source.	Exit sleep mode by any interrupt source.
	All-module clock stop mode	Exit all-module clock stop mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection interrupt, USB resume, RTC alarm, RTC period, USBA resume, IWDT, software configurable interrupt 146 to 157).	Exit all-module clock stop mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection interrupt, USB resume, RTC alarm, RTC period, IWDT, software configurable interrupt 146 to 157).
	Software standby mode	Exit software standby mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, RTC period, USBA resume, IWDT).	Exit software standby mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, RTC period, IWDT).
	Deep software standby mode	Exit deep software standby mode by NMI pin interrupt, any among a subset of external pin interrupts, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, RTC period, USBA resume).	Exit deep software standby mode by NMI pin interrupt, any among a subset of external pin interrupts, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, RTC period).

Table 2.19 Comparison of Interrupt Controller Registers

Register	Bit	RX64M (ICUA)	RX66N (ICUD)
NMISR	ECCRAMST	RAM error interrupt status flag	—
	EXNMIST	—	Expanded non-maskable interrupt status flag
NMIER	ECCRAMEN	RAM error interrupt enable bit	—
	EXNMIEN	—	Expanded non-maskable interrupt enable bit
EXNMISR	—	—	Expanded non-maskable interrupt status register
EXNMIER	—	—	Expanded non-maskable interrupt enable register
EXNMICLR	—	—	Expanded non-maskable interrupt status clear register
GRPIE0	—	—	Group IE0 interrupt request register
GRPBL2	—	—	Group BL2 interrupt request register
GENIE0	—	—	Group IE0 interrupt request enable register
GENBL2	—	—	Group BL2 interrupt request enable register
GCRIE0	—	—	Group IE0 interrupt clear register
PIBRk	—	Software configurable interrupt B request register k (k = 0h to Ah)	Software configurable interrupt B request register k (k = 0h to Bh)
PIARk	—	Software configurable interrupt A request register k (k = 0h to Bh)	Software configurable interrupt A request register k (k = 0h to Ah, Ch)

2.11 Buses

Table 2.20 is a comparative overview of the buses, and Table 2.21 is a comparison of bus registers.

Table 2.20 Comparative Overview of Buses

Item		RX64M	RX66N
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, expansion RAM, ECCRAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, expansion RAM, ECCRAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	Connected to RAM	Connected to RAM
	Memory bus 2	Connected to code flash memory	Connected to code flash memory
	Memory bus 3	Connected to ECCRAM	Connected to expansion RAM and ECCRAM
Internal main buses	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DMAC, DTC, and EDMAC • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the DMAC, DTC, and extended bus master • Connected to on-chip memory (RAM, expansion RAM, ECCRAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, DMAC, EXDMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK) (EXDMAC operates in synchronization with the BCLK)	• Connected to peripheral modules (DTC, DMAC, EXDMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK) (EXDMAC operates in synchronization with the BCLK)
	Internal peripheral bus 2	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral module clock (PCLKB)	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1 and 3 to 5) • Operates in synchronization with the peripheral module clock (PCLKB)

Item		RX64M	RX66N
Internal peripheral buses	Internal peripheral bus 3	• Connected to peripheral modules (USBb, PDC, and standby RAM) • Operates in synchronization with the peripheral module clock (PCLKB)	• Connected to peripheral modules (USBb, PDC, and standby RAM) • Operates in synchronization with the peripheral module clock (PCLKB)
	Internal peripheral bus 4	• Connected to peripheral modules (EDMAC, ETHERC, EPTPC, MTU3, GPT, SCIF, RSPI, USBA, and AES) • Operates in synchronization with the peripheral module clock (PCLKA)	• Connected to peripheral modules (EDMAC, ETHERC, PMGI, GPTW, MTU, SCIi, and RSPI) • Operates in synchronization with the peripheral module clock (PCLKA)
	Internal peripheral bus 5	Reserved area	• Connected to peripheral modules (GLCDC and DRW2D) • Operates in synchronization with the peripheral module clock (PCLKA)
	Internal peripheral bus 6	• Connected to code flash (in P/E) and data flash memory • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to code flash (in P/E) and data flash memory • Operates in synchronization with the FlashIF clock (FCLK)
External bus	CS area	• Connected to external devices • Operates in synchronization with the external-bus clock (BCLK)	• Connected to external devices • Operates in synchronization with the external-bus clock (BCLK)
	SDRAM area	• Connected to SDRAM • Operates in synchronization with the SDRAM clock (SDCLK)	• Connected to SDRAM • Operates in synchronization with the SDRAM clock (SDCLK)

Table 2.21 Comparison of Bus Registers

Register	Bit	RX64M	RX66N
BERSR1	MST[2:0]	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: EDMAC 1 1 1: EXDMAC	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Extended bus master 1 1 1: EXDMAC
BUSPRI	BPRA[1:0]	Memory bus 1 and 3 (RAM/ECCRAM) priority control bits	Memory bus 1 and 3 (RAM/expansion RAM/ECCRAM) priority control bits
EBMAPCR	—	—	Extended bus master priority control register

2.12 Data Transfer Controller

Table 2.22 is a comparative overview of the data transfer controllers, and Table 2.23 is a comparison of data transfer controller registers.

Table 2.22 Comparative Overview of Data Transfer Controllers

Item	RX64M (DTCa)	RX66N (DTCb)
Number of transfer channels	Equal to number of all interrupt sources that can start a DTC transfer.	Equal to number of all interrupt sources that can start a DTC transfer.
Transfer modes	• Normal transfer mode — A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address returns to the transfer start address when the number of data transfers equals the repeat size. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, or 1,024 bytes. • Block transfer mode — A single activation leads to the transfer of a single block of data. — The maximum block size is 256 × 32 bits = 1,024 bytes.	• Normal transfer mode — A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address returns to the transfer start address when the number of data transfers equals the repeat size. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, or 1,024 bytes. • Block transfer mode — A single activation leads to the transfer of a single block of data. — The maximum block size is 256 × 32 bits = 1,024 bytes.
Chain transfer function	• Multiple data transfer types can be executed sequentially in response to a single transfer request. • Either “performed only when the transfer counter reaches 0” or “every time” can be selected.	• Multiple data transfer types can be executed sequentially in response to a single transfer request. • Either “performed only when the transfer counter reaches 0” or “every time” can be selected.
Sequence transfer	—	A complex series of transfers can be registered as a sequence. Any sequence can be selected by the transfer data and executed. • Only one sequence transfer trigger source can be selected at a time. • Up to 256 sequences can correspond to a single trigger source. • The data that is initially transferred in response to a transfer request determines the sequence. • The entire sequence can be executed on a single request, or the sequence can be suspended in the middle and resumed on the next transfer request (sequence division).

Item	RX64M (DTCa)	RX66N (DTCb)
Transfer space	• 16 MB in short-address mode (within 0000 0000h to 007F FFFFh or FF80 0000h to FFFF FFFFh, excluding reserved areas) • 4 GB in full-address mode (within 0000 0000h to FFFF FFFFh, excluding reserved areas)	• 16 MB in short-address mode (within 0000 0000h to 007F FFFFh or FF80 0000h to FFFF FFFFh, excluding reserved areas) • 4 GB in full-address mode (within 0000 0000h to FFFF FFFFh, excluding reserved areas)
Data transfer units	• Single data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data units	• Single data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data units
CPU interrupt sources	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.
Event link function	An event link request is generated after each data transfer (for block transfer, after each block is transferred).	An event link request is generated after each data transfer (for block transfer, after each block is transferred).
Read skip	Reading of the transfer information can be skipped when the same transfer is repeated.	Reading of the transfer information can be skipped when the same transfer is repeated.
Write-back skip	Write-back of transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.	Write-back of transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.
Write-back disable	—	Ability to disable write-back of transfer information
Displacement addition	—	Ability to add displacement to the transfer source address (selectable by each transfer information)
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Table 2.23 Comparison of Data Transfer Controller Registers

Register	Bit	RX64M (DTCa)	RX66N (DTCb)
MRA	WBDIS	—	Write-back disable bit
MRB	SQEND	—	Sequence transfer end bit
	INDX	—	Index table reference bit
MRC	—	—	DTC mode register C
DTCIBR	—	—	DTC index table base register
DTCOR	—	—	DTC operation register
DTCSQE	—	—	DTC sequence transfer enable register
DTCDISP	—	—	DTC address displacement register

2.13 Event Link Controller

Table 2.24 is a comparative overview of the event link controllers, Table 2.25 is a comparison of event link controller registers, Table 2.26 lists correspondences between ELSRn registers and peripheral modules, and Table 2.27 shows correspondences between values set in ELSRn.ELS[7:0] and event signal names and numbers.

Table 2.24 Comparative Overview of Event Link Controllers

Item	RX64M (ELC)	RX66N (ELC)
Event link function	• 119 event signals can be directly connected to modules. • Operation of timer modules while inputting an event signal can be selected. • Event linkage operation is possible on ports B and E. — Single port*1: Event link operation can be enabled on a single port corresponding to the specified bit. — Port group*1: Among the eight I/O ports, event link operation can be enabled for a group of ports corresponding to multiple specified bits.	• 123 event signals can be directly interconnected to modules. • Operation of timer modules while inputting an event signal can be selected. • Event linkage operation is possible on ports B and E. — Single port*1: Event link operation can be specified on a single port. — Port group*1: Event linkage operation can be specified by grouping multiple designated ports among up to eight ports.
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Note: 1. An event is generated when the corresponding input signal on a single port or port group set to input changes.

Table 2.25 Comparison of Event Link Controller Registers

Register	Bit	RX64M (ELC)	RX66N (ELC)
ELSRn	—	Event Link Setting Register n (n = 0, 3, 4, 7, 10 to 13, 15, 16, 18 to 28, 33, 35 to 38, and 41 to 45)	Event Link Setting Register n (n = 0, 3, 4, 7, 10 to 13, 15, 16, 18 to 28, 33, 35 to 38, 45, and 48 to 57)
	ELS[7:0]	Event link select bits 00h: Event output to the corresponding peripheral module is disabled. 01h to BDh: Specifies the number of the event signal to be linked. Settings other than the above are prohibited.	Event link select bits 00h: Event signal output to the corresponding peripheral module is disabled. 01h to CDh: Specifies the number of the event signal to be linked. Settings other than the above are prohibited.
ELOPI	—	Event link option setting register I	—
ELOPJ	—	Event link option setting register J	—

Table 2.26 Correspondence between ELSRn Registers and Peripheral Modules

Register	RX64M (ELC)	RX66N (ELC)
ELSR0	MTU0	MTU0
ELSR3	MTU3	MTU3
ELSR4	MTU4	MTU4
ELSR7	CMT1	CMT1
ELSR10	TMR0	TMR0
ELSR11	TMR1	TMR1
ELSR12	TMR2	TMR2
ELSR13	TMR3	TMR3
ELSR15	S12AD (ELCTRG0N)	S12AD (ELCTRG00N)
ELSR16	DA0	DA0
ELSR18	ICU (interrupt 1)	ICU (interrupt 1)
ELSR19	ICU (interrupt 2)	ICU (interrupt 2)
ELSR20	Output port group 1	Output port group 1
ELSR21	Output port group 2	Output port group 2
ELSR22	Input port group 1	Input port group 1
ELSR23	Input port group 2	Input port group 2
ELSR24	Single port 0	Single port 0
ELSR25	Single port 1	Single port 1
ELSR26	Single port 2	Single port 2
ELSR27	Single port 3	Single port 3
ELSR28	Clock source switching to LOCO	Clock source switching to LOCO
ELSR33	CMTW0	CMTW0
ELSR35	TPU0	TPU0
ELSR36	TPU1	TPU1
ELSR37	TPU2	TPU2
ELSR38	TPU3	TPU3
ELSR41	GPT0	—
ELSR42	GPT1	—
ELSR43	GPT2	—
ELSR44	GPT3	—
ELSR45	S12AD1 (ELCTRG1N)	S12AD1 (ELCTRG10N)
ELSR48	—	GPTW event source A (common to all channels)
ELSR49	—	GPTW event source B (common to all channels)
ELSR50	—	GPTW event source C (common to all channels)
ELSR51	—	GPTW event source D (common to all channels)
ELSR52	—	GPTW event source E (common to all channels)
ELSR53	—	GPTW event source F (common to all channels)
ELSR54	—	GPTW event source G (common to all channels)
ELSR55	—	GPTW event source H (common to all channels)
ELSR56	—	S12AD (ELCTRG01N)
ELSR57	—	S12AD1 (ELCTRG11N)

Table 2.27 Correspondence between Values Set in ELSRn.ELS[7:0] Bits and Event Signal Names and Numbers

Value of ELS[7:0] Bits	Peripheral Module	RX64M (ELC)	RX66N (ELC)
01h	Multifunction timer pulse unit 3	MTU0 compare match 0A	MTU0 compare match 0A
02h		MTU0 compare match 0B	MTU0 compare match 0B
03h		MTU0 compare match 0C	MTU0 compare match 0C
04h		MTU0 compare match 0D	MTU0 compare match 0D
05h		MTU0 compare match 0E	MTU0 compare match 0E
06h		MTU0 compare match 0F	MTU0 compare match 0F
07h		MTU0 overflow	MTU0 overflow
10h		MTU3 compare match 3A	MTU3 compare match 3A
11h		MTU3 compare match 3B	MTU3 compare match 3B
12h		MTU3 compare match 3C	MTU3 compare match 3C
13h		MTU3 compare match 3D	MTU3 compare match 3D
14h		MTU3 overflow	MTU3 overflow
15h		MTU4 compare match 4A	MTU4 compare match 4A
16h		MTU4 compare match 4B	MTU4 compare match 4B
17h		MTU4 compare match 4C	MTU4 compare match 4C
18h		MTU4 compare match 4D	MTU4 compare match 4D
19h		MTU4 overflow	MTU4 overflow
1Ah		MTU4 underflow	MTU4 underflow
1Fh	Compare match timer	CMT1 compare match 1	CMT1 compare match 1
22h	8-bit timer	TMR0 compare match A0	TMR0 compare match A0
23h		TMR0 compare match B0	TMR0 compare match B0
24h		TMR0 overflow	TMR0 overflow
25h		TMR1 compare match A1	TMR1 compare match A1
26h		TMR1 compare match B1	TMR1 compare match B1
27h		TMR1 overflow	TMR1 overflow
28h		TMR2 compare match A2	TMR2 compare match A2
29h		TMR2 compare match B2	TMR2 compare match B2
2Ah		TMR2 overflow	TMR2 overflow
2Bh		TMR3 compare match A3	TMR3 compare match A3
2Ch		TMR3 compare match B3	TMR3 compare match B3
2Dh		TMR3 overflow	TMR3 overflow
2Eh	Realtime clock	RTC cycle (select 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, 1, or 2 seconds)	RTC periodic event (select 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, 1, or 2 seconds)
31h	Independent watchdog timer	IWDT underflow or refresh error	IWDT underflow or refresh error
3Ah	Serial communications interface	SCI5 error (receive error or error signal detection)	SCI5 error (receive error or error signal detection)
3Bh		SCI5 receive data full	SCI5 receive data full
3Ch		SCI5 transmit data empty	SCI5 transmit data empty
3Dh		SCI5 transmit end	SCI5 transmit end
4Eh	I^2C bus interface	RIIC0 communication error or event generation	RIIC0 communication error or event generation
4Fh		RIIC0 receive data full	RIIC0 receive data full
50h		RIIC0 transmit data empty	RIIC0 transmit data empty
51h		RIIC0 transmit end	RIIC0 transmit end

Value of ELS[7:0] Bits	Peripheral Module	RX64M (ELC)	RX66N (ELC)
52h	Serial peripheral interface	RSPI0 error (mode fault, overrun, or parity error)	RSPI0 error (mode fault, overrun, underrun, or parity error)
53h		RSPI0 idle	RSPI0 idle
54h		RSPI0 receive data full	RSPI0 receive data full
55h		RSPI0 transmit data empty	RSPI0 transmit data empty
56h		RSPI0 transmit end	RSPI0 transmit end
58h	12-bit A/D converter	S12AD A/D conversion end	S12AD A/D conversion end
5Bh	Voltage detection circuit	LVD1 voltage detection	LVD1 voltage detection
5Ch		LVD2 voltage detection	LVD2 voltage detection
5Dh	DMA controller	DMAC0 transfer end	DMAC0 transfer end
5Eh		DMAC1 transfer end	DMAC1 transfer end
5Fh		DMAC2 transfer end	DMAC2 transfer end
60h		DMAC3 transfer end	DMAC3 transfer end
61h	Data transfer controller	DTC transfer end	DTC transfer end
62h	Clock generation circuit	Oscillation stop detection of clock generation circuit	Oscillation stop detection of clock generation circuit
63h	I/O ports	Input edge detection of input port group 1	Input edge detection of input port group 1
64h		Input edge detection of input port group 2	Input edge detection of input port group 2
65h		Input edge detection of single input port 0	Input edge detection of single input port 0
66h		Input edge detection of single input port 1	Input edge detection of single input port 1
67h		Input edge detection of single input port 2	Input edge detection of single input port 2
68h		Input edge detection of single input port 3	Input edge detection of single input port 3
69h	Event link controller	Software event	Software event
6Ah	Data operation circuit	DOC data operation condition met signal	DOC data operation condition met
6Ch	12-bit A/D converter	S12AD1 A/D conversion end	S12AD1 A/D conversion end
7Eh	Compare match timer W	CMTW channel 0 compare match	CMTW channel 0 compare match
80h	General PWM timer	GPT0 compare match A	GPTW0 compare match A
81h		GPT0 compare match B	GPTW0 compare match B
82h		GPT0 compare match C	GPTW0 compare match C
83h		GPT0 compare match D	GPTW0 compare match D
84h		—	GPTW0 compare match E
85h		—	GPTW0 compare match F
86h		GPT0 overflow	GPTW0 overflow
87h		GPT0 underflow	GPTW0 underflow
88h		GPT1 compare match A	GPTW1 compare match A
89h		GPT1 compare match B	GPTW1 compare match B
8Ah		GPT1 compare match C	GPTW1 compare match C
8Bh		GPT1 compare match D	GPTW1 compare match D

Value of ELS[7:0] Bits	Peripheral Module	RX64M (ELC)	RX66N (ELC)
8Ch	General PWM timer	—	GPTW1 compare match E
8Dh		—	GPTW1 compare match F
8Eh		GPT1 overflow	GPTW1 overflow
8Fh		GPT1 underflow	GPTW1 underflow
90h		GPT2 compare match A	GPTW2 compare match A
91h		GPT2 compare match B	GPTW2 compare match B
92h		GPT2 compare match C	GPTW2 compare match C
93h		GPT2 compare match D	GPTW2 compare match D
94h		—	GPTW2 compare match E
95h		—	GPTW2 compare match F
96h		GPT2 overflow	GPTW2 overflow
97h		GPT2 underflow	GPTW2 underflow
98h		GPT3 compare match A	GPTW3 compare match A
99h		GPT3 compare match B	GPTW3 compare match B
9Ah		GPT3 compare match C	GPTW3 compare match C
9Bh		GPT3 compare match D	GPTW3 compare match D
9Ch		—	GPTW3 compare match E
9Dh		—	GPTW3 compare match F
9Eh		GPT3 overflow	GPTW3 overflow
9Fh		GPT3 underflow	GPTW3 underflow
A0h	Ethernet controller	EPTPC STCA timer 0 rising edge detection	—
A1h		EPTPC STCA timer 1 rising edge detection	—
A2h		EPTPC STCA timer 2 rising edge detection	—
A3h		EPTPC STCA timer 3 rising edge detection	—
A4h		EPTPC STCA timer 4 rising edge detection	—
A5h		EPTPC STCA timer 5 rising edge detection	—
A6h		EPTPC STCA timer 0 falling edge detection	—
A7h		EPTPC STCA timer 1 falling edge detection	—
A8h		EPTPC STCA timer 2 falling edge detection	—
A9h		EPTPC STCA timer 3 falling edge detection	—
AAh		EPTPC STCA timer 4 falling edge detection	—
ABh		EPTPC STCA timer 5 falling edge detection	—
ACh	16-bit timer pulse unit	TPU0 compare match A	TPU0 compare match A
ADh		TPU0 compare match B	TPU0 compare match B
AEh		TPU0 compare match C	TPU0 compare match C
AFh		TPU0 compare match D	TPU0 compare match D
B0h		TPU0 overflow	TPU0 overflow
B1h		TPU1 compare match A	TPU1 compare match A
B2h		TPU1 compare match B	TPU1 compare match B

Value of ELS[7:0] Bits	Peripheral Module	RX64M (ELC)	RX66N (ELC)
B3h	16-bit timer pulse unit	TPU1 overflow	TPU1 overflow
B4h		TPU1 underflow	TPU1 underflow
B5h		TPU2 compare match A	TPU2 compare match A
B6h		TPU2 compare match B	TPU2 compare match B
B7h		TPU2 overflow	TPU2 overflow
B8h		TPU2 underflow	TPU2 underflow
B9h		TPU3 compare match A	TPU3 compare match A
BAh		TPU3 compare match B	TPU3 compare match B
BBh		TPU3 compare match C	TPU3 compare match C
BCh		TPU3 compare match D	TPU3 compare match D
BDh		TPU3 overflow	TPU3 overflow
C6h	General PWM timer	—	GPTW0 A/D converter start request A
C7h		—	GPTW0 A/D converter start request B
C8h		—	GPTW1 A/D converter start request A
C9h		—	GPTW1 A/D converter start request B
CAh		—	GPTW2 A/D converter start request A
CBh		—	GPTW2 A/D converter start request B
CCh		—	GPTW3 A/D converter start request A
CDh		—	GPTW3 A/D converter start request B

2.14 I/O Ports

Table 2.28 is a comparative overview of the I/O ports of 176-pin products, and Table 2.29 is a comparison of I/O port registers.

Table 2.28 Comparative Overview of I/O Ports of 176-Pin Products

Item	RX64M (176-Pin)	RX66N (176-Pin)
PORT0	P00 to P03, P05, P07	P00 to P03, P05, P07
PORT1	P10 to P17	P10 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P53	P50 to P57
PORT6	P60 to P67	P60 to P67
PORT7	P70 to P77	P70 to P77
PORT8	P80 to P83, P86, P87	P80 to P87
PORT9	P90 to P97	P90 to P97
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7
PORTF	PF0 to PF5	PF0 to PF5
PORTG	PG0 to PG7	PG0 to PG7
PORTJ	PJ3, PJ5	PJ0 to PJ3, PJ5

Table 2.29 Comparison of I/O Port Registers

Register	Bit	RX64M	RX66N
PDR	B0 to B7	Pm0 to Pm7 I/O select bits (m = 0 to 9, A to G, and J)	Pm0 to Pm7 I/O select bits (m = 0 to 9, A to H, J to N, and Q)
PODR	B0 to B7	Pm0 to Pm7 output data store bits (m = 0 to 9, A to G, and J)	Pm0 to Pm7 output data store bits (m = 0 to 9, A to H, J to N, and Q)
PIDR	B0 to B7	Pm0 to Pm7 bits (m = 0 to 9, A to G, and J)	Pm0 to Pm7 bits (m = 0 to 9, A to H, J to N, and Q)
PMR	B0 to B7	Pm0 to Pm7 pin mode control bits (m = 0 to 9, A to G, and J)	Pm0 to Pm7 pin mode control bits (m = 0 to 9, A to H, J to N, and Q)
ODR0	B0	Pm0 output type select bit (m = 0 to 9, A to G, and J)	Pm0 output type select bit (m = 0 to 9, A to H, J to N, and Q)
	B2	Pm1 output type select bit (m = 0 to 9, A to G, and J)	Pm1 output type select bit (m = 0 to 9, A to H, J to N, and Q)
	B3	PE1 output type select bit (m = 0 to 9, A to G, and J)	PE1 output type select bit (m = 0 to 9, A to H, J to N, and Q)
	B4	Pm2 output type select bit (m = 0 to 9, A to G, and J)	Pm2 output type select bit (m = 0 to 9, A to H, J to N, and Q)
	B6	Pm3 output type select bit (m = 0 to 9, A to G, and J)	Pm3 output type select bit (m = 0 to 9, A to H, J to N, and Q)
ODR1	B0	Pm4 output type select bit (m = 0 to 9, A to G, and J)	Pm4 output type select bit (m = 0 to 9, A to H, J to N, and Q)
	B2	Pm5 output type select bit (m = 0 to 9, A to G, and J)	Pm5 output type select bit (m = 0 to 9, A to H, J to N, and Q)
	B4	Pm6 output type select bit (m = 0 to 9, A to G, and J)	Pm6 output type select bit (m = 0 to 9, A to H, J to N, and Q)
	B6	Pm7 output type select bit (m = 0 to 9, A to G, and J)	Pm7 output type select bit (m = 0 to 9, A to H, J to N, and Q)
PCR	B0 to B7	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A to G, and J)	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A to H, J to N, and Q)
DSCR	B0 to B7	Pm0 to Pm7 drive capacity control bits (m = 0, 2, 5, 9, A to E, and G)	Pm0 to Pm7 drive capacity control bits (m = 0 to 2, 5, 7 to 9, A to E, G, H, J to N, and Q)
DSCR2	—	—	Drive capacity control register 2

2.15 Multi-Function Pin Controller

Table 2.30 is a comparison of multi-function pin controller registers.

Table 2.30 Comparison of Multi-Function Pin Controller Registers

Register	Bit	RX64M (MPC)	RX66N (MPC)
PmnPFS	—	For details of the pin function control registers, refer to the User's Manual: Hardware of each MCU.	
PFBCR0	ADRHMS ADRHMS2	A16 to A23 output enable bit (b1) A16 to A23 output enable 2 bit (b2) b2 b1 0 0: Set PC0 to PC7. 0 1: Set P90 to P97. 1 0: Set PC0, PC1, P71, P72, P74, and PC5 to PC7. 1 1: Setting prohibited.	A16 to A23 output enable bit (b1) A16 to A23 output enable 2 bit (b2) b2 b1 0 0: Set PC0 to PC7. 0 1: 224- and 176-pin products: Set P90 to P97. 145- and 144-pin products: Set P90 to P93 (A20 to A23 not assigned). 1 0: Set PC0, PC1, P71, P72, P74, and PC5 to PC7. 1 1: Setting prohibited. On 100-pin products, set these bits to 00b.
PFBCR1	WAITS[1:0]	WAIT select bits b1 b0 0 0: Setting invalid 0 1: Set P55 as WAIT# input pin. 1 0: Set PC5 as WAIT# input pin. 1 1: Set P51 as WAIT# input pin.	WAIT select bits Specifies the port set as the WAIT# input pin in combination with the PFBCR3.WAITS2 bit. For details, refer to RX66N Group User's Manual: Hardware.
	MDSDE	SDRAM pin enable bit	SDRAM pin enable bit*1
	DQM1E	DQM1 enable bit	DQM1 enable bit*1
	SDCLKE	SDCLK enable bit	SDCLK enable bit*1
PFBCR2	—	—	External bus control register 2
PFBCR3	—	—	External bus control register 3
PFENET	PHYMODE1	Ethernet channel 1 mode set bit	—

Note: 1. These are reserved bits on 100-pin products. These bits are read as 0. The write value should be 0.

2.16 Port Output Enable 3

Table 2.31 is a comparative overview of the port output enable 3 modules, and Table 2.32 is a comparison of port output enable 3 registers.

Table 2.31 Comparative Overview of Port Output Enable 3 Modules

Item	RX64M (POE3a)	RX66N (POE3a)
Pin status while output is disabled	High-impedance	High-impedance
Pins subject to high-impedance control	• MTU output pins — MTU0 pin (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) — MTU3 pin (MTIOC3B, MTIOC3D) — MTU4 pin (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) — MTU6 pin (MTIOC6B, MTIOC6D) — MTU7 pin (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D) • GPT output pins — GPT0 pin (GTIOC0A, GTIOC0B) — GPT1 pin (GTIOC1A, GTIOC1B) — GPT2 pin (GTIOC2A, GTIOC2B) — GPT3 pin (GTIOC3A, GTIOC3B)	• MTU output pins — MTU0 pin (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) — MTU3 pin (MTIOC3B, MTIOC3D) — MTU4 pin (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) — MTU6 pin (MTIOC6B, MTIOC6D) — MTU7 pin (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D)
High-impedance request generation conditions	• Input pin changes When signal input occurs on pin POE0#, POE4#, POE8#, POE10#, or POE11# • Short circuit of output pins: When an output signal level (active level) combination listed below (short circuit) continues for one or more cycles [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D — MTIOC6B and MTIOC6D — MTIOC7A and MTIOC7C — MTIOC7B and MTIOC7D [GPT output pins] — GTIOC0A and GTIOC0B — GTIOC1A and GTIOC1B — GTIOC2A and GTIOC2B • Making of register setting • Detection of stopped oscillation on main clock oscillator	• Input pin changes When signal input occurs on pin POE0#, POE4#, POE8#, POE10#, or POE11# • Short circuit of output pins: When an output signal level (active level) combination listed below (short circuit) continues for one or more cycles [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D — MTIOC6B and MTIOC6D — MTIOC7A and MTIOC7C — MTIOC7B and MTIOC7D • Making of SPOER register setting • Detection of stopped oscillation on main clock oscillator

Item	RX64M (POE3a)	RX66N (POE3a)
Functions	• Input pins POE0#, POE4#, POE8#, POE10#, and POE11# can each be set for falling edge, PCLK/8 × 16, PCLK/16 × 16, or PCLK/128 × 16 low sampling.	• Input pins POE0#, POE4#, POE8#, POE10#, and POE11# can each be set for falling edge, PCLK/8 × 16, PCLK/16 × 16, or PCLK/128 × 16 low sampling.
	• The MTU complementary PWM output pins, the MTU0 pins, the GPT output pins, and the GPT3 pins can be put in the high-impedance state by falling-edge or low-level sampling of the POE0#, POE4#, POE8#, POE10#, or POE11# pin.	• The outputs of all the target pins can be put in the high-impedance state by falling-edge or low-level sampling of the POE0#, POE4#, POE8#, POE10#, or POE11# pin.
	• The MTU complementary PWM output pins, the MTU0 pins, the GPT output pins, and the GPT3 pins can be put in the high-impedance state when oscillation stop of the clock generator circuit is detected.	• The outputs of all the target pins can be put in the high-impedance state when oscillation stop of the clock generator is detected.
	• The MTU complementary PWM output pins or the GPT output pins can be put in the high-impedance state when the output levels of the MTU complementary PWM output pins or the GPT output pins (GPT0, GPT1, and GPT2) are compared and simultaneous active-level output continues for one clock cycle or more.	• The MTU complementary PWM outputs can be put in the high-impedance state when the output levels of the MTU complementary PWM output pins are compared and simultaneous active-level output continues for one clock cycle or more.
	• The MTU complementary PWM output pins, the MTU0 pins, the GPT output pins, and the GPT3 pins can be put in the high-impedance state by modifying the settings of the POE registers.	• The outputs of all the target pins can be put in the high-impedance state by modifying the settings of the POE3 registers.
	• Interrupts can be generated by input-level sampling or output-level comparison results.	• Interrupts can be generated by input-level sampling or output-level comparison results.

Table 2.32 Comparison of Port Output Enable 3 Registers

Register	Bit	RX64M (POE3a)	RX66N (POE3a)
OCSR1	OSF1	Output short flag 1 This flag indicates that at least one of the three pairs of two-phase output pins for MTU complementary PWM output (pins MTU3 and MTU4) or GPT output (pins GPT0 to GPT2) has simultaneously entered the active level. [Setting condition] When at least one of the three pairs of two-phase output pins has simultaneously entered the active level. [Clearing condition] When 0 is written to the OSF1 flag after reading it as 1 To write 0 to this flag, the inactive level must be output from the MTU complementary PWM output pins or GPT output pins.	Output short flag 1 This flag indicates that at least one of the three pairs of two-phase output pins for MTU complementary PWM output (pins MTU3 and MTU4) has simultaneously entered the active level. If high-impedance control is not enabled for the corresponding pins, this flag is not set to 1. [Setting condition] • When simultaneous active-level output continues on pins MTIOC3B and MTIOC3D for one clock cycle or more while the value of the POECR2.MTU3BDZE bit is 1. • When simultaneous active-level output continues on pins MTIOC4A and MTIOC4C for one clock cycle or more while the value of the POECR2.MTU4ACZE bit is 1. • When simultaneous active-level output continues on pins MTIOC4B and MTIOC4D for one clock cycle or more while the value of the POECR2.MTU4BDZE bit is 1. [Clearing condition] When 0 is written to the OSF1 flag after reading it as 1 To write 0 to this flag, the inactive level must be output from the MTU complementary PWM output pins.
ALR1	OLSG0A	MTIOC3B/GTIOC0A pin active level setting bit	MTIOC3B pin active level setting bit
	OLSG0B	MTIOC3D/GTIOC0B pin active level setting bit	MTIOC3D pin active level setting bit
	OLSG1A	MTIOC4A/GTIOC1A pin active level setting bit	MTIOC4A pin active level setting bit
	OLSG1B	MTIOC4C/GTIOC1B pin active level setting bit	MTIOC4C pin active level setting bit
	OLSG2A	MTIOC4B/GTIOC2A pin active level setting bit	MTIOC4B pin active level setting bit
	OLSG2B	MTIOC4D/GTIOC2B pin active level setting bit	MTIOC4D pin active level setting bit

Register	Bit	RX64M (POE3a)	RX66N (POE3a)
SPOER	MTUCH34HIZ	MTU3 and MTU4 or GPT0 to GPT2 output high-impedance enable bit	MTU3 and MTU4 pin high-impedance enable bit
	GPT01HIZ	GPT0 and GPT1 output high-impedance enable bit	—
	GPT23HIZ	GPT2 and GPT3 output high-impedance enable bit	—
POECR2	MTU4BDZE*1	MTIOC4B/MTIOC4D high-impedance enable bit	MTIOC4B/MTIOC4D pin high-impedance enable bit
	MTU4ACZE*1	MTIOC4A/MTIOC4C high-impedance enable bit	MTIOC4A/MTIOC4C pin high-impedance enable bit
	MTU3BDZE*1	MTIOC3B/MTIOC3D high-impedance enable bit	MTIOC3B/MTIOC3D pin high-impedance enable bit
POECR3	—	Port output enable control register 3	—
POECR4	IC2ADDMT34ZE *1	MTU3 and MTU4 high-impedance POE4F add bit	MTU3 and MTU4 high-impedance condition POE4F add bit
	IC3ADDMT34ZE *1	MTU3 and MTU4 high-impedance POE8F add bit	MTU3 and MTU4 high-impedance condition POE8F add bit
	IC4ADDMT34ZE *1	MTU3 and MTU4 high-impedance POE10F add bit	MTU3 and MTU4 high-impedance condition POE10F add bit
	IC5ADDMT34ZE *1	MTU3 and MTU4 high-impedance POE11F add bit	MTU3 and MTU4 high-impedance condition POE11F add bit
POECR6	—	Port output enable control register 6	—
G0SELR	—	GPT0 pin select register	—
G1SELR	—	GPT1 pin select register	—
G2SELR	—	GPT2 pin select register	—
G3SELR	—	GPT3 pin select register	—
M6SELR	—	—	MTU6 pin select register
MGSELR	—	MTU/GPT pin function select register	—

Note: 1. On the RX64M the GPT and MTU pins can be controlled, but on the RX66N only the MTU pins can be controlled.

2.17 General PWM Timer

Table 2.33 is a comparative overview of general PWM timers, and Table 2.34 is a comparison of general PWM timer registers.

Table 2.33 Comparative Overview of General PWM Timers

Item	RX64M (GPTA)	RX66N (GPTW)
Functions	• 16 bits × 4 channels • Up-count or down-count operation (saw waves) or up/down-count operation (triangle waves) for each counter • Operating modes — Saw-wave PWM mode — Saw-wave one-shot pulse mode — Triangle-wave PWM mode 1 — Triangle-wave PWM mode 2 — Triangle-wave PWM mode 3 • Independently selectable clock source for each channel • Two input/output pins per channel • Two output compare/input capture registers per channel • For each pair of output compare/input capture registers for each channel, four registers are provided as buffer registers and are capable of operating as compare registers when buffering is not in use. • During output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetric PWM waveforms. • Registers for setting up frame cycles in each channel (with capability for generating interrupts at overflow or underflow) • Generation of dead time during PWM operation • Simultaneous start and clearing of desired channel counters • Operation of count start, count stop, counter restart, or input capture based on ELC settings	• 32 bits × 4 channels • Up-count or down-count operation (saw waves) or up/down-count operation (triangle waves) for each counter • Operating modes — Saw-wave PWM mode — Saw-wave one-shot pulse mode — Triangle-wave PWM mode 1 — Triangle-wave PWM mode 2 — Triangle-wave PWM mode 3 • Independently selectable clock source for each channel • Two input/output pins per channel • Two output compare/input capture registers per channel • For each pair of output compare/input capture registers for each channel, four registers are provided as buffer registers and are capable of operating as compare registers when buffering is not in use. • During output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetric PWM waveforms. • Registers for setting up frame cycles in each channel (with capability for generating interrupts at overflow or underflow) • Generation of dead time during PWM operation • Simultaneous start, stop, and clearing of desired channel counters • Operation of count start, count stop, counter clearing, up-counting, down-counting, or input capture by up to of eight ELC events based on ELC settings

Item	RX64M (GPTA)	RX66N (GPTW)
Functions	• Count start, counter clearing, or count stop in response to external or internal triggers (hardware sources) • Internal trigger sources: software or compare match • A/D converter start trigger generation function • Event signals for compare match A to D and for overflow/underflow can be output to the ELC. • Ability to select noise filter for each pin input path • Bus clock: PCLKA, GPTA count reference clock: PCLKA	• Count start, count stop, counter clearing, up-counting, down-counting, or input capture at detection of two input signal conditions • Count start, count stop, counter clearing, up-counting, down-counting, or input capture by up to four external triggers • Function to control output negation by output disable requests from the POEG • A/D converter start trigger generation function • Event signals for compare match A to F and for overflow/underflow can be output to the ELC. • Ability to select noise filter for each pin input path • Bus clock: PCLKA, GPTW count reference clock: PCLKA

Table 2.34 Comparison of General PWM Timer Registers

Register	Bit	RX64M (GPTA)	RX66N (GPTW)
GTSTR	—	General PWM timer software start register GTSTR is a 16-bit register.	General PWM timer software start register GTSTR is a 32-bit register.
	CST0 (RX64M) CSTRT0 (RX66N)	GPT0.GTCNT count start bit	Channel 0 count start bit
	CST1 (RX64M) CSTRT1 (RX66N)	GPT1.GTCNT count start bit	Channel 1 count start bit
	CST2 (RX64M) CSTRT2 (RX66N)	GPT2.GTCNT count start bit	Channel 2 count start bit
	CST3 (RX64M) CSTRT3 (RX66N)	GPT3.GTCNT count start bit	Channel 3 count start bit
NFCR	—	Noise filter control register	—
GTHSCR	—	General PWM timer hardware source start/stop control register	—
GTHCCR	—	General PWM timer hardware source clear control register	—
GTHSSR	—	General PWM timer hardware start source select register	—
GTHPSR	—	General PWM timer hardware stop/clear source select register	—
GTWP	—	General PWM timer write-protection register GTWP is a 16-bit register.	General PWM timer write-protection register GTWP is a 32-bit register.
	WP0 to WP3 (RX64M) WP (RX66N)	GPT0 to GPT3 register write enable bits	Register write disabled bits
	STRWP	—	GTSTR.CSTRT bit write disabled bit
	STPWP	—	GTSTP.CSTOP bit write disabled bit
	CLRWP	—	GTCLR.CCLR bit write disabled bit
	CMNWP	—	Common register write disabled bit
	PRKEY[7:0]	—	GTWP key code bits
GTSYNC	—	General PWM timer sync register	—
GTETINT	—	General PWM timer external trigger input interrupt register	—
GTBDR	—	General PWM timer buffer operation disable register	—
GTSWP	—	General PWM timer start write-protection register	—

Register	Bit	RX64M (GPTA)	RX66N (GPTW)
GTIOR	—	General PWM timer I/O control register GTIOR is a 16-bit register.	General PWM timer I/O control register GTIOR is a 32-bit register.
	GTIOA[5:0] (RX64M) GTIOA[4:0] (RX66N)	GTIOCnA pin function select bits (b5 to b0) Refer to RX64M Group User's Manual: Hardware for details.	GTIOCnA pin function select bits (b4 to b0) Refer to RX66N Group User's Manual: Hardware for details.
	OAE	—	GTIOCnA pin output enable bit
	OADF[1:0]	—	GTIOCnA pin negate value setting bits
	NFAEN	—	GTIOCnA pin input noise filter enable bit
	NFCSA[1:0]	—	GTIOCnA pin input noise filter sampling clock select bits
	GTIOB[5:0] (RX64M) GTIOB[4:0] (RX66N)	GTIOCnB pin function select bits (b13 to b8) Refer to RX64M Group User's Manual: Hardware for details.	GTIOCnB pin function select bits (b20 to b16) Refer to RX66N Group User's Manual: Hardware for details.
	OBDFLT	GTIOCnB pin output value setting at count stop bit (b14)	GTIOCnB pin output value setting at count stop bit (b22)
	OBHLD	GTIOCnB pin output retention at start/stop count (b15)	GTIOCnB pin output retention at start/stop count (b23)
	OBE	—	GTIOCnB pin output enable bit
	OBDF[1:0]	—	GTIOCnB pin negate value setting bits
	NFBEN	—	GTIOCnB pin input noise filter enable bit
	NFCSB[1:0]	—	GTIOCnB pin input noise filter sampling clock select bits
GTINTAD	—	General PWM timer interrupt output setting register GTINTAD is a 16-bit register.	General PWM timer interrupt output setting register GTINTAD is a 32-bit register.
	EINT	Dead time error interrupt enable bit	—
	ADTRAUEN	GTADTRA compare match (up-counting) A/D converter start request enable bit (b12)	GTADTRA register compare match (up-counting) A/D converter start request enable bit (b16)
	ADTRADEN	GTADTRA compare match (down-counting) A/D converter start request enable bit (b13)	GTADTRA register compare match (down-counting) A/D converter start request enable bit (b17)
	ADTRBUEN	GTADTRB compare match (up-counting) A/D converter start request enable bit (b14)	GTADTRB register compare match (up-counting) A/D converter start request enable bit (b18)
	ADTRBDEN	GTADTRB compare match (down-counting) A/D converter start request enable bit (b15)	GTADTRB register compare match (down-counting) A/D converter start request enable bit (b19)

Register	Bit	RX64M (GPTA)	RX66N (GPTW)
GTINTAD	GRP[1:0]	—	Output stop group select bits
	GRPDTE	—	Dead time error output stop detection enable bit
	GRPABH	—	Simultaneous high output stop detection enable bit
	GRPABL	—	Simultaneous low output stop detection enable bit
GTCR	—	General PWM timer control register GTCR is a 16-bit register.	General PWM timer control register GTCR is a 32-bit register.
	CST	—	Count start bit
	ICDS	—	Input capture operation select at count stop bit
	MD[2:0]	Mode select bits (b2 to b0) b2 b0 0 0 0: Sawtooth-wave PWM mode (single buffer or double buffer possible) 0 0 1: Sawtooth-wave one-shot pulse mode (fixed buffer operation) 0 1 0: Setting prohibited. 0 1 1: Setting prohibited. 1 0 0: Triangle-wave PWM mode 1 (16-bit transfer at trough) (single buffer or double buffer possible) 1 0 1: Triangle-wave PWM mode 2 (16-bit transfer at crest and trough) (single buffer or double buffer possible) 1 1 0: Triangle-wave PWM mode 3 (32-bit transfer at trough) (fixed buffer operation) 1 1 1: Setting prohibited.	Mode select bits (b18 to b16) b18 b16 0 0 0: Sawtooth-wave PWM mode (single buffer or double buffer possible) 0 0 1: Sawtooth-wave one-shot pulse mode (fixed buffer operation) 0 1 0: Setting prohibited. 0 1 1: Setting prohibited. 1 0 0: Triangle-wave PWM mode 1 (32-bit transfer at trough) (single buffer or double buffer possible) 1 0 1: Triangle-wave PWM mode 2 (32-bit transfer at crest and trough) (single buffer or double buffer possible) 1 1 0: Triangle-wave PWM mode 3 (64-bit transfer at trough) (fixed buffer operation) 1 1 1: Setting prohibited.

Register	Bit	RX64M (GPTA)	RX66N (GPTW)
GTCR	TPCS[1:0] (RX64M) TPCS[3:0] (RX66N)	Timer prescaler select bits (b9 to b8) b9 b8 0 0: PCLKA 0 1: PCLKA/2 1 0: PCLKA/4 1 1: PCLKA/8	Timer prescaler select bits (b26 to b23) b26 b23 0 0 0 0: PCLKA 0 0 0 1: PCLKA/2 0 0 1 0: PCLKA/4 0 0 1 1: PCLKA/8 0 1 0 0: PCLKA/16 0 1 0 1: PCLKA/32 0 1 1 0: PCLKA/64 0 1 1 1: Setting prohibited. 1 0 0 0: PCLKA/256 1 0 0 1: Setting prohibited. 1 0 1 0: PCLKA/1024 1 0 1 1: Setting prohibited. 1 1 0 0: GTETRGA (via the POEG) 1 1 0 1: GTETRGB (via the POEG) 1 1 1 0: GTETRGC (via the POEG) 1 1 1 1: GTETRGD (via the POEG)
	CCLR[1:0]	Count clear source select bits	—
GTBER	—	General PWM timer buffer enable register GTBER is a 16-bit register.	General PWM timer buffer enable register GTBER is a 32-bit register.
	BD[0]	—	GTCCRA/GTCCRB registers buffer operation disable bit
	BD[1]	—	GTPR register buffer operation disable bit
	BD[2]	—	GTADTRA/GTADTRB registers buffer operation disable bit
	BD[3]	—	GTDVU/GTDVD registers buffer operation disable bit
	DBRTECA	—	GTCCRA register double buffer repeat operation enable bit
	DBRTECB	—	GTCCRB register double buffer repeat operation enable bit
	CCRA[1:0]	GTCCRA buffer operation bits (b1 and b0)	GTCCRA register buffer operation bits (b17 and 16)
	CCRB[1:0]	GTCCRB buffer operation bits (b3 and b2)	GTCCRB register buffer operation bits (b19 and 18)
	PR[1:0]	GTPR buffer operation bits (b5 and b4)	GTPR register buffer operation bits (b21 and b20)
	CCRSWT	GTCCRA and GTCCRB forcible buffer operation bit (b6)	GTCCRA and GTCCRB registers forcible buffer operation bit (b22)
	ADTTA[1:0]	GTADTRA buffer transfer timing select bits (b9 and b8)	GTADTRA register buffer transfer timing select bits (b25 and b24)

Register	Bit	RX64M (GPTA)	RX66N (GPTW)
GTBER	ADTDA	GTADTRA double buffer operation bit (b10)	GTADTRA register double buffer operation bit (b26)
	ADTTB[1:0]	GTADTRB buffer transfer timing select bits (b13 and b12)	GTADTRB register buffer transfer timing select bits (b29 and b28)
	ADTDB	GTADTRB double buffer operation bit (b14)	GTADTRB register double buffer operation bit (b30)
GTUDC	—	General PWM timer count direction register	—
GTITC	—	General PWM timer interrupt and A/D converter start request skipping setting register GTITC is a 16-bit register.	General PWM timer interrupt and A/D converter start request skipping setting register GTITC is a 32-bit register.
GTST	—	General PWM timer status register GTST is a 16-bit register.	General PWM timer status register GTST is a 32-bit register.
	DTEF	Dead time error flag (b11)	Dead time error flag (b28)
	ADTRAUF	—	GTADTRA register compare match (up-counting) A/D converter start request flag
	ADTRADF	—	GTADTRA register compare match (down-counting) A/D converter start request flag
	ADTRBUF	—	GTADTRB register compare match (up-counting) A/D converter start request flag
	ADTRBDF	—	GTADTRB register compare match (down-counting) A/D converter start request flag
	ODF	—	Output stop request flag
	OABHF	—	Simultaneous high output flag
	OABLF	—	Simultaneous low output flag
GTCNT	—	General PWM timer counter The GTCNT counter is a 16-bit readable/writable counter. Access in 8-bit units to the GTCNT counter is prohibited; it must be accessed in 16-bit units.	General PWM timer counter The GTCNT register is a 32-bit readable/writable counter. Access in 8-bit or 16-bit units to the GTCNT register is prohibited; it must be accessed in 32-bit units. Set the GTCNT counter within a range of 0 ≤ GTCNT counter ≤ GTPR register.
GTCCRm	—	General PWM timer compare capture register m (m = A to F) GTCCRm register is a 16-bit readable/writable register.	General PWM timer compare capture register m (m = A to F) GTCCRm register is a 32-bit readable/writable register. Access in 8-bit or 16-bit units to the GTCCRm register is prohibited; it must be accessed in 32-bit units.

Register	Bit	RX64M (GPTA)	RX66N (GPTW)
GTPR	—	General PWM timer period setting register GTPR register is a 16-bit readable/writable register.	General PWM timer period setting register GTPR register is a 32-bit readable/writable counter. Access in 8-bit or 16-bit units to the GTPR register is prohibited; it must be accessed in 32-bit units.
GTPBR	—	General PWM timer period setting buffer register GTPBR register is a 16-bit readable/writable register.	General PWM timer period setting buffer register GTPBR register is a 32-bit readable/writable counter. Access in 8-bit or 16-bit units to the GTPBR register is prohibited; it must be accessed in 32-bit units.
GTPDBR	—	General PWM timer period setting double-buffer register GTPDBR register is a 16-bit readable/writable register.	General PWM timer period setting double-buffer register GTPDBR register is a 32-bit readable/writable counter. Access in 8-bit or 16-bit units to the GTPDBR register is prohibited; it must be accessed in 32-bit units.
GTADTRm	—	A/D converter start request timing register m (m = A or B) GTADTRm register is a 16-bit readable/writable register. Access in 8-bit unit to the GTADTRm register is prohibited; it must be accessed in 16-bit units.	A/D converter start request timing register m (m = A or B) GTADTRm register is a 32-bit readable/writable counter. Access in 8-bit or 16-bit units to the GTADTRm register is prohibited; it must be accessed in 32-bit units.
GTADTBRm	—	A/D converter start request timing buffer register m (m = A or B) GTADTBRm register is a 16-bit readable/writable register. Access in 8-bit unit to the GTADTBRm register is prohibited; it must be accessed in 16-bit units.	A/D converter start request timing buffer register m (m = A or B) GTADTBRm register is a 32-bit readable/writable counter. Access in 8-bit or 16-bit units to the GTADTBRm register is prohibited; it must be accessed in 32-bit units.

Register	Bit	RX64M (GPTA)	RX66N (GPTW)
GTADTDBRm	—	A/D converter start request timing double-buffer register m (m = A or B) GTADTDBRm register is a 16-bit readable/writable register. Access in 8-bit unit to the GTADTDBRm register is prohibited; it must be accessed in 16-bit units.	A/D converter start request timing double-buffer register m (m = A or B) GTADTDBRm register is a 32-bit readable/writable counter. Access in 8-bit or 16-bit units to the GTADTDBRm register is prohibited; it must be accessed in 32-bit units.
GTONCR	—	General PWM timer output negate control register	—
GTDTCR	—	General PWM timer dead time control register GTDTCR register is a 16-bit register.	General PWM timer dead time control register GTDTCR register is a 32-bit register.
GTDVm	—	General PWM timer dead time value register m (m = U or D) GTDVm register is a 16-bit readable/writable register. Access in 8-bit unit to the GTDVm register is prohibited; it must be accessed in 16-bit units.	General PWM timer dead time value register m (m = U or D) GTDVm register is a 32-bit readable/writable counter. Access in 8-bit or 16-bit units to the GTDVm register is prohibited; it must be accessed in 32-bit units.
GTDBm	—	General PWM timer dead time value buffer register m (m = U or D) GTDBm register is a 16-bit readable/writable register.	General PWM timer dead time value buffer register m (m = U or D) GTDBm register is a 32-bit readable/writable counter. Access in 8-bit or 16-bit units to the GTDBm register is prohibited; it must be accessed in 32-bit units.
GTSOS	—	General PWM timer output protection function status register GTSOS register is a 16-bit register.	General PWM timer output protection function status register GTSOS register is a 32-bit register.
GTSOTR	—	General PWM timer output protection function temporary release register GTSOTR register is a 16-bit register.	General PWM timer output protection function temporary release register GTSOTR register is a 32-bit register.
GTSTP	—	—	General PWM timer software stop register
GTCLR	—	—	General PWM timer software clear register
GTSSR	—	—	General PWM timer start source select register

Register	Bit	RX64M (GPTA)	RX66N (GPTW)
GTPSR	—	—	General PWM timer stop source select register
GTCSR	—	—	General PWM timer clear source select register
GTUPSR	—	—	General PWM timer count-up source select register
GTDNSR	—	—	General PWM timer count-down source select register
GTICASR	—	—	General PWM timer input capture source select register A
GTICBSR	—	—	General PWM timer input capture source select register B
GTUDDTYC	—	—	General PWM timer count direction and duty setting register
GTADSMR	—	—	General PWM timer A/D converter start request signal monitoring register
GTEITC	—	—	General PWM timer extended interrupt skipping counter control register
GTEITLI1	—	—	General PWM timer extended interrupt skipping setting register 1
GTEITLI2	—	—	General PWM timer extended interrupt skipping setting register 2
GTEITLB	—	—	General PWM timer extended buffer transfer skipping setting register
GTSECSR	—	—	General PWM timer operation enable bit simultaneous control channel select register
GTSECR	—	—	General PWM timer operation enable bit simultaneous control register

2.18 Ethernet Controller

Table 2.35 is a comparative overview of the Ethernet controllers.

Table 2.35 Comparative Overview of Ethernet Controllers

Item	RX64M (ETHERC)	RX66N (ETHERC)
Number of channels	2 channels	1 channel
Protocol	Flow control compliant with IEEE 802.3x	Flow control compliant with IEEE 802.3x
Data transmission/ reception	Ability to transmit and receive frames compliant with Ethernet/IEEE 802.3 standard	Ability to transmit and receive frames compliant with Ethernet/IEEE 802.3 standard
Communication speed	Support for 10 Mbps and 100 Mbps	Support for 10 Mbps and 100 Mbps
Communication modes	Support for full-duplex and half-duplex modes	Support for full-duplex and half-duplex modes
Interfaces	Support for Media Independent Interface (MII) and Reduced Media Independent Interface (RMII) in compliance with IEEE 802.3u standard	Support for Media Independent Interface (MII) and Reduced Media Independent Interface (RMII) in compliance with IEEE 802.3u standard
Functions	Magic Packet™*1 detection and Wake on LAN (WOL) signal output	Magic Packet™*1 detection and Wake on LAN (WOL) signal output

Note: 1. Magic Packet is a trademark of Advanced Micro Devices, Inc.

2.19 DMA Controller for the Ethernet Controller

Table 2.36 is a comparative overview of the DMA controller for the Ethernet controllers, and Table 2.37 is a comparison of DMA controller for the Ethernet controller registers.

Table 2.36 Comparative Overview of DMA Controller for the Ethernet Controllers

Item	RX64M (EDMACa)	RX66N (EDMACa)
Number of channels	3 channels	1 channel
Data transmission/ reception	• Control or data transmission and reception using descriptors • Support for single-buffer frame transmission and reception (1 buffer per frame) and multi-buffer frame transmission and reception (multiple buffers per frame)	• Control or data transmission and reception using descriptors • Support for single-buffer frame transmission and reception (1 buffer per frame) and multi-buffer frame transmission and reception (multiple buffers per frame)
Functions	• Block transfer (32-byte units) to minimize system bus occupation time • Write-back of transmit/receive frame state to descriptors • Insertion of padding in receive data	• Block transfer (32-byte units) to minimize system bus occupation time • Write-back of transmit/receive frame state to descriptors • Insertion of padding in receive data
Low power consumption function	Ability to transition to module-stop state to reduce power consumption	Ability to transition to module-stop state to reduce power consumption

Table 2.37 Comparison of DMA Controller for the Ethernet Controller Registers

Register	Bit	RX64M (EDMACa)	RX66N (EDMACa)
EDMR	SWR	Software reset bit Writing 1 to this bit resets the EDMAC and ETHERC on the corresponding channel. In the case of PTPEDMAC, the ETHERC is not reset. Note that the TDLAR, RDLAR, RMFCR, TFUCR, and RFOCR registers are not reset by this bit. This bit are read as 0.	Software reset bit Writing 1 to this bit resets the EDMAC and ETHERC. Note that the TDLAR, RDLAR, RMFCR, TFUCR, and RFOCR registers are not reset by this bit. This bit are read as 0.
FDR	RFD[4:0]	Receive FIFO depth bits b4 b0 0 1 1 1 1: 4,096 bytes Settings other than the above are prohibited.	Receive FIFO depth bits b4 b0 0 0 1 1 1: 1,968 bytes Settings other than the above are prohibited.

Register	Bit	RX64M (EDMACa)	RX66N (EDMACa)
FCFTR	RFDO[2:0]	Receive FIFO data PAUSE output threshold bits b2 b0 0 0 0: When 224 (256 − 32) bytes of data is stored in the receive FIFO. 0 0 1: When 480 (512 − 32) bytes of data is stored in the receive FIFO. : 1 1 0: When 1,760 (1,792 − 32) bytes of data is stored in the receive FIFO. 1 1 1: When 2,016 (2,048 − 32) bytes of data is stored in the receive FIFO.	Receive FIFO data PAUSE output threshold bits b2 b0 0 0 0: When 224 (256 − 32) bytes of data is stored in the receive FIFO. 0 0 1: When 480 (512 − 32) bytes of data is stored in the receive FIFO. : 1 1 0: When 1,760 (1,792 − 32) bytes of data is stored in the receive FIFO. 1 1 1: When 1,952 (2,048 − 96) bytes of data is stored in the receive FIFO.

2.20 USB 2.0 FS Host/Function Module

Table 2.38 is a comparison of USB 2.0 FS Host/Function module registers.

Table 2.38 Comparison of USB 2.0 FS Host/Function Module Registers

Register	Bit	RX64M (USBb)	RX66N (USBb)
PIPEnTRN	TRNCNT [15:0] (RX64M) — (RX66N)	PIPEn transaction counter register (n = 1 to 5)	PIPEn transaction counter register (n = 1 to 5)
PHYSLEW	SLEWR00	Driver cross point adjustment 00 bit 0: When the Host controller is selected 1: When the Function controller is selected	Driver cross point adjustment 00 bit Set this bit to 1.
	SLEWR01	Driver cross point adjustment 01 bit 0: When the Function controller is selected 1: When the Host controller is selected	Driver cross point adjustment 01 bit Set this bit to 0.
	SLEWF01	Driver cross point adjustment 01 bit 0: When the Function controller is selected 1: When the Host controller is selected	Driver cross point adjustment 01 bit Set this bit to 0.

2.21 Serial Communications Interface

Table 2.39 is a comparative overview of the serial communications interfaces, Table 2.40 is a comparison of SCI channel specifications, and Table 2.41 is a comparison of serial communications interface registers.

Table 2.39 Comparative Overview of Serial Communications Interfaces

Item		RX64M (SCIg, SCIh)	RX66N (SCIj, SCIi, SCIh)
Number of channels		• SCIg: 8 channels • SCIh: 1 channel	• SCIj: 3 channels • SCIi: 1 channel • SCIh: 1 channel
Serial communications modes		• Asynchronous operation • Clock synchronous operation • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous operation • Clock synchronous operation • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		Bit rate specifiable using on-chip baud rate generator.	Bit rate specifiable using on-chip baud rate generator.
Full-duplex communication		• Transmitter: Support for continuous transmission using double-buffering • Receiver: Support for continuous reception using double-buffering	• Transmitter: Support for continuous transmission using double-buffering • Receiver: Support for continuous reception using double-buffering
Data transfer		Selectable between LSB-first and MSB-first*1	Selectable between LSB-first and MSB-first*1
Interrupt sources		• Transmit end, transmit data empty, receive data full, receive error • Completion of generation of a start condition, restart condition, or stop condition (simple I²C mode)	• Transmit end, transmit data empty, receive data full, receive error, receive data ready (SCI7 to SCI12), and data match (SCI0 to SCI12) • Completion of generation of a start condition, restart condition, or stop condition (simple I²C mode)
Low power consumption function		Ability to set individual channels to the module stop state	Ability to set individual channels to the module stop state
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even, odd, or none	Even, odd, or none
	Receive error detection function	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	Ability to use CTSn# and RTSn# pins for transmission and reception control	Ability to use CTSn# and RTSn# pins for transmission and reception control
	Transmit/receive FIFO	—	Ability to use 16-stage FIFOs for transmission and reception (SCI7 to SCI11)
	Data match detection	—	Ability to compare receive data and comparison data, and generates an interrupt when they match (SCI0 to SCI11)

Item		RX64M (SCIg, SCIh)	RX66N (SCIj, SCIi, SCIh)
Asynchronous mode	Start-bit detection	Selectable between low level and falling edge	Selectable between low level and falling edge
	Break detection	Ability to detect a break by reading the RXDn pin level directly when a framing error occurs	When a framing error occurs, a break can be detected by reading the RXDn pin level directly or reading the SPTR.RXDMON flag (SCI0 to SCI11).
	Clock source	• Selectable between internal or external clock • Ability to input transfer rate clock from TMR (SCI5, SCI6, and SCI12)	• Selectable between internal or external clock • Ability to input transfer rate clock from TMR (SCI5, SCI6, and SCI12)
	Double-speed mode	Ability to select baud rate generator double-speed mode	Ability to select baud rate generator double-speed mode
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation function	The input signal paths from the RXDn pins incorporate digital noise filters.	The input signal paths from the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	Ability to use CTSn# and RTSn# pins for transmission and reception control	Ability to use CTSn# and RTSn# pins for transmission and reception control
	Transmit/receive FIFO	—	Ability to use 16-stage FIFOs for transmission and reception (SCI7 to SCI11)
Smart card interface mode	Error processing	• Automatic transmission of an error signal at detection of a parity error during reception • Automatic re-transmission of data at reception of an error signal during transmission	• Automatic transmission of an error signal at detection of a parity error during reception • Automatic re-transmission of data at reception of an error signal during transmission
	Data type	Support for direct convention and inverse convention	Support for direct convention and inverse convention
Simple I^2C mode	Communication format	I^2C bus format	I^2C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer speed	Support for fast mode	Support for fast mode
	Noise cancellation	• The SSCLn and SSDAn input signal paths incorporate digital noise filters. • The noise cancellation interval is adjustable.	• The SSCLn and SSDAn input signal paths incorporate digital noise filters. • The noise cancellation interval is adjustable.

Item		RX64M (SCIg, SCIh)	RX66N (SCIj, SCIi, SCIh)
Simple SPI mode	Data length	8 bits	8 bits
	Error detection	Overrun error	Overrun error
	SS input pin function	Ability to place output pins in high-impedance state by applying a high-level signal to the SSn# pin.	Ability to place output pins in high-impedance state by applying a high-level signal to the SSn# pin.
	Clock settings	Ability to select among four clock phase and clock polarity settings	Ability to select among four clock phase and clock polarity settings
Extended serial mode (supported by SCI12 only)	Start frame transmission	• Ability to output break field low width/output completion interrupt function • Bus collision detection function/detection interrupt function	• Ability to output break field low width/output completion interrupt function • Bus collision detection function/detection interrupt function
	Start frame reception	• Ability to detect break field low width/detection completion interrupt function • Control field 0 and control field 1 data comparison/match interrupt function • Ability to select between two data types for comparison (primary and secondary) in control field 1 • Ability to set priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include control field 0 • Bit rate measurement function	• Ability to detect break field low width/detection completion interrupt function • Control field 0 and control field 1 data comparison/match interrupt function • Ability to select between two data types for comparison (primary and secondary) in control field 1 • Ability to set priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include control field 0 • Bit rate measurement function
	I/O control function	• Ability to select polarity of TXDX12 and RXDX12 signals • Ability to specify digital filter function for RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select sampling timing for data received on RXDX12	• Ability to select polarity of TXDX12 and RXDX12 signals • Ability to specify digital filter function for RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select sampling timing for data received on RXDX12
	Timer function	Usable as reload timer	Usable as reload timer
Bit rate modulation function		Ability to reduce errors by correcting output from the on-chip baud rate generator	Ability to reduce errors by correcting output from the on-chip baud rate generator
Event link function (supported by SCI5 only)		• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output	• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output

Note: 1. Simple I^2C mode can only be used with MSB-first data transfer.

Table 2.40 Comparison of SCI Channel Specifications

Item	RX64M (SCIg, SCIh)	RX66N (SCIj, SCIi, SCIh)
Asynchronous mode	SCI0 to SCI7, SCI12	SCI0 to SCI12
Clock synchronous mode	SCI0 to SCI7, SCI12	SCI0 to SCI12
Smart card interface mode	SCI0 to SCI7, SCI12	SCI0 to SCI12
Simple I^2C mode	SCI0 to SCI7, SCI12	SCI0 to SCI12
Simple SPI mode	SCI0 to SCI7, SCI12	SCI0 to SCI12
FIFO mode	—	SCI7 to SCI11
Data match detection	—	SCI0 to SCI11
Extended serial mode	SCI12	SCI12
TMR clock input	SCI5, SCI6, SCI12	SCI5, SCI6, SCI12
Event link function	SCI5	SCI5
Peripheral module clock	PCLKB: SCI0 to SCI7, SCI12	PCLKB: SCI0 to SCI6, SCI12 PCLKA: SCI7 to SCI11

Table 2.41 Comparison of Serial Communications Interface Registers

Register	Bit	RX64M (SCIg, SCIh)	RX66N (SCIj, SCIi, SCIh)
FRDR	—	—	Receive FIFO data register
FTDR	—	—	Transmit FIFO data register
SSRFIFO	—	—	Serial status register
SEMR	ABCSE	—	Asynchronous mode base clock select extended bit*1
FCR	—	—	FIFO control register
FDR	—	—	FIFO data count register
LSR	—	—	Line status register
CDR	—	—	Comparison data register
DCCR	—	—	Data comparison control register
SPTR	—	—	Serial port register

Note: 1. This bit is reserved on SCI12. It is read as 0. The write value should be 0.

2.22 I²C Bus Interface

Table 2.42 is a comparative overview of the I²C bus interfaces.

Table 2.42 Comparative Overview of I²C Bus Interfaces

Item	RX64M (RIICa)	RX66N (RIICa)
Number of channels	2 channels	3 channels
Communication format	• I²C bus format or SMBus format • Selectable between master mode and slave mode • Automatic securing of set-up times, hold times, and bus-free times to match the specified transfer speed	• I²C bus format or SMBus format • Selectable between master mode and slave mode • Automatic securing of set-up times, hold times, and bus-free times to match the specified transfer speed
Transfer speed	Support for Fast-mode Plus (up to 1 Mbps)	Support for Fast-mode Plus (up to 1 Mbps)
SCL clock	Ability to select duty cycle of SCL clock within range of 4% to 96% during master operation	Ability to select duty cycle of SCL clock within range of 4% to 96% during master operation
Issuing and detecting conditions	Start, restart, and stop conditions are generated automatically. Start conditions (including restart conditions) and stop conditions are detectable.	Start, restart, and stop conditions are generated automatically. Start conditions (including restart conditions) and stop conditions are detectable.
Slave address	• Ability to set up to three different slave addresses • Support for 7- and 10-bit address formats (along with use of both at once) • Ability to detect general call addresses, device ID addresses, and SMBus host addresses	• Ability to set up to three different slave addresses • Support for 7- and 10-bit address formats (along with use of both at once) • Ability to detect general call addresses, device ID addresses, and SMBus host addresses
Acknowledgment	• Automatic loading of acknowledge bit during transmission — Ability to suspend the next data transfer automatically on detection of a not-acknowledge bit • Automatic transmission of acknowledge bit during reception — Support for software control of value of the acknowledge bit according to the received data when a wait between the eighth and ninth clock cycles is selected	• Automatic loading of acknowledge bit during transmission — Ability to suspend the next data transfer automatically on detection of a not-acknowledge bit • Automatic transmission of acknowledge bit during reception — Support for software control of value of the acknowledge bit according to the received data when a wait between the eighth and ninth clock cycles is selected
Wait function	Ability to implement a wait by holding the SCL clock signal low • Wait between the eighth and ninth clock cycles • Wait between the ninth and first clock cycles	Ability to implement a wait by holding the SCL clock signal low • Wait between the eighth and ninth clock cycles • Wait between the ninth and first clock cycles
SDA output delay function	Ability to delay output timing of transmitted data, including the acknowledge bit	Ability to delay output timing of transmitted data, including the acknowledge bit

Item	RX64M (RIICa)	RX66N (RIICa)
Arbitration	• Multi-master support — Ability to synchronize operation with the clock of another master in cases of conflict with the SCL clock — Ability to detect loss of arbitration in case of an SDA line signal state mismatch when a start condition issuance conflict occurs — Ability to detect loss of arbitration when a start transmit data mismatch occurs during master operation • Ability to detect loss of arbitration due to start condition issuance when the bus is busy (to prevent issuance of duplicate start conditions) • Ability to detect loss of arbitration in case of an SDA line signal state mismatch when a not-acknowledge bit is sent • Ability to detect loss of arbitration when a data mismatch occurs during slave transmission	• Multi-master support — Ability to synchronize operation with the clock of another master in cases of conflict with the SCL clock — Ability to detect loss of arbitration in case of an SDA line signal state mismatch when a start condition issuance conflict occurs — Ability to detect loss of arbitration when a start transmit data mismatch occurs during master operation • Ability to detect loss of arbitration due to start condition issuance when the bus is busy (to prevent issuance of duplicate start conditions) • Ability to detect loss of arbitration in case of an SDA line signal state mismatch when a not-acknowledge bit is sent • Ability to detect loss of arbitration when a data mismatch occurs during slave transmission
Timeout detection function	Ability to detect extended stopping of the SCL clock using built-in time-out function	Ability to detect extended stopping of the SCL clock using built-in time-out function
Noise cancellation	Built-in digital noise filters for SCL and SDA signals, and ability to adjust the noise cancellation width by software.	Built-in digital noise filters for SCL and SDA signals, and ability to adjust the noise cancellation width by software.
Interrupt sources	Four sources • Communication error/event occurrence, arbitration detection, NACK detection, timeout detection, start condition (including restart condition) detection, or stop condition detection • Receive data full (including match with slave address) • Transmit data empty (including match with slave address) • Transmission complete	Four sources • Communication error/event occurrence, arbitration detection, NACK detection, timeout detection, start condition (including restart condition) detection, or stop condition detection • Receive data full (including match with slave address) • Transmit data empty (including match with slave address) • Transmission complete
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state
RIIC operating modes	Four modes: Master transmit mode, master receive mode, slave transmit mode, and slave receive mode	Four modes: Master transmit mode, master receive mode, slave transmit mode, and slave receive mode

Item	RX64M (RIICa)	RX66N (RIICa)
Event link function (output)	Four sources (RIIC0) • Communication error/event occurrence, arbitration detection, NACK detection, timeout detection, start condition (including restart condition) detection, or stop condition detection • Receive data full (including match with slave address) • Transmit data empty (including match with slave address) • Transmission complete	Four sources (RIIC0) • Communication error/event occurrence, arbitration detection, NACK detection, timeout detection, start condition (including restart condition) detection, or stop condition detection • Receive data full (including match with slave address) • Transmit data empty (including match with slave address) • Transmission complete

2.23 Serial Peripheral Interface

Table 2.43 is a comparative overview of the serial peripheral interfaces, and Table 2.44 is a comparison of serial peripheral interface registers.

Table 2.43 Comparative Overview of Serial Peripheral Interfaces

Item	RX64M (RSPIa)	RX66N (RSPIc)
Number of channels	1 channel	3 channels
RSPI transfer functions	• Ability to use MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals to implement serial communication through SPI operation (four-wire method) or clock synchronous operation (three-wire method). • Ability to perform transmit-only operation • Communication mode: Selectable between full-duplex and transmit-only • Ability to switch the polarity of RSPCK • Ability to switch the phase of RSPCK	• Ability to use MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals to implement serial communication through SPI operation (four-wire method) or clock synchronous operation (three-wire method). • Ability to perform transmit-only operation • Communication mode: Selectable between full-duplex and transmit-only • Ability to switch the polarity of RSPCK • Ability to switch the phase of RSPCK
Data format	• Selectable between MSB-first and LSB-first • Ability to select transfer bit length among 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, and 32 bits • 128-bit transmit/receive buffers • Ability to transfer up to four frames in each round of transmission/reception (with up to 32 bits per frame)	• Selectable between MSB-first and LSB-first • Ability to select transfer bit length among 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, and 32 bits • 128-bit transmit/receive buffers • Ability to transfer up to four frames in each round of transmission/reception (with up to 32 bits per frame) • Ability to perform byte swapping of transmit and receive data
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (division ratio: 2 to 4,096). • In slave mode, PCLK divided by a minimum of 8 can be input as RSPCK (RSPCK maximum frequency: PCLK divided by 8). — Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (division ratio: 2 to 4,096). • In slave mode, PCLK divided by a minimum of 4 can be input as RSPCK (RSPCK maximum frequency: PCLK divided by 4). — Width at high level: 2 cycles of PCLK; width at low level: 2 cycles of PCLK
Buffer configuration	• Double buffer configuration for both the transmit and receive buffers • 128 bits for the transmit/receive buffers	• Double buffer configuration for both the transmit and receive buffers • 128 bits for the transmit/receive buffers
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection

Item	RX64M (RSPIa)	RX66N (RSPIc)
SSL control function	• Four SSL pins (SSLA0 to SSLA3) per channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode, the SSLA0 pin is input, and SSLA1 to SSLA3 pins are either output or unused. • In slave mode, the SSLA0 pin is input, and SSLA1 to SSLA3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Controllable wait until next-access SSL output assertion (next-access delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Function for changing SSL polarity	• Four SSL pins (SSLx0 to SSLx3) per channel • In single-master mode, SSLx0 to SSLx3 pins are output. • In multi-master mode, the SSLx0 pin is input, and SSLx1 to SSLx3 pins are either output or unused. • In slave mode, the SSLx0 pin is input, and SSLx1 to SSLx3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Controllable wait until next-access SSL output assertion (next-access delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Function for changing SSL polarity
Control during master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following items can be set: — SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value at SSL negation can be specified. • RSPCK auto-stop function	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following items can be set: — SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value at SSL negation can be specified. • RSPCK auto-stop function
Interrupt sources	Interrupt sources • Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, or parity error) • RSPI idle interrupt (RSPI idle)	Interrupt sources • Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, underrun, or parity error) • RSPI idle interrupt (RSPI idle)
Event link function (output)	The following events can be output to the event link controller (RSPI0): • Receive buffer full event signal • Transmit buffer empty event signal • Mode fault, overrun, or parity error event signal • RSPI idle event signal • Transmission-completed event signal	The following events can be output to the event link controller (RSPI0): • Receive buffer full event signal • Transmit buffer empty event signal • Mode fault, overrun, underrun, or parity error event signal • RSPI idle event signal • Transmission-completed event signal

Item	RX64M (RSPIa)	RX66N (RSPIc)
Other functions	• Function for switching between CMOS and open-drain output • Function for initializing the RSPI • Loopback mode	• Function for switching between CMOS and open-drain output • Function for initializing the RSPI • Loopback mode
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.44 Comparison of Serial Peripheral Interface Registers

Register	Bit	RX64M (RSPIa)	RX66N (RSPIc)
SPSR	MODF	Mode fault error flag 0: No mode fault error occurred. 1: A mode fault error occurred.	Mode fault error flag 0: No mode fault error or underrun error occurred. 1: A mode fault error or underrun error occurred.
	UDRF	—	Underrun error flag
SPDR	—	RSPI data register Available access sizes: • Longword (SPDCR.SPLW = 1) • Word (SPDCR.SPLW = 0)	RSPI data register Available access sizes: • Longword (SPDCR.SPLW = 1, SPDCR.SPBYT = 0) • Word (SPDCR.SPLW = 0, SPDCR.SPBYT = 0) • Byte (SPDCR.SPBYT = 1)
SPDCR	SPBYT	—	RSPI byte access specification bit
SPDCR2	—	—	RSPI data control register 2

2.24 CRC Calculator

Table 2.45 is a comparative overview of the CRC calculators, and Table 2.46 is a comparison of CRC calculator registers.

Table 2.45 Comparative Overview of CRC Calculators

Item	RX64M (CRC)	RX66N (CRCA)	
Data size	8 bits	8 bits	32 bits
Data for CRC calculation	CRC codes are generated 8n-bit data units (where n is a whole number).	CRC codes are generated 8n-bit data units (where n is a whole number).	CRC codes are generated 32n-bit data units (where n is a whole number).
CRC processing method	8-bit parallel execution	8-bit parallel execution	32-bit parallel execution
CRC generation polynomial	Ability to select among three generation polynomials • 8-bit CRC $X^8 + X^2 + X + 1$ • 16-bit CRC $X^{16} + X^{15} + X^2 + 1$, $X^{16} + X^{12} + X^5 + 1$	Ability to select among three generation polynomials • 8-bit CRC $X^8 + X^2 + X + 1$ • 16-bit CRC $X^{16} + X^{15} + X^2 + 1$, $X^{16} + X^{12} + X^5 + 1$	Ability to select among two generation polynomials • 32-bit CRC $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$, $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$
CRC calculation switching	The bit order of the CRC calculation result can be switched to accommodate LSB-first or MSB-first for communication.	The bit order of the CRC calculation result can be switched to accommodate LSB-first or MSB-first for communication.	
Low power consumption function	Ability to specify transition to module stop state	Ability to transition to module stop state	

Table 2.46 Comparison of CRC Calculator Registers

Register	Bit	RX64M (CRC)	RX66N (CRCA)
CRCCR	GPS[1:0] (RX64M) GPS[2:0] (RX66N)	CRC generating polynomial switching bits (b1, b0) b1 b0 0 0: No calculation 0 1: 8-bit CRC ($X^8 + X^2 + X + 1$) 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$) 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$)	CRC generating polynomial switching bits (b2 to b0) b2 b0 0 0 0: No calculation 0 0 1: 8-bit CRC ($X^8 + X^2 + X + 1$) 0 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$) 0 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$) 1 0 0: 32-bit CRC ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1: 32-bit CRC ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) 1 1 0: No calculation 1 1 1: No calculation
	LMS	CRC calculation switching bit (b2)	CRC calculation switching bit (b6)
CRCDIR	—	CRC data input register Available access sizes: • Byte	CRC data input register Available access sizes: • Longword (for 32-bit CRC generation) • Byte (for 16-bit or 8-bit CRC generation)
CRCDOR	—	CRC data output register Available access sizes: • Word When generating 8-bit CRCs, the lower-order byte (bits b7 to b0) is used.	CRC data output register Available access sizes: • Longword (for 32-bit CRC generation) • Word (for 16-bit CRC generation) • Byte (for 8-bit CRC generation)

2.25 Serial Sound Interface (SSI)/Enhanced Serial Sound Interface (SSIE)

Table 2.47 is a comparative overview of the serial sound interface and enhanced serial sound interface, and Table 2.48 is a comparison of serial sound interface and enhanced serial sound interface registers.

Table 2.47 Comparative Overview of Serial Sound Interface and Enhanced Serial Sound Interface

Item		RX64M (SSI)	RX66N (SSIE)
Number of channels		2 channels (SSI0 and SSI1)	2 channels (SSIE0 and SSIE1)
Operating mode		Non-compressed mode	Non-compressed mode
Transfer modes		• Master/slave • Transmission, reception, or transception (transception on SSI0 only)	• Master/slave • Transmission, reception, or transception (transception on SSIE0 only)
Data formats		• I^2S format supported. • MSB-first supported. Selectable between left-justified and right-justified formats.	• I^2S format • Left-justified format • Right-justified format • Monaural format • TDM format
Serial data		• Fixed at MSB first • System word length: 8, 16, 24, or 32 bits • Data word length: 8, 16, 18, 20, 22, or 24 bits • Polarity of the padding bits is selectable. • Mute function	• Fixed at MSB first • System word length: Selectable among 8, 16, 24, 32, 48, 64, 128, or 256 bits • Data word length: Selectable among 8, 16, 18, 20, 22, 24, or 32 bits • Polarity of the padding bits is selectable. • Mute function
Bit clock (SSISCK: RX64M) (BCK: RX66N)	In master mode	• Clock source: AUDIO_MCLK • Frequency: Selectable among: 1/1, 1/2, 1/4, 1/6, 1/8, 1/12, 1/16, 1/24, 1/32, 1/48, 1/64, 1/96, or 1/128 of the AUDIO_MCLK frequency	• Clock source: AUDIO_CLK • Frequency: Selectable among: 1/1, 1/2, 1/4, 1/6, 1/8, 1/12, 1/16, 1/24, 1/32, 1/48, 1/64, 1/96, or 1/128 of the AUDIO_CLK frequency • Ability to select supply or stop while data transfer is halted
	In master and slave modes	Ability to select polarity (rising or falling edge)	Ability to select polarity (rising or falling edge)
Word select (SSIWS: RX64M) LR clock (LRCK: RX66N)		• Ability to select polarity (low or high) • Ability to select supply or stop while data transfer is halted	• Ability to select polarity (low or high) • Ability to select supply or stop while data transfer is halted
FIFO	Capacity	• Transmit FIFO: 4 bytes × 8 stages • Receive FIFO: 4 bytes × 8 stages	• Transmit FIFO: 4 bytes × 32 stages • Receive FIFO: 4 bytes × 32 stages
	Data alignment	Ability to select alignment of data (left-justified or right-justified) in the FIFO	Ability to select alignment of data (left-justified or right-justified) in the FIFO
Interrupts		• Data transfer error/idle state • Receive data full • Transmit data empty	• Data transfer error/idle state • Receive data full • Transmit data empty

Item	RX64M (SSI)	RX66N (SSIE)
Low power consumption function	• Ability to specify that modules enter the module stop state	• Module stop function • Master clock (MCK) supply stop function

Table 2.48 Comparison of Serial Sound Interface and Enhanced Serial Sound Interface Registers

Register	Bit	RX64M (SSI)	RX66N (SSIE)
SSICR	PDTA	Parallel data allocation bit (When data word length is 8 or 16 bits) 0: The lower bits of parallel data (SSIFTDR, SSIFRDR) are transferred prior to the upper bits. 1: The upper bits of parallel data (SSIFTDR, SSIFRDR) are transferred prior to the lower bits. (When data word length is 18, 20, 22, or 24 bits) 0: Parallel data (SSIFTDR, SSIFRDR) is left-justified. 1: Parallel data (SSIFTDR, SSIFRDR) is right-justified.	Data alignment select bit Sets the data alignment of the SSIFTDR and SSIFRDR registers. 0: Data is left-justified. 1: Data is right-justified.
	SWSP (RX64M) LRCKP (RX66N)	Word select polarity bit	LR clock polarity select bit
	SCKP (RX64M) BCKP (RX66N)	Serial bit clock polarity bit	Bit clock polarity select bit
	SWSD	Word select direction bit	—
	SCKD	Serial bit clock direction bit	—
	MST	—	Master mode bit
	SWL[2:0]	System word length bits Set the system word length to (serial bit clock frequency / 2) fs. b18 b16 0 0 0: 8 bits (serial bit clock frequency = 16 fs) 0 0 1: 16 bits (serial bit clock frequency = 32 fs) 0 1 0: 24 bits (serial bit clock frequency = 48 fs) 0 1 1: 32 bits (serial bit clock frequency = 64 fs) Settings other than the above are prohibited.	System word length select bits b18 b16 0 0 0: 8 bits 0 0 1: 16 bits 0 1 0: 24 bits 0 1 1: 32 bits 1 0 0: 48 bits 1 0 1: 64 bits 1 1 0: 128 bits 1 1 1: 256 bits

Register	Bit	RX64M (SSI)	RX66N (SSIE)
SSICR	DWL[2:0]	Data word length bits b21 b19 0 0 0: 8 bits 0 0 1: 16 bits 0 1 0: 18 bits 0 1 1: 20 bits 1 0 0: 22 bits 1 0 1: 24 bits Settings other than the above are prohibited.	Data word length select bits b21 b19 0 0 0: 8 bits 0 0 1: 16 bits 0 1 0: 18 bits 0 1 1: 20 bits 1 0 0: 22 bits 1 0 1: 24 bits 1 1 0: 32 bits 1 1 1: Setting prohibited.
	CHNL[1:0]	Channels bits	—
	FRM[1:0]	—	Frame word length select bits
	CKS	Audio clock select bit	—
SSISR	IDST	Idle status flag	—
	RSWNO	Receive system word number flag	—
	RCHNO[1:0]	Receive channel number flag	—
	TSWNO	Transmit system word number flag	—
	TCHNO[1:0]	Transmit channel number flag	—
SSIFCR	RTRG[1:0]	Receive FIFO threshold setting bits	—
	TTRG[1:0]	Transmit FIFO threshold setting bits	—
	BSW	—	Byte swap bit
SSIFSR	RDC[3:0] (RX64M) RDC[5:0] (RX66N)	Receive data indicate flag (b11 to b8)	Receive FIFO data count bits (b13 to b8)
	TDC[3:0] (RX64M) TDC[5:0] (RX66N)	Transmit data indicate flag (b27 to b24)	Transmit FIFO data count bits (b29 to b24)
SSIFTDR	—	Transmit FIFO data register Transmit data must be written to this register in 64-bit (two stages of FIFO) units regardless of the data word length setting.	Transmit FIFO data register The access size differs according to the data word length. For details, refer to RX66N Group User's Manual: Hardware.
		The value after a reset differs.	
SSIFRDR	—	Receive FIFO data register	Receive FIFO data register The access size differs according to the data word length. For details, refer to RX66N Group User's Manual: Hardware.
		The value after a reset differs.	
SSITDMR	—	TDM mode register	—
SSIOFR	—	—	Audio format register
SSISCR	—	—	FIFO status control register

2.26 SD Host Interface

Table 2.49 is a comparative overview of the SD host interfaces, and Table 2.50 is a comparison of SD host interface registers.

Table 2.49 Comparative Overview of the SD Host Interfaces

Item	RX64M (SDHI)	RX66N (SDHI)
SD bus interface	• Compatible with SD memory cards and SDIO cards*1. • Transfer bus mode selectable between wide bus (4-bit) mode and default bus (1-bit) modes. • Compatible with SD, SDHC, and SDXC SD memory card formats.	• Compatible with SD memory cards and SDIO cards*1. • Transfer bus mode selectable between wide bus (4-bit) mode and default bus (1-bit) modes. • Compatible with SD, SDHC, and SDXC SD memory card formats.
Transfer modes	Selectable between high-speed and default speed modes.	Selectable between high-speed and default speed modes.
SDHI clock	SDHI clock generated by dividing peripheral module clock B (PCLKB) by n (n = 2, 4, 8, 16, 32, 64, 128, 256, or 512).	SDHI clock generated by dividing peripheral module clock B (PCLKB) by n (n = 1, 2, 4, 8, 16, 32, 64, 128, 256, or 512).
Error checking functions	• CRC7 (command/response) • CRC16 (transfer data)	• CRC7 (command/response) • CRC16 (transfer data)
Interrupt sources	Four sources: • Card access interrupt (CACI) • SDIO access interrupt (SDACI) • Card detection interrupt (CDETI) • SD buffer access interrupt (SBFAI)	Four sources: • Card access interrupt (CACI) • SDIO access interrupt (SDACI) • Card detection interrupt (CDETI) • SD buffer access interrupt (SBFAI)
DMA transfer request sources	• DMAC and DTC can be activated by the SD buffer access (SBFAI) interrupt • SD buffer is read and write accessible by DMAC and DTC.	• DMAC and DTC can be activated by the SD buffer access (SBFAI) interrupt • SD buffer is read and write accessible by DMAC and DTC.
Other functions	• Card detection function • Write protection function	• Card detection function • Write protection function

Note: 1. Not compatible with SPI bus interface, embedded SDIO shared bus, 8-bit SD bus, or SDIO suspend/resume functions.

Table 2.50 Comparison of SD Host Interface Registers

Register	Bit	RX64M (SDHI)	RX66N (SDHI)
SDCLKCR	CLKSEL[7:0]	SDHI clock frequency select bits b7 b0 0 0 0 0 0 0 0 0: PCLKB divided by 2 0 0 0 0 0 0 0 1: PCLKB divided by 4 0 0 0 0 0 0 1 0: PCLKB divided by 8 0 0 0 0 0 1 0 0: PCLKB divided by 16 0 0 0 0 1 0 0 0: PCLKB divided by 32 0 0 0 1 0 0 0 0: PCLKB divided by 64 0 0 1 0 0 0 0 0: PCLKB divided by 128 0 1 0 0 0 0 0 0: PCLKB divided by 256 1 0 0 0 0 0 0 0: PCLKB divided by 512 Settings other than the above are prohibited.	SDHI clock frequency select bits b7 b0 0 0 0 0 0 0 0 0: PCLKB divided by 2 0 0 0 0 0 0 0 1: PCLKB divided by 4 0 0 0 0 0 0 1 0: PCLKB divided by 8 0 0 0 0 0 1 0 0: PCLKB divided by 16 0 0 0 0 1 0 0 0: PCLKB divided by 32 0 0 0 1 0 0 0 0: PCLKB divided by 64 0 0 1 0 0 0 0 0: PCLKB divided by 128 0 1 0 0 0 0 0 0: PCLKB divided by 256 1 0 0 0 0 0 0 0: PCLKB divided by 512 1 1 1 1 1 1 1 1: PCLKB*1 Settings other than the above are prohibited.

Note: 1. When setting the CLKSEL[7:0] bits to 11111111b, or when changing their setting from 11111111b to another value, follow the steps below:
(1) Clear the CLKEN bit to 0. Do not change the value of the other bits at this time.
(2) Change the value of the CLKSEL[7:0] bits. Do not change the value of the other bits at this time.
(3) Set the CLKEN bit to 1. Do not change the value of the other bits at this time.

2.27 Boundary Scan

Table 2.51 is a comparative overview of boundary scan, and Table 2.52 is a comparison of boundary scan registers.

Table 2.51 Comparative Overview of Boundary Scan

Item	RX64M	RX66N
Boundary scan enable/disable	Boundary scan is enabled when the RES# pin and the BSCANP pin are driven high and the EMLE pin is driven low.	Boundary scan is enabled when the RES# pin and the BSCANP pin are driven high and the EMLE pin is driven low.
Dedicated boundary scan pins	Pins exclusively for use by the JTAG when the boundary scan function is enabled (TDO, TCK, TDI, TMS, and TRST#): 177-pin TFLGA/176-pin LFBGA: PF0, PF1, PF2, PF3, and PF4 145-pin TFLGA: P26, P27, P30, P31, and P34	Pins exclusively for use by the JTAG when the boundary scan function is enabled (TDO, TCK, TDI, TMS, and TRST#): 224-pin LFBGA/176-pin LFBGA: PF0, PF1, PF2, PF3, and PF4 145-pin TFLGA: P26, P27, P30, P31, and P34
Six test modes	• BYPASS mode • EXTEST mode • SAMPLE/PRELOAD mode • CLAMP mode • HIGHZ mode • IDCODE mode	• BYPASS mode • EXTEST mode • SAMPLE/PRELOAD mode • CLAMP mode • HIGHZ mode • IDCODE mode

Table 2.52 Comparison of Boundary Scan Registers

Register	Bit	RX64M	RX66N
JTIDR	—	ID code register	ID code register
		The value after a reset differs.	

2.28 12-Bit A/D Converter

Table 2.53 is a comparative overview of the 12-bit A/D converters, and Table 2.54 is a comparison of 12-bit A/D converter registers.

Table 2.53 Comparative Overview of 12-Bit A/D Converters

Item	RX64M (S12ADC)	RX66N (S12ADFa)
Number of units	2 units (S12AD, S12AD1)	2 units (S12AD, S12AD1)
Input channels	Unit 0: 8 channels Unit 1: 21 channels + one extended	S12AD: 8 channels, S12AD1: 21 channels + one extended
Extended analog function	Temperature sensor output, internal reference voltage	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	0.48 µs per channel (12-bit conversion mode) 0.45µs per channel (10-bit conversion mode) 0.42µs per channel (8-bit conversion mode) (when A/D conversion clock ADCLK = 60 MHz)	0.48 µs per channel (12-bit conversion mode) 0.45 µs per channel (10-bit conversion mode) 0.42 µs per channel (8-bit conversion mode) (when A/D conversion clock ADCLK = 60 MHz)
A/D conversion clock	• The available peripheral module clock (PCLKB) and A/D conversion clock (ADCLK) frequency division ratio settings are as follows: PCLKB:ADCLK frequency division ratio = 1:1, 1:2, 1:4, or 1:8 • ADCLK is set by the clock generation circuit (CPG).	• The available peripheral module clock (PCLK) and A/D conversion clock (ADCLK) frequency ratio settings are as follows: PCLK:ADCLK frequency ratio = 1:1, 2:1, 4:1, or 8:1 • ADCLK is set by the clock generation circuit.
Data registers	• 29 registers (unit 0: 8, unit 1: 21) for analog input, one for A/D-converted data duplication in double trigger mode per unit, and two for A/D-converted data duplication during extended operation in double trigger mode per unit. • One register for temperature sensor (unit 1 only) • One register for internal reference voltage (unit 1 only) • A/D conversion results are stored in 12-bit A/D data registers. • 8-, 10-, and 12-bit accuracy output of A/D conversion results • In A/D-converted value addition mode, the value obtained by adding up A/D-converted results is stored as (conversion accuracy bit count + 2 bits) in the A/D data registers.	• 29 registers (S12AD: 8, S12AD1: 21) for analog input, one for A/D-converted data duplication in double trigger mode per unit, and two for A/D-converted data duplication during extended operation in double trigger mode per unit. • One register for temperature sensor (S12AD1) • One register for internal reference voltage (S12AD1) • One register for self-diagnosis per unit • A/D conversion results are stored in 12-bit A/D data registers. • 8-, 10-, and 12-bit accuracy output of A/D conversion results • In A/D-converted value addition mode, the value obtained by adding up A/D-converted results is stored as (conversion accuracy bit count + 2 bits / 4 bits) in the A/D data registers.

Item	RX64M (S12ADC)	RX66N (S12ADFa)
Data registers	• Double trigger mode (selectable in single scan or group scan mode) — The first piece of A/D-converted analog input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers) — A/D-converted analog input data on one selected channel is stored in the duplication register prepared for each trigger.	• Double trigger mode (selectable in single scan or group scan mode) — The first piece of A/D-converted analog input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers) — A/D-converted analog input data on one selected channel is stored in the duplication register prepared for each trigger.
Operating modes	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 8 (unit 0) or 21 (unit 1) arbitrarily selected channels, on the temperature sensor output (unit 1 only), or on the internal reference voltage (unit 1 only). — A/D conversion is performed only once on the extended analog input (unit 1 only). • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs of up to 8 (unit 0) or 21 (unit 1) arbitrarily selected channels, on the temperature sensor output (unit 1 only), or on the internal reference voltage (unit 1 only). — A/D conversion is performed repeatedly on the extended analog input (unit 1 only).	The operating mode can be set independently for two units. • Single scan mode: — A/D conversion is performed only once on arbitrarily selected analog inputs. — A/D conversion is performed only once on the temperature sensor output (S12AD1). — A/D conversion is performed only once on the internal reference voltage (S12AD1). — A/D conversion is performed only once on the extended analog input (S12AD1). • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs of arbitrarily selected channels, the temperature sensor output (S12AD1), or internal reference voltage (S12AD1). — A/D conversion is performed repeatedly on the extended analog input (S12AD1).

Item	RX64M (S12ADC)	RX66N (S12ADFa)
Operating modes	• Group scan mode: — Analog inputs of up to 8 (unit 0) or 21 (unit 1) arbitrarily selected channels, the temperature sensor output (unit 1 only), and the internal reference voltage (unit 1 only) are divided into group A and group B, and A/D conversion of the analog inputs selected on a group basis is performed only once. — The conditions for starting scanning of groups A and B (synchronous trigger) can be selected independently, allowing A/D conversion of each group to be started at different times. • Group scan mode (group A priority control selected): — When a group A trigger (synchronous or asynchronous) is input during A/D conversion on group B, A/D conversion on group B is stopped and A/D conversion is performed on group A. — It is possible to specify restarting (rescan) of A/D conversion on group B after completion of A/D conversion on group A.	• Group scan mode: — Two (groups A and B) or three (groups A, B, and C) can be selected as the number of the groups to be used. (Only the combination of groups A and B can be selected when the number of the groups is two.) — Analog inputs on arbitrarily selected channels, the temperature sensor output (S12AD1), and the internal reference voltage (S12AD1) are divided into groups A and B or into groups A, B, and C, and A/D conversion is performed only once on the inputs selected in group units. — The conditions for starting scanning of groups A, B, and C (synchronous trigger) can be selected independently, allowing A/D conversion of each group to be started at different times. • Group scan mode (group priority control selected): — If a higher-priority group trigger is input during scanning of a lower-priority group, scan of the lower-priority group is stopped and scan of the higher-priority group is started. The priority order is group A (highest) > group B > group C (lowest). Whether or not to restart scanning of (rescan) the lower-priority group after processing for the higher-priority group completes, is selectable. Rescan can also be set to start either from the first selected channel or from the channel on which A/D conversion is not completed.
Conditions for A/D conversion start	• Software trigger • Synchronous trigger — A/D conversion start can be triggered by the multi-function timer pulse unit (MTU), general-purpose PWM timer (GPT), event link controller (ELC), 8-bit timer (TMR), or 16-bit timer pulse unit (TPU). • Asynchronous trigger — A/D conversion start can be triggered by external trigger pin ADTRG0# (unit 0) or ADTRG1# (unit 1).	• Software trigger • Synchronous trigger — A/D conversion start can be triggered by the multi-function timer pulse unit (MTU), 8-bit timer (TMR), 16-bit timer pulse unit (TPU), or event link controller (ELC). • Asynchronous trigger — A/D conversion start can be triggered by external trigger pin ADTRG0# (S12AD) or DTRG1# (S12AD1) (independently for two units).

Item	RX64M (S12ADC)	RX66N (S12ADFa)
Functions	• Sample-and-hold function • Channel-dedicated sample-and-hold function (three channels for unit 0 only; ability to specify continuous sampling) • Variable sampling state count • 12-bit A/D converter self-diagnostic function • Ability to select between A/D-converted value addition mode and average mode • Analog input disconnection detection assist function (discharge function/ precharge function) • Double trigger mode (duplication of A/D conversion data) • 12-, 10-, or 8-bit conversion switching • Automatic clearing function for A/D data registers • Extended analog input • Digital comparison (ability to select window function)	• Channel-dedicated sample-and-hold function (three channels for S12AD only) • Variable sampling state count (ability to specify on per channel basis) • 12-bit A/D converter self-diagnostic function • Ability to select between A/D-converted value addition mode and average mode • Analog input disconnection detection assist function (discharge function/ precharge function) • Double trigger mode (duplication of A/D conversion data) • 12-, 10-, or 8-bit conversion switching • Automatic clearing function for A/D data registers • Extended analog input • Comparison function (windows A and B)
Interrupt sources	• In modes other than double trigger mode and group scan mode, a scan end interrupt request (S12ADI) can be generated on completion of single scan. • In double trigger mode, a scan end interrupt request (S12ADI) can be generated on completion of double scan. • In group scan mode, a scan end interrupt request (S12ADI) can be generated on completion of group A scan, a group B scan end interrupt request (S12GBADI) can be generated on completion of group B scan.	• In modes other than double trigger mode and group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of single scan (independently for two units). • In double trigger mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of double scan (independently for two units). • In group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of group A scan, a group B scan end interrupt request (S12GBADI or S12GBADI1) can be generated on completion of group B scan, and a group C scan end interrupt request (S12GCADI or S12GCADI1) can be generated on completion of group C scan.

Item	RX64M (S12ADC)	RX66N (S12ADFa)
Interrupt sources	• When double trigger group scan mode is selected, a scan end interrupt request (S12ADI) can be generated on completion of double scan of group A, a group B scan end interrupt request (S12GBADI) can be generated on completion of group B scan. • A compare interrupt (S12CMPI) can be generated upon a match with the comparison condition of the digital compare function. • The S12ADI and S12GBADI interrupts can be used to activate the DMA controller (DMAC) and data transfer controller (DTC).	• When double trigger group scan mode is selected, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of double scan of group A, and a corresponding scan end interrupt request (S12GBADI/S12GCADI or S12GBADI1/S12GCADI1) can be generated on completion of group B or group C scan. • A compare interrupt request (S12CMPAI, S12CMPAI1, S12CMPBI, or S12CMPBI1) can be generated upon a match with the comparison condition of the digital compare function. • The S12ADI/S12ADI1, S12GBADI/S12GBADI1, and S12GCADI/S12GCADI1 interrupts can be used to activate the DMA controller (DMAC) and data transfer controller (DTC).
Event linking function	• An ELC event is generated on completion of scans other than group B scan in group scan mode. • Ability to trigger scanning start from the ELC	• An ELC event is generated upon completion of all scans. • Ability to trigger scanning start from the ELC
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.54 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX64M (S12ADC)	RX66N (S12ADFa)
ADRD	AD[11:0] (RX64M) — (RX66N)	12-bit A/D converted value	12-bit A/D converted value
	DIAGST[1:0] (RX64M) — (RX66N)	Self-diagnosis status bits	Self-diagnosis status bits
ADANSA0	[S12AD.ADANSA0] ANSA0[15:0] (RX64M) ANSA0n (n = 00 to 07) (RX66N) [S12AD1.ADANSA0] ANSA0[15:0] (RX64M) ANSA0n (n = 00 to 15) (RX66N)	A/D conversion channel select bits	A/D conversion channel select bits
ADANSA1	ANSA1[4:0] (RX64M) ANSA1n (n = 00 to 04) (RX66N)	A/D conversion channel select bits	A/D conversion channel select bits
ADANSB0	[S12AD.ADANSB0] ANSB0[15:0] (RX64M) ANSB0n (n = 00 to 07) (RX66N) [S12AD1.ADANSB0] ANSB0[15:0] (RX64M) ANSB0n (n = 00 to 15) (RX66N)	A/D conversion channel select bits	A/D conversion channel select bits
ADANSB1	ANSB1[4:0] (RX64M) ANSB1n (n = 00 to 04) (RX66N)	A/D conversion channel select bits	A/D conversion channel select bits
ADANSC0	—	—	A/D channel select register C0
ADANSC1	—	—	A/D channel select register C1
ADADS0	[S12AD.ADADS0] ADS0[15:0] (RX64M) ADS0n (n = 00 to 07) (RX66N) [S12AD1.ADADS0] ADS0[15:0] (RX64M) ADS0n (n = 00 to 15) (RX66N)	A/D-converted value addition/average channel select bits	A/D-converted value addition/average channel select bits
ADADS1	ADS1[4:0](RX64M) ADS1n (n = 00 to 04) (RX66N)	A/D-converted value addition/average channel select bits	A/D-converted value addition/average channel select bits

Register	Bit	RX64M (S12ADC)	RX66N (S12ADFa)
ADADC	ADC[1:0] (RX64M) ADC[2:0] (RX66N)	Addition count select bits (b1, b0) b1 b0 0 0: 1-time conversion (no addition; same as normal conversion) 0 1: 2-time conversion (addition once) 1 0: 3-time conversion (addition twice)*1 1 1: 4-time conversion (addition three times)	Addition count select bits (b2 to b0) b2 b0 0 0 0: 1-time conversion (no addition; same as normal conversion) 0 0 1: 2-time conversion (addition once) 0 1 0: 3-time conversion (addition twice)*1 0 1 1: 4-time conversion (addition three times) 1 0 1: 16-time conversion (addition 15 times)*1 Settings other than the above are prohibited.
ADGCEXCR	—	—	A/D group C extended input control register
ADGCTRGR	—	—	A/D group C trigger select register
ADSSTRn	—	A/D sampling state register n (n = 0 to 7, L, T and O)	A/D sampling state register n (n = 0 to 15, L, T, and O)
ADGSPCR	LGRRS	—	Restart channel select bit
ADCMPCR	CMPAB[1:0]	—	Window A/B complex conditions setting bits
	CMPBE	—	Comparison window B enable bit
	CMPAE	—	Comparison window A enable bit
	CMPBIE	—	Comparison window B interrupt enable bit
	WCMPE	Window function setting bit (b6)	Window function setting bit (b14)
	CMPIE (RX64M) CMPAIE (RX66N)	Compare interrupt enable bit (b7)	Comparison A interrupt enable bit (b15)
ADCMPANSR0	[S12AD.ADCMPANSR0] CMPS0[15:0] (RX64M) CMPCHA0n (n = 00 to 07) (RX66N) [S12AD1.ADCMPANSR0] CMPS0[15:0] (RX64M) CMPCHA0n (n = 00 to 15) (RX66N)	Compare channel select bits	Comparison window A channel select bits
ADCMPANSR1	CMPS1[4:0] (RX64M) CMPCHA1n (n = 00 to 04) (RX66N)	Compare channel select bits	Comparison window A channel select bits

Register	Bit	RX64M (S12ADC)	RX66N (S12ADFa)
ADCMPLR0	[S12AD.ADCMPLR0] CMPL0[15:0] (RX64M) CMPLCHA0n (n = 00 to 07) (RX66N) [S12AD1.ADCMPLR0] CMPL0[15:0] (RX64M) CMPLCHA0n (n = 00 to 15) (RX66N)	Compare level select bits	Comparison window A comparison condition select bits
ADCMPLR1	CMPL1[4:0] (RX64M) CMPLCHA1n (n = 00 to 04) (RX66N)	Compare level select bits	Comparison window A comparison condition select bits
ADCMPDRy	—	A/D compare data register y (y = 0 and 1) The format used differs depending on the following conditions. For details, refer to RX64M Group User's Manual: Hardware. • The value of the A/D data register format select bit (flush-right or flush-left) • The value of the A/D-conversion accuracy specification bit (12 bits, 10 bits, or 8 bits) • The value of A/D-converted value addition/average mode select register (A/D-converted value addition mode selected or not selected)	A/D compare function window A low-side (y = 0)/ high-side (y = 1) level setting register The format used differs depending on the following conditions. For details, refer to RX66N Group User's Manual: Hardware. • The value of the A/D data register format select bit (flush-right or flush-left) • The value of the A/D-conversion accuracy specification bit (12 bits, 10 bits, or 8 bits) • The value of the A/D-converted value addition/average mode select register (A/D-converted value addition mode selected or not selected) • The value of the A/D-converted value addition/average count select register (addition/average mode or addition count selected)
ADCMPSR0	[S12AD.ADCMPSR0] CMPF0[15:0](RX64M) CMPSTCHA0n (n = 00 to 07) (RX66N) [S12AD1.ADCMPSR0] CMPF0[15:0](RX64M) CMPSTCHA0n (n = 00 to 15) (RX66N)	Compare flag	Comparison window A flag

Register	Bit	RX64M (S12ADC)	RX66N (S12ADFa)
ADCMPSR1	CMPF1[4:0](RX64M) CMPSTCHA1n (n = 00 to 04) (RX66N)	Compare flag	Comparison window A flag
ADWINMON	—	—	A/D comparison function window A/B status monitoring register
ADCMPBNSR	—	—	A/D comparison function window B channel select register
ADWINLLB	—	—	A/D comparison function window B lower level setting register
ADWINULB	—	—	A/D comparison function window B upper level setting register
ADCMPBSR	—	—	A/D comparison function window B channel status register
ADSAM	—	—	A/D conversion time setting register
ADSAMPR	—	—	A/D conversion time setting protection release register

Note: 1. When average mode is selected (ADADC.AVEE = 1), do not select three-time conversion or 16-time conversion (RX66N Group only).

2.29 12-Bit D/A Converter

Table 2.55 is a comparison of 12-bit D/A converter registers.

Table 2.55 Comparison of 12-Bit D/A Converter Registers

Register	Bit	RX64M (R12DA)	RX66N (R12DAa)
DAASWCR	—	—	D/A output amplifier stabilization wait control register

2.30 RAM

Table 2.56 is a comparative overview of RAM, and Table 2.57 is a comparison of RAM registers.

Table 2.56 Comparative Overview of RAM

Item	RX64M		RX66N		
	Without ECC Error Correction (RAM)	**With ECC Error Correction (ECCRAM)**	**RAM**	**Expansion RAM**	**ECCRAM**
Capacity	512 KB (RAM0: 512 KB)	32 KB	512 KB	512 KB	32 KB
Address	RAM0: 0000 0000h to 0007 FFFFh	ECCRAM: 00FF 8000h to 00FF FFFFh	0000 0000h to 0007 FFFFh	0080 0000h to 0087 FFFFh	00FF 8000h to 00FF FFFFh
Memory bus	Memory bus 1	Memory bus 3 (ECCRAM)	Memory bus 1	Memory bus 3	Memory bus 3
Access	• Single-cycle access is possible for both reading and writing. • RAM can be enabled or disabled.	• The ECCRAM function can be enabled or disabled. • The ECC function is disabled: Access takes two cycles for reading or writing. • The ECC function is enabled (when no error has occurred): Access takes two cycles for reading or writing. • The ECC function is enabled (when an error has occurred): Access takes three cycles for reading or writing.	• Single-cycle access is possible for both reading and writing. • RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. • Expansion RAM can be enabled or disabled.	• The ECCRAM function can be enabled or disabled. • The ECC function is disabled: Access takes two cycles for reading or writing. • The ECC function is enabled (when no error has occurred): Access takes two cycles for reading or writing. • The ECC function is enabled (when an error has occurred): Access takes three cycles for reading or writing.
Data retention function	Not available in deep software standby mode		Not available in deep software standby mode		
Low power consumption function	Ability to specify module stop state		Transition to module stop state can be enabled separately for RAM, expansion RAM, and ECCRAM.		
Error checking	• Detection of 1-bit errors • A non-maskable interrupt or interrupt is generated in response to an error.	• ECC error correction: — Correction of 1-bit errors and detection of 2-bit errors • A non-maskable interrupt or interrupt is generated in response to an error.	• Parity checking: 1-bit error detection • A non-maskable interrupt or interrupt is generated in response to an error.		• ECC error correction: — Correction of 1-bit errors and detection of 2-bit errors • A non-maskable interrupt or interrupt is generated in response to an error.

Table 2.57 Comparison of RAM Registers

Register	Bit	RX64M	RX66N
EXRAMMODE	—	—	Expansion RAM operating mode control register
EXRAMSTS	—	—	Expansion RAM error status register
EXRAMECAD	—	—	Expansion RAM error address capture register
EXRAMPRCR	—	—	Expansion RAM protection register

2.31 Standby RAM

Table 2.58 is a comparative overview of standby RAM.

Table 2.58 Comparative Overview of Standby RAM

Item	RX64M	RX66N
RAM capacity	8 KB	8 KB
RAM address	000A 4000h to 000A 5FFFh	000A 4000h to 000A 5FFFh
Access	• Both read and write operations take 2 or 3 cycles of PCLKB when ICLK ≥ PCLKB; 2 cycles of ICLK are needed when ICLK < PCLKB. • Ability to enable or disable RAM access • The endian order conforms to the endian setting of the chip. • Non-aligned access is prohibited. Correct operation is not guaranteed if non-aligned access is attempted.	• Both read and write operations take 3 or 4 cycles of PCLKB when ICLK ≥ PCLKB; 2 or 3 cycles of ICLK are needed when ICLK < PCLKB. • Ability to enable or disable RAM access • The endian order conforms to the endian setting of the chip. • Non-aligned access is prohibited. Correct operation is not guaranteed if non-aligned access is attempted.
Data retention function	Data can be retained in deep software standby mode.	Data can be retained in deep software standby mode.
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

2.32 Flash Memory

Table 2.59 is a comparative overview of flash memory, and Table 2.60 is a comparison of flash memory registers.

Table 2.59 Comparative Overview of Flash Memory

Item	RX64M		RX66N (FLASH)	
	Code Flash Memory	**Data Flash Memory**	**Code Flash Memory**	**Data Flash Memory**
Memory capacity	• User area: Up to 4 MB • User boot area: 32 KB	Data area: 64 KB	User area: Up to 4 MB	Data area: 32 KB
Address	• When capacity is 4.0 MB: FFC0 0000h to FFFF FFFFh • When capacity is 3.0 MB: FFD0 0000h to FFFF FFFFh • When capacity is 2.5 MB: FFD8 0000h to FFFF FFFFh • When capacity is 2.0 MB: FFE0 0000h to FFFF FFFFh	0010 0000h to 0010 FFFFh	• When capacity is 4 MB: FFC0 0000h to FFFF FFFFh • When capacity is 2 MB: FFE0 0000h to FFFF FFFFh	0010 0000h to 0010 FFFFh
ROM cache	—	—	• Capacity: 8 KB • Mapping method: direct mapping • Line size: 16 bytes	—
Read cycle	High-speed mode that takes one cycle of ICLK	A read operation takes eight cycles of FCLK for word or byte access.	• While ROM cache operation is enabled: — When the cache is hit: one cycle — when the cache is missed: One to two cycles • When ROM cache operation is disabled: One cycle	Reading proceeds in every cycle of FCLK.
Value after erasure	FFh	Undefined	FFh	Undefined

Item	RX64M		RX66N (FLASH)	
	Code Flash Memory	**Data Flash Memory**	**Code Flash Memory**	**Data Flash Memory**
Programming/ erasing method	• Programming or erasure of the code flash memory and data flash memory by means of FACI commands specified in the FACI command issuing area (007E 0000h) • Programming or erasure through transfer by a dedicated flash-memory programmer via a serial interface (serial programming) • Programming or erasure of flash memory by a user program (self-programming)		• Programming or erasure of the code flash memory and data flash memory, and programming of the option-setting memory, by means of FACI commands specified in the FACI command issuing area (007E 0000h) (self-programming) • Programming or erasure through transfer by a serial-programmer via a serial interface (serial programming)	
Security function	Protects against illicit tampering or reading of data in flash memory		Protects against illicit tampering or reading of data in flash memory	
Protection function	Protects against erroneous rewriting of the flash memory		Protects against erroneous rewriting of the flash memory	
Dual bank function	—	—	The dual-bank configuration enables safe updating in cases where programming is suspended. • Linear mode: the code flash memory is used as one area. • Dual mode: the code flash memory is divided into two areas.	—
Trusted memory (TM) function	Protects against illicit reading of blocks 8 and 9 in the code flash memory		Protects against unauthorized reading of the code flash memory. • Linear mode: blocks 8 and 9 • Dual mode: blocks 8, 9, 78, and 79	—
Background operation (BGO)	• The code flash memory can be read while the code flash memory is being programmed or erased. • The code flash memory can be read while the data flash memory is being programmed or erased.		• The code flash memory can be read while the code flash memory is being programmed or erased. • The data flash memory can be read while the code flash memory is being programmed or erased. • The code flash memory can be read while the data flash memory is being programmed or erased.	
Units of programming and erasure	• Unit of programming for the user area or user boot area: 256 bytes • Unit of erasure for the user area: Block	• Unit of programming for data area: 4 bytes • Unit of erasure for data area: 64 bytes	• Unit of programming for the user area: 128 bytes • Unit of erasure for the user area: Block	• Unit of programming for data area: 4 bytes • Unit of erasure for data area: 64, 128, or 256 bytes

Item	RX64M		RX66N (FLASH)	
	Code Flash Memory	**Data Flash Memory**	**Code Flash Memory**	**Data Flash Memory**
Other functions	• Interrupts can be accepted during self-programming. • The initial settings of the MCU can be specified in the option-setting memory.		• Interrupts can be accepted during self-programming. • The initial settings of the MCU can be specified in the option-setting memory.	
On-board programming (serial programming/ self-programming)	• Programming/erasure in boot mode (for the SCI interface) — The asynchronous serial interface (SCI1) is used. — The transfer rate is adjusted automatically. — The user boot area can also be programmed or erased. • Programming/erasure in boot mode (USB interface) — USBb is used. — Dedicated hardware is not required, so direct connection to a PC is possible. • Programming/erasure in user boot mode — Support for original boot programs created by the user. • Programming or erasure by a routine for code flash memory or data flash memory programming within the user program — This allows the code flash memory or data flash memory to be programed or erased without resetting the system.		• Programming/erasure in boot mode (for the SCI interface) — The asynchronous serial interface (SCI1) is used. — The transfer rate is adjusted automatically. • Programming/erasure in boot mode (USB interface) — USB is used. — Dedicated hardware is not required, so direct connection to a PC is possible. • Programming/erasure in boot mode (FINE interface) — FINE is used. • Programming or erasure by self-programming — This allows the flash memory to be programed or erased without resetting the system.	
Off-board programming (programming and erasure by dedicated parallel programmer)	Programming or erasure of the user area or user boot area are possible by using a flash writer.	Programming or erasure of the data area by using a flash writer is not possible.	Programming or erasure of the code flash memory or option-setting memory are possible by using a parallel programmer.	Programming or erasure of the data flash memory by using a parallel programmer is not possible.
Unique ID	A 12-byte ID code is provided for each MCU.		A 16-byte ID code is provided for each MCU.	

Table 2.60 Comparison of Flash Memory Registers

Register	Bit	RX64M	RX66N (FALSH)
ROMCE	—	—	ROM cache enable register
ROMCIV	—	—	ROM cache invalidate register
NCRGn	—	—	Non-cacheable area n address register (n = 0 or 1)
NCRCn	—	—	Non-cacheable area n setting register (n = 0 or 1)
FWEPROR	—	Flash P/E protect register	—
FWEPROR	FLWE[1:0]	Flash programming and erasure enable bits b1 b0 0 0: Disables programming and erasure, programming and erasure of lock bits, and blank checking. 0 1: Enables programming and erasure, programming and erasure of lock bits, and blank checking. 1 0: Disables programming and erasure, programming and erasure of lock bits, and blank checking. 1 1: Disables programming and erasure, programming and erasure of lock bits, and blank checking.	Flash programming and erasure enabling bits b1 b0 0 0: Disables programming and erasure, and blank checking. 0 1: Enables programming and erasure, and blank checking. 1 0: Disables programming and erasure, and blank checking. 1 1: Disables programming and erasure, and blank checking.
FASTAT	ECRCT	Error flag	—
FAEINT	ECRCTIE	Error interrupt enable bit	—
FSADDR	FSADDR [31:0]	Start address for FACI command processing bits [Command]: [Address boundary] • Programming (code flash memory): 256-byte • Programming (data flash memory): 4-byte • Block erase (code flash memory): 8 KB or 32 KB • Block erase (data flash memory): 64-byte • Blank check: 4-byte • Configuration setting: 16-byte • Lock-bit programming: 8 KB or 32 KB • Lock-bit read: 8 KB or 32 KB	Start address for FACI command processing bits [Command]: [Address boundary] • Programming (code flash memory): 128-byte • Programming (data flash memory): 4-byte • Block erase (code flash memory): 8 KB or 32 KB • Block erase (data flash memory): 64-byte • Multi-block erase (data flash memory): 64-, 128-, or 256-byte • Blank check (data flash memory): 4-byte • Configuration setting: 16-byte
FCURAME	—	FCURAM enable register	—

Register	Bit	RX64M	RX66N (FALSH)
FSTATR	FRCRCT	1-bit error correction monitor flag	—
	FRDTCT	2-bit error correction monitor flag	—
	FCUERR	FCU error flag	—
	FRDY	Flash ready flag 0: Programming, block erase, P/E suspend, P/E resume, forced stop, blank check, configuration setting, lock bit programming, or lock bit read command processing in progress. 1: None of the above is being processed.	Flash ready flag 0: Programming, block erase, multi-block erase, P/E suspend, P/E resume, forced stop, blank check, or configuration setting command processing in progress. 1: None of the above is being processed.
	OTERR	Other error flag	—
	SECERR	Security error flag	—
	FESETERR	FENTRY setting error flag	—
	ILGCOMERR	Illegal command error flag	—
FPROTR	—	Flash protect register	—
FSUINITR	SUINIT	Set-up initialization bit 0: The FEADDR, FPROTR, FCPSR, FSADDR, FENTRYR, and FBCCNT flash sequencer set-up registers retain their current values. 1: The FEADDR, FPROTR, FCPSR, FSADDR, FENTRYR, and FBCCNT flash sequencer set-up registers are initialized.	Set-up initialization bit 0: The FEADDR, FCPSR, FSADDR, FENTRYR, and FBCCNT flash sequencer set-up registers retain their current values. 1: The FEADDR, FCPSR, FSADDR, FENTRYR, and FBCCNT flash sequencer set-up registers are initialized.
FLKSTAT	—	Lock bit status register	—
FPESTAT	—	Flash P/E status register	—
FPSADDR	PSADR[18:0] (RX64M) PSADR[16:0] (RX66N)	Programmed area start address bits (b18 to b0)	Programmed area start address bits (b16 to b0)
FAWMON	—	—	Flash access window monitor register
FSUACR	—	—	Start-up area control register
EEPFCLK	—	—	Data flash memory access frequency setting register
UIDRn	—	—	Unique ID register n (n = 0 to 3)

2.33 Packages

As indicated in Table 2.61, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage. For details, refer to RX Family Design Guide for Migration between RX Family: Differences in Package External Form (R01AN4591EJ).

Table 2.61 Comparison of Packages

Package Type	Renesas Code	
	RX64M	RX66N
224-pin LFBGA	×	○
177-pin TFLGA	○	×
176-pin LFQFP	PLQP0176KB-A	PLQP0176KB-C
144-pin LFQFP	PLQP0144KA-A	PLQP0144KA-B
100-pin TFLGA	○	×
100-pin LFQFP	PLQP0100KB-A	PLQP0100KB-B

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by blue text. Items that exists on both groups with different specifications are indicated by red text. **Black text** indicates there is no differences in the item's specifications between groups.

3.1 176-Pin LFBGA Package

Table 3.1 is a comparative listing of the pin functions of 176-pin LFBGA package products.

Table 3.1 Comparative Listing of 176-Pin LFBGA Package Pin Functions

176-Pin LFBGA	RX64M	RX66N
A1	AVSS0	AVSS0
A2	AVCC0	AVCC0
A3	VREFL0	VREFL0
A4	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
A5	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
A6	VCC	VCC
A7	VSS	VSS
A8	P94/A20/D20/ET1_ERXD0/RMII1_RXD0	P94/D20/A20
A9	VCC	VCC
A10	P97/A23/D23/ET1_ERXD3	TRSYNC1/P97/D23/A23
A11	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ MMC_D0-B/SDHI_D0-B/QIO0-B/QMO-B/ IRQ6/AN106	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/IRQ6/AN106
A12	P60/CS0#/ET1_TX_EN/RMII1_TXD_EN	P60/CS0#
A13	P63/CS3#/CAS#	P63/CAS#/D2[A2/D2]/CS3#
A14	PE1/D9[A9/D9]/MTIOC4C/MTIOC3B/ GTIOC1B-A/PO18/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/MMC_D5-B/ ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/GTIOC1B/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLB2-B/MMC_D5-B/LCD_DATA15-B/ ANEX1
A15	PE2/D10[A10/D10]/MTIOC4A/GTIOC0B-A/ PO23/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/MMC_D6-B/IRQ7-DS/AN100	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/GTIOC0B/RXD12/SMISO12/ SSCL12/RXDX12/SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/AN100
B1	P05/IRQ13/DA1	P05/SSILRCK1/IRQ13/DA1
B2	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
B3	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
B4	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
B5	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
B6	P91/A17/D17/ET1_COL/SCK7/AN115	P91/D17/A17/SCK7/AN115
B7	P92/A18/D18/POE4#/ET1_CRS/ RMII1_CRS_DV/RXD7/SMISO7/SSCL7/ AN116	P92/D18/A18/POE4#/RXD7/SMISO7/SSCL7/ AN116
B8	PD1/D1[A1/D1]/MTIOC4B/GTIOC1A-E/ POE0#/CTX0/IRQ1/AN109	PD1/D1[A1/D1]/MTIOC4B/POE0#/GTIOC1A/ MOSIC-A/CTX0/LCD_DATA23-B/IRQ1/ AN109
B9	P96/A22/D22/ET1_ERXD2	TRDATA5/P96/D22/A22
B10	PD4/D4[A4/D4]/MTIOC8B/POE11#/ MMC_CMD-B/SDHI_CMD-B/QSSL-B/IRQ4/ AN112	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/QSSL-B/SDHI_CMD-B/ MMC_CMD-B/LCD_DATA20-B/IRQ4/AN112

176-Pin LFBGA	RX64M	RX66N
B11	PG1/D25/ET1_RX_ER/RMII1_RX_ER	TRDATA7/PG1/D25
B12	VSS	VSS
B13	P64/CS4#/WE#	P64/WE#/D3[A3/D3]/CS4#
B14	PE0/D8[A8/D8]/MTIOC3D/GTIOC2B-A/ SCK12/MMC_D4-B/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/ GTIOC2B/SCK12/SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0
B15	PE3/D11[A11/D11]/MTIOC4B/GTIOC2A-A/ PO26/POE8#/TOC3/CTS12#/RTS12#/ SS12#/ET0_ERXD3/MMC_D7-B/AN101	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/TOC3/POE8#/GTIOC2A/CTS12#/ RTS12#/SS12#/ET0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101
C1	AVSS1	AVSS1
C2	AVCC1	AVCC1
C3	VREFH0	VREFH0
C4	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
C5	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
C6	P90/A16/D16/ET1_RX_DV/TXD7/SMOSI7/ SSDA7/AN114	P90/D16/A16/TXD7/SMOSI7/SSDA7/AN114
C7	PD0/D0[A0/D0]/GTIOC1B-E/POE4#/IRQ0/ AN108	PD0/D0[A0/D0]/POE4#/GTIOC1B/ LCD_EXTCLK-B/IRQ0/AN108
C8	PD2/D2[A2/D2]/MTIOC4D/GTIOC0B-E/TIC2/ CRX0/MMC_D2-B/SDHI_D2-B/QIO2_B/ IRQ2/AN110	PD2/D2[A2/D2]/MTIOC4D/TIC2/GTIOC0B/ MISOC-A/CRX0/QIO2-B/SDHI_D2-B/ MMC_D2-B/LCD_DATA22-B/IRQ2/AN110
C9	PD3/D3[A3/D3]/MTIOC8D/GTIOC0A-E/ POE8#/TOC2/MMC_D3-B/SDHI_D3-B/ QIO3-B/IRQ3/AN111	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ GTIOC0A/RSPCKC-A/QIO3-B/SDHI_D3-B/ MMC_D3-B/LCD_DATA21-B/IRQ3/AN111
C10	PG0/D24/ET1_RX_CLK/REF50CK1	TRDATA6/PG0/D24
C11	VCC	VCC
C12	P62/CS2#/RAS#	P62/RAS#/D1[A1/D1]/CS2#
C13	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/ GTIOC1A-A/PO28/ET0_ERXD2/AN102	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/SSLB0-B/ ET0_ERXD2/LCD_DATA12-B/AN102
C14	VSS	VSS
C15	P70/SDCLK	P70/SDCLK
D1	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/ AN119	P01/TMCI0/RXD6/SMISO6/SSCL6/ SSIBCK0/IRQ9/AN119
D2	P02/TMCI1/SCK6/IRQ10/AN120	P02/TMCI1/SCK6/SSIBCK1/IRQ10/AN120
D3	P03/IRQ11/DA0	P03/SSIDATA1/IRQ11/DA0
D4	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/ AN118	P00/TMRI0/TXD6/SMOSI6/SSDA6/ AUDIO_CLK/IRQ8/AN118
D5	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
D6	P93/A19/D19/POE0#/ET1_LINKSTA/CTS7#/ RTS7#/SS7#/AN117	P93/D19/A19/POE0#/CTS7#/RTS7#/SS7#/ AN117
D7	P95/A21/D21/ET1_ERXD1/RMII1_RXD1	TRDATA4/P95/D21/A21
D8	VSS	VSS
D9	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/ MMC_CLK-B/SDHI_CLK-B/QSPCLK-B/ IRQ5/AN113	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/ MTCLKA/POE10#/SSLC1-A/QSPCLK-B/ SDHI_CLK-B/MMC_CLK-B/LCD_DATA19-B/ IRQ5/AN113
D10	PD7/D7[A7/D7]/MTIC5U/POE0#/MMC_D1-B/ SDHI_D1-B/QIO1-B/QMI-B/IRQ7/AN107	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B/ LCD_DATA17-B/IRQ7/AN107
D11	P61/CS1#/SDCS#	P61/SDCS#/D0[A0/D0]/CS1#

176-Pin LFBGA	RX64M	RX66N
D12	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/ GTIOC0A-A/ET0_RX_CLK/REF50CK0/ IRQ5/AN103	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/RSPCKB-B/ ET0_RX_CLK/REF50CK0/LCD_DATA11-B/ IRQ5/AN103
D13	VCC	VCC
D14	PE7/D15[A15/D15]/MTIOC6A/GTIOC3A-E/ TOC1/MMC_RES#-B/SDHI_WP-B/IRQ7/ AN105	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/GTIOC3A/MISOB-B/SDHI_WP/ MMC_RES#-B/LCD_DATA9-B/IRQ7/AN105
D15	P65/CS5#/CKE	P65/CKE/CS5#
E1	PJ5/POE8#/CTS2#/RTS2#/SS2#	PJ5/POE8#/CTS2#/RTS2#/SS2#/SSIRXD0
E2	EMLE	EMLE
E3	PF5/IRQ4	PF5/WAIT#/SSILRCK0/IRQ4
E4	VSS	VSS
E12	PE6/D14[A14/D14]/MTIOC6C/GTIOC3B-E/ TIC1/MMC_CD-B/SDHI_CD-B/IRQ6/AN104	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/GTIOC3B/MOSIB-B/SDHI_CD/ MMC_CD-B/LCD_DATA10-B/IRQ6/AN104
E13	TRDATA0/PG2/D26/ET1_TX_CLK	TRDATA0/PG2/D26
E14	TRDATA1/PG3/D27/ET1_ETXD0/ RMII1_TXD0	TRDATA1/PG3/D27
E15	P67/CS7#/DQM1/MTIOC7C/GTIOC1B-C/ CRX2/IRQ15	P67/DQM1/CS7#/MTIOC7C/GTIOC1B/ CRX2/IRQ15
F1	VBATT	VBATT
F2	VCL	VCL
F3	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/ CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0#	PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/ SS6#/CTS0#/RTS0#/SS0#/SSITXD0/ ET0_EXOUT
F4	BSCANP	BSCANP
F12	P66/CS6#/DQM0/MTIOC7D/GTIOC2B-C/ CTX2	P66/DQM0/CS6#/MTIOC7D/GTIOC2B/CTX2
F13	TRSYNC/PG4/D28/ET1_ETXD1/ RMII1_TXD1	TRSYNC/PG4/D28
F14	PA0/A0/BC0#/DQM2/MTIOC4A/MTIOC6D/ GTIOC0B-C/TIOCA0/CACREF/PO16/ SSLA1-B/ET0_TX_EN/RMII0_TXD_EN	PA0/DQM2/BC0#/A0/MTIOC4A/MTIOC6D/ TIOCA0/PO16/CACREF/GTIOC0B/SSLA1-B/ ET0_TX_EN/RMII0_TXD_EN/LCD_DATA8-B
F15	VSS	VSS
G1	XCIN	XCIN
G2	XCOUT	XCOUT
G3	MD/FINED	MD/FINED
G4	TRST#/PF4	TRST#/PF4
G12	TRCLK/PG5/D29/ET1_ETXD2	TRCLK/PG5/D29
G13	TRDATA2/PG6/D30/ET1_ETXD3	TRDATA2/PG6/D30
G14	PA1/A1/DQM3/MTIOC0B/MTCLKC/ MTIOC7B/GTIOC2A-C/TIOCB0/PO17/ SCK5/SSLA2-B/ET0_WOL/IRQ11	PA1/DQM3/A1/MTIOC0B/MTCLKC/ MTIOC7B/TIOCB0/PO17/GTIOC2A/SCK5/ SSLA2-B/ET0_WOL/LCD_DATA7-B/IRQ11
G15	VCC	VCC
H1	XTAL/P37	XTAL/P37
H2	VSS	VSS
H3	RES#	RES#
H4	UPSEL/P35/NMI	UPSEL/P35/NMI

176-Pin LFBGA	RX64M	RX66N
H12	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/PMGI0_MDC/LCD_DATA4-B/ IRQ5-DS
H13	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ ET0_MDIO/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ ET0_MDIO/PMGI0_MDIO/LCD_DATA5-B/ IRQ6-DS
H14	PA2/A2/MTIOC7A/GTIOC1A-C/PO18/ RXD5/SMISO5/SSCL5/SSLA3-B	PA2/A2/MTIOC7A/PO18/GTIOC1A/RXD5/ SMISO5/SSCL5/SSLA3-B/LCD_DATA6-B
H15	TRDATA3/PG7/D31/ET1_TX_ER	TRDATA3/PG7/D31
J1	EXTAL/P36	EXTAL/P36
J2	VCC	VCC
J3	P34/MTIOC0A/TMCI3/PO12/POE10#/SCK6/ SCK0/ET0_LINKSTA/IRQ4	P34/MTIOC0A/TMCI3/PO12/POE10#/SCK6/ SCK0/ET0_LINKSTA/IRQ4
J4	TMS/PF3	TMS/PF3
J12	PA5/A5/MTIOC6B/GTIOC0A-C/TIOCB1/ PO21/RSPCKA-B/ET0_LINKSTA	PA5/A5/MTIOC6B/TIOCB1/PO21/GTIOC0A/ RSPCKA-B/ET0_LINKSTA/LCD_DATA3-B
J13	VSS	VSS
J14	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/ LCD_DATA1-B
J15	PA6/A6/MTIC5V/MTCLKB/GTETRG-C/ TIOCA2/TMCI3/PO22/POE10#/CTS5#/ RTS5#/SS5#/MOSIA-B/ET0_EXOUT	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/GTETRGB/CTS5#/RTS5#/ SS5#/MOSIA-B/ET0_EXOUT/LCD_DATA2-B
K1	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/RXD0/ SMISO6/SMISO0/SSCL6/SSCL0/CRX0/ PCKO/IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/SMISO6/ SSCL6/RXD0/SMISO0/SSCL0/CRX0/PCKO/ IRQ3-DS
K2	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCOUT/RTCIC2/POE0#/POE10#/TXD6/ TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCIC2/RTCOUT/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS
K3	TDI/PF2/RXD1/SMISO1/SSCL1	TDI/PF2/RXD1/SMISO1/SSCL1
K4	TCK/PF1/SCK1	TCK/PF1/SCK1
K12	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/ RTS4#/CTS6#/RTS6#/SS4#/SS6#/ ET0_RX_CLK/REF50CK0	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/ RTS4#/SS4#/CTS6#/RTS6#/SS6#/ ET0_RX_CLK/REF50CK0/LCD_TCON2-B
K13	P71/A18/CS1#/ET0_MDIO	P71/A18/CS1#/ET0_MDIO/PMGI0_MDIO
K14	VCC	VCC
K15	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/ RXD6/SMISO4/SMISO6/SSCL4/SSCL6/ ET0_ERXD1/RMII0_RXD1/IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/ SMISO4/SSCL4/RXD6/SMISO6/SSCL6/ ET0_ERXD1/RMII0_RXD1/LCD_DATA0-B/ IRQ12
L1	P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/ RTS1#/SS1#/ET1_MDC/IRQ1-DS	P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/ RTS1#/SS1#/SSLB0-A/IRQ1-DS
L2	P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/ RXD1/SMISO1/SSCL1/ET1_MDIO/IRQ0-DS	P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/ RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS
L3	TDO/PF0/TXD1/SMOSI1/SSDA1	TDO/PF0/TXD1/SMOSI1/SSDA1
L4	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ SSIDATA1/HSYNC/ADTRG0#	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/ MTCLKB/TIOCA4/PO5/RXD3/SMISO3/ SSCL3/SSIDATA1/SDHI_CD/HSYNC/ ADTRG0#

176-Pin LFBGA	RX64M	RX66N
L12	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9*2/ ET0_ETXD1/RMII0_TXD1	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ ET0_ETXD1/RMII0_TXD1
L13	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ ET0_RX_ER/RMII0_RX_ER	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ ET0_RX_ER/RMII0_RX_ER/LCD_TCON1-B
L14	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD4/TXD6/SMOSI4/SMOSI6/ SSDA4/SSDA6/ET0_ERXD0/RMII0_RXD0/ IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD4/SMOSI4/SSDA4/TXD6/ SMOSI6/SSDA6/ET0_ERXD0/RMII0_RXD0/ LCD_TCON3-B/IRQ4-DS
L15	P72/A19/CS2#/ET0_MDC	P72/A19/CS2#/ET0_MDC/PMGI0_MDC/ LCD_DATA23-A
M1	P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/ ET1_WOL	P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/ RSPCKB-A
M2	P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/ ET1_EXOUT	P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A
M3	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SSISCK1/PIXCLK	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SSIBCK1/SDHI_WP/PIXCLK
M4	P86/MTIOC4D/GTIOC2B-B/TIOCA0/ RXD10*2/PIXD1	P86/MTIOC4D/TIOCA0/GTIOC2B/SMISO10/ SSCL10/RXD10/PIXD1
M5	VCC_USB	CLKOUT25M/PJ2/TXD8/SMOSI8/SSDA8/ SSLC3-B/LCD_TCON2-A
M6	AVCC_USBA	PJ1/MTIOC6A/RXD8/SMISO8/SSCL8/ SSLC2-B/LCD_TCON3-A
M7	USBA_RREF	P85/MTIOC6C/TIOCC0/LCD_DATA1-A
M8	VCC_USBA	P55/D0[A0/D0]/EDREQ0/WAIT#/MTIOC4D/ TMO3/TXD7/SMOSI7/SSDA7/MISOC-B/ CRX1/ET0_EXOUT/LCD_DATA5-A/IRQ10
M9	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A
M10	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/ GTIOC1A-D/TMRI2/PO29/SCK8*2/ RSPCKA-A/RTS8#*2/ET0_ETXD2/ MMC_D5-A	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/GTIOC1A/SCK8/ RTS8#/SCK10/RSPCKA-A/ET0_ETXD2/ MMC_D5-A/LCD_DATA11-A
M11	P81/EDACK0/MTIOC3D/GTIOC0B-D/PO27/ RXD10*2/ET0_ETXD0/RMII0_TXD0/ MMC_D3-A/SDHI_CD-A/QIO3-A	P81/EDACK0/MTIOC3D/PO27/GTIOC0B/ SMISO10/SSCL10/RXD10/ET0_ETXD0/ RMII0_TXD0/QIO3-A/SDHI_CD/MMC_D3-A/ LCD_DATA13-A
M12	P77/CS7#/PO23/TXD11*2/ET0_RX_ER/ RMII0_RX_ER/MMC_CLK-A/SDHI_CLK-A/ QSPCLK-A	P77/CS7#/PO23/SMOSI11/SSDA11/TXD11/ ET0_RX_ER/RMII0_RX_ER/QSPCLK-A/ SDHI_CLK-A/MMC_CLK-A/LCD_DATA17-A
M13	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9*2/ ET0_CRS/RMII0_CRS_DV	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ ET0_CRS/RMII0_CRS_DV
M14	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9*2/ RTS9#*2/ET0_ETXD0/RMII0_TXD0	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9/RTS9#/SCK11/ ET0_ETXD0/RMII0_TXD0/LCD_CLK-B
M15	PB4/A12/TIOCA4/PO28/CTS9#*2/ ET0_TX_EN/RMII0_TXD_EN	PB4/A12/TIOCA4/PO28/CTS9#/SS9#/ SS11#/CTS11#/RTS11#/ET0_TX_EN/ RMII0_TXD_EN/LCD_TCON0-B
N1	VCC	VCC

176-Pin LFBGA	RX64M	RX66N
N2	P23/EDACK0/MTIOC3D/MTCLKD/ GTIOC0A-B/TIOCD3/PO3/TXD3/CTS0#/ RTS0#/SMOSI3/SS0#/SSDA3/SSISCK0/ PIXD7	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/GTIOC0A/TXD3/SMOSI3/SSDA3/ CTS0#/RTS0#/SS0#/CTX1/SSIBCK0/ SDHI_D1-C/PIXD7
N3	P22/EDREQ0/MTIOC3B/MTCLKC/ GTIOC1A-B/TIOCC3/ TMO0/PO2/SCK0/USB0_OVRCURB/ USBA_OVRCURB/AUDIO_MCLK/PIXD6	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/GTIOC1A/SCK0/ USB0_OVRCURB/AUDIO_CLK/ SDHI_D0-C/PIXD6
N4	P15/MTIOC0B/MTCLKB/GTETRG-B/ TIOCB2/TCLKB/TMCI2/PO13/RXD1/SCK3/ SMISO1/SSCL1/CRX1-DS/USBA_VBUSEN/ SSIWS1/PIXD0/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/GTETRGA/RXD1/SMISO1/ SSCL1/SCK3/CRX1-DS/SSILRCK1/PIXD0/ IRQ5
N5	P12/WR3#/BC3#/MTIC5U/TMCI1/RXD2/ SMISO2/SSCL2/SCL0[FM+]/IRQ2	P12/WR3#/BC3#/MTIC5U/TMCI1/ GTADSM0/RXD2/SMISO2/SSCL2/ SCL0[FM+]/LCD_TCON1-A/IRQ2
N6	VSS_USB	PJ0/MTIOC6B/SCK8/SSLC1-B/ LCD_DATA0-A
N7	VSS2_USBA	P84/MTIOC6D/LCD_DATA2-A
N8	VSS1_USBA	P54/D1[A1/D1]/EDACK0/ALE/MTIOC4B/ TMCI1/CTS2#/RTS2#/SS2#/MOSIC-B/CTX1/ ET0_LINKSTA/LCD_DATA6-A
N9	P51/WR1#/BC1#/WAIT#/SCK2	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A
N10	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ GTIOC3A-D/TMO2/TOC0/PO31/CACREF/ TXD8*2/MISOA-A/ET0_COL/MMC_D7-A/ IRQ14	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/PO31/TOC0/CACREF/GTIOC3A/ TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/ET0_COL/MMC_D7-A/ LCD_DATA9-A/IRQ14
N11	P82/EDREQ1/MTIOC4A/GTIOC2A-D/PO28/ TXD10*2/ET0_ETXD1/RMII0_TXD1/ MMC_D4-A	P82/EDREQ1/MTIOC4A/PO28/GTIOC2A/ SMOSI10/SSDA10/TXD10/ET0_ETXD1/ RMII0_TXD1/MMC_D4-A/LCD_DATA12-A
N12	PC3/A19/MTIOC4D/GTIOC1B-D/TCLKB/ PO24/TXD5/SMOSI5/SSDA5/ET0_TX_ER/ MMC_D0-A/SDHI_D0-A/QIO0-A/QMO-A	PC3/A19/MTIOC4D/TCLKB/PO24/GTIOC1B/ TXD5/SMOSI5/SSDA5/ET0_TX_ER/QMO-A/ QIO0-A/SDHI_D0-A/MMC_D0-A/ LCD_DATA16-A
N13	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14
N14	P73/CS3#/PO16/ET0_WOL	P73/CS3#/PO16/ET0_WOL/LCD_EXTCLK-A
N15	VSS	VSS
P1	VSS	VSS
P2	P17/MTIOC3A/MTIOC3B/MTIOC4B/ GTIOC0B-B/TIOCB0/TCLKD/TMO1/PO15/ POE8#/SCK1/TXD3/SMOSI3/SSDA3/ SDA2-DS/SSITXD0/PIXD3/IRQ7/ADTRG1#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/GTIOC0B/ SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/ SSITXD0/SDHI_D3-C/PIXD3/IRQ7/ ADTRG1#
P3	P87/MTIOC4C/GTIOC1B-B/TIOCA2/ TXD10*2/PIXD2	P87/MTIOC4C/TIOCA2/GTIOC1B/SMOSI10/ SSDA10/TXD10/SDHI_D2-C/PIXD2
P4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/LCD_CLK-A/IRQ4
P5	USB0_DP	VCC_USB
P6	AVSS_USBA	VSS_USB
P7	USBA_DM	P57/RXD7/SMISO7/SSCL7/SSLC0-B/ LCD_DATA3-A

176-Pin LFBGA	RX64M	RX66N
P8	P10/ALE/MTIC5W/TMRI3/ USBA_OVRCURA/IRQ0	P10/ALE/MTIC5W/TMRI3/IRQ0
P9	P52/RD#/RXD2/SMISO2/SSCL2	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A
P10	P83/EDACK1/MTIOC4C/GTIOC0A-D/ CTS10#*2/ET0_CRS/RMII0_CRS_DV/ SCK10*2	P83/EDACK1/MTIOC4C/GTIOC0A/SCK10/ SS10#/CTS10#/ET0_CRS/RMII0_CRS_DV/ LCD_DATA8-A
P11	PC6/A22/CS1#/MTIOC3C/MTCLKA/ GTIOC3B-D/TMCI2/TIC0/PO30/RXD8*2/ MOSIA-A/ET0_ETXD3/MMC_D6-A/IRQ13	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/PO30/TIC0/GTIOC3B/ RXD8/SMISO8/SSCL8/SMISO10/SSCL10/ RXD10/MOSIA-A/ET0_ETXD3/MMC_D6-A/ LCD_DATA10-A/IRQ13
P12	PC4/A20/CS3#/MTIOC3D/MTCLKC/ GTETRG-D/TMCI1/PO25/POE0#/SCK5/ CTS8#*2/SSLA0-A/ET0_TX_CLK/ MMC_D1-A/SDHI_D1-A/QIO1-A/QMI-A	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/GTETRGC/SCK5/CTS8#/ SS8#/SS10#/CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK/QMI-A/QIO1-A/SDHI_D1-A/ MMC_D1-A/LCD_DATA15-A
P13	PC2/A18/MTIOC4B/GTIOC2B-D/TCLKA/ PO21/RXD5/SMISO5/SSCL5/ SSLA3-A/ET0_RX_DV/MMC_CD-A/ SDHI_D3-A	PC2/A18/MTIOC4B/TCLKA/PO21/GTIOC2B/ RXD5/SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV/SDHI_D3-A/MMC_CD-A/ LCD_DATA19-A
P14	P75/CS5#/PO20/SCK11*2/RTS11#*2/ ET0_ERXD0/RMII0_RXD0/ MMC_RES#-A/SDHI_D2-A	P75/CS5#/PO20/SCK11/RTS11#/ ET0_ERXD0/RMII0_RXD0/SDHI_D2-A/ MMC_RES#-A/LCD_DATA20-A
P15	VCC	VCC
R1	P21/MTIOC1B/MTIOC4A/GTIOC2A-B/ TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/ USB0_EXICEN/USBA_EXICEN/SSIWS0/ PIXD5/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/GTIOC2A/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/SDHI_CLK-C/ PIXD5/IRQ9
R2	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/USB0_ID/USBA_ID/ SSIRXD0/PIXD4/IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMD-C/PIXD4/IRQ8
R3	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/SCL2-DS/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/SMOSI1/ SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/ USB0_VBUSEN/USB0_VBUS/ USB0_OVRCURB/IRQ6/ADTRG0#
R4	P13/WR2#/BC2#/MTIOC0B/TIOCA5/TMO3/ PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/ IRQ3/ADTRG1#	P13/WR2#/BC2#/MTIOC0B/TIOCA5/TMO3/ PO13/GTADSM1/TXD2/SMOSI2/SSDA2/ SDA0[FM+]/LCD_TCON0-A/IRQ3/ADTRG1#
R5	USB0_DM	USB0_DM
R6	PVSS_/USBA	USB0_DP
R7	USBA_DP	CLKOUT25M/P56/EDACK1/MTIOC3C/ TIOCA1/SCK7/RSPCKC-B/LCD_DATA4-A
R8	P11/MTIC5V/TMCI3/SCK2/USBA_VBUS/ USBA_VBUSEN/IRQ1	P11/MTIC5V/TMCI3/SCK2/LCD_DATA7-A/ IRQ1
R9	P53*1/BCLK	P53*1/BCLK
R10	VSS	VSS
R11	VCC	VCC
R12	P80/EDREQ0/MTIOC3B/PO26/SCK10*2/ RTS10#*2/ET0_TX_EN/RMII0_TXD_EN/ MMC_D2-A/SDHI_WP-A/QIO2-A	P80/EDREQ0/MTIOC3B/PO26/SCK10/ RTS10#/ET0_TX_EN/RMII0_TXD_EN/ QIO2-A/SDHI_WP/MMC_D2-A/ LCD_DATA14-A

176-Pin LFBGA	RX64M	RX66N
R13	P76/CS6#/PO22/RXD11*2/ET0_RX_CLK/ REF50CK0/MMC_CMD-A/SDHI_CMD-A/ QSSL-A	P76/CS6#/PO22/SMISO11/SSCL11/RXD11/ ET0_RX_CLK/REF50CK0/QSSL-A/ SDHI_CMD-A/MMC_CMD-A/ LCD_DATA18-A
R14	P74/A20/CS4#/PO19/CTS11#*2/ ET0_ERXD1/RMII0_RXD1	P74/A20/CS4#/PO19/SS11#/CTS11#/ ET0_ERXD1/RMII0_RXD1/LCD_DATA21-A
R15	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/LCD_DATA22-A/ IRQ12

Notes: 1. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.
2. Pins for FIFO embedded serial communications interface (SCIFA).

3.2 176-Pin LFQFP Package

Table 3.2 is a comparative listing of the pin functions of 176-pin LFQFP package products.

Table 3.2 Comparative Listing of 176-Pin LFQFP Package Pin Functions

176-Pin LFQFP	RX64M	RX66N
1	AVSS0	AVSS0
2	P05/IRQ13/DA1	P05/SSILRCK1/IRQ13/DA1
3	AVCC1	AVCC1
4	P03/IRQ11/DA0	P03/SSIDATA1/IRQ11/DA0
5	AVSS1	AVSS1
6	P02/TMCI1/SCK6/IRQ10/AN120	P02/TMCI1/SCK6/SSIBCK1/IRQ10/AN120
7	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/ AN119	P01/TMCI0/RXD6/SMISO6/SSCL6/ SSIBCK0/IRQ9/AN119
8	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/ AN118	P00/TMRI0/TXD6/SMOSI6/SSDA6/ AUDIO_CLK/IRQ8/AN118
9	PF5/IRQ4	PF5/WAIT#/SSILRCK0/IRQ4
10	EMLE	EMLE
11	PJ5/POE8#/CTS2#/RTS2#/SS2#	PJ5/POE8#/CTS2#/RTS2#/SS2#/SSIRXD0
12	VSS	VSS
13	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/ CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0#	PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/ SS6#/CTS0#/RTS0#/SS0#/SSITXD0/ ET0_EXOUT
14	VCL	VCL
15	VBATT	VBATT
16	NC	NC
17	TRST#/PF4	TRST#/PF4
18	MD/FINED	MD/FINED
19	XCIN	XCIN
20	XCOUT	XCOUT
21	RES#	RES#
22	XTAL/P37	XTAL/P37
23	VSS	VSS
24	EXTAL/P36	EXTAL/P36
25	VCC	VCC
26	UPSEL/P35/NMI	UPSEL/P35/NMI
27	P34/MTIOC0A/TMCI3/PO12/POE10#/SCK6/ SCK0/ET0_LINKSTA/IRQ4	P34/MTIOC0A/TMCI3/PO12/POE10#/SCK6/ SCK0/ET0_LINKSTA/IRQ4
28	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/RXD0/ SMISO6/SMISO0/SSCL6/SSCL0/CRX0/ PCKO/IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/SMISO6/ SSCL6/RXD0/SMISO0/SSCL0/CRX0/PCKO/ IRQ3-DS
29	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCOUT/RTCIC2/POE0#/POE10#/TXD6/ TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCIC2/RTCOUT/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS
30	TMS/PF3	TMS/PF3
31	TDI/PF2/RXD1/SMISO1/SSCL1	TDI/PF2/RXD1/SMISO1/SSCL1
32	P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/ RTS1#/SS1#/ET1_MDC/IRQ1-DS	P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/ RTS1#/SS1#/SSLB0-A/IRQ1-DS
33	P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/ RXD1/SMISO1/SSCL1/ET1_MDIO/IRQ0-DS	P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/ RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS

176-Pin LFQFP	RX64M	RX66N
34	TCK/PF1/SCK1	TCK/PF1/SCK1
35	TDO/PF0/TXD1/SMOSI1/SSDA1	TDO/PF0/TXD1/SMOSI1/SSDA1
36	P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/ ET1_WOL	P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/ RSPCKB-A
37	P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/ ET1_EXOUT	P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A
38	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ SSIDATA1/HSYNC/ADTRG0#	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/ MTCLKB/TIOCA4/PO5/RXD3/SMISO3/ SSCL3/SSIDATA1/SDHI_CD/HSYNC/ ADTRG0#
39	VCC	VCC
40	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SSISCK1/PIXCLK	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SSIBCK1/SDHI_WP/PIXCLK
41	VSS	VSS
42	P23/EDACK0/MTIOC3D/MTCLKD/ GTIOC0A-B/TIOCD3/PO3/TXD3/CTS0#/ RTS0#/SMOSI3/SS0#/SSDA3/SSISCK0/ PIXD7	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/GTIOC0A/TXD3/SMOSI3/SSDA3/ CTS0#/RTS0#/SS0#/CTX1/SSIBCK0/ SDHI_D1-C/PIXD7
43	P22/EDREQ0/MTIOC3B/MTCLKC/ GTIOC1A-B/TIOCC3/TMO0/PO2/SCK0/ USB0_OVRCURB/USBA_OVRCURB/ AUDIO_MCLK/PIXD6	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/GTIOC1A/SCK0/ USB0_OVRCURB/AUDIO_CLK/ SDHI_D0-C/PIXD6
44	P21/MTIOC1B/MTIOC4A/GTIOC2A-B/ TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/ USB0_EXICEN/USBA_EXICEN/SSIWS0/ PIXD5/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/GTIOC2A/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/SDHI_CLK-C/ PIXD5/IRQ9
45	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/USB0_ID/USBA_ID/ SSIRXD0/PIXD4/IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMD-C/PIXD4/IRQ8
46	P17/MTIOC3A/MTIOC3B/MTIOC4B/ GTIOC0B-B/TIOCB0/TCLKD/TMO1/PO15/ POE8#/SCK1/TXD3/SMOSI3/SSDA3/ SDA2-DS/SSITXD0/PIXD3/IRQ7/ADTRG1#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/GTIOC0B/ SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/ SSITXD0/SDHI_D3-C/PIXD3/IRQ7/ ADTRG1#
47	P87/MTIOC4C/GTIOC1B-B/TIOCA2/ TXD10*2/PIXD2	P87/MTIOC4C/TIOCA2/GTIOC1B/SMOSI10/ SSDA10/TXD10/SDHI_D2-C/PIXD2
48	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/SCL2-DS/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/SMOSI1/ SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/ USB0_VBUSEN/USB0_VBUS/ USB0_OVRCURB/IRQ6/ADTRG0#
49	P86/MTIOC4D/GTIOC2B-B/TIOCA0/ RXD10*2/PIXD1	P86/MTIOC4D/TIOCA0/GTIOC2B/SMISO10/ SSCL10/RXD10/PIXD1
50	P15/MTIOC0B/MTCLKB/GTETRG-B/ TIOCB2/TCLKB/TMCI2/PO13/RXD1/SCK3/ SMISO1/SSCL1/CRX1-DS/USBA_VBUSEN/ SSIWS1/PIXD0/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/GTETRGA/RXD1/SMISO1/ SSCL1/SCK3/CRX1-DS/SSILRCK1/PIXD0/ IRQ5
51	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/GTETRGD/CTS1#/RTS1#/ SS1#/CTX1/USB0_OVRCURA/LCD_CLK-A/ IRQ4

176-Pin LFQFP	RX64M	RX66N
52	P13/WR2#/BC2#/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG1#	P13/WR2#/BC2#/MTIOC0B/TIOCA5/TMO3/PO13/GTADSM1/TXD2/SMOSI2/SSDA2/SDA0[FM+]/LCD_TCON0-A/IRQ3/ADTRG1#
53	P12/WR3#/BC3#/MTIC5U/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/IRQ2	P12/WR3#/BC3#/MTIC5U/TMCI1/GTADSM0/RXD2/SMISO2/SSCL2/SCL0[FM+]/LCD_TCON1-A/IRQ2
54	VCC_USB	VCC_USB
55	USB0_DM	USB0_DM
56	USB0_DP	USB0_DP
57	VSS_USB	VSS_USB
58	AVCC_USBA	CLKOUT25M/PJ2/TXD8/SMOSI8/SSDA8/SSLC3-B/LCD_TCON2-A
59	USBA_RREF	PJ1/MTIOC6A/RXD8/SMISO8/SSCL8/SSLC2-B/LCD_TCON3-A
60	AVSS_USBA	PJ0/MTIOC6B/SCK8/SSLC1-B/LCD_DATA0-A
61	PVSS_USBA	P85/MTIOC6C/TIOCC0/LCD_DATA1-A
62	VSS2_USBA	P84/MTIOC6D/LCD_DATA2-A
63	USBA_DM	P57/RXD7/SMISO7/SSCL7/SSLC0-B/LCD_DATA3-A
64	USBA_DP	CLKOUT25M/P56/EDACK1/MTIOC3C/TIOCA1/SCK7/RSPCKC-B/LCD_DATA4-A
65	VSS1_USBA	P55/D0[A0/D0]/EDREQ0/WAIT#/MTIOC4D/TMO3/TXD7/SMOSI7/SSDA7/MISOC-B/CRX1/ET0_EXOUT/LCD_DATA5-A/IRQ10
66	VCC_USBA	P54/D1[A1/D1]/EDACK0/ALE/MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/MOSIC-B/CTX1/ET0_LINKSTA/LCD_DATA6-A
67	P11/MTIC5V/TMCI3/SCK2/USBA_VBUS/USBA_VBUSEN/IRQ1	P11/MTIC5V/TMCI3/SCK2/LCD_DATA7-A/IRQ1
68	P10/ALE/MTIC5W/TMRI3/USBA_OVRCURA/IRQ0	P10/ALE/MTIC5W/TMRI3/IRQ0
69	P53*[1]/BCLK	P53*[1]/BCLK
70	P52/RD#/RXD2/SMISO2/SSCL2	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A
71	P51/WR1#/BC1#/WAIT#/SCK2	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A
72	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A
73	VSS	VSS
74	P83/EDACK1/MTIOC4C/GTIOC0A-D/CTS10#*[2]/ET0_CRS/RMII0_CRS_DV/SCK10*[2]	P83/EDACK1/MTIOC4C/GTIOC0A/SCK10/SS10#/CTS10#/ET0_CRS/RMII0_CRS_DV/LCD_DATA8-A
75	VCC	VCC
76	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/GTIOC3A-D/TMO2/TOC0/PO31/CACREF/TXD8*[2]/MISOA-A/ET0_COL/MMC_D7-A/IRQ14	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/PO31/TOC0/CACREF/GTIOC3A/TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/ET0_COL/MMC_D7-A/LCD_DATA9-A/IRQ14
77	PC6/A22/CS1#/MTIOC3C/MTCLKA/GTIOC3B-D/TMCI2/TIC0/PO30/RXD8*[2]/MOSIA-A/ET0_ETXD3/MMC_D6-A/IRQ13	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/PO30/TIC0/GTIOC3B/RXD8/SMISO8/SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/ET0_ETXD3/MMC_D6-A/LCD_DATA10-A/IRQ13

176-Pin LFQFP	RX64M	RX66N
78	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/ GTIOC1A-D/TMRI2/PO29/SCK8*2/ RSPCKA-A/RTS8#*2/ET0_ETXD2/ MMC_D5-A	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/GTIOC1A/SCK8/ RTS8#/SCK10/RSPCKA-A/ET0_ETXD2/ MMC_D5-A/LCD_DATA11-A
79	P82/EDREQ1/MTIOC4A/GTIOC2A-D/PO28/ TXD10*2/ET0_ETXD1/RMII0_TXD1/ MMC_D4-A	P82/EDREQ1/MTIOC4A/PO28/GTIOC2A/ SMOSI10/SSDA10/TXD10/ET0_ETXD1/ RMII0_TXD1/MMC_D4-A/LCD_DATA12-A
80	P81/EDACK0/MTIOC3D/GTIOC0B-D/PO27/ RXD10*2/ET0_ETXD0/RMII0_TXD0/ MMC_D3-A/SDHI_CD-A/QIO3-A	P81/EDACK0/MTIOC3D/PO27/GTIOC0B/ SMISO10/SSCL10/RXD10/ET0_ETXD0/ RMII0_TXD0/QIO3-A/SDHI_CD/MMC_D3-A/ LCD_DATA13-A
81	P80/EDREQ0/MTIOC3B/PO26/SCK10*2/ RTS10#*2/ET0_TX_EN/RMII0_TXD_EN/ MMC_D2-A/SDHI_WP-A/QIO2-A	P80/EDREQ0/MTIOC3B/PO26/SCK10/ RTS10#/ET0_TX_EN/RMII0_TXD_EN/ QIO2-A/SDHI_WP/MMC_D2-A/ LCD_DATA14-A
82	PC4/A20/CS3#/MTIOC3D/MTCLKC/ GTETRG-D/TMCI1/PO25/POE0#/SCK5/ CTS8#*2/SSLA0-A/ET0_TX_CLK/ MMC_D1-A/SDHI_D1-A/QIO1-A/QMI-A	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/GTETRGC/SCK5/CTS8#/ SS8#/SS10#/CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK/QMI-A/QIO1-A/SDHI_D1-A/ MMC_D1-A/LCD_DATA15-A
83	PC3/A19/MTIOC4D/GTIOC1B-D/TCLKB/ PO24/TXD5/SMOSI5/SSDA5/ET0_TX_ER/ MMC_D0-A/SDHI_D0-A/QIO0-A/QMO-A	PC3/A19/MTIOC4D/TCLKB/PO24/GTIOC1B/ TXD5/SMOSI5/SSDA5/ET0_TX_ER/QMO-A/ QIO0-A/SDHI_D0-A/MMC_D0-A/ LCD_DATA16-A
84	P77/CS7#/PO23/TXD11*2/ET0_RX_ER/ RMII0_RX_ER/MMC_CLK-A/SDHI_CLK-A/ QSPCLK-A	P77/CS7#/PO23/SMOSI11/SSDA11/TXD11/ ET0_RX_ER/RMII0_RX_ER/QSPCLK-A/ SDHI_CLK-A/MMC_CLK-A/LCD_DATA17-A
85	P76/CS6#/PO22/RXD11*2/ET0_RX_CLK/ REF50CK0/MMC_CMD-A/SDHI_CMD-A/ QSSL-A	P76/CS6#/PO22/SMISO11/SSCL11/RXD11/ ET0_RX_CLK/REF50CK0/QSSL-A/ SDHI_CMD-A/MMC_CMD-A/ LCD_DATA18-A
86	PC2/A18/MTIOC4B/GTIOC2B-D/TCLKA/ PO21/RXD5/SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV/MMC_CD-A/SDHI_D3-A	PC2/A18/MTIOC4B/TCLKA/PO21/GTIOC2B/ RXD5/SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV/SDHI_D3-A/MMC_CD-A/ LCD_DATA19-A
87	P75/CS5#/PO20/SCK11*2/RTS11#*2/ ET0_ERXD0/RMII0_RXD0/MMC_RES#-A/ SDHI_D2-A	P75/CS5#/PO20/SCK11/RTS11#/ ET0_ERXD0/RMII0_RXD0/SDHI_D2-A/ MMC_RES#-A/LCD_DATA20-A
88	P74/A20/CS4#/PO19/CTS11#*2/ ET0_ERXD1/RMII0_RXD1	P74/A20/CS4#/PO19/SS11#/CTS11#/ ET0_ERXD1/RMII0_RXD1/LCD_DATA21-A
89	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/LCD_DATA22-A/ IRQ12
90	VCC	VCC
91	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14
92	VSS	VSS
93	P73/CS3#/PO16/ET0_WOL	P73/CS3#/PO16/ET0_WOL/LCD_EXTCLK-A
94	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9*2/ ET0_CRS/RMII0_CRS_DV	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ ET0_CRS/RMII0_CRS_DV
95	PB6/A14/MTIOC3D/TIOCA5/PO30/ RXD9*2/ET0_ETXD1/RMII0_TXD1	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ ET0_ETXD1/RMII0_TXD1

176-Pin LFQFP	RX64M	RX66N
96	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9*2/RTS9#*2/ ET0_ETXD0/RMII0_TXD0	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9/RTS9#/SCK11/ ET0_ETXD0/RMII0_TXD0/LCD_CLK-B
97	PB4/A12/TIOCA4/PO28/CTS9#*2/ ET0_TX_EN/RMII0_TXD_EN	PB4/A12/TIOCA4/PO28/CTS9#/SS9#/ SS11#/CTS11#/RTS11#/ ET0_TX_EN/RMII0_TXD_EN/LCD_TCON0-B
98	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ ET0_RX_ER/RMII0_RX_ER	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ ET0_RX_ER/RMII0_RX_ER/LCD_TCON1-B
99	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/ RTS4#/CTS6#/RTS6#/SS4#/SS6#/ ET0_RX_CLK/REF50CK0	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/ RTS4#/SS4#/CTS6#/RTS6#/SS6#/ ET0_RX_CLK/REF50CK0/LCD_TCON2-B
100	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD4/TXD6/SMOSI4/SMOSI6/ SSDA4/SSDA6/ET0_ERXD0/RMII0_RXD0/ IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD4/SMOSI4/SSDA4/TXD6/ SMOSI6/SSDA6/ET0_ERXD0/RMII0_RXD0/ LCD_TCON3-B/IRQ4-DS
101	P72/A19/CS2#/ET0_MDC	P72/A19/CS2#/ET0_MDC/PMGI0_MDC/ LCD_DATA23-A
102	P71/A18/CS1#/ET0_MDIO	P71/A18/CS1#/ET0_MDIO/PMGI0_MDIO
103	VCC	VCC
104	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/ RXD6/SMISO4/SMISO6/SSCL4/SSCL6/ ET0_ERXD1/RMII0_RXD1/IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/ SMISO4/SSCL4/RXD6/SMISO6/SSCL6/ ET0_ERXD1/RMII0_RXD1/LCD_DATA0-B/ IRQ12
105	VSS	VSS
106	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/ LCD_DATA1-B
107	PA6/A6/MTIC5V/MTCLKB/GTETRG-C/ TIOCA2/TMCI3/PO22/POE10#/CTS5#/ RTS5#/SS5#/MOSIA-B/ET0_EXOUT	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/GTETRGB/CTS5#/RTS5#/ SS5#/MOSIA-B/ET0_EXOUT/LCD_DATA2-B
108	PA5/A5/MTIOC6B/GTIOC0A-C/TIOCB1/ PO21/RSPCKA-B/ET0_LINKSTA	PA5/A5/MTIOC6B/TIOCB1/PO21/GTIOC0A/ RSPCKA-B/ET0_LINKSTA/LCD_DATA3-B
109	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/PMGI0_MDC/LCD_DATA4-B/ IRQ5-DS
110	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ ET0_MDIO/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ ET0_MDIO/PMGI0_MDIO/LCD_DATA5-B/ IRQ6-DS
111	TRDATA3/PG7/D31/ET1_TX_ER	TRDATA3/PG7/D31
112	PA2/A2/MTIOC7A/GTIOC1A-C/PO18/RXD5/ SMISO5/SSCL5/SSLA3-B	PA2/A2/MTIOC7A/PO18/GTIOC1A/RXD5/ SMISO5/SSCL5/SSLA3-B/LCD_DATA6-B
113	TRDATA2/PG6/D30/ET1_ETXD3	TRDATA2/PG6/D30
114	PA1/A1/DQM3/MTIOC0B/MTCLKC/ MTIOC7B/GTIOC2A-C/TIOCB0/PO17/SCK5/ SSLA2-B/ET0_WOL/IRQ11	PA1/DQM3/A1/MTIOC0B/MTCLKC/ MTIOC7B/TIOCB0/PO17/GTIOC2A/SCK5/ SSLA2-B/ET0_WOL/LCD_DATA7-B/IRQ11
115	VCC	VCC
116	TRCLK/PG5/D29/ET1_ETXD2	TRCLK/PG5/D29
117	VSS	VSS
118	PA0/A0/BC0#/DQM2/MTIOC4A/MTIOC6D/ GTIOC0B-C/TIOCA0/CACREF/PO16/ SSLA1-B/ET0_TX_EN/RMII0_TXD_EN	PA0/DQM2/BC0#/A0/MTIOC4A/MTIOC6D/ TIOCA0/PO16/CACREF/GTIOC0B/SSLA1-B/ ET0_TX_EN/RMII0_TXD_EN/LCD_DATA8-B

176-Pin LFQFP	RX64M	RX66N
119	TRSYNC/PG4/D28/ET1_ETXD1/ RMII1_TXD1	TRSYNC/PG4/D28
120	P67/CS7#/DQM1/MTIOC7C/GTIOC1B-C/ CRX2/IRQ15	P67/DQM1/CS7#/MTIOC7C/GTIOC1B/ CRX2/IRQ15
121	TRDATA1/PG3/D27/ET1_ETXD0/ RMII1_TXD0	TRDATA1/PG3/D27
122	P66/CS6#/DQM0/MTIOC7D/GTIOC2B-C/ CTX2	P66/DQM0/CS6#/MTIOC7D/GTIOC2B/ CTX2
123	TRDATA0/PG2/D26/ET1_TX_CLK	TRDATA0/PG2/D26
124	P65/CS5#/CKE	P65/CKE/CS5#
125	PE7/D15[A15/D15]/MTIOC6A/GTIOC3A-E/ TOC1/MMC_RES#-B/SDHI_WP-B/IRQ7/ AN105	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/GTIOC3A/MISOB-B/SDHI_WP/ MMC_RES#-B/LCD_DATA9-B/IRQ7/AN105
126	PE6/D14[A14/D14]/MTIOC6C/GTIOC3B-E/ TIC1/MMC_CD-B/SDHI_CD-B/IRQ6/AN104	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/GTIOC3B/MOSIB-B/SDHI_CD/ MMC_CD-B/LCD_DATA10-B/IRQ6/AN104
127	VCC	VCC
128	P70/SDCLK	P70/SDCLK
129	VSS	VSS
130	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/ GTIOC0A-A/ET0_RX_CLK/REF50CK0/ IRQ5/AN103	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/RSPCKB-B/ ET0_RX_CLK/REF50CK0/LCD_DATA11-B/ IRQ5/AN103
131	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/ GTIOC1A-A/PO28/ET0_ERXD2/AN102	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/SSLB0-B/ ET0_ERXD2/LCD_DATA12-B/AN102
132	PE3/D11[A11/D11]/MTIOC4B/GTIOC2A-A/ PO26/POE8#/TOC3/CTS12#/RTS12#/ SS12#/ET0_ERXD3/MMC_D7-B/AN101	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/TOC3/POE8#/GTIOC2A/CTS12#/ RTS12#/SS12#/ET0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101
133	PE2/D10[A10/D10]/MTIOC4A/GTIOC0B-A/ PO23/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/MMC_D6-B/IRQ7-DS/AN100	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/GTIOC0B/RXD12/SMISO12/ SSCL12/RXDX12/SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/AN100
134	PE1/D9[A9/D9]/MTIOC4C/MTIOC3B/ GTIOC1B-A/PO18/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/MMC_D5-B/ ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/GTIOC1B/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLB2-B/MMC_D5-B/LCD_DATA15-B/ ANEX1
135	PE0/D8[A8/D8]/MTIOC3D/GTIOC2B-A/ SCK12*[2]/MMC_D4-B/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/ GTIOC2B/SCK12/SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0
136	P64/CS4#/WE#	P64/WE#/D3[A3/D3]/CS4#
137	P63/CS3#/CAS#	P63/CAS#/D2[A2/D2]/CS3#
138	P62/CS2#/RAS#	P62/RAS#/D1[A1/D1]/CS2#
139	P61/CS1#/SDCS#	P61/SDCS#/D0[A0/D0]/CS1#
140	VSS	VSS
141	P60/CS0#/ET1_TX_EN/RMII1_TXD_EN	P60/CS0#
142	VCC	VCC
143	PD7/D7[A7/D7]/MTIC5U/POE0#/MMC_D1-B/ SDHI_D1-B/QIO1-B/QMI-B/IRQ7/AN107	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B/ LCD_DATA17-B/IRQ7/AN107
144	PG1/D25/ET1_RX_ER/RMII1_RX_ER	TRDATA7/PG1/D25

176-Pin LFQFP	RX64M	RX66N
145	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ MMC_D0-B/SDHI_D0-B/QIO0-B/QMO-B/ IRQ6/AN106	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/IRQ6/AN106
146	PG0/D24/ET1_RX_CLK/REF50CK1	TRDATA6/PG0/D24
147	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/ MMC_CLK-B/SDHI_CLK-B/QSPCLK-B/ IRQ5/AN113	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/ MTCLKA/POE10#/SSLC1-A/QSPCLK-B/ SDHI_CLK-B/MMC_CLK-B/LCD_DATA19-B/ IRQ5/AN113
148	PD4/D4[A4/D4]/MTIOC8B/POE11#/ MMC_CMD-B/SDHI_CMD-B/QSSL-B/IRQ4/ AN112	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/QSSL-B/SDHI_CMD-B/ MMC_CMD-B/LCD_DATA20-B/IRQ4/AN112
149	P97/A23/D23/ET1_ERXD3	TRSYNC1/P97/D23/A23
150	PD3/D3[A3/D3]/MTIOC8D/GTIOC0A-E/ POE8#/TOC2/MMC_D3-B/SDHI_D3-B/ QIO3-B/IRQ3/AN111	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ GTIOC0A/RSPCKC-A/QIO3-B/SDHI_D3-B/ MMC_D3-B/LCD_DATA21-B/IRQ3/AN111
151	VSS	VSS
152	P96/A22/D22/ET1_ERXD2	TRDATA5/P96/D22/A22
153	VCC	VCC
154	PD2/D2[A2/D2]/MTIOC4D/GTIOC0B-E/TIC2/ CRX0/MMC_D2-B/SDHI_D2-B/QIO2_B/ IRQ2/AN110	PD2/D2[A2/D2]/MTIOC4D/TIC2/GTIOC0B/ MISOC-A/CRX0/QIO2-B/SDHI_D2-B/ MMC_D2-B/LCD_DATA22-B/IRQ2/AN110
155	P95/A21/D21/ET1_ERXD1/RMII1_RXD1	TRDATA4/P95/D21/A21
156	PD1/D1[A1/D1]/MTIOC4B/GTIOC1A-E/ POE0#/CTX0/IRQ1/AN109	PD1/D1[A1/D1]/MTIOC4B/POE0#/GTIOC1A/ MOSIC-A/CTX0/LCD_DATA23-B/IRQ1/ AN109
157	P94/A20/D20/ET1_ERXD0/RMII1_RXD0	P94/D20/A20
158	PD0/D0[A0/D0]/GTIOC1B-E/POE4#/IRQ0/ AN108	PD0/D0[A0/D0]/POE4#/GTIOC1B/ LCD_EXTCLK-B/IRQ0/AN108
159	P93/A19/D19/POE0#/ET1_LINKSTA/CTS7#/ RTS7#/SS7#/AN117	P93/D19/A19/POE0#/CTS7#/RTS7#/SS7#/ AN117
160	P92/A18/D18/POE4#/ET1_CRS/ RMII1_CRS_DV/RXD7/SMISO7/SSCL7/ AN116	P92/D18/A18/POE4#/RXD7/SMISO7/SSCL7/ AN116
161	P91/A17/D17/ET1_COL/SCK7/AN115	P91/D17/A17/SCK7/AN115
162	VSS	VSS
163	P90/A16/D16/ET1_RX_DV/TXD7/SMOSI7/ SSDA7/AN114	P90/D16/A16/TXD7/SMOSI7/SSDA7/AN114
164	VCC	VCC
165	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
166	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
167	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
168	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
169	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
170	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
171	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
172	VREFL0	VREFL0
173	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
174	VREFH0	VREFH0
175	AVCC0	AVCC0
176	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#

Notes: 1. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.
2. Pins for FIFO embedded serial communications interface (SCIFA).

3.3 145-Pin TFLGA Package

Table 3.3 is a comparative listing of the pin functions of 145-pin TFLGA package products.

Table 3.3 Comparative Listing of 145-Pin TFLGA Package Pin Functions

145-Pin TFLGA	RX64M	RX66N
A1	AVSS0	AVSS0
A2	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
A3	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
A4	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
A5	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
A6	P90/A16/TXD7/SMOSI7/SSDA7/AN114	P90/A16/TXD7/SMOSI7/SSDA7/AN114
A7	P92/A18/POE4#/RXD7/SMISO7/SSCL7/ AN116	P92/A18/POE4#/RXD7/SMISO7/SSCL7/ AN116
A8	PD2/D2[A2/D2]/MTIOC4D/GTIOC0B-E/TIC2/ CRX0/MMC_D2-B/SDHI_D2-B/QIO2-B/ IRQ2/AN110	PD2/D2[A2/D2]/MTIOC4D/TIC2/GTIOC0B/ MISOC-A/CRX0/QIO2-B/SDHI_D2-B/ MMC_D2-B/LCD_DATA22-B/IRQ2/AN110
A9	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ MMC_D0-B/SDHI_D0-B/QIO0-B/QMO-B/ IRQ6/AN106	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/IRQ6/AN106
A10	VSS	VSS
A11	P62/CS2#/RAS#	P62/RAS#/D1[A1/D1]/CS2#
A12	PE1/D9[A9/D9]/MTIOC4C/MTIOC3B/ GTIOC1B-A/PO18/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/MMC_D5-B/ ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/GTIOC1B/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLB2-B/MMC_D5-B/LCD_DATA15-B/ ANEX1
A13	PE3/D11[A11/D11]/MTIOC4B/GTIOC2A-A/ PO26/POE8#/TOC3/CTS12#/RTS12#/ SS12#/ET0_ERXD3/MMC_D7-B/AN101	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/TOC3/POE8#/GTIOC2A/CTS12#/ RTS12#/SS12#/ET0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101
B1	AVCC1	AVCC1
B2	AVCC0	AVCC0
B3	P05/IRQ13/DA1	P05/SSILRCK1/IRQ13/DA1
B4	VREFL0	VREFL0
B5	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
B6	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
B7	P91/A17/SCK7/AN115	P91/A17/SCK7/AN115
B8	PD0/D0[A0/D0]/GTIOC1B-E/POE4#/IRQ0/ AN108	PD0/D0[A0/D0]/POE4#/GTIOC1B/ LCD_EXTCLK-B/IRQ0/AN108
B9	PD4/D4[A4/D4]/MTIOC8B/POE11#/ MMC_CMD-B/SDHI_CMD-B/QSSL-B/IRQ4/ AN112	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/QSSL-B/SDHI_CMD-B/ MMC_CMD-B/LCD_DATA20-B/IRQ4/AN112
B10	VCC	VCC
B11	P61/CS1#/SDCS#	P61/SDCS#/D0[A0/D0]/CS1#
B12	PE2/D10[A10/D10]/MTIOC4A/GTIOC0B-A/ PO23/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/MMC_D6-B/IRQ7-DS/AN100	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/GTIOC0B/RXD12/SMISO12/ SSCL12/RXDX12/SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/AN100
B13	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/ GTIOC1A-A/PO28/ET0_ERXD2/AN102	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/SSLB0-B/ ET0_ERXD2/LCD_DATA12-B/AN102
C1	AVSS1	AVSS1

145-Pin TFLGA	RX64M	RX66N
C2	P02/TMCI1/SCK6/IRQ10/AN120	P02/TMCI1/SCK6/SSIBCK1/IRQ10/AN120
C3	VREFH0	VREFH0
C4	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
C5	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
C6	VSS	VSS
C7	PD1/D1[A1/D1]/MTIOC4B/GTIOC1A-E/ POE0#/CTX0/IRQ1/AN109	PD1/D1[A1/D1]/MTIOC4B/POE0#/GTIOC1A/ MOSIC-A/CTX0/LCD_DATA23-B/IRQ1/ AN109
C8	PD3/D3[A3/D3]/MTIOC8D/GTIOC0A-E/ POE8#/TOC2/MMC_D3-B/SDHI_D3-B/ QIO3-B/IRQ3/AN111	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ GTIOC0A/RSPCKC-A/QIO3-B/SDHI_D3-B/ MMC_D3-B/LCD_DATA21-B/IRQ3/AN111
C9	PD7/D7[A7/D7]/MTIC5U/POE0#/ MMC_D1-B/SDHI_D1-B/QIO1-B/QMI-B/ IRQ7/AN107	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B/ LCD_DATA17-B/IRQ7/AN107
C10	P63/CS3#/CAS#	P63/CAS#/D2[A2/D2]/CS3#
C11	PE0/D8[A8/D8]/MTIOC3D/GTIOC2B-A/ SCK12/MMC_D4-B/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/ GTIOC2B/SCK12/SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0
C12	P70/SDCLK	P70/SDCLK
C13	VSS	VSS
D1	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/ AN118	P00/TMRI0/TXD6/SMOSI6/SSDA6/ AUDIO_CLK/IRQ8/AN118
D2	PF5/IRQ4	PF5/WAIT#/SSILRCK0/IRQ4
D3	P03/IRQ11/DA0	P03/SSIDATA1/IRQ11/DA0
D4	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/ AN119	P01/TMCI0/RXD6/SMISO6/SSCL6/ SSIBCK0/IRQ9/AN119
D5	VCC	VCC
D6	P93/A19/POE0#/CTS7#/RTS7#/SS7#/AN117	P93/A19/POE0#/CTS7#/RTS7#/SS7#/AN117
D7	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/ MMC_CLK-B/SDHI_CLK-B/QSPCLK-B/ IRQ5/AN113	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/ MTCLKA/POE10#/SSLC1-A/QSPCLK-B/ SDHI_CLK-B/MMC_CLK-B/ LCD_DATA19-B/IRQ5/AN113
D8	P60/CS0#	P60/CS0#
D9	P64/CS4#/WE#	P64/WE#/D3[A3/D3]/CS4#
D10	PE7/D15[A15/D15]/MTIOC6A/GTIOC3A-E/ TOC1/MMC_RES#-B/SDHI_WP-B/IRQ7/ AN105	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/GTIOC3A/MISOB-B/SDHI_WP/ MMC_RES#-B/LCD_DATA9-B/IRQ7/AN105
D11	VCC	VCC
D12	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/ GTIOC0A-A/ET0_RX_CLK/REF50CK0/ IRQ5/AN103	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/RSPCKB-B/ ET0_RX_CLK/REF50CK0/LCD_DATA11-B/ IRQ5/AN103
D13	PE6/D14[A14/D14]/MTIOC6C/GTIOC3B-E/ TIC1/MMC_CD-B/SDHI_CD-B/IRQ6/ AN104	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/GTIOC3B/MOSIB-B/SDHI_CD/ MMC_CD-B/LCD_DATA10-B/IRQ6/AN104
E1	VSS	VSS
E2	VCL	VCL
E3	PJ5/POE8#/CTS2#/RTS2#/SS2#	PJ5/POE8#/CTS2#/RTS2#/SS2#/SSIRXD0
E4	EMLE	EMLE
E5	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004

145-Pin TFLGA	RX64M	RX66N
E10	PA0/A0/BC0#/MTIOC4A/MTIOC6D/ GTIOC0B-C/TIOCA0/CACREF/PO16/ SSLA1-B/ET0_TX_EN/RMII0_TXD_EN	PA0/BC0#/A0/MTIOC4A/MTIOC6D/TIOCA0/ PO16/CACREF/GTIOC0B/SSLA1-B/ ET0_TX_EN/RMII0_TXD_EN/LCD_DATA8-B
E11	P66/CS6#/DQM0/MTIOC7D/GTIOC2B-C/ CTX2	P66/DQM0/CS6#/MTIOC7D/GTIOC2B/CTX2
E12	P65/CS5#/CKE	P65/CKE/CS5#
E13	P67/CS7#/DQM1/MTIOC7C/GTIOC1B-C/ CRX2/IRQ15	P67/DQM1/CS7#/MTIOC7C/GTIOC1B/ CRX2/IRQ15
F1	XCIN	XCIN
F2	XCOUT	XCOUT
F3	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/ CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0#	PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/ SS6#/CTS0#/RTS0#/SS0#/SSITXD0/ ET0_EXOUT
F4	VBATT	VBATT
F10	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ ET0_MDIO/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ ET0_MDIO/PMGI0_MDIO/LCD_DATA5-B/ IRQ6-DS
F11	VSS	VSS
F12	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ GTIOC2A-C/TIOCB0/PO17/SCK5/ SSLA2-B/ET0_WOL/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/GTIOC2A/SCK5/SSLA2-B/ ET0_WOL/LCD_DATA7-B/IRQ11
F13	PA2/A2/MTIOC7A/GTIOC1A-C/PO18/RXD5/ SMISO5/SSCL5/SSLA3-B	PA2/A2/MTIOC7A/PO18/GTIOC1A/RXD5/ SMISO5/SSCL5/SSLA3-B/LCD_DATA6-B
G1	XTAL/P37	XTAL/P37
G2	RES	RES#
G3	MD/FINED	MD/FINED
G4	BSCANP	BSCANP
G10	PA5/A5/MTIOC6B/TIOCB1/GTIOC0A-C/ PO21/RSPCKA-B/ET0_LINKSTA	PA5/A5/MTIOC6B/TIOCB1/PO21/GTIOC0A/ RSPCKA-B/ET0_LINKSTA/LCD_DATA3-B
G11	PA6/A6/MTIC5V/MTCLKB/GTETRG-C/ TIOCA2/TMCI3/PO22/POE10#/CTS5#/ RTS5#/SS5#/MOSIA-B/ET0_EXOUT	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/GTETRGB/CTS5#/RTS5#/ SS5#/MOSIA-B/ET0_EXOUT/LCD_DATA2-B
G12	VCC	VCC
G13	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/PMGI0_MDC/LCD_DATA4-B/ IRQ5-DS
H1	EXTAL/P36	EXTAL/P36
H2	VCC	VCC
H3	VSS	VSS
H4	UPSEL/P35/NMI	UPSEL/P35/NMI
H10	P72/A19/CS2#/ET0_MDC	P72/A19/CS2#/ET0_MDC/PMGI0_MDC
H11	P71/A18/CS1#/ET0_MDIO	P71/A18/CS1#/ET0_MDIO/PMGI0_MDIO
H12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/ RXD6/SMISO4/SMISO6/SSCL4/SSCL6/ ET0_ERXD1/RMII0_RXD1/IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/ SMISO4/SSCL4/RXD6/SMISO6/SSCL6/ ET0_ERXD1/RMII0_RXD1/LCD_DATA0-B/ IRQ12
H13	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/ LCD_DATA1-B
J1	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/ET0_LINKSTA/IRQ4	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/ET0_LINKSTA/IRQ4

145-Pin TFLGA	RX64M	RX66N
J2	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/RXD0/ SMISO6/SMISO0/SSCL6/SSCL0/CRX0/ PCKO/IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/SMISO6/ SSCL6/RXD0/SMISO0/SSCL0/CRX0/PCKO/ IRQ3-DS
J3	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCOUT/RTCIC2/POE0#/POE10#/TXD6/ TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCIC2/RTCOUT/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS
J4	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/IRQ0-DS	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS
J10	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ ET0_RX_ER/RMII0_RX_ER	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ ET0_RX_ER/RMII0_RX_ER/LCD_TCON1-B
J11	PB4/A12/TIOCA4/PO28/CTS9#*2/ ET0_TX_EN/RMII0_TXD_EN	PB4/A12/TIOCA4/PO28/CTS9#/SS9#/ SS11#/CTS11#/RTS11#/ET0_TX_EN/ RMII0_TXD_EN/LCD_TCON0-B
J12	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/ RTS4#/CTS6#/RTS6#/SS4#/SS6#/ ET0_RX_CLK/REF50CK0	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/ RTS4#/SS4#/CTS6#/RTS6#/SS6#/ ET0_RX_CLK/REF50CK0/LCD_TCON2-B
J13	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD4/TXD6/SMOSI4/SMOSI6/ SSDA4/SSDA6/ET0_ERXD0/RMII0_RXD0/ IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD4/SMOSI4/SSDA4/TXD6/ SMOSI6/SSDA6/ET0_ERXD0/RMII0_RXD0/ LCD_TCON3-B/IRQ4-DS
K1	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/ SCK1/RSPCKB-A
K2	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ CTS3#/RTS3#/SMOSI1/SS3#/SSDA1	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A
K3	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/IRQ1-DS	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS
K4	P15/MTIOC0B/MTCLKB/GTETRG-B/TIOCB2 /TCLKB/TMCI2/PO13/RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/SSIWS1/PIXD0/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/GTETRGA/RXD1/SMISO1/ SSCL1/SCK3/CRX1-DS/SSILRCK1/ PIXD0/IRQ5
K5	TRDATA2/P54/ALE/EDACK0/MTIOC4B/ TMCI1/CTS2#/RTS2#/SS2#/CTX1/ ET0_LINKSTA	TRDATA2/P54/ALE/D1[A1/D1]/EDACK0/ MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/ CTX1/ET0_LINKSTA
K6	P53*1/BCLK	P53*1/BCLK
K7	P51/WR1#/BC1#/WAIT#/SCK2	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A
K8	VCC	VCC
K9	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/ SCK10*2/RTS10#*2/ET0_TX_EN/ RMII0_TXD_EN/MMC_D2-A/SDHI_WP-A/ QIO2-A	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/ SCK10/RTS10#/ET0_TX_EN/ RMII0_TXD_EN/QIO2-A/SDHI_WP/ MMC_D2-A
K10	P76/CS6#/PO22/RXD11*2/ET0_RX_CLK/ REF50CK0/MMC_CMD-A/SDHI_CMD-A/ QSSL-A	TRDATA6/P76/CS6#/PO22/SMISO11/ SSCL11/RXD11/ET0_RX_CLK/REF50CK0/ QSSL-A/SDHI_CMD-A/MMC_CMD-A
K11	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9*2/ ET0_CRS/RMII0_CRS_DV	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ ET0_CRS/RMII0_CRS_DV

145-Pin TFLGA	RX64M	RX66N
K12	PB6/A14/MTIOC3D/TIOCA5/PO30/ RXD9*2/ET0_ETXD1/RMII0_TXD1	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ ET0_ETXD1/RMII0_TXD1
K13	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9*2/RTS9#*2/ ET0_ETXD0/RMII0_TXD0	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9/RTS9#/SCK11/ ET0_ETXD0/RMII0_TXD0/LCD_CLK-B
L1	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ SSIDATA1/HSYNC/ADTRG0#	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/ MTCLKB/TIOCA4/PO5/RXD3/SMISO3/ SSCL3/SSIDATA1/SDHI_CD/HSYNC/ ADTRG0#
L2	P23/EDACK0/MTIOC3D/MTCLKD/ GTIOC0A-B/TIOCD3/PO3/TXD3/CTS0#/ RTS0#/SMOSI3/SS0#/SSDA3/SSISCK0/ PIXD7	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/GTIOC0A/TXD3/SMOSI3/SSDA3/ CTS0#/RTS0#/SS0#/CTX1/SSIBCK0/ SDHI_D1-C/PIXD7
L3	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/SCL2-DS/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/SMOSI1/ SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/ USB0_VBUSEN/USB0_VBUS/ USB0_OVRCURB/IRQ6/ADTRG0#
L4	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SSISCK1/PIXCLK	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SSIBCK1/SDHI_WP/PIXCLK
L5	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ ADTRG1#	P13/MTIOC0B/TIOCA5/TMO3/PO13/ GTADSM1/TXD2/SMOSI2/SSDA2/ SDA0[FM+]/IRQ3/ADTRG1#
L6	P56/EDACK1/MTIOC3C/TIOCA1	CLKOUT25M/P56/EDACK1/MTIOC3C/ TIOCA1/SCK7
L7	P52/RD#/RXD2/SMISO2/SSCL2	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A
L8	TRCLK/P83/EDACK1/MTIOC4C/ GTIOC0A-D/CTS10#*2/ET0_CRS/ RMII0_CRS_DV/SCK10*2	TRCLK/P83/EDACK1/MTIOC4C/GTIOC0A/ SCK10/SS10#/CTS10#/ET0_CRS/ RMII0_CRS_DV
L9	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/ GTIOC1A-D/TMRI2/PO29/SCK8*2/ RSPCKA-A/RTS8#*2/ET0_ETXD2/ MMC_D5-A	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/GTIOC1A/SCK8/ RTS8#/SCK10/RSPCKA-A/ET0_ETXD2/ MMC_D5-A
L10	PC4/A20/CS3#/MTIOC3D/MTCLKC/ GTETRG-D/TMCI1/PO25/POE0#/SCK5/ CTS8#*2/SSLA0-A/ET0_TX_CLK/ MMC_D1-A/SDHI_D1-A/QIO1-A/QMI-A	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/GTETRGC/SCK5/CTS8#/ SS8#/SS10#/CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK/QMI-A/QIO1-A/SDHI_D1-A/ MMC_D1-A
L11	PC2/A18/MTIOC4B/GTIOC2B-D/TCLKA/ PO21/RXD5/SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV/MMC_CD-A/SDHI_D3-A	PC2/A18/MTIOC4B/TCLKA/PO21/GTIOC2B/ RXD5/SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV/SDHI_D3-A/MMC_CD-A
L12	P73/CS3#/PO16/ET0_WOL	TRDATA4/P73/CS3#/PO16/ET0_WOL
L13	VSS	VSS
M1	P22/EDREQ0/MTIOC3B/MTCLKC/ GTIOC1A-B/TIOCC3/TMO0/PO2/SCK0/ USB0_OVRCURB/AUDIO_MCLK/PIXD6	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/GTIOC1A/SCK0/ USB0_OVRCURB/AUDIO_CLK/ SDHI_D0-C/PIXD6
M2	P17/MTIOC3A/MTIOC3B/MTIOC4B/ GTIOC0B-B/TIOCB0/TCLKD/TMO1/PO15/ POE8#/SCK1/TXD3/SMOSI3/SSDA3/ SDA2-DS/SSITXD0/PIXD3/IRQ7/ADTRG1#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/GTIOC0B/ SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/ SSITXD0/SDHI_D3-C/PIXD3/IRQ7/ ADTRG1#

145-Pin TFLGA	RX64M	RX66N
M3	P86/MTIOC4D/GTIOC2B-B/TIOCA0/ RXD10*2/PIXD1	P86/MTIOC4D/TIOCA0/GTIOC2B/SMISO10/ SSCL10/RXD10/PIXD1
M4	P12/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/IRQ2	P12/TMCI1/GTADSM0/RXD2/SMISO2/ SSCL2/SCL0[FM+]/IRQ2
M5	VCC_USB	VCC_USB
M6	VSS_USB	VSS_USB
M7	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A
M8	PC6/A22/CS1#/MTIOC3C/MTCLKA/ GTIOC3B-D/TMCI2/TIC0/PO30/RXD8*2/ MOSIA-A/ET0_ETXD3/MMC_D6-A/IRQ13	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/PO30/TIC0/GTIOC3B/ RXD8/SMISO8/SSCL8/SMISO10/SSCL10/ RXD10/MOSIA-A/ET0_ETXD3/MMC_D6-A/ IRQ13
M9	TRDATA1/P81/EDACK0/MTIOC3D/ GTIOC0B-D/PO27/RXD10*2/ET0_ETXD0/ RMII0_TXD0/MMC_D3-A/SDHI_CD-A/ QIO3-A	TRDATA1/P81/EDACK0/MTIOC3D/PO27/ GTIOC0B/SMISO10/SSCL10/ RXD10/ET0_ETXD0/RMII0_TXD0/QIO3-A/ SDHI_CD/MMC_D3-A
M10	P77/CS7#/PO23/TXD11*2/ET0_RX_ER/ RMII0_RX_ER/MMC_CLK-A/SDHI_CLK-A/ QSPCLK-A	TRDATA7/P77/CS7#/PO23/SMOSI11/ SSDA11/TXD11/ET0_RX_ER/ RMII0_RX_ER/QSPCLK-A/SDHI_CLK-A/ MMC_CLK-A
M11	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14
M12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/IRQ12
M13	VCC	VCC
N1	P21/MTIOC1B/MTIOC4A/GTIOC2A-B/ TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/ USB0_EXICEN/SSIWS0/PIXD5/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/GTIOC2A/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/SDHI_CLK-C/ PIXD5/IRQ9
N2	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/USB0_ID/SSIRXD0/PIXD4/ IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMD-C/PIXD4/IRQ8
N3	P87/MTIOC4C/GTIOC1B-B/TIOCA2/ TXD10*2/PIXD2	P87/MTIOC4C/TIOCA2/GTIOC1B/SMOSI10/ SSDA10/TXD10/SDHI_D2-C/PIXD2
N4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/GTETRGD/CTS1#/RTS1#/ SS1#/CTX1/USB0_OVRCURA/IRQ4
N5	USB0_DM	USB0_DM
N6	USB0_DP	USB0_DP
N7	TRDATA3/P55/WAIT#/EDREQ0/MTIOC4D/ TMO3/CRX1/ET0_EXOUT/IRQ10	TRDATA3/P55/D0[A0/D0]/WAIT#/EDREQ0/ MTIOC4D/TMO3/TXD7/SMOSI7/SSDA7/ CRX1/ET0_EXOUT/IRQ10
N8	VSS	VSS
N9	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ GTIOC3A-D/TMO2/TOC0/PO31/CACREF/ TXD8*2/MISOA-A/ET0_COL/MMC_D7-A/ IRQ14	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/PO31/TOC0/CACREF/GTIOC3A/ TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/ET0_COL/MMC_D7-A/ IRQ14
N10	TRSYNC/P82/EDREQ1/MTIOC4A/ GTIOC2A-D/PO28/TXD10*2/ET0_ETXD1/ RMII0_TXD1/MMC_D4-A	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/ GTIOC2A/SMOSI10/SSDA10/ TXD10/ET0_ETXD1/RMII0_TXD1/ MMC_D4-A

145-Pin TFLGA	RX64M	RX66N
N11	PC3/A19/MTIOC4D/GTIOC1B-D/TCLKB/ PO24/TXD5/SMOSI5/SSDA5/ET0_TX_ER/ MMC_D0-A/SDHI_D0-A/QIO0-A/QMO-A	PC3/A19/MTIOC4D/TCLKB/PO24/GTIOC1B/ TXD5/SMOSI5/SSDA5/ET0_TX_ER/QMO-A/ QIO0-A/SDHI_D0-A/MMC_D0-A
N12	P75/CS5#/PO20/SCK11*2/RTS11#*2/ ET0_ERXD0/RMII0_RXD0/MMC_RES#-A/ SDHI_D2-A	TRSYNC1/P75/CS5#/PO20/SCK11/RTS11#/ ET0_ERXD0/RMII0_RXD0/SDHI_D2-A/ MMC_RES#-A
N13	P74/A20/CS4#/PO19/CTS11#*2/ ET0_ERXD1/RMII0_RXD1	TRDATA5/P74/A20/CS4#/PO19/SS11#/ CTS11#/ET0_ERXD1/RMII0_RXD1

Notes: 1. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.
2. Pins for FIFO embedded serial communications interface (SCIFA).

3.4 144-Pin LFQFP Package

Table 3.4 is a comparative listing of the pin functions of 144-pin LFQFP package products.

Table 3.4 Comparative Listing of 144-Pin LFQFP Package Pin Functions

144-Pin LFQFP	RX64M	RX66N
1	AVSS0	AVSS0
2	P05/IRQ13/DA1	P05/SSILRCK1/IRQ13/DA1
3	AVCC1	AVCC1
4	P03/IRQ11/DA0	P03/SSIDATA1/IRQ11/DA0
5	AVSS1	AVSS1
6	P02/TMCI1/SCK6/IRQ10/AN120	P02/TMCI1/SCK6/SSIBCK1/IRQ10/AN120
7	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/ AN119	P01/TMCI0/RXD6/SMISO6/SSCL6/ SSIBCK0/IRQ9/AN119
8	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/ AN118	P00/TMRI0/TXD6/SMOSI6/SSDA6/ AUDIO_CLK/IRQ8/AN118
9	PF5/IRQ4	PF5/WAIT#/SSILRCK0/IRQ4
10	EMLE	EMLE
11	PJ5/POE8#/CTS2#/RTS2#/SS2#	PJ5/POE8#/CTS2#/RTS2#/SS2#/SSIRXD0
12	VSS	VSS
13	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/ CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0#	PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/ SS6#/CTS0#/RTS0#/SS0#/SSITXD0/ ET0_EXOUT
14	VCL	VCL
15	VBATT	VBATT
16	MD/FINED	MD/FINED
17	XCIN	XCIN
18	XCOUT	XCOUT
19	RES	RES#
20	XTAL/P37	XTAL/P37
21	VSS	VSS
22	EXTAL/P36	EXTAL/P36
23	VCC	VCC
24	UPSEL/P35/NMI	UPSEL/P35/NMI
25	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/ET0_LINKSTA/IRQ4	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/ET0_LINKSTA/IRQ4
26	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/RXD0/ SMISO6/SMISO0/SSCL6/SSCL0/CRX0/ PCKO/IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/SMISO6/ SSCL6/RXD0/SMISO0/SSCL0/CRX0/PCKO/ IRQ3-DS
27	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCOUT/RTCIC2/POE0#/POE10#/TXD6/ TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCIC2/RTCOUT/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS
28	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/IRQ1-DS	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS
29	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/IRQ0-DS	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS
30	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/ SCK1/RSPCKB-A

144-Pin LFQFP	RX64M	RX66N
31	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ CTS3#/RTS3#/SMOSI1/SS3#/SSDA1	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A
32	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ SSIDATA1/HSYNC/ADTRG0#	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/ MTCLKB/TIOCA4/PO5/RXD3/SMISO3/ SSCL3/SSIDATA1/SDHI_CD/HSYNC/ ADTRG0#
33	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SSISCK1/PIXCLK	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SSIBCK1/SDHI_WP/PIXCLK
34	P23/EDACK0/MTIOC3D/MTCLKD/ GTIOC0A-B/TIOCD3/PO3/TXD3/CTS0#/ RTS0#/SMOSI3/SS0#/SSDA3/SSISCK0/ PIXD7	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/GTIOC0A/TXD3/SMOSI3/SSDA3/ CTS0#/RTS0#/SS0#/CTX1/SSIBCK0/ SDHI_D1-C/PIXD7
35	P22/EDREQ0/MTIOC3B/MTCLKC/ GTIOC1A-B/TIOCC3/TMO0/PO2/SCK0/ USB0_OVRCURB/AUDIO_MCLK/PIXD6	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/GTIOC1A/SCK0/ USB0_OVRCURB/AUDIO_CLK/SDHI_D0-C/ PIXD6
36	P21/MTIOC1B/MTIOC4A/GTIOC2A-B/ TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/ USB0_EXICEN/SSIWS0/PIXD5/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/GTIOC2A/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/SDHI_CLK-C/ PIXD5/IRQ9
37	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/USB0_ID/SSIRXD0/PIXD4/ IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMD-C/PIXD4/IRQ8
38	P17/MTIOC3A/MTIOC3B/MTIOC4B/ GTIOC0B-B/TIOCB0/TCLKD/TMO1/PO15/ POE8#/SCK1/TXD3/SMOSI3/SSDA3/ SDA2-DS/SSITXD0/PIXD3/IRQ7/ADTRG1#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/GTIOC0B/ SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/ SSITXD0/SDHI_D3-C/PIXD3/IRQ7/ ADTRG1#
39	P87/MTIOC4C/GTIOC1B-B/TIOCA2/ TXD10*2/PIXD2	P87/MTIOC4C/TIOCA2/GTIOC1B/SMOSI10/ SSDA10/TXD10/SDHI_D2-C/PIXD2
40	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/SCL2-DS/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/SMOSI1/ SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/ USB0_VBUSEN/USB0_VBUS/ USB0_OVRCURB/IRQ6/ADTRG0#
41	P86/MTIOC4D/GTIOC2B-B/TIOCA0/ RXD10*2/PIXD1	P86/MTIOC4D/TIOCA0/GTIOC2B/SMISO10/ SSCL10/RXD10/PIXD1
42	P15/MTIOC0B/MTCLKB/GTETRG-B/ TIOCB2/TCLKB/TMCI2/PO13/RXD1/SCK3/ SMISO1/SSCL1/CRX1-DS/SSIWS1/PIXD0/ IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/GTETRGA/RXD1/SMISO1/ SSCL1/SCK3/CRX1-DS/SSILRCK1/ PIXD0/IRQ5
43	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/GTETRGD/CTS1#/RTS1#/ SS1#/CTX1/USB0_OVRCURA/IRQ4
44	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ ADTRG1#	P13/MTIOC0B/TIOCA5/TMO3/PO13/ GTADSM1/TXD2/SMOSI2/SSDA2/ SDA0[FM+]/IRQ3/ADTRG1#
45	P12/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/IRQ2	P12/TMCI1/GTADSM0/RXD2/SMISO2/ SSCL2/SCL0[FM+]/IRQ2
46	VCC_USB	VCC_USB
47	USB0_DM	USB0_DM
48	USB0_DP	USB0_DP

144-Pin LFQFP	RX64M	RX66N
49	VSS_USB	VSS_USB
50	P56/EDACK1/MTIOC3C/TIOCA1	CLKOUT25M/P56/EDACK1/MTIOC3C/ TIOCA1/SCK7
51	TRDATA3/P55/WAIT#/EDREQ0/MTIOC4D/ TMO3/CRX1/ET0_EXOUT/IRQ10	TRDATA3/P55/D0[A0/D0]/WAIT#/EDREQ0/ MTIOC4D/TMO3/TXD7/SMOSI7/SSDA7/ CRX1/ET0_EXOUT/IRQ10
52	TRDATA2/P54/ALE/EDACK0/MTIOC4B/ TMCI1/CTS2#/RTS2#/SS2#/CTX1/ ET0_LINKSTA	TRDATA2/P54/ALE/D1[A1/D1]/EDACK0/ MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/ CTX1/ET0_LINKSTA
53	P53*1/BCLK	P53*1/BCLK
54	P52/RD#/RXD2/SMISO2/SSCL2	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A
55	P51/WR1#/BC1#/WAIT#/SCK2	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A
56	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A
57	VSS	VSS
58	TRCLK/P83/EDACK1/MTIOC4C/ GTIOC0A-D/CTS10#*2/ET0_CRS/ RMII0_CRS_DV/SCK10*2	TRCLK/P83/EDACK1/MTIOC4C/GTIOC0A/ SCK10/SS10#/CTS10#/ET0_CRS/ RMII0_CRS_DV
59	VCC	VCC
60	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ GTIOC3A-D/TMO2/TOC0/PO31/CACREF/ TXD8*2/MISOA-A/ET0_COL/MMC_D7-A/ IRQ14	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/PO31/TOC0/CACREF/GTIOC3A/ TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/ET0_COL/MMC_D7-A/ IRQ14
61	PC6/A22/CS1#/MTIOC3C/MTCLKA/ GTIOC3B-D/TMCI2/TIC0/PO30/RXD8*2/ MOSIA-A/ET0_ETXD3/MMC_D6-A/IRQ13	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/PO30/TIC0/GTIOC3B/ RXD8/SMISO8/SSCL8/SMISO10/SSCL10/ RXD10/MOSIA-A/ET0_ETXD3/MMC_D6-A/ IRQ13
62	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/ GTIOC1A-D/TMRI2/PO29/ SCK8*2/RSPCKA-A/RTS8#*2/ ET0_ETXD2/MMC_D5-A	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/GTIOC1A/SCK8/ RTS8#/SCK10/RSPCKA-A/ET0_ETXD2/ MMC_D5-A
63	TRSYNC/P82/EDREQ1/MTIOC4A/ GTIOC2A-D/PO28/TXD10*2/ET0_ETXD1/ RMII0_TXD1/MMC_D4-A	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/ GTIOC2A/SMOSI10/SSDA10/TXD10/ ET0_ETXD1/RMII0_TXD1/MMC_D4-A
64	TRDATA1/P81/EDACK0/MTIOC3D/ GTIOC0B-D/PO27/RXD10*2/ET0_ETXD0/ RMII0_TXD0/MMC_D3-A/SDHI_CD-A/ QIO3-A	TRDATA1/P81/EDACK0/MTIOC3D/PO27/ GTIOC0B/SMISO10/SSCL10/RXD10/ ET0_ETXD0/RMII0_TXD0/QIO3-A/ SDHI_CD/MMC_D3-A
65	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/ SCK10*2/RTS10#*2/ET0_TX_EN/ RMII0_TXD_EN/MMC_D2-A/SDHI_WP-A/ QIO2-A	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/ SCK10/RTS10#/ET0_TX_EN/ RMII0_TXD_EN/QIO2-A/SDHI_WP/ MMC_D2-A
66	PC4/A20/CS3#/MTIOC3D/MTCLKC/ GTETRG-D/TMCI1/PO25/POE0#/SCK5/ CTS8#*2/SSLA0-A/ET0_TX_CLK/ MMC_D1-A/SDHI_D1-A/QIO1-A/QMI-A	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/GTETRGC/SCK5/CTS8#/ SS8#/SS10#/CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK/QMI-A/QIO1-A/SDHI_D1-A/ MMC_D1-A
67	PC3/A19/MTIOC4D/GTIOC1B-D/TCLKB/ PO24/TXD5/SMOSI5/SSDA5/ET0_TX_ER/ MMC_D0-A/SDHI_D0-A/QIO0-A/QMO-A	PC3/A19/MTIOC4D/TCLKB/PO24/GTIOC1B/ TXD5/SMOSI5/SSDA5/ET0_TX_ER/QMO-A/ QIO0-A/SDHI_D0-A/MMC_D0-A

144-Pin LFQFP	RX64M	RX66N
68	P77/CS7#/PO23/TXD11*2/ET0_RX_ER/ RMII0_RX_ER/MMC_CLK-A/SDHI_CLK-A/ QSPCLK-A	TRDATA7/P77/CS7#/PO23/SMOSI11/ SSDA11/TXD11/ET0_RX_ER/ RMII0_RX_ER/QSPCLK-A/SDHI_CLK-A/ MMC_CLK-A
69	P76/CS6#/PO22/RXD11*2/ET0_RX_CLK/ REF50CK0/MMC_CMD-A/SDHI_CMD-A/ QSSL-A	TRDATA6/P76/CS6#/PO22/SMISO11/ SSCL11/RXD11/ET0_RX_CLK/REF50CK0/ QSSL-A/SDHI_CMD-A/MMC_CMD-A
70	PC2/A18/MTIOC4B/GTIOC2B-D/TCLKA/ PO21/RXD5/SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV/MMC_CD-A/SDHI_D3-A	PC2/A18/MTIOC4B/TCLKA/PO21/GTIOC2B/ RXD5/SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV/SDHI_D3-A/MMC_CD-A
71	P75/CS5#/PO20/SCK11*2/RTS11#*2/ ET0_ERXD0/RMII0_RXD0/MMC_RES#-A/ SDHI_D2-A	TRSYNC1/P75/CS5#/PO20/SCK11/RTS11#/ ET0_ERXD0/RMII0_RXD0/SDHI_D2-A/ MMC_RES#-A
72	P74/A20/CS4#/PO19/CTS11#*2/ ET0_ERXD1/RMII0_RXD1	TRDATA5/P74/A20/CS4#/PO19/SS11#/ CTS11#/ET0_ERXD1/RMII0_RXD1
73	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/IRQ12
74	VCC	VCC
75	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14
76	VSS	VSS
77	P73/CS3#/PO16/ET0_WOL	TRDATA4/P73/CS3#/PO16/ET0_WOL
78	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9*2/ ET0_CRS/RMII0_CRS_DV	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ ET0_CRS/RMII0_CRS_DV
79	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9*2/ ET0_ETXD1/RMII0_TXD1	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ ET0_ETXD1/RMII0_TXD1
80	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9*2/RTS9#*2/ ET0_ETXD0/RMII0_TXD0	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9/RTS9#/SCK11/ ET0_ETXD0/RMII0_TXD0/LCD_CLK-B
81	PB4/A12/TIOCA4/PO28/CTS9#*2/ ET0_TX_EN/RMII0_TXD_EN	PB4/A12/TIOCA4/PO28/CTS9#/SS9#/ SS11#/CTS11#/RTS11#/ET0_TX_EN/ RMII0_TXD_EN/LCD_TCON0-B
82	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ ET0_RX_ER/RMII0_RX_ER	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ ET0_RX_ER/RMII0_RX_ER/LCD_TCON1-B
83	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/ RTS4#/CTS6#/RTS6#/SS4#/SS6#/ ET0_RX_CLK/REF50CK0	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/ RTS4#/SS4#/CTS6#/RTS6#/SS6#/ ET0_RX_CLK/REF50CK0/LCD_TCON2-B
84	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD4/TXD6/SMOSI4/SMOSI6/ SSDA4/SSDA6/ET0_ERXD0/RMII0_RXD0/ IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD4/SMOSI4/SSDA4/TXD6/ SMOSI6/SSDA6/ET0_ERXD0/RMII0_RXD0/ LCD_TCON3-B/IRQ4-DS
85	P72/A19/CS2#/ET0_MDC	P72/A19/CS2#/ET0_MDC/PMGI0_MDC
86	P71/A18/CS1#/ET0_MDIO	P71/A18/CS1#/ET0_MDIO/PMGI0_MDIO
87	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/ RXD6/SMISO4/SMISO6/SSCL4/SSCL6/ ET0_ERXD1/RMII0_RXD1/IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/ SMISO4/SSCL4/RXD6/SMISO6/SSCL6/ ET0_ERXD1/RMII0_RXD1/LCD_DATA0-B/ IRQ12
88	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/ LCD_DATA1-B

144-Pin LFQFP	RX64M	RX66N
89	PA6/A6/MTIC5V/MTCLKB/GTETRG-C/ TIOCA2/TMCI3/PO22/POE10#/CTS5#/ RTS5#/SS5#/MOSIA-B/ET0_EXOUT	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/GTETRGB/CTS5#/RTS5#/ SS5#/MOSIA-B/ET0_EXOUT/LCD_DATA2-B
90	PA5/A5/MTIOC6B/TIOCB1/GTIOC0A-C/ PO21/RSPCKA-B/ET0_LINKSTA	PA5/A5/MTIOC6B/TIOCB1/PO21/GTIOC0A/ RSPCKA-B/ET0_LINKSTA/LCD_DATA3-B
91	VCC	VCC
92	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/PMGI0_MDC/LCD_DATA4-B/ IRQ5-DS
93	VSS	VSS
94	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ ET0_MDIO/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ ET0_MDIO/PMGI0_MDIO/LCD_DATA5-B/ IRQ6-DS
95	PA2/A2/MTIOC7A/GTIOC1A-C/PO18/ RXD5/SMISO5/SSCL5/SSLA3-B	PA2/A2/MTIOC7A/PO18/GTIOC1A/RXD5/ SMISO5/SSCL5/SSLA3-B/LCD_DATA6-B
96	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ GTIOC2A-C/TIOCB0/PO17/SCK5/SSLA2-B/ ET0_WOL/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/GTIOC2A/SCK5/SSLA2-B/ ET0_WOL/LCD_DATA7-B/IRQ11
97	PA0/A0/BC0#/MTIOC4A/MTIOC6D/ GTIOC0B-C/TIOCA0/CACREF/PO16/ SSLA1-B/ET0_TX_EN/RMII0_TXD_EN	PA0/BC0#/A0/MTIOC4A/MTIOC6D/TIOCA0/ PO16/CACREF/GTIOC0B/SSLA1-B/ ET0_TX_EN/RMII0_TXD_EN/LCD_DATA8-B
98	P67/CS7#/DQM1/MTIOC7C/GTIOC1B-C/ CRX2/IRQ15	P67/DQM1/CS7#/MTIOC7C/GTIOC1B/ CRX2/IRQ15
99	P66/CS6#/DQM0/MTIOC7D/GTIOC2B-C/ CTX2	P66/DQM0/CS6#/MTIOC7D/GTIOC2B/CTX2
100	P65/CS5#/CKE	P65/CKE/CS5#
101	PE7/D15[A15/D15]/MTIOC6A/GTIOC3A-E/ TOC1/MMC_RES#-B/SDHI_WP-B/IRQ7/ AN105	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/GTIOC3A/MISOB-B/SDHI_WP/ MMC_RES#-B/LCD_DATA9-B/IRQ7/AN105
102	PE6/D14[A14/D14]/MTIOC6C/GTIOC3B-E/ TIC1/MMC_CD-B/SDHI_CD-B/IRQ6/AN104	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/GTIOC3B/MOSIB-B/SDHI_CD/ MMC_CD-B/LCD_DATA10-B/IRQ6/AN104
103	VCC	VCC
104	P70/SDCLK	P70/SDCLK
105	VSS	VSS
106	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/ GTIOC0A-A/ET0_RX_CLK/REF50CK0/ IRQ5/AN103	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/RSPCKB-B/ ET0_RX_CLK/REF50CK0/LCD_DATA11-B/ IRQ5/AN103
107	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/ GTIOC1A-A/PO28/ET0_ERXD2/AN102	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/SSLB0-B/ ET0_ERXD2/LCD_DATA12-B/AN102
108	PE3/D11[A11/D11]/MTIOC4B/GTIOC2A-A/ PO26/POE8#/TOC3/CTS12#/RTS12#/ SS12#/ET0_ERXD3/MMC_D7-B/AN101	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/TOC3/POE8#/GTIOC2A/CTS12#/ RTS12#/SS12#/ET0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101
109	PE2/D10[A10/D10]/MTIOC4A/GTIOC0B-A/ PO23/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/MMC_D6-B/IRQ7-DS/AN100	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/GTIOC0B/RXD12/SMISO12/ SSCL12/RXDX12/SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/AN100

144-Pin LFQFP	RX64M	RX66N
110	PE1/D9[A9/D9]/MTIOC4C/MTIOC3B/ GTIOC1B-A/PO18/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/MMC_D5-B/ ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/GTIOC1B/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLB2-B/MMC_D5-B/LCD_DATA15-B/ ANEX1
111	PE0/D8[A8/D8]/MTIOC3D/GTIOC2B-A/ SCK12/MMC_D4-B/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/ GTIOC2B/SCK12/SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0
112	P64/CS4#/WE#	P64/WE#/D3[A3/D3]/CS4#
113	P63/CS3#/CAS#	P63/CAS#/D2[A2/D2]/CS3#
114	P62/CS2#/RAS#	P62/RAS#/D1[A1/D1]/CS2#
115	P61/CS1#/SDCS#	P61/SDCS#/D0[A0/D0]/CS1#
116	VSS	VSS
117	P60/CS0#	P60/CS0#
118	VCC	VCC
119	PD7/D7[A7/D7]/MTIC5U/POE0#/MMC_D1-B/ SDHI_D1-B/QIO1-B/QMI-B/IRQ7/AN107	PD7/D7[A7/D7]/MTIC5U/POE0#/ SSLC3-A/QMI-B/QIO1-B/SDHI_D1-B/ MMC_D1-B/LCD_DATA17-B/IRQ7/AN107
120	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ MMC_D0-B/SDHI_D0-B/QIO0-B/QMO-B/ IRQ6/AN106	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/IRQ6/AN106
121	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/ MMC_CLK-B/SDHI_CLK-B/QSPCLK-B/ IRQ5/AN113	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/ MTCLKA/POE10#/SSLC1-A/QSPCLK-B/ SDHI_CLK-B/MMC_CLK-B/LCD_DATA19-B/ IRQ5/AN113
122	PD4/D4[A4/D4]/MTIOC8B/POE11#/ MMC_CMD-B/SDHI_CMD-B/QSSL-B/IRQ4/ AN112	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/QSSL-B/SDHI_CMD-B/ MMC_CMD-B/LCD_DATA20-B/IRQ4/AN112
123	PD3/D3[A3/D3]/MTIOC8D/GTIOC0A-E/ POE8#/TOC2/MMC_D3-B/SDHI_D3-B/ QIO3-B/IRQ3/AN111	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ GTIOC0A/RSPCKC-A/QIO3-B/SDHI_D3-B/ MMC_D3-B/LCD_DATA21-B/IRQ3/AN111
124	PD2/D2[A2/D2]/MTIOC4D/GTIOC0B-E/TIC2/ CRX0/MMC_D2-B/SDHI_D2-B/QIO2-B/ IRQ2/AN110	PD2/D2[A2/D2]/MTIOC4D/TIC2/GTIOC0B/ MISOC-A/CRX0/QIO2-B/SDHI_D2-B/ MMC_D2-B/LCD_DATA22-B/IRQ2/AN110
125	PD1/D1[A1/D1]/MTIOC4B/GTIOC1A-E/ POE0#/CTX0/IRQ1/AN109	PD1/D1[A1/D1]/MTIOC4B/POE0#/GTIOC1A/ MOSIC-A/CTX0/LCD_DATA23-B/IRQ1/ AN109
126	PD0/D0[A0/D0]/GTIOC1B-E/POE4#/IRQ0/ AN108	PD0/D0[A0/D0]/POE4#/GTIOC1B/ LCD_EXTCLK-B/IRQ0/AN108
127	P93/A19/POE0#/CTS7#/RTS7#/SS7#/AN117	P93/A19/POE0#/CTS7#/RTS7#/SS7#/AN117
128	P92/A18/POE4#/RXD7/SMISO7/SSCL7/ AN116	P92/A18/POE4#/RXD7/SMISO7/SSCL7/ AN116
129	P91/A17/SCK7/AN115	P91/A17/SCK7/AN115
130	VSS	VSS
131	P90/A16/TXD7/SMOSI7/SSDA7/AN114	P90/A16/TXD7/SMOSI7/SSDA7/AN114
132	VCC	VCC
133	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
134	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
135	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
136	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
137	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
138	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002

144-Pin LFQFP	RX64M	RX66N
139	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
140	VREFL0	VREFL0
141	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
142	VREFH0	VREFH0
143	AVCC0	AVCC0
144	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#

Notes: 1. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.
2. Pins for FIFO embedded serial communications interface (SCIFA).

3.5 100-Pin LFQFP Package

Table 3.5 is a comparative listing of the pin functions of 100-pin LFQFP package products.

Table 3.5 Comparative Listing of 100-Pin LFQFP Package Pin Functions

100-Pin LFQFP	RX64M	RX66N
1	AVCC1	AVCC1
2	EMLE	EMLE
3	AVSS1	AVSS1
4	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/ CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0#	PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/ SS6#/CTS0#/RTS0#/SS0#/SSITXD0/ ET0_EXOUT
5	VCL	VCL
6	VBATT	VBATT
7	MD/FINED	MD/FINED
8	XCIN	XCIN
9	XCOUT	XCOUT
10	RES#	RES#
11	XTAL/P37	XTAL/P37
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36
14	VCC	VCC
15	UPSEL/P35/NMI	UPSEL/P35/NMI
16	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/ET0_LINKSTA/IRQ4	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/ET0_LINKSTA/IRQ4
17	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/RXD0/ SMISO6/SMISO0/SSCL6/SSCL0/CRX0/ IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/SMISO6/ SSCL6/RXD0/SMISO0/SSCL0/CRX0/ IRQ3-DS
18	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCOUT/RTCIC2/POE0#/POE10#/TXD6/ TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCIC2/RTCOUT/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/IRQ2-DS
19	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/IRQ1-DS	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS
20	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/IRQ0-DS	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS
21	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/ RSPCKB-A
22	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ CTS3#/RTS3#/SMOSI1/SS3#/SSDA1	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A
23	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ SSIDATA1/ADTRG0#	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/ MTCLKB/TIOCA4/PO5/RXD3/SMISO3/ SSCL3/SSIDATA1/ADTRG0#
24	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SSISCK1	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SSIBCK1
25	P23/EDACK0/MTIOC3D/MTCLKD/ GTIOC0A-B/TIOCD3/PO3/TXD3/CTS0#/ RTS0#/SMOSI3/SS0#/SSDA3/SSISCK0	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/GTIOC0A/TXD3/SMOSI3/SSDA3/ CTS0#/RTS0#/SS0#/CTX1/SSIBCK0

100-Pin LFQFP	RX64M	RX66N
26	P22/EDREQ0/MTIOC3B/MTCLKC/ GTIOC1A-B/TIOCC3/TMO0/PO2/SCK0/ USB0_OVRCURB/AUDIO_MCLK	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/GTIOC1A/SCK0/ USB0_OVRCURB/AUDIO_CLK
27	P21/MTIOC1B/MTIOC4A/GTIOC2A-B/ TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/ USB0_EXICEN/SSIWS0/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/GTIOC2A/RXD0/SMISO0/SSCL0/ USB0_EXICEN/SSILRCK0/SCL1/IRQ9
28	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/USB0_ID/SSIRXD0/IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/USB0_ID/SSIRXD0/SDA1/ IRQ8
29	P17/MTIOC3A/MTIOC3B/MTIOC4B/ GTIOC0B-B/TIOCB0/TCLKD/TMO1/PO15/ POE8#/SCK1/TXD3/SMOSI3/SSDA3/ SDA2-DS/SSITXD0/IRQ7/ADTRG1#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/GTIOC0B/ SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/ SSITXD0/IRQ7/ADTRG1#
30	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/SCL2-DS/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/SMOSI1/ SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/ USB0_VBUSEN/USB0_VBUS/ USB0_OVRCURB/IRQ6/ADTRG0#
31	P15/MTIOC0B/MTCLKB/GTETRG-B/ TIOCB2/TCLKB/TMCI2/PO13/RXD1/SCK3/ SMISO1/SSCL1/CRX1-DS/SSIWS1/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/GTETRGA/RXD1/SMISO1/ SSCL1/SCK3/CRX1-DS/SSILRCK1/IRQ5
32	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/GTETRGD/CTS1#/RTS1#/ SS1#/CTX1/USB0_OVRCURA/IRQ4
33	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ ADTRG1#	P13/MTIOC0B/TIOCA5/TMO3/PO13/ GTADSM1/TXD2/SMOSI2/SSDA2/ SDA0[FM+]/IRQ3/ADTRG1#
34	P12/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/IRQ2	P12/TMCI1/GTADSM0/RXD2/SMISO2/ SSCL2/SCL0[FM+]/IRQ2
35	VCC_USB	VCC_USB
36	USB0_DM	USB0_DM
37	USB0_DP	USB0_DP
38	VSS_USB	VSS_USB
39	P55/WAIT#/EDREQ0/MTIOC4D/TMO3/ CRX1/ET0_EXOUT/IRQ10	P55/D0[A0/D0]/WAIT#/EDREQ0/MTIOC4D/ TMO3/CRX1/ET0_EXOUT/IRQ10
40	P54/ALE/EDACK0/MTIOC4B/TMCI1/CTS2#/ RTS2#/SS2#/CTX1/ET0_LINKSTA	P54/ALE/D1[A1/D1]/EDACK0/MTIOC4B/ TMCI1/CTS2#/RTS2#/SS2#/CTX1/ ET0_LINKSTA
41	P53*1/BCLK	P53*1/BCLK
42	P52/RD#/RXD2/SMISO2/SSCL2	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A
43	P51/WR1#/BC1#/WAIT#/SCK2	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A
44	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A
45	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ GTIOC3A-D/TMO2/TOC0/PO31/CACREF/ TXD8*2/MISOA-A/ET0_COL/IRQ14	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/PO31/TOC0/CACREF/GTIOC3A/ TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/ET0_COL/IRQ14
46	PC6/A22/CS1#/MTIOC3C/MTCLKA/ GTIOC3B-D/TMCI2/TIC0/PO30/RXD8*2/ MOSIA-A/ET0_ETXD3/IRQ13	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/PO30/TIC0/GTIOC3B/ RXD8/SMISO8/SSCL8/SMISO10/SSCL10/ RXD10/MOSIA-A/ET0_ETXD3/IRQ13

100-Pin LFQFP	RX64M	RX66N
47	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/ GTIOC1A-D/TMRI2/PO29/ SCK8*2/RSPCKA-A/RTS8#*2/ ET0_ETXD2	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/GTIOC1A/SCK8/ RTS8#/SCK10/RSPCKA-A/ET0_ETXD2
48	PC4/A20/CS3#/MTIOC3D/MTCLKC/ GTETRG-D/TMCI1/PO25/POE0#/SCK5/ CTS8#*2/SSLA0-A/ET0_TX_CLK	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/GTETRGC/SCK5/CTS8#/ SS8#/SS10#/CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK
49	PC3/A19/MTIOC4D/GTIOC1B-D/TCLKB/ PO24/TXD5/SMOSI5/SSDA5/ET0_TX_ER	PC3/A19/MTIOC4D/TCLKB/PO24/GTIOC1B/ TXD5/SMOSI5/SSDA5/ET0_TX_ER
50	PC2/A18/MTIOC4B/GTIOC2B-D/TCLKA/ PO21/RXD5/SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV	PC2/A18/MTIOC4B/TCLKA/PO21/GTIOC2B/ RXD5/SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV
51	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/IRQ12
52	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14
53	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9*2/ ET0_CRS/RMII0_CRS_DV	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ ET0_CRS/RMII0_CRS_DV
54	PB6/A14/MTIOC3D/TIOCA5/PO30/ RXD9*2/ET0_ETXD1/RMII0_TXD1	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ ET0_ETXD1/RMII0_TXD1
55	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9*2/RTS9#*2/ ET0_ETXD0/RMII0_TXD0	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9/RTS9#/SCK11/ ET0_ETXD0/RMII0_TXD0/LCD_CLK-B
56	PB4/A12/TIOCA4/PO28/CTS9#*2/ ET0_TX_EN/RMII0_TXD_EN	PB4/A12/TIOCA4/PO28/CTS9#/SS9#/ SS11#/CTS11#/RTS11#/ET0_TX_EN/ RMII0_TXD_EN/LCD_TCON0-B
57	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK6/ ET0_RX_ER/RMII0_RX_ER	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK6/ ET0_RX_ER/RMII0_RX_ER/LCD_TCON1-B
58	PB2/A10/TIOCC3/TCLKC/PO26/CTS6#/ RTS6#/SS6#/ET0_RX_CLK/REF50CK0	PB2/A10/TIOCC3/TCLKC/PO26/CTS6#/ RTS6#/SS6#/ET0_RX_CLK/REF50CK0/ LCD_TCON2-B
59	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD6/SMOSI6/SSDA6/ ET0_ERXD0/RMII0_RXD0/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD6/SMOSI6/SSDA6/ ET0_ERXD0/RMII0_RXD0/LCD_TCON3-B/ IRQ4-DS
60	VCC	VCC
61	PB0/A8/MTIC5W/TIOCA3/PO24/RXD6/ SMISO6/SSCL6/ET0_ERXD1/RMII0_RXD1/ IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD6/ SMISO6/SSCL6/ET0_ERXD1/RMII0_RXD1/ LCD_DATA0-B/IRQ12
62	VSS	VSS
63	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/ LCD_DATA1-B
64	PA6/A6/MTIC5V/MTCLKB/GTETRG-C/ TIOCA2/TMCI3/PO22/POE10#/CTS5#/ RTS5#/SS5#/MOSIA-B/ET0_EXOUT	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/GTETRGB/CTS5#/RTS5#/ SS5#/MOSIA-B/ET0_EXOUT/LCD_DATA2-B
65	PA5/A5/MTIOC6B/TIOCB1/GTIOC0A-C/ PO21/RSPCKA-B/ET0_LINKSTA	PA5/A5/MTIOC6B/TIOCB1/PO21/GTIOC0A/ RSPCKA-B/ET0_LINKSTA/LCD_DATA3-B

100-Pin LFQFP	RX64M	RX66N
66	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/PMGI0_MDC/LCD_DATA4-B/ IRQ5-DS
67	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ ET0_MDIO/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ ET0_MDIO/PMGI0_MDIO/LCD_DATA5-B/ IRQ6-DS
68	PA2/A2/MTIOC7A/GTIOC1A-C/PO18/RXD5/ SMISO5/SSCL5/SSLA3-B	PA2/A2/MTIOC7A/PO18/GTIOC1A/RXD5/ SMISO5/SSCL5/SSLA3-B/LCD_DATA6-B
69	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ GTIOC2A-C/TIOCB0/PO17/SCK5/ SSLA2-B/ET0_WOL/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/GTIOC2A/SCK5/SSLA2-B/ ET0_WOL/LCD_DATA7-B/IRQ11
70	PA0/A0/BC0#/MTIOC4A/MTIOC6D/ GTIOC0B-C/TIOCA0/CACREF/PO16/ SSLA1-B/ET0_TX_EN/RMII0_TXD_EN	PA0/BC0#/A0/MTIOC4A/MTIOC6D/TIOCA0/ PO16/CACREF/GTIOC0B/SSLA1-B/ ET0_TX_EN/RMII0_TXD_EN/LCD_DATA8-B
71	PE7/D15[A15/D15]/MTIOC6A/GTIOC3A-E/ TOC1/MMC_RES#-B/SDHI_WP-B/IRQ7/ AN105	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/GTIOC3A/MISOB-B/SDHI_WP/ MMC_RES#-B/LCD_DATA9-B/IRQ7/AN105
72	PE6/D14[A14/D14]/MTIOC6C/GTIOC3B-E/ TIC1/MMC_CD-B/SDHI_CD-B/IRQ6/AN104	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/GTIOC3B/MOSIB-B/SDHI_CD/ MMC_CD-B/LCD_DATA10-B/IRQ6/AN104
73	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/ GTIOC0A-A/ET0_RX_CLK/REF50CK0/ IRQ5/AN103	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/RSPCKB-B/ ET0_RX_CLK/REF50CK0/LCD_DATA11-B/ IRQ5/AN103
74	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/ GTIOC1A-A/PO28/ET0_ERXD2/AN102	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/SSLB0-B/ ET0_ERXD2/LCD_DATA12-B/AN102
75	PE3/D11[A11/D11]/MTIOC4B/GTIOC2A-A/ PO26/POE8#/TOC3/CTS12#/RTS12#/ SS12#/ET0_ERXD3/MMC_D7-B/AN101	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/TOC3/POE8#/GTIOC2A/CTS12#/ RTS12#/SS12#/ET0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101
76	PE2/D10[A10/D10]/MTIOC4A/GTIOC0B-A/ PO23/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/MMC_D6-B/IRQ7-DS/AN100	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/GTIOC0B/RXD12/SMISO12/ SSCL12/RXDX12/SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/AN100
77	PE1/D9[A9/D9]/MTIOC4C/MTIOC3B/ GTIOC1B-A/PO18/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/MMC_D5-B/ ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/GTIOC1B/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLB2-B/MMC_D5-B/LCD_DATA15-B/ ANEX1
78	PE0/D8[A8/D8]/MTIOC3D/GTIOC2B-A/ SCK12/MMC_D4-B/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/ GTIOC2B/SCK12/SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0
79	PD7/D7[A7/D7]/MTIC5U/POE0#/ MMC_D1-B/SDHI_D1-B/QIO1-B/QMI-B/ IRQ7/AN107	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B/ LCD_DATA17-B/IRQ7/AN107
80	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ MMC_D0-B/SDHI_D0-B/QIO0-B/QMO-B/ IRQ6/AN106	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/IRQ6/AN106

100-Pin LFQFP	RX64M	RX66N
81	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/ MMC_CLK-B/SDHI_CLK-B/QSPCLK-B/ IRQ5/AN113	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/ MTCLKA/POE10#/SSLC1-A/QSPCLK-B/ SDHI_CLK-B/MMC_CLK-B/LCD_DATA19-B/ IRQ5/AN113
82	PD4/D4[A4/D4]/MTIOC8B/POE11#/ MMC_CMD-B/SDHI_CMD-B/QSSL-B/IRQ4/ AN112	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/QSSL-B/SDHI_CMD-B/ MMC_CMD-B/LCD_DATA20-B/IRQ4/AN112
83	PD3/D3[A3/D3]/MTIOC8D/GTIOC0A-E/ POE8#/TOC2/MMC_D3-B/SDHI_D3-B/ QIO3-B/IRQ3/AN111	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ GTIOC0A/RSPCKC-A/QIO3-B/SDHI_D3-B/ MMC_D3-B/LCD_DATA21-B/IRQ3/AN111
84	PD2/D2[A2/D2]/MTIOC4D/GTIOC0B-E/ TIC2/CRX0/MMC_D2-B/SDHI_D2-B/ QIO2-B/IRQ2/AN110	PD2/D2[A2/D2]/MTIOC4D/TIC2/GTIOC0B/ MISOC-A/CRX0/QIO2-B/SDHI_D2-B/ MMC_D2-B/LCD_DATA22-B/IRQ2/AN110
85	PD1/D1[A1/D1]/MTIOC4B/GTIOC1A-E/ POE0#/CTX0/IRQ1/AN109	PD1/D1[A1/D1]/MTIOC4B/POE0#/GTIOC1A/ MOSIC-A/CTX0/LCD_DATA23-B/IRQ1/ AN109
86	PD0/D0[A0/D0]/GTIOC1B-E/POE4#/IRQ0/ AN108	PD0/D0[A0/D0]/POE4#/GTIOC1B/ LCD_EXTCLK-B/IRQ0/AN108
87	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
88	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
89	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
90	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
91	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
92	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
93	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
94	VREFL0	VREFL0
95	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
96	VREFH0	VREFH0
97	AVCC0	AVCC0
98	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
99	AVSS0	AVSS0
100	P05/IRQ13/DA1	P05/SSILRCK1/IRQ13/DA1

Notes: 1. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.
2. Pins for FIFO embedded serial communications interface (SCIFA).

4. Important Information when Migrating Between MCUs

4.1 Notes on Pin Design

4.1.1 VCL Pin (External Capacitor)

To stabilize the internal power supply on the RX66N Group, connect a 0.22 µF smoothing capacitor to the VCL pin.

4.1.2 Inserting Decoupling Capacitors between AVCC and AVSS Pins

To prevent destruction of the RX66N Group's analog input pins (AN000 to AN007 and AN100 to AN120) by abnormal voltage such as an excessive surge, insert capacitors between AVCCn and AVSSn, and connect a protective circuit to protect the analog input pins (AN000 to AN007 and AN100 to AN120).

For details, refer to "Notes on Noise Prevention" in the 12-Bit A/D Converter section of RX66N Group User's Manual: Hardware.

4.2 Notes on Functional Design

This section presents software-related considerations regarding function settings that differ between the RX64M Group and the RX66N Group.

For differences between modules and functions, refer to 2, Comparative Overview of Specifications. For further information, refer to the User's Manual: Hardware of each MCU group, listed in 5, Reference Documents.

4.2.1 Flash Access Window Setting Register (FAW)

On the RX66N Group, once the access window protect bit (FSPR) in the flash access window setting register (FAW) is cleared to 0, it cannot be set to 1 once again.

For details, refer to RX66N Group User's Manual: Hardware, referenced in section 5, Reference Documents.

4.2.2 Clock Frequency Settings

The RX64M Group and the RX66N Group have different limits on clock frequency settings. Refer to Table 4.1 for details.

Table 4.1 Comparison of Limits on Clock Frequency Settings

Item	RX64M	RX66N
Clock frequency setting limits	ICLK ≥ BCLK PCLKA ≥ PCLKB PCLKB ≥ PCLKC PCLKB ≥ PCLKD	ICLK ≥ BCLK PCLKA ≥ PCLKB PCLKB ≥ PCLKC PCLKB ≥ PCLKD
Clock frequency ratio limits	ICLK:FCLK = N:1 or 1:N ICLK:PCLKA = N:1 or 1:N ICLK:PCLKB = N:1 or 1:N ICLK:PCLKC = N:1 or 1:N ICLK:PCLKD = N:1 or 1:N	ICLK:FCLK = N:1 or 1:N ICLK:PCLKA = N:1 or 1:N ICLK:PCLKB = N:1 or 1:N ICLK:PCLKC = N:1 or 1:N ICLK:PCLKD = N:1 or 1:N ICLK:BCLK = N:1

4.2.3 Using a Low CL Crystal Oscillator

When connecting an on-chip debugging emulator to the FINED pin of the RX64M Group, set the RCR3.RTCDV[2:0] bits to 110b (drive capacity for standard CL) even when using a low CL oscillator.

On the RX66N Group, set the RCR3.RTCDV[2:0] bits to 001b (drive capacity for low CL) and debug at room temperature.

4.2.4 Battery Backup Function

The RX66N Group is not provided with a function for detecting a voltage drop on the VBATT pin. The operation of the RTC cannot be assured if the voltage from the VBATT pin drops below the range in which operation is guaranteed. Therefore, if the VBATT voltage does drop below this range, make initial settings to the RTC after the power supply is restored.

4.2.5 Compare Function Limitations

On the RX66N Group the compare function of the 12-bit A/D converter is subject to the following limitations:

(1) If temperature sensor or internal reference voltage is selected for window A, window B operation is prohibited.
(2) If temperature sensor or internal reference voltage is selected for window B, window A operation is prohibited.
(3) Window A and window B must not be set to the same channel.
(4) Make settings such that the high-side reference value is greater than or equal to the low-side reference value.

4.2.6 Initial Setting Procedure for Output Buffer Amplifier

To use the output buffer amplifier with the 12-bit D/A converter of the RX66N Group, follow the steps below to enable amplifier output.

(1) Confirm that both the DACR.DAE and DACR.DAOEn bits are cleared to 0.
(2) Write 0000h to the DADRn register.
(3) Set the DAASWCR.DAASWn bit to 1.
(4) Set the DAAMPCR.DAAMPn bit to 1.
(5) Set the DACR.DAE bit or the DACR.DAOEn bit to 1. The output buffer amplifier is activated.
(6) After waiting a minimum of 3 μs, clear the DAASWCR.DAASWn bit to 0.
(7) Write the value to be converted to the DADRn register.

Note that clearing the DACR.DAE and DACR.DAOEn bits to 0 while the output buffer amplifier is operating will cause it to enter the stopped state. To use the output buffer amplifier again, it is necessary to redo steps (1) to (7).

4.2.7 Running RAM Self-Diagnostics on Register Save Banks

On the RX66N Group the register save banks are configured in the RAM. The register save banks are buffered, so writing to a bank with the SAVE instruction and then reading from the same bank with the RSTR instruction immediately afterwards may result in data being read from the buffer rather than from the RAM memory cells. When running RAM self-diagnostics on a register save bank, follow the steps below to ensure that the previously written data is read from the RAM rather than from the buffer.

(1) Use the SAVE instruction to write data to the bank on which self-diagnostics will be run.
(2) Use the SAVE instruction to write data to a bank other than that written to in step (1).
(3) Use the RSTR instruction to read data from the bank written to in step (1).

4.2.8 ROM Cache

The RX66N Group has an 8 KB ROM cache, but it is not operational immediately after a reset is canceled.

To use the ROM cache, set the ROMCE.ROMCEN bit to 1.

4.2.9 Transferring Firmware to FCU RAM

In order to use FCU commands on the RX64M Group, it is first necessary to save the FCU firmware to the FCU RAM. This processing is not required on the RX66N Group.

4.2.10 User Boot Mode

RX64M Group has UB code A, UB code B and user boot mode, but none of these exist on the RX66N Group.

When using the startup program protection function on the RX66N Group, it is possible to use a user-defined interface to program and erase the user area in the flash memory instead of user boot mode. For details, refer to the “Startup Program Protection Function” section in RX66N Group User’s Manual: Hardware, referenced in section 5, Reference Documents.

5. Reference Documents

User's Manual: Hardware

RX64M Group User's Manual: Hardware, Rev. 1.10 (R01UH0377EJ)
(The latest version can be downloaded from the Renesas Electronics website.)

RX64M Group, RX71M Group Flash Memory User's Manual: Hardware Interface,
Rev. 1.10 (R01UH0435)
(The latest version can be downloaded from the Renesas Electronics website.)

RX66N Group User's Manual: Hardware, Rev. 1.00 (R01UH0825)

Application Note

Design Guide for Migration between RX Family: Differences in Package External form (R01AN4591EJ)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This application note reflects the content of the following technical updates:

- TN-RX*-A0147B/E
- TN-RX*-A0212A/E
- TN-RX*-A0210A/E
- TN-RX*-A0207A/E
- TN-RX*-A195A/E
- TN-RX*-A193A/E
- TN-RX*-A192A/E
- TN-RX*-A187A/E
- TN-RX*-A178A/E
- TN-RX*-A177A/E
- TN-RX*-A175A/E
- TN-RX*-A174A/E
- TN-RX*-A173A/E
- TN-RX*-A172A/E
- TN-RX*-A161A/E
- TN-RX*-A160A/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Sep. 30, 2019	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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