RX660 Group, RX66T Group

Differences Between the RX660 Group and the RX66T Group

Introduction

This application note is intended as a reference to points of difference between the peripheral functions, I/O registers, and pin functions of the RX660 Group and RX66T Group, as well as a guide to key points to consider when migrating between the two groups.

Unless specifically otherwise noted, the information in this application note applies to the 144-pin package version of the RX660 Group and RX66T Group as the maximum specifications. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the User's Manual: Hardware of the products in question.

Target Devices

RX660 Group and RX66T Group

Contents

1. Comparison of Built-In Functions of RX660 Group and RX66T Group

A comparison of the built-in functions of the RX660 Group and RX66T Group is provided below. For details of the functions, see section 2, Comparative Overview of Specifications and section 5, Reference Documents.

Table 1.1 is Comparison of Built-In Functions of RX660 Group and RX66T Group.

Table 1.1 Comparison of Built-In Functions of RX660 Group and RX66T Group

Function	RX66T	RX660
CPU	▲	
Operating modes	■	
Address space	■	
Reset	○	
Option-setting memory (OFSM)	○	
Voltage detection circuit (LVDA)	○	
Clock generation circuit	●	
Clock frequency accuracy measurement circuit (CAC)	●	
Low power consumption	●/■	
Register write protection function	●	
Exception Handling	○	
Interrupt controller (ICUF for RX66T, and ICUC for RX660)	●/▲	
Buses	■	
Memory-protection unit (MPU)	○	
DMA controller (DMACAa)	○	
Data transfer controller (DTCa for RX66T, and DTCb for RX660)	●	
Event link controller (ELC)	▲	
I/O ports	▲	
Multi-function pin controller (MPC)	●/■	
Multi-function timer pulse unit 3 (MTU3d for RX66T, and MTU3a for RX660)	▲/■	
Port output enable 3 (POE3B for RX66T, and POE3a for RX660)	▲/■	
General purpose PWM timer (GPTW)	○	×
High resolution PWM waveform generation circuit (HRPWM)	○	×
Port output enable for GPTW (POEG)	○	×
8-bit timer (TMRb)	▲	
Compare match timer (CMT)	○	
Compare match timer W (CMTW)	×	○
Realtime clock (RTCBa)	×	○
Low-Power Timer (LPT)	○	×
Watchdog timer (WDTA)	○	
Independent watchdog timer (IWDTa)	○	
USB2.0FS host or function module (USBb)	○	×
Serial communications interface (SCIj, SCIi, SCIh for RX66T) (SCIk, SCIm, SCIh for RX660)	▲	
Serial communications interface (RSCI)	×	○
Remote control signal receiver (REMCa)	×	○
I²C bus interface (RIICa)	▲	
CAN module (CAN): RX66T CANFD module (CANFD-Lite): RX660	●	

Function	RX66T	RX660
Serial peripheral interface (RSPIc for RX66T, and RSPId for RX660)	●	
CRC calculator (CRCA)	○	
Remote control signal receiver (REMCa)	×	○
Trigonometric function calculator (TFU)	×	○
Trusted Secure IP (TSIP-Lite)	○	×
12-bit A/D converter (S12ADH)	▲	
12-bit D/A converter (R12DAb)	▲	
Temperature sensor (TEMPS)	▲	
Comparator C (CMPC)	▲	
Data operation circuit (DOC for RX66T, and DOCA for RX660)	▲	
RAM	▲/■	
Flash memory (FLASH)	▲/■	
Packages	▲	

○: Available, ×: Unavailable, ●: Differs due to added functionality, ▲: Differs due to change in functionality, ■: Differs due to removed functionality.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Differences in register specifications are not listed.

2.1 CPU

Table 2.1 is Comparative Overview of CPU.

Table 2.1 Comparative Overview of CPU

Item	RX66T	RX660
CPU	• Maximum operating frequency: 160 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • 111 instructions — Standard provided instructions: 111 Basic instructions: 77 Single-precision floating point instructions: 11 DSP instructions: 23 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian and big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 × 32 bits • Barrel shifter: 32 bits	• Maximum operating frequency: 120 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • 113 instructions — Standard provided instructions: 111 Basic instructions: 77, variable-length instruction format Single-precision floating point instructions: 11 DSP instructions: 23 — Instructions for register bank save function: 2 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian and big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits
FPU	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard
Register bank save function	—	• Fast collective saving and restoration of the values of CPU registers • 16 save register banks

2.2 Operating Modes

Table 2.2 is Comparative Overview of Operating Modes, and Table 2.3 is Comparison of Operating Mode Registers.

Table 2.2 Comparative Overview of Operating Modes

Item	RX66T	RX660
Operating modes specified by mode setting pins	Single-chip mode	Single-chip mode
	Boot mode (SCI interface) Boot mode (USB interface) User boot mode Boot mode (FINE interface)	Boot mode (SCI interface) User boot mode Boot mode (FINE interface)
Operating modes selected by register settings	Single-chip mode and user boot mode On-chip ROM disabled extended mode On-chip ROM enabled extended mode	Single-chip mode and user boot mode On-chip ROM disabled extended mode On-chip ROM enabled extended mode

Table 2.3 Comparison of Operating Mode Registers

Register	Bit	RX66T	RX660
SYSCR1	ECCRAME	ECCRAM enable bit	—
VOLSR	USBVON	USB power supply control bit	—
	PGAVLS	PGA operating condition setting bit	—

2.3 Address Space

Figure 2.1 is a Comparative Memory Map of Single-Chip Mode.

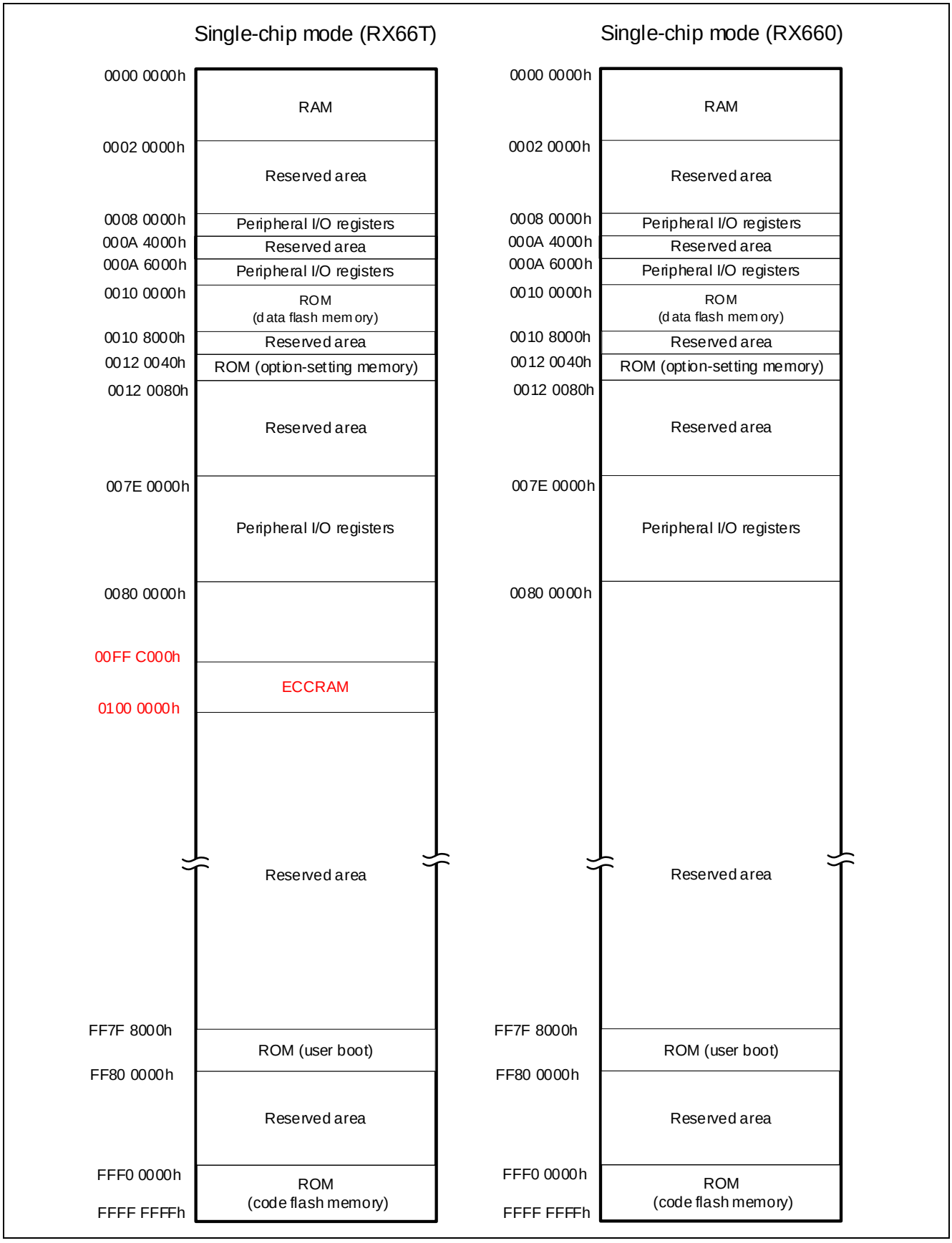

Figure 2.1 Comparative Memory Map of Single-Chip Mode

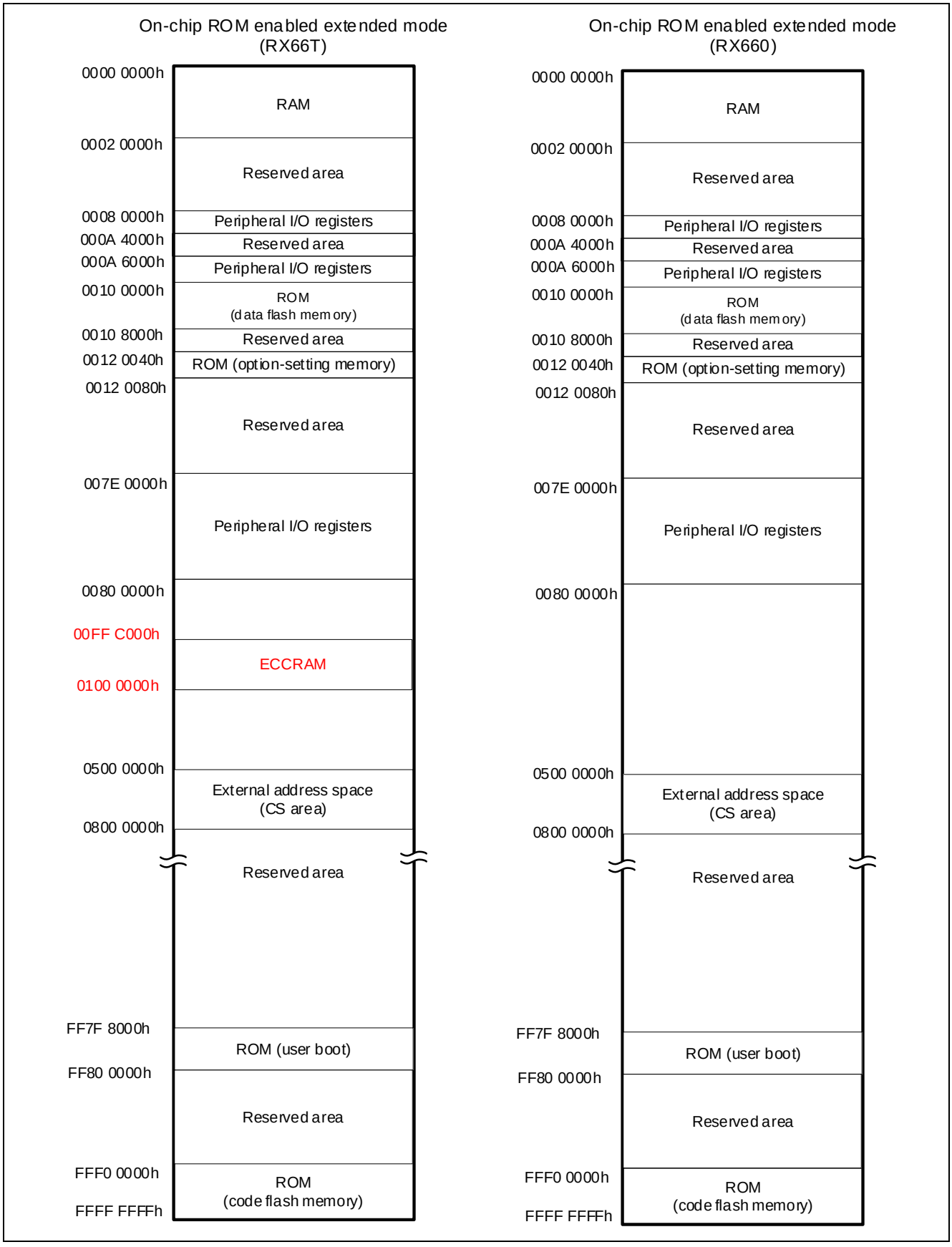

Figure 2.2 Comparative Memory Map of On-chip ROM Enabled Extended Mode

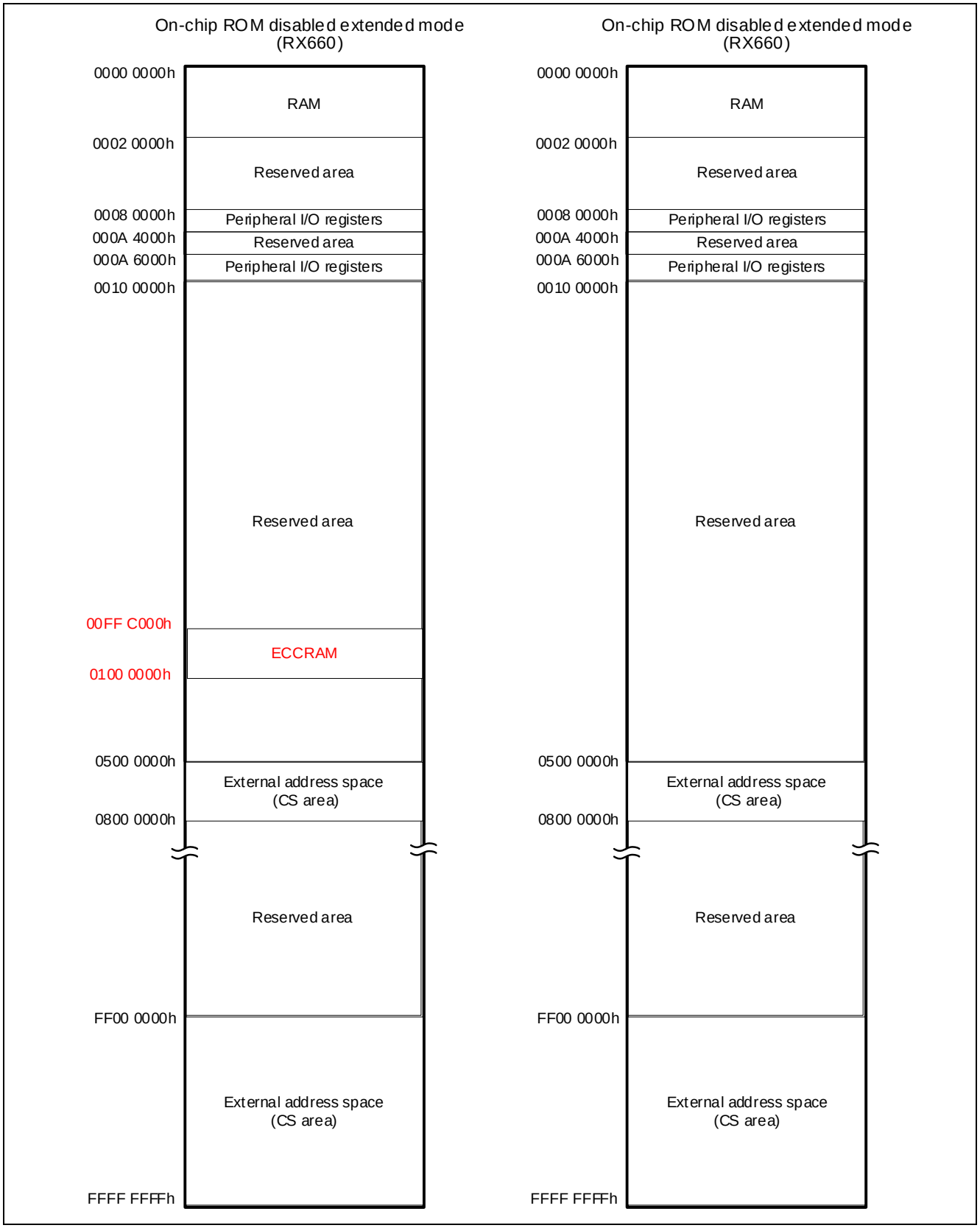

Figure 2.3 Comparative Memory Map of On-chip ROM Disabled Extended Mode

2.4 Clock Generation Circuit

Table 2.4 is Comparative Overview of Clock Generation Circuits, and Table 2.5 is Comparison of Clock Generation Circuit Registers.

Table 2.4 Comparative Overview of Clock Generation Circuits

Item	RX66T	RX660
Use	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the RSPI, SCIi, MTU3 (internal peripheral bus), GPTW (internal peripheral bus), and HRPWM (internal peripheral bus). • Generates the peripheral module clock (PCLKB) supplied to the peripheral modules. • Generates the counter reference clock for peripheral modules and the HRPWM reference clock (PCLKC) to be supplied to the MTU3 and GPTW. • Generates the peripheral module clock (for analog conversion) (PCLKD) to be supplied to the S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the USB clock (UCLK) to be supplied to the USBb. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.	• Generates the system clock (ICLK) to be supplied to the CPU, TFU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the RSPI, SCIm, RSCI, MTU, and CANFD. • Generates the peripheral module clock (PCLKB) supplied to the peripheral modules. • Generates the peripheral module clock (for analog conversion) (PCLKD) to be supplied to the S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CANFD clock (CANFDCLK) to be supplied to the CANFD. • Generates the CANFD main clock (CANFDMCLK) to be supplied to the CANFD. • Generates the RTC sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the REMC sub-clock (REMSCLK) to be supplied to the REMC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.

Item	RX66T	RX660
Operating frequency	• ICLK: 160 MHz (max) • PCLKA: 120 MHz (max) • PCLKB: 60 MHz (max) • PCLKC: 160 MHz (max) • PCLKD: 8 MHz to 60 MHz (when 12-bit A/D converter is operating) • FCLK: — 4 MHz to 60 MHz (during programming or erasing of code flash memory or data flash memory) — 60MHz(max) (for reading from the data flash) • BCLK: 60 MHz (max) • BCLK pin output: 40 MHz (max.) • UCLK: 48MHz (max) • CACCLK: Same as clock from respective oscillators • CANMCLK: 24 MHz (max) • IWDTCLK: 120 kHz	• ICLK: 120 MHz (max) • PCLKA: 120 MHz (max) • PCLKB: 60 MHz (max) • PCLKD: 8 MHz to 60 MHz (when 12-bit A/D converter is operating) • FCLK: — 4 MHz to 60 MHz (during programming or erasing of code flash memory or data flash memory) — 60MHz(max) (for reading from the data flash) • BCLK: 60 MHz (max) • BCLK pin output: 40 MHz (max.) • CACCLK:Same as clock from respective oscillators • CANFDCLK: 60 MHz (max) • CANFDMCLK: 24 MHz (max) • RTCSCLK: 32.768 kHz • REMCLK 32.768 kH • IWDTCLK: 120 kHz
Main clock oscillator	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24MHz (max) • Connectable resonator or additional circuit: Ceramic resonator, crystal • Connection pins: EXTAL and XTAL • Oscillation stop detection function: When detecting a main clock oscillation stop, this function switches the system clock source to the LOCO and drives the MTU and GPTW pins to the high-impedance state.	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24MHz (max) • Connectable resonator or additional circuit: Ceramic resonator, crystal • Connection pins: EXTAL and XTAL • Oscillation stop detection function: When detecting a main clock oscillation stop, this function switches the system clock source to the LOCO and drives the MTU pin to the high-impedance state.
Sub-clock oscillator	—	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: Crystal • Connection pins: XCIN and XCOUT
PLL frequency synthesizer	• Input clock source: Main clock, HOCO • Input pulse frequency division ratio: Selectable from 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable from 10 to 30 • Oscillation frequency: 120MHz to 240MHz	• Input clock source: Main clock, HOCO • Input pulse frequency division ratio: Selectable from 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable from 10 to 30 • Output clock frequency of PLL frequency synthesizer: 120 MHz to 240 MHz

Item	RX66T	RX660
High-speed on-chip oscillator (HOCO)	• Oscillation frequency: Selectable from 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control	• Oscillation frequency: Selectable from 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control • FLL function (only present in products incorporating a sub-clock oscillator)
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 240 kHz	Oscillation frequency: 240 kHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 120 kHz	Oscillation frequency: 120 kHz
BCLK pin output control function	• Selectable between BCLK clock output or high-level output. • Output clock selectable between BCLK or BCLK/2.	• Selectable between BCLK clock output or high-level output. • Output clock selectable between BCLK or BCLK/2.
Event link function (output)	Detection of stopping of the main clock oscillator	Detection of stopping of the main clock oscillator
Event link function (input)	Switching of the clock source to the low-speed on-chip oscillator	Switching of the clock source to the low-speed on-chip oscillator

Table 2.5 Comparison of Clock Generation Circuit Registers

Register	Bit	RX66T	RX660
SCKCR	PCKC[3:0]	Peripheral module clock (PCLKC) select bit b7 b4 0 0 0 0: x1/1 0 0 0 1: x1/2 0 0 1 0: x1/4 0 0 1 1: x1/8 0 0 0 0: x1/16 0 1 0 1: x1/32 0 1 1 0: x1/64 Settings other than the above are prohibited.	The PCLKC is not implemented on this MCU. These bits should be set to 0001b.
MEMWAIT	—	Memory wait cycle setting register	—
SCKCR2	UCK[3:0]	USB clock (UCLK) select bit	—
	CFDCK[3:0]	—	CANFD clock (CANFDCLK) select bit
SCKCR3	CKSEL[2:0]	Clock source select bit b10 b8 0 0 0: LOCO is selected. 0 0 0: HOCO is selected. 0 1 0: Main clock oscillator is selected. 1 0 0: PLL circuit is selected. Settings other than the above are prohibited.	Clock source select bit b10 b8 0 0 0: LOCO is selected. 0 0 0: HOCO is selected 0 1 0: Main clock oscillator is selected. 0 1 0: Sub-clock oscillator is selected. 1 0 0: PLL circuit is selected. Settings other than the above are prohibited.
SOSCCR	—	—	Sub-clock oscillator control register
FLLCR1	—	—	FLL control register 1
FLLCR2	—	—	FLL control register 2
OSCOVFSR	SOOVF	—	Sub-clock oscillation stabilization flag
SOSCWTCR	—	—	Sub-clock oscillator wait control register
SOFCR	—	—	Sub-clock oscillator forced oscillation control register

2.5 Clock Frequency Accuracy Measurement Circuit

Table 2.6 is Comparative Overview of Clock Frequency Accuracy Measurement Circuits.

Table 2.6 Comparative Overview of Clock Frequency Accuracy Measurement Circuits

Item	RX66T	RX660
Measurement target clocks	• The frequency of the following clocks can be measured: • Main clock • HOCO clock • LOCO clock • IWDT-dedicated clock (IWDTCLK) • Peripheral module clock B (PCLKB)	• The frequency of the following clocks can be measured: • Main clock • Sub-clock • HOCO clock • LOCO clock • IWDT-dedicated clock (IWDTCLK) • Peripheral module clock B (PCLKB)
Measurement reference clocks	• External clock input to the CACREF pin • Main clock • HOCO clock • LOCO clock • IWDT-dedicated clock (IWDTCLK) • Peripheral module clock B (PCLKB)	• External clock input to the CACREF pin • Main clock • Sub-clock • HOCO clock • LOCO clock • IWDT-dedicated clock (IWDTCLK) • Peripheral module clock B (PCLKB)
Selectable functions	Digital filter function	Digital filter function
Interrupt sources	• Measurement end interrupt • Frequency error interrupt • Overflow interrupt	• Measurement end interrupt • Frequency error interrupt • Overflow interrupt
Low power consumption function	Transition to the module stop state is possible.	Transition to the module stop state is possible.

Table 2.7 Comparison of Clock Frequency Accuracy Measurement Registers

Register	Bit	RX66T (CAC)	RX660 (CAC)
CACR1	FMCS[2:0]	Measurement target clock select bits b3 b1 0 0 0: Main clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock B (PCLKB) Settings other than the above are prohibited.	Measurement target clock select bits b3 b1 0 0 0: Main clock 0 0 1: Sub-clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock B (PCLKB) Settings other than the above are prohibited.
CACR2	RSCS[2:0]	Measurement reference clock select bits b3 b1 0 0 0: Main clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock B (PCLKB) Settings other than the above are prohibited.	Measurement reference clock select bits b3 b1 0 0 0: Main clock 0 0 1: Sub-clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock B (PCLKB) Settings other than the above are prohibited.

2.6 Low Power Consumption

Table 2.8 is Comparative Overview of Low Power Consumption Functions, Table 2.9 is Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode, and Table 2.10 is Comparison of Low Power Consumption Registers.

Table 2.8 Comparative Overview of Low Power Consumption Functions

Item	RX66T	RX660
Reducing power consumption by switching clock signals	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, and PCLKD), external bus clock (BCLK), and flash interface clock (FCLK).	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, and PCLKD), external bus clock (BCLK), and flash interface clock (FCLK).
BCLK output control function	Selectable from BCLK output and high-level output	Selectable from BCLK output and high-level output
Module stop function	Each peripheral module can be stopped independently by the module stop control register.	Each peripheral module can be stopped independently by the module stop control register.
Function for transition to low power consumption mode	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.
Low power consumption modes	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode

Table 2.9 Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX66T	RX660
Sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupts	Interrupts
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	—	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM, ECCRAM (RX66T)	Operation possible (retained)	Operation possible (retained)
	Flash memory	Operation	Operation
	USBFS host or function module (USBb)	Operation possible	—
	Watchdog timer (WDT)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	—	Operation possible
	Port output enable (POE)	Operation possible	Operation possible
	Remote control signal receiver (REMC)	—	Operation possible
	8-bit timer (unit 0, unit1) (TMR)	Operation possible	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Operation possible	Operation possible
	I/O ports	Operation	Operation
All-module clock stop mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupts	Interrupts
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	—	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM, ECCRAM (RX66T)	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	USBFS host or function module (USBb)	Stopped	—

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX66T	RX660
All-module clock stop mode	Watchdog timer (WDT)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Port output enable (POE)	Operation possible	Operation possible
	Remote control signal receiver (REMC)	—	Operation possible
	8-bit timer (unit 0 and unit1) (TMR)	Operation possible	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained
Software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupts	Interrupts
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Stopped	Stopped
	Sub-clock oscillator	—	Operation possible
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Stopped
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Stopped	Stopped
	CPU	Stopped (retained)	Stopped (retained)
	RAM, ECCRAM (RX66T)	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	USBFS host or function module (USBb)	Stopped	—
	Watchdog timer (WDT)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	—	Operation possible
	Port output enable (POE)	Stopped (retained)	Stopped (retained)
	Remote control signal receiver (REMC)	—	Operation possible
	8-bit timer (unit 0 and unit1) (TMR)	Stopped (retained)	Stopped (retained)
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained
Deep software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupts	Interrupts
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Stopped	Stopped
	Sub-clock oscillator	—	Operation possible
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Stopped

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX66T	RX660
Deep software standby mode	IWDT-dedicated on-chip oscillator	Stopped (undefined)	Stopped (undefined)
	PLL	Stopped	Stopped
	CPU	Stopped (undefined)	Stopped (undefined)
	RAM, ECCRAM (RX66T)	Stopped (undefined)	Stopped (undefined)
	Flash memory	Stopped (retained)	Stopped (retained)
	USBFS host or function module (USBb)	Stopped (undefined)	—
	Watchdog timer (WDT)	Stopped (undefined)	Stopped (undefined)
	Independent watchdog timer (IWDT)	Stopped (undefined)	Stopped (undefined)
	Realtime clock (RTC)	—	Operation possible
	Port output enable (POE)	Stopped (undefined)	Stopped (undefined)
	Remote control signal receiver (REMC)	—	Stopped (undefined)
	8-bit timer (unit 0 and unit1) (TMR)	Stopped (undefined)	Stopped (undefined)
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (undefined)	Stopped (undefined)
	I/O ports	Retained	Retained

“Operation possible” means that whether the state is operating or stopped is controlled by the control register setting.

“Stopped (retained)” means that internal register values are retained and internal operations are suspended.

“Stopped (undefined)” means that internal register values are undefined and power is not supplied to the internal circuit.

Table 2.10 Comparison of Low Power Consumption Registers

Register	Bit	RX66T	RX660
MSTPCRA	MSTPA0	—	Compare match timer W (unit 1) module stop bit
	MSTPA1	—	Compare match timer W (unit 0) module stop bit
	MSTPA2	8-bit timer 7, 6 (unit 3) module stop bit	—
	MSTPA3	8-bit timer 5, 4 (unit 2) module stop bit	—
	MSTPA7	General purpose PWM timer/high resolution PWM/GPTW-dedicated port output enable module stop bit	—
	MSTPA16	12-bit A/D converter (unit 1) module stop bit	—
	MSTPA23	12-bit A/D converter (unit 2) module stop bit	—
MSTPCRB	MSTPB0	CAN module 0 module stop bit(Note 1)	—
	MSTPB19	Universal serial bus 2.0 FS interface module stop bit(Note 2)	—
	MSTPB24	—	Serial communications interface 7 module stop bit
	MSTPB27	—	Serial communications interface 4 module stop bit
	MSTPB28	—	Serial communications interface 3 module stop bit
	MSTPB29	—	Serial communications interface 2 module stop bit
	MSTPB31	—	Serial communications interface 0 module stop bit
MSTPCRC	MSTPC6	ECCRAM module stop bit	—
	MSTPC17	—	I^2C bus interface 2 module stop bit
	MSTPC25	—	Serial communications interface 10 module stop bit
MSTPCRD	MSTPD0	Module stop D0 setting bit	—
	MSTPD1	Module stop D1 setting bit	—
	MSTPD4	Module stop D4 setting bit	—
	MSTPD5	Module stop D5 setting bit	—
	MSTPD6	Module stop D6 setting bit	—
	MSTPD7	Module stop D7 setting bit	Remote control signal receiver module stop bit
	MSTPD10	—	CANFD module stop bit
	MSTPD27	Trusted Secure IP-Lite module stop bit	—
DPSIER2	DRTCIIE	—	RTC periodic interrupt deep-standby cancellation signal enable bit
	DRTCAIE	—	RTC alarm interrupt deep-standby cancellation signal enable bit

Register	Bit	RX66T	RX660
DPSIFR2	DRTCIIF	—	RTC periodic interrupt deep-standby cancellation flag
	DRTCAIF	—	RTC alarm interrupt deep-standby cancellation flag

Note 1. When rewriting the MSTPB0 bit, confirm that the clock oscillation controlled by theMSTPB0 bit is stable. To enter the software standby mode after rewriting the MSTPB0 bit, wait for 2 cycles of the CAN clock (CANMCLK) after the rewrite, and then execute the WAIT instruction.

Note 2. To enter the software standby mode after rewriting the MSTPB19 bit, wait for 2 cycles of the USBb clock (UCLK) after the rewrite, and then execute the WAIT instruction.

2.7 Register Write Protection Function

Table 2.11 is Comparative Overview of Register Write Protection Functions.

Table 2.11 Comparative Overview of Register Write Protection Functions

Item	RX66T	RX660
PRC0 bit	• Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, OSTDCR, OSTDSR	• Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, FLLCR1, FLLCR2, OSTDCR, OSTDSR
PRC1 bit	• Registers related to the operating modes: SYSCR0, SYSCR1, VOLSR • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, RSTCKCR, DPSBYCR, DPSIER0 to 2, DPSIFR0 to 2, DPSIEGR0 to 2 • Registers related to the clock generation circuit: MOSCWTCR, MOFCR, HOCOPCR • Software reset register: SWRR	• Registers related to the operating modes: SYSCR0, SYSCR1, VOLSR • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, RSTCKCR, DPSBYCR, DPSIER0 to 2, DPSIFR0 to 2, DPSIEGR0 to 2 • Registers related to the clock generation circuit: MOSCWTCR, SOSCWTCR, MOFCR, SOFCR, HOCOPCR • Software reset register: SWRR
PRC3 bit	• Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	• Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

2.8 Interrupt Controller

Table 2.12 is Comparative Overview of Interrupt Controllers, and Table 2.13 is Comparison of Interrupt Controller Registers.

Table 2.12 Comparative Overview of Interrupt Controllers

Item		RX66T (ICUC)	RX660 (ICUF)
Interrupts	Peripheral function interrupts	Interrupts from peripheral modules • Interrupt detection method: Edge detection/level detection (fixed for each interrupt source) • Group interrupt: Multiple interrupt sources are grouped together and treated as a single interrupt source. — Group IE0 interrupt: Interrupt sources of coprocessors that use CLK as the operating clock (edge detection) — Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) — Group BL0/BL1/BL2 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) — Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.	Interrupts from peripheral modules • Interrupt detection method: Edge detection/level detection (fixed for each interrupt source) • Group interrupt: Multiple interrupt sources are grouped together and treated as a single interrupt source. — Group IE0 interrupt: Interrupt sources of coprocessors that use CLK as the operating clock (edge detection) — Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) — Group BL0/BL1/BL2 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) — Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt B: Any of the interrupt sources for peripheral modules that use PCLKB as the operating clock can be assigned to interrupt vector numbers 128 to 207. • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.

Item		RX66T (ICUb)	RX660 (ICUF)
Interrupts	External pin interrupts	Interrupts by input signals on IRQi pins (i = 0 to 15) • Interrupt detection: Detection of low level, falling edge, rising edge, or rising and falling edges can be set for each detection source. • A digital filter can be used to remove noise.	Interrupts by input signals on IRQi pins (i = 0 to 15) • Interrupt detection: Detection of low level, falling edge, rising edge, or rising and falling edges can be set for each detection source. • A digital filter can be used to remove noise.
	Software interrupts	• An interrupt request can be generated by writing to a register. • Number of sources: 2	• An interrupt request can be generated by writing to a register. • Number of sources: 2
	Interrupt priority level	The priority level is set with the interrupt source priority register r (IPRr) (r = 000 to 255).	The priority level is set with the interrupt source priority register r (IPRr) (r = 000 to 255).
	Fast interrupt function	It is possible to reduce the CPU's interrupt response time. This setting can be used for one interrupt source only.	It is possible to reduce the CPU's interrupt response time. This setting can be used for one interrupt source only.
	DTC and DMAC control	The DTC and DMAC can be activated by an interrupt source.	The DTC and DMAC can be activated by an interrupt source.
Non-maskable interrupts	NMI pin interrupt	Interrupt by the input signal on the NMI pin • Interrupt detection: Falling edge or rising edge • A digital filter can be used to remove noise.	Interrupt by the input signal on the NMI pin • Interrupt detection: Falling edge or rising edge • A digital filter can be used to remove noise.
	Oscillation stop detection interrupt	Interrupt at detection of main clock oscillation stop	Interrupt at detection of main clock oscillation stop
	WDT underflow/ refresh error interrupt	Interrupt occurs when the watchdog timer underflows or a refresh error occurs.	Interrupt occurs when the watchdog timer underflows or a refresh error occurs.
	IWDT underflow/ refresh error interrupt	Interrupt occurs when the independent watchdog timer underflows or a refresh error occurs.	Interrupt occurs when the independent watchdog timer underflows or a refresh error occurs.
	Voltage monitoring 1 interrupt	Voltage monitoring interrupt of voltage detection circuit 1 (LVD1)	Interrupt from voltage detection circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Voltage monitoring interrupt of voltage detection circuit 2 (LVD2)	Interrupt from voltage detection circuit 2 (LVD2)
	RAM error interrupt	Interrupt occurs when a parity check error is detected in the RAM or an ECC error is detected in the ECCRAM	Interrupt occurs when a parity check error is detected in the RAM.

Item		RX66T (ICUb)	RX660 (ICUF)
Return from low power consumption state	Sleep mode	Exit sleep mode by any interrupt source.	Exit sleep mode by any interrupt source.
	All-module clock stop mode	Exit all-module clock stop mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection, USB0 resume, IWDT, or TMR0 to 3).	Exit all-module clock stop mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection interrupt, RTC alarm, RTC period, IWDT, REMC interrupt, or software configurable interrupt 146 to 157).
	Software standby mode	Exit software standby mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB0 resume, or IWDT).	Exit software standby mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, RTC alarm, RTC period, IWDT, or REMC interrupt).
	Deep software standby mode	Exit deep software standby mode by NMI pin interrupt, any among a subset of external pin interrupts, or peripheral interrupt (voltage monitoring 1 or voltage monitoring 2).	Exit deep software standby mode by NMI pin interrupt, any among a subset of external pin interrupts, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, RTC alarm, or RTC period).

Table 2.13 Comparison of Interrupt Controller Registers

Register	Bit	RX66T (ICUb)	RX660 (ICUF)
GRPBE0	—	Group BE0 interrupt request register	—
GRPBL2	—	—	Group BL2 interrupt request register
GENBE0	—	Group BE0 interrupt request enable register	—
GENBL2	—	—	Group BL2 interrupt request enable register
GCRBE0	—	Group BE0 interrupt clear register	—
PIBRk	—	—	Software configurable interrupt B request register k
PIARk	—	Software configurable interrupt A request register k (k = 0h to 12h)	Software configurable interrupt A request register k (k = 0h to 5h, Bh, Ch)
SLIBXRn	—	—	Software configurable interrupt B source select register Xn
SLIBRn	—	—	Software configurable interrupt B source select register n

2.9 Buses

Table 2.14 is Comparative Overview of Buses, and Table 2.15 is Comparison of Bus Registers.

Table 2.14 Comparative Overview of Buses

Item		RX66T	RX660
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ECCRAM, or code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ECCRAM, or code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	Connected to RAM	Connected to RAM
	Memory bus 2	Connected to ROM	Connected to code flash memory
	Memory bus 3	Connected to ECCRAM	—
Internal main buses	Internal main bus 1	• Connected to CPU • Operates in synchronization with the system clock (ICLK)	• Connected to CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DTC and DMAC • Connected to on-chip memory (RAM, ECCRAM, or code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the DTC and DMAC • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)

Item		RX66T	RX660
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (TFU, DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 3	• Connected to peripheral modules (USBb and CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (DOC, REMC, CANFD, CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 4	• Connected to peripheral modules (MTU3, GPTW, HRPWM, RSPI, and SCIi) • Operates in synchronization with the peripheral-module clock (PCLKA)	• Connected to peripheral modules (MTU, RSPI, SCIi) • Operates in synchronization with the peripheral-module clock (PCLKA)
	Internal peripheral bus 5	Reserved area	• Connected to peripheral modules (RSCI, CANFD) • Operates in synchronization with the peripheral-module clock (PCLKA)
	Internal peripheral bus 6	• Connected to code flash memory (in P/E) and data flash memory • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to code flash memory (in P/E) and data flash memory • Operates in synchronization with the FlashIF clock (FCLK)
External bus	CS area	• Connected to an external device • Operates in synchronization with the external bus clock (BCLK)	• Connected to an external device • Operates in synchronization with the external bus clock (BCLK)

Table 2.15 Comparison of Bus Registers

Register	Bit	RX66T	RX660
BUSPRI	BPHB[1:0]	Priority control bits for internal peripheral buses 4 and 5	Internal peripheral bus 4 priority control bits
	BPEB[1:0]	—	External bus priority control bits

2.10 Data Transfer Controller

Table 2.16 is Comparative Overview of Data Transfer Controllers, and Table 2.17 is Comparison of Data Transfer Controller Registers.

Table 2.16 Comparative Overview of Data Transfer Controllers

Item	RX66T (DTCa)	RX660 (DTCb)
Number of transfer channels	Equal to number of all interrupt sources that can start a DTC transfer.	Equal to number of all interrupt sources that can start a DTC transfer.
Transfer modes	• Normal transfer mode — A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address returns to the transfer start address when the number of data transfers equals the repeat size. — The maximum number of repeat transfers is 256 and the maximum data transfer size is 256 × 32 bits, or 1,024 bytes. • Block transfer mode — A single activation leads to the transfer of a single block of data. — The maximum block size is 256 × 32 bits = 1,024 bytes.	• Normal transfer mode — A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address returns to the transfer start address when the number of data transfers equals the repeat size. — The maximum number of repeat transfers is 256 and the maximum data transfer size is 256 × 32 bits, or 1,024 bytes. • Block transfer mode — A single activation leads to the transfer of a single block of data. — The maximum block size is 256 × 32 bits = 1,024 bytes.
Chain transfer function	• Multiple types of data transfer can be performed sequentially in response to a single transfer request. • Either “performed only when the transfer counter reaches 0” or “every time” can be selected.	• Multiple types of data transfer can be performed sequentially in response to a single transfer request. • Either “performed only when the transfer counter reaches 0” or “every time” can be selected.
Sequence transfer	—	A complex series of transfers can be registered as a sequence. Any sequence can be selected by the transfer data and executed. • Only one sequence transfer trigger source can be selected at a time. • Up to 256 sequences can correspond to a single trigger source. • The data that is initially transferred in response to a transfer request determines the sequence. • The entire sequence can be executed on a single request, or the sequence can be suspended in the middle and resumed on the next transfer request (sequence division).

Item	RX66T (DTCa)	RX660 (DTCb)
Transfer space	• 16 MB in short-address mode (from 0000 0000h to 007F FFFFh or from FF80 0000h to FFFF FFFFh, excluding reserved areas) • 4 GB in full-address mode (within 0000 0000h to FFFF FFFFh, excluding reserved areas)	• 16 MB in short-address mode (from 0000 0000h to 007F FFFFh or from FF80 0000h to FFFF FFFFh, excluding reserved areas) • 4 GB in full-address mode (within 0000 0000h to FFFF FFFFh, excluding reserved areas)
Data transfer units	• Single data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data units	• Single data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data units
CPU interrupt requests	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.
Event link function	An event link request is generated after one data transfer (for block transfers, after one block).	An event link request is generated after one data transfer (for block transfers, after one block).
Read skip	Reading of the transfer information can be skipped when the same transfer is repeated.	Reading of the transfer information can be skipped when the same transfer is repeated.
Write-back skip	Write-back of transferred data that is not updated can be skipped when the address of the transfer source or	Write-back of transferred data that is not updated can be skipped when the address of the transfer source or
Write-back disable	—	Ability to disable write-back of transfer information
Displacement addition	—	Ability to add displacement to the transfer source address (selectable by each transfer information)
Low power consumption function	Transition to the module stop state is possible.	Transition to the module stop state is possible.

Table 2.17 Comparison of Data Transfer Controller Registers

Register	Bit	RX66T (DTCa)	RX660 (DTCb)
MRA	WBDIS	—	Write-back disable bit(Note 1)
MRB	SQEND	—	Sequence transfer end bit
	INDX	—	Index table reference bit
MRC	—	—	DTC mode register C
DTCIBR	—	—	DTC index table base register
DTCOR	—	—	DTC operation register
DTCSQE	—	—	DTC sequence transfer enable register
DTCDISP	—	—	DTC address displacement register

Note 1. Transfer information is usually allocated to a RAM area, but it can be allocated to a ROM area by setting the MRA.WBDIS bit to 1 (no write-back).

2.11 Event Link Controller

Table 2.18 is Comparative Overview of Event Link Controllers, Table 2.19 is Comparison of Event Link Controller Registers, Table 2.20 is Correspondence between ELSRn Registers and Peripheral Modules, and Table 2.21 is Correspondence between Values Set in ELSRn.ELS[7:0] Bits and Event Signal Names and Numbers.

Table 2.18 Comparative Overview of Event Link Controllers

Item	RX66T (ELC)	RX660 (ELC)
Event link function	• 188 types of event signals can be directly connected to peripheral modules. • The operation of peripheral timer modules at event input is selectable. • Event link operation is possible for port B and port E. — Single port: Event link operation can be enabled for a single specified port. — Port group: Event link operation can be enabled for multiple specified ports within a group of up to eight ports.	• 83 types of event signals can be directly connected to peripheral modules. • The operation of peripheral timer modules at event input is selectable. • Event link operation is possible for port B and port E. — Single port: Event link operation can be enabled for a single specified port. — Port group: Event link operation can be enabled for multiple specified ports within a group of up to eight ports.
Low power consumption function	Transition to the module stop state is possible.	Transition to the module stop state is possible.

Table 2.19 Comparison of Event Link Controller Registers

Register	Bit	RX66T (ELC)	RX660 (ELC)
ELSRn	—	Event link setting register n (n = 0, 3, 4, 7, 10 to 13, 15, 16, 18 to 28, 30, 31, or 45 to 58)	Event link setting register n (n = 0, 3, 4, 7, 10 to 13, 15, 16, 18 to 28, 30, 31, 32, or 56)
ELOPE	MTU8MD [1:0]	—	MTU8 operation select bits
	MTU9MD [1:0]	MTU9 operation select bits	—

Table 2.20 Correspondence between ELSRn Registers and Peripheral Modules

Register	RX66T (ELC)	RX660 (ELC)
ELSR0	MTU0	MTU0
ELSR3	MTU3	MTU3
ELSR4	MTU4	MTU4
ELSR7	CMT1	CMT1
ELSR10	TMR0	TMR0
ELSR11	TMR1	TMR1
ELSR12	TMR2	TMR2
ELSR13	TMR3	TMR3
ELSR15	S12AD (ELCTRG00N)	S12AD (ELCTRG00N)
ELSR16	DA0	DA0
ELSR18	ICU (interrupt 1)	ICU (interrupt 1)
ELSR19	ICU (interrupt 2)	ICU (interrupt 2)
ELSR20	Output port group 1	Output port group 1
ELSR21	Output port group 2	Output port group 2
ELSR22	Input port group 1	Input port group 1
ELSR23	Input port group 2	Input port group 2
ELSR24	Single port 0	Single port 0
ELSR25	Single port 1	Single port 1
ELSR26	Single port 2	Single port 2
ELSR27	Single port 3	Single port 3
ELSR28	Clock source switching to LOCO	Clock source switching to LOCO
ELSR30	MTU6	MTU6
ELSR31	MTU7	MTU7
ELSR32	—	MTU8
ELSR45	S12AD1 (ELCTRG10N)	—
ELSR46	S12AD2 (ELCTRG20N)	—
ELSR47	MTU9	—
ELSR48	GPTW event cause A (common to all channels)	—
ELSR49	GPTW event cause B (common to all channels)	—
ELSR50	GPTW event cause C (common to all channels)	—
ELSR51	GPTW event cause D (common to all channels)	—
ELSR52	GPTW event cause E (common to all channels)	—
ELSR53	GPTW event cause F (common to all channels)	—
ELSR54	GPTW event cause G (common to all channels)	—
ELSR55	GPTW event cause H (common to all channels)	—
ELSR56	S12AD (ELCTRG01N)	S12AD (ELCTRG01N)
ELSR57	S12AD1(ELCTRG11N)	—
ELSR58	S12AD2(ELCTRG21N)	—

Table 2.21 Correspondence between Values Set in ELSRn.ELS[7:0] Bits and Event Signal Names and Numbers

ELS[7:0] Value of Bits	Peripheral Module (RX66T)	RX66T (ELC)	Peripheral Module (RX660)	RX660 (ELC)
01h	Multi-function timer pulse unit 3	MTU0 compare match 0A	Multi-function timer pulse unit 3	MTU0 compare match 0A
02h		MTU0 compare match 0B		MTU0 compare match 0B
03h		MTU0 compare match 0C		MTU0 compare match 0C
04h		MTU0 compare match 0D		MTU0 compare match 0D
05h		MTU0 compare match 0E		MTU0 compare match 0E
06h		MTU0 compare match 0F		MTU0 compare match 0F
07h		MTU0 overflow		MTU0 overflow
10h		MTU3 compare match 3A		MTU3 compare match 3A
11h		MTU3 compare match 3B		MTU3 compare match 3B
12h		MTU3 compare match 3C		MTU3 compare match 3C
13h		MTU3 compare match 3D		MTU3 compare match 3D
14h		MTU3 overflow		MTU3 overflow
15h		MTU4 compare match 4A		MTU4 compare match 4A
16h		MTU4 compare match 4B		MTU4 compare match 4B
17h		MTU4 compare match 4C		MTU4 compare match 4C
18h		MTU4 compare match 4D		MTU4 compare match 4D
19h		MTU4 overflow		MTU4 overflow
1Ah		MTU4 underflow		MTU4 underflow
1Eh		MTU6 compare match 6A		MTU6 compare match 6A
1Fh		MTU6 compare match 6B		MTU6 compare match 6B
20h		MTU6 compare match 6C		MTU6 compare match 6C
21h		MTU6 compare match 6D		MTU6 compare match 6D
22h		MTU6 overflow		MTU6 overflow
23h		MTU7 compare match 7A		MTU7 compare match 7A
24h		MTU7 compare match 7B		MTU7 compare match 7B
25h		MTU7 compare match 7C		MTU7 compare match 7C
26h		MTU7 compare match 7D		MTU7 compare match 7D
27h		MTU7 overflow		MTU7 overflow
28h		MTU7 underflow		MTU7 underflow
29h		—		MTU8 compare match 8A
2Ah		—		MTU8 compare match 8B
2Bh		—		MTU8 compare match 8C
2Ch		—		MTU8 compare match 8D
2Dh		—		MTU8 overflow
2Fh		MTU9 compare match 9A		—
30h		MTU9 compare match 9B		—
31h		MTU9 compare match 9C		—
32h		MTU9 compare match 9D		—
33h		MTU9 compare match 9E		—
34h		MTU9 compare match 9F		—
35h		MTU9 overflow		—
37h	Compare match timer	CMT1 compare match 1	Compare match timer	CMT1 compare match 1

ELS[7:0] Value of Bits	Peripheral Module (RX66T)	RX66T (ELC)	Peripheral Module (RX660)	RX660 (ELC)
3Ch	8-bit timer	TMR0 compare match A0	8-bit timer	TMR0 compare match A0
3Dh		TMR0 compare match B0		TMR0 compare match B0
3Eh		TMR0 overflow		TMR0 overflow
3Fh		TMR1 compare match A1		TMR1 compare match A1
40h		TMR1 compare match B1		TMR1 compare match B1
41h		TMR1 overflow		TMR1 overflow
42h		TMR2 compare match A2		TMR2 compare match A2
43h		TMR2 compare match B2		TMR2 compare match B2
44h		TMR2 overflow		TMR2 overflow
45h		TMR3 compare match A3		TMR3 compare match A3
46h		TMR3 compare match B3		TMR3 compare match B3
47h		TMR3 overflow		TMR3 overflow
48h	General purpose PWM timer	GPTW0 compare match A	—	—
49h		GPTW0 compare match B	—	—
4Ah		GPTW0 compare match C	—	—
4Bh		GPTW0 compare match D	—	—
4Ch		GPTW0 compare match E	—	—
4Dh		GPTW0 compare match F	—	—
4Eh		GPTW0 overflow	—	—
4Fh		GPTW0 underflow	—	—
50h		GPTW0 A/D conversion start request A	—	—
51h		A/D conversion start request B	—	—
52h		GPTW1 compare match A	—	—
53h		GPTW1 compare match B	—	—
54h		GPTW1 compare match C	—	—
55h		GPTW1 compare match D	—	—
56h		GPTW1 compare match E	—	—
57h		GPTW1 compare match F	—	—
58h		GPTW1 overflow	—	—
59h		GPTW1 underflow	—	—
5Ah		GPTW1 A/D conversion start request A	—	—
5Bh		A/D conversion start request B	—	—
5Ch		GPTW2 compare match A	—	—
5Dh		GPTW2 compare match B	—	—
5Eh		GPTW2 compare match C	—	—
5Fh		GPTW2 compare match D	—	—
60h		GPTW2 compare match E	—	—
61h		GPTW2 compare match F	—	—
62h		GPTW2 overflow	—	—
63h		GPTW2 underflow	—	—
64h		GPTW2 A/D conversion start request A	—	—
65h		GPTW2 A/D conversion start request B	—	—

ELS[7:0] Value of Bits	Peripheral Module (RX66T)	RX66T (ELC)	Peripheral Module (RX660)	RX660 (ELC)
66h	General purpose PWM timer	GPTW3 compare match A	—	—
67h		GPTW3 compare match B	—	—
68h		GPTW3 compare match C	—	—
69h		GPTW3 compare match D	—	—
6Ah		GPTW3 compare match E	—	—
6Bh		GPTW3 compare match F	—	—
6Ch		GPTW3 overflow	—	—
6Dh		GPTW3 underflow	—	—
6Eh		GPTW3 A/D conversion start request A	—	—
6Fh		GPTW3 A/D conversion start request B	—	—
70h		GPTW4 compare match A	—	—
71h		GPTW4 compare match B	—	—
72h		GPTW4 compare match C	—	—
73h		GPTW4 compare match D	—	—
74h		GPTW4 compare match E	—	—
75h		GPTW4 compare match F	—	—
76h		GPTW4 overflow	—	—
77h		GPTW4 underflow	—	—
78h		GPTW4 A/D conversion start request A	—	—
79h		GPTW4 A/D conversion start request B	—	—
7Ah		GPTW5 compare match A	—	—
7Bh		GPTW5 compare match B	—	—
7Ch		GPTW5 compare match C	—	—
7Dh		GPTW5 compare match D	—	—
7Eh		GPTW5 compare match E	—	—
7Fh		GPTW5 compare match F	—	—
80h		GPTW5 overflow	—	—
81h		GPTW5 underflow	—	—
82h		GPTW5 A/D conversion start request A	—	—
83h		GPTW5 A/D conversion start request B	—	—
84h		GPTW6 compare match A	—	—
85h		GPTW6 compare match B	—	—
86h		GPTW6 compare match C	—	—
87h		GPTW6 compare match D	—	—
88h		GPTW6 compare match E	—	—
89h		GPTW6 compare match F	—	—
8Ah		GPTW6 overflow	—	—
8Bh		GPTW6 underflow	—	—
8Ch		GPTW6 A/D conversion start request A	—	—
8Dh		GPTW6 A/D conversion start request B	—	—
8Eh		GPTW7 compare match A	—	—
8Fh		GPTW7 compare match B	—	—

ELS[7:0] Value of Bits	Peripheral Module (RX66T)	RX66T (ELC)	Peripheral Module (RX660)	RX660 (ELC)
90h	General purpose PWM timer	GPTW7 compare match C	—	—
91h		GPTW7 compare match D	—	—
92h		GPTW7 compare match E	—	—
93h		GPTW7 compare match F	—	—
94h		GPTW7 overflow	—	—
95h		GPTW7 underflow	—	—
96h		GPTW7 A/D conversion start request A	—	—
97h		GPTW7 A/D conversion start request B	—	—
98h		GPTW8 compare match A	—	—
99h		GPTW8 compare match B	—	—
9Ah		GPTW8 compare match C	—	—
9Bh		GPTW8 compare match D	—	—
9Ch		GPTW8 compare match E	—	—
9Dh		GPTW8 compare match F	—	—
9Eh		GPTW8 overflow	—	—
9Fh		GPTW8 underflow	—	—
A0h		GPTW8 A/D conversion start request A	—	—
A1h		GPTW8 A/D conversion start request B	—	—
A2h		GPTW9 compare match A	—	—
A3h		GPTW9 compare match B	—	—
A4h		GPTW9 compare match C	—	—
A5h		GPTW9 compare match D	—	—
A6h		GPTW9 compare match E	—	—
A7h		GPTW9 compare match F	—	—
A8h		GPTW9 overflow	—	—
A9h		GPTW9 underflow	—	—
AAh		GPTW9 A/D conversion start request A	—	—
ABh		GPTW9 A/D conversion start request B	—	—
ACh	—	—	Realtime clock	RTC periodic event (select 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/32, 1/16, 1/8, 1/4, 1/2, 1, or 2 seconds)
AFh	Independent watchdog timer	IWDT underflow or refresh error	—	—
B8h	Serial communications interface	SCI5 error (receive error or error signal detection)	Serial communications interface	SCI5 error (receive error or error signal detection)
B9h		SCI5 receive data full	—	SCI5 receive data full
BAh		SCI5 transmit data empty	—	SCI5 transmit data empty
BBh		SCI5 transmit end	—	SCI5 transmit end

ELS[7:0] Value of Bits	Peripheral Module (RX66T)	RX66T (ELC)	Peripheral Module (RX660)	RX660 (ELC)
CCh	I²C Bus Interface	RIIC0 communication error or event generation	I²C bus interface	RIIC0 communication error or event generation
CDh		RIIC0 receive data full	—	RIIC0 receive data full
CEh		RIIC0 transmit data empty	—	RIIC0 transmit data empty
CFh		RIIC0 transmit end	—	RIIC0 transmit end
D0h	Serial peripheral interface	RSPI0 error (mode fault, overrun, underrun, or parity error)	Serial peripheral interface	RSPI0 error (mode fault, overrun, underrun, or parity error)
D1h		RSPI0 idle		RSPI0 idle
D2h		RSPI0 receive buffer full		RSPI0 receive buffer full
D3h		RSPI0 transmit buffer empty		RSPI0 transmit buffer empty
D4h		RSPI0 transmit end		RSPI0 transmit end
D6h	12-bit A/D converter	S12AD A/D conversion end	12-bit A/D converter	S12AD A/D conversion end
D8h		S12AD1 A/D conversion end		—
DAh		S12AD2 A/D conversion end		—
DCh	Comparator C	Comparator C0 comparison result change	Comparator C	Comparator C0 comparison result change
DDh		Comparator C1 comparison result change		Comparator C1 comparison result change
DEh		Comparator C2 comparison result change		Comparator C2 comparison result change
DFh		Comparator C3 comparison result change		Comparator C3 comparison result change
E0h		Comparator C4 comparison result change		—
E1h		Comparator C5 comparison result change		—
E2h	Voltage detection circuit	LVD1 voltage detection	Voltage detection circuit	LVD1 voltage detection
E3h		LVD2 voltage detection		LVD2 voltage detection
E4h	DMA controller	DMAC0 transfer end	DMA controller	DMAC0 transfer end
E5h		DMAC1 transfer end		DMAC1 transfer end
E6h		DMAC2 transfer end		DMAC2 transfer end
E7h		DMAC3 transfer end		DMAC3 transfer end
E8h	Data transfer controller	DTC transfer end	Data transfer controller	DTC transfer end
E9h	Clock generation circuit	Oscillation stop detection of the clock generation circuit	Clock generation circuit	Oscillation stop detection of the clock generation circuit
EAh	I/O ports	Input edge detection of input port group 1	I/O ports	Input edge detection of input port group 1
EBh		Input edge detection of input port group 2		Input edge detection of input port group 2
ECh		Input edge detection of single input port 0		Input edge detection of single input port 0
EDh		Input edge detection of single input port 1		Input edge detection of single input port 1

ELS[7:0] Value of Bits	Peripheral Module (RX66T)	RX66T (ELC)	Peripheral Module (RX660)	RX660 (ELC)
EEh	I/O ports	Input edge detection of single input port 2	I/O ports	Input edge detection of single input port 2
EFh		Input edge detection of single input port 3		Input edge detection of single input port 3
F0h	Event link controller	Software event	Event link controller	Software event
F1h	Data operation circuit	DOC data operation condition met	Data operation circuit	DOC data operation condition met
Settings other than the above are prohibited.				

2.12 I/O Ports

Table 2.23 to Table 2.27 provide comparative overviews of I/O ports, Table 2.28 shows Comparison of I/O Port Functions, and Table 2.30 is Comparison of I/O Port Registers.

Table 2.22 Comparative Overview of I/O Ports (144-Pin)

Port Symbol	RX66T (144-Pin)	RX660 (144-Pin)
PORT0	P00, P01	P00 to P07
PORT1	P10 to P17	P12 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P55	P50 to P56
PORT6	P60 to P65	P60 to P67
PORT7	P70 to P76	P70 to P77
PORT8	P80 to P82	P80 to P83, P86, P87
PORT9	P90 to P96	P90 to P93
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC6	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE6	PE0 to PE7
PORTF	PF0 to PF3	PF5 to PF7
PORTG	PG0 to PG2	—
PORTH	PH0 to PH7	PH0 to PH3, PH6(Note 1), PH7(Note 1)
PORTJ	—	PJ1, PJ3 to PJ7
PORTK	PK0 to PK2	PK2 to PK5
PORTL	—	PL0, PL1
PORTN	—	PN6, PN7

Note 1. PH6 and PH7 are not present on products provided with a sub-clock oscillator.

Table 2.23 Comparative Overview of I/O Ports (100-pin: Product with programmable gain amplifier (PGA) pseudo-differential input)

Port Symbol	RX66T (100-pin product without USB)	RX660 (100-Pin)
PORT0	P00, P01	P03(Note 2) to P07
PORT1	P10, P11	P12 to P17
PORT2	P20 to P24, P27	P20 to P27
PORT3	P30 to P33, P36, P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P52 to P55	P50 to P55
PORT6	P60 to P65	—
PORT7	P70 to P76	—
PORT8	P80 to P82	—
PORT9	P90 to P96	—
PORTA	PA0 to PA5	PA0 to PA7
PORTB	PB0 to PB6, PB7(Note 3)	PB0 to PB7
PORTC	—	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE5	PE0 to PE7
PORTH	PH0, PH4	PH0 to PH3, PH6(Note 1), PH7(Note 1)

Port Symbol	RX66T (100-pin product without USB)	RX660 (100-Pin)
PORTJ	—	PJ1, PJ3, PJ6, PJ7
PORTN	—	PN6

Note 1. PH6 and PH7 are not present on products provided with a sub-clock oscillator.
Note 2. P03 is not present on products provided with a JTAG.
Note 3. Not present on products provided with a USB.

Table 2.24 Comparative Overview of I/O Ports (100-pin: Product without programmable gain amplifier (PGA) pseudo-differential input)

Port Symbol	RX66T (100-Pin)	RX660 (100-Pin)
PORT0	P00, P01	P03(Note 2) to P07
PORT1	P10, P11	P12 to P17
PORT2	P20 to P24	P20 to P27
PORT3	P30 to P33, P36,P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P55	P50 to P55
PORT6	P60 to P65	—
PORT7	P70 to P76	—
PORT8	P80 to P82	—
PORT9	P90 to P96	—
PORTA	PA0 to PA5	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	—	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE5	PE0 to PE7
PORTH	—	PH0 to PH3, PH6(Note 1), PH7(Note 1)
PORTJ	—	PJ1, PJ3, PJ6, PJ7
PORTN	—	PN6

Note 1. PH6 and PH7 are not present on products provided with a sub-clock oscillator.
Note 2. P03 is not present on products provided with a JTAG.

Table 2.25 Comparative Overview of I/O Ports (80-Pin)

Port Symbol	RX66T (80-Pin)	RX660 (80-Pin)
PORT0	P00, P01	P03 to P07
PORT1	P10, P11	P12 to P17
PORT2	P20 to P22, P27	P20, P21, P26, P27
PORT3	P30, P31, P36, P37	P30 to P32, P34 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P52 to P55	P54, P55
PORT6	P62, P64, P65	—
PORT7	P70 to P76	—
PORT9	P90 to P96	—
PORTA	PA3, PA5	PA0 to PA6
PORTB	PB0 to PB6	PB0 to PB7
PORTC	—	PC2 to PC7
PORTD	PD2 to PD7	PD0 to PD2
PORTE	PE2 to PE4	PE0 to PE5
PORTH	PH0, PH4	PH0 to PH3, PH6(Note 1), PH7(Note 1)
PORTJ	—	PJ1, PJ6, PJ7

Port Symbol	RX66T (80-Pin)	RX660 (80-Pin)
PORTN	—	PN6

Note 1. PH6 and PH7 are not present on products provided with a sub-clock oscillator.
Note 2. PC0 and PC1 are only valid when selected in port switching register A.

Table 2.26 Comparative Overview of I/O Ports (64-Pin)

Port Symbol	RX66T (64-Pin)	RX660 (64-Pin)
PORT0	P00, P01	P03, P07
PORT1	P11	P14 to P17
PORT2	P20 to P22	P26, P27
PORT3	P36, P37	P30 to P32, P35 to P37
PORT4	P40 to P42, P44 to P46	P40 to P47
PORT5	P52 to P54	P54, P55
PORT6	P64, P65	—
PORT7	P70 to P76	—
PORT9	P90 to P96	—
PORTA	—	PA0, PA1, PA3, PA4, PA6
PORTB	PB0 to PB6	PB0, PB1, PB3, PB5 to PB7
PORTC	—	PC2 to PC7
PORTD	PD3 to PD7	—
PORTE	PE2	PE0 to PE5
PORTH	PH0, PH4	PH0 to PH3, PH6(Note 1), PH7(Note 1)
PORTJ	—	PJ6, PJ7
PORTN	—	PN6

Note 1. PH6 and PH7 are not present on products provided with a sub-clock oscillator.

Table 2.27 Comparative Overview of I/O Ports (48-Pin)

Port Symbol	RX66T (48-Pin)	RX660 (48-Pin)
PORT0	P00	—
PORT1	P10, P11	P14 to P17
PORT2	—	P26, P27
PORT3	P36, P37	P30, P31, P35 to P37
PORT4	P40 to P44	P40 to P42, P45 to P47
PORT6	P62, P64, P65	—
PORT7	P71 to P76	—
PORT9	P94	—
PORTA	PA3, PA5	PA1, PA3, PA4, PA6
PORTB	PB0 to PB6	PB0, PB1, PB3, PB5
PORTC	—	PC4 to PC7
PORTD	PD3, PD5, PD7	—
PORTE	PE2	PE1 to PE4
PORTH	—	PH0 to PH3
PORTJ	—	PJ6, PJ7
PORTN	—	PN6

Table 2.28 Comparison of I/O Port Functions

Item	Port Symbol	RX66T	RX660
Input pull-up function	PORT0	P00, P01	P00 to P07
	PORT1	P10 to P17	P12 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P37	P30 to P34, P36, P37
	PORT4	P43, P47	P40 to P47
	PORT5	P50 to P55	P50 to P56
	PORT6	P60 to P65	P60 to P67
	PORT7	P70 to P76	P70 to P77
	PORT8	P80 to P82	P80 to P83, P86, P87
	PORT9	P90 to P96	P90 to P93
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC6	PC0 to PC7
	PORTD	PD0 to PD7	PD0 to PD7
	PORTE	PE0 to PE1, PE3 to PE7	PE0 to PE7
	PORTF	PF0 to PF3	PF5 to PF7
	PORTG	PG0 to PG2	—
	PORTH	PH1 to PH3, PH5 to PH7	PH0 to PH3, PH6, PH7
	PORTJ	—	PJ1, PJ3 to PJ7
	PORTK	PK0 to PK2	PK2 to PK5
	PORTL	—	PL0, PL1
	PORTN	—	PN6, PN7
Open drain output function	PORT0	P00, P01	P00 to P07
	PORT1	P10 to P17	P12 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P37	P30 to P34, P36, P37
	PORT4	P43, P47	P40 to P47
	PORT5	P50 to P55	P50 to P56
	PORT6	P60 to P65	P60 to P67
	PORT7	P70 to P76	P70 to P77
	PORT8	P80 to P82	P80 to P83, P86, P87
	PORT9	P90 to P96	P90 to P93
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC6	PC0 to PC7
	PORTD	PD0 to PD7	PD0 to PD7
	PORTE	PE0 to PE1, PE3 to PE7	PE0 to PE7
	PORTF	PF0 to PF3	PF5 to PF7
	PORTG	PG0 to PG2	—
	PORTH	PH1 to PH3, PH5 to PH7	PH0 to PH3, PH6, PH7
	PORTJ	—	PJ1, PJ3 to PJ7
	PORTK	PK0 to PK2	PK2 to PK5
	PORTL	—	PL0, PL1
	PORTN	—	PN6, PN7
5 V tolerant	PORT1	—	P12, P13, P16, P17
	PORTB	PB1, PB2	—
	PORTC	PC0	—
	PORTD	PD2	—

Table 2.29 Comparison of Driving Ability Switching on I/O Ports

Port Symbol	Driving Ability Switching	RX66T	RX660
PORT0	Fixed to normal output	—	P03, P05 to P07
	Normal/high	P00, P01	P00 to P02, P04
PORT1	Fixed to normal output	—	—
	Normal/high	P10 to P17	P12 to P17
PORT2	Fixed to normal output	—	—
	Normal/high	P20 to P27	P20 to P27
PORT3	Fixed to normal output	P36, P37	P36, P37
	Normal/high	P30 to P35	P30 to P34
PORT4	Fixed to normal output	P43, P47	P40 to P47
	Normal/high	—	—
PORT5	Fixed to normal output	P50 to P55	—
	Normal/high	—	P50 to P56
PORT6	Fixed to normal output	P60 to P65	—
	Normal/high	—	P60 to P67
PORT7	Fixed to normal output	P70	—
	Normal/high	—	P70 to P77
	Normal/high/large current output	P71 to P76	—
PORT8	Fixed to normal output	—	—
	Normal/high	P80, P82	P80 to P83, P86, P87
	Normal/high/large current output	P81	—
PORT9	Fixed to normal output	—	—
	Normal/high	P96	P90 to P93
	Normal/high/large current output	P90 to P95	—
PORTA	Fixed to normal output	—	—
	Normal/high	PA0 to PA7	PA0 to PA7
PORTB	Fixed to normal output	—	—
	Normal/high	PB0 to PB4, PB6, PB7	PB0 to PB7
	Normal/high/large current output	PB5	—
PORTC	Fixed to normal output	—	—
	Normal/high	PC0 to PC6	PC0 to PC7
PORTD	Fixed to normal output	—	—
	Normal/high	PD0 to PD2, PD4 to PD7	PD0 to PD7
	Normal/high/large current output	PD3	—
PORTE	Fixed to normal output	—	—
	Normal/high	PE0 to PE1, PE3 to PE6	PE0 to PE7
PORTF	Fixed to normal output	—	—
	Normal/high	PF0 to PF3	PF5 to PF7
PORTG	Fixed to normal output	—	—
	Normal/high	PG0 to PG2	—
PORTH	Fixed to normal output	PH1 to PH3, PH5 to PH7	—
	Normal/high	—	PH0 to PH3, PH6, PH7
PORTJ	Fixed to normal output	—	PJ6, PJ7
	Normal/high	—	PJ1, PJ3 to PJ5
PORTK	Fixed to normal output	—	—
	Normal/high	PK0 to PK2	PK2 to PK5
PORTL	Fixed to normal output	—	—
	Normal/high	—	PL0, PL1
PORTN	Fixed to normal output	—	—
	Normal/high	—	PN6, PN7

Table 2.30 Comparison of I/O Port Registers

Register	Bit	RX66T	RX660
PDR	B0 to B7	Pm0 to 7 I/O select bits (m = 0 to 9, A to H, K)	Pm0 to 7 I/O select bits (m = 0 to 9, A to F, H, J to L, N)
PODR	B0 to B7	Pm0 to Pm7 output data store bits (m = 0 to 9, A to H, K)	Pm0 to Pm7 output data store bits (m = 0 to 9, A to F, H, J to L, N)
PIDR	B0 to B7	Pm0 to Pm7 bits (m = 0 to 9, A to H, K)	Pm0 to Pm7 bits (m = 0 to 9, A to F, H, J to L, N)
PMR	B0 to B7	Pm0 pin mode control bits (m = 0 to 9, A to H, K)	Pm0 to Pm7 pin mode control bits (m = 0 to 9, A to F, H, J to L, N)
ODR0	B0, B2, B4, B6	Pm0, Pm2, Pm4, and Pm6 output type select bits (m = 0 to 9, A to H, K)	Pm0, Pm2, Pm4, and Pm6 output type select bits (m = 0 to 9, A to E, H, J to L)
ODR1	B0, B2, B4, B6	Pm4, Pm5, Pm6, and Pm7 output type select bits (m = 1 to 7, 9, A to E, H)	Pm4, Pm5, Pm6, and Pm7 output type select bits (m = 0 to 8, A to F, H, J, K, N)
PCR	B0 to B7	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A to H, K)	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A to F, H, J to L, N)
DSCR	—	Drive capacity control register (m =0 to 3, 7 to 9, A to G, K)	Drive capacity control register (m = 0 to 3, 5 to 9, A to F, H, J to L, N)
DSCR2	—	Drive capacity control register 2	—

2.13 Multi-Function Pin Controller

Table 2.31 is Comparison of Multiplexed Pin Assignments, and Table 2.32 to Table 2.52 are Comparisons of Multi-Function Pin Controller Registers.

In the following comparison of the assignments of multiplexed pins, **orange text** pins that exist on the RX66T Group only and **blue text** designates pins that exist on the RX660 Group only. A circle (○) indicates that a function is assigned, a cross (×) that the pin does not exist or that no function is assigned, and grayed out items mean that the function is not implemented.

Table 2.31 Comparison of Multiplexed Pin Assignments

Module/ Function	Pin Function	Port Allocation	RX66T					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Interrupts	NMI (input)	PE2	○	○	○	○	○	×	×	×	×	×
		P35	×	×	×	×	×	○	○	○	○	○
	IRQ0-DS (input)	P10	○	○	○	×	○	×	×	×	×	×
		P30	×	×	×	×	×	○	○	○	○	○
	IRQ0 (input)	P52	○	○	○	○	×	×	×	×	×	×
		PE5	○	○	×	×	×	×	×	×	×	×
		PG0	○	×	×	×	×	×	×	×	×	×
		P50	×	×	×	×	×	○	○	×	×	×
		P60	×	×	×	×	×	○	×	×	×	×
		P70	×	×	×	×	×	○	×	×	×	×
		P90	×	×	×	×	×	○	×	×	×	×
		PA0	×	×	×	×	×	○	○	○	○	×
		PD0	×	×	×	×	×	○	○	○	×	×
		PH1	×	×	×	×	×	○	○	○	○	○
	IRQ1-DS (input)	P11	○	○	○	○	○	×	×	×	×	×
		P31	×	×	×	×	×	○	○	○	○	○
	IRQ1 (input)	P53	○	○	○	○	×	×	×	×	×	×
		PA5	○	○	○	×	○	×	×	×	×	×
		PE4	○	○	○	×	×	×	×	×	×	×
		PG1	○	×	×	×	×	×	×	×	×	×
		P51	×	×	×	×	×	○	○	×	×	×
		P61	×	×	×	×	×	○	×	×	×	×
		P71	×	×	×	×	×	○	×	×	×	×
		PD1	×	×	×	×	×	○	○	○	×	×
		PH2	×	×	×	×	×	○	○	○	○	○
	IRQ2-DS (input)	PE3	○	○	○	×	×	×	×	×	×	×
		P32	×	×	×	×	×	○	○	○	○	×
	IRQ2 (input)	P00	○	○	○	○	○	×	×	×	×	×
		P54	○	○	○	○	×	×	×	×	×	×
		PB6	○	○	○	○	○	×	×	×	×	×
		PD4	○	○	○	○	×	×	×	×	×	×
		PG2	○	×	×	×	×	×	×	×	×	×
		P12	×	×	×	×	×	○	○	○	×	×
		P52	×	×	×	×	×	○	○	×	×	×
		P62	×	×	×	×	×	○	×	×	×	×
		P82	×	×	×	×	×	○	×	×	×	×
		PB2	×	×	×	×	×	○	○	○	×	×
		PD2	×	×	×	×	×	○	○	○	×	×

Module/ Function	Pin Function	Port Allocation	RX66T					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Interrupts	IRQ3-DS (input)	PB4	○	○	○	○	○	×	×	×	×	×
		P33	×	×	×	×	×	○	○	×	×	×
	IRQ3 (input)	P34	○	×	×	×	×	×	×	×	×	×
		P55	○	○	○	×	×	×	×	×	×	×
		P82	○	○	×	×	×	×	×	×	×	×
		PE6	○	×	×	×	×	×	×	×	×	×
		P13	×	×	×	×	×	○	○	○	×	×
		P23	×	×	×	×	×	○	○	×	×	×
		P53	×	×	×	×	×	○	○	×	×	×
		P63	×	×	×	×	×	○	×	×	×	×
		P83	×	×	×	×	×	○	×	×	×	×
		PB3	×	×	×	×	×	○	○	○	○	○
		PD3	×	×	×	×	×	○	○	×	×	×
	IRQ4-DS (input)	P96	○	○	○	○	×	×	×	×	×	×
		PB1	×	×	×	×	×	○	○	○	○	○
	IRQ4 (input)	P01	○	○	○	○	×	×	×	×	×	×
		P24	○	○	×	×	×	×	×	×	×	×
		P60	○	○	×	×	×	×	×	×	×	×
		PB1	○	○	○	○	○	×	×	×	×	×
		P14	×	×	×	×	×	○	○	○	○	○
		P34	×	×	×	×	×	○	○	○	×	×
		P37	×	×	×	×	×	○	○	○	○	○
		P54	×	×	×	×	×	○	○	○	○	×
		P64	×	×	×	×	×	○	×	×	×	×
		PB4	×	×	×	×	×	○	○	○	×	×
		PD4	×	×	×	×	×	○	○	×	×	×
		PF5	×	×	×	×	×	○	×	×	×	×
	IRQ5-DS (input)	P70	○	○	○	○	×	×	×	×	×	×
		PA4	×	×	×	×	×	○	○	○	○	○
	IRQ5 (input)	P61	○	○	×	×	×	×	×	×	×	×
		P80	○	○	×	×	×	×	×	×	×	×
		PD6	○	○	○	○	×	×	×	×	×	×
		PF2	○	×	×	×	×	×	×	×	×	×
		P15	×	×	×	×	×	○	○	○	○	○
		P25	×	×	×	×	×	○	○	×	×	×
		P36	×	×	×	×	×	○	○	○	○	○
		PA5	×	×	×	×	×	○	○	○	×	×
		PC5	×	×	×	×	×	○	○	○	○	○
		PD5	×	×	×	×	×	○	○	×	×	×
		PE5	×	×	×	×	×	○	○	○	○	×
	IRQ6-DS (input)	P21	○	○	○	○	×	×	×	×	×	×
		PA3	×	×	×	×	×	○	○	○	○	○
	IRQ6 (input)	P31	○	○	○	×	×	×	×	×	×	×
		P35	○	×	×	×	×	×	×	×	×	×
		P62	○	○	○	×	○	×	×	×	×	×
		PD5	○	○	○	○	○	×	×	×	×	×
		P16	×	×	×	×	×	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX66T					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Interrupts	IRQ6 (input)	P26	×	×	×	×	×	○	○	○	○	○
		P56	×	×	×	×	×	○	×	×	×	×
		PB6	×	×	×	×	×	○	○	○	○	×
		PD6	×	×	×	×	×	○	○	×	×	×
		PE6	×	×	×	×	×	○	○	×	×	×
	IRQ7-DS (input)	P20	○	○	○	○	×	×	×	×	×	×
		PE2	×	×	×	×	×	○	○	○	○	○
	IRQ7 (input)	P30	○	○	○	×	×	×	×	×	×	×
		P63	○	○	×	×	×	×	×	×	×	×
		PA6	○	×	×	×	×	×	×	×	×	×
		PE0	○	○	×	×	×	×	×	×	×	×
		P17	×	×	×	×	×	○	○	○	○	○
		P27	×	×	×	×	×	○	○	○	○	○
		P77	×	×	×	×	×	○	×	×	×	×
		PA7	×	×	×	×	×	○	○	×	×	×
		PD7	×	×	×	×	×	○	○	×	×	×
		PE7	×	×	×	×	×	○	○	×	×	×
	IRQ8-DS (input)	PK1	○	×	×	×	×	×	×	×	×	×
		P40	×	×	×	×	×	○	○	○	○	○
	IRQ8 (input)	P64	○	○	○	○	○	×	×	×	×	×
		PB0	○	○	○	○	○	×	×	×	×	×
		PD7	○	○	○	○	○	×	×	×	×	×
		P00	×	×	×	×	×	○	×	×	×	×
		P20	×	×	×	×	×	○	○	○	×	×
		P73	×	×	×	×	×	○	×	×	×	×
		P80	×	×	×	×	×	○	×	×	×	×
		PE0	×	×	×	×	×	○	○	○	○	×
	IRQ9-DS (input)	PK2	○	×	×	×	×	×	×	×	×	×
		P41	×	×	×	×	×	○	○	○	○	○
	IRQ9 (input)	P12	○	×	×	×	×	×	×	×	×	×
		P65	○	○	○	○	○	×	×	×	×	×
		PB3	○	○	○	○	○	×	×	×	×	×
		P01	×	×	×	×	×	○	×	×	×	×
		P21	×	×	×	×	×	○	○	○	×	×
		P81	×	×	×	×	×	○	×	×	×	×
		P91	×	×	×	×	×	○	×	×	×	×
		PE1	×	×	×	×	×	○	○	○	○	○
	IRQ10-DS (input)	PC5	○	×	×	×	×	×	×	×	×	×
		P42	×	×	×	×	×	○	○	○	○	○
	IRQ10 (input)	P13	○	×	×	×	×	×	×	×	×	×
		P22	○	○	○	○	×	×	×	×	×	×
		P25	○	×	×	×	×	×	×	×	×	×
		P02	×	×	×	×	×	○	×	×	×	×
		P55	×	×	×	×	×	○	○	○	○	×
		P72	×	×	×	×	×	○	×	×	×	×
		P92	×	×	×	×	×	○	×	×	×	×
		PA2	×	×	×	×	×	○	○	○	×	×
		PC2	×	×	×	×	×	○	○	○	○	×

Module/ Function	Pin Function	Port Allocation	RX66T					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Interrupts	IRQ11-DS (input)	PC6	○	×	×	×	×	×	×	×	×	×
		P43	×	×	×	×	×	○	○	○	○	×
	IRQ11 (input)	P14	○	×	×	×	×	×	×	×	×	×
		P23	○	○	×	×	×	×	×	×	×	×
		P26	○	×	×	×	×	×	×	×	×	×
		P03	×	×	×	×	×	○	○ (Note 1)	○	○	×
		P93	×	×	×	×	×	○	×	×	×	×
		PA1	×	×	×	×	×	○	○	○	○	○
		PC3	×	×	×	×	×	○	○	○	○	×
		PE3	×	×	×	×	×	○	○	○	○	○
		PJ3	×	×	×	×	×	○	○	×	×	×
	IRQ12-DS (input)	P32	○	○	×	×	×	×	×	×	×	×
		P44	×	×	×	×	×	○	○	○	○	×
	IRQ12 (input)	P15	○	×	×	×	×	×	×	×	×	×
		PC0	○	×	×	×	×	×	×	×	×	×
		PF0	○	×	×	×	×	×	×	×	×	×
		P24	×	×	×	×	×	○	○	×	×	×
		P74	×	×	×	×	×	○	×	×	×	×
		PB0	×	×	×	×	×	○	○	○	○	○
		PC1	×	×	×	×	×	○	○	×	×	×
		PC4	×	×	×	×	×	○	○	○	○	○
		PE4	×	×	×	×	×	○	○	○	○	○
	IRQ13-DS (input)	P33	○	○	×	×	×	×	×	×	×	×
		P45	×	×	×	×	×	○	○	○	○	○
	IRQ13 (input)	P16	○	×	×	×	×	×	×	×	×	×
		PC1	○	×	×	×	×	×	×	×	×	×
		PF1	○	×	×	×	×	×	×	×	×	×
		P05	×	×	×	×	×	○	○	○	×	×
		P65	×	×	×	×	×	○	×	×	×	×
		P75	×	×	×	×	×	○	×	×	×	×
		PB5	×	×	×	×	×	○	○	○	○	○
		PC6	×	×	×	×	×	○	○	○	○	○
		PJ5	×	×	×	×	×	○	×	×	×	×
	IRQ14-DS (input)	PA1	○	○	×	×	×	×	×	×	×	×
		P46	×	×	×	×	×	○	○	○	○	○
	IRQ14 (input)	P17	○	×	×	×	×	×	×	×	×	×
		PC3	○	×	×	×	×	×	×	×	×	×
		PF3	○	×	×	×	×	×	×	×	×	×
		P66	×	×	×	×	×	○	×	×	×	×
		P76	×	×	×	×	×	○	×	×	×	×
		P86	×	×	×	×	×	○	×	×	×	×
		PA6	×	×	×	×	×	○	○	○	○	○
		PC0	×	×	×	×	×	○	○	×	×	×
		PC7	×	×	×	×	×	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX66T					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Interrupts	IRQ15-DS (input)	PK0	○	×	×	×	×	×	×	×	×	×
		P47	×	×	×	×	×	○	○	○	○	○
	IRQ15 (input)	P27	○	×	○	×	×	×	×	×	×	×
		PC2	○	×	×	×	×	×	×	×	×	×
		PE1	○	○	×	×	×	×	×	×	×	×
		P07	×	×	×	×	×	○	○	○	○	×
		P22	×	×	×	×	×	○	○	×	×	×
		P67	×	×	×	×	×	○	×	×	×	×
		P87	×	×	×	×	×	○	×	×	×	×
		PB7	×	×	×	×	×	○	○	○	○	×
Multi-function timer unit 3	MTIOC0A (input/output) or MTIOC0A# (input/output)	P31	○	○	○	×	×					
		PB3	○	○	○	○	○					
	MTIOC0A (input/output)	P34						○	○	○	×	×
		PB3						○	○	○	○	○
		PC4						○	○	○	○	○
	MTIOC0B (input/output) or MTIOC0B# (input/output)	P30	○	○	○	×	×					
		PB2	○	○	○	○	○					
		PC0	○	×	×	×	×					
	MTIOC0B (input/output)	P13						○	○	○	×	×
		P15						○	○	○	○	○
		PA1						○	○	○	○	○
	MTIOC0C (input/output) or MTIOC0C# (input/output)	P27	○	×	○	×	×					
		PB1	○	○	○	○	○					
		PC1	○	×	×	×	×					
	MTIOC0C (input/output)	P32						○	○	○	○	×
		PB1						○	○	○	○	○
		PC5						○	○	○	○	○
	MTIOC0D (input/output) or MTIOC0D# (input/output)	PB0	○	○	○	○	○					
		PC2	○	×	×	×	×					
	MTIOC0D (input/output)	P33						○	○	×	×	×
		PA3						○	○	○	○	○
	MTIOC1A (input/output) or MTIOC1A# (input/output)	P27	○	×	○	×	×					
		PA5	○	○	○	×	○					
		PC6	○	×	×	×	×					
	MTIOC1A (input/output)	P20						○	○	○	×	×
		PE4						○	○	○	○	○
	MTIOC1B (input/output) or MTIOC1B# (input/output)	PA4	○	○	×	×	×					
		PC5	○	×	×	×	×					
	MTIOC1B (input/output)	P21						○	○	○	×	×
		PB5						○	○	○	○	○
		PE3						○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX66T					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Multi-function timer unit 3	MTIOC2A (input/output) or MTIOC2A# (input/output)	P35	○	×	×	×	×					
		PA3	○	○	○	×	○					
	MTIOC2A (input/output)	P26						○	○	○	○	○
		PB5						○	○	○	○	○
	MTIOC2B (input/output) or MTIOC2B# (input/output)	P34	○	×	×	×	×					
		PA2	○	○	×	×	×					
	MTIOC2B (input/output)	P27						○	○	○	○	○
		PE5						○	○	○	○	×
	MTIOC3A (input/output) or MTIOC3A# (input/output)	P11	○	○	○	○	○					
		P33	○	○	×	×	×					
	MTIOC3A (input/output)	P14						○	○	○	○	○
		P17						○	○	○	○	○
		PC1						○	○	×	×	×
		PC7						○	○	○	○	○
		PJ1						○	○	○	×	×
	MTIOC3B (input/output) or MTIOC3B# (input/output)	P12	○	×	×	×	×					
		P71	○	○	○	○	○					
	MTIOC3B (input/output)	P17						○	○	○	○	○
		P22						○	○	×	×	×
		P80						○	×	×	×	×
		PA1						○	○	○	○	○
		PB7						○	○	○	○	×
		PC5						○	○	○	○	○
		PE1						○	○	○	○	○
		PH0						○	○	○	○	○
	MTIOC3C (input/output) or MTIOC3C# (input/output)	P32	○	○	×	×	×					
	MTIOC3C (input/output)	P16						○	○	○	○	○
		P56						○	×	×	×	×
		PC0						○	○	×	×	×
		PC6						○	○	○	○	○
		PJ3						○	○	×	×	×
	MTIOC3D (input/output) or MTIOC3D# (input/output)	P15	○	×	×	×	×					
		P74	○	○	○	○	○					
	MTIOC3D (input/output)	P16						○	○	○	○	○
		P23						○	○	×	×	×

Module/ Function	Pin Function	Port Allocation	RX66T					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Multi-function timer unit 3	MTIOC3D (input/output)	P81						○	×	×	×	×
		PA6						○	○	○	○	○
		PB0						○	○	○	○	○
		PB6						○	○	○	○	×
		PC4						○	○	○	○	○
		PE0						○	○	○	○	×
		PH1						○	○	○	○	○
	MTIOC4A (input/output) or MTIOC4A# (input/output)	P13	○	×	×	×	×					
		P72	○	○	○	○	○					
	MTIOC4A (input/output)	P21						○	○	○	×	×
		P24						○	○	×	×	×
		P55						○	○	○	○	×
		P82						○	×	×	×	×
		PA0						○	○	○	○	×
		PB3						○	○	○	○	○
		PE2						○	○	○	○	○
		PE4						○	○	○	○	○
	MTIOC4B (input/output) or MTIOC4B# (input/output)	P14	○	×	×	×	×					
		P73	○	○	○	○	○					
	MTIOC4B (input/output)	P17						○	○	○	○	○
		P30						○	○	○	○	○
		P54						○	○	○	○	×
		PC2						○	○	○	○	×
		PD1						○	○	○	×	×
		PE3						○	○	○	○	○
	MTIOC4C (input/output) or MTIOC4C# (input/output)	P16	○	×	×	×	×					
		P75	○	○	○	○	○					
	MTIOC4C (input/output)	P25						○	○	×	×	×
		P83						○	×	×	×	×
		P87						○	×	×	×	×
		PA4						○	○	○	○	○
		PB1						○	○	○	○	○
		PE1						○	○	○	○	○
		PE5						○	○	○	○	×
		PH2						○	○	○	○	○
	MTIOC4D (input/output) or MTIOC4D# (input/output)	P17	○	×	×	×	×					
		P76	○	○	○	○	○					
	MTIOC4D (input/output)	P31						○	○	○	○	○
		P55						○	○	○	○	×

Module/ Function	Pin Function	Port Allocation	RX66T					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Multi-function timer unit 3	MTIOC4D (input/output)	P86						○	×	×	×	×
		PA3						○	○	○	○	○
		PC3						○	○	○	○	×
		PD2						○	○	○	×	×
		PE4						○	○	○	○	○
		PH3						○	○	○	○	○
	MTIC5U (input/output) or MTIC5U# (input/output)	P24	○	○	×	×	×					
		P82	○	○	×	×	×					
	MTIC5U (input)	P12						○	○	○	×	×
		PA4						○	○	○	○	○
		PD7						○	○	×	×	×
	MTIC5V (input/output) or MTIC5V# (input/output)	P23	○	○	×	×	×					
		P81	○	○	×	×	×					
	MTIC5V (input)	PA3						○	○	○	○	○
		PA6						○	○	○	○	○
		PD6						○	○	×	×	×
	MTIC5W (input/output) or MTIC5W# (input/output)	P22	○	○	○	○	×					
		P80	○	○	×	×	×					
	MTIC5W (input)	PB0						○	○	○	○	○
		PD5						○	○	×	×	×
	MTIOC6A (input/output) or MTIOC6A# (input/output)	PA1	○	○	×	×	×					
	MTIOC6A (input/output)	PE7						○	○	×	×	×
	MTIOC6B (input/output) or MTIOC6B# (input/output)	P95	○	○	○	○	×					
	MTIOC6B (input/output)	PA5						○	○	○	×	×
		PA6						○	○	○	○	×
	MTIOC6C (input/output) or MTIOC6C# (input/output)	PA0	○	○	×	×	×					
	MTIOC6C (input/output)	PE6						○	○	×	×	×
	MTIOC6D (input/output) or MTIOC6D# (input/output)	P92	○	○	○	○	×					

Module/ Function	Pin Function	Port Allocation	RX66T					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Multi-function timer unit 3	MTIOC6D (input/output)	PA0						○	○	○	○	×
	MTIOC7A (input/output) or MTIOC7A# (input/output)	P94	○	○	○	○	○					
	MTIOC7A (input/output)	PA2						○	○	○	×	×
		PE2						○	○	○	○	○
	MTIOC7B (input/output) or MTIOC7B# (input/output)	P93	○	○	○	○	×					
	MTIOC7B (input/output)	PA1						○	○	○	○	○
	MTIOC7C (input/output) or MTIOC7C# (input/output)	P91	○	○	○	○	×					
	MTIOC7C (input/output)	P67						○	×	×	×	×
		PA4						○	○	○	○	○
	MTIOC7D (input/output) or MTIOC7D# (input/output)	P90	○	○	○	○	×					
	MTIOC7D (input/output)	P66						○	×	×	×	×
		PE4						○	○	○	○	○
	MTIOC8A (input/output)	PD6						○	○	×	×	×
	MTIOC8B (input/output)	PD4						○	○	×	×	×
	MTIOC8C (input/output)	PD5						○	○	×	×	×
	MTIOC8D (input/output)	PD3						○	○	×	×	×
	MTIOC9A (input/output) or MTIOC9A# (input/output)	P00	○	○	○	○	○					
		P21	○	○	○	○	×					
		P26	○	×	×	×	×					
		P35	○	×	×	×	×					
		PD7	○	○	○	○	○					
	MTIOC9B (input/output)	P22	○	○	○	○	×					
	MTIOC9B (input/output) or MTIOC9B# (input/output)	P10	○	○	○	×	○					
		P34	○	×	×	×	×					
		PC4	○	×	×	×	×					
		PE0	○	○	×	×	×					
	MTIOC9C (input/output) or MTIOC9C# (input/output)	P01	○	○	○	○	×					
		P20	○	○	○	○	×					
		P25	○	×	×	×	×					

Module/ Function	Pin Function	Port Allocation	RX66T					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Multi-function timer unit 3	MTIOC9C (input/output) or MTIOC9C# (input/output)	PC6	○	×	×	×	×					
		PD6	○	○	○	○	×					
	MTIOC9D (input/output)	P11	○	○	○	○	○					
	MTIOC9D (input/output) or MTIOC9D# (input/output)	PC3	○	×	×	×	×					
		PC5	○	×	×	×	×					
		PE1	○	○	×	×	×					
		PE5	○	○	×	×	×					
	MTCLKA (input) or MTCLKA# (input)	P21	○	○	○	○	×					
		P33	○	○	×	×	×					
		PA7	○	×	×	×	×					
	MTCLKA (input)	P14						○	○	○	○	○
		P24						○	○	×	×	×
		PA4						○	○	○	○	○
		PC6						○	○	○	○	○
	MTCLKB (input) or MTCLKB# (input)	P20	○	○	○	○	×					
		P32	○	○	×	×	×					
		PA6	○	×	×	×	×					
	MTCLKB (input)	P15						○	○	○	○	○
		P25						○	○	×	×	×
		PA6						○	○	○	○	○
		PC7						○	○	○	○	○
	MTCLKC (input) or MTCLKC# (input)	P11	○	○	○	○	○					
		P31	○	○	○	×	×					
		PA7	○	×	×	×	×					
		PE4	○	○	○	×	×					
	MTCLKC (input)	P22						○	○	×	×	×
		PA1						○	○	○	○	○
		PC4						○	○	○	○	○
	MTCLKD (input) or MTCLKD# (input)	P10	○	○	○	×	○					
		P22	○	○	○	○	×					
		P30	○	○	○	×	×					
		PA6	○	×	×	×	×					
		PE3	○	○	○	×	×					
	MTCLKD (input)	P23						○	○	×	×	×
		PA3						○	○	○	○	○
		PC5						○	○	○	○	○
	ADSM0 (output)	PA7	○	×	×	×	×					
		PB2	○	○	○	○	○					
		PC2	○	×	×	×	×					
	ADSM1 (output)	PA6	○	×	×	×	×					
		PB1	○	○	○	○	○					
		PC1	○	×	×	×	×					

Module/ Function	Pin Function	Port Allocation	RX66T					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
General purpose PWM timer	GTIOC0A (input/output) or GTIOC0A# (input/output)	P12	○	×	×	×	×					
		P71	○	○	○	○	○					
		PD2	○	○	○	×	×					
		PD7	○	○	○	○	○					
		PG1	○	×	×	×	×					
	GTIOC0B (input/output) or GTIOC0B# (input/output)	P15	○	×	×	×	×					
		P74	○	○	○	○	○					
		PD1	○	○	×	×	×					
		PD6	○	○	○	○	×					
		PG2	○	×	×	×	×					
	GTIOC1A (input/output) or GTIOC1A# (input/output)	P13	○	×	×	×	×					
		P72	○	○	○	○	○					
		PD0	○	○	×	×	×					
		PD5	○	○	○	○	○					
		PK2	○	×	×	×	×					
	GTIOC1B (input/output) or GTIOC1B# (input/output)	P16	○	×	×	×	×					
		P75	○	○	○	○	○					
		PB7	○	○	×	×	×					
		PD4	○	○	○	○	×					
		PG0	○	×	×	×	×					
	GTIOC2A (input/output) or GTIOC2A# (input/output)	P14	○	×	×	×	×					
		P73	○	○	○	○	○					
		PB6	○	○	○	○	○					
		PD3	○	○	○	○	○					
		PK0	○	×	×	×	×					
	GTIOC2B (input/output) or GTIOC2B# (input/output)	P17	○	×	×	×	×					
		P76	○	○	○	○	○					
		PB5	○	○	○	○	○					
		PD2	○	○	○	×	×					
		PK1	○	×	×	×	×					
	GTIOC3A (input/output) or GTIOC3A# (input/output)	P32	○	○	×	×	×					
		PD1	○	○	×	×	×					
		PD7	○	○	○	○	○					
		PE5	○	○	×	×	×					
	GTIOC3B (input/output) or GTIOC3B# (input/output)	P11	○	○	○	○	○					
		P33	○	○	×	×	×					
		PD0	○	○	×	×	×					
		PD6	○	○	○	○	×					
	GTIOC4A (input/output) or GTIOC4A# (input/output)	P71	○	○	○	○	○					
		P95	○	○	○	○	×					
	GTIOC4B (input/output) or GTIOC4B# (input/output)	P74	○	○	○	○	○					
		P92	○	○	○	○	×					

Module/ Function	Pin Function	Port Allocation	RX66T					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
General purpose PWM timer	GTIOC5A (input/output) or GTIOC5A# (input/output)	P72	○	○	○	○	○					
		P94	○	○	○	○	○					
	GTIOC5B (input/output) or GTIOC5B# (input/output)	P75	○	○	○	○	○					
		P91	○	○	○	○	×					
	GTIOC6A (input/output) or GTIOC6A# (input/output)	P73	○	○	○	○	○					
		P93	○	○	○	○	×					
	GTIOC6B (input/output) or GTIOC6B# (input/output)	P76	○	○	○	○	○					
		P90	○	○	○	○	×					
	GTIOC7A (input/output) or GTIOC7A# (input/output)	P12	○	×	×	×	×					
		P95	○	○	○	○	×					
	GTIOC7B (input/output) or GTIOC7B# (input/output)	P15	○	×	×	×	×					
		P92	○	○	○	○	×					
	GTIOC8A (input/output) or GTIOC8A# (input/output)	P13	○	×	×	×	×					
		P94	○	○	○	○	○					
	GTIOC8B (input/output) or GTIOC8B# (input/output)	P16	○	×	×	×	×					
		P91	○	○	○	○	×					
	GTIOC9A (input/output) or GTIOC9A# (input/output)	P14	○	×	×	×	×					
		P93	○	○	○	○	×					
	GTIOC9B (input/output) or GTIOC9B# (input/output)	P17	○	×	×	×	×					
		P90	○	○	○	○	×					
	GTETRGA (input)	P01	○	○	○	○	×					
		P11	○	○	○	○	○					
		P70	○	○	○	○	×					
		P96	○	○	○	○	×					
		PB4	○	○	○	○	○					
		PD5	○	○	○	○	○					
		PE3	○	○	○	×	×					
		PE4	○	○	○	×	×					
		PE6	○	×	×	×	×					

Module/ Function	Pin Function	Port Allocation	RX66T					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
General purpose PWM timer	GTETRGA (input)	PF3	○	×	×	×	×					
		PG2	○	×	×	×	×					
	GTETRGB (input)	P01	○	○	○	○	×					
		P10	○	○	○	×	○					
		P34	○	×	×	×	×					
		P70	○	○	○	○	×					
		P96	○	○	○	○	×					
		PB4	○	○	○	○	○					
		PD4	○	○	○	○	×					
		PE3	○	○	○	×	×					
		PE4	○	○	○	×	×					
		PE5	○	○	×	×	×					
		PE6	○	×	×	×	×					
		PF2	○	×	×	×	×					
	GTETRGC (input)	P01	○	○	○	○	×					
		P11	○	○	○	○	○					
		P70	○	○	○	○	×					
		P96	○	○	○	○	×					
		PB4	○	○	○	○	○					
		PD3	○	○	○	○	○					
		PE3	○	○	○	×	×					
		PE4	○	○	○	×	×					
		PE6	○	×	×	×	×					
		PF1	○	×	×	×	×					
	GTETRGD (input)	P01	○	○	○	○	×					
		P10	○	○	○	×	○					
		P70	○	○	○	○	×					
		P96	○	○	○	○	×					
		PB4	○	○	○	○	○					
		PE3	○	○	○	×	×					
		PE4	○	○	○	×	×					
		PE5	○	○	×	×	×					
		PE6	○	×	×	×	×					
		PF0	○	×	×	×	×					
	GTADSM0 (output)	P35	○	×	×	×	×					
		PA3	○	○	○	×	○					
		PA7	○	×	×	×	×					
		PB2	○	○	○	○	○					
		PC2	○	×	×	×	×					
	GTADSM1 (output)	P34	○	×	×	×	×					
		PA2	○	○	×	×	×					
		PA6	○	×	×	×	×					
		PB1	○	○	○	○	○					
		PC1	○	×	×	×	×					

Module/ Function	Pin Function	Port Allocation	RX66T					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Port output enable 3	POE0# (input)	P70	○	○	○	○	×	×	×	×	×	×
		P32	×	×	×	×	×	○	○	○	○	×
		P93	×	×	×	×	×	○	×	×	×	×
		PC4	×	×	×	×	×	○	○	○	○	○
		PD1	×	×	×	×	×	○	○	○	×	×
		PD7	×	×	×	×	×	○	○	×	×	×
	POE4# (input)	P96	○	○	○	○	×	×	×	×	×	×
		P33	×	×	×	×	×	○	○	×	×	×
		P92	×	×	×	×	×	○	×	×	×	×
		PB5	×	×	×	×	×	○	○	○	○	○
		PD0	×	×	×	×	×	○	○	○	×	×
		PD6	×	×	×	×	×	○	○	×	×	×
	POE8# (input)	PB4	○	○	○	○	○	×	×	×	×	×
		P17	×	×	×	×	×	○	○	○	○	○
		P30	×	×	×	×	×	○	○	○	○	○
		PD3	×	×	×	×	×	○	○	×	×	×
		PE3	×	×	×	×	×	○	○	○	○	○
		PJ5	×	×	×	×	×	○	×	×	×	×
	POE9# (input)	P11	○	○	○	○	○					
		P27	○	×	○	×	×					
	POE10# (input)	PE2	○	○	○	○	○	×	×	×	×	×
		PE4	○	○	○	×	×	×	×	×	×	×
		PE6	○	×	×	×	×	×	×	×	×	×
		P32	×	×	×	×	×	○	○	○	○	×
		P34	×	×	×	×	×	○	○	○	×	×
		PA6	×	×	×	×	×	○	○	○	○	○
		PD5	×	×	×	×	×	○	○	×	×	×
	POE11# (input)	PE3	○	○	○	×	×	×	×	×	×	×
		P33	×	×	×	×	×	○	○	×	×	×
		PB3	×	×	×	×	×	○	○	○	○	○
		PD4	×	×	×	×	×	○	○	×	×	×
	POE12# (input)	P01	○	○	○	○	×					
		P10	○	○	○	×	○					
		PK2	○	×	×	×	×					
	POE13# (input)	PK1	○	×	×	×	×					
	POE14# (input)	PK0	○	×	×	×	×					
8-bit timer	TMO0 (output)	P33	○	○	×	×	×	×	×	×	×	×
		P35	○	×	×	×	×	×	×	×	×	×
		PB0	○	○	○	○	○	×	×	×	×	×
		PD3	○	○	○	○	○	×	×	×	×	×
		P22	×	×	×	×	×	○	○	×	×	×
		PB3	×	×	×	×	×	○	○	○	○	○
		PH1	×	×	×	×	×	○	○	○	○	○
	TMCI0 (input)	P01	×	×	×	×	×	○	×	×	×	×
		P21	×	×	×	×	×	○	○	○	×	×
		PB1	○	○	○	○	○	○	○	○	○	○
		PD4	○	○	○	○	×	×	×	×	×	×
		PH3	×	×	×	×	×	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX66T					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
8-bit timer	TMRI0 (input)	P00	×	×	×	×	×	○	×	×	×	×
		P20	×	×	×	×	×	○	○	○	×	×
		PA4	×	×	×	×	×	○	○	○	○	○
		PB2	○	○	○	○	○	×	×	×	×	×
		PD5	○	○	○	○	○	×	×	×	×	×
		PH2	×	×	×	×	×	○	○	○	○	○
	TMO1 (output)	PD6	○	○	○	○	×	×	×	×	×	×
		PF0	○	×	×	×	×	×	×	×	×	×
		P17	×	×	×	×	×	○	○	○	○	○
		P26	×	×	×	×	×	○	○	○	○	○
	TMCI1 (input)	PD2	○	○	○	×	×	×	×	×	×	×
		PE0	○	○	×	×	×	×	×	×	×	×
		P02	×	×	×	×	×	○	×	×	×	×
		P12	×	×	×	×	×	○	○	○	×	×
		P54	×	×	×	×	×	○	○	○	○	×
		PC4	×	×	×	×	×	○	○	○	○	○
	TMRI1 (input)	PD7	○	○	○	○	○	×	×	×	×	×
		P24	×	×	×	×	×	○	○	×	×	×
		PB5	×	×	×	×	×	○	○	○	○	○
	TMO2 (output)	P23	○	○	×	×	×	×	×	×	×	×
		PA0	○	○	×	×	×	×	×	×	×	×
		PA7	○	×	×	×	×	×	×	×	×	×
		PD1	○	○	×	×	×	×	×	×	×	×
		P16	×	×	×	×	×	○	○	○	○	○
		PC7	×	×	×	×	×	○	○	○	○	○
	TMCI2 (input)	P24	○	○	×	×	×	×	×	×	×	×
		P15	×	×	×	×	×	○	○	○	○	○
		P31	×	×	×	×	×	○	○	○	○	○
		PC6	×	×	×	×	×	○	○	○	○	○
	TMRI2 (input)	P22	○	○	○	○	×	×	×	×	×	×
		P14	×	×	×	×	×	○	○	○	○	○
		PC5	×	×	×	×	×	○	○	○	○	○
	TMO3 (output)	P11	○	○	○	○	○	×	×	×	×	×
		PF2	○	×	×	×	×	×	×	×	×	×
		P13	×	×	×	×	×	○	○	○	×	×
		P32	×	×	×	×	×	○	○	○	○	×
		P55	×	×	×	×	×	○	○	○	○	×
	TMCI3 (input)	PA5	○	○	○	×	○	×	×	×	×	×
		P27	×	×	×	×	×	○	○	○	○	×
		P34	×	×	×	×	×	○	○	○	×	×
		PA6	×	×	×	×	×	○	○	○	○	×
	TMRI3 (input)	P10	○	○	○	×	○	×	×	×	×	×
		P30	×	×	×	×	×	○	○	○	○	×
		P33	×	×	×	×	×	○	○	×	×	×
	TMO4 (output)	P22	○	○	○	○	×					
		P34	○	×	×	×	×					
		P82	○	○	×	×	×					

Module/ Function	Pin Function	Port Allocation	RX66T					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
8-bit timer	TMO4 (output)	PA1	○	○	×	×	×					
		PD2	○	○	○	×	×					
	TMCI4 (input)	P21	○	○	○	○	×					
		P81	○	○	×	×	×					
	TMRI4 (input)	P20	○	○	○	○	×					
		P80	○	○	×	×	×					
	TMO5 (output)	PE1	○	○	×	×	×					
		PF1	○	×	×	×	×					
	TMCI5 (input)	PE0	○	○	×	×	×					
	TMRI5 (input)	PD7	○	○	○	○	○					
	TMO6 (output)	P24	○	○	×	×	×					
		P32	○	○	×	×	×					
		PA6	○	×	×	×	×					
		PD0	○	○	×	×	×					
	TMCI6 (input)	P30	○	○	○	×	×					
		PD4	○	○	○	○	×					
	TMRI6 (input)	P31	○	○	○	×	×					
		PD5	○	○	○	○	○					
	TMO7 (output)	PA2	○	○	×	×	×					
		PF3	○	×	×	×	×					
	TMCI7 (input)	PA4	○	○	×	×	×					
	TMRI7 (input)	PA3	○	○	○	×	○					
Serial communications interface	RXD0 (input) or SMISO0 (input/output) or SSCL0 (input/output)	P21						○	○	○	×	×
		P33						○	○	×	×	×
	TXD0 (output) or SMOSI0 (input/output) or SSDA0 (input/output)	P20						○	○	○	×	×
		P32						○	○	○	×	×
	SCK0 (input/output)	P22						○	○	×	×	×
		P34						○	○	○	×	×
	CTS0# (input) or RTS0# (output) or SS0# (input)	P23						○	○	×	×	×
		PJ3						○	○	×	×	×
	RXD1 (input) or SMISO1 (input/output) or SSCL1 (input/output)	P34	○	×	×	×	×	×	×	×	×	×
		PC3	○	×	×	×	×	×	×	×	×	×
		PD5	○	○	○	○	○	×	×	×	×	×
		P15	×	×	×	×	×	○	○	○	○	○
		P30	×	×	×	×	×	○	○	○	○	○
	TXD1 (output) or SMOSI1 (input/output) or SSDA1 (input/output)	P35	○	×	×	×	×	×	×	×	×	×
		PC4	○	×	×	×	×	×	×	×	×	×
		PD3	○	○	○	○	○	×	×	×	×	×
		P16	×	×	×	×	×	○	○	○	○	○
		P26	×	×	×	×	×	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX66T					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial communications interface	SCK1 (input/output)	P25	○	×	×	×	×	×	×	×	×	×
		PD4	○	○	○	○	×	×	×	×	×	×
		P17	×	×	×	×	×	○	○	○	○	○
		P27	×	×	×	×	×	○	○	○	○	○
	CTS1# (input) or RTS1# (output) or SS1# (input)	P26	○	×	×	×	×	×	×	×	×	×
		PD6	○	○	○	○	×	×	×	×	×	×
		P14	×	×	×	×	×	○	○	○	○	○
		P31	×	×	×	×	×	○	○	○	○	○
	RXD2 (input) or SMISO2 (input/output) or SSCL2 (input/output)	P12						○	○	×	×	×
		P52						○	○	×	×	×
	TXD2 (output) or SMOSI2 (input/output) or SSDA2 (input/output)	P13						○	○	×	×	×
		P50						○	○	×	×	×
	SCK2 (input/output)	P51						○	○	×	×	×
	CTS2# (input) or RTS2# (output) or SS2# (input)	P54						○	○	×	×	×
		PJ5						○	×	×	×	×
	RXD3 (input) or SMISO3 (input/output) or SSCL3 (input/output)	P16						○	○	○	○	○
		P25						○	○	×	×	×
	TXD3 (output) or SMOSI3 (input/output) or SSDA3 (input/output)	P17						○	○	○	○	○
		P23						○	○	×	×	×
	SCK3 (input/output)	P15						○	○	○	○	○
		P24						○	○	×	×	×
	CTS3# (input) or RTS3# (output) or SS3# (input)	P26						○	○	○	○	○
	RXD4 (input) or SMISO4 (input/output) or SSCL4 (input/output)	PB0						○	○	○	○	○
		PK4						○	×	×	×	×
	TXD4 (output) or SMOSI4 (input/output) or SSDA4 (input/output)	PB1						○	○	○	○	○
		PK5						○	×	×	×	×

Module/ Function	Pin Function	Port Allocation	RX66T					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial communications interface	SCK4 (input/output)	P70						○	×	×	×	×
		PB3						○	○	○	○	○
	CTS4# (input) or RTS4# (output) or SS4# (input)	PB2						○	○	○	×	×
		PE6						○	○	×	×	×
	RXD5 (input) or SMISO5 (input/output) or SSCL5 (input/output)	PA2	×	×	×	×	×	○	○	○	×	×
		PA3	×	×	×	×	×	○	○	○	○	○
		PB6	○	○	○	○	○	×	×	×	×	×
		PC2	×	×	×	×	×	○	○	○	○	×
		PE0	○	○	×	×	×	×	×	×	×	×
		PK0	○	×	×	×	×	×	×	×	×	×
	TXD5 (output) or SMOSI5 (input/output) or SSDA5 (input/output)	PA4	×	×	×	×	×	○	○	○	○	○
		PB5	○	○	○	○	○	×	×	×	×	×
		PC3	×	×	×	×	×	○	○	○	○	×
		PD7	○	○	○	○	○	×	×	×	×	×
		PK1	○	×	×	×	×	×	×	×	×	×
	SCK5 (input/output)	PA1	×	×	×	×	×	○	○	○	○	○
		PB7	○	○	×	×	×	×	×	×	×	×
		PC1	×	×	×	×	×	○	○	×	×	×
		PC4	×	×	×	×	×	○	○	○	○	○
		PD2	○	○	○	×	×	×	×	×	×	×
		PK2	○	×	×	×	×	×	×	×	×	×
	CTS5# (input) or RTS5# (output) or SS5# (input)	PA6	×	×	×	×	×	○	○	○	○	○
		PB4	○	○	○	○	○	×	×	×	×	×
		PC0	×	×	×	×	×	○	○	×	×	×
		PE1	○	○	×	×	×	×	×	×	×	×
	RXD6 (input) or SMISO6 (input/output) or SSCL6 (input/output)	P01	×	×	×	×	×	○	×	×	×	×
		P33	×	×	×	×	×	○	○	×	×	×
		P80	○	○	×	×	×	×	×	×	×	×
		PA5	○	○	○	×	○	×	×	×	×	×
		PB0	×	×	×	×	×	○	○	○	○	○
		PB1	○	○	○	○	○	×	×	×	×	×
	TXD6 (output) or SMOSI6 (input/output) or SSDA6 (input/output)	P00	×	×	×	×	×	○	×	×	×	×
		P32	×	×	×	×	×	○	○	○	○	×
		P81	○	○	×	×	×	×	×	×	×	×
		PB0	○	○	○	○	○	×	×	×	×	×
		PB1	×	×	×	×	×	○	○	○	○	○
		PB2	○	○	○	○	○	×	×	×	×	×
	SCK6 (input/output)	P02	×	×	×	×	×	○	×	×	×	×
		P34	×	×	×	×	×	○	○	○	×	×
		P82	○	○	×	×	×	×	×	×	×	×
		PA4	○	○	×	×	×	×	×	×	×	×
		PB3	○	○	○	○	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX66T					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial communications interface	CTS6# (input) or RTS6# (output) or SS6# (input)	P10	○	○	○	×	○	×	×	×	×	×
		PA2	○	○	×	×	×	×	×	×	×	×
		PB2	×	×	×	×	×	○	○	○	×	×
		PJ3	×	×	×	×	×	○	○	×	×	×
	RXD7 (input) or SMISO7 (input/output) or SSCL7 (input/output)	P92						○	×	×	×	×
	TXD7 (output) or SMOSI7 (input/output) or SSDA7 (input/output)	P55						○	×	×	×	×
		P90						○	×	×	×	×
	SCK7 (input/output)	P56						○	×	×	×	×
		P91						○	×	×	×	×
	CTS7# (input) or RTS7# (output) or SS7# (input)	P93						○	×	×	×	×
	RXD8 (input) or SMISO8 (input/output) or SSCL8 (input/output)	P22	○	○	○	○	×	×	×	×	×	×
		PA5	○	○	○	×	×	×	×	×	×	×
		PC0	○	×	×	×	×	×	×	×	×	×
		PD1	○	○	×	×	×	×	×	×	×	×
		PC6	×	×	×	×	×	○	○	○	○	○
	TXD8 (output) or SMOSI8 (input/output) or SSDA8 (input/output)	P21	○	○	○	○	×	×	×	×	×	×
		P23	○	○	×	×	×	×	×	×	×	×
		PA4	○	○	×	×	×	×	×	×	×	×
		PC1	○	×	×	×	×	×	×	×	×	×
		PD0	○	○	×	×	×	×	×	×	×	×
		PC7	×	×	×	×	×	○	○	○	○	○
	SCK8 (input/output)	P20	○	○	○	○	×	×	×	×	×	×
		P24	○	○	×	×	×	×	×	×	×	×
		P30	○	○	○	×	×	×	×	×	×	×
		PA3	○	○	○	×	×	×	×	×	×	×
		PC2	○	×	×	×	×	×	×	×	×	×
		PD2	○	○	○	×	×	×	×	×	×	×
		PC5	×	×	×	×	×	○	○	○	○	○
	CTS8# (input) or RTS8# (output) or SS8# (input)	P20	○	○	○	○	×	×	×	×	×	×
		P24	○	○	×	×	×	×	×	×	×	×
		P30	○	○	○	×	×	×	×	×	×	×
		P35	○	×	×	×	×	×	×	×	×	×
		P96	○	○	○	○	×	×	×	×	×	×
		PK1	○	×	×	×	×	×	×	×	×	×
		PC4	×	×	×	×	×	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX66T					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial communications interface	RXD9 (input) or SMISO9 (input/output) or SSCL9 (input/output)	P00	○	○	○	○	○	×	×	×	×	×
		PA2	○	○	×	×	×	×	×	×	×	×
		PG0	○	×	×	×	×	×	×	×	×	×
		PB6	×	×	×	×	×	○	○	○	○	×
		PK3	×	×	×	×	×	○	×	×	×	×
	TXD9 (output) or SMOSI9 (input/output) or SSDA9 (input/output)	P01	○	○	○	○	×	×	×	×	×	×
		PA1	○	○	×	×	×	×	×	×	×	×
		PA3	○	○	○	×	○	×	×	×	×	×
		PG1	○	×	×	×	×	×	×	×	×	×
		PB7	×	×	×	×	×	○	○	○	○	×
		PK2	×	×	×	×	×	○	×	×	×	×
	SCK9 (input/output)	PA0	○	○	×	×	×	×	×	×	×	×
		PE4	○	○	○	×	×	×	×	×	×	×
		PE5	○	○	×	×	×	×	×	×	×	×
		PG2	○	×	×	×	×	×	×	×	×	×
		P60	×	×	×	×	×	○	×	×	×	×
		PB5	×	×	×	×	×	○	○	○	○	×
	CTS9# (input) or RTS9# (output) or SS9# (input)	P34	○	×	×	×	×	×	×	×	×	×
		P70	○	○	○	○	×	×	×	×	×	×
		PE3	○	○	○	×	×	×	×	×	×	×
		PE5	○	○	×	×	×	×	×	×	×	×
		PK2	○	×	×	×	×	×	×	×	×	×
		P61	×	×	×	×	×	○	×	×	×	×
		PB4	×	×	×	×	×	○	○	○	×	×
	RXD10 (input) or SMISO10 (input/output) or SSCL10 (input/output)	P81						○	×	×	×	×
		P86						○	×	×	×	×
		PC6						○	○	○	○	○
	TXD10 (output) or SMOSI10 (input/output) or SSDA10 (input/output)	P82						○	×	×	×	×
		P87						○	×	×	×	×
		PC7						○	○	○	○	○
	SCK10 (input/output)	P80						○	×	×	×	×
		P83						○	×	×	×	×
		PC5						○	○	○	○	○
	RTS10# (output)	P80						○	×	×	×	×
	CTS10# (input) or SS10# (input)	P83						○	×	×	×	×
	CTS10# (input) or RTS10# (output) or SS10# (input)	PC4						○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX66T					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial communications interface	RXD11 (input) or SMISO11 (input/output) or SSCL11 (input/output)	PA1	○	○	×	×	×	×	×	×	×	×
		PA7	○	×	×	×	×	×	×	×	×	×
		PB6	○	○	○	○	○	○	○	○	○	×
		PC6	○	×	×	×	×	×	×	×	×	×
		PD5	○	○	○	○	○	×	×	×	×	×
		PF1	○	×	×	×	×	×	×	×	×	×
		P76	×	×	×	×	×	○	×	×	×	×
	TXD11 (output) or SMOSI11 (input/output) or SSDA11 (input/output)	PA0	○	○	×	×	×	×	×	×	×	×
		PA6	○	×	×	×	×	×	×	×	×	×
		PB5	○	○	○	○	○	×	×	×	×	×
		PC5	○	×	×	×	×	×	×	×	×	×
		PD3	○	○	○	○	○	×	×	×	×	×
		PF0	○	×	×	×	×	×	×	×	×	×
		P77	×	×	×	×	×	○	×	×	×	×
		PB7	×	×	×	×	×	○	○	○	○	×
	SCK11 (input/output)	PA2	○	○ (Note 3)	×	×	×	×	×	×	×	×
		PB4	○	○	○	○	○	×	×	×	×	×
		PB7	○	○	×	×	×	×	×	×	×	×
		PD4	○	○	○	○	×	×	×	×	×	×
		PF2	○	×	×	×	×	×	×	×	×	×
	SCK11 (input/output)	P75	×	×	×	×	×	○	×	×	×	×
		PB5	×	×	×	×	×	○	○	○	○	×
	CTS11# (input) or RTS11# (output) or SS11# (input)	PB0	○	○	○	○	○	×	×	×	×	×
		PB4	○	○	○	○	○	○	○	○	×	×
		PD6	○	○	○	○	×	×	×	×	×	×
		PF3	○	×	×	×	×	×	×	×	×	×
	RTS11# (output)	P75						○	×	×	×	×
	CTS11# (input) or SS11# (input)	P74						○	×	×	×	×
	RXD12 (input) or SMISO12 (input/output) or SSCL12 (input/output) or RXDX12 (input)	P00	○	○	○	○	○	×	×	×	×	×
		P22	○	○	○	○	×	×	×	×	×	×
		P80	○	○	×	×	×	×	×	×	×	×
		PA7	○	×	×	×	×	×	×	×	×	×
		PB6	○	○	○	○	○	×	×	×	×	×
		PC3	○	×	×	×	×	×	×	×	×	×
		PA2	×	×	×	×	×	○	○	○	×	×
		PE2	×	×	×	×	×	○	○	○	○	○
	TXD12 (output) or SMOSI12 (input/output) or SSDA12 (input/output) or TXDX12 (output) or SIOX12 (input/output)	P01	○	○	○	○	×	×	×	×	×	×
		P21	○	○	○	○	×	×	×	×	×	×
		P23	○	○	×	×	×	×	×	×	×	×
		P81	○	○	×	×	×	×	×	×	×	×
		PA6	○	×	×	×	×	×	×	×	×	×
		PB5	○	○	○	○	○	×	×	×	×	×
		PC4	○	×	×	×	×	×	×	×	×	×
		PA4	×	×	×	×	×	○	○	○	○	○
		PE1	×	×	×	×	×	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX66T					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial communications interface	SCK12 (input/output)	P82	○	○	×	×	×	×	×	×	×	×
		PB7	○	○	×	×	×	×	×	×	×	×
		PA1	×	×	×	×	×	○	○	○	○	○
		PE0	×	×	×	×	×	○	○	○	○	×
	CTS12# (input) or RTS12# (output) or SS12# (input)	PE1	○	○	×	×	×	×	×	×	×	×
		PA6	×	×	×	×	×	○	○	○	○	○
		PE3	×	×	×	×	×	○	○	○	○	○
	RXD010 (input) or SMISO010 (input/output) or SSCL010 (input/output)	P81						○	×	×	×	×
		P86						○	×	×	×	×
		PC6						○	○	○	○	○
	TXD010 (output) or SMOSI010 (input/output) or SSDA010 (input/output)	P82						○	×	×	×	×
		P87						○	×	×	×	×
		PC7						○	○	○	○	○
	SCK010 (input/output) or RTS010# (output) or DE010 (output)	P80						○	×	×	×	×
	SCK010 (input/output) or CTS010# (input) or SS010# (input)	P83						○	×	×	×	×
	SCK010 (input/output)	PC5						○	○	○	○	○
	CTS010# (input) or RTS010# (output) or SS010# (input) or DE010 (output)	PC4						○	○	○	○	○
	RXD011 (input) or SMISO011 (input/output) or SSCL011 (input/output)	P76						○	×	×	×	×
		PB6						○	○	○	○	×
		PC0						○	×	×	×	×
	TXD011 (output) or SMOSI011 (input/output) or SSDA011 (input/output)	P77						○	×	×	×	×
		PB7						○	○	○	○	×
		PC1						○	○	×	×	×
	SCK011 (input/output) or RTS011# (output) or DE011 (output)	P75						○	×	×	×	×
	SCK011 (input/output)	PB5						○	○	○	○	×
	TXDA011 (output)	PC1						○	○	×	×	×
	TXDB011 (output)	PC2						○	○	○	○	×
	CTS011# (input) or SS011# (input)	P74						○	×	×	×	×

Module/ Function	Pin Function	Port Allocation	RX66T					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial communications interface	CTS011# (input) or RTS011# (output) or SS011# (input) or DE011 (output)	PB4						○	○	○	×	×
I²C bus interface	SCL0 (input/output)	P12	×	×	×	×	×	○	○	○	×	×
		PB1	○	○	○	○	○	×	×	×	×	×
	SDA0 (input/output)	P13	×	×	×	×	×	○	○	○	×	×
		PB2	○	○	○	○	○	×	×	×	×	×
	SCL2 (input/output)	P16						○	○	○	○	○
	SDA2 (input/output)	P17						○	○	○	○	○
USB2.0FS host or function module	USB0_VBUS (input)	PC0	○	×	×	×	×					
		PD2	○	×	×	×	×					
	USB0_EXICEN (output)	PA0	○	×	×	×	×					
		PC1	○	×	×	×	×					
	USB0_VBUSEN (output)	PA0	○	×	×	×	×					
		PC1	○	×	×	×	×					
		PB5	○	×	×	×	×					
	USB0_OVRCURA (input)	PA1	○	×	×	×	×					
		PB6	○	×	×	×	×					
		PC2	○	×	×	×	×					
	USB0_OVRCURB (input)	P34	○	×	×	×	×					
		PB4	○	×	×	×	×					
USB2.0FS host or function module	USB0_OVRCURB (input)	PB7	○	×	×	×	×					
		PE0	○	×	×	×	×					
	USB0_ID (input)	PA1	○	×	×	×	×					
		PC2	○	×	×	×	×					
CAN module	CTX0 (output)	P23	○	○	×	×	×	×	×	×	×	×
		PA0	○	○	×	×	×	×	×	×	×	×
		PA6	○	×	×	×	×	×	×	×	×	×
		PB5	○	○	○	○	○	×	×	×	×	×
		PC5	○	×	×	×	×	×	×	×	×	×
		PD7	○	○	○	○	○	×	×	×	×	×
		PF2	○	×	×	×	×	×	×	×	×	×
		P14	×	×	×	×	×	○	○	○	○	○
		P32	×	×	×	×	×	○	○	○	○	×
		P54	×	×	×	×	×	○	○	○	○	×
		PD1	×	×	×	×	×	○	○	○	×	×
	CRX0 (input)	P22	○	○	○	○	×	×	×	×	×	×
		PA1	○	○	×	×	×	×	×	×	×	×
		PA7	○	×	×	×	×	×	×	×	×	×
		PB6	○	○	○	○	○	×	×	×	×	×
		PC6	○	×	×	×	×	×	×	×	×	×
		PE0	○	○	×	×	×	×	×	×	×	×
		PF3	○	×	×	×	×	×	×	×	×	×
		P15	×	×	×	×	×	○	○	○	○	○
		P33	×	×	×	×	×	○	○	×	×	×
		P55	×	×	×	×	×	○	○	○	○	×
		PD2	×	×	×	×	×	○	○	○	×	×

Module/ Function	Pin Function	Port Allocation	RX66T					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial peripheral interface	RSPCKA (input/output)	P20	○	○	○	○	×	×	×	×	×	×
		P24	○	○	×	×	×	×	×	×	×	×
		PA4	○	○	×	×	×	×	×	×	×	×
		PB3	○	○	○	○	○	×	×	×	×	×
		PD0	○	○	×	×	×	×	×	×	×	×
		PA5	×	×	×	×	×	○	○	○	×	×
		PB0	×	×	×	×	×	○	○	○	○	○
		PC5	×	×	×	×	×	○	○	○	○	○
	MOSIA (input/output)	P21	○	○	○	○	×	×	×	×	×	×
		P23	○	○	×	×	×	×	×	×	×	×
		PB0	○	○	○	○	○	×	×	×	×	×
		PD2	○	○	○	×	×	×	×	×	×	×
		P16	×	×	×	×	×	○	○	○	○	○
		PA6	×	×	×	×	×	○	○	○	○	○
		PC6	×	×	×	×	×	○	○	○	○	○
	MISOA (input/output)	P22	○	○	○	○	×	×	×	×	×	×
		PA5	○	○	○	×	○	×	×	×	×	×
		PD1	○	○	×	×	×	×	×	×	×	×
		P17	×	×	×	×	×	○	○	○	○	○
		PA7	×	×	×	×	×	○	○	×	×	×
		PC7	×	×	×	×	×	○	○	○	○	○
	SSLA0 (input/output)	P30	○	○	○	×	×	×	×	×	×	×
		PA3	○	○	○	×	○	×	×	×	×	×
		PD6	○	○	○	○	×	×	×	×	×	×
		PA4	×	×	×	×	×	○	○	○	○	○
		PC4	×	×	×	×	×	○	○	○	○	○
	SSLA1 (output)	P31	○	○	○	×	×	×	×	×	×	×
		PA2	○	○	×	×	×	×	×	×	×	×
		PD7	○	○	○	○	○	×	×	×	×	×
		PA0	×	×	×	×	×	○	○	○	○	×
		PC0	×	×	×	×	×	○	○	×	×	×
	SSLA2 (output)	P32	○	○	×	×	×	×	×	×	×	×
		PA1	○	○	×	×	×	○	○	○	○	○
		PE0	○	○	×	×	×	×	×	×	×	×
		PC1	×	×	×	×	×	○	○	×	×	×
	SSLA3 (output)	P33	○	○	×	×	×	×	×	×	×	×
		PA0	○	○	×	×	×	×	×	×	×	×
		PE1	○	○	×	×	×	×	×	×	×	×
		PA2	×	×	×	×	×	○	○	○	×	×
		PC2	×	×	×	×	×	○	○	○	○	×

Module/ Function	Pin Function	Port Allocation	RX66T					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
12-bit A/D converter	AN000 (input)	P40	○	○	○	○	○	○	○	○	○	○
	AN001 (input)	P41	○	○	○	○	○	○	○	○	○	○
	AN002 (input)	P42	○	○	○	○	○	○	○	○	○	○
	AN003 (input)	P43	○	○	○	×	○	○	○	○	○	×
	AN004 (input)	PH1	○	×	×	×	×	×	×	×	×	×
		P44	×	×	×	×	×	○	○	○	○	×
	AN005 (input)	PH2	○	×	×	×	×	×	×	×	×	×
		P45	×	×	×	×	×	○	○	○	○	○
	AN006 (input)	PH3	○	×	×	×	×	×	×	×	×	×
		P46	×	×	×	×	×	○	○	○	○	○
	AN007 (input)	PH0	○	×	○	○	×	×	×	×	×	×
		P47	×	×	×	×	×	○	○	○	○	○
	AN008 (input)	PE0						○	○	○	○	×
	AN009 (input)	PE1						○	○	○	○	○
	AN010 (input)	PE2						○	○	○	○	○
	AN011 (input)	PE3						○	○	○	○	○
	AN012 (input)	PE4						○	○	○	○	○
	AN013 (input)	PE5						○	○	○	○	×
	AN014 (input)	PE6						○	○	×	×	×
	AN015 (input)	PE7						○	○	×	×	×
	AN016 (input)	PD0						○	○	○	×	×
	AN017 (input)	PD1						○	○	○	×	×
	AN018 (input)	PD2						○	○	○	×	×
	AN019 (input)	PD3						○	○	×	×	×
	AN020 (input)	PD4						○	○	×	×	×
	AN021 (input)	PD5						○	○	×	×	×
	AN022 (input)	PD6						○	○	×	×	×
	AN023 (input)	PD7						○	○	×	×	×
	ADTRG0# (input)	P07	×	×	×	×	×	○	○	○	○	×
		P16	×	×	×	×	×	○	○	○	○	○
		P20	○	○	○	○	×	×	×	×	×	×
		P25	×	×	×	×	×	○	○	×	×	×
		PA1	○	○	×	×	×	○	○	○	○	○
		PA4	○	○	×	×	×	×	×	×	×	×
		PH0	×	×	×	×	×	○	○	○	○	○
	ADST0 (output)	P26	○	×	×	×	×	×	×	×	×	×
		PD6	○	○	○	○	×	×	×	×	×	×
		PE5	○	○	×	×	×	×	×	×	×	×
		PA4	×	×	×	×	×	○	○	○	○	○
		PH1	×	×	×	×	×	○	○	○	○	○
	PGAVSS0 (input)	PH0	○	×	○	○	×					
	AN100 (input)	P44	○	○	○	○	○					
	AN101 (input)	P45	○	○	○	○	×					
	AN102 (input)	P46	○	○	○	○	×					
	AN103 (input)	P47	○	○	○	×	×					
	AN104 (input)	PH5	○	×	×	×	×					
	AN105 (input)	PH6	○	×	×	×	×					
	AN106 (input)	PH7	○	×	×	×	×					
	AN107 (input)	PH4	○	×	○	○	×					

Module/ Function	Pin Function	Port Allocation	RX66T					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
12-bit A/D converter	ADTRG1# (input)	P21	○	○	○	○	×					
		PA5	○	○	○	×	○					
	ADST1 (output)	P00	○	○	○	○	○					
		P25	○	×	×	×	×					
	PGAVSS1 (input)	PH4	○	×	○	○	×					
	AN200 (input)	P52	○	○	○	○	×					
	AN201 (input)	P53	○	○	○	○	×					
	AN202 (input)	P54	○	○	○	○	×					
	AN203 (input)	P55	○	○	○	×	×					
	AN204 (input)	P50	○	○	×	×	×					
	AN205 (input)	P51	○	○	×	×	×					
	AN206 (input)	P60	○	○	×	×	×					
	AN207 (input)	P61	○	○	×	×	×					
	AN208 (input)	P62	○	○	○	×	○					
	AN209 (input)	P63	○	○	×	×	×					
	AN210 (input)	P64	○	○	○	○	○					
	AN211 (input)	P65	○	○	○	○	○					
	AN216 (input)	P20	○	○	○	○	×					
	AN217 (input)	P21	○	○	○	○	×					
	ADTRG2# (input)	P22	○	○	○	○	×					
		PB0	○	○	○	○	○					
	ADST2 (output)	P01	○	○	○	○	×					
		PC4	○	×	×	×	×					
	DA0 (output)	P64	○	○	○	○	○	×	×	×	×	×
		P03	×	×	×	×	×	○	○ (Note 1)	○	○	×
	DA1 (output)	P65	○	○	○	○	○	×	×	×	×	×
		P05	×	×	×	×	×	○	○	○	×	×
Clock frequency accuracy measurement circuit	CACREF (input)	P00	○	○	○	○	○	×	×	×	×	×
		P23	○	○	×	×	×	×	×	×	×	×
		PB3	○	○	○	○	○	×	×	×	×	×
		PA0	×	×	×	×	×	○	○	○	○	×
		PC7	×	×	×	×	×	○	○	○	○	○
		PH0	×	×	×	×	×	○	○	○	○	○
Comparator	COMP0 (output)	P00	○	○	○	○	○	×	×	×	×	×
		P24	○	○	×	×	×	×	×	×	×	×
		PF3	○	×	×	×	×	×	×	×	×	×
		PG2	○	×	×	×	×	×	×	×	×	×
		PE5	×	×	×	×	×	○	○	○	○	×
	COMP1 (output)	P01	○	○	○	○	×	×	×	×	×	×
		P23	○	○	×	×	×	×	×	×	×	×
		PF2	○	×	×	×	×	×	×	×	×	×
		PG1	○	×	×	×	×	×	×	×	×	×
		PB1	×	×	×	×	×	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX66T					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Comparator	COMP2 (output)	P22	○	○	○	○	×	×	×	×	×	×
		PF1	○	×	×	×	×	×	×	×	×	×
		PG0	○	×	×	×	×	×	×	×	×	×
		P17	×	×	×	×	×	○	○	○	○	○
	COMP3 (output)	P30	○	○	○	×	×	○	○	○	○	○
		P80	○	○	×	×	×	×	×	×	×	×
		PC0	○	×	×	×	×	×	×	×	×	×
		PF0	○	×	×	×	×	×	×	×	×	×
		PK2	○	×	×	×	×	×	×	×	×	×
	COMP4 (output)	P20	○	○	○	○	×					
		P81	○	○	×	×	×					
		PC1	○	×	×	×	×					
		PC3	○	×	×	×	×					
		PK1	○	×	×	×	×					
	COMP5 (output)	P21	○	○	○	○	×					
		P82	○	○	×	×	×					
		PC2	○	×	×	×	×					
		PC4	○	×	×	×	×					
		PK0	○	×	×	×	×					
	CVREFC0 (input)	PH3	○	×	×	×	×	×	×	×	×	×
		PE2	×	×	×	×	×	○	○	○	○	○
	CVREFC1 (input)	PH7	○	×	×	×	×	×	×	×	×	×
		PA4	×	×	×	×	×	○	○	○	○	○
	CVREFC2 (input)	P14						○	○	○	○	○
	CVREFC3 (input)	P27						○	○	○	○	○
	CMPC00 (input)	P40	○	○	○	○	○	×	×	×	×	×
		PE1	×	×	×	×	×	○	○	○	○	○
	CMPC01 (input)	P40	○	○	○	○	○					
	CMPC02 (input)	P52	○	○	○	○	×					
	CMPC03 (input)	P60	○	○	×	×	×					
	CMPC10 (input)	P41	○	○	○	○	○	×	×	×	×	×
		PA3	×	×	×	×	×	○	○	○	○	○
	CMPC11 (input)	P41	○	○	○	○	○					
	CMPC12 (input)	P53	○	○	○	○	×					
	CMPC13 (input)	P61	○	○	×	×	×					
	CMPC20 (input)	P42	○	○	○	○	○	×	×	×	×	×
		P15	×	×	×	×	×	○	○	○	○	○
	CMPC21 (input)	P42	○	○	○	○	○					
	CMPC22 (input)	P54	○	○	○	○	×					
	CMPC23 (input)	P63	○	○	×	×	×					
	CMPC30 (input)	P44	○	○	○	○	○	×	×	×	×	×
		P26	×	×	×	×	×	○	○	○	○	○
	CMPC31 (input)	P44	○	○	○	○	○					
	CMPC32 (input)	P55	○	○	○	×	×					
	CMPC33 (input)	P64	○	○	○	○	○					
	CMPC40 (input)	P45	○	○	○	○	×					
	CMPC41 (input)	P45	○	○	○	○	×					
	CMPC42 (input)	P50	○	○	×	×	×					
	CMPC43 (input)	P62	○	○	○	×	○					

Module/ Function	Pin Function	Port Allocation	RX66T					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Comparator	CMPC50 (input)	P46	○	○	○	○	×					
	CMPC51 (input)	P46	○	○	○	○	×					
	CMPC52 (input)	P51	○	○	×	×	×					
	CMPC53 (input)	P65	○	○	○	○	○					
Compare match timer W	TOC0 (output)	PC7						○	○	○	○	○
	TIC0 (input)	PC6						○	○	○	○	○
	TOC1 (output)	PE7						○	○	×	×	×
		PH2						○	○	○	○	○
	TIC1 (input)	PE6						○	○	×	×	×
		PH1						○	○	○	○	○
	TOC2 (output)	PB5						○	○	○	○	○
		PD3						○	○	×	×	×
	TIC2 (input)	PB3						○	○	○	○	○
		PD2						○	○	○	×	×
	TOC3 (output)	PE3						○	○	○	○	○
	TIC3 (input)	PE2						○	○	○	○	○
Realtime clock	RTCOUT (output)	P16						○	○	○	○	×
		P32						○	○	○	○	×
	RTCIC0 (input) (Note 2, Note 3)	P30						○	○	○	○	×
	RTCIC1 (input) (Note 2, Note 3)	P31						○	○	○	○	×
	RTCIC2 (input) (Note 2, Note 3)	P32						○	○	○	○	×
Remote control signal receiver	PMC0 (input)	P51						○	○	×	×	×
		P53						○	○	×	×	×
		PB3						○	○	○	○	○
		PC3						○	○	○	○	×
		PC4						○	○	○	○	○
		PC5						○	○	○	○	○

Note 1. Not present on products provided with a JTAG.
Note 2. Not available on products without a sub-clock oscillator.
Note 3. To use this pin function, set the corresponding pin to general input (clear the PORTm.PDR.Bn and PORTm.PMR.Bn bits to 0).

Table 2.32 Comparison of P0n Pin Function Control Registers (P0nPFS)

Register	Bit	RX66T (n = 0 or 1)	RX660 (n = 0 to 3, 5, or 7)
P00PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC9A 000011b: MTIOC9A# 000111b: CACREF 001001b: ADST1 001010b: RXD9/SMISO9/SSCL9 001100b: RXD12/SMISO12/SSCL12/ RXDX12 011110b: COMP0	Pin function select bits 000000b: Hi-Z 000101b: TMRI0 001010b: TXD6/SMOSI6/SSDA6
P01PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC9C 000011b: MTIOC9C# 000111b: POE12# 001001b: ADST2 001010b: TXD9/SMOSI9/SSDA9 001100b: TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD 011110b: COMP1	Pin function select bits 000000b: Hi-Z 000101b: TMCI0 001010b: RXD6/SMISO6/SSCL6
P02PFS	PSEL[5:0]	—	P02 pin function select bits
P07PFS	PSEL[5:0]	—	P07 pin function select bits
P0nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P00: IRQ2 (48/64/80/100/112/144-pin) P01: IRQ4 (64/80/100/112/144-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P00: IRQ8 (144-pin) P01: IRQ9 (144-pin) P02: IRQ10 (144-pin) P03: IRQ11 (144/100(Note 1)/80/64-pin) P05: IRQ13 (144/100/80-pin) P07: IRQ15 (144/100/80/64-pin)
	ASEL	—	Analog function select bit

Note 1. Not present on products provided with a JTAG.

Table 2.33 Comparison of P1n Pin Function Control Registers (P1nPFS)

Register	Bit	RX66T (n = 0 to 7)	RX660 (n = 2 to 7)
P10PFS	PSEL[5:0]	P10 pin function select bits	—
P11PFS	PSEL[5:0]	P11 pin function select bits	—
P12PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000011b: MTIOC3B# 010100b: GTIOC0A 010101b: GTIOC7A 010110b: GTIOC0A# 010111b: GTIOC7A#	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000101b: TMCI1 001010b: RXD2(Note 2)/SMISO2(Note 2)/ SSCL2(Note 2) 001111b: SCL0
P13PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000011b: MTIOC4A# 010100b: GTIOC1A 010101b: GTIOC8A 010110b: GTIOC1A# 010111b: GTIOC8A#	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000101b: TMO3 001010b: TXD2/SMOSI2/SSDA2 001111b: SDA0
P14PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000011b: MTIOC4B# 010100b: GTIOC2A 010101b: GTIOC9A 010110b: GTIOC2A# 010111b: GTIOC9A#	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKA 000101b: TMRI2 001011b: CTS1#/RTS1#/SS1# 010000b: CTX0

Register	Bit	RX66T (n = 0 to 7)	RX660 (n = 2 to 7)
P15PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000011b: MTIOC3D# 010100b: GTIOC0B 010101b: GTIOC7B 010110b: GTIOC0B# 010111b: GTIOC7B#	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKB 000101b: TMCI2 001010b: RXD1/SMISO1/SSCL1 001011b: SCK3 010000b: CRX0
P16PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000011b: MTIOC4C# 010100b: GTIOC1B 010101b: GTIOC8B 010110b: GTIOC1B# 010111b: GTIOC8B#	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTIOC3D 000101b: TMO2 000111b: RTCOUT(Note 1) 001000b: ADTRG0# 001010b: TXD1/SMOSI1/SSDA1 001011b: RXD3/SMISO3/SSCL3 001101b: MOSIA 001111b: SCL2
P17PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000011b: MTIOC4D# 010100b: GTIOC2B 010101b: GTIOC9B 010110b: GTIOC2B# 010111b: GTIOC9B#	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTIOC3B 000101b: TMO1 000111b: POE8# 001000b: MTIOC4B 001010b: SCK1 001011b: TXD3/SMOSI3/SSDA3 001101b: MISOA 001111b: SDA2 011110b: COMP2

Register	Bit	RX66T (n = 0 to 7)	RX660 (n = 2 to 7)
P1nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P10: IRQ0-DS (48/80/100/112/144-pin) P11: IRQ1-DS (48/64/80/100/112/144-pin) P12: IRQ9 (112/144-pin) P13: IRQ10 (112/144-pin) P14: IRQ11 (112/144-pin) P15: IRQ12 (112/144-pin) P16: IRQ13 (112/144-pin) P17: IRQ14 (112/144-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P12: IRQ2 (144/100/80-pin) P13: IRQ3 (144/100/80-pin) P14: IRQ4 (144/100/80/64/48-pin) P15: IRQ5 (144/100/80/64/48-pin) P16: IRQ6 (144/100/80/64/48-pin) P17: IRQ7 (144/100/80/64/48-pin)
	ASEL	—	Analog function select bit

Note 1. Not available on products without a sub-clock oscillator.
Note 2. Not supported on 80-pin products.

Table 2.34 Comparison of P2n Pin Function Control Registers (P2nPFS)

Register	Bit	RX66T (n = 0 to 7)	RX660 (n = 0 to 7)
P20PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC9C 000010b: MTCLKB 000011b: MTIOC9C# 000100b: MTCLKB# 000101b: TMRI4 001001b: ADTRG0# 001010b: CTS8#/RTS8#/SS8# 001011b: SCK8 001101b: RSPCKA 011110b: COMP4	Pin function select bits 000000b: Hi-Z 000001b: MTIOC1A 000101b: TMRI0 001010b: TXD0/SMOSI0/SSDA0
P21PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC9A 000010b: MTCLKA 000011b: MTIOC9A# 000100b: MTCLKA# 000101b: TMCI4 001001b: ADTRG1# 001010b: TXD8/SMOSI8/SSDA8 001100b: TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12 001101b: MOSIA 011110b: COMP5	Pin function select bits 000000b: Hi-Z 000001b: MTIOC1B 000101b: TMCI0 001000b: MTIOC4A 001010b: RXD0/SMISO0/SSCL0

Register	Bit	RX66T (n = 0 to 7)	RX660 (n = 0 to 7)
P22PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5W 000010b: MTCLKD 000011b: MTIC5W# 000100b: MTCLKD# 000101b: TMRI2 000110b: TMO4 001000b: MTIOC9B 001001b: ADTRG2# 001010b: RXD8/SMISO8/SSCL8 001100b: RXD12/SMISO12/ SSCL12/RXDX12 001101b: MISOA 010000b: CRX0 011110b: COMP2	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKC 000101b: TMO0 001010b: SCK0
P23PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000011b: MTIC5V# 000101b: TMO2 000111b: CACREF 001010b: TXD8/SMOSI8/SSDA8 001100b: TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12 001101b: MOSIA 010000b: CTX0 011110b: COMP1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKD 001010b: TXD3/SMOSI3/SSDA3 001011b: CTS0#/RTS0#/SS0#
P24PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000011b: MTIC5U# 000101b: TMCI2 000110b: TMO6 001010b: CTS8#/RTS8#/SS8# 001011b: SCK8 001101b: RSPCKA 011110b: COMP0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000010b: MTCLKA 000101b: TMRI1 001010b: SCK3
P25PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC9C 000011b: MTIOC9C# 001001b: ADST1 001010b: SCK1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000010b: MTCLKB 001001b: ADTRG0# 001010b: RXD3/SMISO3/SSCL3

Register	Bit	RX66T (n = 0 to 7)	RX660 (n = 0 to 7)
P26PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC9A 000011b: MTIOC9A# 001001b: ADST0 001010b: CTS1#/RTS1#/SS1#	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2A 000101b: TMO1 001010b: TXD1/SMOSI1/SSDA1 001011b: CTS3#/RTS3#/SS3#
P27PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC1A 000010b: MTIOC0C 000011b: MTIOC1A# 000100b: MTIOC0C# 000111b: POE9#	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2B 000101b: TMCI3 001010b: SCK1
P2nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P20: IRQ7-DS (64/80/100/112/144-pin) P21: IRQ6-DS (64/80/100/112/144-pin) P22: IRQ10 (64/80/100/112/144-pin) P23: IRQ11 (100/112/144-pin) P24: IRQ4 (100/112/144-pin) P25: IRQ10 (144-pin) P26: IRQ11 (144-pin) P27: IRQ15 (80/100(Note 1)/112/144-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P20: IRQ8 (144/100/80-pin) P21: IRQ9 (144/100/80-pin) P22: IRQ15 (144/100-pin) P23: IRQ3 (144/100-pin) P24: IRQ12 (144/100-pin) P25: IRQ5 (144/100-pin) P26: IRQ6 (144/100/80/64/48-pin) P27: RQ7 (144/100/80/64/48-pin)
	ASEL	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin P20: AN216 (64/80/100/112/144-pin) P21: AN217 (64/80/100/112/144-pin)	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin P26: CMPC30 (144/100/80/64/48-pin) P27: CVREFC3 (144/100/80/64/48-pin)

Note 1. Supported only on products provided with PGA pseudo-differential input

Table 2.35 Comparison of P3n Pin Function Control Registers (P3nPFS)

Register	Bit	RX66T (n = 0 to 5)	RX660 (n = 0 to 4, 6, or 7)
P30PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKD 000011b: MTIOC0B# 000100b: MTCLKD# 000101b: TMCI6 001010b: SCK8 001011b: CTS8#/RTS8#/SS8# 001101b: SSLA0 011110b: COMP3	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000101b: TMRI3 000111b: POE8# 001010b: RXD1/SMISO1/SSCL1 011110b: COMP3
P31PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0A 000010b: MTCLKC 000011b: MTIOC0A# 000100b: MTCLKC# 000101b: TMRI6 001101b: SSLA1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000101b: TMCI2 001011b: CTS1#/RTS1#/SS1#
P32PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTCLKB 000011b: MTIOC3C# 000100b: MTCLKB# 000101b: TMO6 001101b: SSLA2 010100b: GTIOC3A 010110b: GTIOC3A#	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0C 000101b: TMO3 000111b: RTCOUT(Note 1) 001000b: POE0# 001010b: TXD6/SMOSI6/SSDA6 001011b: TXD0/SMOSI0/SSDA0 010000b: CTX0 100001b: POE10#

Register	Bit	RX66T (n = 0 to 5)	RX660 (n = 0 to 4, 6, or 7)
P33PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKA 000011b: MTIOC3A# 000100b: MTCLKA# 000101b: TMO0 001101b: SSLA3 010100b: GTIOC3B 010110b: GTIOC3B#	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0D 000101b: TMRI3 001000b: POE4# 001010b: RXD6/SMISO6/SSCL6 001011b: RXD0/SMISO0/SSCL0 010000b: CRX0 100001b: POE11#
P34PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2B 000010b: MTIOC9B 000011b: MTIOC2B# 000100b: MTIOC9B# 000101b: TMO4 001010b: CTS9#/RTS9#/SS9# 001011b: RXD1/SMISO1/SSCL1 010001b: USB0_OVRCURB 010100b: GTADSM1 010101b: GTETRGB	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0A 000101b: TMCI3 000111b: POE10# 001010b: SCK6 001011b: SCK0
P35PFS	PSEL[5:0]	P35 pin function select bits	—
P3nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ7 (80/100/112/144-pin) P31: IRQ6 (80/100/112/144-pin) P32: IRQ12-DS (100/112/144-pin) P33: IRQ13-DS (100/112/144-pin) P34: IRQ3 (144-pin) P35: IRQ6 (144-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0-DS (144/100/80/64/48-pin) P31: IRQ1-DS (144/100/80/64/48-pin) P32: IRQ2-DS (144/100/80/64-pin) P33: IRQ3-DS (144/100-pin) P34: IRQ4 (144/100/80-pin) P36: IRQ5 (144/100/80/64/48-pin) P37: IRQ4 (144/100/80/64/48-pin)

Note 1. Not available on products without a sub-clock oscillator.

Table 2.36 Comparison of P4n Pin Function Control Registers (P4nPFS)

Register	Bit	RX66T (n = 0 to 7)	RX660 (n = 0 to 7)
P4nPFS	ISEL	—	Interrupt input function select bit
	ASEL	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin P40: AN000, CMPC00, CMPC01 (48/64/80/100/112/144-pin) P41: AN001, CMPC10, CMPC11 (48/64/80/100/112/144-pin) P42: AN002, CMPC20, CMPC21 (48/64/80/100/112/144-pin) P43: AN003 (48/80/100/112/144-pin) P44: AN100, CMPC30, CMPC31 (48/64/80/100/112/144-pin) P45: AN101, CMPC40, CMPC41 (64/80/100/112/144-pin) P46: AN102, CMPC50, CMPC51 (64/80/100/112/144-pin) P47: AN103 (80/100/112/144-pin)	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin P40: AN000 (144/100/80/64/48-pin) P41: AN001 (144/100/80/64/48-pin) P42: AN002 (144/100/80/64/48-pin) P43: AN003 (144/100/80/64-pin) P44: AN004 (144/100/80/64-pin) P45: AN005 (144/100/80/64/48-pin) P46: AN006 (144/100/80/64/48-pin) P47: AN007 (144/100/80/64/48-pin)

Table 2.37 Comparison of P5n Pin Function Control Registers (P5nPFS)

Register	Bit	RX66T (n = 1, 2, 4, or 5)	RX660 (n = 0 to 6)
P5nPFS	PSEL[5:0]	—	P5n pin function control register
	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P52: IRQ0 (64/80/100/112/144-pin) P53: IRQ1 (64/80/100/112/144-pin) P54: IRQ2 (64/80/100/112/144-pin) P55: IRQ3 (80/100/112/144-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P50: IRQ0 (144/100-pin) P51: IRQ1 (144/100-pin) P52: IRQ2 (144/100-pin) P53: IRQ3 (144/100-pin) P54: IRQ4 (144/100/80/64-pin) P55: IRQ10 (144/100/80/64-pin) P56: IRQ6 (144-pin)
	ASEL	Analog function select bit	—

Table 2.38 Comparison of P6n Pin Function Control Registers (P6nPFS)

Register	Bit	RX66T (n = 0 to 5)	RX660 (n = 0 to 7)
P6nPFS	PSEL[5:0]	—	P6n pin function control register
	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P60: IRQ4 (100/112/144-pin) P61: IRQ5 (100/112/144-pin) P62: IRQ6 (48/80/100/112/144-pin) P63: IRQ7 (100/112/144-pin) P64: IRQ8 (48/64/80/100/112/144-pin) P65: IRQ9 (48/64/80/100/112/144-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P60: IRQ0 (144-pin) P61: IRQ1 (144-pin) P62: IRQ2 (144-pin) P63: IRQ3 (144-pin) P64: IRQ4 (144-pin) P65: IRQ13 (144-pin) P66: IRQ14 (144-pin) P67: IRQ15 (144-pin)
	ASEL	Analog function select bit	—

Table 2.39 Comparison of P7n Pin Function Control Registers (P7nPFS)

Register	Bit	RX66T (n = 0 to 6)	RX660 (n = 0 to 7)
P70PFS	PSEL[5:0]	Pin function control register 000000b: Hi-Z 000111b: POE0# 001010b: CTS9#/RTS9#/SS9# 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD	Pin function control register 000000b: Hi-Z 001010b: SCK4
P71PFS	PSEL[5:0]	P71 pin function control register	—
P72PFS	PSEL[5:0]	P72 pin function control register	—
P73PFS	PSEL[5:0]	P73 pin function control register	—
P74PFS	PSEL[5:0]	Pin function control register 000000b: Hi-Z 000001b: MTIOC3D 000011b: MTIOC3D# 010100b: GTIOC0B 010101b: GTIOC4B 010110b: GTIOC0B# 010111b: GTIOC4B#	Pin function control register 000000b: Hi-Z 001011b: CTS11#/SS11# 101101b: CTS011#/SS011#

Register	Bit	RX66T (n = 0 to 6)	RX660 (n = 0 to 7)
P75PFS	PSEL[5:0]	Pin function control register 000000b: Hi-Z 000001b: MTIOC4C 000011b: MTIOC4C# 010100b: GTIOC1B 010101b: GTIOC5B 010110b: GTIOC1B# 010111b: GTIOC5B#	Pin function control register 000000b: Hi-Z 001010b: SCK11 001011b: RTS11# 101100b: SCK011 101101b: RTS011# 101110b: DE011
P76PFS	PSEL[5:0]	Pin function control register 000000b: Hi-Z 000001b: MTIOC4D 000011b: MTIOC4D# 010100b: GTIOC2B 010101b: GTIOC6B 010110b: GTIOC2B# 010111b: GTIOC6B#	Pin function control register 000000b: Hi-Z 001010b: RXD11/SMISO11/SSCL11 001011b: RXD011/SMISO011/ SSCL011 101100b: TXD011/SMOSI011/ SSDA011
P77PFS	PSEL[5:0]	—	P77 pin function control register
P7nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P70: IRQ5-DS (64/80/100/112/144-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P70: IRQ0 (144-pin) P71: IRQ1 (144-pin) P72: IRQ10 (144-pin) P73: IRQ8 (144-pin) P74: IRQ12 (144-pin) P75: IRQ13 (144-pin) P76: IRQ14 (144-pin) P77: IRQ7 (144-pin)

Table 2.40 Comparison of P8n Pin Function Control Registers (P8nPFS)

Register	Bit	RX66T (n = 0 to 2)	RX660 (n = 0 to 3, 6, or 7)
P80PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5W 000011b: MTIC5W# 000101b: TMRI4 001010b: RXD6/SMISO6/SSCL6 001100b: RXD12/SMISO12/ SSCL12/RXDX12 011110b: COMP3	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 001010b: SCK10 001011b: RTS10# 101100b: SCK010 101101b: RTS010# 101110b: DE010
P81PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000011b: MTIC5V# 000101b: TMCI4 001010b: TXD6/SMOSI6/SSDA6 001100b: TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12 011110b: COMP4	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 001010b: RXD10/SMISO10/SSCL10 101100b: RXD010/SMISO010/ SSCL010
P82PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000011b: MTIC5U# 000101b: TMO4 001010b: SCK6 001100b: SCK12 011110b: COMP5	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 001010b: TXD10/SMOSI10/SSDA10 101100b: TXD010/SMOSI010/ SSDA010
P83PFS	PSEL[5:0]	—	P83 pin function select bits
P86PFS	PSEL[5:0]	—	P86 pin function select bits
P87PFS	PSEL[5:0]	—	P87 pin function select bits
P8nPFS	—	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P80: IRQ5 (100/112/144-pin) P82: IRQ3 (100/112/144-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P80: IRQ8 (144-pin) P81: IRQ9 (144-pin) P82: IRQ2 (144-pin) P83: IRQ3 (144-pin) P86: IRQ14 (144-pin) P87: IRQ15 (144-pin)

Table 2.41 Comparison of P9n Pin Function Control Registers (P9nPFS)

Register	Bit	RX66T (n = 0 to 6)	RX660 (n = 0 to 3)
P90PFS	PSEL[5:0]	Pin function control register 000000b: Hi-Z 000001b: MTIOC7D 000011b: MTIOC7D# 010100b: GTIOC6B 010101b: GTIOC9B 010110b: GTIOC6B# 010111b: GTIOC9B#	Pin function control register 000000b: Hi-Z 001010b: TXD7/SMOSI7/SSDA7
P91PFS	PSEL[5:0]	Pin function control register 000000b: Hi-Z 000001b: MTIOC7C 000011b: MTIOC7C# 010100b: GTIOC5B 010101b: GTIOC8B 010110b: GTIOC5B# 010111b: GTIOC8B#	Pin function control register 000000b: Hi-Z 001010b: SCK7
P92PFS	PSEL[5:0]	Pin function control register 000000b: Hi-Z 000001b: MTIOC6D 000011b: MTIOC6D# 010100b: GTIOC4B 010101b: GTIOC7B 010110b: GTIOC4B# 010111b: GTIOC7B#	Pin function control register 000000b: Hi-Z 001000b: POE4# 001010b: RXD7/SMISO7/SSCL7
P93PFS	PSEL[5:0]	Pin function control register 000000b: Hi-Z 000001b: MTIOC7B 000011b: MTIOC7B# 010100b: GTIOC6A 010101b: GTIOC9A 010110b: GTIOC6A# 010111b: GTIOC9A#	Pin function control register 000000b: Hi-Z 001000b: POE0# 001011b: CTS7#/RTS7#/SS7#
P94PFS	PSEL[5:0]	P94 pin function control register	—
P95PFS	PSEL[5:0]	P95 pin function control register	—
P96PFS	PSEL[5:0]	P96 pin function control register	—

Register	Bit	RX66T (n = 0 to 6)	RX660 (n = 0 to 3)
P9nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P96: IRQ4-DS (64/80/100/112/144-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P90: IRQ0 (144-pin) P91: IRQ9 (144-pin) P92: IRQ10 (144-pin) P93: IRQ11 (144-pin)

Table 2.42 Comparison of PAn Pin Function Control Registers (PAnPFS)

Register	Bit	RX66T (n = 0 to 7)	RX660 (n = 0 to 7)
PA0PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC6C 000011b: MTIOC6C# 000101b: TMO2 001010b: SCK9 001011b: TXD11/SMOSI11/SSDA11 001101b: SSLA3 010000b: CTX0 010001b: USB0_EXICEN 010010b: USB0_VBUSEN	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000111b: CACREF 001000b: MTIOC6D 001101b: SSLA1
PA1PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC6A 000011b: MTIOC6A# 000101b: TMO4 001001b: ADTRG0# 001010b: TXD9/SMOSI9/SSDA9 001011b: RXD11/SMISO11/SSCL11 001101b: SSLA2 010000b: CRX0 010001b: USB0_ID 010010b: USB0_OVRCURA	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKC 001000b: MTIOC7B 001001b: ADTRG0# 001010b: SCK5 001100b: SCK12 001101b: SSLA2 100111b: MTIOC3B

Register	Bit	RX66T (n = 0 to 7)	RX660 (n = 0 to 7)
PA2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2B 000011b: MTIOC2B# 000101b: TMO7 001010b: CTS6#/RTS6#/SS6# 001011b: RXD9/SMISO9/SSCL9 001100b: SCK11 001101b: SSLA1 010100b: GTADSM1	Pin function select bits 000000b: Hi-Z 001000b: MTIOC7A 001010b: RXD5/SMISO5/SSCL5 001100b: RXD12/SMISO12/ SSCL12/RXDX12 001101b: SSLA3
PA3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2A 000011b: MTIOC2A# 000101b: TMRI7 001010b: TXD9/SMOSI9/SSDA9 001011b: SCK8 001101b: SSLA0 010100b: GTADSM0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0D 000010b: MTCLKD 001000b: MTIC5V 001010b: RXD5/SMISO5/SSCL5 100111b: MTIOC4D
PA4PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC1B 000011b: MTIOC1B# 000101b: TMCI7 001001b: ADTRG0# 001010b: SCK6 001011b: TXD8/SMOSI8/SSDA8 001101b: RSPCKA	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000010b: MTCLKA 000101b: TMRI0 001000b: MTIOC4C 001001b: ADST0 001010b: TXD5/SMOSI5/SSDA5 001100b: TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12 001101b: SSLA0 100111b: MTIOC7C
PA5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC1A 000011b: MTIOC1A# 000101b: TMCI3 001001b: ADTRG1# 001010b: RXD6/SMISO6/SSCL6 001011b: RXD8/SMISO8/SSCL8 001101b: MISOA	Pin function select bits 000000b: Hi-Z 001000b: MTIOC6B 001101b: RSPCKA

Register	Bit	RX66T (n = 0 to 7)	RX660 (n = 0 to 7)
PA6PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTCLKB 000010b: MTCLKD 000011b: MTCLKB# 000100b: MTCLKD# 000101b: TMO6 001001b: ADSM1 001011b: TXD11/SMOSI11/SSDA11 001100b: TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12 010000b: CTX0 010100b: GTADSM1	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000010b: MTCLKB 000101b: TMCI3 000111b: POE10# 001000b: MTIOC3D 001011b: CTS5#/RTS5#/SS5# 001100b: CTS12#/RTS12#/SS12# 001101b: MOSIA 100111b: MTIOC6B
PA7PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTCLKA 000010b: MTCLKC 000011b: MTCLKA# 000100b: MTCLKC# 000101b: TMO2 001001b: ADSM0 001011b: RXD11/SMISO11/SSCL11 001100b: RXD12/SMISO12/ SSCL12/RXDX12 010000b: CRX0 010100b: GTADSM0	Pin function select bits 000000b: Hi-Z 001101b: MISOA
PAnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA1: IRQ14-DS (100/112/144-pin) PA5: IRQ1 (48/80/100/112/144-pin) PA6: IRQ7 (144-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA0: IRQ0 (144/100/80/64-pin) PA1: IRQ11 (144/100/80/64/48-pin) PA2: IRQ10 (144/100/80-pin) PA3: IRQ6-DS (144/100/80/64/48-pin) PA4: IRQ5-DS (144/100/80/64/48-pin) PA5: IRQ5 (144/100/80-pin) PA6: IRQ14 (144/100/80/64/48-pin) PA7: IRQ7 (144/100-pin)
	ASEL	—	Analog function select bit

Table 2.43 Comparison of PBn Pin Function Control Registers (PBnPFS)

Register	Bit	RX66T (n = 0 to 7)	RX660 (n = 0 to 7)
PB0PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0D 000011b: MTIOC0D# 000101b: TMO0 001001b: ADTRG2# 001010b: TXD6/SMOSI6/SSDA6 001011b: CTS11#/RTS11#/SS11# 001101b: MOSIA	Pin function select bits 000000b: Hi-Z 000001b: MTIC5W 000010b: MTIOC3D 001010b: RXD4/SMISO4/SSCL4 001011b: RXD6/SMISO6/SSCL6 001101b: RSPCKA
PB1PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0C 000011b: MTIOC0C# 000101b: TMCI0 001001b: ADSM1 001010b: RXD6/SMISO6/SSCL6 001111b: SCL0 010100b: GTADSM1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0C 000010b: MTIOC4C 000101b: TMCI0 001010b: TXD4/SMOSI4/SSDA4 001011b: TXD6/SMOSI6/SSDA6 011110b: COMP1
PB2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000011b: MTIOC0B# 000101b: TMRI0 001001b: ADSM0 001010b: TXD6/SMOSI6/SSDA6 001111b: SDA0 010100b: GTADSM0	Pin function select bits 000000b: Hi-Z 001010b: CTS4#/RTS4#/SS4# 001011b: CTS6#/RTS6#/SS6#
PB3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0A 000011b: MTIOC0A# 000111b: CACREF 001010b: SCK6 001101b: RSPCKA	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0A 000010b: MTIOC4A 000101b: TMO0 000111b: POE11# 001010b: SCK4 001011b: SCK6 011101b: TIC2 100110b: PMC0

Register	Bit	RX66T (n = 0 to 7)	RX660 (n = 0 to 7)
PB4PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000111b: POE8# 001010b: CTS5#/RTS5#/SS5# 001011b: SCK11 001100b: CTS11#/RTS11#/SS11# 010001b: USB0_OVRCURB 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD	Pin function select bits 000000b: Hi-Z 001011b: CTS9#/RTS9#/SS9# 100100b: CTS11#/RTS11#/SS11# 101100b: CTS011#/RTS011#/SS011# 101110b: DE011
PB5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001010b: TXD5/SMOSI5/SSDA5 001011b: TXD11/SMOSI11/SSDA11 001100b: TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12 010000b: CTX0 010001b: USB0_VBUSEN 010100b: GTIOC2B 010110b: GTIOC2B#	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2A 000010b: MTIOC1B 000101b: TMRI1 000111b: POE4# 001010b: SCK9 011101b: TOC2 100100b: SCK11 101100b: SCK011
PB6PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001010b: RXD5/SMISO5/SSCL5 001011b: RXD11/SMISO11/SSCL11 001100b: RXD12/SMISO12/ SSCL12/RXDX12 010000b: CRX0 010001b: USB0_OVRCURA 010100b: GTIOC2A 010110b: GTIOC2A#	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 001010b: RXD9/SMISO9/SSCL9 100100b: RXD11/SMISO11/SSCL11 101100b: RXD011/SMISO011/ SSCL011

Register	Bit	RX66T (n = 0 to 7)	RX660 (n = 0 to 7)
PB7PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001010b: SCK5 001011b: SCK11 001100b: SCK12 010000b: CRX0 010001b: USB0_OVRCURB 010100b: GTIOC1B 010110b: GTIOC1B#	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 001010b: TXD9/SMOSI9/SSDA9 100100b: TXD11/SMOSI11/SSDA11 101100b: TXD011/SMOSI011/ SSDA011
PBnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB0: IRQ8 (48/64/80/100/112/144-pin) PB1: IRQ4 (48/64/80/100/112/144-pin) PB3: IRQ9 (48/64/80/100/112/144-pin) PB4: IRQ3-DS (48/64/80/100/112/144-pin) PB6: IRQ2 (48/64/80/100/112/144-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB0: IRQ12 (144/100/80/64/48-pin) PB1: IRQ4-DS (144/100/80/64/48-pin) PB2: IRQ2 (144/100/80-pin) PB3: IRQ3 (144/100/80/64/48-pin) PB4: IRQ4 (144/100/80-pin) PB5: IRQ13 (144/100/80/64/48-pin) PB6: IRQ6 (144/100/80/64-pin) PB7: IRQ15 (144/100/80/64-pin)

Table 2.44 Comparison of PCn Pin Function Control Registers (PCnPFS)

Register	Bit	RX66T (n = 0 to 6)	RX660 (n = 0 to 7)
PC0PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000011b: MTIOC0B# 001010b: RXD8/SMISO8/SSCL8 010001b: USB0_VBUS 011110b: COMP3	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 001011b: CTS5#/RTS5#/SS5# 001101b: SSLA1 101100b: RXD011/SMISO011/ SSCL011

Register	Bit	RX66T (n = 0 to 6)	RX660 (n = 0 to 7)
PC1PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0C 000011b: MTIOC0C# 001001b: ADSM1 001010b: TXD8/SMOSI8/SSDA8 010001b: USB0_EXICEN 010010b: USB0_VBUSEN 010100b: GTADSM1 011110b: COMP4	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 001010b: SCK5 001101b: SSLA2 101100b: TXD011/SMOSI011/ SSDA011/TXDA011
PC2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0D 000011b: MTIOC0D# 001001b: ADSM0 001010b: SCK8 010001b: USB0_ID 010010b: USB0_OVRCURA 010100b: GTADSM0 011110b: COMP5	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 001010b: RXD5/SMISO5/SSCL5 001101b: SSLA3 101100b: TXDB011
PC3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC9D 000011b: MTIOC9D# 001010b: RXD1/SMISO1/SSCL1 001100b: RXD12/SMISO12/ SSCL12/RXDX12 011110b: COMP4	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 001010b: TXD5/SMOSI5/SSDA5 100110b: PMC0

Register	Bit	RX66T (n = 0 to 6)	RX660 (n = 0 to 7)
PC4PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC9B 000011b: MTIOC9B# 001001b: ADST2 001010b: TXD1/SMOSI1/SSDA1 001100b: TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12 011110b: COMP5	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKC 000101b: TMCI1 000111b: POE0# 001000b: MTIOC0A 001010b: SCK5 001011b: CTS8#/RTS8#/SS8# 001101b: SSLA0 100100b: CTS10#/RTS10#/SS10# 100110b: PMC0 101100b: CTS010#/RTS010#/SS010# 101110b: DE010
PC5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC1B 000010b: MTIOC9D 000011b: MTIOC1B# 000100b: MTIOC9D# 001011b: TXD11/SMOSI11/SSDA11 010000b: CTX0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKD 000101b: TMRI2 001000b: MTIOC0C 001010b: SCK8 001101b: RSPCKA 100100b: SCK10 100110b: PMC0 101100b: SCK010
PC6PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC1A 000010b: MTIOC9C 000011b: MTIOC1A# 000100b: MTIOC9C# 001011b: RXD11/SMISO11/SSCL11 010000b: CRX0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTCLKA 000101b: TMCI2 001010b: RXD8/SMISO8/SSCL8 001101b: MOSIA 011101b: TIC0 100100b: RXD10/SMISO10/SSCL10 101100b: RXD010/SMISO010/ SSCL010

Register	Bit	RX66T (n = 0 to 6)	RX660 (n = 0 to 7)
PC7PFS	PSEL[5:0]	—	PC7 pin function select bits
PCnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PC0: IRQ12 (112/144-pin) PC1: IRQ13 (112/144-pin) PC2: IRQ15 (112/144-pin) PC3: IRQ14 (144-pin) PC5: IRQ10-DS (144-pin) PC6: IRQ11-DS (144-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PC0: IRQ14 (144/100-pin) PC1: IRQ12 (144/100-pin) PC2: IRQ10 (144/100/80/64-pin) PC3: IRQ11 (144/100/80/64-pin) PC4: IRQ12 (144/100/80/64/48-pin) PC5: IRQ5 (144/100/80/64/48-pin) PC6: IRQ13 (144/100/80/64/48-pin) PC7: IRQ14 (144/100/80/64/48-pin)

Table 2.45 Comparison of PDn Pin Function Control Registers (PDnPFS)

Register	Bit	RX66T (n = 0 to 6)	RX660 (n = 0 to 7)
PD0PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000101b: TMO6 001011b: TXD8/SMOSI8/SSDA8 001101b: RSPCKA 010100b: GTIOC3B 010101b: GTIOC1A 010110b: GTIOC3B# 010111b: GTIOC1A#	Pin function select bits 000000b: Hi-Z 001000b: POE4#
PD1PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000101b: TMO2 001011b: RXD8/SMISO8/SSCL8 001101b: MISOA 010100b: GTIOC3A 010101b: GTIOC0B 010110b: GTIOC3A# 010111b: GTIOC0B#	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 001000b: POE0# 010000b: CTX0
PD2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000101b: TMCI1 000110b: TMO4 001010b: SCK5 001011b: SCK8 001101b: MOSIA 010001b: USB0_VBUS 010100b: GTIOC2B 010101b: GTIOC0A 010110b: GTIOC2B# 010111b: GTIOC0A#	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 010000b: CRX0 011101b: TIC2

Register	Bit	RX66T (n = 0 to 6)	RX660 (n = 0 to 7)
PD3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000101b: TMO0 001010b: TXD1/SMOSI1/SSDA1 001011b: TXD11/SMOSI11/SSDA11 010100b: GTIOC2A 010101b: GTETRGC 010110b: GTIOC2A#	Pin function select bits 000000b: Hi-Z 000111b: POE8# 001000b: MTIOC8D 011101b: TOC2
PD4PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000101b: TMCI0 000110b: TMCI6 001010b: SCK1 001011b: SCK11 010100b: GTIOC1B 010101b: GTETRGB 010110b: GTIOC1B#	Pin function select bits 000000b: Hi-Z 000111b: POE11# 001000b: MTIOC8B
PD5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000101b: TMRI0 000110b: TMRI6 001010b: RXD1/SMISO1/SSCL1 001011b: RXD11/SMISO11/SSCL11 010100b: GTIOC1A 010101b: GTETRGA 010110b: GTIOC1A#	Pin function select bits 000000b: Hi-Z 000001b: MTIC5W 000111b: POE10# 001000b: MTIOC8C

Register	Bit	RX66T (n = 0 to 6)	RX660 (n = 0 to 7)
PD6PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC9C 000011b: MTIOC9C# 000101b: TMO1 001001b: ADST0 001010b: CTS1#/RTS1#/SS1# 001011b: CTS11#/RTS11#/SS11# 001101b: SSLA0 010100b: GTIOC0B 010101b: GTIOC3B 010110b: GTIOC0B# 010111b: GTIOC3B#	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000111b: POE4# 001000b: MTIOC8A
PD7PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC9A 000011b: MTIOC9A# 000101b: TMRI1 000110b: TMRI5 001010b: TXD5/SMOSI5/SSDA5 001101b: SSLA1 010000b: CTX0 010100b: GTIOC0A 010101b: GTIOC3A 010110b: GTIOC0A# 010111b: GTIOC3A#	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000111b: POE0#
PDnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PD4: IRQ2 (64/80/100/112/144-pin) PD5: IRQ6 (48/64/80/100/112/144-pin) PD6: IRQ5 (64/80/100/112/144-pin) PD7: IRQ8 (48/64/80/100/112/144-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PD0: IRQ0 (144/100/80-pin) PD1: IRQ1 (144/100/80-pin) PD2: IRQ2 (144/100/80-pin) PD3: IRQ3 (144/100-pin) PD4: IRQ4 (144/100-pin) PD5: IRQ5 (144/100-pin) PD6: IRQ6 (144/100-pin) PD7: IRQ7 (144/100-pin)
	ASEL	—	Analog function select bit

Table 2.46 Comparison of PEn Pin Function Control Registers (PEnPFS)

Register	Bit	RX66T (n = 0 to 6)	RX660 (n = 0 to 7)
PE0PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC9B 000011b: MTIOC9B# 000101b: TMCI1 000110b: TMCI5 001010b: RXD5/SMISO5/SSCL5 001101b: SSLA2 010000b: CRX0 010001b: USB0_OVRCURB	Pin function select bits 000000b: Hi-Z 001000b: MTIOC3D 001100b: SCK12
PE1PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC9D 000011b: MTIOC9D# 000101b: TMO5 001010b: CTS5#/RTS5#/SS5# 001100b: CTS12#/RTS12#/SS12# 001101b: SSLA3	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 001000b: MTIOC3B 001100b: TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12
PE2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000111b: POE10#	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 001000b: MTIOC7A 001100b: RXD12/SMISO12/ SSCL12/RXDX12 011101b: TIC3
PE3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000010b: MTCLKD 000100b: MTCLKD# 000111b: POE11# 001010b: CTS9#/RTS9#/SS9# 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000111b: POE8# 001000b: MTIOC1B 001100b: CTS12#/RTS12#/SS12# 011101b: TOC3

Register	Bit	RX66T (n = 0 to 6)	RX660 (n = 0 to 7)
PE4PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000010b: MTCLKC 000100b: MTCLKC# 000111b: POE10# 001010b: SCK9 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000010b: MTIOC1A 001000b: MTIOC4A 100111b: MTIOC7D
PE5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC9D 000011b: MTIOC9D# 001001b: ADST0 001010b: SCK9 001011b: CTS9#/RTS9#/SS9# 010100b: GTIOC3A 010101b: GTETRGB 010110b: GTIOC3A# 010111b: GTETRGD	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000010b: MTIOC2B 011110b: COMP0
PE6PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000111b: POE10# 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD	Pin function select bits 000000b: Hi-Z 001000b: MTIOC6C 001010b: CTS4#/RTS4#/SS4# 011101b: TIC1
PE7PFS	PSEL[5:0]	—	PE7 pin function select bits

Register	Bit	RX66T (n = 0 to 6)	RX660 (n = 0 to 7)
PEnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE0: IRQ7 (100/112/144-pin) PE1: IRQ15 (100/112/144-pin) PE3: IRQ2-DS (80/100/112/144-pin) PE4: IRQ1 (80/100/112/144-pin) PE5: IRQ0 (100/112/144-pin) PE6: IRQ3 (144-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE0: IRQ8 (144/100/80/64-pin) PE1: IRQ9 (144/100/80/64/48-pin) PE2: IRQ7-DS (144/100/80/64/48-pin) PE3: IRQ11 (144/100/80/64/48-pin) PE4: IRQ12 (144/100/80/64/48-pin) PE5: IRQ5 (100/80/64-pin) PE6: IRQ6 (144/100-pin) PE7: IRQ7 (144/100-pin)
	ASEL	—	Analog function select bit

Table 2.47 Comparison of PF5 Pin Function Control Register (PF5PFS)

Register	Bit	RX66T (n = 0 to 3)	RX660
PF5PFS	PSEL[5:0]	PFn pin function select bits	—
	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PF0: IRQ12 (144-pin) PF1: IRQ13 (144-pin) PF2: IRQ5 (144-pin) PF3: IRQ14 (144-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PF5: IRQ4 (144-pin)

Table 2.48 Comparison of PGn Pin Function Control Register (PGnPFS)

Register	Bit	RX66T (n = 0 to 2)	RX660
PGnPFS	—	PGn pin function control register	—

Table 2.49 Comparison of PHn Pin Function Control Register (PHnPFS)

Register	Bit	RX66T (n = 0 to 7)	RX660 (n 0 to 3)
PH0PFS	PSEL[5:0]	—	PHn pin function select bits
	ISEL	—	Interrupt input function select bit
	ASEL	Analog function select bit	—

Table 2.50 Comparison of PJn Pin Function Control Register (PJnPFS)

Register	Bit	RX66T	RX660 (n = 1, 3, or 5)
PJnPFS	—	—	PJn pin function control register

Table 2.51 Comparison of PKn Pin Function Control Registers (PKnPFS)

Register	Bit	RX66T (n = 0 to 2)	RX660 (n = 2 to 5)
PK0PFS	PSEL[5:0]	PK0 pin function control register	—
PK1PFS	PSEL[5:0]	PK1 pin function control register	—
PK2PFS	PSEL[5:0]	Pin function control register 000000b: Hi-Z 000111b: POE12# 001010b: CTS9#/RTS9#/SS9# 001011b: SCK5 010101b: GTIOC1A 010111b: GTIOC1A# 011110b: COMP3	Pin function control register 000000b: Hi-Z 001010b: TXD9/SMOSI9/SSDA9
PK3PFS	PSEL[5:0]	—	PK3 pin function control register
PK4PFS	PSEL[5:0]	—	PK4 pin function control register
PK5PFS	PSEL[5:0]	—	PK5 pin function control register
PKnPFS	ISEL	Interrupt input function select bit	—

Table 2.52 Comparisons of Multi-Function Pin Controller Registers

Register	Bit	RX66T	RX660
PFCSS0	CS0S (RX66T) CS0S[1:0] (RX660)	CS0# output pin select bits 0: P96 is set as CS0# output pin. 1: PC0 is set as CS0# output pin.	CS0# output pin select bits b1 b0 0 0: P24 is set as CS0# output pin. 0 1: P60 is set as CS0# output pin. 1 x: PC7 is set as CS0# output pin.
	CS1S[1:0]	CS1# output pin select bits b3 b2 0 0: P80 is set as CS1# output pin. 0 1: PK0 is set as CS1# output pin. 1 0: PF1 is set as CS1# output pin. 1 1: PC2 is set as CS1# output pin.	CS1# output pin select bits b3 b2 0 0: P25 is set as CS1# output pin. 0 1: P61 is set as CS1# output pin. 1 0: P71 is set as CS1# output pin. 1 1: PC6 is set as CS1# output pin.
	CS2S[1:0]	CS2# output pin select bits b5 b4 0 0: P81 is set as CS2# output pin. 0 1: P26 is set as CS2# output pin. 1 x: PF2 is set as CS2# output pin.	CS2# output pin select bits b5 b4 0 0: P26 is set as CS2# output pin. 0 1: P62 is set as CS2# output pin. 1 0: P72 is set as CS2# output pin. 1 1: PC5 is set as CS2# output pin.

Register	Bit	RX66T	RX660
PFCSS0	CS3S (RX66T) CS3S[1:0] (RX660)	CS3# output pin select bits 0: PF3 is set as CS3# output pin. 1: P25 is set as CS3# output pin.	CS3# output pin select bits b7 b6 0 0: P27 is set as CS3# output pin. 0 1: P63 is set as CS3# output pin. 1 0: P73 is set as CS3# output pin. 1 1: PC4 is set as CS3# output pin.
PFBCR0	ADRLE	A0 to A7 output enable bit Products with RAM capacity 64 KB: 0: PB0, PA2, PF0, PB4 to PB7, and PD0 to PD2 are configured as I/O ports. 1: PB0, PA2, PF0, PB4 to PB7, and PD0 to PD2 are configured as external address buses A0 to A7. Products with RAM capacity 128 KB: 0: PB0, PA2, PF0, PA3 to PA5, PB0 to PB3, PB4 to PB7, and PD0 to PD2 are configured as I/O ports. 1: PB0, PA2, PF0, PA3 to PA5, PB0 to PB3, PB4 to PB7, and PD0 to PD2 are configured as external address buses A0 to A7.	A0 to A7 output enable bit 0: PA0 to PA7 are configured as I/O ports. 1: PA0 to PA7 are configured as external address buses A0 to A7.
	ADRHMS (RX66T) ADRHMS ADRHMS2 (RX660)	A12 to A20 output select bits Products with RAM capacity 64 KB: 0: P65 to P60, and P55 to P53 are configured as external address buses A12 to A20. 1: Setting prohibited. Products with RAM capacity 128 KB: This bit is used in conjunction with the PFBCR4.ADRHMS bit to select pins of the external address bus.	A12 to A20 output select bits 1 and 2 The ADRHMS and ADRHMS2 bits are configured to select output. 0 0: PC0 to PC4 are set. 0 1: PC0, PC1, P71, P72, and P74 are set. 1 0: P90 to P93 are set. (No allocation of A20) 1 1: Setting prohibited.

Register	Bit	RX66T	RX660
PFBCR0	DHE	D8 to D15 output enable bit 0: Output disabled on external data buses D8 to D15 (set as I/O ports) 1: Output enabled on data buses D8 to D15 D8 to D10: P32 to P30 D11 to D15: Selected in the PFBCR2 register	D8 to D15 output enable bit 0: PE0 to PE7 are configured as I/O ports. 1: PE0 to PE7 are configured as external data buses D8 to D15.
	WR1BC1E	WR1# or BC1 # output enable bit 0: PE0 is set as I/O port. 1: PE0 is set as WR1# or BC1#	WR1# or BC1 # output enable bit 0: P51 is set as I/O port. 1: P51 is set as WR1# or BC1#.
PFBCR1	WAITS[1:0]	WAIT select bit b1 b0 0 0: P82, PE0, and P96 are not configured as WAIT# input pins. 0 1: P82 is set as WAIT# input pin. 1 0: PE0 is set as WAIT# input pin. 1 1: P96 is set as WAIT# input pin.	External bus control register 1 b1 b0 0 0: Setting invalid(Note 1) 0 1: P55 is set as WAIT# input pin. 1 0: PC5 is set as WAIT# input pin. 1 1: P51 is set as WAIT# input pin.
PFBCR2	DHS	D11 to D15 select bit	—
	A0S[1:0]	A0/BC0# select bit	—
	D0S[1:0]	—	D0 select bit
	D1S[1:0]	—	D1 select bit
	D2S[1:0]	—	D2 select bit
	D3S[1:0]	—	D3 select bit
PFBCR3	RDS	RD# select bit	—
	DLHS	—	D4 to D7 select bit
PFBCR4	—	External bus control register 4	—

Note 1. Even if this bit is set to 00b in 144- and 100-pin products, P55 is set as WAIT# input pin.

2.14 Multi- Function Timer Pulse Unit 3

Table 2.53 is Comparative Overview of Multi-Function Timer Pulse Unit 3 , and Table 2.54 is Comparison of Multi-Function Timer Pulse Unit 2 and 3 Registers.

Table 2.53 Comparative Overview of Multi-Function Timer Pulse Unit 3

Item	RX66T (MTU3d)	RX660 (MTU3a)
Pulse input/output	Max. 28 lines	Max. 28 lines
Pulse input	3 lines	3 lines
Count clocks	11 clocks for each channel (14 for MTU0 and MTU9, 12 for MTU2, 10 for MTU5, and 4 for MTU1 and MTU2 (when LWA = 1))	11 clocks for each channel (14 for MTU0, 12 for MTU2, 10 for MTU5, and four each for MTU1 and MTU2 (when LWA = 1))
Available operations	[MTU0 to MTU4, MTU6, MTU7, MTU8, MTU9] • Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Simultaneous register input/output by synchronous counter operation • Up to 14-phase PWM output in combination with synchronous operation	[MTU0 to MTU4, MTU6, MTU7, MTU8] • Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) (excluding MTU8) • Simultaneous writing to multiple timer counters (TCNT) (excluding MTU8) • Simultaneous register input/output by synchronous counter operation (excluding MTU8) • Up to 12-phase PWM output in combination with synchronous operation (excluding MTU8)
	[MTU0, MTU3, MTU4, MTU6, MTU7, MTU8, MTU9] • Ability to specify buffer operation	[MTU0, MTU3, MTU4, MTU6, MTU7, MTU8] • Ability to specify buffer operation
	[MTU1, MTU2] • Independent specification of phase counting mode • Ability to specify 32-bit phase counting mode linked to MTU1 or MTU2 (when TMDR3.LWA = 1) • Cascade connection operation	[MTU1, MTU2] • Independent specification of phase counting mode • Ability to specify 32-bit phase counting mode linked to MTU1 or MTU2 (when TMDR3.LWA = 1) • Cascade connection operation
	[MTU3, MTU4, MTU6, MTU7] • Ability to produce 12-phase waveform output, comprising six phases each of positive and negative output, in complementary PWM or reset PWM mode, through linked operation of MTU3 or MTU4 and MTU6 or MTU7 • In complementary PWM mode, ability to transfer data from the buffer register to a temporary register at peaks or troughs of the timer counter or when writes to the buffer register (MTU4.TGRD or MTU7.TGRD) occur • Ability to specify double buffer function in complementary PWM mode	[MTU3, MTU4, MTU6, MTU7] • Ability to produce 12-phase waveform output, comprising six phases each of positive and negative output, in complementary PWM or reset PWM mode, through linked operation of MTU3 or MTU4 and MTU6 or MTU7 • In complementary PWM mode, ability to transfer data from the buffer register to a temporary register at peaks or troughs of the timer counter or when writes to the buffer register (MTU4.TGRD or MTU7.TGRD) occur • Ability to specify double buffer function in complementary PWM mode

Item	RX66T (MTU3d)	RX660 (MTU3a)
Available operations	[MTU3, MTU4] • Through linked operation with MTU0, ability to specify the AC synchronous motor (brushless DC motor) drive mode using complementary PWM or reset PWM and to select two types (chopping or level) of waveform output	[MTU3, MTU4] • Through linked operation with MTU0, ability to specify the AC synchronous motor (brushless DC motor) drive mode using complementary PWM or reset PWM and to select two types (chopping or level) of waveform output
	[MTU5] • Can be used as a dead time compensation counter.	[MTU5] • Can be used as a dead time compensation counter.
	[MTU6, MTU7] • Through linked operation with MTU9, ability to specify the AC synchronous motor (brushless DC motor) drive mode using complementary PWM or reset PWM and to select two types (chopping or level) of waveform output	—
	—	[MTU0/MTU5, MTU1, MTU2, MTU8] Ability to use the MTU1 and MTU2 in combination and specify 32-bit phase counting mode linked to the MTU0 or MTU5 and MTU8
Interrupt skipping function	Ability to skip interrupts at counter peak or trough and A/D converter conversion start triggers in complementary PWM mode	Ability to skip interrupts at counter peak or trough and A/D converter conversion start triggers in complementary PWM mode
Interrupt sources	45 sources	43 sources
Buffer operation	Automatic transfer of register data (transfer from buffer register to timer register)	Automatic transfer of register data (transfer from buffer register to timer register)
Trigger generation	• Ability to generate A/D converter start trigger • Ability to start A/D conversion at user-specified timing using A/D conversion start request delay function Ability to synchronize operation with PWM output	• Ability to generate A/D converter start trigger • Ability to start A/D conversion at user-specified timing using A/D conversion start request delay function Ability to synchronize operation with PWM output
Low power consumption function	Transition to the module stop state is possible.	Transition to the module stop state is possible.

Table 2.54 Comparison of Multi-Function Timer Pulse Unit 2 and 3 Registers

Register	Bit	RX66T (MTU3d)	RX660 (MTU3a)
TMDR1	BFE	Buffer operation E bit 0: MTU0.TGRE and MTU0.TGRF, and MTU9.TGRE and MTU9.TGRF operate normally. 1: MTU0.TGRE and MTU0.TGRF, and MTU9.TGRE and MTU9.TGRF are used for buffer operation.	Buffer operation E bit 0: MTU0.TGRE and MTU0.TGRF operate normally. 1: MTU0.TGRE and MTU0.TGRF are used for buffer operation.
TBTM	TTSE	Timing select E bit 0: Data is transferred from MTU0.TGRF to MTU0.TGRE or from MTU9.TGRF to MTU9.TGRE when compare match E occurs in MTU0 or MTU9. 1: Data is transferred from MTU0.TGRF to MTU0.TGRE or from MTU9.TGRF to MTU9.TGRE when MTU0.TCNT or MTU9.TCNT is cleared.	Timing select E bit 0: Data is transferred from MTU0.TGRF to MTU0.TGRE when compare match E occurs in MTU0 1: Data is transferred from MTU0.TGRF to MTU0.TGRE when MTU0.TCNT is cleared.
TSTR / TSTRA / TSTRB	CST8	—	Counter start 8 bit
	CST9	Counter start 9 bit	—
TSYRA / TSYRB	SYNC9	Timer synchronization 9 bit	—
TCSYSTR	SCH9	Synchronous start 9 bit	—
TGCRA/TGCRB (RX66T) TGCRA (RX660)	—	Timer gate control register m (m = A or B)	Timer gate control register A
NFCRn	—	Noise filter control register n (n = 0 to 4, 6, 7, 9, or C)	Noise filter control register n (n = 0 to 4, 6, 7, 8, or C)
TADSTRGR0	—	A/D conversion start request select register 0	—
TADSTRGR1	—	A/D conversion start request select register 1	—

2.15 Port Output Enable 3

Table 2.55 is Comparative Overview of Port Output Enable 3, and Table 2.56 is Comparison of Port Output Enable 3 Registers.

Table 2.55 Comparative Overview of Port Output Enable 3

Item	RX66T (POE3B)	RX660 (POE3a)
Pin status while output is disabled	• High-impedance • General I/O port	• High-impedance
Output stop control target pins (RX66T) High-impedance control target pins (RX660)	• MTU output pins — MTU0 pin (MTIOC0A, MTIOC0D, MTIOC0C, MTIOC0D) — MTU3 pin (MTIOC3B, MTIOC3D) — MTU4 pin (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) — MTU6 pin (MTIOC6B, MTIOC6D) — MTU7 pin (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D) — MTU9 pin (MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D) • GPTW output pins — GPTW0 pins (GTIOC0A, GTIOC0B) — GPTW1 pins (GTIOC1A, GTIOC1B) — GPTW2 pins (GTIOC2A, GTIOC2B) — GPTW3 pins (GTIOC3A, GTIOC3B) — GPTW4 pins (GTIOC4A, GTIOC4B) — GPTW5 pins (GTIOC5A, GTIOC5B) — GPTW6 pins (GTIOC6A, GTIOC6B) — GPTW7 pins (GTIOC7A, GTIOC7B) — GPTW8 pins (GTIOC8A, GTIOC8B) — GPTW9 pins (GTIOC9A, GTIOC9B)	— MTU output pins — MTU0 pin (MTIOC0A, MTIOC0D, MTIOC0C, MTIOC0D) — MTU3 pin (MTIOC3B, MTIOC3D) — MTU4 pin (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) — MTU6 pin (MTIOC6B, MTIOC6D) — MTU7 pin (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D)

Item	RX66T (POE3B)	RX660 (POE3a)
Conditions for generating output stop request (RX66T) Conditions for generating high impedance request (RX660)	• Input pin changes When signal input occurs on pin POE0#, POE4#, POE8#, POE9#, POE10#, POE11#, POE12#, POE13#, or POE14#	• Input pin changes When signal input occurs on pin POE0# to POE3# and POE8#.
	• Short circuit of output pins: A match (short circuit) of output signal levels (active level) lasting one or more cycles on one of the combinations of pins listed below [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D — MTIOC6B and MTIOC6D — MTIOC7A and MTIOC7C — MTIOC7B and MTIOC7D	• Short circuit of output pins: A match (short circuit) of output signal levels (active level) lasting one or more cycles on one of the combinations of pins listed below [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D — MTIOC6B and MTIOC6D — MTIOC7A and MTIOC7C — MTIOC7B and MTIOC7D
	[GPTW output pins] — GTIOC0A and GTIOC0B — GTIOC1A and GTIOC1B — GTIOC2A and GTIOC2B — GTIOC4A and GTIOC4B — GTIOC5A and GTIOC5B — GTIOC6A and GTIOC6B — GTIOC7A and GTIOC7B — GTIOC8A and GTIOC8B — GTIOC9A and GTIOC9B • SPOER register settings are specified. • Detection of stopped oscillation on main clock oscillator • Detection of comparator C (CMPC) output	• SPOER register settings are specified. • Detection of stopped oscillation on main clock oscillator
Functions	• Falling-edge detection or low level detection can be set for each of the POE0#, POE4#, POE8#, POE9#, POE10#, POE11#, POE12#, POE13#, and POE14# pins. For low level detection, the sampling clock can be selected from PCLK/1, PCLK/2, PCLK/4, PCLK/8, PCLK/16, and PCLK/128, and the sampling count can be selected from 4 times, 8 times, and 16 times.	• Falling-edge detection or sampling of the low level 16 times at PCLK/8, PCLK/16, or PCLK/128 can be set for each of the POE0#, POE4#, POE8#, POE10#, and POE11# input pins.
	• Output on all control target pins can be stopped on detection of the falling edge of input or low level on the POE0#, POE4#, POE8#, POE9#, POE10#, POE11#, POE12#, POE13#, or POE14# pin.	• Output on all control target pins can be placed in the high-impedance state on detection of falling edges or sampling of the low level on the POE0#, POE4#, POE8#, POE10#, and POE11# pins.

Item	RX66T (POE3B)	RX660 (POE3a)
Functions	• Output on all control target pins can be stopped when oscillation stop is detected in the clock generation circuit. • It is possible to compare levels output on pins for complementary PWM output from the MTU, and when simultaneous output of the active level continues for one or more cycles, output on the pins can be stopped. • It is possible to compare levels output on GPTW output pins (GPTW0 to GPTW2, GPTW4 to GPTW6, and GPTW7 to GPTW9 pins), and when simultaneous output of the active level continues for at least one cycle, output on the pins can be stopped. • Output on all control target pins can be stopped on detection of output of Comparator C (CMPC). • Output on all control target pins can be stopped by modifying settings of POE3 registers. • Interrupts can be generated in response to the results of input level sampling or output-level comparison.	• Output on all control target pins can be placed in the high-impedance state when oscillation by the clock generation circuit stops. • It is possible to compare levels output on pins for complementary PWM output from the MTU, and when simultaneous output of the active level continues for one or more cycles, output on the pins can be placed in the high-impedance state. • Output on all control target pins can be placed in the high-impedance state by modifying settings of POE3 registers. • Interrupts can be generated in response to the results of input level sampling or output-level comparison.

Table 2.56 Comparison of Port Output Enable 3 Registers

Register	Bit	RX66T (POE3B)	RX660 (POE3a)
ICSR1	POE0M[3:0] (RX66T) POE0M[1:0] (RX660)	POE0 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge of POE0# pin input. 0 0 0 1: Samples the level of the POE0# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 0 1 0: Samples the level of the POE0# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 0 1 1: Samples the level of the POE0# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 0 0: Samples the level of the POE0# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 0 1: Samples the level of the POE0# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 1 0: Samples the level of the POE0# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified number of times. Settings other than the above are prohibited.	POE0 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE0# pin input. 0 1: Samples the low level of the POE0# pin input 16 times at PCLK/8 clock pulses, and accepts a request when all are low level. 1 0: Samples the low level of the POE0# pin input 16 times at PCLK/16 clock pulses, and accepts a request when all are low level. 1 1: Samples the low level of the POE0# pin input 16 times at PCLK/128 clock pulses, and accepts a request when all are low level.
	POE0M2[3:0]	POE0 sampling count select bit	—
	POE0F	POE0 flag 0: An output stop request has not been input to the POE0# pin. 1: An output stop request has been input to the POE0# pin.	POE0 flag 0: A high-impedance request has not been input to the POE0# pin. 1: A high-impedance request has been input to the POE0# pin.

Register	Bit	RX66T (POE3B)	RX660 (POE3a)
ICSR2	POE4M[3:0] (RX66T) POE4M[1:0] (RX660)	POE4 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge of POE4# pin input. 0 0 0 1: Samples the level of the POE4# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 0 1 0: Samples the level of the POE4# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 0 1 1: Samples the level of the POE4# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 0 0: Samples the level of the POE4# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 0 1: Samples the level of the POE4# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 1 0: Samples the level of the POE4# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified number of times. Settings other than the above are prohibited.	POE4 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE4# pin input. 0 1: Samples the low level of the POE4# pin input 16 times at PCLK/8 clock pulses, and accepts a request when all are low level. 1 0: Samples the low level of the POE4# pin input 16 times at PCLK/16 clock pulses, and accepts a request when all are low level. 1 1: Samples the low level of the POE4# pin input 16 times at PCLK/128 clock pulses, and accepts a request when all are low level.
	POE4M2[3:0]	POE4 sampling count select bit	—
	POE4F	POE4 flag 0: An output stop request has not been input to the POE4# pin. 1: An output stop request has been input to the POE4# pin.	POE4 flag 0: A high-impedance request has not been input to the POE4# pin. 1: A high-impedance request has been input to the POE4# pin.

Register	Bit	RX66T (POE3B)	RX660 (POE3a)
ICSR3	POE8M[3:0] (RX66T) POE8M[1:0] (RX660)	POE8 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge of POE8# pin input. 0 0 0 1: Samples the level of the POE8# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 0 1 0: Samples the level of the POE8# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 0 1 1: Samples the level of the POE8# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 0 0: Samples the level of the POE8# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 0 1: Samples the level of the POE8# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 1 0: Samples the level of the POE8# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified number of times. Settings other than the above are prohibited.	POE8 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE8# pin input. 0 1: Samples the low level of the POE8# pin input 16 times at PCLK/8 clock pulses, and accepts a request when all are low level. 1 0: Samples the low level of the POE8# pin input 16 times at PCLK/16 clock pulses, and accepts a request when all are low level. 1 1: Samples the low level of the POE8# pin input 16 times at PCLK/128 clock pulses, and accepts a request when all are low level.
	POE8M2[3:0]	POE8 sampling count select bit	—
	POE8F	POE8 flag 0: An output stop request has not been input to the POE8# pin. 1: An output stop request has been input to the POE8# pin.	POE8 flag 0: A high-impedance request has not been input to the POE8# pin. 1: A high-impedance request has been input to the POE8# pin.

Register	Bit	RX66T (POE3B)	RX660 (POE3a)
ICSR4	POE10M[3:0] (RX66T) POE10M[1:0] (RX660)	POE10 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge of POE10# pin input. 0 0 0 1: Samples the level of the POE10# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 0 1 0: Samples the level of the POE10# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 0 1 1: Samples the level of the POE10# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 0 0: Samples the level of the POE10# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 0 1: Samples the level of the POE10# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 1 0: Samples the level of the POE10# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified number of times. Settings other than the above are prohibited.	POE10 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE10# pin input. 0 1: Samples the low level of the POE10# pin input 16 times at PCLK/8 clock pulses, and accepts a request when all are low level. 1 0: Samples the low level of the POE10# pin input 16 times at PCLK/16 clock pulses, and accepts a request when all are low level. 1 1: Samples the low level of the POE10# pin input 16 times at PCLK/128 clock pulses, and accepts a request when all are low level.
	POE10M2[3:0]	POE10 sampling count select bit	—
	POE10F	POE10 flag 0: An output stop request has not been input to the POE10# pin. 1: An output stop request has been input to the POE10# pin.	POE10 flag 0: A high-impedance request has not been input to the POE10# pin. 1: A high-impedance request has been input to the POE10# pin.

Register	Bit	RX66T (POE3B)	RX660 (POE3a)
ICSR5	POE11M[3:0] (RX66T) POE11M[1:0] (RX660)	POE11 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge of POE11# pin input. 0 0 0 1: Samples the level of the POE11# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 0 1 0: Samples the level of the POE11# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 0 1 1: Samples the level of the POE11# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 0 0: Samples the level of the POE11# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 0 1: Samples the level of the POE11# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 1 0: Samples the level of the POE11# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified number of times. Settings other than the above are prohibited.	POE11 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE11# pin input. 0 1: Samples the low level of the POE11# pin input 16 times at PCLK/8 clock pulses, and accepts a request when all are low level. 1 0: Samples the low level of the POE11# pin input 16 times at PCLK/16 clock pulses, and accepts a request when all are low level. 1 1: Samples the low level of the POE11# pin input 16 times at PCLK/128 clock pulses, and accepts a request when all are low level.
	POE11M2[3:0]	POE11 sampling count select bit	—
	POE11F	POE11 flag 0: An output stop request has not been input to the POE11# pin. 1: An output stop request has been input to the POE11# pin.	POE11 flag 0: A high-impedance request has not been input to the POE11# pin. 1: A high-impedance request has been input to the POE11# pin.

Register	Bit	RX66T (POE3B)	RX660 (POE3a)
ICSR6	OSTSTE	Output stop enable bit when oscillation stops 0: Does not stop output on control target pins when an oscillation stop is detected. 1: Stops output on control target pins when an oscillation stop is detected.	Oscillation stop high-impedance enable bit 0: Does not put the output on control target pins in the high-impedance state when an oscillation stop is detected. 1: Puts the output on control target pins in the high-impedance state when an oscillation stop is detected.
	OSTSTF	Oscillation stop detection flag 0: A high-impedance request is not generated due to the oscillation stop. 1: A high-impedance request is generated due to the oscillation stop.	Oscillation stop detection flag 0: A high-impedance request is not generated due to the oscillation stop. 1: A high-impedance request is generated due to the oscillation stop.
ICSR7	—	Output level control/status register 7	—
ICSR8	—	Output level control/status register 8	—
ICSR9	—	Output level control/status register 9	—
ICSR10	—	Output level control/status register 10	—
OCSR1	OCE1	Simultaneous conduction stop enable bit 1 0: Does not stop outputs when they simultaneously go to an active level. 1: Stops outputs when they simultaneously go to an active level.	Simultaneous conduction high-impedance enable 1 bit 0: Does not put the outputs in the high-impedance state when they simultaneously go to an active level. 1: Puts the outputs in the high-impedance state when they simultaneously go to an active level.
OCSR2	OCE2	Simultaneous conduction stop enable bit 2 0: Does not stop outputs when they simultaneously go to an active level. 1: Stops outputs when they simultaneously go to an active level.	Simultaneous conduction high-impedance enable 2 bit 0: Does not put the outputs in the high-impedance state when they simultaneously go to an active level. 1: Puts the outputs in the high-impedance state when they simultaneously go to an active level.
OCSR3	—	Output level control/status register 3	—
OCSR4	—	Output level control/status register 4	—
OCSR5	—	Output level control/status register 5	—
ALR2	—	Active level register 2	—
ALR3	—	Active level register 3	—
ALR4	—	Active level register 4	—
ALR5	—	Active level register 5	—

Register	Bit	RX66T (POE3B)	RX660 (POE3a)
SPOER	MTUCH34HIZ	MTU3 and MTU4 pin output stop enable bit 0: Does not stop output on pins. 1: Stops output on pins.	MTU3 and MTU4 pin high-impedance enable bit 0: Does not put the outputs in the high-impedance state. 1: Puts the outputs in the high-impedance state.
	MTUCH67HIZ	MTU6 and MTU7 pin output stop enable bit 0: Does not stop output on pins. 1: Stops output on pins.	MTU6 and MTU7 pin high-impedance enable bit 0: Does not put the outputs in the high-impedance state. 1: Puts the outputs in the high-impedance state.
	MTUCH0HIZ	MTU0 pin output stop enable bit 0: Does not stop output on pins. 1: Stops output on pins.	MTU0 pin high-impedance enable bit 0: Does not put the outputs in the high-impedance state. 1: Puts the outputs in the high-impedance state.
	GPT01HIZ	GPTW0 and GPTW1 pin output stop enable bit	—
	GPT23HIZ	GPTW2 and GPTW3 pin output stop enable bit	—
	MTUCH9HIZ	MTU9 pin output stop enable bit	—
	GPT02HIZ	GPTW0 to GPTW2 pin output stop enable bit	—
	GPT46HIZ	GPTW4 to GPTW6 pin output stop enable bit	—
	GPT79HIZ	GPTW7 to GPTW9 pin output stop enable bit	—
POECR3	—	Port output enable control register 3	—
POECR4	CMADDMT34ZE	Bit for adding CFLAG to the MTU3 and MTU4 output stop conditions	—
	IC1ADDMT34ZE	Bit for adding POE0F to the MTU3 and MTU4 output stop conditions	—
	IC2ADDMT34ZE	Bit for adding POE4F to the MTU3 and MTU4 output stop conditions 0: Does not stop output on pins. 1: Stops output on pins.	Bit for adding POE4F to the MTU3 and MTU4 high-impedance conditions 0: Does not put the outputs in the high-impedance state. 1: Puts the outputs in the high-impedance state.
	IC3ADDMT34ZE	Bit for adding POE8F to the MTU3 and MTU4 output stop conditions 0: Does not stop output on pins. 1: Stops output on pins.	Bit for adding POE8F to the MTU3 and MTU4 high-impedance conditions 0: Does not put the outputs in the high-impedance state. 1: Puts the outputs in the high-impedance state.

Register	Bit	RX66T (POE3B)	RX660 (POE3a)
POECR4	IC4ADDMT34ZE	Bit for adding POE10F to the MTU3 and MTU4 output stop conditions 0: Does not stop output on pins. 1: Stops output on pins.	Bit for adding POE10F to the MTU3 and MTU4 high-impedance conditions 0: Does not put the outputs in the high-impedance state. 1: Puts the outputs in the high-impedance state.
	IC5ADDMT34ZE	Bit for adding POE12Fto the TU3 and MTU4 output stop conditions 0: Does not stop output on pins. 1: Stops output on pins.	Bit for adding POE11F to the MTU3 and MTU4 high-impedance conditions 0: Does not put the outputs in the high-impedance state. 1: Puts the outputs in the high-impedance state.
	IC6ADDMT34ZE	Bit for adding POE12Fto the MTU3 and MTU4 output stop conditions	—
	IC8ADDMT34ZE	Bit for adding POE9F to the MTU3 and MTU4 output stop conditions	—
	IC9ADDMT34ZE	Bit for adding POE13F to the MTU3 and MTU4 output stop conditions	—
	IC10ADDMT34ZE	Bit for adding POE14F to the MTU3 and MTU4 output stop conditions	—
	IC1ADDMT67ZE	—	Bit for adding POE0F to the MTU6 and MTU7 high-impedance conditions
	IC3ADDMT67ZE	—	Bit for adding POE8F to the MTU6 and MTU7 high-impedance conditions
	IC4ADDMT67ZE	—	Bit for adding POE10F to the MTU6 and MTU7 high-impedance conditions
	IC5ADDMT67ZE	—	Bit for adding POE11F to the MTU6 and MTU7 high-impedance conditions
POECR4B	—	Port output enable control register 4B	—
POECR5	CMADDMT0ZE	Bit for adding CFLAG to the MTU0 output stop conditions	—
	IC1ADDMT0ZE	Bit for adding POE0F to the MTU0 output stop conditions 0: The flag is not added to the output stop control conditions. 1: The flag is added to the output stop control conditions.	Bit for adding POE0F to the MTU0 high-impedance conditions 0: The flag is not added to the high-impedance control conditions. 1: The flag is added to the high-impedance control conditions.
	IC2ADDMT0ZE	Bit for adding POE4F to the MTU0 output stop conditions 0: The flag is not added to the output stop control conditions. 1: The flag is added to the output stop control conditions.	Bit for adding POE4F to the MTU0 high-impedance conditions 0: The flag is not added to the high-impedance control conditions. 1: The flag is added to the high-impedance control conditions.
	IC3ADDMT0ZE	Bit for adding POE8F to the MTU0 output stop conditions	—

Register	Bit	RX66T (POE3B)	RX660 (POE3a)
POECR5	IC4ADDMT0ZE	Bit for adding POE10F to the MTU0 output stop conditions 0: The flag is not added to the output stop control conditions. 1: The flag is added to the output stop control conditions.	Bit for adding POE10F to the MTU0 high-impedance conditions 0: The flag is not added to the high-impedance control conditions. 1: The flag is added to the high-impedance control conditions.
	IC5ADDMT0ZE	Bit for adding POE11F to the MTU0 output stop conditions 0: The flag is not added to the output stop control conditions. 1: The flag is added to the output stop control conditions.	Bit for adding POE11F to the MTU0 high-impedance conditions 0: The flag is not added to the high-impedance control conditions. 1: The flag is added to the high-impedance control conditions.
	IC6ADDMT0ZE	Bit for adding POE12F to the MTU0 output stop conditions	—
	IC8ADDMT0ZE	Bit for adding POE9F to the MTU0 output stop conditions	—
	IC9ADDMT0ZE	Bit for adding POE13F to the MTU0 output stop conditions	—
	IC10ADDMT0ZE	Bit for adding POE14F to the MTU0 output stop conditions	—
POECR6	—	Port output enable control register 6	—
POECR6B	—	Port output enable control register 6B	—
POECR7	—	Port output enable control register 7	—
POECR8	—	Port output enable control register 8	—
POECR9	—	Port output enable control register 9	—
POECR10	—	Port output enable control register 10	—
POECR11	—	Port output enable control register 11	—
PMMCR0	—	Port mode mask control register 0	—
PMMCR1	—	Port mode mask control register 1	—
PMMCR2	—	Port mode mask control register 2	—
PMMCR3	—	Port mode mask control register 3	—
POECMPFR	—	Port output enable comparator detection flag register	—
POECMPSEL	—	Port output enable comparator request select register	—
POECMPEXm	—	Port output enable comparator request extension select register m (m = 0 to 8)	—

Register	Bit	RX66T (POE3B)	RX660 (POE3a)
M0SELR1	M0ASEL[3:0]	MTU0-A (MTIOC0A) pin select bits b3 b0 0 0 0 0: Does not control the output stop state for any MTIOC0A pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC0A pin is assigned to PB3. 0 0 1 0: Controls the output stop state on the assumption that the MTIOC0A pin is assigned to P31.(Note 1) Settings other than the above are prohibited.	MTU0-A (MTIOC0A) pin select bits (Note 1) b3 b0 0 0 0 0: Controls the high-impedance state on the assumption that the MTIOC0A pin is assigned to P34.(Note 1) 0 0 1 0: Controls the high-impedance state on the assumption that the MTIOC0A pin is assigned to PB3. Settings other than the above are prohibited.
	M0BSEL[3:0]	MTU0-B (MTIOC0B) pin select bits b7 b4 0 0 0 0: Does not control the output stop state for any MTIOC0B pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC0B pin is assigned to PB2. 0 0 1 0: Controls the output stop state on the assumption that the MTIOC0B pin is assigned to P30.(Note 1) 0 0 1 1: Controls the output stop state on the assumption that the MTIOC0B pin is assigned to PC0.(Note 3) Settings other than the above are prohibited.	MTU0-B (MTIOC0B) pin select bits b7 b4 0 0 0 0: Controls the high-impedance state on the assumption that the MTIOC0B pin is assigned to P13.(Note 1) 0 0 0 1: Controls the high-impedance state on the assumption that the MTIOC0B pin is assigned to P15. 0 0 1 0: Controls the high-impedance state on the assumption that the MTIOC0B pin is assigned to PA1. Settings other than the above are prohibited.

Register	Bit	RX66T (POE3B)	RX660 (POE3a)
M0SELR2	M0CSEL[3:0]	MTU0-C (MTIOC0C) pin select bits b3 b0 0 0 0 0: Does not control the output stop state for any MTIOC0C pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC0C pin is assigned to PB1. 0 0 1 0: Controls the output stop state on the assumption that the MTIOC0C pin is assigned to P27.(Note 4) 0 0 1 1: Controls the output stop state on the assumption that the MTIOC0C pin is assigned PC1.(Note 5) Settings other than the above are prohibited.	MTU0-C (MTIOC0C) pin select bits (Note 2) b3 b0 0 0 0 0: Controls the high-impedance state on the assumption that the MTIOC0C pin is assigned to P32.(Note 2) 0 0 1 0: Controls the high-impedance state on the assumption that the MTIOC0C pin is assigned to PB1. Settings other than the above are prohibited.
	M0DSEL[3:0]	MTU0-D (MTIOC0D) pin select bits b7 b4 0 0 0 0: Does not control the output stop state for any MTIOC0D pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC0D pin is assigned to PB0. 0 0 1 1: Controls the output stop state on the assumption that the MTIOC0D pin is assigned to PC2.(Note 5) Settings other than the above are prohibited.	MTU0-D (MTIOC0D) pin select bits b7 b4 0 0 0 0: Controls the high-impedance state on the assumption that the MTIOC0D pin is assigned to P33.(Note 2) 0 0 1 0: Controls the high-impedance state on the assumption that the MTIOC0D pin is assigned to PA3. Settings other than the above are prohibited.

Register	Bit	RX66T (POE3B)	RX660 (POE3a)
M3SELR	M3BSEL[3:0]	MTU3-B (MTIOC3B) pin select bits b3 b0 0 0 0 0: Does not control the output stop state for any MTIOC3B pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC3B pin is assigned to P71. 0 0 1 0: Controls the output stop state on the assumption that the MTIOC3B pin is assigned to P12.(Note 5) Settings other than the above are prohibited.	MTU3-B (MTIOC3B) pin select bits b3 b0 0 0 0 0: Controls the high-impedance state on the assumption that the MTIOC3B pin is assigned to PE1. 0 0 0 1: Controls the high-impedance state on the assumption that the MTIOC3B pin is assigned to P22.(Note 3) 0 0 1 0: Controls the high-impedance state on the assumption that the MTIOC3B pin is assigned to P80.(Note 5) 0 0 1 1: Controls the high-impedance state on the assumption that the MTIOC3B pin is assigned to PC5. 0 1 0 0: Controls the high-impedance state on the assumption that the MTIOC3B pin is assigned to PB7.(Note 2) 0 1 0 1: Controls the high-impedance state on the assumption that the MTIOC3B pin is assigned to P17. Settings other than the above are prohibited.

Register	Bit	RX66T (POE3B)	RX660 (POE3a)
M3SELR	M3DSEL[3:0]	MTU3-D (MTIOC3D) pin select bits b7 b4 0 0 0 0: Does not control the output stop state for any MTIOC3D pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC3D pin is assigned to P74. 0 0 1 0: Controls the output stop state on the assumption that the MTIOC3D pin is assigned to P15.(Note 5) Settings other than the above are prohibited.	MTU3-D (MTIOC3D) pin select bits b7 b4 0 0 0 0: Controls the high-impedance state on the assumption that the MTIOC3D MTIOC3B pin is assigned to PE0.(Note 2) 0 0 0 1: Controls the high-impedance state on the assumption that the MTIOC3D pin is assigned to P23.(Note 3) 0 0 1 0: Controls the high-impedance state on the assumption that the MTIOC3D pin is assigned to PC4. 0 0 1 1: Controls the high-impedance state on the assumption that the MTIOC3D pin is assigned to P81.(Note 5) 0 1 0 0: Controls the high-impedance state on the assumption that the MTIOC3D pin is assigned to PB6.(Note 2) 0 1 0 1: Controls the high-impedance state on the assumption that the MTIOC3D pin is assigned to P16. Settings other than the above are prohibited.

Register	Bit	RX66T (POE3B)	RX660 (POE3a)
M4SELR1	M4ASEL[3:0]	MTU4-A (MTIOC4A) pin select bits b3 b0 0 0 0 0: Does not control the output stop state for any MTIOC4A pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC4A pin is assigned to P72. 0 0 1 0: Controls the output stop state on the assumption that the MTIOC4A pin is assigned to P13.(Note 5) Settings other than the above are prohibited.	MTU4-A (MTIOC4A) pin select bits b3 b0 0 0 0 0: Controls the high-impedance state on the assumption that the MTIOC4A pin is assigned to PE2. 0 0 0 1: Controls the high-impedance state on the assumption that the MTIOC4A pin is assigned to P21.(Note 1) 0 0 1 0: Controls the high-impedance state on the assumption that the MTIOC4A pin is assigned to PB3. 0 0 1 1: Controls the high-impedance state on the assumption that the MTIOC4A pin is assigned to P82.(Note 5) 0 1 0 0: Controls the high-impedance state on the assumption that the MTIOC4A pin is assigned to PA0.(Note 2) 0 1 0 1: Controls the high-impedance state on the assumption that the MTIOC4A pin is assigned to P24.(Note 3) Settings other than the above are prohibited.

Register	Bit	RX66T (POE3B)	RX660 (POE3a)
M4SELR1	M4CSEL[3:0]	MTU4-C (MTIOC4C) pin select bits b7 b4 0 0 0 0: Does not control the output stop state for any MTIOC4C pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC4C pin is assigned to P75. 0 0 1 0: Controls the output stop state on the assumption that the MTIOC4C pin is assigned to P16.(Note 5) Settings other than the above are prohibited.	MTU4-C (MTIOC4C) pin select bits b7 b4 0 0 0 0: Controls the high-impedance state on the assumption that the MTIOC4C pin is assigned to PE5.(Note 2) 0 0 0 1: Controls the high-impedance state on the assumption that the MTIOC4C pin is assigned to P87.(Note 5) 0 0 1 0: Controls the high-impedance state on the assumption that the MTIOC4C pin is assigned to PB1. 0 0 1 1: Controls the high-impedance state on the assumption that the MTIOC4C pin is assigned to P83.(Note 5) 0 1 0 0: Controls the high-impedance state on the assumption that the MTIOC4C pin is assigned to PE1. 0 1 0 1: Controls the high-impedance state on the assumption that the MTIOC4C pin is assigned to P25.(Note 3) Settings other than the above are prohibited.

Register	Bit	RX66T (POE3B)	RX660 (POE3a)
M4SELR2	M4BSEL[3:0]	MTU4-B (MTIOC4B) pin select bits b3 b0 0 0 0 0: Does not control the output stop state for any MTIOC4B pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC4B pin is assigned to P73. 0 0 1 0: Controls the output stop state on the assumption that the MTIOC4B pin is assigned to P14.(Note 5) Settings other than the above are prohibited.	MTU4-B (MTIOC4B) pin select bits b3 b0 0 0 0 0: Controls the high-impedance state on the assumption that the MTIOC4B pin is assigned to PE3. 0 0 0 1: Controls the high-impedance state on the assumption that the MTIOC4B pin is assigned to P17. 0 0 1 0: Controls the high-impedance state on the assumption that the MTIOC4B pin is assigned to P54.(Note 2) 0 0 1 1: Controls the high-impedance state on the assumption that the MTIOC4B pin is assigned to PC2.(Note 2) 0 1 0 0: Controls the high-impedance state on the assumption that the MTIOC4B pin is assigned to PD1.(Note 1) 0 1 0 1: Controls the high-impedance state on the assumption that the MTIOC4B pin is assigned to P30. Settings other than the above are prohibited.

Register	Bit	RX66T (POE3B)	RX660 (POE3a)
M4SELR2	M4DSEL[3:0]	MTU4-D (MTIOC4D) pin select bits b7 b4 0 0 0 0: Does not control the output stop state for any MTIOC4D pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC4D pin is assigned to P76. 0 0 1 0: Controls the output stop state on the assumption that the MTIOC4D pin is assigned to P17.(Note 5) Settings other than the above are prohibited.	MTU4-D (MTIOC4D) pin select bits b7 b4 0 0 0 0: Controls the high-impedance state on the assumption that the MTIOC4D pin is assigned to PE4. 0 0 0 1: Controls the high-impedance state on the assumption that the MTIOC4D pin is assigned to P86.(Note 5) 0 0 1 0: Controls the high-impedance state on the assumption that the MTIOC4D pin is assigned to P55.(Note 2) 0 0 1 1: Controls the high-impedance state on the assumption that the MTIOC4D pin is assigned to PC3.(Note 2) 0 1 0 0: Controls the high-impedance state on the assumption that the MTIOC4D pin is assigned to PD2.(Note 1) 0 1 0 1: Controls the high-impedance state on the assumption that the MTIOC4D pin is assigned to P31. Settings other than the above are prohibited.
M6SELR	—	MTU6 pin select register	—
M7SELR1	—	MTU7 pin select register 1	—
M7SELR2	—	MTU7 pin select register 2	—
M9SELR1	—	MTU9 pin select register 1	—
M9SELR2	—	MTU9 pin select register 2	—
G0SELR	—	GPTW0 pin select register	—
G1SELR	—	GPTW1 pin select register	—
G2SELR	—	GPTW2 pin select register	—
G3SELR	—	GPTW3 pin select register	—
G4SELR	—	GPTW4 pin select register	—
G5SELR	—	GPTW5 pin select register	—
G6SELR	—	GPTW6 pin select register	—
G7SELR	—	GPTW7 pin select register	—
G8SELR	—	GPTW8 pin select register	—
G9SELR	—	GPTW9 pin select register	—

Note 1. This can be selected for products with 80 more pins.
Note 2. This can be selected for products with 64 more pins.
Note 3. This can be selected for products with 100 more pins.
Note 4. This can be selected for 144-pin, 112-pin, and 80-pin products and 100-pin products with PGA pseudo-differential input.
Note 5. This can be selected for 144-pin products only.

2.16 8-Bit Timer

Table 2.57 is Comparative Overview of 8-Bit Timers.

Table 2.57 Comparative Overview of 8-Bit Timers

Item	RX66T (TMRb)	RX660 (TMRb)
Count clocks	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock: External count clock	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock: External count clock
Number of channels	(8 bits × 2 channels) × 4 units	(8 bits × 2 channels) × 2 units
compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selectable among compare match A or B, or an external counter reset signal.	Selectable among compare match A or B, or an external counter reset signal.
Timer output	Output pulses with a user-defined duty cycle or PWM output	Output pulses with a user-defined duty cycle or PWM output
Cascading of two channels	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits, TMR4 for the upper 8 bits and TMR5 for the lower 8 bits, TMR6 for the upper 8 bits and TMR7 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches, TMR5 can be used to count TMR4 compare matches, TMR7 can be used to count TMR6 compare matches).	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
Event link function (output)	Compare match A, compare match B, and overflow (TMR0 to TMR3)	Compare match A, compare match B, and overflow (TMR0 to TMR3)
Event link function (input)	Ability to perform one of three actions according to accepted event (1) Counter start (TMR0 to TMR3) (2) Event counter (TMR0 to TMR3) (3) Counter restart (TMR0 to TMR3)	Ability to perform one of three actions according to accepted event (1) Counter start (TMR0 to TMR3) (2) Event counter (TMR0 to TMR3) (3) Counter restart (TMR0 to TMR3)
Generation of trigger to start A/D converter	Compare match A of TMR0, TMR2, TMR4 or TMR6	Compare match A of TMR0 or TMR2
DTC activation	The DTC can be activated by compare match A interrupts or compare match B interrupts.	The DTC can be activated by compare match A interrupts or compare match B interrupts.
Generation of SCI basic clock	Generation of SCI basic clock	Generation of SCI basic clock

Item	RX66T (TMRb)	RX660 (TMRb)
Generation of REMC operation clock	—	Generation of REMC (remote control signal receiver) operation clock
Low power consumption function	Transition to the module stop state is possible for each unit.	Transition to the module stop state is possible for each unit.

2.17 Serial Communications Interface

Table 2.58 is Comparative Overview of Serial Communications Interfaces, Table 2.59 is Comparison of Serial Communications Interface Channel Specifications, and Table 2.60 is Comparison of Serial Communications Interface Registers.

Table 2.58 Comparative Overview of Serial Communications Interfaces

Item		RX66T (SCIj, SCIi, SCIh)	RX660 (SCIk, SCIm, SCIh)
Number of channels		• SCIj: 5 channels • SCIi: 1 channel • SCIh: 1 channel	• SCIk: 10 channels • SCIm: 2 channels • SCIh: 1 channel
Serial communications modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable as LSB first or MSB first transfer.	Selectable as LSB first or MSB first transfer.
I/O signal level inversion		—	The levels of input and output signals can be inverted independently.
Interrupt sources		• Transmit end, transmit data empty, receive data full, receive error, receive data ready, and data match • Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)	• Transmit end, transmit data empty, receive data full, receive error, receive data ready, and data match • Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)
Low power consumption function		Transition to the module stop state is possible for each channel.	Transition to the module stop state is possible for each channel.
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection function	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.

Item		RX66T (SCIj, SCIi, SCIh)	RX660 (SCIk, SCIm, SCIh)
Asynchronous mode	Transmit/receive FIFO	Ability to use 16-stage FIFOs for transmission and reception (SCI11)	Ability to use 16-stage FIFOs for transmission and reception (SCI10 and SCI11)
	Data match detection	Compares receive data and comparison data register, and generates an interrupt request when they are matched (SCI11).	Compares receive data and comparison data register, and generates interrupt when they are matched (SCI0 to SCI11).
	Start-bit detection	Low level or falling edge is selectable.	Low level or falling edge is selectable.
	Receive data sampling timing adjustment	—	The receive data sampling point can be shifted from the center of the data forward or backward to a base point.
	Transmit signal change timing adjustment	—	Either the falling or rising edge of the transmit data can be delayed.
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly or by reading the SPTR.RXDMON flag.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly or by reading the SPTR.RXDMON flag.
	Clock source	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5, SCI6, and SCI12).	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5, SCI6, and SCI12).
	Double-speed mode	Baud rate generator double-speed mode is selectable.	Baud rate generator double-speed mode is selectable.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	CTSn and RTSn pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Transmit/receive FIFO	Ability to use 16-stage FIFOs for transmission and reception	Ability to use 16-stage FIFOs for transmission and reception
Smart card interface mode	Error processing	• An error signal can be automatically transmitted when detecting a parity error during reception • Data can be automatically retransmitted when receiving an error signal during transmission	• An error signal can be automatically transmitted when detecting a parity error during reception. • Data can be automatically retransmitted when receiving an error signal during transmission.
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.

Item		RX66T (SCIj, SCIi, SCIh)	RX660 (SCIk, SCIm, SCIh)
Simple I²C mode	Communication format	I²C bus format	I²C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer speed	Fast mode is supported.	Fast mode is supported.
	Noise cancellation	• The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters. • The interval for noise cancellation is adjustable.	• The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters. • The interval for noise cancellation is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.
Extended serial mode (supported by SCI12 only)	Start frame transmission	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection
	Start frame reception	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two kinds of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two kinds of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates

Item		RX66T (SCIj, SCIi, SCIh)	RX660 (SCIk, SCIm, SCIh)
Extended serial mode (supported by SCI12 only)	I/O control function	• Ability to select polarity or TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select receive data sampling timing of RXDX12 pin	• Ability to select polarity or TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select receive data sampling timing of RXDX12 pin
	Timer function	Usable as reloading timer	Usable as reloading timer
Bit rate modulation function		Correction of outputs from the on-chip baud rate generator can reduce errors.	Correction of outputs from the on-chip baud rate generator can reduce errors.
Event link function		• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output	• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output

Table 2.59 Comparison of Serial Communications Interface Channel Specifications

Item	RX66T (SCIj, SCIi, SCIh)	RX660 (SCIk, SCIm, SCIh)
Asynchronous mode	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12
Clock synchronous mode	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12
Smart card interface mode	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12
Simple I^2C mode	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12
Simple SPI mode	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6 SCI7, SCI8, SCI9, SCI10, SCI11, SCI12
FIFO mode	SCI11	SCI10, SCI11
Data match detection	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11
Extended serial mode	SCI12	SCI12
TMR clock input	SCI5, SCI6, SCI12	SCI5, SCI6, SCI12
Event link function	SCI5	SCI5
Peripheral module clock	PCLKA: SCI11 PCLKB: SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	PCLKA: SCI10, SCI11 PCLKB: SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI12

Table 2.60 Comparison of Serial Communications Interface Registers

Register	Bit	RX66T (SCIj, SCIi, SCIh)	RX660 (SCIk, SCIm, SCIh)
SEMR	ITE	—	Immediate transmission enable bit
SPTR	RXDMON	RXD line monitoring flag 0: RXDn pin is at the low level. 1: RXDn pin is at the high level.	RXD line monitoring flag When the RINV bit is set to 0: 0: RXDn pin is at the low level. 1: RXDn pin is at the high level. When the RINV bit is set to 1: 0: RXDn pin is at the high level. 1: RXDn pin is at the low level.
	RINV	—	Receiver input invert bit
	TINV	—	Transmission output inversion bit
	RTADJ	—	Receive data sampling timing adjustment bit
	TTADJ	—	Transmit signal change timing adjustment bit
TMGR	—	—	Transmit/receive timing select register

2.18 I²C Bus Interface

Table 2.61 is Comparison of I2C Bus Interface Registers.

Table 2.61 Comparison of I²C Bus Interface Registers

Register	Bit	RX66T (RIICa)	RX660 (RIICa)
ICCR1	SDAI	SDA line monitor bit 0: SDA0 line is low. 1: SDA0 line is high.	SDA line monitor bit 0: SDAn line is low. 1: SDAn line is high.
	SCLI	SCL line monitor bit 0: SCL0 line is low. 1: SCL0 line is high.	SCL line monitor bit 0: SCLn line is low. 1: SCLn line is high.
	SDAO	SDA output control/monitor bit • Read 0: The SDA0 pin has been driven low. 1: The SDA0 pin has been released. • Write 0: The SDA0 pin is driven low. 1: The SDA0 pin is released.	SDA output control/monitor bit • Read 0: SDAn pin driven low. 1: SDAn pin released. • Write 0: SDAn pin driven low. 1: SDAn pin released. (High-level output is achieved through an external pull-up resistor.)
	SCLO	SCL output control/monitor bit • Read 0: The SCL0 pin has been driven low. 1: The SCL0 pin has been released. • Write 0: The SCL0 pin is driven low. 1: The SCL0 pin is released. (High-level output is achieved through an external pull-up resistor.)	SCL output control/monitor bit • Read 0: The SCLn pin has been driven low. 1: The SCLn pin has been released. • Write 0: The SCLn pin is driven low. 1: The SCLn pin is released. (High-level output is achieved through an external pull-up resistor.)
	IICRST	I²C-bus interface internal reset bit 0: Releases RIIC reset or internal reset. 1: Initiates RIIC reset or internal reset. (Clears the bit counter and the SCL0/SDA0 output latch.)	I²C-bus interface internal reset bit 0: Releases RIIC reset or internal reset. 1: Initiates RIIC reset or internal reset. (Clears the bit counter and the SCLn/SDAn output latch.)
	ICE	I²C-bus interface enable bit 0: Disabled (SCL0 and SDA0 pins in inactive state). 1: Enabled (SCL0 and SDA0 pins in active state). (Combined with the IICRST bit to select either RIIC or internal reset.)	I²C-bus interface enable bit 0: Disabled (SCLn and SDAn pins in inactive state). 1: Enabled (SCLn and SDAn pins in active state). (Combined with the IICRST bit to select either RIIC or internal reset.)

Register	Bit	RX66T (RIICa)	RX660 (RIICa)
ICMR2	TMOL	Timeout L count control bit 0: Count-up is disabled while the SCL0 line is low. 1: Count-up is enabled while the SCL0 line is low.	Timeout L count control bit 0: Count-up is disabled while the SCLn line is low. 1: Count-up is enabled while the SCLn line is low.
	TMOH	Timeout H count control bit 0: Count-up is disabled while the SCL0 line is high. 1: Count-up is enabled while the SCL0 line is high.	Timeout H count control bit 0: Count-up is disabled while the SCLn line is high. 1: Count-up is enabled while the SCLn line is high.
ICMR3	RDRFS	RDRF flag set timing select bit 0: The RDRF flag is set to 1 at the rising edge of the ninth SCL clock cycle. (The SCL0 line is not held low at the falling edge of the eighth clock pulse.) 1: The RDRF flag is set to 1 at the rising edge of the eighth SCL clock cycle. (The SCL0 line is held low at the falling edge of the eighth clock cycle.) Low-hold is released by writing a value to the ACKBT bit.	RDRF flag set timing select bit 0: The RDRF flag is set to 1 at the rising edge of the ninth SCL clock cycle. (The SCLn line is not held low at the falling edge of the eighth clock cycle.) 1: The RDRF flag is set to 1 at the rising edge of the eighth SCL clock cycle. (The SCLn line is not held low at the falling edge of the eighth clock cycle.) Low-hold is released by writing a value to the ACKBT bit.

2.19 CAN Module and CANFD Module

Table 2.62 is Comparative Overview of CAN Module and CANFD Module, and Table 2.63 is Comparison of CAN Module/CANFD Module Registers.

Table 2.62 Comparative Overview of CAN Module and CANFD Module

Item	RX66T (CAN)	RX660 (CANFD-Lite)
Protocol	Conforming to the ISO 11898-1 standard (standard frame or extension frame)	Conforming to the ISO 11898-1:2015 specifications
Bit rate (RX66T) Data transfer rate (RX660)	Programming is possible with a maximum bit rate of 1 Mbps (fCAN is equal to or larger than 8 MHz). — fCAN: CAN clock source	• Arbitration phase: Maximum of 1 Mbps • Data phase: Maximum 8 Mbps(Note 1)
Operating frequency	PCLKB: 60MHz (max) CANFDMCLK: 24 MHz (max)	• Register block: Maximum of 60 MHz (PCLKB) • Message buffer RAM: Maximum of 120 MHz (PCLKA)
Operating clock for data link layer (DLL clock)	—	Maximum of 60 MHz (either CANFDMCLK or CANFDCLK can be selected)
Message box (RX66T) Message buffer (RX660)	32 mailboxes: Two mail box modes can be selected. • Normal mailbox mode: 32 mailboxes can be configured for transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for transmission or reception. The remaining mailboxes can be configured as a 4-stage transmit FIFO and a 4-stage receive FIFO.	• 32 receive message buffers • Four transmit message buffers • One transmit queue Automatic transfer of messages to the transmit queue is supported.
Frame type	• Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID) • Remote frame in base format (11-bit ID) • Remote frame in extended format (29-bit ID)	Classic CAN (CAN 2.0) • Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID) • Remote frame in base format (11-bit ID) • Remote frame in extended format (29-bit ID) CAN FD(Note 1) • Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID)

Item	RX66T (CAN)	RX660 (CANFD-Lite)
Reception	• Data frames and remote frames can be received. • The ID format to be received (base ID only, extended ID only, or both base ID and extended ID) can be selected. • The one-shot receive function can be selected. • Overwrite mode (message is overwritten) or overrun mode (message is discarded) can be selected. • Reception end interrupt can be enabled or disabled individually for each mailbox.	• Data frames and remote frames can be received. • The ID format to be received (base ID only, extended ID only, or both base ID and extended ID) can be selected. • Receive message buffer interrupt can be enabled or disabled individually for each message buffer.
Data length	0 to 8 bytes	Classic CAN: 0 to 8 bytes CAN FD: 0 to 8, 12, 16, 20, 24, 32, 48, and 64 bytes(Note 1)
Acceptance filter	• Eight acceptance masks (an individual mask for every four mailboxes) • Mailbox masks can be enabled or disabled individually.	Filtering is possible in the following fields: • IDE bit (base format, extended format, or both) • ID field • RTR bit (data frame or remote frame) (only for Classic CAN) • DLC field Data (data length) The protection function when the payload size is exceeded is provided. Acceptance filter list (AFL) entries can be updated during communication.
Transmission	• Data frames and remote frames can be sent. • The ID format to be sent (base ID only, extended ID only, or both base ID and extended ID) can be selected. • The one-shot transmission function can be selected. • Either ID priority transmission mode or mailbox number priority transmission mode can be selected. • Transmission requests can be aborted (completion of abort can be confirmed with a flag). • Transmission end interrupt can be enabled or disabled individually for each mailbox.	• Data frames and remote frames can be sent. • The ID format to be sent (base ID only or extended ID only) can be selected. • The one-shot transmission function can be selected. • Either ID priority transmission mode or message buffer number priority transmission mode can be selected. • Transmission requests can be aborted (completion of abort can be confirmed with a flag). • Channel transmission interrupt can be enabled and disabled.
FIFO	• 24 mailboxes can be configured for transmission or reception. • The remaining mailboxes can be configured as a 4-stage transmit FIFO and a 4-stage receive FIFO.	The FIFO size is programmable. • Two receive FIFOs • One common FIFO (Whether to use the FIFO as a receive FIFO or transmit FIFO can be selected.)
Automatic transmission interval adjustment	—	• Available when the common FIFO is configured as a transmit FIFO • The interval between messages sent from the FIFO can be adjusted.

Item	RX66T (CAN)	RX660 (CANFD-Lite)
Bus-off recovery method	How to recover from the bus-off state can be selected. • Conforming to the ISO 11898-1 standard • The mode automatically changes to CAN Halt mode when bus off starts. • The mode automatically changes to CAN Halt mode when bus off ends. • A program causes a transition to CAN Halt mode. • A program causes a transition to error active state.	How to recover from the bus-off state can be selected. • Normal mode (ISO 11898-1 compliant) • Automatically enters CH_HALT mode when bus off starts. • Automatically enters CAN Halt mode when bus off ends • Software causes a transition CH_HALT mode (during bus-off recovery period). • A program causes a transition to error active state.
Timestamp function	• Timestamp function with a 16-bit counter • The reference clock can be selected from 1, 2, 4, and 8 bit time.	Transmission and reception timestamp function
Interrupt function	• Five types of interrupt sources (reception end interrupt, transmission end interrupt, receive FIFO interrupt, transmit FIFO interrupt, and error interrupt)	Receive FIFO interrupt Global error interrupt Channel transmission interrupt Channel error interrupt Common FIFO reception interrupt Receive message buffer interrupt
CAN sleep mode	Current consumption can be reduced by stopping the CAN clock.	Module start/stop function for each CAN node (CH_SLEEP mode and GL_SLEEP mode)
Software support	—	Label information is automatically added to received messages.
Software support units	Three software support unis • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support	—
Test modes	Three test modes are provided for user evaluation: • Listen-only mode • Self test mode 0 (external loopback) • Self test mode 1 (internal loopback)	• Basic test mode • Listen-only mode • Self test mode 0 (external loopback) • Self test mode 1 (internal loopback)
Low power consumption function (RX66T) Power down function (RX660)	Transition to the module stop state is possible.	Module start/stop function for each CAN node (CH_SLEEP mode and GL_SLEEP mode) Transition to the module stop state is possible.
RAM	—	RAM with ECC protection

Note 1. This is only available for products that support the CAN FD protocol.

Table 2.63 Comparison of CAN Module/CANFD Module Registers

Register	Bit	RX66T (CAN)	RX660 (CANFD-Lite)
CTLR	—	Control register	—
BCR	—	Bit configuration register	—
MKRk	—	Mask register k (k = 0 to 7)	—
FIDCR0 FIDCR1	—	FIFO receive ID comparison register	—
MKIVLR	—	Mask disable register	—
MBj	—	Mailbox register j (j = 0 to 31)	—
MIER	—	Mailbox interrupt enable register	—
MCTLj	—	Message control register j (j = 0 to 3)	—
RFCR	—	Receive FIFO control register	—
RFPCR	—	Receive FIFO pointer control register	—
TFCR	—	Transmit FIFO control register	—
TFPCR	—	Transmit FIFO pointer control register	—
STR	—	Status register	—
MSMR	—	Mailbox search mode register	—
MSSR	—	Mailbox search status register	—
CSSR	—	Channel search support register	—
AFSR	—	Acceptance filter support register	—
EIER	—	Error interrupt enable register	—
EIFR	—	Error interrupt source decision register	—
RECR	—	Receive error count register	—
TECR	—	Transmit error count register	—
ECSR	—	Error code storage register	—
TSR	—	Timestamp register	—
TCR	—	Test control register	—
NBCR	—	—	Nominal bit rate configuration register
CHCR	—	—	Channel control register
CHSR	—	—	Channel status register
CHESR	—	—	Channel error status register
DBCR	—	—	Data bit rate configuration register
FDCFG	—	—	CAN FD configuration register
FDCTR	—	—	CAN FD control register
FDSTS	—	—	CAN FD status register
FDCRC	—	—	CAN FD CRC register
GCFG	—	—	Global configuration register
GCR	—	—	Global control register
GSR	—	—	Global status register
GESR	—	—	Global error status register
TISR	—	—	Transmit interrupt status register
TSCR	—	—	Timestamp counter register
AFCR	—	—	Acceptance filter list control register
AFCFG	—	—	Acceptance filter list configuration register

Register	Bit	RX66T (CAN)	RX660 (CANFD-Lite)
AFLn.IDR	—	—	Acceptance filter list n ID register (n = 0 to 15)
AFLn.MASK	—	—	Acceptance filter list n mask register (n = 0 to 15)
AFLn.PTR0	—	—	Acceptance filter list n pointer register 0 (n = 0 to 15)
AFLn.PTR1	—	—	Acceptance filter list n pointer register 1 (n = 0 to 15)
RMCR	—	—	Receive message buffer configuration register
RMNDR	—	—	Receive message buffer new data register
RFCRn	—	—	Receive FIFO n configuration register (n = 0 or 1)
RFSRn	—	—	Receive FIFO n status register (n = 0 or 1)
RFPCRn	—	—	Receive FIFO n pointer control register (n = 0 or 1)
CFCR0	—	—	Common FIFO 0 configuration register
CFSR0	—	—	Common FIFO 0 status register
CFPCR0	—	—	Common FIFO 0 pointer control register
FESR	—	—	FIFO empty status register
FFSR	—	—	FIFO full status register
FMLSR	—	—	FIFO message lost status register
RFISR	—	—	Receive FIFO interrupt status register
DTCR	—	—	DMA transfer control register
DTSR	—	—	DMA transfer status register
TMCRn	—	—	Transmit message buffer n control register (n = 0 to 3)
TMSRn	—	—	Transmit message buffer n status register (n = 0 to 3)
TMTRSR0	—	—	Transmit message buffer transmission request status register 0
TMARSR0	—	—	Transmit message buffer transmission abort request status register 0
TMTCSR0	—	—	Transmit message buffer transmission completion status register 0
TMTASR0	—	—	Transmit message buffer transmission abort status register 0
TMIER0	—	—	transmission message buffer interrupt enable register 0
TQCR0	—	—	Transmit queue 0 configuration register
TQSR0	—	—	Transmit queue 0 status register
TQPCR0	—	—	Transmit queue 0 pointer control register
THCR	—	—	Transmission history configuration register
THSR	—	—	Transmission history status register

Register	Bit	RX66T (CAN)	RX660 (CANFD-Lite)
THACR0	—	—	Transmission history access register 0
THACR1	—	—	Transmission history access register 1
THPCR	—	—	Transmission history pointer control register
GRCR	—	—	Global reset control register
GTMCR	—	—	Global test mode configuration register
GTMER	—	—	Global test mode enable register
GTMLKR	—	—	Global test mode lock key register
RTPARk	—	—	RAM test page access register k (k = 0 to 63)
AFIGSR	—	—	Acceptance filter list ignore entry setting register
AFIGER	—	—	Acceptance filter list ignore entry enable register
RMIER	—	—	Receive message buffer interrupt enable register
ECCSR	—	—	ECC control/status register
ECTMR	—	—	ECC test mode register
ECTDR	—	—	ECC decoder test data register
ECEAR	—	—	ECC error address register

2.20 Serial Peripheral Interface

Table 2.64 is Comparative Overview of Serial Peripheral Interfaces, and Table 2.65 is Comparison of Serial Peripheral Interface Registers.

Table 2.64 Comparative Overview of Serial Peripheral Interfaces

Item	RX66T (RSPIc)	RX660 (RSPId)
Number of channels	1 channel	1 channel
RSPI transfer functions	• Use of MOSI (Master out/slave in), MISO (Master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Communication modes: Full-duplex or simplex (transmit-only) can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK	• Use of MOSI (Master out/slave in), MISO (Master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Communication modes: Full-duplex or simplex (transmit-only or reception-only (in slave mode)) can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK
Data format	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits). • Byte swapping of transmit and receive data is selectable	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits). • Byte swapping of transmit and receive data is selectable • Ability to invert the logic level of transmit/receive data
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4). — Width at high level: 2 cycles of PCLK — Width at low level: 2 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4). — Width at high level: 2 cycles of PCLK — Width at low level: 2 cycles of PCLK
Buffer configuration	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers

Item	RX66T (RSPIc)	RX660 (RSPId)
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection
SSL control function	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Range: 1 to 8 RSPCK cycles — (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Range: 1 to 8 RSPCK cycles — (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) — Range: 1 to 8 RSPCK cycles — (set in RSPCK-cycle units) • Function for changing SSL polarity	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Range: 1 to 8 RSPCK cycles — (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Range: 1 to 8 RSPCK cycles — (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) — Range: 1 to 8 RSPCK cycles — (set in RSPCK-cycle units) • Function for changing SSL polarity
Control in master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function • The delay between data bytes can be shortened during burst transfers.
Interrupt sources	• Interrupt sources — Receive buffer full interrupt — Transmit buffer empty interrupt — Error interrupt (mode fault, overrun, underrun, or parity error) — Idle interrupt	• Interrupt sources — Receive buffer full interrupt — Transmit buffer empty interrupt — Error interrupt (mode fault, overrun, underrun, or parity error) — Idle interrupt — Communication end interrupt

Item	RX66T (RSPIc)	RX660 (RSPId)
Event link function (output)	• Interrupt sources — Receive buffer full events — Transmit buffer empty events — Error events (mode fault, overrun, underrun, and parity error) — Idle events — Communication completion events	• Interrupt sources — Receive buffer full events — Transmit buffer empty events — Error events (mode fault, overrun, underrun, and parity error) — Idle events — Communication completion events
Other functions	• Function for initializing the RSPI • Loopback mode	• Function for initializing the RSPI • Loopback mode
Low power consumption function	• Transition to the module stop state is possible.	• Transition to the module stop state is possible.

Table 2.65 Comparison of Serial Peripheral Interface Registers

Register	Bit	RX66T (RSPIc)	RX660 (RSPId)
SPSR	SPCF	—	Communication completion flag
SPDCR2	DINV	—	Transfer data invert bit
SPCR3	—	—	RSPI control register 3

2.21 12-Bit A/D Converter

Table 2.66 is Comparative Overview of 12-Bit A/D Converters, and Table 2.67 is Comparison of 12-Bit A/D Converter Registers.

Table 2.66 Comparative Overview of 12-Bit A/D Converters

Item	RX66T (S12ADH)	RX660 (S12ADH)
Number of units	Three units (S12AD, S12AD1, and S12AD2)	One unit (S12AD)
Input channels	S12AD: 8 channels, S12AD1: 8 channels, S12AD2: 14 channels	24 channels
Extended analog function	Temperature sensor output, internal reference voltage (S12AD2 only)	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	0.9 µs per channel (when A/D conversion clock (ADCLK) = 60 MHz)	0.9 µs per channel (when A/D conversion clock (ADCLK) = 60 MHz)
A/D conversion clock	Peripheral module clock PCLKB and A/D conversion clock (ADCLK) can be set so that the frequency division ratio should be one of the following. PCLKB to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 1:1 ADCLK is set by using the clock generation circuit. The A/D conversion clock (ADCLK) can operate at frequencies from a maximum of 60 MHz to a minimum of 8 MHz.	Peripheral module clock PCLKB and A/D conversion clock (ADCLK) can be set so that the frequency division ratio should be one of the following. PCLKB to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1 ADCLK is set using the clock generation circuit. The A/D conversion clock (ADCLK) can operate at frequencies from a maximum of 60 MHz to a minimum of 8 MHz.

Item	RX66T (S12ADH)	RX660 (S12ADH)
Data registers	• 30 registers for analog input (S12AD: 8 registers, S12AD1: 8 registers, S12AD2: 14 registers), one register for A/D-converted data duplication in double trigger mode for each unit, and two registers for A/D-converted data duplication during extended operation in double trigger mode for each unit • One register for temperature sensor output (S12AD2) • One register for internal reference (S12AD2) • One register for self-diagnosis for each unit • The results of A/D conversion are stored in 12-bit A/D data registers. • The results of A/D conversion are stored in 12-bit A/D data registers. • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes) The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers) A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.	• 24 registers for analog input, one for A/D-converted data duplication in double trigger mode Two registers for A/D-converted data duplication during extended operation in double trigger mode • One register for temperature sensor output • One register for internal reference • One register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes) The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers) A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.

Item	RX66T (S12ADH)	RX660 (S12ADH)
Operating mode	The operating mode can be set individually for each of three units. • Single scan mode: A/D conversion is performed only once on arbitrarily selected analog inputs. A/D conversion is performed only once on the temperature sensor output (S12AD2). A/D conversion is performed only once on the internal reference voltage (S12AD2). • Continuous scan mode: A/D conversion is performed repeatedly on arbitrarily selected analog inputs. • Group scan mode: Two (groups A and B) or three (groups A, B, and C) can be selected as the number of groups to be used. (Only the combination of groups A and B can be selected when the number of groups is two.) Arbitrarily selected analog input channels, the temperature sensor output (S12AD2), and the internal reference voltage (S12AD2) are divided into two groups (group A and B) or three groups (group A, B, and C), and A/D conversion of the analog input selected on a group basis is performed only once. The scanning start condition for groups A, B, and C (synchronous trigger) can be independently selected, allowing A/D conversion of each group to be started independently. • Group scan mode (Group priority control selected) If a higher-priority group trigger is input during scanning of a lower-priority group, scanning of the lower-priority group stops and scanning of the higher-priority group starts. The priority order is group A (highest) > group B > group C (lowest). Whether or not to restart scanning (rescan) of the lower-priority group after processing for the higher-priority group completes, is selectable. Rescan can also be set to start either from the first selected channel or from the channel on which A/D conversion did not complete.	• Single scan mode: A/D conversion is performed only once on arbitrarily selected analog inputs. A/D conversion is performed only once on the temperature sensor output. A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: A/D conversion is performed repeatedly on arbitrarily selected analog inputs. • Group scan mode: Two (groups A and B) or three (groups A, B, and C) can be selected as the number of groups to be used. (Only the combination of groups A and B can be selected when the number of groups is two.) Arbitrarily selected analog input channels, the temperature sensor output, and the internal reference voltage are divided into two groups (group A and B) or three groups (group A, B, and C), and A/D conversion of the analog input selected on a group basis is performed only once. The scanning start condition for groups A, B, and C (synchronous trigger) can be independently selected, allowing A/D conversion of each group to be started independently. • Group scan mode (Group priority control selected) If a higher-priority group trigger is input during scanning of a lower-priority group, scanning of the lower-priority group stops and scanning of the higher-priority group starts. The priority order is group A (highest) > group B > group C (lowest). Whether or not to restart scanning (rescan) of the lower-priority group after processing for the higher-priority group completes, is selectable. Rescan can also be set to start either from the first selected channel or from the channel on which A/D conversion did not complete.

Item	RX66T (S12ADH)	RX660 (S12ADH)
Conditions for A/D conversion start	• Software trigger • Synchronous trigger • Trigger by the multi-function timer pulse unit (MTU), 8-bit timer (TMR), or event link controller (ELC) • Asynchronous trigger A/D conversion can be triggered by the external trigger ADTRG0# (S12AD), ADTRG1# (S12AD1), and ADTRG2# (S12AD2) pins (individually for each of three units.)	• Software trigger • Synchronous trigger • Trigger by the multi-function timer pulse unit (MTU), 8-bit timer (TMR), or event link controller (ELC) • Asynchronous trigger A/D conversion can be triggered by the external trigger ADTRG0# pin.
Functions	• Sample & hold function dedicated to channels (three channels for S12AD and 3 channels for S12AD1) (Constant sampling can be set.) • Variable sampling time (settable on a per-channel basis) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers • Compare function (window A and window B) • Order of channel conversion can be specified for each unit. • Input signal amplification function using the programmable gain amplifier (3-channel single-ended input or pseudo-differential input can be selected for each unit.)	• Variable sampling time (settable on a per-channel basis) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers • Compare function (window A and window B) • Ability to specify the channel conversion priority

Item	RX66T (S12ADH)	RX660 (S12ADH)
Interrupt sources	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of single scan (individually for each of 3 units.)	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI) can be generated on completion of single scan.
	• In double trigger mode, A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of double scan (individually for each of 3 units)).	• In double trigger mode, A/D scan end interrupt request (S12ADI) can be generated on completion of double scan.
	• In group scan mode, an A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of group A scan, an A/D scan end interrupt request (S12GBADI, S12GBADI1, or S12GBADI2) for group B can be generated on completion of group B scan, and an A/D scan end interrupt request (S12GCADI, S12GCADI1, or S12GCADI2 for group C can be generated on completion of group C scan.	• In group scan mode, an A/D scan end interrupt request (S12ADI) can be generated on completion of group A scan, an A/D scan end interrupt request (S12GBADI) for group B can be generated on completion of group B scan, and an A/D scan end interrupt request (S12GCADI) for group C can be generated on completion of group C scan.
	• When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of a double scan of group A. A corresponding scan end interrupt request (S12GBADI/S12GCADI, S12GBADI1/S12GCADI1, or S12GBADI2/S12GCADI2) can be generated on completion of a group B or group C scan.	• When double trigger mode is selected in group scan mode, A/D scan end interrupt request (S12ADI) can be generated on completion of double scan of group A. A corresponding scan end interrupt request (S12GBADI or S12GCADI) can be generated on completion of a group B or group C scan.
	• A compare interrupt request (S12CMPAI, S12CMPAI1, S12CMPAI2, S12CMPBI, S12CMPBI1, or S12CMPBI2) can be generated upon a match with the comparison condition for the digital compare function.	• A compare interrupt request (S12CMPAI or S12CMPBI) can be generated upon a match with the comparison condition for the digital compare function.
	• The S12ADI/S12ADI1/S12ADI2, S12GBADI/S12GBADI1/S12GBADI2, and S12GCADI/S12GCADI1/ S12GCADI2 interrupts can activate the DMA controller (DMAC) or data transfer controller (DTC).	• The S12ADI, S12GBADI, and S12GCADI interrupts can activate the DMA controller (DMAC) or data transfer controller (DTC).

Item	RX66T (S12ADH)	RX660 (S12ADH)
Event link function	• An event can be output upon completion of all scans. • In single scan mode, an event can be output when the compare function window condition is met. • Scan can be started by a trigger output by the ELC.	• An event can be output upon completion of all scans. • In single scan mode, an event can be output when the compare function window condition is met. • Scan can be started by a trigger output by the ELC.
Low power consumption function	Transition to the module stop state is possible.	Transition to the module stop state is possible.

Table 2.67 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX66T (S12ADH)	RX660 (S12ADH)
ADDRy	—	A/D data register y (y = 0 to 11, 16, or 17)	A/D data register y (y = 0 to 23)
ADANSA0	ANSA008 to ANSA015	—	A/D conversion channel select bits
ADANSA1	ANSA102 to ANSA107	—	A/D conversion channel select bits
ADANSB0	ANSB008 to ANSB015	—	A/D conversion channel select bits
ADANSB1	ANSB102 to ANSB107	—	A/D conversion channel select bits
ADANSC0	ANSC008 to ANSC015	—	A/D channel select register C0
ADANSC1	ANSC102 to ANSC107	—	A/D channel select register C1
ADSCSn	—	A/D channel conversion order setting register n (n = 0 to 13)	A/D channel conversion order setting register n (n = 0 to 23)
ADADS0	ADS008 to ADS015	—	A/D-converted value addition/average function select bits
ADADS1	ADS102 to ADS107	—	A/D-converted value addition/average function select bits
ADSSTRn	—	A/D sampling state register n (n = 0 to 11, L, T, or O)	A/D sampling state register n (n = 0 to 15, L, T, or O)
ADSHCR	—	A/D sample and hold circuit control register	—
ADSHMSR	—	A/D sample and hold operating mode select register	—
ADCMPANSR0	CMPCHA008 to CMPCHA015	—	Compare window A channel select bits
ADCMPANSR1	CMPCHA102 to CMPCHA107	—	Compare window A channel select bits
ADCMPLR0	CMPLCHA008 to CMPLCHA015	—	Compare window A comparison condition select bits
ADCMPLR1	CMPLCHA102 to CMPLCHA107	—	Compare window A comparison condition select bits
ADCMPSR0	CMPSTCHA008 to CMPSTCHA015	—	Compare window A flag

Register	Bit	RX66T (S12ADH)	RX660 (S12ADH)
ADCMPSR1	CMPSTCHA102 to CMPSTCHA107	—	Compare window A flag
ADCMPBNSR	CMPCHB[5:0]	Compare window B channel select bits These bits select channels to be compared with the compare window B conditions. b5 b0 0 0 0 0 0 0: AN000 0 0 0 0 0 1: AN001 0 0 0 0 1 0: AN002 : : 0 0 0 1 1 0: AN006 0 0 0 1 1 1: AN007 Settings other than the above are prohibited.	Compare window B channel select bits These bits select channels to be compared with the compare window B conditions. b5 b0 0 0 0 0 0 0: AN000 0 0 0 0 0 1: AN001 0 0 0 0 1 0: AN002 : : 0 1 0 1 1 0: AN022 0 1 0 1 1 1: AN023 1 0 0 0 0 0: Temperature sensor 1 0 0 0 0 1: Internal reference voltage Settings other than the above are prohibited.
ADPGACR	—	A/D programmable gain amplifier control register	—
ADPGAGS0	—	A/D programmable gain amplifier gain setting register 0	—
ADPGADCR0	—	A/D programmable gain differential input control register	—
ADVREFCR	—	—	A/D reference voltage control register

2.22 12-Bit D/A Converter

Table 2.68 is Comparative Overview of 12-bit D/A Converters.

Table 2.68 Comparative Overview of 12-bit D/A Converters

Item	RX66T (R12DAb)	RX660 (R12DAb)
Resolution	12-bit	12 bits
Output channels	2 channel	2 channel
Measure against interference between analog modules	• Measure against interference between D/A and A/D converters: D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable signal output by the 12-bit A/D converter (unit 2). This reduces degradation of A/D conversion accuracy due to interference by controlling the timing of the 12-bit D/A converter inrush current with the enable signal.	• Measure against interference between D/A and A/D converters: D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable signal output by the 12-bit A/D converter. This reduces degradation of A/D conversion accuracy due to interference by controlling the timing of the 12-bit /A converter inrush current with the enable signal.
Low power consumption function	Transition to the module stop state is possible.	Transition to the module stop state is possible.
Event link function (input)	Ability to start D/A conversion on channel 0 when an event signal is input	Ability to start D/A conversion on channel 0 when an event signal is input
Output destination selection	Output to external pins and to comparator C can be controlled independently.	Output to external pins and to comparator C can be controlled independently.

2.23 Temperature Sensor

Table 2.69 is Comparative Overview of Temperature Sensors.

Table 2.69 Comparative Overview of Temperature Sensors

Item	RX66T (TEMPS)	RX660 (TEMPS)
Temperature sensor voltage output	The temperature sensor outputs a voltage to the 12-bit A/D converter (unit 2).	The temperature sensor outputs a voltage to the 12-bit A/D converter (unit 0).
Temperature sensor calibration data	Reference data measured for each chip at the time of shipment from the factory is stored in a register.	Reference data measured for each chip at the time of shipment from the factory is stored in a register.

2.24 Comparator C

Table 2.70 is Comparative Overview of Comparator C, and Table 2.71 is Comparison of Comparator C Registers.

Table 2.70 Comparative Overview of Comparator C

Item	RX66T (CMPC)	RX660 (CMPC)
Number of channels	6 channels (comparator C0 to comparator C5)	4 channels (comparator C0 to comparator C3)
Analog input voltage	Input voltage on CMPCnm pin (n = channel number, m = 0 to 3)	Input voltage on CMPCn0 pin (n = channel number)
Reference input voltage	Input voltage on CVREFC0 or CVREFC1 pin, output voltage of on-chip D/A converter 0, or output voltage of on-chip D/A converter 1	Input voltage on CVREFC0 to CVREFC3 pins or output voltage of on-chip D/A converter 0 or on-chip D/A converter 1
Comparison result	The comparison result can be output externally.	The comparison result can be output externally.
Digital filter function	• One of three sampling periods can be selected. • The filter function can also be disabled. • A noise-filtered signal can be used to generate interrupt request output, event output to the ELC, and POE cause output, and comparison results can be read from registers.	• One of three sampling periods can be selected. • The filter function can also be disabled. • A noise-filtered signal can be used to generate interrupt request output and event output to the ELC, and comparison results can be read from registers.
Interrupt request signal	• An interrupt request is generated upon detection of a valid edge of the comparison result. • The rising edge, falling edge, or both edges of the comparison result can be selected as valid edges.	• An interrupt request is generated upon detection of a valid edge of the comparison result. • The rising edge, falling edge, or both edges of the comparison result can be selected as valid edges.
Low power consumption function	Transition to the module stop state is possible.	Transition to the module stop state is possible.

Table 2.71 Comparison of Comparator C Registers

Register	Bit	RX66T (CMPC)	RX660 (CMPC)
CMPSEL0	CMPSEL[3:0]	Comparator input select register • For Comparator C b3 b0 0 0 0 0: No input 0 0 0 1: CMPC00 is selected. 0 0 1 0: CMPC01 is selected. 0 1 0 0: CMPC02 is selected. 1 0 0 0: CMPC03 is selected. Settings other than the above are prohibited. • For Comparator C1 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC10 is selected. 0 0 1 0: CMPC11 is selected. 0 1 0 0: CMPC12 is selected. 1 0 0 0: CMPC13 is selected. Settings other than the above are prohibited. • For Comparator C2 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC20 is selected. 0 0 1 0: CMPC21 is selected. 0 1 0 0: CMPC22 is selected. 1 0 0 0: CMPC23 is selected. Settings other than the above are prohibited. • For Comparator C3 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC30 is selected. 0 0 1 0: CMPC31 is selected. 0 1 0 0: CMPC32 is selected. 1 0 0 0: CMPC33 is selected. Settings other than the above are prohibited.	Comparator input select register • For Comparator C b3 b0 0 0 0 0: No input 0 0 0 1: CMPC00 is selected. Settings other than the above are prohibited. • For Comparator C1 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC10 is selected. Settings other than the above are prohibited. • For Comparator C2 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC20 is selected. Settings other than the above are prohibited. • For Comparator C3 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC30 is selected. Settings other than the above are prohibited.

Register	Bit	RX66T (CMPC)	RX660 (CMPC)
CMPSEL0	CMPSEL[3:0]	• For Comparator C4 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC40 is selected. 0 0 1 0: CMPC41 is selected. 0 1 0 0: CMPC42 is selected. 1 0 0 0: CMPC43 is selected. Settings other than the above are prohibited.	
	—	• For Comparator C5 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC50 is selected. 0 0 1 0: CMPC51 is selected. 0 1 0 0: CMPC52 is selected. 1 0 0 0: CMPC53 is selected. Settings other than the above are prohibited.	—
CMPSEL1	CVRS[3:0]	Reference input voltage select bits b3 b0 0 0 0 0: No input 0 0 0 1: Output of on-chip D/A converter 1 is selected for the reference input voltage. 0 0 1 0: Output of on-chip D/A converter 0 is selected for the reference input voltage. 0 1 0 0: CVREFC1 input is selected for the reference input voltage. 1 0 0 0: CVREFC0 input is selected for the reference input voltage. Settings other than the above are prohibited.	Reference input voltage select bits b3 b0 0 0 0 0: No input 0 0 0 1: Output of on-chip D/A converter 1 is selected for the reference input voltage. 0 0 1 0: Output of on-chip D/A converter 0 is selected for the reference input voltage. 1 0 0 0: CVREFCn input (n = 0 to 3) is selected for the reference input voltage. Settings other than the above are prohibited.

2.25 Data Operation Circuit

Table 2.72 is Comparative Overview of Data Operation Circuits, and Table 2.73 is Comparison of Data Operation Circuit Registers.

Table 2.72 Comparative Overview of Data Operation Circuits

Item	RX66T (DOC)	RX660 (DOCA)
Data operation functions	• 16-bit data comparison, addition, and subtraction	• Comparison of 16- or 32-bit data (match/mismatch, greater/less, in/out of range) • Addition or subtraction of 16- or 32 bit data
Low power consumption function	Transition to the module stop state is possible.	Transition to the module stop state is possible.
Interrupts	• The compared values either match or mismatch • The result of data addition is greater than FFFFh (overflow). • The result of data subtraction is less than 0000h (underflow).	• When data comparison result matches detection condition • When data addition result is greater than FFFFh (when DOCR.DOPSZ = 0) or FFFF FFFFh (when DOCR.DOPSZ = 1) (overflow) • When data subtraction result is less than 0000h (when DOCR.DOPSZ = 0) or 0000 0000h (when DOCR.DOPSZ = 1) (underflow)
Event link function (output)	• The compared values either match or mismatch. • The result of data addition is greater than FFFFh (overflow). • The result of data subtraction is less than 0000h (underflow).	• When data comparison result matches detection condition • When data addition result is greater than FFFFh (when DOCR.DOPSZ = 0) or FFFF FFFFh (when DOCR.DOPSZ = 1) (overflow) • When data subtraction result is less than 0000h (when DOCR.DOPSZ = 0) or 0000 0000h (when DOCR.DOPSZ = 1) (underflow)

Table 2.73 Comparison of Data Operation Circuit Registers

Register	Bit	RX66T (DOC)	RX660 (DOCA)
DOCR	DOPSZ	—	Data operation size select bit
	DCSEL (RX66T) DCSEL[2:0] (RX660)	Detection condition select bit 0: Data mismatches are detected. 1: Data matches are detected.	Detection condition select bits b6 b4 0 0 0: Mismatch (DODIR ≠ DODSR0) 0 0 1: Match (DODIR = DODSR0) 0 1 0: Less (DODIR < DODSR0) 0 1 1: Greater (DODIR > DODSR0) 1 0 0: In range (DODSR0 < DODIR < DODSR1) 1 0 1: Out of range (DODIR < DODSR0, DODSR1 < DODIR) Other than above: Setting prohibited.
	DOPCF	Data operation circuit flag	—
	DOPCFCL	DOPCF clear bit	—
DOSR	—	—	DOC status register
DOSCR	—	—	DOC status clear register
DODIR	—	DOC data input register	DOC data input register
		16-bit readable/writable register.	32-bit readable/writable register.
DODSR (RX66T) DODSR0/ DODSR1 (RX660)	—	DOC data setting register	DOC data setting registers 0 DOC data setting registers 1
		16-bit readable/writable register.	32-bit readable/writable register.

2.26 RAM

Table 2.74 is Comparative Overview of RAM.

Table 2.74 Comparative Overview of RAM

Item	RX66T		RX660
	Without ECC (Error Checking and Correcting feature) (RAM)	**With ECC (Error Checking and Correcting feature) (ECCRAM)**	—
RAM capacity	64 KB 128 KB	16 KB	128 KB
RAM address	For RAM capacity 48 KB 0000 0000h to 0000 FFFFh For RAM capacity 128 KB 0000 0000h to 0001 FFFFh	00FF C000h to 00FF FFFFh	• RAM:0000 0000h to 0001 FFFFh
Memory buses	Memory bus 1	Memory bus 3	Memory bus 1
Access	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.	• The ECC feature can be enabled or disabled. [When MEMWAIT is set to 0] • If the ECC feature is disabled: Two-cycle access is possible for both reading and writing. • If the ECC feature is enabled (no error): Two-cycle access is possible for both reading and writing. • If the ECC feature is enabled (an error occurred): Three-cycle access is possible for both reading and writing. [When MEMWAIT is set to 1] If the ECC feature is disabled: Three-cycle access is possible for both reading and writing. • If the ECC feature is enabled (no error): Three-cycle access is possible for reading and four-cycle access is possible for writing. • If the ECC feature is enabled (an error occurred): Five-cycle access is possible for both reading and writing.	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.

Item	RX66T		RX660
	Without ECC (Error Checking and Correcting feature) (RAM)	**With ECC (Error Checking and Correcting feature) (ECCRAM)**	—
Data retention function	Not available in deep software standby mode		Not available in deep software standby mode
Low power consumption function	RAM and ECCRAM can individually transfer to the module stop state.		Transition to the module stop state is possible.
Error checking	• Detection of 1-bit errors • A non-maskable interrupt or an interrupt is generated when an error occurs.	• ECC (Error Checking and Correcting feature) Correction of 1-bit errors and detection of 2-bit errors • A non-maskable interrupt or an interrupt is generated when an error occurs.	• Parity check: Detection of 1-bit errors • A non-maskable interrupt or an interrupt is generated when an error occurs.

2.27 Flash Memory

Table 2.75 is Comparative Overview of Flash Memory, and Table 2.76 is Comparison of Flash Memory Registers.

Table 2.75 Comparative Overview of Flash Memory

Item	RX66T		RX660	
	Code Flash Memory	**Data Flash Memory**	**Code Flash Memory**	**Data Flash Memory**
Memory capacity	• User area: Up to 1 MB • User boot area: 32 KB	• Data area: 32 KB	• User area: Up to 1 MB • User boot area: 32 KB	• Data area: 32 KB
ROM cache	• Capacity: 8 KB • Mapping method: Direct map • Line size: 16 bytes	—	—	
Read cycles	• When ROM cache operation is enabled: One cycle in response to a cache hit If a cache miss occurs, one or two cycles if ICLK is equal to or smaller than 120 MHz, and two or three cycles if ICLK is larger than 120 MHz • When ROM cache operation is prohibited: One cycle if ICLK is equal to or smaller than 120 MHz Two cycles if ICLK is larger than 120 MHz	16-bit or 8-bit read access requires 8 FCLK clock cycles.	One cycle	16-bit or 8-bit read access requires 8 FCLK clock cycles.
Value after erasure	FFh	Undefined	FFh	Undefined
Programming/ erasing method	• FACI commands specified in the FACI command issuing area (007E 0000h) can be used to program and erase the code flash memory and data flash memory. • A flash memory programmer can be used to program and erase the flash memory via a serial interface (serial programming). • A user program can be used to program and erase the flash memory (self-programming).		• FACI commands specified in the FACI command issuing area (007E 0000h) can be used to program and erase the code flash memory and data flash memory. • A flash memory programmer can be used to program and erase the flash memory via a serial interface (serial programming). • A user program can be used to program and erase the flash memory (self-programming).	
Security function	Protects against illicit tampering with or reading of data in flash memory.		Protects against illicit tampering with or reading of data in flash memory.	

Item	RX66T		RX660	
	Code Flash Memory	Data Flash Memory	Code Flash Memory	Data Flash Memory
Trusted Memory (TM) function	Protects against illicit reading of blocks 8 and 9 in the code flash memory.		Protects against illicit reading of blocks 8 and 9 in the code flash memory.	
Units of programming and erasure	Programming the user area and user boot area: 256 bytes Erasure of user area: Block units	Programming the data area: 4 bytes Erasure of data area: Block units	Programming the user area and user boot area: 256 bytes Erasure of user area: Block units	Programming the data area: 4 bytes Erasure of data area: Block units
Other functions	Interrupts can be accepted during self-programming.		Interrupts can be accepted during self-programming.	
On-board programming (serial programming and self-programming)	• Programming/erasure in boot mode (SCI interface) — The asynchronous serial interface (SCI1) is used. — The communication speed is adjusted automatically. — Programming and erasure of the user boot area is also possible. • Programming/erasure in boot mode (USB interface) — USB0 is used. — PC can be directly connected. No special hardware is needed. • Programming/erasure in boot mode (FINE interface) — FINE is used. • Programming/erasure in user boot mode — A user-specific boot program can be created. • Programming/erasure in single-chip mode — Programming or erasure by a routine within a user program for writing to the code flash memory or data flash memory is possible.		• Programming/erasure in boot mode (SCI interface) — The asynchronous serial interface (SCI1) is used. — The communication speed is adjusted automatically. — Programming and erasure of the user boot area is also possible. • Programming/erasure in boot mode (FINE interface) — FINE is used. • Programming/erasure in user boot mode — A user-specific boot program can be created. • Programming/erasure in single-chip mode — Programming or erasure by a routine within a user program for writing to the code flash memory or data flash memory is possible.	
Off-board programming (programming and erasure using a parallel programmer)	Programming or erasure of the user area or user boot area by using a parallel programmer is possible.	Programming or erasure of the data area using a parallel programmer is not possible.	Programming or erasure of the user area or user boot area by using a parallel programmer is possible.	Programming or erasure of the data area using a parallel programmer is not possible.
Protection function	Protects against erroneous programming of the flash memory.		Protects against erroneous programming of the flash memory.	
Background operation (BGO) function	The user area can be read while the data area is being programmed or erased.		The user area can be read while the data area is being programmed or erased.	
Unique ID	A unique 12-byte ID code is provided for each MCU.		A unique 12-byte ID code is provided for each MCU.	

Table 2.76 Comparison of Flash Memory Registers

Register	Bit	RX66T	RX660 (FLASH)
ROMCE	—	ROM cache enable register	—
ROMCIV	—	ROM cache disable register	—
NCRGn	—	Non-cacheable area n address register	—
NCRCn	—	Non-cacheable area n configuration register	

2.28 Packages

As indicated in Table 2.77, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage.

Table 2.77 Packages

Package Type	RENESAS Code	
	RX66T	RX660
112-pin LFQFP	○	×
80-pin LQFP	PLQP0080JA-B	PLQP0080KB-B
80-pin LFQFP	PLQP0080KB-B	PLQP0064KB-C

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by **blue text**. Items that exists on both groups with different specifications are indicated by **red text**. **Black text** indicates there is no differences in the item's specifications between groups.

3.1 144-Pin Package

Table 3.1 is Comparative Listing of 144-Pin Package Pin Functions.

Table 3.1 Comparative Listing of 144-Pin Package Pin Functions

144-Pin LFQFP	RX66T	RX660
1	P14/MTIOC4B/ MTIOC4B#/GTIOC2A/GTIOC9A/GTIOC2A#/ GTIOC9A#/IRQ11	AVSS0
2	P13/MTIOC4A/ MTIOC4A#/GTIOC1A/GTIOC8A/GTIOC1A#/ GTIOC8A#/IRQ10	P05/IRQ13/DA1
3	P12/MTIOC3B/ MTIOC3B#/GTIOC0A/GTIOC7A/GTIOC0A#/ GTIOC7A#/IRQ9	P06
4	PE6/RD#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE10#/ IRQ3	P03/IRQ11/DA0
5	PE5/BCLK/MTIOC9D/MTIOC9D#/ GTIOC3A/GTETRGB/GTIOC3A#/ GTETRGD/SCK9/CTS9#/RTS9#/SS9#/ IRQ0/ADST0	P04
6	VCC	P02/TMCI1/SCK6/IRQ10
7	EMLE	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9
8	VSS	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8
9	UB/P00/A11/MTIOC9A/ MTIOC9A#/ CACREF/RXD9/SMISO9/SSCL9/RXD12/ SMISO12/SSCL12/RXDX12/ IRQ2/ADST1/COMP0	PF5/IRQ4
10	VCL	EMLE(Note 1)/PN7(Note 2)
11	MD/FINED	PJ5/POE8#/CTS2#/RTS2#/SS2#/IRQ13
12	P01/A10/MTIOC9C/MTIOC9C#/ GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE12#/TXD9/SMOSI9/SSDA9/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ IRQ4/ADST2/COMP1	PJ4
13	PE4/A9/MTCLKC/MTCLKC#/ GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE10#/SCK9/IRQ1	PJ3/MTIOC3C/CTS6#/RTS6#/SS6#/ CTS0#/RTS0#/SS0#/IRQ11
14	PE3/A8/MTCLKD/ MTCLKD#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE11#/CTS9#/ RTS9#/SS9#/IRQ2-DS	VCL
15	RES#	PJ1/MTIOC3A
16	XTAL/P37	MD/FINED/PN6

144-Pin LFQFP	RX66T	RX660
17	VSS	XCIN(Note 3)/PH7(Note 4)
18	EXTAL/P36	XCOUT(Note 3)/PH6(Note 4)
19	VCC	RES#
20	UPSEL/PE2/POE10#/NMI	XTAL/P37/IRQ4
21	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/ TMO5/CTS5#/RTS5#/SS5#/CTS12#/ RTS12#/SS12#/SSLA3/IRQ15	VSS
22	PE0/WR1#/BC1#/WAIT#/MTIOC9B/ MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/ SSCL5/SSLA2/CRX0/ USB0_OV RCURB/IRQ7	EXTAL/P36/IRQ5
23	TRST#/PD7/MTIOC9A/ MTIOC9A#/GTIOC0A/GTIOC3A/GTIOC0A#/ GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/ SSDA5/SSLA1/CTX0/IRQ8	VCC
24	TMS/PD6/MTIOC9C/MTIOC9C#/ GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/ TMO1/CTS1#/RTS1#/SS1#/CTS11#/ RTS11#/SS11#/SSLA0/IRQ5/ADST0	P35/NMI
25	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6	TRST#(Note 1)/P34/MTIOC0A/TMCI3/ POE10#/SCK6/SCK0/IRQ4
26	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/ TMCI0/TMCI6/SCK1/SCK11/IRQ2	P33/MTIOC0D/TMRI3/ POE4#/POE11#/RXD6/SMISO6/SSCL6/ RXD0/SMISO0/SSCL0/CRX0-A/IRQ3-DS
27	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11	P32/MTIOC0C/TMO3/RTCIC2(Note 5)/ RTCOUT(Note 5)/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0-A/IRQ2-DS
28	TRCLK/PD2/A7/GTIOC2B/ GTIOC0A/GTIOC2B#/GTIOC0A#/TMCI1/ TMO4/SCK5/SCK8/ MOSIA/USB0_VB US	TMS(Note 1)/P31/MTIOC4D/TMCI2/ RTCIC1(Note 5)/CTS1#/RTS1#/SS1#/IRQ1-DS
29	TRDATA3/PD1/A6/GTIOC3A/GTIOC0B/ GTIOC3A#/GTIOC0B#/TMO2/RXD8/ SMISO8/ SSCL8/MISOA	TDI(Note 1)/P30/MTIOC4B/TMRI3/RTCIC0(Note 5)/ POE8#/RXD1/SMISO1/ SSCL1/IRQ0-DS/ COMP3
30	TRDATA2/PD0/A5/GTIOC3B/ GTIOC1A/GTIOC3B#/GTIOC1A#/TMO6/ TXD8/SMOSI8/ SSDA8/RSPCKA	TCK(Note 1)/P27/CS3#/MTIOC2B/TMCI3/ SCK1/IRQ7/CVREFC3
31	TRDATA7/PF3/A19/CS3#/GTETRGA/ TMO7/CTS11#/RTS11#/ SS11#/CRX0/IRQ14/COMP0	TDO(Note 1)/P26/CS2#/MTIOC2A/TMO1/ TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/ IRQ6/CMPC30
32	TRDATA6/PF2/A18/CS2#/GTETRGB/ TMO3/SCK11/CTX0/IRQ5/COMP1	P25/CS1#/MTIOC4C/MTCLKB/RXD3/ SMISO3/ SSCL3/IRQ5/ADTRG0#
33	TRDATA5/PF1/A17/CS1#/GTETRGC/TMO5/ RXD11/SMISO11/SSCL11/ IRQ13/COMP2	P24/CS0#/MTIOC4A/MTCLKA/ TMRI1/SCK3/IRQ12
34	TRDATA4/PF0/A0/BC0#/GTETRGD/ TMO1/TXD11/SMOSI11/SSDA11/ IRQ12/COMP3	P23/MTIOC3D/MTCLKD/TXD3/ SMOSI3/SSDA3/CTS0#/RTS0#/SS0#/IRQ3
35	USB0_DM	P22/MTIOC3B/MTCLKC/TMO0/ SCK0/IRQ15

144-Pin LFQFP	RX66T	RX660
36	USB0_DP	P21/MTIOC1B/TMCI0/ MTIOC4A/RXD0/SMISO0/ SSCL0/IRQ9
37	VSS_USB	P20/MTIOC1A/TMRI0/TXD0/SMOSI0/ SSDA0/IRQ8
38	VCC_USB	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ MTIOC4B/SCK1/TXD3/SMOSI3/SSDA3/ MISOA-C/SDA2/IRQ7/COMP2
39	TRDATA1/PB7/A4/GTIOC1B/GTIOC1B#/ SCK5/SCK11/ SCK12/USB0_OV RCURB	P87/MTIOC4C/SMOSI10/SSDA10/ TXD10/TXD010-B/SMOSI010-B/ SSDA010-B/IRQ15
40	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/ RXD5/SMISO5/SSCL5/ RXD11/SMISO11/SSCL11/RXD12/ SMISO12/SSCL12/RXDX12/ CRX0/USB0_OV RCURA/IRQ2	P16/MTIOC3C/MTIOC3D/TMO2/ RTCOUT/TXD1/SMOSI1/SSDA1/RXD3/ SMISO3/SSCL3/MOSIA-C/SCL2/ IRQ6/ADTRG0#
41	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/ TXD5/SMOSI5/SSDA5/TXD11/ SMOSI11/SSDA11/TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/ CTX0/USB0_VB USEN	P86/MTIOC4D/SMISO10/SSCL10/RXD10/ RXD010-B/SMISO010-B/SSCL010-B/IRQ14
42	VCC	P15/MTIOC0B/MTCLKB/ TMCI2/RXD1/SMISO1/SSCL1/SCK3/ CRX0-C/IRQ5/CMPC20
43	TRSYNC1/PB4/A1/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE8#/ CTS5#/RTS5#/SS5#/SCK11/CTS11#/ RTS11#/SS11#/USB0_OV RCURB/IRQ3-DS	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/CTX0-C/IRQ4/CVREFC2
44	VSS	P13/MTIOC0B/TMO3/TXD2/SMOSI2/ SSDA2/SDA0/IRQ3
45	PC2/CS1#/MTIOC0D/MTIOC0D#/ GTADSM0/SCK8/USB0_ID/ USB0_OVRCURA/IRQ15/ADSM0/ COMP5	P12/MTIC5U/TMCI1/RXD2/SMISO2/ SSCL2/SCL0/IRQ2
46	PC1/A16/MTIOC0C/MTIOC0C#/ GTADSM1/TXD8/SMOSI8/SSDA8/ USB0_EXICEN/USB0_VBUSEN/ IRQ13/ADSM1/ COMP4	PH3/MTIOC4D/TMCI0
47	PC0/CS0#/MTIOC0B/MTIOC0B#/ RXD8/SMISO8/SSCL8/USB0_VBUS/ IRQ12/COMP3	PH2/MTIOC4C/TMRI0/TOC1/IRQ1
48	PB3/A7/MTIOC0A/ MTIOC0A#/CACREF/SCK6/RSPCKA/IRQ9	PH1/MTIOC3D/TMO0/TIC1/IRQ0/ADST0
49	PB2/A6/MTIOC0B/MTIOC0B#/ GTADSM0/TMRI0/TXD6/SMOSI6/ SSDA6/SDA0/ADSM0	PH0/MTIOC3B/CACREF/ADTRG0#
50	PB1/A5/MTIOC0C/MTIOC0C#/ GTADSM1/TMCI0/RXD6/SMISO6/ SSCL6/SCL0/IRQ4/ADSM1	P56/MTIOC3C/SCK7/IRQ6
51	PB0/A0/BC0#/A4/MTIOC0D/MTIOC0D#/ TMO0/TXD6/SMOSI6/SSDA6/ CTS11#/RTS11#/SS11#/MOSIA/ IRQ8/ADTRG2#	TRDATA3(Note 1)/P55/D0[A0/D0]/WAIT#/ MTIOC4D/MTIOC4A/TMO3/TXD7/ SMOSI7/SSDA7/CRX0-D/IRQ10

144-Pin LFQFP	RX66T	RX660
52	PA7/A15/MTCLKA/MTCLKC/MTCLKA#/ MTCLKC#/GTADSM0/TMO2/RXD11/ SMISO11/SSCL11/RXD12/SMISO12/ SSCL12/RXDX12/CRX0/ADSM0	TRDATA2(Note 1)/P54/ALE/D1[A1/D1]/ MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/ CTX0-D/IRQ4
53	PA6/A14/MTCLKB/MTCLKD/ MTCLKB#/MTCLKD#/GTADSM1/TMO6/ TXD11/SMOSI11/SSDA11/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ CTX0/IRQ7/ADSM1	P53/BCLK/PMC0/IRQ3
54	PA5/A3/MTIOC1A/MTIOC1A#/TMCI3/ RXD6/SMISO6/SSCL6/RXD8/SMISO8/ SSCL8/MISOA/IRQ1/ADTRG1#	P52/RD#/RXD2/SMISO2/SSCL2/IRQ2
55	PA4/A2/MTIOC1B/MTIOC1B#/TMCI7/ SCK6/TXD8/SMOSI8/SSDA8/RSPCKA/ ADTRG0#	P51/WR1#/BC1#/ WAIT#/SCK2/PMC0/IRQ1
56	PA3/A1/MTIOC2A/ MTIOC2A#/ GTADSM0/TMRI7/TXD9/SMOSI9/SSDA9/ SCK8/SSLA0	P50/WR0#/WR#/TXD2/SMOSI2/ SSDA2/IRQ0
57	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/ GTADSM1/TMO7/CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/ SCK11/SSLA1	VSS
58	PA1/MTIOC6A/MTIOC6A#/ TMO4/TXD9/SMOSI9/SSDA9/RXD11/ SMISO11/SSCL11/SSLA2/CRX0/USB0_ID/ USB0_OV RCURA/IRQ14-DS/ADTRG0#	TRCLK(Note 1)/P83/MTIOC4C/SCK10/SS10#/ CTS10#/SCK010-B/CTS010#-A/ SS010#-A/IRQ3
59	PA0/MTIOC6C/MTIOC6C#/TMO2/ SCK9/TXD11/SMOSI11/SSDA11/SSLA3/ CTX0/USB0_EXICEN/USB0_VBUSEN	VCC
60	P35/A13/MTIOC2A/MTIOC9A/ MTIOC2A#/MTIOC9A#/GTADSM0/TMO0/ CTS8#/RTS8#/SS8#/TXD1/ SMOSI1/SSDA1/IRQ6	UB/PC7/CS0#/MTIOC3A/MTCLKB/ TMO2/CACREF/TOC0/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/TXD10/ TXD010-C/SMOSI010-C/ SSDA010-C/MISOA-A/IRQ14
61	P34/A12/MTIOC2B/MTIOC9B/MTIOC2B#/ MTIOC9B#/GTADSM1/GTETRGB/ TMO4/CTS9#/RTS9#/SS9#/RXD1/SMISO1/ SSCL1/USB0_OV RCURB/IRQ3	PC6/D2[A2/D2]/CS1#/MTIOC3C/ MTCLKA/TMCI2/TIC0/RXD8/SMISO8/ SSCL8/SMISO10/SSCL10/RXD10/ RXD010-C/SMISO010-C/SSCL010-C/ MOSIA-A/IRQ13
62	PC6/MTIOC1A/MTIOC9C/MTIOC1A#/ MTIOC9C#/RXD11/SMISO11/ SSCL11/CRX0/IRQ11-DS	PC5/D3[A3/D3]/CS2#/WAIT#/ MTIOC3B/MTCLKD/TMRI2/MTIOC0C/SCK8/ SCK10/SCK010-C/RSPCKA-A/PMC0/IRQ5
63	PC5/MTIOC1B/MTIOC9D/MTIOC1B#/ MTIOC9D#/TXD11/SMOSI11/ SSDA11/CTX0/IRQ10-DS	TRSYNC(Note 1)/P82/MTIOC4A/ SMOSI10/SSDA10/TXD10/TXD010-A/ SMOSI010-A/SSDA010-A/IRQ2
64	VCC	TRDATA1(Note 1)/P81/MTIOC3D/SMISO10/ SSCL10/RXD10/RXD010-A/SMISO010-A/ SSCL010-A/IRQ9
65	P96/CS0#/WAIT#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE4#/CTS8#/ RTS8#/SS8#/IRQ4-DS	TRDATA0(Note 1)/P80/MTIOC3B/SCK10/ RTS10#/SCK010-A/RTS010#-A/ DE010-A/IRQ8

144-Pin LFQFP	RX66T	RX660
66	VSS	PC4/A20/CS3#/MTIOC3D/MTCLKC/ TMCI1/POE0#/MTIOC0A/SCK5/CTS8#/ RTS8#/SS8#/SS10#/CTS10#/RTS10#/ CTS010#-B/RTS010#-B/SS010#-B/ DE010-B/SSLA0-A/PMC0/IRQ12
67	P95/MTIOC6B/MTIOC6B#/ GTIOC4A/GTIOC7A/GTIOC4A#/GTIOC7A#	PC3/A19/MTIOC4D/TXD5/SMOSI5/ SSDA5/PMC0/IRQ11
68	P94/MTIOC7A/MTIOC7A#/ GTIOC5A/GTIOC8A/GTIOC5A#/GTIOC8A#	TRDATA7(Note 1)/P77/SMOSI11/SSDA11/ TXD11/TXD011-A/SMOSI011-A/ SSDA011-A/IRQ7
69	P93/MTIOC7B/MTIOC7B#/ GTIOC6A/GTIOC9A/GTIOC6A#/GTIOC9A#	TRDATA6(Note 1)/P76/SMISO11/SSCL11/ RXD11/RXD011-A/SMISO011-A/ SSCL011-A/IRQ14
70	P92/MTIOC6D/MTIOC6D#/ GTIOC4B/GTIOC7B/GTIOC4B#/GTIOC7B#	PC2/A18/MTIOC4B/RXD5/SMISO5/ SSCL5/TXDB011-A/SSLA3-A/IRQ10
71	P91/MTIOC7C/MTIOC7C#/ GTIOC5B/GTIOC8B/GTIOC5B#/GTIOC8B#	TRSYNC1(Note 1)/P75/SCK11/RTS11#/ SCK011-A/RTS011#-A/DE011-A/IRQ13
72	P90/MTIOC7D/MTIOC7D#/ GTIOC6B/GTIOC9B/GTIOC6B#/GTIOC9B#	TRDATA5(Note 1)/P74/A20/SS11#/CTS11#/ CTS011#-A/SS011#-A/IRQ12
73	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#	PC1/A17/MTIOC3A/SCK5/ TXD011-C/SMOSI011-C/SSDA011-C/ TXDA011-C/SSLA2-A/IRQ12
74	P75/D1[A1/D1]/MTIOC4C/ MTIOC4C#/GTIOC1B/GTIOC5B/GTIOC1B#/ GTIOC5B#	PL1
75	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#	PC0/A16/MTIOC3C/CTS5#/RTS5#/ SS5#/RXD011-C/SMISO011-C/ SSCL011-C/SSLA1-A/IRQ14
76	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#	PL0
77	P72/D4[A4/D4]/MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#	TRDATA4(Note 1)/P73/CS3#/IRQ8
78	P71/D5[A5/D5]/MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#	PB7/A15/MTIOC3B/TXD9/SMOSI9/SSDA9/ SMOSI11/SSDA11/TXD11/TXD011-B/ SMOSI011-B/SSDA011-B/IRQ15
79	P70/D6[A6/D6]/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE0#/ CTS9#/RTS9#/SS9#/IRQ5-DS	PB6/A14/MTIOC3D/RXD9/SMISO9/SSCL9/ SMISO11/SSCL11/RXD11/RXD011-B/ SMISO011-B/SSCL011-B/IRQ6
80	PG2/D11[A11/D11]/GTETRGA/GTIOC0B/ GTIOC0B#/SCK9/IRQ2/COMP0	PB5/A13/MTIOC2A/MTIOC1B/ TMRI1/POE4#/TOC2/SCK9/SCK11/ SCK011-B/IRQ13
81	PG1/D12[A12/ D12]/GTIOC0A/GTIOC0A#/ TXD9/SMOSI9/SSDA9/IRQ1/COMP1	PB4/A12/CTS9#/RTS9#/SS9#/SS11#/ CTS11#/RTS11#/CTS011#-B/ RTS011#-B/SS011#-B/DE011-B/IRQ4
82	PG0/D13[A13/D13]/GTIOC1B/GTIOC1B#/ RXD9/SMISO9/SSCL9/IRQ0/COMP2	PB3/A11/MTIOC0A/MTIOC4A/ TMO0/POE11#/TIC2/SCK4/SCK6/ PMC0/IRQ3
83	PK2/D14[A14/D14]/GTIOC1A/GTIOC1A#/ POE12#/CTS9#/RTS9#/ SS9#/SCK5/ IRQ9-DS/COMP3	PB2/A10/CTS4#/RTS4#/SS4#/ CTS6#/RTS6#/SS6#/IRQ2

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84	PK1/D15[A15/D15]/GTIOC2B/GTIOC2B#/ POE13#/CTS8#/RTS8#/SS8#/TXD5/ SMOSI5/SSDA5/IRQ8-DS/COMP4	PB1/A9/MTIOC0C/MTIOC4C/ TMCI0/TXD4/SMOSI4/SSDA4/TXD6/ SMOSI6/SSDA6/IRQ4-DS/COMP1
85	PK0/CS1#/GTIOC2A/GTIOC2A#/ POE14#/RXD5/SMISO5/ SSCL5/ IRQ15-DS/COMP5	P72/A19/CS2#/IRQ10
86	P33/D7[A7/D7]/MTIOC3A/ MTCLKA/MTIOC3A#/MTCLKA#/GTIOC3B/ GTIOC3B#/TMO0/SSLA3/IRQ13-DS	P71/A18/CS1#/IRQ1
87	P32/D8[A8/D8]/MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/GTIOC3A/ GTIOC3A#/TMO6/SSLA2/IRQ12-DS	PB0/A8/MTIC5W/MTIOC3D/RXD4/ SMISO4/SSCL4/RXD6/SMISO6/SSCL6/ RSPCKA-C/IRQ12
88	VCC	PA7/A7/MISOA-B/IRQ7
89	P31/D9[A9/D9]/MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6	PA6/A6/MTIC5V/MTCLKB/TMCI3/ POE10#/MTIOC3D/MTIOC6B/CTS5#/ RTS5#/SS5#/CTS12#/RTS12#/SS12#/ MOSIA-B/IRQ14
90	VSS	PA5/A5/MTIOC6B/RSPCKA-B/IRQ5
91	P30/D10[A10/D10]/MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/TMCI6/SCK8/CTS8#/ RTS8#/SS8#/SSLA0/IRQ7/COMP3	VCC
92	P27/CS3#/MTIOC1A/MTIOC0C/ MTIOC1A#/MTIOC0C#/POE9#/IRQ15	PA4/A4/MTIC5U/MTCLKA/TMRI0/ MTIOC4C/MTIOC7C/TXD5/SMOSI5/SSDA5/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ SSLA0-B/IRQ5-DS/CVREFC1/ADST0
93	P26/CS2#/MTIOC9A/MTIOC9A#/ CTS1#/RTS1#/ SS1#/IRQ11/ADST0	VSS
94	P25/CS3#/MTIOC9C/MTIOC9C#/ SCK1/IRQ10/ADST1	PA3/A3/MTIOC0D/MTCLKD/ MTIC5V/MTIOC4D/RXD5/SMISO5/SSCL5/ IRQ6-DS/CMPC10
95	P24/D11[A11/D11]/MTIC5U/MTIC5U#/ TMCI2/TMO6/CTS8#/RTS8#/SS8#/SCK8/ RSPCKA/IRQ4/COMP0	PA2/A2/MTIOC7A/RXD5/SMISO5/ SSCL5/RXD12/SMISO12/SSCL12/RXDX12/ SSLA3-B/IRQ10
96	P23/D12[A12/D12]/MTIC5V/MTIC5V#/ TMO2/CACREF/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ MOSIA/CTX0/IRQ11/COMP1	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ MTIOC3B/SCK5/SCK12/SSLA2-B/ IRQ11/ADTRG0#
97	P22/D13[A13/D13]/MTIC5W/MTCLKD /MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/ TMO4/RXD8/SMISO8/SSCL8/RXD12/ SMISO12/SSCL12/RXDX12/MISOA/CRX0/ IRQ10/ADTRG2#/COMP2	PA0/BC0#/A0/MTIOC4A/CACREF/ MTIOC6D/SSLA1-B/IRQ0
98	PC4/A20/MTIOC9B/MTIOC9B#/TXD1/ SMOSI1/SSDA1/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/ADST2/COMP5	P67/MTIOC7C/IRQ15
99	PC3/MTIOC9D/MTIOC9D#/ RXD1/SMISO1/SSCL1/RXD12/SMISO12/ SSCL12/RXDX12/IRQ14/COMP4	P66/MTIOC7D/IRQ14

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100	P21/D14[A14/D14]/MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/TMCI4/TXD8/ SMOSI8/SSDA8/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/MOSIA/IRQ6-DS/ AN217/ADTRG1#/COMP5	P65/IRQ13
101	P20/D15[A15/D15]/MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/TMRI4/ CTS8#/RTS8#/SS8#/SCK8/RSPCKA/ IRQ7-DS/AN216/ADTRG0#/COMP4	PE7/D15[A15/D15]/ D7[A7/D7]/MTIOC6A/TOC1/IRQ7/AN015
102	P65/A12/IRQ9/AN211/CMPC53/DA1	PE6/D14[A14/D14]/ D6[A6/D6]/MTIOC6C/TIC1/CTS4#/RTS4#/ SS4#/IRQ6/AN014
103	P64/A13/IRQ8/AN210/CMPC33/DA0	PK5/TXD4/SMOSI4/ SSDA4
104	AVCC2	P70/SCK4/IRQ0
105	AVCC2	PK4/RXD4/SMISO4/ SSCL4
106	AVSS2	PE5/D13[A13/D13]/ D5[A5/D5]/MTIOC4C/MTIOC2B/ IRQ5/AN013/COMP0
107	P63/A14/A12/IRQ7/AN209/CMPC23	PE4/D12[A12/D12]/ D4[A4/D4]/MTIOC4D/MTIOC1A/MTIOC4A/ MTIOC7D/IRQ12/AN012
108	P62/A15/A13/IRQ6/AN208/CMPC43	PE3/D11[A11/D11]/ D3[A3/D3]/MTIOC4B/POE8#/MTIOC1B/ TOC3/CTS12#/RTS12#/SS12#/ IRQ11/AN011
109	P61/A16/A14/IRQ5/AN207/CMPC13	PE2/D10[A10/D10]/ D2[A2/D2]/MTIOC4A/MTIOC7A/TIC3/ RXD12/SMISO12/SSCL12/RXDX12/ IRQ7-DS/AN010/CVREFC0
110	P60/A17/A15/IRQ4/AN206/CMPC03	PE1/D9[A9/D9]/ D1[A1/D1]/MTIOC4C/MTIOC3B/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/IRQ9/ AN009/CMPC00
111	P55/A18/A16/IRQ3/AN203/CMPC32	PE0/D8[A8/D8]/ D0[A0/D0]/MTIOC3D/SCK12/IRQ8/AN008
112	P54/A19/A17/IRQ2/AN202/CMPC22	P64/D3[A3/D3]/IRQ4
113	P53/A20/A18/IRQ1/AN201/CMPC12	P63/D2[A2/D2]/CS3#/IRQ3
114	P52/IRQ0/AN200/CMPC02	P62/D1[A1/D1]/CS2#/IRQ2
115	P51/AN205/CMPC52	P61/D0[A0/D0]/ CS1#/CTS9#/RTS9#/SS9#/IRQ1
116	P50/AN204/CMPC42	PK3/RXD9/SMISO9/ SSCL9
117	PH7/AN106/CVREFC1	P60/CS0#/SCK9/IRQ0
118	PH6/AN105	PK2/TXD9/SMOSI9/ SSDA9
119	PH5/AN104	TRDATA3(Note 1)/PD7/ D7[A7/D7]/MTIC5U/POE0#/IRQ7/AN023
120	P47/AN103	TRDATA2(Note 1)/PD6/D6[A6/D6]/ MTIC5V/POE4#/MTIOC8A/IRQ6/AN022
121	P46/AN102/CMPC50/CMPC51	TRCLK(Note 1)/PD5/D5[A5/D5]/ MTIC5W/POE10#/MTIOC8C/IRQ5/AN021
122	P45/AN101/CMPC40/CMPC41	TRSYNC(Note 1)/PD4/D4[A4/D4]/ POE11#/MTIOC8B/IRQ4/AN020

144-Pin LFQFP	RX66T	RX660
123	P44/AN100/CMPC30/CMPC31	TRDATA1(Note 1)/PD3/D3[A3/D3]/ POE8#/MTIOC8D/TOC2/IRQ3/AN019
124	PH4/AN107/PGAVSS1	TRDATA0(Note 1)/PD2/D2[A2/D2]/ MTIOC4D/TIC2/CRX0-B/IRQ2/AN018
125	PH3/AN006/CVREFC0	TRDATA7(Note 1)/PD1/D1[A1/D1]/ MTIOC4B/POE0#/CTX0-B/IRQ1/AN017
126	PH2/AN005	TRDATA6(Note 1)/PD0/D0[A0/D0]/ POE4#/IRQ0/AN016
127	PH1/AN004	TRSYNC1(Note 1)/P93/A19/ POE0#/CTS7#/RTS7#/SS7#/IRQ11
128	P43/AN003	TRDATA5(Note 1)/P92/A18/POE4#/ RXD7/SMISO7/ SSCL7/IRQ10
129	P42/AN002/CMPC20/CMPC21	TRDATA4(Note 1)/P91/A17/SCK7/IRQ9
130	P41/AN001/CMPC10/CMPC11	PF7
131	P40/AN000/CMPC00/CMPC01	P90/A16/TXD7/SMOSI7/SSDA7/IRQ0
132	PH0/AN007/PGAVSS0	PF6
133	AVCC1	P47/IRQ15-DS/AN007
134	AVCC0	P46/IRQ14-DS/AN006
135	AVSS0	P45/IRQ13-DS/AN005
136	AVSS1	P44/IRQ12-DS/AN004
137	P82/ALE/WAIT#/MTIC5U/MTIC5U#/ TMO4/SCK6/SCK12/IRQ3/COMP5	P43/IRQ11-DS/AN003
138	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/ TXD6/SMOSI6/SSDA6/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/COMP4	P42/IRQ10-DS/AN002
139	P80/CS1#/MTIC5W/MTIC5W#/ TMRI4/RXD6/SMISO6/SSCL6/RXD12/ SMISO12/SSCL12/RXDX12/IRQ5/COMP3	P41/IRQ9-DS/AN001
140	P11/RD#/MTIOC3A/MTCLKC/ MTIOC3A#/MTCLKC#/MTIOC9D/GTIOC3B/ GTETRGA/GTIOC3B#/GTETRGC/TMO3/ POE9#/IRQ1-DS	VREFL0/PJ7
141	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0-DS	P40/IRQ8-DS/AN000
142	P17/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC9B/GTIOC2B#/GTIOC9B#/IRQ14	VREFH0/PJ6
143	P16/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC8B/GTIOC1B#/GTIOC8B#/IRQ13	AVCC0
144	P15/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC7B/GTIOC0B#/GTIOC7B#/IRQ12	P07/IRQ15/ADTRG0#

Note 1. Not present on products without a JTAG.
Note 2. Not present on products provided with a JTAG.
Note 3. Not present on products without a sub-clock oscillator
Note 4. Not present on products provided with a sub-clock oscillator.
Note 5. Not available on products without a sub-clock oscillator.

3.2 100-Pin Package

Table 3.2 is Comparative Listing of 100-Pin Package Pin Functions.

Table 3.2 Comparative Listing of 100-Pin Package Pin Functions

100-Pin LFQFP	RX66T	RX660
1	PE5/BCLK/MTIOC9D/MTIOC9D#/ GTIOC3A/GTETRGB/GTIOC3A#/ GTETRGD/SCK9/CTS9#/RTS9#/SS9#/ IRQ0/ADST0	P06
2	EMLE	EMLE(Note 1)/P03(Note 2)/IRQ11(Note 2)/DA0(Note 2)
3	VSS	P04
4	UB/P00/A11/MTIOC9A/MTIOC9A#/ CACREF/RXD9/SMISO9/SSCL9/RXD12/ SMISO12/SSCL12/RXDX12/IRQ2/ADST1/ COMP0	PJ3/MTIOC3C/CTS6#/RTS6#/SS6#/CTS0#/ RTS0#/SS0#/IRQ11
5	VCL	VCL
6	MD/FINED	PJ1/MTIOC3A
7	P01/A10/MTIOC9C/MTIOC9C#/ GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE12#/TXD9/SMOSI9/ SSDA9/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/IRQ4/ADST2/COMP1	MD/FINED/PN6
8	PE4/A9/MTCLKC/MTCLKC#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/ POE10#/SCK9/IRQ1	XCIN(Note 3)/PH7(Note 4)
9	PE3/A8/MTCLKD/MTCLKD#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/ POE11#/CTS9#/RTS9#/SS9#/IRQ2-DS	XCOUT(Note 3)/PH6(Note 4)
10	RES#	RES#
11	XTAL/P37	XTAL/P37/IRQ4
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36/IRQ5
14	VCC	VCC
15	PE2/POE10#/NMI	P35/NMI
16	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/ TMO5/CTS5#/RTS5#/SS5#/CTS12#/ RTS12#/SS12#/SSLA3/IRQ15	TRST#(Note 1)/P34/MTIOC0A/TMCI3/ POE10#/SCK6/SCK0/IRQ4
17	PE0/WR1#/BC1#/WAIT#/MTIOC9B/ MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/ SSCL5/SSLA2/CRX0/IRQ7	P33/MTIOC0D/TMRI3/POE4#/POE11#/ RXD6/SMISO6/SSCL6/RXD0/SMISO0/ SSCL0/CRX0-A/IRQ3-DS
18	TRST#/PD7/MTIOC9A/MTIOC9A#/ GTIOC0A/GTIOC3A/GTIOC0A#/ GTIOC3A#/TMRI1/TMRI5/TXD5/ SMOSI5/SSDA5/SSLA1/CTX0/IRQ8	P32/MTIOC0C/TMO3/RTCIC2(Note 5)/ RTCOUT(Note 5)/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0-A/IRQ2-DS
19	TMS/PD6/MTIOC9C/MTIOC9C#/ GTIOC0B/GTIOC3B/GTIOC0B#/ GTIOC3B#/TMO1/CTS1#/RTS1#/SS1#/ CTS11#/RTS11#/SS11#/SSLA0/IRQ5/ ADST0	TMS(Note 1)/P31/MTIOC4D/TMCI2/ RTCIC1(Note 5)/CTS1#/RTS1#/SS1#/IRQ1-DS

100-Pin LFQFP	RX66T	RX660
20	TDI/PD5/GTIOC1A/GTETRGA/ GTIOC1A#/TMRI0/TMRI6/RXD1/ SMISO1/SSCL1/RXD11/SMISO11/ SSCL11/IRQ6	TDI(Note 1)/P30/MTIOC4B/TMRI3/ RTCIC0(Note 5)/POE8#/RXD1/SMISO1/SSCL1/ IRQ0-DS/COMP3
21	TCK/PD4/GTIOC1B/GTETRGB/ GTIOC1B#/TMCI0/TMCI6/SCK1/ SCK11/IRQ2	TCK(Note 1)/P27/CS3#/MTIOC2B/TMCI3/SCK1/ IRQ7/CVREFC3
22	TDO/PD3/GTIOC2A/GTETRGC/ GTIOC2A#/TMO0/TXD1/SMOSI1/ SSDA1/TXD11/SMOSI11/SSDA11	TDO(Note 1)/P26/CS2#/MTIOC2A/TMO1/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/IRQ6/ CMPC30
23	TRCLK/PD2/A7/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/TMCI1/TMO4/ SCK5/SCK8/MOSIA	P25/CS1#/MTIOC4C/MTCLKB/RXD3/ SMISO3/SSCL3/IRQ5/ADTRG0#
24	TRDATA3/PD1/A6/GTIOC3A/GTIOC0B/ GTIOC3A#/GTIOC0B#/TMO2/RXD8/ SMISO8/SSCL8/MISOA	P24/CS0#/MTIOC4A/MTCLKA/TMRI1/SCK3/ IRQ12
25	TRDATA2/PD0/A5/GTIOC3B/GTIOC1A/ GTIOC3B#/GTIOC1A#/TMO6/ TXD8/SMOSI8/SSDA8/RSPCKA	P23/MTIOC3D/MTCLKD/TXD3/SMOSI3/ SSDA3/CTS0#/RTS0#/SS0#/IRQ3
26	TRDATA1/PB7/A4/GTIOC1B/GTIOC1B#/ SCK5/SCK11/SCK12	P22/MTIOC3B/MTCLKC/TMO0/SCK0/IRQ15
27	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/ RXD5/SMISO5/SSCL5/RXD11/SMISO11/ SSCL11/RXD12/SMISO12/SSCL12/ RXDX12/CRX0/IRQ2	P21/MTIOC1B/TMCI0/MTIOC4A/RXD0/ SMISO0/SSCL0/IRQ9
28	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/ TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/ SSDA11/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0	P20/MTIOC1A/TMRI0/TXD0/SMOSI0/ SSDA0/IRQ8
29	VCC	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ MTIOC4B/SCK1/TXD3/SMOSI3/SSDA3/ MISOA-C/SDA2/IRQ7/COMP2
30	PB4/A1/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/IRQ3-DS	P16/MTIOC3C/MTIOC3D/TMO2/ RTCOUT(Note 5)/TXD1/SMOSI1/SSDA1/ RXD3/SMISO3/SSCL3/ MOSIA-C/SCL2/IRQ6/ADTRG0#
31	VSS	P15/MTIOC0D/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/SCK3/ CRX0-C/IRQ5/CMPC20
32	PB3/A7(Note 6)/MTIOC0A/MTIOC0A#/ CACREF/SCK6/RSPCKA/IRQ9	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/CTX0-C/IRQ4/CVREFC2
33	PB2/A6(Note 6)/MTIOC0B/MTIOC0B#/ GTADSM0/TMRI0/TXD6/SMOSI6/SSDA6/ SDA0/ADSM0	P13/MTIOC0B/TMO3/TXD2/SMOSI2/SSDA2/ SDA0/IRQ3
34	PB1/A5(Note 6)/MTIOC0C/MTIOC0C#/ GTADSM1/TMCI0/RXD6/SMISO6/SSCL6/ SCL0/IRQ4/ADSM1	P12/MTIC5U/TMCI1/RXD2/SMISO2/SSCL2/ SCL0/IRQ2
35	PB0/A0/A4(Note 6)/BC0#/MTIOC0D/ MTIOC0D#/TMO0/TXD6/SMOSI6/SSDA6/ CTS11#/RTS11#/SS11#/MOSIA/IRQ8/ ADTRG2#	PH3/MTIOC4D/TMCI0

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36	PA5/A3(Note 6)/MTIOC1A/MTIOC1A#/ TMCI3/RXD6/SMISO6/SSCL6/RXD8/ SMISO8/SSCL8/MISOA/IRQ1/ADTRG1#	PH2/MTIOC4C/TMRI0/TOC1/IRQ1
37	PA4/A2(Note 6)/MTIOC1B/MTIOC1B#/ TMCI7/SCK6/TXD8/SMOSI8/SSDA8/ RSPCKA/ADTRG0#	PH1/MTIOC3D/TMO0/TIC1/IRQ0/ADST0
38	PA3/A1(Note 6)/MTIOC2A/MTIOC2A#/ GTADSM0/TMRI7/TXD9/SMOSI9/ SSDA9/SCK8/SSLA0	PH0/MTIOC3B/CACREF/ADTRG0#
39	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/ GTADSM1/TMO7/CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/SCK11(Note 6)/SSLA1	P55/D0[A0/D0]/WAIT#/MTIOC4D/MTIOC4A/ TMO3/CRX0-D/IRQ10
40	PA1/MTIOC6A/MTIOC6A#/TMO4/TXD9/ SMOSI9/SSDA9/RXD11/SMISO11/ SSCL11/SSLA2/CRX0/IRQ14-DS/ADTRG0#	P54/ALE/D1[A1/D1]/MTIOC4B/TMCI1/ CTS2#/RTS2#/SS2#/CTX0-D/IRQ4
41	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK9/ TXD11/SMOSI11/SSDA11/SSLA3/CTX0	P53/BCLK/PMC0/IRQ3
42	VCC	P52/RD#/RXD2/SMISO2/SSCL2/IRQ2
43	P96/CS0#/WAIT#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/ POE4#/CTS8#/RTS8#/SS8#/IRQ4-DS	P51/WR1#/BC1#/WAIT#/SCK2/PMC0/IRQ1
44	VSS	P50/WR0#/WR#/TXD2/SMOSI2/ SSDA2/IRQ0
45	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#	UB/PC7/CS0#/MTIOC3A/MTCLKB/TMO2/ CACREF/TOC0/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/TXD10/ TXD010-C/SMOSI010-C/ SSDA010-C/MISOA-A/IRQ14
46	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#	PC6/D2[A2/D2]/CS1#/MTIOC3C/MTCLKA/ TMCI2/TIC0/RXD8/SMISO8/SSCL8/ SMISO10/SSCL10/RXD10/RXD010-C/ SMISO010-C/SSCL010-C/MOSIA-A/IRQ13
47	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#	PC5/D3[A3/D3]/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/MTIOC0C/SCK8/SCK10/ SCK010-C/RSPCKA-A/PMC0/IRQ5
48	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/P OE0#/MTIOC0A/SCK5/CTS8#/RTS8#/ SS8#/SS10#/CTS10#/RTS10#/ CTS010#-B/RTS010#-B/SS010#-B/ DE010-B/SSLA0-A/PMC0/IRQ12
49	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#	PC3/A19/MTIOC4D/TXD5/SMOSI5/SSDA5/ PMC0/IRQ11
50	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#	PC2/A18/MTIOC4B/RXD5/SMISO5/SSCL5/ TXDB011-A/SSLA3-A/IRQ10
51	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#	PC1/A17/MTIOC3A/SCK5/ TXD011-C/SMOSI011-C/ SSDA011-C/TXDA011-C/SSLA2-A/IRQ12
52	P75/D1[A1/D1]/MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#	PC0/A16/MTIOC3C/CTS5#/RTS5#/SS5#/ RXD011-C/SMISO011-C/ SSCL011-C/RXD011-C/SSLA1-A/IRQ14

100-Pin LFQFP	RX66T	RX660
53	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#	PB7/A15/MTIOC3B/TXD9/SMOSI9/SSDA9/ SMOSI11/SSDA11/TXD11/ TXD011-B/SMOSI011-B/SSDA011-B/IRQ15
54	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#	PB6/A14/MTIOC3D/RXD9/SMISO9/SSCL9/ SMISO11/SSCL11/RXD11/ RXD011-B/SMISO011-B/SSCL011-B/IRQ6
55	P72/D4[A4/D4]/ MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC5A/GTIOC1A#/GTIOC5A#	PB5/A13/MTIOC2A/MTIOC1B/TMRI1/ POE4#/TOC2/SCK9/SCK11/ SCK011-B/IRQ13
56	P71/D5[A5/D5]/ MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC4A/GTIOC0A#/GTIOC4A#	PB4/A12/CTS9#/RTS9#/SS9#/SS11#/ CTS11#/RTS11#/CTS011#-B/ RTS011#-B/SS011#-B/DE011-B/IRQ4
57	P70/D6[A6/D6]/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE0#/CTS9#/ RTS9#/SS9#/IRQ5-DS	PB3/A11/MTIOC0A/MTIOC4A/TMO0/ POE11#/TIC2/SCK4/SCK6/PMC0/IRQ3
58	P33/D7[A7/D7]/MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/GTIOC3B/ GTIOC3B#/TMO0/SSLA3/IRQ13-DS	PB2/A10/CTS4#/RTS4#/SS4#/CTS6#/ RTS6#/SS6#/IRQ2
59	P32/D8[A8/D8]/MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/GTIOC3A/GTIOC3A#/ TMO6/SSLA2/IRQ12-DS	PB1/A9/MTIOC0C/MTIOC4C/TMCI0/TXD4/ SMOSI4/SSDA4/TXD6/SMOSI6/SSDA6/ IRQ4-DS/COMP1
60	VCC	VCC
61	P31/D9[A9/D9]/MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/TMRI6/SSLA1/ IRQ6	PB0/A8/MTIC5W/MTIOC3D/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/ RSPCKA-C/IRQ12
62	VSS	VSS
63	P30/D10[A10/D10]/MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/TMCI6/SCK8/ CTS8#/RTS8#/SS8#/SSLA0/IRQ7/COMP3	PA7/A7/MISOA-B/IRQ7
64	P24/D11[A11/D11]/MTIC5U/MTIC5U#/ TMCI2/TMO6/CTS8#/RTS8#/SS8#/ SCK8/RSPCKA/IRQ4/COMP0	PA6/A6/MTIC5V/MTCLKB/TMCI3/POE10#/ MTIOC3D/MTIOC6B/CTS5#/RTS5#/SS5#/ CTS12#/RTS12#/SS12#/MOSIA-B/IRQ14
65	P23/D12[A12/D12]/MTIC5V/MTIC5V#/ TMO2/CACREF/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/ SIOX12/MOSIA/CTX0/IRQ11/COMP1	PA5/A5/MTIOC6B/RSPCKA-B/IRQ5
66	P22/D13[A13/D13]/MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/ TMO4/RXD8/SMISO8/SSCL8/RXD12/ SMISO12/SSCL12/RXDX12/MISOA/ CRX0/IRQ10/ADTRG2#/COMP2	PA4/A4/MTIC5U/MTCLKA/TMRI0/MTIOC4C/ MTIOC7C/TXD5/SMOSI5/SSDA5/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLA0-B/IRQ5-DS/CVREFC1/ADST0
67	P21/D14[A14/D14]/MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/TMCI4/TXD8/ SMOSI8/SSDA8/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/MOSIA/ IRQ6-DS/AN217/ADTRG1#/COMP5	PA3/A3/MTIOC0D/MTCLKD/MTIC5V/ MTIOC4D/RXD5/SMISO5/SSCL5/ IRQ6-DS/CMPC10
68	P20/D15[A15/D15]/MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/TMRI4/CTS8#/ RTS8#/SS8#/SCK8/RSPCKA/ IRQ7-DS/AN216/ADTRG0#/COMP4	PA2/A2/MTIOC7A/RXD5/SMISO5/SSCL5/ RXD12/SMISO12/SSCL12/RXDX12/ SSLA3-B/IRQ10

100-Pin LFQFP	RX66T	RX660
69	P65/A12/IRQ9/AN211/CMPC53/DA1	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ MTIOC3B/SCK5/SCK12/SSLA2-B/ IRQ11/ADTRG0#
70	P64/A13/IRQ8/AN210/CMPC33/DA0	PA0/BC0#/A0/MTIOC4A/CACREF/ MTIOC6D/SSLA1-B/IRQ0
71	AVCC2	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/IRQ7/AN015
72	AVCC2	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/CTS4#/RTS4#/SS4#/IRQ6/AN014
73	AVSS2	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/IRQ5/AN013/COMP0
74	P63/A12(Note 6)/A14/IRQ7/AN209/CMPC23	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/MTIOC4A/MTIOC7D/ IRQ12/AN012
75	P62/A13((Note 6)/A15/IRQ6/AN208/CMPC43	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ POE8#/MTIOC1B/TOC3/CTS12#/RTS12#/ SS12#/IRQ11/AN011
76	P61/A14((Note 6)/A16/IRQ5/AN207/CMPC13	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ MTIOC7A/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/IRQ7-DS/AN010/CVREFC0
77	P60/A15((Note 6)/A17/IRQ4/AN206/CMPC03	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/IRQ9/AN009/CMPC00
78	P55/A16((Note 6)/A18/IRQ3/AN203/CMPC32	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/ SCK12/IRQ8/AN008
79	P54/A17((Note 6)/A19/IRQ2/AN202/CMPC22	PD7/D7[A7/D7]/MTIC5U/POE0#/IRQ7/ AN023
80	P53/A18(Note 6)/A20/IRQ1/AN201/CMPC12	PD6/D6[A6/D6]/MTIC5V/POE4#/MTIOC8A/ IRQ6/AN022
81	P52/IRQ0/AN200/CMPC02	PD5/D5[A5/D5]/MTIC5W/POE10#/MTIOC8C/ IRQ5/AN021
82	P51/AN205/CMPC52	PD4/D4[A4/D4]/POE11#/MTIOC8B/IRQ4/ AN020
83	P50/AN204/CMPC42	PD3/D3[A3/D3]/POE8#/MTIOC8D/TOC2/ IRQ3/AN019
84	P47/AN103	PD2/D2[A2/D2]/MTIOC4D/TIC2/ CRX0-B/IRQ2/AN018
85	P46/AN102/CMPC50/CMPC51	PD1/D1[A1/D1]/MTIOC4B/POE0#/ CTX0-B/IRQ1/AN017
86	P45/AN101/CMPC40/CMPC41	PD0/D0[A0/D0]/POE4#/IRQ0/AN016
87	P44/AN100/CMPC30/CMPC31	P47/IRQ15-DS/AN007
88	P43/AN003	P46/IRQ14-DS/AN006
89	P42/AN002/CMPC20/CMPC21	P45/IRQ13-DS/AN005
90	P41/AN001/CMPC10/CMPC11	P44/IRQ12-DS/AN004
91	P40/AN000/CMPC00/CMPC01	P43/IRQ11-DS/AN003
92	AVCC1	P42/IRQ10-DS/AN002
93	AVCC0	P41/IRQ9-DS/AN001
94	AVSS0	VREFL0/PJ7
95	AVSS1	P40/IRQ8-DS/AN000

100-Pin LFQFP	RX66T	RX660
96	P82/ALE/WAIT#/MTIC5U/MTIC5U#/ TMO4/SCK6/SCK12/IRQ3/COMP5	VREFH0/PJ6
97	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/ TXD6/SMOSI6/SSDA6/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/COMP4	AVCC0
98	P80/CS1#/MTIC5W/MTIC5W#/TMRI4/ RXD6/SMISO6/SSCL6/RXD12/ SMISO12/SSCL12/RXDX12/IRQ5/COMP3	P07/IRQ15/ADTRG0#
99	P11/RD#/MTIOC3A/MTCLKC/ MTIOC3A#/MTCLKC#/MTIOC9D/ GTIOC3B/GTETRGA/GTIOC3B#/ GTETRGC/TMO3/POE9#/IRQ1-DS	AVSS0
100	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/ TMRI3/POE12#/CTS6#/RTS6#/SS6#/ IRQ0-DS	P05/IRQ13/DA1

Note 1. Not present on products without a JTAG.
Note 2. Not present on products provided with a JTAG.
Note 3. Not present on products without a sub-clock oscillator
Note 4. Not present on products provided with a sub-clock oscillator.
Note 5. Not available on products without a sub-clock oscillator.
Note 6. Only for products with RAM capacity 128 KB

3.3 80-Pin Package

Table 3.3 is Comparative Listing of 80-Pin Package Pin Functions.

Table 3.3 Comparative Listing of 80-Pin Package Pin Functions

80-Pin LFQFP	RX66T	RX660
1	EMLE	P06
2	VSS	P03/IRQ11/DA0
3	UB/P00/MTIOC9A/MTIOC9A#/CACREF/ RXD9/SMISO9/SSCL9/RXD12/SMISO12/ SSCL12/RXDX12/IRQ2/ADST1/COMP0	P04
4	VCL	VCL
5	MD/FINED	PJ1/MTIOC3A
6	P01/MTIOC9C/MTIOC9C#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE12#/ TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/IRQ4/ ADST2/COMP1	MD/FINED/PN6
7	PE4/MTCLKC/MTCLKC#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE10#/ SCK9/IRQ1	XCIN(Note 1)/PH7(Note 2)
8	PE3/MTCLKD/MTCLKD#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/ POE11#/CTS9#/RTS9#/SS9#/IRQ2-DS	XCOUT(Note 1)/PH6(Note 2)
9	RES#	RES#
10	XTAL/P37	XTAL/P37/IRQ4
11	VSS	VSS
12	EXTAL/P36	EXTAL/P36/IRQ5
13	VCC	VCC
14	PE2/POE10#/NMI	P35/NMI
15	TRST#/PD7/MTIOC9A/MTIOC9A#/ GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/ TMRI1/TMRI5/TXD5/SMOSI5/SSDA5/ SSLA1/CTX0/IRQ8	P34/MTIOC0A/TMCI3/POE10#/SCK6/SCK0/ IRQ4
16	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/ GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/ CTS1#/RTS1#/SS1#/CTS11#/RTS11#/ SS11#/SSLA0/IRQ5/ADST0	P32/MTIOC0C/TMO3/RTCIC2/RTCOUT/ POE0#/POE10#/TXD6/SMOSI6/SSDA6/ TXD0/SMOSI0/SSDA0/CTX0-A/IRQ2-DS
17	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6	P31/MTIOC4D/TMCI2/RTCIC1/CTS1#/ RTS1#/SS1#/IRQ1-DS
18	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/T MCI0/TMCI6/SCK1/SCK11/IRQ2	P30/MTIOC4B/TMRI3/RTCIC0/POE8#/ RXD1/SMISO1/SSCL1/IRQ0-DS/COMP3
19	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11	P27/MTIOC2B/TMCI3/SCK1/IRQ7/ CVREFC3
20	PD2/GTIOC2B/GTIOC0A/GTIOC2B#/ GTIOC0A#/TMCI1/TMO4/SCK5/SCK8/ MOSIA	P26/MTIOC2A/TMO1/TXD1/SMOSI1/ SSDA1/CTS3#/RTS3#/SS3#/IRQ6/CMPC30
21	PB6/GTIOC2A/GTIOC2A#/RXD5/SMISO5/ SSCL5/RXD11/SMISO11/SSCL11/RXD12/ SMISO12/SSCL12/RXDX12/CRX0/IRQ2	P21/MTIOC1B/TMCI0/MTIOC4A/RXD0/ SMISO0/SSCL0/IRQ9

80-Pin LFQFP	RX66T	RX660
22	PB5/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/ SSDA5/TXD11/SMOSI11/SSDA11/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/CTX0	P20/MTIOC1A/TMRI0/TXD0/SMOSI0/ SSDA0/IRQ8
23	VCC	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ MTIOC4B/SCK1/TXD3/SMOSI3/SSDA3/ MISOA-C/SDA2/IRQ7/COMP2
24	PB4/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/ CTS5#/RTS5#/SS5#/SCK11/CTS11#/ RTS11#/SS11#/IRQ3-DS	P16/MTIOC3C/MTIOC3D/TMO2/RTCOUT/ TXD1/SMOSI1/SSDA1/ RXD3/SMISO3/SSCL3/ MOSIA-C/SCL2/IRQ6/ADTRG0#
25	VSS	P15/MTIOC0B/MTCLKB/ TMCI2/RXD1/SMISO1/SSCL1/SCK3/ CRX0-C/IRQ5/CMPC20
26	PB3/MTIOC0A/MTIOC0A#/CACREF/SCK6/ RSPCKA/IRQ9	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/CTX0-C/IRQ4/CVREFC2
27	PB2/MTIOC0B/MTIOC0B#/GTADSM0/ TMRI0/TXD6/SMOSI6/SSDA6/SDA0/ADSM0	P13/MTIOC0B/TMO3/SDA0/IRQ3
28	PB1/MTIOC0C/MTIOC0C#/GTADSM1/ TMCI0/RXD6/SMISO6/SSCL6/SCL0/IRQ4/ ADSM1	P12/MTIC5U/TMCI1/SCL0/IRQ2
29	PB0/MTIOC0D/MTIOC0D#/TMO0/TXD6/ SMOSI6/SSDA6/CTS11#/ RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#	PH3/MTIOC4D/TMCI0
30	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/ SMISO6/SSCL6/RXD8/SMISO8/SSCL8/ MISOA/IRQ1/ADTRG1#	PH2/MTIOC4C/TMRI0/TOC1/IRQ1
31	PA3/MTIOC2A/MTIOC2A#/GTADSM0/ TMRI7/TXD9/SMOSI9/SSDA9/SCK8/SSLA0	PH1/MTIOC3D/TMO0/TIC1/IRQ0/ADST0
32	VCC	PH0/MTIOC3B/CACREF/ADTRG0#
33	P96/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE4#/CTS8#/RTS8#/SS8#/ IRQ4-DS	P55/MTIOC4D/MTIOC4A/TMO3/ CRX0-D/IRQ10
34	VSS	P54/MTIOC4B/TMCI1/CTX0-D/IRQ4
35	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#	UB/PC7/MTIOC3A/MTCLKB/TMO2/ CACREF/TOC0/TXD8/SMOSI8/SSDA8/ SMOSI10/SSDA10/TXD10/TXD010-C/ SMOSI010-C/SSDA010-C/MISOA-A/IRQ14
36	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#	PC6/MTIOC3C/MTCLKA/TMCI2/TIC0/RXD8/ SMISO8/SSCL8/SMISO10/SSCL10/RXD10/ RXD010-C/SMISO010-C/ SSCL010-C/MOSIA-A/IRQ13
37	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#	PC5/MTIOC3B/MTCLKD/TMRI2/MTIOC0C/ SCK8/SCK10/SCK010-C/ RSPCKA-A/PMC0/IRQ5
38	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/ MTIOC0A/SCK5/CTS8#/RTS8#/SS8#/ SS10#/CTS10#/RTS10#/CTS010#-B/ RTS010#-B/SS010#-B/DE010-B/ SSLA0-A/PMC0/IRQ12
39	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5/ PMC0/IRQ11

80-Pin LFQFP	RX66T	RX660
40	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/ TXDB011-A/SSLA3-A/IRQ10
41	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC6B/GTIOC2B#/GTIOC6B#	PB7/MTIOC3B/TXD9/SMOSI9/SSDA9/ SMOSI11/SSDA11/TXD11/ TXD011-B/SMOSI011-B/ SSDA011-B/IRQ15
42	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC5B/GTIOC1B#/GTIOC5B#	PB6/MTIOC3D/RXD9/SMISO9/SSCL9/ SMISO11/SSCL11/RXD11/ RXD011-B/SMISO011-B/SSCL011-B/IRQ6
43	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC4B/GTIOC0B#/GTIOC4B#	PB5/MTIOC2A/MTIOC1B/TMRI1/POE4#/ TOC2/SCK9/SCK11/SCK011-B/IRQ13
44	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC6A/GTIOC2A#/GTIOC6A#	PB4/CTS9#/RTS9#/SS9#/SS11#/CTS11#/ RTS11#/CTS011#-B/RTS011#-B/ SS011#-B/DE011-B/IRQ4
45	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC5A/GTIOC1A#/GTIOC5A#	PB3/MTIOC0A/MTIOC4A/TMO0/POE11#/ TIC2/SCK4/SCK6/PMC0/IRQ3
46	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC4A/GTIOC0A#/GTIOC4A#	PB2/CTS4#/RTS4#/SS4#/CTS6#/RTS6#/ SS6#/IRQ2
47	P70/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE0#/CTS9#/RTS9#/SS9#/ IRQ5-DS	PB1/MTIOC0C/MTIOC4C/ TMCI0/TXD4/SMOSI4/SSDA4/TXD6/ SMOSI6/SSDA6/IRQ4-DS/COMP1
48	VCC	VCC
49	P31/MTIOC0A/MTCLKC/MTIOC0A#/ MTCLKC#/TMRI6/SSLA1/IRQ6	PB0/MTIC5W/MTIOC3D/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/ RSPCKA-C/IRQ12
50	VSS	VSS
51	P30/MTIOC0B/MTCLKD/MTIOC0B#/ MTCLKD#/TMCI6/SCK8/CTS8#/RTS8#/ SS8#/SSLA0/IRQ7/COMP3	PA6/MTIC5V/MTCLKB/TMCI3/POE10#/ MTIOC3D/MTIOC6B/CTS5#/RTS5#/SS5#/ CTS12#/RTS12#/SS12#/MOSIA-B/IRQ14
52	P27/MTIOC1A/MTIOC0C/MTIOC1A#/ MTIOC0C#/POE9#/IRQ15	PA5/MTIOC6B/RSPCKA-B/IRQ5
53	P22/MTIC5W/MTCLKD/MTIC5W#/ MTCLKD#/MTIOC9B/MTCLKD/MTIOC9B/ TMRI2/TMO4/RXD8/SMISO8/IRQ10/ ADTRG2#/COMP2	PA4/MTIC5U/MTCLKA/TMRI0/MTIOC4C/ MTIOC7C/TXD5/SMOSI5/SSDA5/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLA0-B/IRQ5-DS/CVREFC1/ADST0
54	P21/MTIOC9A/MTCLKA/MTIOC9A#/ MTCLKA#/TMCI4/TXD8/SMOSI8/ SSDA8/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/MOSIA/IRQ6-DS/AN217/ ADTRG1#/COMP5	PA3/MTIOC0D/MTCLKD/MTIC5V/MTIOC4D/ RXD5/SMISO5/SSCL5/IRQ6-DS/CMPC10
55	P20/MTIOC9C/MTCLKB/MTIOC9C#/ MTCLKB#/TMRI4/CTS8#/RTS8#/SS8#/ SCK8/RSPCKA/IRQ7-DS/AN216/ ADTRG0#/COMP4	PA2/MTIOC7A/RXD5/SMISO5/SSCL5/ RXD12/SMISO12/SSCL12/RXDX12/ SSLA3-B/IRQ10
56	P65/IRQ9/AN211/CMPC53/DA1	PA1/MTIOC0B/MTCLKC/MTIOC7B/ MTIOC3B/SCK5/SCK12/SSLA2-B/IRQ11/ ADTRG0#
57	P64/IRQ8/AN210/CMPC33/DA0	PA0/MTIOC4A/CACREF/MTIOC6D/ SSLA1-B/IRQ0
58	AVCC2	PE5/MTIOC4C/MTIOC2B/IRQ5/AN013/ COMP0

80-Pin LFQFP	RX66T	RX660
59	AVSS2	PE4/MTIOC4D/MTIOC1A/MTIOC4A/ MTIOC7D/IRQ12/AN012
60	P62/IRQ6/AN208/CMPC43	PE3/MTIOC4B/POE8#/MTIOC1B/TOC3/ CTS12#/RTS12#/SS12#/IRQ11/AN011
61	P55/IRQ3/AN203/CMPC32	PE2/MTIOC4A/MTIOC7A/TIC3/RXD12/ SMISO12/SSCL12/RXDX12/ IRQ7-DS/AN010/CVREFC0
62	P54/IRQ2/AN202/CMPC22	PE1/MTIOC4C/MTIOC3B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/IRQ9/AN009 /CMPC00
63	P53/IRQ1/AN201/CMPC12	PE0/MTIOC3D/SCK12/IRQ8/AN008
64	P52/IRQ0/AN200/CMPC02	PD2/MTIOC4D/TIC2/CRX0-B/IRQ2/AN018
65	P47/AN103	PD1/MTIOC4B/POE0#/CTX0-B/IRQ1/AN017
66	P46/AN102/CMPC50/CMPC51	PD0/POE4#/IRQ0/AN016
67	P45/AN101/CMPC40/CMPC41	P47/IRQ15-DS/AN007
68	P44/AN100/CMPC30/CMPC31	P46/IRQ14-DS/AN006
69	PH4/AN107/PGAVSS1	P45/IRQ13-DS/AN005
70	P43/AN003	P44/IRQ12-DS/AN004
71	P42/AN002/CMPC20/CMPC21	P43/IRQ11-DS/AN003
72	P41/AN001/CMPC10/CMPC11	P42/IRQ10-DS/AN002
73	P40/AN000/CMPC00/CMPC01	P41/IRQ9-DS/AN001
74	PH0/AN007/PGAVSS0	VREFL0/PJ7
75	AVCC1	P40/IRQ8-DS/AN000
76	AVCC0	VREFH0/PJ6
77	AVSS0	AVCC0
78	AVSS1	P07/IRQ15/ADTRG0#
79	P11/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/MTIOC9D/GTIOC3B/GTETRGA/ GTIOC3B#/GTETRGC/TMO3/ POE9#/IRQ1-DS	AVSS0
80	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0-DS	P05/IRQ13/DA1

Note 1. Not present on products without a sub-clock oscillator
Note 2. Not present on products provided with a sub-clock oscillator.

3.4 64-Pin Package

Table 3.4 is Comparative Listing of 64-Pin Package Pin Functions.

Table 3.4 Comparative Listing of 64-Pin Package Pin Functions

64-Pin LFQFP/ LQFP	RX66T	RX660
1	EMLE	P03/IRQ11/DA0
2	UB/P00/MTIOC9A/MTIOC9A#/CACREF/ RXD9/SMISO9/SSCL9/RXD12/SMISO12/ SSCL12/RXDX12/IRQ2/ADST1/COMP0	VCL
3	VCL	MD/FINED/PN6
4	MD/FINED	XCIN(Note 1)/PH7(Note 2)
5	P01/MTIOC9C/MTIOC9C#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE12#/TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/IRQ4/ADST2/ COMP1	XCOUT(Note 1)/PH6(Note 2)
6	RES#	RES#
7	XTAL/P37	XTAL/P37/IRQ4
8	VSS	VSS
9	EXTAL/P36	EXTAL/P36/IRQ5
10	VCC	VCC
11	PE2/POE10#/NMI	P35/NMI
12	TRST#/PD7/MTIOC9A/MTIOC9A#/ GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/ TMRI1/TMRI5/TXD5/SMOSI5/SSDA5/ SSLA1/CTX0/IRQ8	P32/MTIOC0C/TMO3/RTCIC2(Note 3)/ RTCOUT(Note 3)/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/CTX0-A/IRQ2-DS
13	TMS/PD6/MTIOC9C/MTIOC9C#/ GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/ TMO1/CTS1#/RTS1#/SS1#/CTS11#/ RTS11#/SS11#/SSLA0/IRQ5/ADST0	P31/MTIOC4D/TMCI2/RTCIC1(Note 3)/CTS1#/ RTS1#/SS1#/IRQ1-DS
14	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6	P30/MTIOC4B/TMRI3/RTCIC0(Note 3)/POE8#/ RXD1/SMISO1/SSCL1/IRQ0-DS/COMP3
15	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/ TMCI0/TMCI6/SCK1/SCK11/IRQ2	P27/MTIOC2B/TMCI3/SCK1/IRQ7/ CVREFC3
16	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11	P26/MTIOC2A/TMO1/TXD1/SMOSI1/ SSDA1/CTS3#/RTS3#/SS3#/IRQ6/CMPC30
17	PB6/GTIOC2A/GTIOC2A#/RXD5/SMISO5/ SSCL5/RXD11/SMISO11/SSCL11/RXD12/ SMISO12/SSCL12/RXDX12/CRX0/IRQ2	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ MTIOC4B/SCK1/TXD3/SMOSI3/SSDA3/ MISOA-C/SDA2/IRQ7/COMP2
18	PB5/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/ SSDA5/TXD11/SMOSI11/SSDA11/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/CTX0	P16/MTIOC3C/MTIOC3D/TMO2/ RTCOUT(Note 3)/TXD1/SMOSI1/SSDA1/RXD3/ SMISO3/SSCL3/MOSIA-C/SCL2/ IRQ6/ADTRG0#
19	PB4/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/IRQ3-DS	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/SCK3/ CRX0-C/IRQ5/CMPC20

64-Pin LFQFP/ LQFP	RX66T	RX660
20	PB3/MTIOC0A/MTIOC0A#/CACREF/SCK6/ RSPCKA/IRQ9	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/CTX0-C/IRQ4/CVREFC2
21	PB2/MTIOC0B/MTIOC0B#/GTADSM0/ TMRI0/TXD6/SMOSI6/SSDA6/SDA0/ADSM0	PH3/MTIOC4D/TMCI0
22	PB1/MTIOC0C/MTIOC0C#/GTADSM1/ TMCI0/RXD6/SMISO6/SSCL6/SCL0/IRQ4/ ADSM1	PH2/MTIOC4C/TMRI0/TOC1/IRQ1
23	PB0/MTIOC0D/MTIOC0D#/TMO0/TXD6/ SMOSI6/SSDA6/CTS11#/RTS11#/SS11#/ MOSIA/IRQ8/ADTRG2#	PH1/MTIOC3D/TMO0/TIC1/IRQ0/ADST0
24	VCC	PH0/MTIOC3B/CACREF/ADTRG0#
25	P96/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE4#/CTS8#/RTS8#/ SS8#/IRQ4-DS	P55/MTIOC4D/MTIOC4A/TMO3/ CRX0-D/IRQ10
26	VSS	P54/MTIOC4B/TMCI1/CTX0-D/IRQ4
27	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#	UB/PC7/MTIOC3A/MTCLKB/TMO2/ CACREF/TOC0/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/TXD10/ TXD010-C/SMOSI010-C/ SSDA010-C/MISOA-A/IRQ14
28	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#	PC6/MTIOC3C/MTCLKA/TMCI2/TIC0/ RXD8/SMISO8/SSCL8/SMISO10/SSCL10/ RXD10/RXD010-C/SMISO010-C/ SSCL010-C/MOSIA-A/IRQ13
29	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#	PC5/MTIOC3B/MTCLKD/TMRI2/MTIOC0C/ SCK8/SCK10/SCK010-C/RSPCKA-A/ PMC0/IRQ5
30	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/ MTIOC0A/SCK5/CTS8#/RTS8#/SS8#/ SS10#/CTS10#/RTS10#/ CTS010#-B/RTS010#-B/SS010#-B/ DE010-B/SSLA0-A/PMC0/IRQ12
31	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5/ PMC0/IRQ11
32	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/ TXDB011-A/SSLA3-A/IRQ10
33	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC6B/GTIOC2B#/GTIOC6B#	PB7/MTIOC3B/TXD9/SMOSI9/SSDA9/ SMOSI11/SSDA11/TXD11/ TXD011-B/SMOSI011-B/SSDA011-B/IRQ15
34	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC5B/GTIOC1B#/GTIOC5B#	PB6/MTIOC3D/RXD9/SMISO9/SSCL9/ SMISO11/SSCL11/RXD11/ RXD011-B/SMISO011-B/SSCL011-B/IRQ6
35	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC4B/GTIOC0B#/GTIOC4B#	PB5/MTIOC2A/MTIOC1B/TMRI1/POE4#/ TOC2/SCK9/SCK11/SCK011-B/IRQ13
36	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC6A/GTIOC2A#/GTIOC6A#	PB3/MTIOC0A/MTIOC4A/TMO0/ POE11#/TIC2/SCK4/SCK6/PMC0/IRQ3
37	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC5A/GTIOC1A#/GTIOC5A#	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD4/ SMOSI4/SSDA4/TXD6/SMOSI6/SSDA6/ IRQ4-DS/COMP1

64-Pin LFQFP/ LQFP	RX66T	RX660
38	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC4A/GTIOC0A#/GTIOC4A#	VCC
39	P70/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE0#/CTS9#/RTS9#/SS9#/ IRQ5-DS	PB0/MTIC5W/MTIOC3D/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/ RSPCKA-C/IRQ12
40	VCC	VSS
41	VSS	PA6/MTIC5V/MTCLKB/TMCI3/POE10#/ MTIOC3D/MTIOC6B/CTS5#/RTS5#/SS5#/ CTS12#/RTS12#/SS12#/MOSIA-B/IRQ14
42	P22/MTIC5W/MTCLKD/MTIC5W#/ MTCLKD#/MTIOC9B/TMRI2/TMO4/RXD8/ SMISO8/SSCL8/RXD12/SMISO12/SSCL12/ RXDX12/MISOA/CRX0/IRQ10/ADTRG2#/ COMP2	PA4/MTIC5U/MTCLKA/TMRI0/MTIOC4C/ MTIOC7C/TXD5/SMOSI5/SSDA5/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLA0-B/IRQ5-DS/CVREFC1/ADST0
43	P21/MTIOC9A/MTCLKA/MTIOC9A#/ MTCLKA#/TMCI4/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ MOSIA/IRQ6-DS/AN217/ADTRG1#/COMP5	PA3/MTIOC0D/MTCLKD/MTIC5V/MTIOC4D/ RXD5/SMISO5/SSCL5/IRQ6-DS/CMPC10
44	P20/MTIOC9C/MTCLKB/MTIOC9C#/ MTCLKB#/TMRI4/CTS8#/RTS8#/SS8#/ SCK8/RSPCKA/IRQ7-DS/AN216/ ADTRG0#/COMP4	PA1/MTIOC0B/MTCLKC/ MTIOC7B/MTIOC3B/SCK5/SCK12/ SSLA2-B/IRQ11/ADTRG0#
45	P65/IRQ9/AN211/CMPC53/DA1	PA0/MTIOC4A/CACREF/MTIOC6D/ SSLA1-B/IRQ0
46	P64/IRQ8/AN210/CMPC33/DA0	PE5/MTIOC4C/MTIOC2B/IRQ5/AN013/ COMP0
47	AVCC2	PE4/MTIOC4D/MTIOC1A/MTIOC4A/ MTIOC7D/IRQ12/AN012
48	AVSS2	PE3/MTIOC4B/POE8#/MTIOC1B/TOC3/ CTS12#/RTS12#/SS12#/IRQ11/AN011
49	P54/IRQ2/AN202/CMPC22	PE2/MTIOC4A/MTIOC7A/TIC3/RXD12/ SMISO12/SSCL12/RXDX12/ IRQ7-DS/AN010/CVREFC0
50	P53/IRQ1/AN202/CMPC22	PE1/MTIOC4C/MTIOC3B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/IRQ9/AN009/ CMPC00
51	P52/IRQ0/AN200/CMPC02	PE0/MTIOC3D/SCK12/IRQ8/AN008
52	P46/AN102/CMPC50/CMPC51	P47/IRQ15-DS/AN007
53	P45/AN101/CMPC40/CMPC41	P46/IRQ14-DS/AN006
54	P44/AN100/CMPC30/CMPC31	P45/IRQ13-DS/AN005
55	PH4/AN107/PGAVSS1	P44/IRQ12-DS/AN004
56	P42/AN002/CMPC20/CMPC21	P43/IRQ11-DS/AN003
57	P41/AN001/CMPC10/CMPC11	P42/IRQ10-DS/AN002
58	P40/AN000/CMPC00/CMPC01	P41/IRQ9-DS/AN001
59	PH0/AN007/PGAVSS0	VREFL0/PJ7
60	AVCC1	P40/IRQ8-DS/AN000
61	AVCC0	VREFH0/PJ6
62	AVSS0	AVCC0
63	AVSS1	P07/IRQ15/ADTRG0#

64-Pin LFQFP/ LQFP	RX66T	RX660
64	P11/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/MTIOC9D/GTIOC3B/GTETRGA/ GTIOC3B#/GTETRGC/TMO3/POE9#/ IRQ1-DS	AVSS0

Note 1. Not present on products without a sub-clock oscillator
Note 2. Not present on products provided with a sub-clock oscillator.
Note 3. Not available on products without a sub-clock oscillator.

3.5 48-Pin Package

Table 3.5 is Comparative Listing of 48-Pin Package Pin Functions.

Table 3.5 Comparative Listing of 48-Pin Package Pin Functions

48-Pin LFQFP/ HWQFN	RX66T	RX660
1	UB/P00/MTIOC9A/MTIOC9A#/CACREF/ RXD9/SMISO9/SSCL9/RXD12/SMISO12/ SSCL12/RXDX12/IRQ2/ADST1/COMP0	VCL
2	VCL	MD/FINED/PN6
3	MD/FINED	RES#
4	RES#	XTAL/P37/IRQ4
5	XTAL/P37	VSS
6	VSS	EXTAL/P36/IRQ5
7	EXTAL/P36	VCC
8	VCC	P35/NMI
9	PE2/POE10#/NMI	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/ IRQ1-DS
10	PD7/MTIOC9A/MTIOC9A#/GTIOC0A/ GTIOC3A/GTIOC0A#/GTIOC3A#/TMRI1/ TMRI5/TXD5/SMOSI5/SSDA5/SSLA1/CTX0/ IRQ8	P30/MTIOC4B/POE8#/RXD1/SMISO1/ SSCL1/IRQ0-DS/COMP3
11	PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6	P27/MTIOC2B/SCK1/IRQ7/CVREFC3
12	PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11	P26/MTIOC2A/TMO1/TXD1/SMOSI1/ SSDA1/CTS3#/RTS3#/SS3#/IRQ6/CMPC30
13	PB6/GTIOC2A/GTIOC2A#/RXD5/SMISO5/ SSCL5/RXD11/SMISO11/SSCL11/RXD12/ SMISO12/SSCL12/RXDX12/CRX0/IRQ2	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ MTIOC4B/SCK1/TXD3/SMOSI3/SSDA3/ MISOA-C/SDA2/IRQ7/COMP2
14	PB5/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/ SSDA5/TXD11/SMOSI11/SSDA11/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/CTX0	P16/MTIOC3C/MTIOC3D/TMO2/ TXD1/SMOSI1/SSDA1/RXD3/SMISO3/ SSCL3/MOSIA-C/SCL2/IRQ6/ADTRG0#
15	PB4/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/IRQ3-DS	P15/MTIOC0D/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/SCK3/ CRX0-C/IRQ5/CMPC20
16	PB3/MTIOC0A/MTIOC0A#/CACREF/SCK6/ RSPCKA/IRQ9	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/CTX0-C/IRQ4/CVREFC2
17	PB2/MTIOC0B/MTIOC0B#/GTADSM0/ TMRI0/TXD6/SMOSI6/SSDA6/SDA0/ADSM0	PH3/MTIOC4D/TMCI0
18	PB1/MTIOC0C/MTIOC0C#/GTADSM1/ TMCI0/RXD6/SMISO6/SSCL6/SCL0/IRQ4/ ADSM1	PH2/MTIOC4C/TMRI0/TOC1/IRQ1
19	PB0/MTIOC0D/MTIOC0D#/TMO0/TXD6/ SMOSI6/SSDA6/CTS11#/RTS11#/SS11#/ MOSIA/IRQ8/ADTRG2#	PH1/MTIOC3D/TMO0/TIC1/IRQ0/ADST0
20	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/ SMISO6/SSCL6/MISOA/IRQ1/ADTRG1#	PH0/MTIOC3B/CACREF/ADTRG0#

48-Pin LFQFP/ HWQFN	RX66T	RX660
21	PA3/MTIOC2A/MTIOC2A#/GTADSM0/ TMRI7/TXD9/SMOSI9/SSDA9/SSLA0	UB/PC7/MTIOC3A/MTCLKB/TMO2/ CACREF/TOC0/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/TXD10/ TXD010-C/SMOSI010-C/ SSDA010-C/MISOA-A/IRQ14
22	VCC	PC6/MTIOC3C/MTCLKA/TMCI2/TIC0/RXD8/ SMISO8/SSCL8/ SMISO10/SSCL10/RXD10/ RXD010-C/SMISO010-C/ SSCL010-C/MOSIA-A/IRQ13
23	VSS	PC5/MTIOC3B/MTCLKD/TMRI2/MTIOC0C/ SCK8/SCK10/SCK010-C/ RSPCKA-A/PMC0/IRQ5
24	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/ MTIOC0A/SCK5/CTS8#/RTS8#/SS8#/ SS10#/CTS10#/RTS10#/ CTS010#-B/RTS010#-B/SS010#-B/ DE010-B/SSLA0-A/PMC0/IRQ12
25	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC6B/GTIOC2B#/GTIOC6B#	PB5/MTIOC2A/MTIOC1B/TMRI1/POE4#/ TOC2/IRQ13
26	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC5B/GTIOC1B#/GTIOC5B#	PB3/MTIOC0A/MTIOC4A/TMO0/ POE11#/TIC2/SCK4/SCK6/PMC0/IRQ3
27	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC4B/GTIOC0B#/GTIOC4B#	PB1/MTIOC0C/MTIOC4C/TMCI0/ TXD4/SMOSI4/SSDA4/TXD6/ SMOSI6/SSDA6/IRQ4-DS/COMP1
28	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC6A/GTIOC2A#/GTIOC6A#	VCC
29	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC5A/GTIOC1A#/GTIOC5A#	PB0/MTIC5W/MTIOC3D/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/ RSPCKA-C/IRQ12
30	MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC4A/GTIOC0A#/GTIOC4A#	VSS
31	VCC	PA6/MTIC5V/MTCLKB/POE10#/ MTIOC3D/CTS5#/RTS5#/SS5#/ CTS12#/RTS12#/SS12#/MOSIA-B/IRQ14
32	VSS	PA4/MTIC5U/MTCLKA/TMRI0/MTIOC4C/ MTIOC7C/TXD5/SMOSI5/SSDA5/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLA0-B/IRQ5-DS/CVREFC1/ADST0
33	P65/IRQ9/AN211/CMPC53/DA1	PA3/MTIOC0D/MTCLKD/MTIC5V/MTIOC4D/ RXD5/SMISO5/SSCL5/IRQ6-DS/CMPC10
34	P64/IRQ8/AN210/CMPC33/DA0	PA1/MTIOC0B/MTCLKC/ MTIOC7B/MTIOC3B/SCK5/SCK12/ SSLA2-B/IRQ11/ADTRG0#
35	AVCC2	PE4/MTIOC4D/MTIOC1A/MTIOC4A/ MTIOC7D/IRQ12/AN012
36	AVSS2	PE3/MTIOC4B/POE8#/MTIOC1B/TOC3/ CTS12#/RTS12#/SS12#/IRQ11/AN011

48-Pin LFQFP/ HWQFN	RX66T	RX660
37	P62/IRQ6/AN208/CMPC43	PE2/MTIOC4A/MTIOC7A/TIC3/RXD12/ SMISO12/SSCL12/RXDX12/ IRQ7-DS/AN010/CVREFC0
38	P44/AN100/CMPC30/CMPC31	PE1/MTIOC4C/MTIOC3B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/IRQ9/AN009/ CMPC00
39	P43/AN003	P47/IRQ15-DS/AN007
40	P42/AN002/CMPC20/CMPC21	P46/IRQ14-DS/AN006
41	P41/AN001/CMPC10/CMPC11	P45/IRQ13-DS/AN005
42	P40/AN000/CMPC00/CMPC01	P42/IRQ10-DS/AN002
43	AVCC1	P41/IRQ9-DS/AN001
44	AVCC0	VREFL0/PJ7
45	AVSS0	P40/IRQ8-DS/AN000
46	AVSS1	VREFH0/PJ6
47	P11/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/MTIOC9D/GTIOC3B/ GTETRGA/GTIOC3B#/GTETRGC/TMO3/ POE9#/IRQ1-DS	AVCC0
48	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0-DS	AVSS0

4. Important Information when Migrating Between MCUs

This section presents important information on differences between the RX660 Group and the RX66T Group.

4.1 Notes on Functional Design, presents information regarding the software.

4.1 Notes on Functional Design

Some software that runs on the RX66T Group is compatible with the RX660 Group. Nevertheless, appropriate caution must be exercised due to differences in aspects such as operation timing and electrical characteristics.

Software-related considerations regarding function settings that differ between the RX660 Group and RX66T Group are as follows:

For differences between modules and functions, refer to 2, Comparative Overview of Specifications For further information, refer to the User's Manual: Hardware of each MCU group, listed in 5, Reference Documents.

4.1.1 RIIC Operating Voltage Setting

When using the RIIC on the RX660 Group, it is necessary to specify the power supply voltage range to preserve the slope characteristics. VCC is set to a value of 4.5 V or greater by default. If it is set to a value less than 4.5 V, make sure to change the voltage range before activating the RIIC. For details, refer to the description of the VOLSR.RICVLS bit in RX660 Group User's Manual: Hardware.

4.1.2 Performing RAM Self-Diagnostics on Save Register Banks

On the RX660 Group save register banks are configured in the RAM.

The save register banks are provided with a buffer, so when a SAVE instruction is used to write data to a register and then a RSTR instruction is used to read data from the same register, the data is actually read from the buffer and not from the RAM memory cells.

When performing self-diagnostics on the RAM in a save register bank, use the following sequence of steps for checking the written data in order to prevent the data from being read from the buffer:

1. Use the SAVE instruction to write data to the bank that is the target of the diagnostic test.
2. Use the SAVE instruction to write data to a bank other than that written to in step 1.
3. Use the RSTR instruction to read data from the bank written to in step 1.

4.1.3 Restrictions on Compare Function

The compare function of the 12-bit A/D converter on the RX660 Group is subject to the following restrictions.

1. The compare function cannot be used together with the self-diagnosis function or double trigger mode. (The compare function is not available for the ADRD, ADDBLDR, ADDBLDRA, and ADDBLDRB registers.)
2. It is necessary to specify single scan mode when using match or mismatch event outputs.
3. When the temperature sensor or internal reference voltage is selected for window A, window B operations are disabled.
4. When the temperature sensor or internal reference voltage is selected for window B, window A operations are disabled.
5. It is not possible to set the same channel for window A and window B.
6. It is necessary to set the reference voltage values such that the high-side reference voltage value is equal to or larger than the low-side reference voltage value.

4.1.4 Initialization of Port Direction Register (PDR)

The method of initializing the PDR register differs between the RX660 Group and RX66T Group, even on products with the same pin count.

4.1.5 MTIOC Pin Output Level when Counter Stops

To generate PWM waveforms in complementary PWM mode on the RX660 Group, MTU4.TGRA (MTU7.TGRA) compare match detection is performed with not only MTU4.TCNT (MTU7.TCNT) but also with MTU3.TCNT (MTU6.TCNT) or TCNTSA (TCNTSB). Therefore, TRGA4N (TRGA7N) is also generated when a compare match with MTU3.TCNT (MTU6.TCNT) or TCNTSA (TCNTSB) occurs. When operating MTU3 and MTU4 (MTU6 and MTU7) in complementary PWM mode to generate A/D conversion start requests, use compare match between MTU4.TCNT (MTU7.TCNT) and MTU4.TADCORA or TADCORB (MTU7.TADCORA or TADCORB) as the A/D conversion start request.

4.1.6 A/D Conversion Start Requests in Complementary PWM Mode

To generate PWM waveforms in complementary PWM mode on the RX660 Group, MTU4.TGRA (MTU7.TGRA) compare match detection is performed with not only MTU4.TCNT (MTU7.TCNT) but also with MTU3.TCNT (MTU6.TCNT) or TCNTSA (TCNTSB). Therefore, TRGA4N (TRGA7N) is also generated when a compare match with MTU3.TCNT (MTU6.TCNT) or TCNTSA (TCNTSB) occurs. When operating MTU3 and MTU4 (MTU6 and MTU7) in complementary PWM mode to generate A/D conversion start requests, use compare match between MTU4.TCNT (MTU7.TCNT) and MTU4.TADCORA or TADCORB (MTU7.TADCORA or TADCORB) as the A/D conversion start request.

4.1.7 Pulse Width of Count Clock Source

The pulse width of the MTU's count clock source differs between the RX66T Group and RX660 Group. For details, refer to Table 4.1. Correct operation cannot be achieved if the pulse width is less than the appropriate value listed below.

Table 4.1 Comparative Overview of Serial Communications Interfaces

Item		RX66T	RX660
Single edge		1.5 or more PCLK cycles	3 PCLKA
Both edges		2.5 or more PCLK cycles	5 PCLKA
Phase counting mode	Phase difference and overlap	1.5 or more PCLK cycles	3 PCLKA
	Pulse width	2.5 or more PCLK cycles	5 PCLKA

4.1.8 High-Impedance Control of Unselected MTU Pins

On the RX660 Group, when high-impedance control is enabled for MTU pins in the POECR1 or POECR2 register and the control conditions are met, output on the pins multiplexed with the MTU function enters the high-impedance state regardless of whether or not the MTU function is selected.

To prevent pin output from entering the high-impedance state unexpectedly, make settings such that the MTU pins selected in the PmnPFS register of the MPC and the MTU pins selected in the pin selection register of the POE3 match.

4.1.9 A/D Scan Conversion End Interrupt Generation

On the RX660 Group, when a scan is started by a software trigger and the ADIE bit has been set to 1, an A/D scan conversion end interrupt is generated when the scan ends, even if double trigger mode is selected.

4.1.10 Input Buffer Control by DIRQnE Bits (n = 0 to 15)

On the RX660 Group, setting a DPSIERy.DIRQnE (y = 0 or 1, n = 0 to 15) bit to 1 enables the input buffer of the corresponding pin among IRQ0-DS to IRQ15-DS. Note that once the input buffer is enabled, inputs on these pins are sent to the corresponding DPSIFRy.DIRQnF (y = 0 or 1, n = 0 to 15) bits, but they are not sent to the interrupt controller, peripheral modules, and I/O ports.

4.1.11 Scan Conversion Time of 12-Bit A/D Converter#

The scan conversion time differs between the RX66T Group and RX660 Group. The scan conversion time (t_{SCAN}) for each group of a single scan where the number of selected channels is n is expressed by the equations below. For details, refer to the description of the 12-bit A/D converter analog input sampling time and scan conversion time in the User's Manual: Hardware of the RX66T Group and RX660 Group, listed in section 5, Reference Documents.

RX66T: $t_{SCAN} = t_D + t_{SPLSH} + (t_{DIS} \times n) + t_{DIAG} + (t_{CONV} \times n) + t_{ED}$

t_{SCAN} (when converting temperature sensor output or internal reference voltage) $= t_D + (t_{ADIS} \times m) + (t_{CONV} \times m) + t_{ED}$

RX660: $t_{SCAN} = t_D + (t_{DIS} \times n) + t_{DIAG} + (t_{CONV} \times n) + t_{ED}$

t_{SCAN} (when converting temperature sensor output or internal reference voltage) $= t_D + (t_{ADIS} \times m) + (tC_{ONV} \times m) + t_{ED}$

t_D	Start-of-scanning-delay time
t_{SPLSH}	Channel-dedicated sample and hold circuit processing time
t_{SPL}	Sampling time
t_{DIS}	Disconnection detection assist processing time
t_{DIAG}	Self-diagnosis A/D conversion processing time
t_{CONV}	A/D conversion processing time
t_{ED}	End-of-scanning-delay time
t_{ADIS}	Auto-discharge processing time during A/D conversion of temperature sensor output and internal reference voltage

4.1.12 D/A Converter Settings

When configuring D/A converter settings on the RX660 Group, first set comparator C as the output destination in the D/A destination select register (DADSELR) and wait for the D/A converter output to stabilize before enabling comparator operation. Similarly, stop the comparator temporarily before making changes to the settings of the D/A converter, then wait for the D/A converter output to stabilize before enabling comparator operation.

4.1.13 Comparator C Operation in Module Stop State

On the RX660 Group the analog circuits of comparator C do not stop operating if a transition to the module stop state is made while comparator C is operating, so the analog power current associated with comparator C remains unchanged. If it is necessary to reduce analog power current consumption in the module stop state, stop operation of comparator C by clearing the CMPCTL.HCMPON bit to 0.

4.1.14 Comparator C Operation in Software Standby Mode

On the RX660 Group, the analog circuits of comparator C do not stop operating if a transition to software standby mode is made while comparator C is operating, so the analog power current associated with comparator C remains unchanged. If it is necessary to reduce analog power current consumption in software standby mode, stop operation of comparator C by clearing the CMPCTL.HCMPON bit to 0.

4.1.15 Timer Mode Register Setting for ELC Event Input

To set the MTU to ELC action operation on the RX660 Group, set the timer mode register (TMDR) of the relevant channel to its initial value (00h).

4.1.16 Clock Frequency Settings

On the RX66T Group the value of the MEMWAIT register must be changed if the ICLK frequency exceeds 120 MHz.

Note that the following restrictions apply when using CANFD with the RX660 group.

Clock frequency setting restrictions when using CANFD:

PCLKA: PCLKB = 2:1

ICLK ≥ BCLK and PCLKA ≥ PCLKB

5. Reference Documents

User's Manual: Hardware

RX66T Group User's Manual: Hardware Rev1.21 (R01UH0749EJ0121)
(The latest version can be downloaded from the Renesas Electronics website.)

RX660 Group User's Manual: Hardware Rev1.00 (R01UH0937EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This module reflects the content of the following technical updates:

TN-RX*-A0260A/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	May.12.22	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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