RX660 Group, RX630 Group

Differences Between the RX660 Group and the RX630 Group

Introduction

This application note is intended as a reference to points of difference between the peripheral functions, I/O registers, and pin functions of the RX660 Group and RX630 Group, as well as a guide to key points to consider when migrating between the two groups.

Unless specifically otherwise noted, the information in this application note applies to the 144-pin package version of the RX660 Group and the 177-pin package version of the RX630 Group as the maximum specifications. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the User's Manual: Hardware of the products in question.

Target Devices

RX660 Group and RX630 Group

Contents

1. Comparison of Built-In Functions of RX660 Group and RX630 Group

A comparison of the built-in functions of the RX660 Group and RX630 Group is provided below. For details of the functions, see section 2, Comparative Overview of Specifications and section 5, Reference Documents.

Table 1.1 is a Comparison of Built-In Functions of RX660 Group and RX630 Group.

Table 1.1 Comparison of Built-In Functions of RX660 Group and RX630 Group

Function	RX630	RX660
CPU	●/▲	
Operating modes	●/■	
Address space	▲	
Resets	○	
Option-setting memory (OFSM)	●/▲	
Voltage detection circuit (LVDA)	▲	
Clock generation circuit	●/▲/■	
Frequency measuring function (MCK)	○	×
Clock frequency accuracy measurement circuit (CAC)	×	○
Low power consumption	▲	
Battery backup function	○	×
Register write protection function	▲	
Exception Handling	●/▲	
Interrupt controller (ICUb for RX630, and ICUF for RX660)	●/▲	
Buses	●	
Memory-protection unit (MPU)	○	
DMA controller (DMACA for RX630, and DMACAa for RX660)	●/▲	
Data transfer controller (DTCa for RX630, and DTCb for RX660)	●	
Event link controller (ELC)	×	○
I/O ports	▲	
Multi-function pin controller (MPC)	●/▲/■	
Multi-function timer pulse unit 2 (MTU2a for RX630) Multi-function timer pulse unit 3 (MTU3a for RX660)	●/▲	
Port output enable 2 (POE2a for RX630) Port output enable 3 (POE3a for RX660)	▲	
16-bit timer pulse unit (TPUa)	○	×
Programmable pulse generator (PPG)	○	×
8-bit timer (TMR for RX630, and TMRb for RX660)	●	
Compare match timer (CMT)	●	
Compare match timer W (CMTW)	×	○
Realtime clock (RTCa for RX630, and RTCC for RX660)	●	
Watchdog timer (WDTA)	▲	
Independent watchdog timer (IWDTa)	▲	
USB2.0 function module (USBa)	○	×
Serial communications interface (SCIc and SCId for RX630, and SCIk, SCIm, and SCIh for RX660)	●/▲	
Serial communications interface (RSCI)	×	○
I²C bus interface (RIIC for RX630, and RIICa for RX660)	▲	
CAN module (CAN for RX630) CAN FD module (CANFD-Lite for RX660)	●/▲	

Serial peripheral interface (RSPI for RX630, and RSPId for RX660)	●	
CRC calculator (CRC for RX630, and CRCA for RX660)	●	
IEBus™ controller (IEB)	○	×
Remote control signal receiver (REMCa)	×	○
Trigonometric function calculator (TFU)	×	○
12-bit A/D converter (S12ADa for RX630, and S12ADH for RX660)	●/▲	
10-bit A/D converter (ADb)	○	×
D/A converter (DAa for RX630) 12-bit D/A converter (R12DAb for RX660)	●	
Temperature sensor	▲	
Comparator C (CMPC)	×	○
Data operation circuit (DOCA)	×	○
RAM	●/▲	
Flash memory (FLASH)	●/▲	
Packages	●/▲	

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Register specification items that have no differences between the groups are not indicated.

2.1 CPU

Table 2.1 is a Comparative Overview of CPU.

Table 2.1 Comparative Overview of CPU

Item	RX630	RX660
CPU	• Maximum operating frequency: 100 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per clock cycle • Address space: — 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Nine 32-bit registers — Accumulator: One 64-bit register • Basic instructions: 73 • Floating point instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian and big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory-protection unit (MPU)	• Maximum operating frequency: 120 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per clock cycle • Address space: — 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • 113 instructions — Standard provided instructions: 111 Basic instructions: 77 Single-precision floating point instructions: 11 DSP instructions: 23 — Instructions for register bank save function: 2 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian and big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits
FPU	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard
Register bank save function	—	• Fast collective saving and restoration of the values of CPU registers • 16 save register banks

2.2 Operating Modes

Table 2.2 is a Comparative Overview of Operating Modes, and Table 2.3 is a Comparison of Operating Mode Registers.

Table 2.2 Comparative Overview of Operating Modes

Item	RX630	RX660
Operating modes specified by mode setting pins	Single-chip mode	Single-chip mode
	Boot mode	Boot mode (SCI interface)
	User boot mode	User boot mode
	—	Boot mode (FINE interface)
	USB boot mode	—
Operating modes selected by register settings	Single-chip mode	Single-chip mode
	User boot mode	User boot mode
	On-chip ROM disabled extended mode	On-chip ROM disabled extended mode
	On-chip ROM enabled extended mode	On-chip ROM enabled extended mode

Table 2.3 Comparison of Operating Mode Registers

Registers	Bit	RX630	RX660
VOLSR	—	—	Voltage level setting register

2.3 Address Space

Figure 2.1 is a Comparative Memory Map of Single-Chip Mode, Figure 2.2 is a Comparative Memory Map of On-chip ROM Enabled Extended Mode, and Figure2.3 is a Comparative Memory Map of On-chip ROM Disabled Extended Mode.

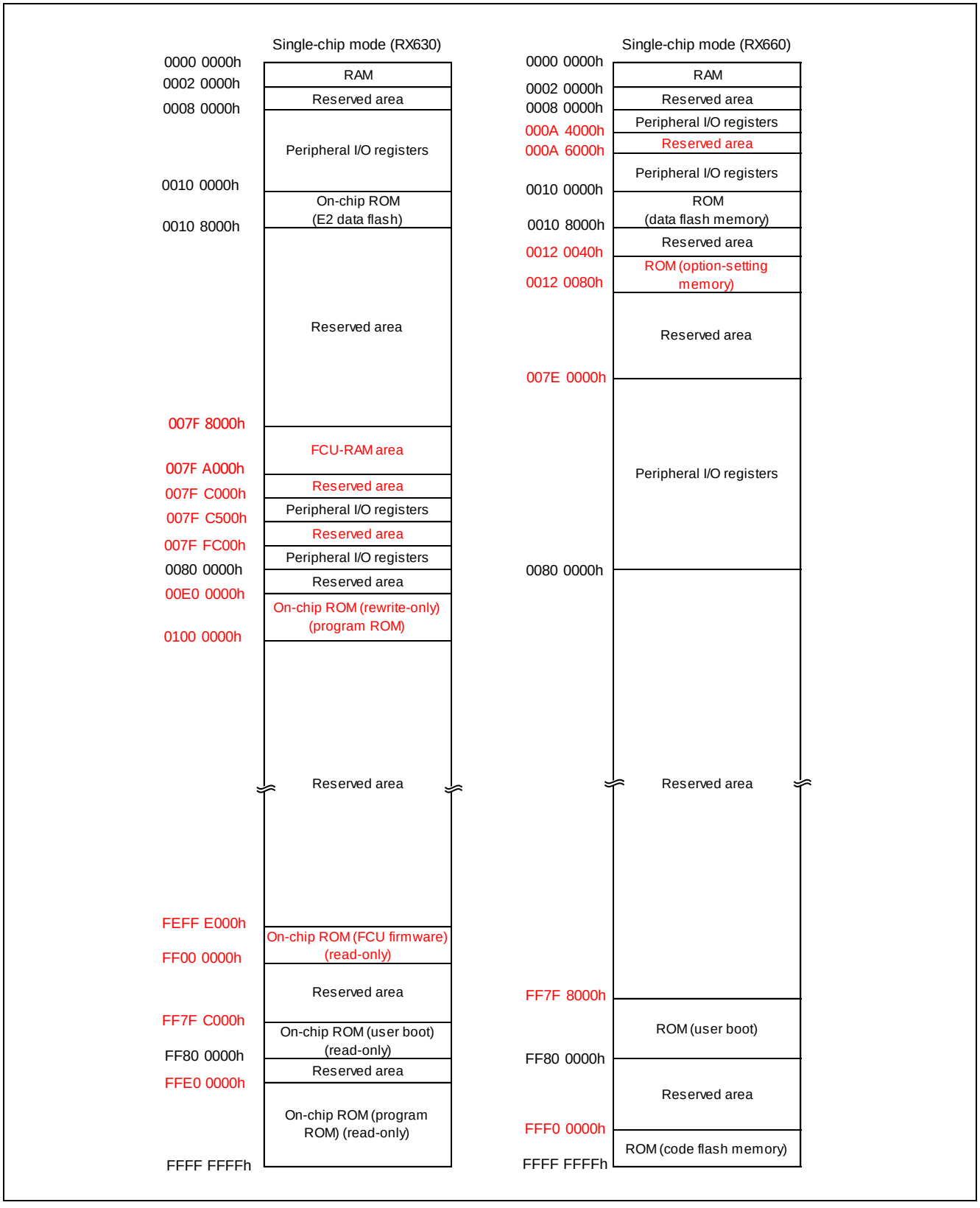

Figure 2.1 Comparative Memory Map of Single-Chip Mode

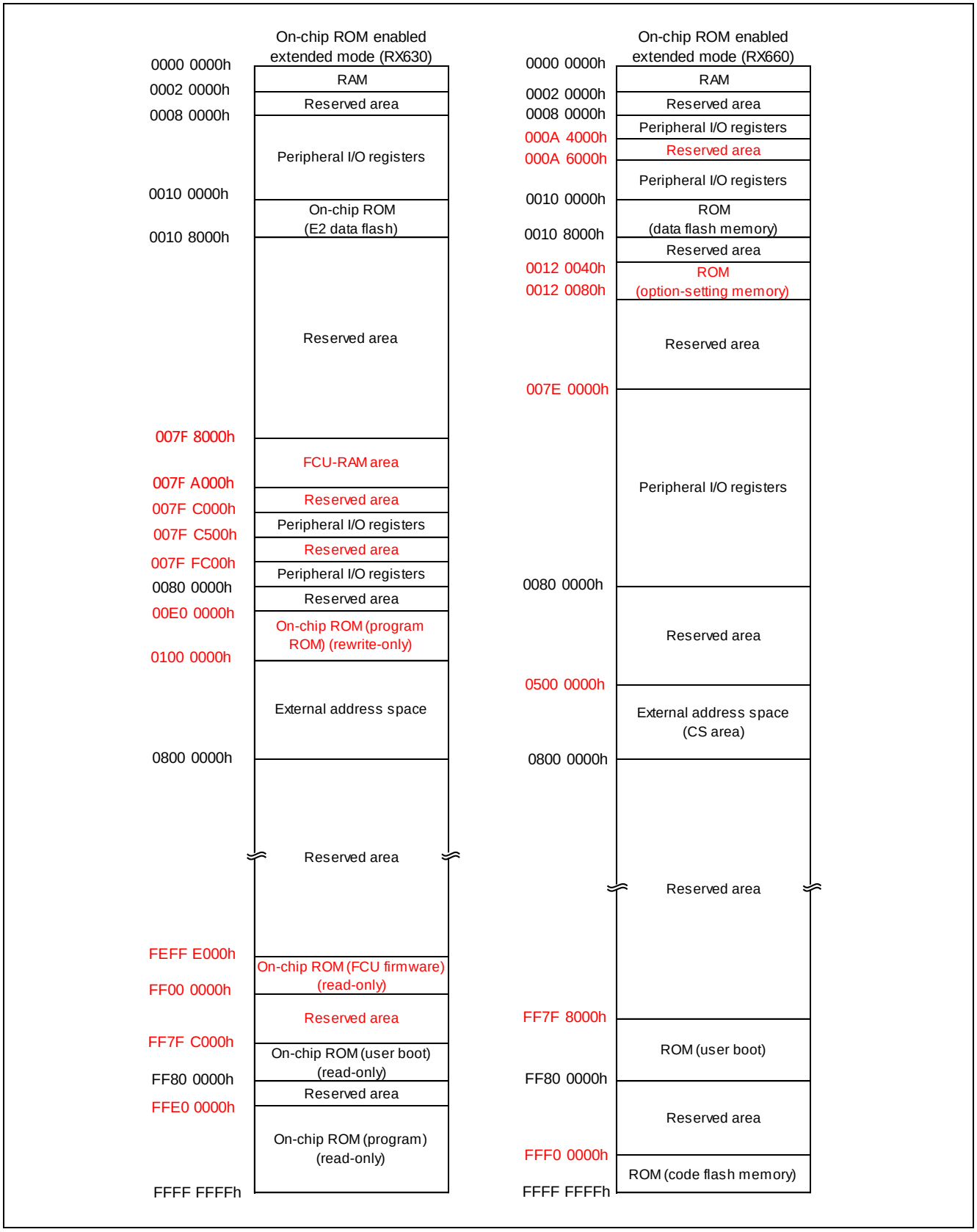

Figure 2.2 Comparative Memory Map of On-chip ROM Enabled Extended Mode

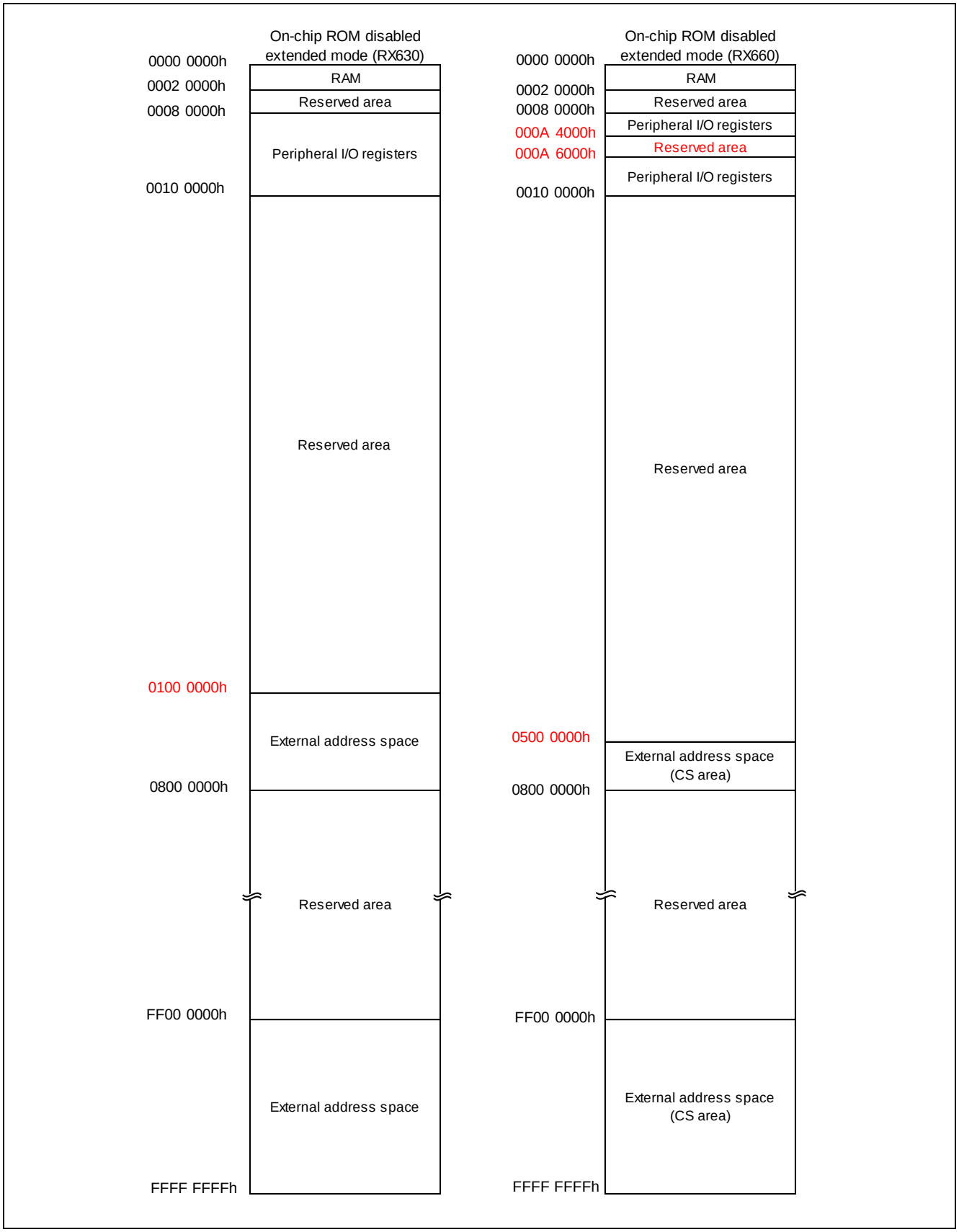

Figure2.3 Comparative Memory Map of On-chip ROM Disabled Extended Mode

2.4 Option-Setting Memory

Figure 2.4 is a Comparison of Option-Setting Memory Areas, and Table 2.4 is a Comparison of Option-Setting Memory Registers.

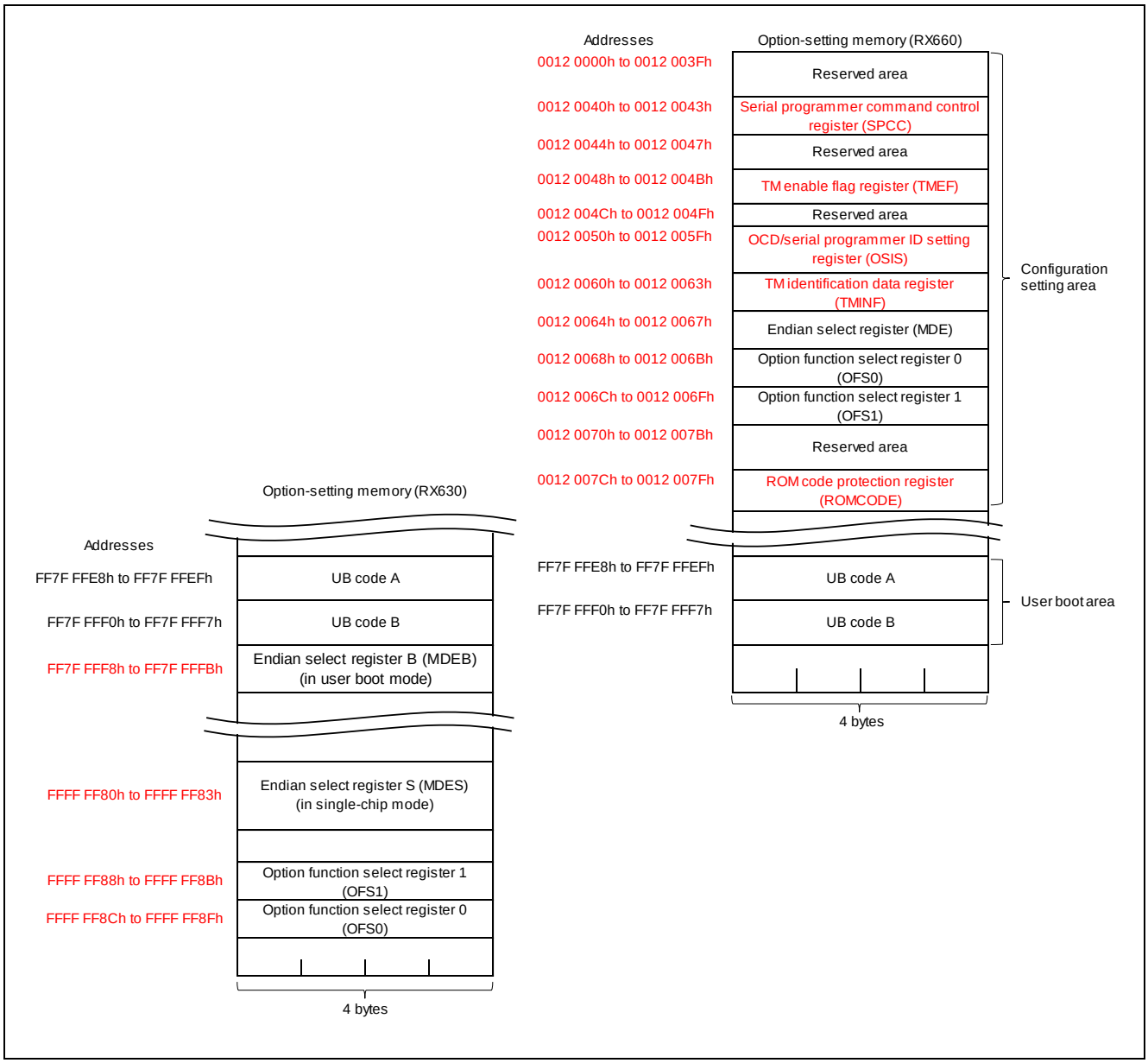

Figure 2.4 Comparison of Option-Setting Memory Areas

Table 2.4 Comparison of Option-Setting Memory Registers

Registers	Bit	RX630	RX660 (OFSM)
SPCC	—	—	Serial programmer command control register
OSIS	—	—	OCD/serial programmer ID setting register
OFS0	IWDTRSTIRQS	IWDT reset interrupt request select bit 0: Non-maskable interrupts are enabled. 1: Resets are enabled.	IWDT reset interrupt request select bit 0: Non-maskable interrupts or interrupt requests are enabled. 1: Resets are enabled.
	WDTRSTIRQS	WDT reset interrupt request select bit 0: Non-maskable interrupts are enabled. 1: Resets are enabled.	WDT reset interrupt request select bit 0: Non-maskable interrupts or interrupt requests are enabled. 1: Resets are enabled.
OFS1	VDSEL[1:0]	—	Voltage detection 0 level select bits
MDEB MDES	—	Endian select register B (in user boot mode) Endian select register S (in single-chip mode)	—
MDE	—	—	Endian select register
TMEF	—	—	TM enable flag register
TMINF	—	—	TM identification data register
ROMCODE	—	—	ROM code protection register

2.5 Voltage Detection Circuit

Table 2.5 is a Comparative Overview of Voltage Detection Circuits, and Table 2.6 is a Comparison of Voltage Detection Circuit Registers.

Table 2.5 Comparative Overview of Voltage Detection Circuits

Item		RX630 (LVDA)			RX660 (LVDA)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	When voltage drops below Vdet0	When voltage rises above or drops past Vdet1	When voltage rises above or drops past Vdet2	When voltage drops below Vdet0	When voltage rises above or drops past Vdet1	When voltage rises above or drops past Vdet2
	Detection voltage	Fixed to one level	Specified by using LVDLVLR.LVD1LVL[3:0] bits	Specified by using LVDLVLR.LVD2LVL[3:0] bits	Selectable from 2 levels by using OFS1.VDSEL[1:0] bits	Selectable from 5 levels using LVDLVLR.LVD1LVL[3:0] bits	Selectable from 5 levels using LVDLVLR.LVD2LVL[3:0] bits
	Monitoring flags	—	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2	—	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2
			LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2DET flag: Vdet2 passage detection		LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2DET flag: Vdet2 passage detection

Item		RX630 (LVDA)			RX660 (LVDA)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
Voltage detection processing	Reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet0 > VCC: CPU restart timing after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable between after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC: CPU restart timing selectable between after specified time with VCC > Vdet2 or Vdet2 > VCC	Reset when Vdet0 > VCC: CPU restart timing after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC: CPU restart timing selectable after specified time with VCC > Vdet2 or Vdet2 > VCC
	Interrupts	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
			Selectable between non-maskable or maskable interrupt	Selectable between non-maskable or maskable interrupt		Selectable between non-maskable or maskable interrupt	Selectable between non-maskable or maskable interrupt
			Interrupt request issued when Vdet1 > VCC, VCC > Vdet1, or both	Interrupt request issued when Vdet2 > VCC, VCC > Vdet2, or both		Interrupt request issued when Vdet1 > VCC, VCC > Vdet1, or both	Interrupt request issued when Vdet2 > VCC, VCC > Vdet2, or both
Digital filter	Enable/ disable switching	No digital filter function	Available	Available	No digital filter function	Available	Available
	Sampling time	—	1/n LOCO frequency × 2 (n: 1, 2, 4, 8)	1/n LOCO frequency × 2 (n: 1, 2, 4, 8)	—	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)
Event link function		—	—	—	—	Available: Event output at Vdet1 passage detection	Available: Event output at Vdet2 passage detection

Table 2.6 Comparison of Voltage Detection Circuit Registers

Register	Bit	RX630 (LVDA)	RX660 (LVDA)
LVD1CR1	LVD1IRQSEL	—	Voltage Monitoring 1 interrupt type select bit
LVD2CR1	LVD2IRQSEL	—	Voltage Monitoring 2 interrupt type select bit
LVDLVLR	LVD1LVL[3:0]	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 1 0 1 0: 2.95 V When writing, settings other than the above are prohibited.	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 1 0 0: 4.57 V (Vdet1_0) 0 1 0 1: 4.47 V (Vdet1_1) 0 1 1 0: 4.32 V (Vdet1_2) 1 0 1 0: 2.93 V (Vdet1_3) 1 0 1 1: 2.88 V (Vdet1_4) Settings other than the above are prohibited.
	LVD2LVL[3:0]	Voltage detection 2 level select bits (Standard voltage during drop in voltage) b7 b4 1 0 1 0: 2.95 V When writing, settings other than the above are prohibited.	Voltage detection 2 level select bits (Standard voltage during drop in voltage) b7 b4 0 1 0 0: 4.57 V (Vdet2_0) 0 1 0 1: 4.47 V (Vdet2_1) 0 1 1 0: 4.32 V (Vdet2_2) 1 0 1 0: 2.93 V (Vdet2_3) 1 0 1 1: 2.88 V (Vdet2_4) Settings other than the above are prohibited.
LVD1CR0	LVD1FSAMP [1:0]	Sampling clock select bits b5 b4 0 0: 1/1 LOCO frequency 0 1: 1/2 LOCO frequency 1 0: 1/4 LOCO frequency 1 1: 1/8 LOCO frequency	Sampling clock select bits b5 b4 0 0: 1/2 LOCO frequency 0 1: 1/4 LOCO frequency 1 0: 1/8 LOCO frequency 1 1: 1/16 LOCO frequency
LVD2CR0	LVD2FSAMP [1:0]	Sampling clock select bits b5 b4 0 0: 1/1 LOCO frequency 0 1: 1/2 LOCO frequency 1 0: 1/4 LOCO frequency 1 1: 1/8 LOCO frequency	Sampling clock select bits b5 b4 0 0: 1/2 LOCO frequency 0 1: 1/4 LOCO frequency 1 0: 1/8 LOCO frequency 1 1: 1/16 LOCO frequency

2.6 Clock Generation Circuit

Table 2.7 is a Comparative Overview of Clock Generation Circuits, and Table 2.8 is a Comparison of Clock Generation Circuit Registers.

Table 2.7 Comparative Overview of Clock Generation Circuits

Item	RX630	RX660
Use	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, ROM, and RAM.	• Generates the system clock (ICLK) to be supplied to the CPU, TFU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the RSPI, SCIm, RSCI, MTU, and CANFD.
	• Generates the peripheral module clock (PCLKB) to be supplied to the peripheral modules.*1	• Generates the peripheral module clock (PCLKB) to be supplied to the peripheral modules. • Generates the peripheral module clock (for analog conversion) (PCLKD) to be supplied to the S12AD.
	• Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the USB clock (UCLK) to be supplied to the USB.	• Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the external bus clock (BCLK) to be supplied to the external bus.
		• Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CANFD clock (CANFDCLK) to be supplied to the CANFD.
	• Generates the CAN clock (CANMCLK) to be supplied to the CAN.	• Generates the CANFD main clock (CANFDMCLK) to be supplied to the CANFD.
	• Generates the IEBUS clock (IECLK) to be supplied to the IEBUS. • Generates the RTC-dedicated sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the RTC-dedicated main clock (RTCMCLK) to be supplied to the RTC.	• Generates the RTC sub-clock (RTCSCLK) to be supplied to the RTC.
		• Generates the REMC sub-clock (REMSCLK) to be supplied to the REMC.
	• Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the JTAG clock (JTAGTCK) to be supplied to the JTAG.	• Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.

Item	RX630	RX660
Operating frequency	• ICLK: 100 MHz (max) • PCLKB: 50 MHz (max) • FCLK: — 4 MHz to 50 MHz (during programming or erasing of the ROM or E2 data flash) — 50 MHz (max) (during reading of E2 data flash) • BCLK: 50 MHz (max) • BCLK pin output: 25 MHz (max) • UCLK: 48 MHz (max) • CANMCLK: 20 MHz (max) • IECLK: 50 MHz (max) • RTCSCLK: 32.768 kHz • RTCMCLK: 4 MHz to 16 MHz • IWDTCLK: 125 kHz • JTAGTCK: 10 MHz (max)	• ICLK: 120 MHz (max) • PCLKA: 120 MHz (max) • PCLKB: 60 MHz (max) • PCLKD: 8 MHz to 60 MHz (when 12-bit A/D converter is operating) • FCLK: — 4 MHz to 60 MHz (during programming or erasing of code flash memory or data flash memory) — 60 MHz (max) (during reading of data flash memory) • BCLK: 60 MHz (max) • BCLK pin output: 40 MHz (max) • CACCLK: Same as clock from respective oscillators • CANFDCLK: 60 MHz (max) • CANFDMCLK: 24 MHz (max) • RTCSCLK: 32.768 kHz • REMCLK: 32.768 kHz • IWDTCLK: 120 kHz
Main clock oscillator	• Resonator frequency: 4 MHz to 16 MHz • External clock input frequency: 20 MHz (max) • Connectable resonator or additional circuit: Ceramic resonator, crystal • Connection pins: EXTAL and XTAL • Oscillation stop detection function: • When a main clock oscillation stop is detected, the system clock source is switched to LOCO and MTU pin can be forcedly driven to high-impedance.	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max) • Connectable resonator or additional circuit: Ceramic resonator, crystal • Connection pins: EXTAL and XTAL • Oscillation stop detection function: • When a main clock oscillation stop is detected, the system clock source is switched to LOCO and MTU pin can be forcedly driven to high-impedance.
Sub-clock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: Crystal • Connection pins: XCIN and XCOUT	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: Crystal • Connection pins: XCIN and XCOUT
PLL circuit (RX630) PLL frequency synthesizer (RX660)	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 16 MHz • Frequency multiplication ratio: Selectable from 8, 10, 12, 16, 20, 24, 25, and 50 • Oscillation frequency: 104 MHz to 200 MHz	• Input clock source: Main clock, HOCO • Input pulse frequency division ratio: Selectable from 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable from 10 to 30 • Output clock frequency of PLL frequency synthesizer: 120 MHz to 240 MHz

Item	RX630	RX660
High-speed on-chip oscillator (HOCO)	• Oscillation frequency: 50 MHz • HOCO power supply control	• Oscillation frequency: Selectable from 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control • FLL function (Not available on products without a sub-clock oscillator.)
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 125 kHz	Oscillation frequency: 240 kHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 125 kHz	Oscillation frequency: 120 kHz
JTAG external clock input (TCK)	Input clock frequency: 10 MHz (max)	—
BCLK pin output control function	• Selectable between BCLK clock output or high-level output. • Output clock selectable between BCLK or BCLK/2.	• Selectable between BCLK clock output or high-level output. • Output clock selectable between BCLK or BCLK/2.
Event link function (output)	—	Detection of stopping of the main clock oscillator
Event link function (input)	—	Switching of the clock source to the low-speed on-chip oscillator

Note: 1. On the RX630 Group, PCLKB = PCLK.

Table 2.8 Comparison of Clock Generation Circuit Registers

Register	Bit	RX630	RX660
SCKCR	PCKD[3:0]	—	Peripheral module clock D (PCLKD) select bits
	PCKA[3:0]	—	Peripheral module clock A (PCLKA) select bits
SCKCR2	IEBCK[3:0]	IEBUS clock (IECLK) select bits	—
	UCK[3:0]	USB clock (UCLK) select bits	—
	CFDCK [3:0]	—	CANFD clock (CANFDCLK) select bits
PLLCR	PLIDIV[1:0]	PLL input frequency division ratio select bits b1 b0 0 0: x1/1 0 1: x1/2 1 0: x1/4 1 1: Setting prohibited.	PLL input frequency division ratio select bits b1 b0 0 0: x1/1 0 1: x1/2 1 0: x1/3 1 1: Setting prohibited.
	PLLSRCSEL	—	PLL clock source select bit
	STC[5:0]	Frequency multiplication factor setting bits b13 b8 0 0 0 1 1 1: ×8 0 0 1 0 0 1: ×10 0 0 1 0 1 1: ×12 0 0 1 1 1 1: ×16 0 1 0 0 1 1: ×20 0 1 0 1 1 1: ×24 0 1 1 0 0 0: ×25	Frequency multiplication factor setting bits b13 b8 0 1 0 0 1 1: ×10.0 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11.0 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12.0 0 1 1 0 0 0: ×12.5 0 1 1 0 0 1: ×13.0 0 1 1 0 1 0: ×13.5 0 1 1 0 1 1: ×14.0 0 1 1 1 0 0: ×14.5 0 1 1 1 0 1: ×15.0 0 1 1 1 1 0: ×15.5 0 1 1 1 1 1: ×16.0 1 0 0 0 0 0: ×16.5 1 0 0 0 0 1: ×17.0 1 0 0 0 1 0: ×17.5 1 0 0 0 1 1: ×18.0 1 0 0 1 0 0: ×18.5 1 0 0 1 0 1: ×19.0 1 0 0 1 1 0: ×19.5 1 0 0 1 1 1: ×20.0 1 0 1 0 0 0: ×20.5 1 0 1 0 0 1: ×21.0 1 0 1 0 1 0: ×21.5 1 0 1 0 1 1: ×22.0 1 0 1 1 0 0: ×22.5 1 0 1 1 0 1: ×23.0 1 0 1 1 1 0: ×23.5 1 0 1 1 1 1: ×24.0

Register	Bit	RX630	RX660
PLLCR	STC[5:0]	1 1 0 0 0 1: ×50 Settings other than the above are prohibited.	1 1 0 0 0 0: ×24.5 1 1 0 0 0 1: ×25.0 1 1 0 0 1 0: ×25.5 1 1 0 0 1 1: ×26.0 1 1 0 1 0 0: ×26.5 1 1 0 1 0 1: ×27.0 1 1 0 1 1 0: ×27.5 1 1 0 1 1 1: ×28.0 1 1 1 0 0 0: ×28.5 1 1 1 0 0 1: ×29.0 1 1 1 0 1 0: ×29.5 1 1 1 0 1 1: ×30.0 Settings other than the above are prohibited.
HOCOCR2	—	—	High-speed on-chip oscillator control register 2
FLLCR1	—	—	FLL control register 1
FLLCR2	—	—	FLL control register 2
OSCOVFSR	—	—	Oscillation stabilization flag register
MOSCWTCR	MSTS[4:0] (RX630) MSTS[7:0] (RX660)	Main clock oscillator wait time setting bits b4 b0 0 0 0 0 0: Waiting time = 2 cycles 0 0 0 0 1: Waiting time = 4 cycles 0 0 0 1 0: Waiting time = 8 cycles 0 0 0 1 1: Waiting time = 16 cycles 0 0 1 0 0: Waiting time = 32 cycles 0 0 1 0 1: Waiting time = 64 cycles 0 0 1 1 0: Waiting time = 512 cycles 0 0 1 1 1: Waiting time = 1024 cycles 0 1 0 0 0: Waiting time = 2048 cycles 0 1 0 0 1: Waiting time = 4096 cycles 0 1 0 1 0: Waiting time = 16384 cycles 0 1 0 1 1: Waiting time = 32768 cycles 0 1 1 0 0: Waiting time = 65536 cycles 0 1 1 0 1: Waiting time = 131072 cycles 0 1 1 1 0: Waiting time = 262144 cycles 0 1 1 1 1: Waiting time = 524288 cycles Settings other than the above are prohibited.	The setting of the MSTS[7:0] bits is calculated with the following formula using the maximum frequency of fLOCO to ensure that the wait time is equal to or longer than the oscillation stabilization time of the main clock. MSTS[7:0] > [tMAINOSC × (fLOCO_max) + 16] / 32 (tMAINOSC: Main clock oscillation stabilization time, fLOCO_max: Maximum fLOCO frequency)
SOSCWTCR	—	—	Sub-clock oscillator wait control register
SOFCR	—	—	Sub-clock oscillator forced oscillation control register
MOFCR	MOFXIN	Main clock oscillator forced oscillation bit	—
	MODRV2 [1:0]	—	Sub-clock oscillator drivability 2 switch bits
	MOSEL	—	Main clock oscillator switch bit

2.7 Low Power Consumption

Table 2.9 is a Comparative Overview of Low Power Consumption Functions, Table 2.10 is a Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode, and Table 2.11 is a Comparison of Low Power Consumption Registers.

Table 2.9 Comparative Overview of Low Power Consumption Functions

Item	RX630	RX660
Reducing power consumption by switching clock signals	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKB), external bus clock (BCLK), and flash interface clock (FCLK).	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, and PCLKD), external bus clock (BCLK), and flash interface clock (FCLK).
BCLK output control function	Selectable from BCLK output and high-level output	Selectable from BCLK output and high-level output
Module stop function	Each peripheral module can be stopped independently.	Each peripheral module can be stopped independently.
Function for transition to low power consumption mode	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.
Low power consumption modes	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode
Function for lower operating power consumption	• Power consumption can be reduced in normal operation, sleep mode, and all-module clock stop mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Three operating power control modes are available — High-speed operating mode — Low-speed operating mode 1 — Low-speed operating mode 2	—

Table 2.10 Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX630	RX660
Sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupts	Interrupts
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM	Operation possible (retained)	Operation possible (retained)
	Flash memory	Operation	Operation
	USB2.0 function module (USB)	Operation possible	—
	Watchdog timer (WDT)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	Port output enable (POE)	—	Operation possible
	Remote control signal receiver (REMC)	—	Operation possible
	8-bit timer (unit 0, unit 1)	Operation possible	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral module	Operation possible	Operation possible
	I/O ports	Operation	Operation
All-module clock stop mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupts	Interrupts
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	USB2.0 function module (USB)	Stopped	—
	Watchdog timer (WDT)	Stopped (retained)	Stopped (retained)

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX630	RX660
All-module clock stop mode	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	Port output enable (POE)	—	Operation possible
	Remote control signal receiver (REMC)	—	Operation possible
	8-bit timer (unit 0, unit 1)	Operation possible	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral module	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained
Software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupts	Interrupts
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Stopped
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Stopped
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Stopped	Stopped
	CPU	Stopped (retained)	Stopped (retained)
	RAM	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	USB2.0 function module (USB)	Stopped	—
	Watchdog timer (WDT)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	Port output enable (POE)	—	Stopped (retained)
	Remote control signal receiver (REMC)	—	Operation possible
	8-bit timer (unit 0, unit 1)	Stopped (retained)	Stopped (retained)
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral module	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained
Deep software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupts	Interrupts
	State after cancellation	Program execution state (reset processing)	Program execution state (reset processing)
	Main clock oscillator	Operation possible	Stopped
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Stopped
	IWDT-dedicated on-chip oscillator	Stopped (undefined)	Stopped (undefined)

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX630	RX660
Deep software standby mode	PLL	Stopped	Stopped
	CPU	Stopped (undefined)	Stopped (undefined)
	RAM	Stopped (retained or undefined)*1	Stopped (undefined)
	Flash memory	Stopped (retained)	Stopped (retained)
	USB2.0 function module (USB)	Stopped (retained or undefined)*2	—
	Watchdog timer (WDT)	Stopped (undefined)	Stopped (undefined)
	Independent watchdog timer (IWDT)	Stopped (undefined)	Stopped (undefined)
	Realtime clock (RTC)	Operation possible	Operation possible
	Port output enable (POE)	—	Stopped (undefined)
	Remote control signal receiver (REMC)	—	Stopped (undefined)
	8-bit timer (unit 0, unit 1)	Stopped (undefined)	Stopped (undefined)
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral module	Stopped (undefined)	Stopped (undefined)
	I/O ports	Retained	Retained

“Operation possible” means that whether the state is operating or stopped is controlled by the control register setting.
“Stopped (retained)” means that internal register values are retained and internal operations are suspended.
“Stopped (undefined)” means that internal register values are undefined and power is not supplied to the internal circuit.

Notes: 1. Whether the state is retained or undefined can be selected by the setting of the deep cut bits (DEEPCUT[1:0]) in the deep standby control register (DPSBYCR).
2. Whether to enable or disable the USB resume detection function can be controlled by the setting of the deep cut bits (DEEPCUT[1:0]) in the deep standby control register (DPSBYCR) When the USB resume detection function is enabled, the values of the registers in the USB resume detecting unit are only retained even in deep software standby mode.

Table 2.11 Comparison of Low Power Consumption Registers

Register	Bit	RX630	RX660
MSTPCRA	MSTPA0	—	Compare match timer W (unit 1) module stop bit
	MSTPA1	—	Compare match timer W (unit 0) module stop bit
	MSTPA4	—	8-bit timer 3 or 2 (unit 1) module stop bit
	MSTPA5	—	8-bit timer 1 or 0 (unit 0) module stop bit
	MSTPA9	Multi-function timer pulse unit module stop bit Target modules: MTU0 to MTU5 0: Cancellation of the module stop state 1: Transition to the module stop state	Multi-function timer pulse unit 3 module stop bit Target module: MTU3 0: Cancellation of the module stop state 1: Transition to the module stop state
	MSTPA10	Programmable pulse generator (unit 1) module stop bit	—
	MSTPA11	Programmable pulse generator (unit 0) module stop bit	—
	MSTPA12	16-bit timer pulse unit 1 (unit 1) module stop bit	—
	MSTPA13	16-bit timer pulse unit 0 (unit 0) module stop bit	—
	MSTPA19	D/A converter module stop bit	12-bit D/A converter module stop bit
	MSTPA23	10-bit A/D converter module stop bit	—
MSTPCRB	MSTPB0	CAN module stop bit	—
	MSTPB1	CAN module 1 module stop bit	—
	MSTPB2	CAN module 2 module stop bit	—
	MSTPB6	—	Data operation circuit module stop bit
	MSTPB8	ELC module stop bit	—
	MSTPB9	—	Event link controller module stop bit
	MSTPB10	—	Comparator C module stop bit
	MSTPB16	Serial peripheral interface 1 module stop bit	—
	MSTPB19	Universal serial bus interface (port 0) module stop bit	—
	MSTPB20	I^2C bus interface 1 module stop bit	—
MSTPCRC	MSTPC0	RAM module stop bit Target module: RAM (0000 0000h to 0000 FFFFh)	RAM module stop bit Target module: RAM (0000 0000h to 0001 FFFFh)
	MSTPC1	RAM1 module stop bit	—
	MSTPC16	I^2C bus interface 3 module stop bit	—
	MSTPC18	IEBUS module stop bit	—
	MSTPC19	Frequency measuring function module stop bit	CAC module stop bit
	MSTPC22	Serial peripheral interface 2 module stop bit	—
MSTPCRD	—	—	Module stop control register D
OPCCR	—	Operating power control register	—

Register	Bit	RX630	RX660
MOSCWTCR	—	Main clock oscillator wait control register	—
SOSCWTCR	—	Sub-clock oscillator wait control register	—
PLLWTCR	—	PLL wait control register	—
DPSBYCR	DEEPCUT [1:0]	Deep cut bit	—
DPSIER2	DRIICDIE	SDA2-DS deep-standby cancellation signal enable bit	—
	DRIICCIE	SCL2-DS deep-standby cancellation signal enable bit	—
	DUSBIE	USB suspend/resume deep-standby cancellation signal enable bit	—
DPSIER3	—	Deep standby interrupt enable register 3	—
DPSIFR2	DRIICDIF	SDA2-DS deep-standby cancellation flag	—
	DRIICCIF	SCL2-DS deep-standby cancellation flag	—
	DUSBIF	USB suspend/resume deep-standby cancellation flag	—
DPSIFR3	—	Deep standby interrupt flag register 3	—
DPSIEGR2	DRIICDEG	SDA2-DS edge select bit	—
	DRIICCEG	SCL2-DS edge select bit	—
DPSIEGR3	—	Deep standby interrupt edge register 3	—

2.8 Register Write Protection Function

Table 2.12 is a Comparative Overview of Register Write Protection Functions.

Table 2.12 Comparative Overview of Register Write Protection Functions

Item	RX630	RX660
PRC0 bit	• Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR	• Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, FLLCR1, FLLCR2, OSTDCR, OSTDSR
PRC1 bit	• Registers related to the operating modes: SYSCR0, SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR, RSTCKCR, MOSCWTCR, SOSCWTCR, PLLWTCR, DPSBYCR, DPSIER0 to 3 DPSIFR0 to 3, DPSIEGR0 to 3 • Registers related to the clock generation circuit: MOFCR, HOCOPCR • Software reset register: SWRR	• Registers related to the operating modes: SYSCR0, SYSCR1, VOLSR • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, RSTCKCR, DPSBYCR, DPSIER0 to 2, DPSIFR0 to 2, DPSIEGR0 to 2 • Registers related to the clock generation circuit: MOSCWTCR, SOSCWTCR, MOFCR, SOFCR, HOCOPCR • Software reset register: SWRR
PRC3 bit	• Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	• Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

2.9 Exception Handling

Table 2.13 is a Comparative Overview of Exception Handling, Table 2.14 is a Vector Comparison, and Table 2.15 is a Comparison of Instructions to Return from Exception Handling Routines.

Table 2.13 Comparative Overview of Exception Handling

Item	RX630	RX660
Exception event	• Undefined instruction exception • Privileged instruction exception • Access exception • Floating-point exception • Reset • Non-maskable interrupts • Interrupts • Unconditional trap	• Undefined instruction exception • Privileged instruction exception • Access exception • Single-precision floating-point exception • Reset • Non-maskable interrupts • Interrupts • Unconditional trap

Table 2.14 Vector Comparison

Item		RX630	RX660
Undefined instruction exception		Fixed vector table	Exception vector table (EXTB)
Privileged instruction exception		Fixed vector table	Exception vector table (EXTB)
Access exception		Fixed vector table	Exception vector table (EXTB)
Floating-point exception		Fixed vector table	Exception vector table (EXTB)
Reset		Fixed vector table	Exception vector table (EXTB)
Non-maskable interrupts		Fixed vector table	Exception vector table (EXTB)
Interrupts	Fast interrupt	FINTV	FINTV
	Other than fast interrupt	Variable vector table (INTB)	Interrupt vector table (INTB)
Unconditional trap		Variable vector table (INTB)	Interrupt vector table (INTB)

Table 2.15 Comparison of Instructions to Return from Exception Handling Routines

Item		RX630	RX660
Undefined instruction exception		RTE	RTE
Privileged instruction exception		RTE	RTE
Access exception		RTE	RTE
Floating-point exception		RTE	RTE
Reset		Return is not possible.	Return is not possible.
Non-maskable interrupts		Prohibited	Prohibited
Interrupts	RTFI	RTFI	RTFI
	RTE	RTE	RTE
Unconditional trap		RTE	RTE

2.10 Interrupt Controller

Table 2.16 is a Comparative Overview of Interrupt Controllers, and Table 2.17 is a Comparison of Interrupt Controller Registers.

Table 2.16 Comparative Overview of Interrupt Controllers

Item		RX630 (ICUb)	RX660 (ICUF)
Interrupts	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection Edge detection or level detection — The detection method is fixed for each source of connected peripheral modules. • Group interrupt functions: Multiple interrupts are allocated to one interrupt vector. — Number of edge detection interrupt groups: 7 (group 0 to 6) — Number of level detection interrupt groups: 1 (group 12)	• Interrupts from peripheral modules • Interrupt detection method: Edge detection or level detection (fixed for each interrupt source) • Group interrupt: Multiple interrupt sources are grouped together and treated as a single interrupt source.*1 — Group IE0 interrupt: Interrupt sources of coprocessors that use ICLK as the operating clock (edge detection) — Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) — Group BL0/BL1/BL2 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) — Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt B: Any of the interrupt sources for peripheral modules that use PCLKB as the operating clock can be assigned to interrupt vector numbers 128 to 207. • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.

Item		RX630 (ICUb)	RX660 (ICUF)
Interrupts	Peripheral function interrupts	• Unit select function: Either of two interrupt requests is selected. — Number of units: 6	—
	External pin interrupts	• Interrupts from IRQ0 to IRQ15 pins • Number of sources: 16 • Interrupt detection: Detection of low level, falling edge, rising edge, or rising and falling edges can be set for each source. • Digital filter function: Provided	• Interrupts by input signals on IRQi pins (i = 0 to 15) • Interrupt detection: Detection of low level, falling edge, rising edge, or rising and falling edges can be set for each source. • A digital filter can be used to remove noise.
	Software interrupts	• Interrupts generated by writing to a register • Number of sources: 1	• An interrupt request can be generated by writing to a register. • Number of sources: 2
	Interrupt priority level	The priority is set with the register.	The priority level is set with the interrupt source priority register r (IPRr) (r = 000 to 255).
	Fast interrupt function	Speeding up the CPU interrupt processing is possible. This setting is used for one interrupt source only.	It is possible to reduce the CPU's interrupt response time. This setting can be used for one interrupt source only.
	DTC and DMAC control	The DTC and DMAC can be activated by an interrupt source.	The DTC and DMAC can be activated by an interrupt source.
Non-maskable interrupts	NMI pin interrupt	• Interrupt from NMI pins • Interrupt detection: — Falling edge — Rising edge • Digital filter function: Provided	• Interrupt by the input signal on the NMI pin • Interrupt detection: — Falling edge — Rising edge • A digital filter can be used to remove noise.
	Oscillation stop detection	Interrupt at detection of oscillation stop	Interrupt at detection of main clock oscillation stop
	WDT underflow/refresh error interrupt	Interrupt occurs when the down counter underflows or a refresh error occurs.	Interrupt occurs when the watchdog timer underflows or a refresh error occurs.
	IWDT underflow/refresh error interrupt	Interrupt occurs when the down counter underflows or a refresh error occurs.	Interrupt occurs when the independent watchdog timer underflows or a refresh error occurs.
	Voltage monitoring 1 interrupt	Voltage monitoring interrupt of voltage detection circuit 1 (LVD1)	Interrupt from voltage detection circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Voltage monitoring interrupt of voltage detection circuit 2 (LVD2)	Interrupt from voltage detection circuit 2 (LVD2)
	RAM error interrupt	—	Interrupt occurs when a parity check error is detected in the RAM.

Item		RX630 (ICUb)	RX660 (ICUF)
Return from low power consumption state	Sleep mode	Exit sleep mode by a non-maskable interrupt or any other interrupt source.	Exit sleep mode by any interrupt source.
	All-module clock stop mode	Exit all-module clock stop mode by non-maskable interrupt, IRQ0 to IRQ15 interrupt, TMR interrupt, USB resume interrupt, or RTC alarm/period interrupt.	Exit all-module clock stop mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection interrupt, RTC alarm, RTC period, IWDT, REMC interrupt, or software configurable interrupt 146 to 157).
	Software standby mode	Exit software standby mode by non-maskable interrupt, IRQ0 to IRQ15 interrupt, USB resume interrupt, or RTC alarm/period interrupt.	Exit software standby mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, RTC alarm, RTC period, IWDT, or REMC interrupt).
	Deep software standby mode	—	Exit deep software standby mode by NMI pin interrupt, any among a subset of external pin interrupts, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, RTC alarm, or RTC period).

Note: 1. Groups to which no interrupt sources are assigned are reserved. No register corresponds to these groups.

Table 2.17 Comparison of Interrupt Controller Registers

Register	Bit	RX630 (ICUb)	RX660 (ICUF)
IPRn*1 (RX630) IPRr (RX660)	—	Interrupt source priority register n (n = 000 to 253)	Interrupt source priority register r (r = 000 to 255)
SWINTR2R	—	—	Software interrupt 2 startup register
DTCERn*2	DTCE	DTC transfer enable bit (n = 027 to 251)	DTC transfer enable bit (n = 026 to 255)
NMISR	RAMST	—	RAM error interrupt status flag
NMIER	RAMEN	—	RAM error interrupt enable bit
GRPm	—	Group m interrupt source register (m = 00 to 06, 12)	—
GRPBL0 GRPBL1 GRPBL2	—	—	Group BL0/BL1/BL2 interrupt request register
GRPAL0	—	—	Group AL0 interrupt request register
GENm	—	Group m interrupt enable register (m = 00 to 06, 12)	—
GENBL0 GENBL1 GENBL2	—	—	Group BL0/BL1/BL2 interrupt request enable register
GENAL0	—	—	Group AL0 interrupt request enable register

Register	Bit	RX630 (ICUb)	RX660 (ICUF)
GENm	—	Group m interrupt enable register (m = 00 to 06, 12)	—
GCRm	—	Group m interrupt clear register (m = 00 to 06, 12)	—
SEL	—	Unit select register	—
PIBRk	—	—	Software configurable interrupt B request register k (k = 0h, 1h, 5h, 6h, 8h to Ah, Ch, Dh)
PIARk	—	—	Software configurable interrupt A request register k (k = 0h to 5h, Bh, Ch)
SLIBXRn	—	—	Software configurable interrupt B source select register Xn (n = 128 to 143)
SLIBRn	—	—	Software configurable interrupt B source select register n (n = 144 to 207)
SLIARn	—	—	Software configurable interrupt A source select register n (n = 208 to 255)
SLIPRCR	—	—	Write-protection register for software configurable interrupt source select register

Notes: 1. On the RX630 Group, this is a reserved area when n is 254 or 255.
2. On the RX630 Group, this is a reserved area when n is 252 to 255.

2.11 Buses

Table 2.18 is a Comparative Overview of Buses, and Table 2.19 is a Comparison of Bus Registers.

Table 2.18 Comparative Overview of Buses

Item		RX630	RX660
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM or code flash memory) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM or code flash memory) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	• Connected to RAM	• Connected to RAM
	Memory bus 2	• Connected to ROM	• Connected to code flash memory
Internal main buses	Internal main bus 1	• Connected to CPU • Operates in synchronization with the system clock (ICLK)	• Connected to CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DTC and DMAC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the DTC and DMAC • Connected to on-chip memory (RAM or code flash memory) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (TFU, DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 3	• Connected to the peripheral module (USB) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (DOC, REMC, CANFD, and CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 4	Reserved area	• Connected to peripheral modules (MTU, RSPI, and SCIi) • Operates in synchronization with the peripheral-module clock (PCLKA)

Item		RX630	RX660
Internal peripheral buses	Internal peripheral bus 5	Reserved area	• Connected to peripheral modules (RSCI and CANFD) • Operates in synchronization with the peripheral-module clock (PCLKA)
	Internal peripheral bus 6	• Connected to ROM (in P/E) and data flash • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to code flash memory (in P/E) and data flash • Operates in synchronization with the FlashIF clock (FCLK)
External bus	CS area	• Connected to an external device • Operates in synchronization with the external bus clock (BCLK)	• Connected to an external device • Operates in synchronization with the external bus clock (BCLK)

Table 2.19 Comparison of Bus Registers

Register	Bit	RX630	RX660
CSnCR	—	CSn control register (n = 0 to 7)	CSn control register (n = 0 to 3)
	BSIZE[1:0]	External bus width select bits b5 b4 0 0: 16-bit bus space is set. 0 1: 32-bit bus space is set. 1 0: 8-bit bus space is set. 1 1: Setting prohibited.	External bus width select bits b5 b4 0 0: 16-bit bus space is set. 0 1: Setting prohibited. 1 0: 8-bit bus space is set. 1 1: Setting prohibited.
CSnREC	—	CSn recovery cycle register (n = 0 to 7)	CSn recovery cycle register (n = 0 to 3)
CSnMOD	—	CSn mode register (n = 0 to 7)	CSn mode register (n = 0 to 3)
CSnWCR1	—	CSn wait control register 1 (n = 0 to 7)	CSn wait control register 1 (n = 0 to 3)
CSnWCR2	—	CSn wait control register 2 (n = 0 to 7)	CSn wait control register 2 (n = 0 to 3)
BUSPRI	BPHB[1:0]	—	Internal peripheral bus 4/5 priority control bits

2.12 Memory-Protection Units

Table 2.20 is a Comparison of Memory-Protection Unit Registers.

Table 2.20 Comparison of Memory-Protection Unit Registers

Register	Bit	RX630(MPU)	RX660(MPU)
MPECLR	CLR	Error status clear bit [When reading] 0: Fixed to read [When writing] 0: Nothing is performed. 1: The MPESTS.DRW, DMPER, and IMPER bits are set to 0.	Error status clear bit [When reading] 0: Fixed to read [When writing] 0: Nothing is performed. 1: The MPESTS.DRW, DA, and IA bits are set to 0.
MPESTS	IA (RX630) IMPER (RX660)	Instruction memory protection error generation bit	Instruction memory protection error generation bit
	DA (RX630) DMPER (RX660)	Data memory protection error generation bit	Data memory protection error generation bit

2.13 DMA Controller

Table 2.21 is a Comparative Overview of DMA Controllers, and Table 2.22 is a Comparison of DMA Controller Registers.

Table 2.21 Comparative Overview of DMA Controllers

Item		RX630 (DMACA)	RX660 (DMACAa)
Number of channels		4 channels (DMACm (m = 0 to 3))	8 channels (DMACm (m = 0 to 7))
Transfer space		512 MB (from 00000000h to 0FFFFFFFh, and from F0000000h to FFFFFFFFh, excluding reserved areas)	512 MB (from 00000000h to 0FFFFFFFh, and from F0000000h to FFFFFFFFh, excluding reserved areas)
Maximum transfer volume		1 M data (Maximum number of transfers in block transfer mode: 1,024 data × 1,024 blocks)	64 M data (Maximum number of transfers in block transfer mode: 1,024 data × 65,536 blocks)
DMAC activation source		• Activation source selectable for each channel — Software trigger — Interrupt requests from peripheral modules or trigger input to external interrupt input pins	• Activation source selectable for each channel — Software trigger — Interrupt requests from peripheral modules or trigger input to external interrupt input pins
Channel priority		Channel 0 > channel 1 > channel 2 > channel 3 (Channel 0: Highest priority)	Channel 0 > channel 1 > channel 2 > channel 3 ... > channel 7 (Channel 0: Highest priority)
Transfer data	Single data	Bit length: 8, 16, or 32 bits	Bit length: 8, 16, or 32 bits
	Block size	Number of data: 1 to 1,024	Number of data: 1 to 1,024
Transfer modes	Normal transfer mode	• One data transfer by one DMA transfer request • Free running mode (setting in which total number of data transfers is not specified) can be set.	• One data transfer by one DMA transfer request • Free running mode (setting in which total number of data transfers is not specified) can be set.
	Repeat transfer mode	• One data transfer by one DMA transfer request • Program returns to the transfer start address on completion of data transfer for the repeat size specified for the transfer source or destination. • Maximum repeat size that can be set: 1,024	• One data transfer by one DMA transfer request • Program returns to the transfer start address on completion of data transfer for the repeat size specified for the transfer source or destination. • Maximum repeat size that can be set: 1,024
	Block transfer mode	• A single DMA transfer request leads to a single data block transfer. • Maximum block size that can be set: 1,024 data	• A single DMA transfer request leads to a single data block transfer. • Maximum block size that can be set: 1,024 data

Item		RX630 (DMACA)	RX660 (DMACAa)
Selective functions	Extended repeat area function	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed • Area of 2 bytes to 128 MB can be set separately as extended repeat area for transfer source and destination.	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed • Area of 2 bytes to 128 MB can be set separately as extended repeat area for transfer source and destination.
Interrupt requests	Transfer end Interrupt	Generated on completion of transferring data volume specified by the transfer counter.	• Generated when the specified number of transfers is completed in normal transfer mode. • Generated when the specified number of repeat transfers is completed in repeat transfer mode. • Generated when the transfer of the specified number of blocks is completed in block transfer mode.
	Transfer escape end Interrupt	Generated when data transfer for the repeat size is completed or the extended repeat area overflows.	Generated when data transfer for the repeat size is completed or the extended repeat area overflows.
Event link function		—	An event link request is generated after each data transfer (in block transfer mode, after each block is transferred).
Low power consumption function		Ability to specify module stop state	Ability to specify module stop state

Table 2.22 Comparison of DMA Controller Registers

Register	Bit	RX630 (DMACA)	RX660 (DMACAa)
DMCRB	—	DMA block transfer count register (b9 to b0)	DMA block transfer count register (b15 to b0)
DMIST	—	—	DMAC74 interrupt status monitor register

2.14 Data Transfer Controller

Table 2.23 is a Comparative Overview of Data Transfer Controllers, and Table 2.24 is a Comparison of Data Transfer Controller Registers.

Table 2.23 Comparative Overview of Data Transfer Controllers

Item	RX630 (DTCa)	RX660 (DTCb)
Number of transfer channels	Equal to the number of all interrupt sources that can activate a DTC	Equal to the number of all interrupt sources that can activate a DTC
Transfer modes	• Normal transfer mode — A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address returns to the transfer start address after the number of data transfers corresponding to the repeat size. — The maximum repeat size is 256 data. • Block transfer mode — A single activation leads to the transfer of a single block. — The maximum block size is 256 data.	• Normal transfer mode — A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address returns to the transfer start address after the number of data transfers corresponding to the repeat size. — The maximum number of repeat transfers is 256, and the maximum transfer size is 256 × 32 bits (1024 bytes). • Block transfer mode — A single activation leads to the transfer of a single block. — Up to 1,024 bytes (256 × 32 bits) can be specified for the block size.
Chain transfer functions	• Channel transfer corresponding to the interrupt source is possible (transferred in response to a DTC activation request from the ICU). • Multiple data transfers can be performed for a single activation source (chain transfer). • Either “executed when the counter is 0” or “always executed” can be selected for chain transfer.	• Multiple types of data transfer can be performed sequentially for a single transfer request. • Either “performed only when the transfer counter becomes 0” or “every time” can be selected.

Item	RX630 (DTCa)	RX660 (DTCb)
Sequence transfer	—	A series of complicated transfers can be registered as a sequence. Any sequence can be selected based on transfer data and executed. • Only one activation source can be selected at a time. • A maximum of 256 sequences can be defined for one activation source. • The data that is first transferred in response to a transfer request determines the sequence. • The entire sequence can be executed on a single transfer request, or the sequence can be suspended in the middle and then resumed on the next transfer request (sequence division).
Transfer space	• 16 MB in short address mode (from 0000 0000h to 007FF FFFh, and from FF80 0000h to FFFF FFFFh, excluding reserved areas) • 4 GB in full-address mode (within 0000 0000h to FFFF FFFFh, excluding reserved areas)	• 16 MB in short address mode (from 0000 0000h to 007F FFFh, and from FF80 0000h to FFFF FFFFh, excluding reserved areas) • 4 GB in full-address mode (within 0000 0000h to FFFF FFFFh, excluding reserved areas)
Data transfer units	• Length of a single data: 8, 16, or 32 bits • Number of data for a single block: 1 to 256 data	• Single data: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data
CPU interrupt requests	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after data transfer of the specified volume.	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after data transfer of the specified volume.
Event link function	—	An event link request is generated after each data transfer (in block transfer mode, after each block is transferred).
Read skip	Read skip of transfer information can be specified.	Reading of the transfer information can be skipped when the same transfer is repeated.
Write-back skip	Write-back can be skipped when the transfer source address or transfer destination address is fixed.	Write-back of the transfer information that is not updated is skipped when the transfer source or destination address is fixed.
Write-back disable	—	Write-back of transfer information can be disabled.

Item	RX630 (DTCa)	RX660 (DTCb)
Displacement addition	—	Displacement can be added to the transfer source address (can be selected for each transfer information).
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Table 2.24 Comparison of Data Transfer Controller Registers

Register	Bit	RX630 (DTCa)	RX660 (DTCb)
MRA	WBDIS	—	Write-back disable bit*1
MRB	SQEND	—	Sequence transfer end bit
	INDX	—	Index table reference bit
MRC	—	—	DTC mode register C
DTCVBR	—	DTC vector base address [Lower 12 bits] These bits are read as 0. The write value should be 0.	DTC vector base register The lower 10 bits are reserved, and the value is fixed to 0. The write value should be 0.
DTCIBR	—	—	DTC index table base register
DTCOR	—	—	DTC operation register
DTCSQE	—	—	DTC sequence transfer enable register
DTCDISP	—	—	DTD address displacement register

Note: 1. Transfer information is placed in the RAM area. However, if the MRA.WBDIS bit is set to 1 (no write-back performed), transfer information can be placed also in the ROM area.

2.15 I/O Ports

Table 2.26 to Table 2.27 provide comparative overviews of I/O ports. Table 2.28 is a Comparison of I/O Port Functions, and Table 2.30 is a Comparison of I/O Port Registers.

Table 2.25 Comparative Overview of I/O Ports (144-Pin)

Port Symbol	RX630 (145-Pin, 144-Pin)	RX660 (144-Pin)
PORT0	P00 to P03, P05, P07	P00 to P07
PORT1	P12 to P17	P12 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P56	P50 to P56
PORT6	P60 to P67	P60 to P67
PORT7	P70 to P77	P70 to P77
PORT8	P80 to P83, P86, P87	P80 to P83, P86, P87
PORT9	P90 to P93	P90 to P93
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7
PORTF	PF5	PF5 to PF7
PORTH	—	PH0 to PH3, PH6*1, PH7*1
PORTJ	PJ3, PJ5	PJ1, PJ3 to PJ7
PORTK	PK2 to PK5	PK2 to PK5
PORTL	PL0, PL1	PL0, PL1
PORTN	—	PN6, PN7

Note: 1. Not present on products with a ROM capacity of 64 KB.

Table 2.26 Comparative Overview of I/O Ports (100-Pin)

Port Symbol	RX630 (100-Pin)	RX660 (100-Pin)
PORT0	P05, P07	P03 to P07
PORT1	P12 to P17	P12 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P55	P50 to P55
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7
PORTH	—	PH0 to PH3, PH6, PH7
PORTJ	PJ3	PJ1, PJ3, PJ6, PJ7
PORTN	—	PN6

Table 2.27 Comparative Overview of I/O Ports (80-Pin)

Port Symbol	RX630 (80-Pin)	RX660 (80-Pin)
PORT0	P05, P07	P03 to P07
PORT1	P12 to P17	P12 to P17
PORT2	P20, P21, P26, P27	P20, P21, P26, P27
PORT3	P30 to P32, P34 to P37	P30 to P32, P34 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P54, P55	P54, P55
PORTA	PA0 to PA6	PA0 to PA6
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC2 to PC7	PC2 to PC7
PORTD	PD0 to PD2	PD0 to PD2
PORTE	PE0 to PE5	PE0 to PE5
PORTH	—	PH0 to PH3, PH6[*1], PH7[*1]
PORTJ	—	PJ1, PJ6, PJ7
PORTN	—	PN6

Note: 1. Not present on products with a ROM capacity of 64 KB.

Table 2.28 Comparison of I/O Port Functions

Item	Port Symbol	RX630	RX660
Input pull-up function	PORT0	P00 to P03, P05, P07	P00 to P07
	PORT1	P10 to P17	P12 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P57	P50 to P56
	PORT6	P60 to P67	P60 to P67
	PORT7	P70 to P77	P70 to P77
	PORT8	P80 to P87	P80 to P83, P86, P87
	PORT9	P90 to P97	P90 to P93
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	PD0 to PD7	PD0 to PD7
	PORTE	PE0 to PE7	PE0 to PE7
	PORTF	PF0 to PF5	PF5 to PF7
	PORTG	PG0, PG1, PG2 to PG7	—
	PORTH	PH4, PH5	PH0 to PH3, PH6, PH7
	PORTJ	PJ3, PJ5	PJ1, PJ3 to PJ5, PJ6, PJ7
	PORTK	PK0 to PK7	PK2 to PK5
	PORTL	PL0 to PL4	PL0, PL1
	PORTN	—	PN6, PN7
Open drain output function	PORT0	P00 to P03, P05, P07	P00 to P07
	PORT1	P10 to P17	P12 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P57	P50 to P56
	PORT6	P60 to P67	P60 to P67
	PORT7	P70 to P77	P70 to P77
	PORT8	P80 to P87	P80 to P83, P86, P87
	PORT9	P90 to P97	P90 to P93
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	PD0 to PD7	PD0 to PD7
	PORTE	PE0 to PE7	PE0 to PE7
	PORTF	PF0 to PF5	PF5 to PF7
	PORTG	PG0, PG1, PG2 to PG7	—
	PORTH	PH4, PH5	PH0 to PH3, PH6, PH7
	PORTJ	PJ3, PJ5	PJ1, PJ3 to PJ5, PJ6, PJ7
	PORTK	PK0 to PK7	PK2 to PK5
	PORTL	PL0 to PL4	PL0, PL1
	PORTN	—	PN6, PN7
5 V tolerant	PORT0	P07	—
	PORT1	P12 to P17	P12, P13, P16, P17
	PORT2	P20 to P25	—
	PORT3	P30 to P34	—
	PORT5	P50 to P52, P54 to P57	—

Item	Port Symbol	RX630	RX660
5 V tolerant	PORT6	P67	—
	PORT7	P74 to P77	—
	PORT8	P80 to P82	—
	PORTA	PA1 to PA4, PA6	—
	PORTB	PB0 to PB7	—
	PORTC	PC0 to PC7	—

Table 2.29 Comparison of Driving Ability Switching on I/O Ports

Port Symbol	Driving Ability Switching	RX630	RX660
PORT0	Fixed to normal	—	P03, P05 to P07
	Normal/high	P00 to P02	P00 to P02, P04
	Fixed to high drive	P03, P05, P07	—
PORT1	Normal/high	—	P12 to P17
	Fixed to high drive	P10 to P17	—
PORT2	Normal/high	P27	P20 to P27
	Fixed to high drive	P20 to P26	—
PORT3	Fixed to normal	P36	P36, P37
	Normal/high	P30 to P34, P37	P30 to P34
PORT4	Fixed to normal	P40 to P47	P40 to P47
PORT5	Normal/high	P50 to P52, P56, P57	P50 to P56
	Fixed to high drive	P53 to P55	—
PORT6	Normal/high	P60 to P67	P60 to P67
PORT7	Normal/high	P70 to P77	P70 to P77
PORT8	Normal/high	—	P80 to P83, P86, P87
	Fixed to high drive	P80 to P87	—
PORT9	Normal/high	P90 to P97	P90 to P93
PORTA	Normal/high	PA0 to PA7	PA0 to PA7
PORTB	Normal/high	PB0 to PB7	PB0 to PB7
PORTC	Normal/high	PC0 to PC7	PC0 to PC7
PORTD	Normal/high	PD0 to PD7	PD0 to PD7
PORTE	Normal/high	PE0 to PE7	PE0 to PE7
PORTF	Normal/high	—	PF5 to PF7
	Fixed to high drive	PF0 to PF5	—
PORTG	Fixed to normal	PG0, PG1	—
	Fixed to high drive	PG2 to PG7	—
PORTH	Normal/high	—	PH0 to PH3, PH6, PH7
	Fixed to high drive	PH4, PH5	—
PORTJ	Fixed to normal	—	PJ6, PJ7
	Normal/high	—	PJ1, PJ3 to PJ5
	Fixed to high drive	PJ3, PJ5	—

Port Symbol	Driving Ability Switching	RX630	RX660
PORTK	Normal/high	—	PK2 to PK5
	Fixed to high drive	PK0 to PK7	—
PORTL	Normal/high	—	PL0, PL1
	Fixed to high drive	PL0 to PL4	—
PORTN	Normal/high	—	PN6, PN7

Table 2.30 Comparison of I/O Port Registers

Register	Bit	RX630	RX660
PDR	B0 to B7	Pm0 to Pm7 I/O select bits (m = 0 to 9, A to H, J to L)	Pm0 to Pm7 I/O select bits (m = 0 to 9, A to F, H, J to L, N)
PODR	B0 to B7	Pm0 to Pm7 output data store bits (m = 0 to 9, A to H, J to L)	Pm0 to Pm7 output data store bits (m = 0 to 9, A to F, H, J to L, N)
PIDR	B0 to B7	Pm0 to Pm7 bits (m = 0 to 9, A to H, J to L)	Pm0 to Pm7 bits (m = 0 to 9, A to F, H, J to L, N)
PMR	—	Pm0 to Pm7 pin mode control bits (m = 0 to 9, A to H, J to L)	Pm0 to Pm7 pin mode control bits (m = 0 to 9, A to F, H, J to L, N)
ODR0	—	Pm1 output type select bits (m = 0 to 9, A to G, J to L) For pins other than the port PE1 pin Odd bit Even bit x 0: CMOS output x 1: N-channel open drain (b1, b3, b5, b7: Reserved) For port PE1 pin b3 b2 0 0: CMOS output 0 1: N-channel open drain 1 0: P-channel open drain 1 1: Setting prohibited.	Pm1 output type select bits (m = 0 to 9, A to E, H, J to L) 0: CMOS output 1: N channel open drain
ODR1	B0, B2, B4, B6	Pm4, Pm5, Pm6, and Pm7 output type select bits (m = 0 to 9, A to H, J to L)	Pm4, Pm5, Pm6, and Pm7 output type select bits (m = 0 to 8, A to F, H, J, K, N)
PCR	B0 to B7	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A to H, J to L)	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A to F, H, J to L, N)
DSCR	—	Drive capacity control register (m =0, 2, 5 to 7, 9, A to E, G)	Drive capacity control register (m = 0 to 3, 5 to 9, A to F, H, J to L, N)

2.16 Multi-Function Pin Controller

Table 2.31 is a Comparison of Multiplexed Pin Assignments, and Table 2.32 to Table 2.51 are Comparisons of Multi-Function Pin Controller Registers.

In the following comparison of the assignments of multiplexed pins, **orange** text pins that exist on the RX630 Group only and **blue** text designates pins that exist on the RX660 Group only. A circle (○) indicates that a function is assigned, a cross (×) that the pin does not exist or that no function is assigned, and grayed out items mean that the function is not implemented.

Table 2.31 Comparison of Multiplexed Pin Assignments

Module/ Function	Pin Function	Port Allocation	RX630			RX660		
			144-Pin	100-Pin	80-Pin	144-Pin	100-Pin	80-Pin
Interrupts	NMI (input)	P35	○	○	○	○	○	○
	IRQ0-DS (input)	P30	○	○	○	○	○	○
	IRQ0 (input)	P50	×	×	×	○	○	×
		P60	×	×	×	○	×	×
		P70	×	×	×	○	×	×
		P90	×	×	×	○	×	×
		PA0	×	×	×	○	○	○
		PD0	○	○	○	○	○	○
		PH1	×	×	×	○	○	○
	IRQ1-DS (input)	P31	○	○	○	○	○	○
	IRQ1 (input)	P51	×	×	×	○	○	×
		P61	×	×	×	○	×	×
		P71	×	×	×	○	×	×
		PD1	○	○	○	○	○	○
		PH2	×	×	×	○	○	○
	IRQ2-DS (input)	P32	○	○	○	○	○	○
	IRQ2 (input)	P12	○	○	○	○	○	○
		P52	×	×	×	○	○	×
		P62	×	×	×	○	×	×
		P82	×	×	×	○	×	×
		PB2	×	×	×	○	○	○
		PD2	○	○	○	○	○	○
	IRQ3-DS (input)	P33	○	○	×	○	○	×
	IRQ3 (input)	P13	○	○	○	○	○	○
		P23	×	×	×	○	○	×
		P53	×	×	×	○	○	×
		P63	×	×	×	○	×	×
		P83	×	×	×	○	×	×
		PB3	×	×	×	○	○	○
		PD3	○	○	×	○	○	×
	IRQ4-DS (input)	PB1	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX630			RX660		
			144-Pin	100-Pin	80-Pin	144-Pin	100-Pin	80-Pin
Interrupts	IRQ4 (input)	P14	○	○	○	○	○	○
		P34	○	○	○	○	○	○
		P37	×	×	×	○	○	○
		P54	×	×	×	○	○	○
		P64	×	×	×	○	×	×
		PB4	×	×	×	○	○	○
		PD4	○	○	×	○	○	×
		PF5	○	×	×	○	×	×
	IRQ5-DS (input)	PA4	○	○	○	○	○	○
	IRQ5 (input)	P15	○	○	○	○	○	○
		P25	×	×	×	○	○	×
		P36	×	×	×	○	○	○
		PA5	×	×	×	○	○	○
		PC5	×	×	×	○	○	○
		PD5	○	○	×	○	○	×
		PE5	○	○	○	○	○	○
	IRQ6-DS (input)	PA3	○	○	○	○	○	○
	IRQ6 (input)	P16	○	○	○	○	○	○
		P26	×	×	×	○	○	○
		P56	×	×	×	○	×	×
		PB6	×	×	×	○	○	○
		PD6	○	○	×	○	○	×
		PE6	○	○	×	○	○	×
	IRQ7-DS (input)	PE2	○	○	○	○	○	○
	IRQ7 (input)	P17	○	○	○	○	○	○
		P27	×	×	×	○	○	○
		P77	×	×	×	○	×	×
		PA7	×	×	×	○	○	×
		PD7	○	○	×	○	○	×
		PE7	○	○	×	○	○	×
	IRQ8-DS (input)	P40	○	○	○	○	○	○
	IRQ8 (input)	P00	○	×	×	○	×	×
		P20	○	○	○	○	○	○
		P73	×	×	×	○	×	×
		P80	×	×	×	○	×	×
		PE0	×	×	×	○	○	○
	IRQ9-DS (input)	P41	○	○	○	○	○	○
	IRQ9 (input)	P01	○	×	×	○	×	×
		P21	○	○	○	○	○	○
		P81	×	×	×	○	×	×
		P91	×	×	×	○	×	×
		PE1	×	×	×	○	○	○
	IRQ10-DS (input)	P42	○	○	○	○	○	○
	IRQ10 (input)	P02	○	×	×	○	×	×
		P55	○	○	○	○	○	○
		P72	×	×	×	○	×	×
		P92	×	×	×	○	×	×
		PA2	×	×	×	○	○	○
		PC2	×	×	×	○	○	○
	IRQ11-DS (input)	P43	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX630			RX660		
			144-Pin	100-Pin	80-Pin	144-Pin	100-Pin	80-Pin
Interrupts	IRQ11 (input)	P03	○	×	×	○	○*1	○
		P93	×	×	×	○	×	×
		PA1	○	○	○	○	○	○
		PC3	×	×	×	○	○	○
		PE3	×	×	×	○	○	○
		PJ3	×	×	×	○	○	×
	IRQ12-DS (input)	P44	○	○	○	○	○	○
	IRQ12 (input)	P24	×	×	×	○	○	×
		P74	×	×	×	○	×	×
		PB0	○	○	○	○	○	○
		PC1	○	○	×	○	○	×
		PC4	×	×	×	○	○	○
		PE4	×	×	×	○	○	○
	IRQ13-DS (input)	P45	○	○	○	○	○	○
	IRQ13 (input)	P05	○	○	○	○	○	○
		P65	×	×	×	○	×	×
		P75	×	×	×	○	×	×
		PB5	×	×	×	○	○	○
		PC6	○	○	○	○	○	○
		PJ5	×	×	×	○	×	×
	IRQ14-DS (input)	P46	○	○	○	○	○	○
	IRQ14 (input)	P66	×	×	×	○	×	×
		P76	×	×	×	○	×	×
		P86	×	×	×	○	×	×
		PA6	×	×	×	○	○	○
		PC0	○	○	×	○	○	×
		PC7	○	○	○	○	○	○
	IRQ15-DS (input)	P47	○	○	○	○	○	○
	IRQ15 (input)	P07	○	○	○	○	○	○
		P22	×	×	×	○	○	×
		P67	○	×	×	○	×	×
		P87	×	×	×	○	×	×
		PB7	×	×	×	○	○	○
Multi-function timer unit 2	MTIOC0A (input/output)	P34	○	○	○	○	○	○
		PB3	○	○	○	○	○	○
		PC4	×	×	×	○	○	○
	MTIOC0B (input/output)	P13	○	○	○	○	○	○
		P15	○	○	○	○	○	○
		PA1	○	○	○	○	○	○
	MTIOC0C (input/output)	P32	○	○	○	○	○	○
		PB1	○	○	○	○	○	○
		PC5	×	×	×	○	○	○
	MTIOC0D (input/output)	P33	○	○	×	○	○	×
		PA3	○	○	○	○	○	○
	MTIOC1A (input/output)	P20	○	○	○	○	○	○
		PE4	○	○	○	○	○	○
	MTIOC1B (input/output)	P21	○	○	○	○	○	○
		PB5	○	○	○	○	○	○
		PE3	×	×	×	○	○	○

Module/ Function	Pin Function	Port Allocation	RX630			RX660		
			144-Pin	100-Pin	80-Pin	144-Pin	100-Pin	80-Pin
Multi-function timer unit 2	MTIOC2A (input/output)	P26	○	○	○	○	○	○
		PB5	○	○	○	○	○	○
	MTIOC2B (input/output)	P27	○	○	○	○	○	○
		PE5	○	○	○	○	○	○
	MTIOC3A (input/output)	P14	○	○	○	○	○	○
		P17	○	○	○	○	○	○
		PC1	○	○	×	○	○	×
		PC7	○	○	○	○	○	○
		PJ1	×	×	×	○	○	○
	MTIOC3B (input/output)	P17	○	○	○	○	○	○
		P22	○	○	×	○	○	×
		P80	○	×	×	○	×	×
		PA1	×	×	×	○	○	○
		PB7	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
		PE1	×	×	×	○	○	○
		PH0	×	×	×	○	○	○
	MTIOC3C (input/output)	P16	○	○	○	○	○	○
		P56	○	×	×	○	×	×
		PC0	○	○	×	○	○	×
		PC6	○	○	○	○	○	○
		PJ3	○	○	×	○	○	×
	MTIOC3D (input/output)	P16	○	○	○	○	○	○
		P23	○	○	×	○	○	×
		P81	○	×	×	○	×	×
		PA6	×	×	×	○	○	○
		PB0	×	×	×	○	○	○
		PB6	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
		PE0	×	×	×	○	○	○
		PH1	×	×	×	○	○	○
	MTIOC4A (input/output)	P21	×	×	×	○	○	○
		P24	○	○	×	○	○	×
		P55	×	×	×	○	○	○
		P82	○	×	×	○	×	×
		PA0	○	○	○	○	○	○
		PB3	○	○	○	○	○	○
		PE2	○	○	○	○	○	○
		PE4	×	×	×	○	○	○
	MTIOC4B (input/output)	P30	○	○	○	○	○	○
		P54	○	○	○	○	○	○
		PC2	○	○	○	○	○	○
		PD1	○	○	○	○	○	○
		PE3	○	○	○	○	○	○
		P17	×	×	×	○	○	○

Module/ Function	Pin Function	Port Allocation	RX630			RX660		
			144-Pin	100-Pin	80-Pin	144-Pin	100-Pin	80-Pin
Multi-function timer unit 2	MTIOC4C (input/output)	P25	○	○	×	○	○	×
		P83	○	×	×	○	×	×
		P87	×	×	×	○	×	×
		PA4	×	×	×	○	○	○
		PB1	○	○	○	○	○	○
		PE1	○	○	○	○	○	○
		PE5	○	○	○	○	○	○
		PH2	×	×	×	○	○	○
	MTIOC4D (input/output)	P31	○	○	○	○	○	○
		P55	○	○	○	○	○	○
		P86	×	×	×	○	×	×
		PA3	×	×	×	○	○	○
		PC3	○	○	○	○	○	○
		PD2	○	○	○	○	○	○
		PE4	○	○	○	○	○	○
		PH3	×	×	×	○	○	○
	MTIC5U (input)	P12	×	×	×	○	○	○
		PA4	○	○	○	○	○	○
		PD7	○	○	×	○	○	×
	MTIC5V (input)	PA3	×	×	×	○	○	○
		PA6	○	○	○	○	○	○
		PD6	○	○	×	○	○	×
	MTIC5W (input)	PB0	○	○	○	○	○	○
		PD5	○	○	×	○	○	×
	MTIOC6A (input/output)	PE7				○	○	×
	MTIOC6B (input/output)	PA5				○	○	○
		PA6				○	○	○
	MTIOC6C (input/output)	PE6				○	○	×
	MTIOC6D (input/output)	PA0				○	○	○
	MTIOC7A (input/output)	PA2				○	○	○
		PE2				○	○	○
	MTIOC7B (input/output)	PA1				○	○	○
	MTIOC7C (input/output)	P67				○	×	×
		PA4				○	○	○
	MTIOC7D (input/output)	P66				○	×	×
		PE4				○	○	○
	MTIOC8A (input/output)	PD6				○	○	×
	MTIOC8B (input/output)	PD4				○	○	×
	MTIOC8C (input/output)	PD5				○	○	×
	MTIOC8D (input/output)	PD3				○	○	×
	MTCLKA (input)	P14	○	○	○	○	○	○
		P24	○	○	×	○	○	×
		PA4	○	○	○	○	○	○
		PC6	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX630			RX660		
			144-Pin	100-Pin	80-Pin	144-Pin	100-Pin	80-Pin
Multi-function timer unit 2	MTCLKB (input)	P15	○	○	○	○	○	○
		P25	○	○	×	○	○	×
		PA6	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	MTCLKC (input)	P22	○	○	×	○	○	×
		PA1	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	MTCLKD (input)	P23	○	○	×	○	○	×
		PA3	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
Port output enable 2	POE0# (input)	PC4	○	○	○	○	○	○
		PD7	○	○	×	○	○	×
		P32	×	×	×	○	○	○
		P93	×	×	×	○	×	×
		PD1	×	×	×	○	○	○
	POE1# (input)	PB5	○	○	○			
		PD6	○	○	×			
	POE2# (input)	P34	○	○	○			
		PA6	○	○	○			
		PD5	○	○	×			
	POE3# (input)	P33	○	○	×			
		PB3	○	○	○			
		PD4	○	○	×			
	POE4# (input)	P33				○	○	×
		P92				○	×	×
		PB5				○	○	○
		PD0				○	○	○
		PD6				○	○	×
	POE8# (input)	P17	○	○	○	○	○	○
		P30	○	○	○	○	○	○
		PD3	○	○	×	○	○	×
		PE3	○	○	○	○	○	○
		PJ5	×	×	×	○	×	×
	POE10# (input)	P32				○	○	○
		P34				○	○	○
		PA6				○	○	○
		PD5				○	○	×
	POE11# (input)	P33				○	○	×
		PB3				○	○	○
		PD4				○	○	×
16-bit timer pulse unit	TIOCA0 (input/output)	P86	○	×	×			
		PA0	○	○	○			
	TIOCB0 (input/output)	P17	○	○	○			
		PA1	○	○	○			
	TIOCC0 (input/output)	P32	○	○	○			
	TIOCD0 (input/output)	P33	○	○	×			
		PA3	○	○	○			
	TIOCA1 (input/output)	P56	○	×	×			
		PA4	○	○	○			

Module/ Function	Pin Function	Port Allocation	RX630			RX660		
			144-Pin	100-Pin	80-Pin	144-Pin	100-Pin	80-Pin
16-bit timer pulse unit	TIOCB1 (input/output)	P16	○	○	○			
		PA5	○	○	○			
	TIOCA2 (input/output)	P87	○	×	×			
		PA6	○	○	○			
	TIOCB2 (input/output)	P15	○	○	○			
		PA7	○	○	×			
	TIOCA3 (input/output)	P21	○	○	○			
		PB0	○	○	○			
	TIOCB3 (input/output)	P20	○	○	○			
		PB1	○	○	○			
	TIOCC3 (input/output)	P22	○	○	×			
		PB2	○	○	○			
	TIOCD3 (input/output)	P23	○	○	×			
		PB3	○	○	○			
	TIOCA4 (input/output)	P25	○	○	×			
		PB4	○	○	○			
	TIOCB4 (input/output)	P24	○	○	×			
		PB5	○	○	○			
	TIOCA5 (input/output)	P13	○	○	○			
		PB6	○	○	○			
	TIOCB5 (input/output)	P14	○	○	○			
		PB7	○	○	○			
	TCLKA (input)	P14	○	○	○			
		PC2	○	○	○			
	TCLKB (input)	P15	○	○	○			
		PA3	○	○	○			
		PC3	○	○	○			
	TCLKC (input)	P16	○	○	○			
		PB2	○	○	○			
		PC0	○	○	×			
	TCLKD (input)	P17	○	○	○			
		PB3	○	○	○			
		PC1	○	○	×			
	TIOCA6 (input/output)	PC6	○	×	×			
	TIOCB6 (input/output)	PC7	○	×	×			
	TIOCC6 (input/output)	PC4	○	×	×			
	TIOCD6 (input/output)	PC5	○	×	×			
	TIOCA7 (input/output)	PD0	○	×	×			
	TIOCB7 (input/output)	PD1	○	×	×			
	TIOCA8 (input/output)	PD2	○	×	×			
	TIOCB8 (input/output)	PD3	○	×	×			
	TIOCA9 (input/output)	PE2	○	×	×			

Module/ Function	Pin Function	Port Allocation	RX630			RX660		
			144-Pin	100-Pin	80-Pin	144-Pin	100-Pin	80-Pin
16-bit timer pulse unit	TIOCB9 (input/output)	PE3	○	×	×			
	TIOCC9 (input/output)	PE0	○	×	×			
	TIOCD9 (input/output)	PE1	○	×	×			
	TIOCA10 (input/output)	PE4	○	×	×			
	TIOCB10 (input/output)	PE5	○	×	×			
	TIOCA11 (input/output)	PE6	○	×	×			
	TIOCB11 (input/output)	PE7	○	×	×			
	TCLKE (input)	PC4	○	×	×			
	TCLKF (input)	PC5	○	×	×			
	TCLKG (input)	PD1	○	×	×			
	TCLKH (input)	PD3	○	×	×			
Programmable pulse generator	PO0 (output)	P20	○	○	○			
	PO1 (output)	P21	○	○	○			
	PO2 (output)	P22	○	○	×			
	PO3 (output)	P23	○	○	×			
	PO4 (output)	P24	○	○	×			
	PO5 (output)	P25	○	○	×			
	PO6 (output)	P26	○	○	○			
	PO7 (output)	P27	○	○	○			
	PO8 (output)	P30	○	○	○			
	PO9 (output)	P31	○	○	○			
	PO10 (output)	P32	○	○	○			
	PO11 (output)	P33	○	○	×			
	PO12 (output)	P34	○	○	○			
	PO13 (output)	P13	○	○	○			
		P15	○	○	○			
	PO14 (output)	P16	○	○	○			
	PO15 (output)	P14	○	○	○			
		P17	○	○	○			
	PO16 (output)	P73	○	×	×			
		PA0	○	○	○			
	PO17 (output)	PA1	○	○	○			
		PC0	○	○	×			
	PO18 (output)	PA2	○	○	○			
		PC1	○	○	×			
		PE1	○	○	○			
	PO19 (output)	P74	○	×	×			
		PA3	○	○	○			
	PO20 (output)	P75	○	×	×			
		PA4	○	○	○			
	PO21 (output)	PA5	○	○	○			
		PC2	○	○	○			
	PO22 (output)	P76	○	×	×			
		PA6	○	○	○			

Module/ Function	Pin Function	Port Allocation	RX630			RX660		
			144-Pin	100-Pin	80-Pin	144-Pin	100-Pin	80-Pin
Programmable pulse generator	PO23 (output)	P77	○	×	×			
		PA7	○	○	×			
		PE2	○	○	○			
	PO24 (output)	PB0	○	○	○			
		PC3	○	○	○			
	PO25 (output)	PB1	○	○	○			
		PC4	○	○	○			
	PO26 (output)	P80	○	×	×			
		PB2	○	○	○			
		PE3	○	○	○			
	PO27 (output)	P81	○	×	×			
		PB3	○	○	○			
	PO28 (output)	P82	○	×	×			
		PB4	○	○	○			
		PE4	○	○	○			
	PO29 (output)	PB5	○	○	○			
		PC5	○	○	○			
	PO30 (output)	PB6	○	○	○			
		PC6	○	○	○			
	PO31 (output)	PB7	○	○	○			
		PC7	○	○	○			
8-bit timer	TMO0 (output)	P22	○	○	×	○	○	×
		PB3	○	○	○	○	○	○
		PH1	×	×	×	○	○	○
	TMCI0 (input)	P01	○	×	×	○	×	×
		P21	○	○	○	○	○	○
		PB1	○	○	○	○	○	○
		PH3	×	×	×	○	○	○
	TMRI0 (input)	P00	○	×	×	○	×	×
		P20	○	○	○	○	○	○
		PA4	○	○	○	○	○	○
		PH2	×	×	×	○	○	○
	TMO1 (output)	P17	○	○	○	○	○	○
		P26	○	○	○	○	○	○
	TMCI1 (input)	P02	○	×	×	○	×	×
		P12	○	○	○	○	○	○
		P54	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	TMRI1 (input)	P24	○	○	×	○	○	×
		PB5	○	○	○	○	○	○
	TMO2 (output)	P16	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	TMCI2 (input)	P15	○	○	○	○	○	○
		P31	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	TMRI2 (input)	P14	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
	TMO3 (output)	P13	○	○	○	○	○	○
		P32	○	○	○	○	○	○
		P55	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX630			RX660		
			144-Pin	100-Pin	80-Pin	144-Pin	100-Pin	80-Pin
8-bit timer	TMCI3 (input)	P27	○	○	○	○	○	○
		P34	○	○	○	○	○	○
		PA6	○	○	○	○	○	○
	TMRI3 (input)	P30	○	○	○	○	○	○
		P33	○	○	×	○	○	×
Serial communications interface	RXD0 (input)/ SMISO0 (input/output)/ SSCL0 (input/output)	P21	○	○	×	○	○	○
		P33	○	○	×	○	○	×
	TXD0 (output)/ SMOSI0 (input/output)/ SSDA0 (input/output)	P20	○	○	×	○	○	○
		P32	○	○	×	○	○	○
	SCK0 (input/output)	P22	○	○	×	○	○	×
		P34	○	○	×	○	○	○
	CTS0# (input)/ RTS0# (output)/ SS0# (input)	P23	○	○	×	○	○	×
		PJ3	○	○	×	○	○	×
	RXD1 (input)/ SMISO1 (input/output)/ SSCL1 (input/output)	P15	○	○	○	○	○	○
		P30	○	○	○	○	○	○
	TXD1 (output)/ SMOSI1 (input/output)/ SSDA1 (input/output)	P16	○	○	○	○	○	○
		P26	○	○	○	○	○	○
	SCK1 (input/output)	P17	○	○	○	○	○	○
		P27	○	○	○	○	○	○
	CTS1# (input)/ RTS1# (output)/ SS1# (input)	P14	○	○	○	○	○	○
		P31	○	○	○	○	○	○
	RXD2 (input)/ SMISO2 (input/output)/ SSCL2 (input/output)	P12	○	○	×	○	○	×
		P52	○	○	×	○	○	×
	TXD2 (output)/ SMOSI2 (input/output)/ SSDA2 (input/output)	P13	○	○	×	○	○	×
		P50	○	○	×	○	○	×
	SCK2 (input/output)	P51	○	○	×	○	○	×
	CTS2# (input)/ RTS2# (output)/ SS2# (input)	P54	○	○	×	○	○	×
		PJ5	×	×	×	○	×	×
	RXD3 (input)/ SMISO3 (input/output)/ SSCL3 (input/output)	P16	○	○	×	○	○	○
		P25	○	○	×	○	○	×

Module/ Function	Pin Function	Port Allocation	RX630			RX660		
			144-Pin	100-Pin	80-Pin	144-Pin	100-Pin	80-Pin
Serial communications interface	TXD3 (output)/ SMOSI3 (input/output)/ SSDA3 (input/output)	P17	○	○	×	○	○	○
		P23	○	○	×	○	○	×
	SCK3 (input/output)	P15	○	○	×	○	○	○
		P24	○	○	×	○	○	×
	CTS3# (input)/ RTS3# (output)/ SS3# (input)	P26	○	○	×	○	○	○
	RXD4 (input)/ SMISO4 (input/output)/ SSCL4 (input/output)	PB0	○	×	×	○	○	○
		PK4	○	×	×	○	×	×
	TXD4 (output)/ SMOSI4 (input/output)/ SSDA4 (input/output)	PB1	○	×	×	○	○	○
		PK5	○	×	×	○	×	×
	SCK4 (input/output)	P70	○	×	×	○	×	×
		PB3	○	×	×	○	○	○
	CTS4# (input)/ RTS4# (output)/ SS4# (input)	PB2	○	×	×	○	○	○
		PE6	○	×	×	○	○	×
	RXD5 (input)/ SMISO5 (input/output)/ SSCL5 (input/output)	PA2	○	○	○	○	○	○
		PA3	○	○	○	○	○	○
		PC2	○	○	○	○	○	○
	TXD5 (output)/ SMOSI5 (input/output)/ SSDA5 (input/output)	PA4	○	○	○	○	○	○
		PC3	○	○	○	○	○	○
	SCK5 (input/output)	PA1	○	○	○	○	○	○
		PC1	○	○	×	○	○	×
		PC4	○	○	○	○	○	○
	CTS5# (input)/ RTS5# (output)/ SS5# (input)	PA6	○	○	○	○	○	○
		PC0	○	○	×	○	○	×
	RXD6 (input)/ SMISO6 (input/output)/ SSCL6 (input/output)	P01	○	×	×	○	×	×
		P33	○	○	×	○	○	×
		PB0	○	○	○	○	○	○
	TXD6 (output)/ SMOSI6 (input/output)/ SSDA6 (input/output)	P00	○	×	×	○	×	×
		P32	○	○	○	○	○	○
		PB1	○	○	○	○	○	○
	SCK6 (input/output)	P02	○	×	×	○	×	×
		P34	○	○	○	○	○	○
		PB3	○	○	○	○	○	○
	CTS6# (input)/ RTS6# (output)/ SS6# (input)	PB2	○	○	○	○	○	○
		PJ3	○	○	×	○	○	×

Module/ Function	Pin Function	Port Allocation	RX630			RX660		
			144-Pin	100-Pin	80-Pin	144-Pin	100-Pin	80-Pin
Serial communications interface	RXD7 (input)/ SMISO7 (input/output)/ SSCL7 (input/output)	P92	○	×	×	○	×	×
	TXD7 (output)/ SMOSI7 (input/output)/ SSDA7 (input/output)	P90	○	×	×	○	×	×
		P55	×	×	×	○	×	×
	SCK7 (input/output)	P91	○	×	×	○	×	×
		P56	×	×	×	○	×	×
	CTS7# (input)/ RTS7# (output)/ SS7# (input)	P93	○	×	×	○	×	×
	RXD8 (input)/ SMISO8 (input/output)/ SSCL8 (input/output)	PC6	○	○	○	○	○	○
	TXD8 (output)/ SMOSI8 (input/output)/ SSDA8 (input/output)	PC7	○	○	○	○	○	○
	SCK8 (input/output)	PC5	○	○	○	○	○	○
	CTS8# (input)/ RTS8# (output)/ SS8# (input)	PC4	○	○	○	○	○	○
	RXD9 (input)/ SMISO9 (input/output)/ SSCL9 (input/output)	PB6	○	○	○	○	○	○
		PK3	○	×	×	○	×	×
	TXD9 (output)/ SMOSI9 (input/output)/ SSDA9 (input/output)	PB7	○	○	○	○	○	○
		PK2	○	×	×	○	×	×
	SCK9 (input/output)	P60	○	×	×	○	×	×
		PB5	○	○	○	○	○	○
	CTS9# (input)/ RTS9# (output)/ SS9# (input)	P61	○	×	×	○	×	×
		PB4	○	○	○	○	○	○
	RXD10 (input)/ SMISO10 (input/output)/ SSCL10 (input/output)	P81	○	×	×	○	×	×
		P86	×	×	×	○	×	×
		PC6	×	×	×	○	○	○
	TXD10 (output)/ SMOSI10 (input/output)/ SSDA10 (input/output)	P82	○	×	×	○	×	×
		P87	×	×	×	○	×	×
		PC7	×	×	×	○	○	○
	SCK10 (input/output)	P80	○	×	×	○	×	×
		P83	×	×	×	○	×	×
		PC5	×	×	×	○	○	○

Module/ Function	Pin Function	Port Allocation	RX630			RX660		
			144-Pin	100-Pin	80-Pin	144-Pin	100-Pin	80-Pin
Serial communications interface	CTS10# (input)/ RTS10# (output)/ SS10# (input)	P83	○	×	×	×	×	×
		PC4	×	×	×	○	○	○
	RXD11 (input)/ SMISO11 (input/output)/ SSCL11 (input/output)	P76	○	×	×	○	×	×
		PB6	×	×	×	○	○	○
	TXD11 (output)/ SMOSI11 (input/output)/ SSDA11 (input/output)	P77	○	×	×	○	×	×
		PB7	×	×	×	○	○	○
	SCK11 (input/output)	P75	○	×	×	○	×	×
		PB5	×	×	×	○	○	○
	CTS11# (input)/ RTS11# (output)/ SS11# (input)	P74	○	×	×	×	×	×
		PB4	×	×	×	○	○	○
	RXD12 (input)/ SMISO12 (input/output)/ SSCL12 (input/output)/ RXDX12 (input)	PE2	○	○	○	○	○	○
		PA2	×	×	×	○	○	○
	TXD12 (output)/ SMOSI12 (input/output)/ SSDA12 (input/output)/ TXDX12 (output)/ SIOX12 (input/output)	PE1	○	○	○	○	○	○
		PA4	×	×	×	○	○	○
	SCK12 (input/output)	PE0	○	○	○	○	○	○
		PA1	×	×	×	○	○	○
	CTS12# (input)/ RTS12# (output)/ SS12# (input)	PE3	○	○	○	○	○	○
		PA6	×	×	×	○	○	○
	RTS10# (output)	P80				○	×	×
	CTS10# (input)/ SS10# (input)	P83				○	×	×
	RTS11# (output)	P75				○	×	×
	CTS11# (input)/ SS11# (input)	P74				○	×	×
	RXD010 (input)/ SMISO010 (input/output)/ SSCL010 (input/output)	P81				○	×	×
		P86				○	×	×
		PC6				○	○	○
	TXD010 (output)/ SMOSI010 (input/output)/ SSDA010 (input/output)	P82				○	×	×
		P87				○	×	×
		PC7				○	○	○

Module/ Function	Pin Function	Port Allocation	RX630			RX660		
			144-Pin	100-Pin	80-Pin	144-Pin	100-Pin	80-Pin
Serial communications interface	SCK010 (input/output)/ RTS010# (output)/ DE010 (output)	P80				○	×	×
	SCK010 (input/output)/ CTS010# (input)/ SS010# (input)	P83				○	×	×
	SCK010 (input/output)	PC5				○	○	○
	CTS010# (input)/ RTS010# (output)/ SS010# (input)/ DE010 (output)	PC4				○	○	○
	RXD011 (input)/ SMISO011 (input/output)/ SSCL011 (input/output)	P76				○	×	×
		PB6				○	○	○
		PC0				○	○	×
	TXD011 (output)/ SMOSI011 (input/output)/ SSDA011 (input/output)	P77				○	×	×
		PB7				○	○	○
		PC1				○	○	×
	SCK011 (input/output)/ RTS011# (output)/ DE011 (output)	P75				○	×	×
	SCK011 (input/output)	PB5				○	○	○
	TXDA011 (output)	PC1				○	○	×
	TXDB011 (output)	PC2				○	○	○
	CTS011# (input)/ SS011# (input)	P74				○	×	×
	CTS011# (input)/ RTS011# (output)/ SS011# (input)/ DE011 (output)	PB4				○	○	○
I^2C bus interface	SCL0[FM+] (input/output)	P12	○	○	○			
	SDA0[FM+] (input/output)	P13	○	○	○			
	SCL1 (input/output)	P21	○	×	×			
	SDA1 (input/output)	P20	○	×	×			
	SCL2-DS (input/output)	P16	○	○	○			
	SDA2-DS (input/output)	P17	○	○	○			
	SCL3 (input/output)	PC0	○	×	×			
	SDA3 (input/output)	PC1	○	×	×			
USB2.0 function module	USB0_DPUPE (output)	P14	○	○	○			
	USB0_VBUS (input)	P16	○	○	○			

Module/ Function	Pin Function	Port Allocation	RX630			RX660		
			144-Pin	100-Pin	80-Pin	144-Pin	100-Pin	80-Pin
CAN module	CRX0 (input)*2	P33	○	○	×			
		PD2	○	○	×			
	CTX0 (output)*2	P32	○	○	×			
		PD1	○	○	×			
	CRX1-DS (input)	P15	○	○	○			
	CRX1 (input)	P55	○	○	○			
	CTX1 (output)	P14	○	○	○			
		P54	○	○	○			
	CRX2 (input)*3	P67	○	×	×			
	CTX2 (output)*3	P66	○	×	×			
CAN FD module	CRX0 (input)	P15				○	○	○
		P33				○	○	×
		P55				○	○	○
		PD2				○	○	○
	CTX0 (output)	P14				○	○	○
		P32				○	○	○
		P54				○	○	○
		PD1				○	○	○
Serial peripheral interface	RSPCKA (input/output)	PA5	○	○	○	○	○	○
		PB0	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
	MOSIA (input/output)	P16	○	○	○	○	○	○
		PA6	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	MISOA (input/output)	P17	○	○	○	○	○	○
		PA7	○	○	×	○	○	×
		PC7	○	○	○	○	○	○
	SSLA0 (input/output)	PA4	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	SSLA1 (output)	PA0	○	○	○	○	○	○
		PC0	○	○	×	○	○	×
	SSLA2 (output)	PA1	○	○	○	○	○	○
		PC1	○	○	×	○	○	×
	SSLA3 (output)	PA2	○	○	○	○	○	○
		PC2	○	○	○	○	○	○
	RSPCKB (input/output)	P27	○	○	○			
		PE1	○	○	○			
		PE5	○	○	○			
	MOSIB (input/output)	P26	○	○	○			
		PE2	○	○	○			
		PE6	○	○	×			
	MISOB (input/output)	P30	○	○	○			
		PE3	○	○	○			
		PE7	○	○	×			
	SSLB0 (input/output)	P31	○	○	○			
		PE4	○	○	○			
	SSLB1 (output)	P50	○	○	×			
		PE0	○	○	○			

Module/ Function	Pin Function	Port Allocation	RX630			RX660		
			144-Pin	100-Pin	80-Pin	144-Pin	100-Pin	80-Pin
Serial peripheral interface	SSLB2 (output)	P51	○	○	×			
		PE1	○	○	○			
	SSLB3 (output)	P52	○	○	×			
		PE2	○	○	○			
	RSPCKC (input/output)	PD3	○	×	×			
	MOSIC (input/output)	PD1	○	×	×			
	MISOC (input/output)	PD2	○	×	×			
	SSLC0 (input/output)	PD4	○	×	×			
	SSLC1 (output)	PD5	○	×	×			
	SSLC2 (output)	PD6	○	×	×			
	SSLC3 (output)	PD7	○	×	×			
IEBus controller	IERXD (input)	P16	○	○	○			
		PC2	○	○	○			
	IETXD (output)	P17	○	○	○			
		PC3	○	○	○			
Realtime clock	RTCOUT (output)	P16	○	○	○	○	○	○
		P32	○	○	○	○	○	○
	RTCIC0 (input)*1	P30	○	○	○	○*3	○*3	○*3
	RTCIC1 (input)*1	P31	○	○	○	○*3	○*3	○*3
	RTCIC2 (input)*1	P32	○	○	○	○*3	○*3	○*3
12-bit A/D converter	AN000 (input)*1	P40	○	○	○	○	○	○
	AN001 (input)*1	P41	○	○	○	○	○	○
	AN002 (input)*1	P42	○	○	○	○	○	○
	AN003 (input)*1	P43	○	○	○	○	○	○
	AN004 (input)*1	P44	○	○	○	○	○	○
	AN005 (input)*1	P45	○	○	○	○	○	○
	AN006 (input)*1	P46	○	○	○	○	○	○
	AN007 (input)*1	P47	○	○	○	○	○	○
	AN008 (input)*1	PD0	○	○	○	○	○	○
	AN009 (input)*1	PD1	○	○	○	○	○	○
	AN010 (input)*1	PD2	○	○	○	○	○	○
	AN011 (input)*1	PD3	○	○	×	○	○	○
	AN012 (input)*1	PD4	○	○	×	○	○	○
	AN013 (input)*1	PD5	○	○	×	○	○	○
	AN014 (input)*1	P90	○	×	×	○	○	×
	AN015 (input)*1	P91	○	×	×	○	○	×
	AN016 (input)*1	P92	○	×	×	○	○	○
	AN017 (input)*1	P93	○	×	×	○	○	○
	AN018 (input)*1	P00	○	×	×	○	○	○
	AN019 (input)*1	P01	○	×	×	○	○	×
	AN020 (input)*1	P02	○	×	×	○	○	×
	AN021 (input)	PD5				○	○	×
	AN022 (input)	PD6				○	○	×
	AN023 (input)	PD7				○	○	×

Module/ Function	Pin Function	Port Allocation	RX630			RX660		
			144-Pin	100-Pin	80-Pin	144-Pin	100-Pin	80-Pin
12-bit A/D converter	ADTRG0# (input)	P07	○	○	○	○	○	○
		P16	○	○	○	○	○	○
		P25	○	○	×	○	○	×
		PA1	×	×	×	○	○	○
		PH0	×	×	×	○	○	○
	ADST0 (output)	PA4				○	○	○
		PH1				○	○	○
10-bit A/D converter	AN0 (input)	PE2	○	○	○			
	AN1 (input)	PE3	○	○	○			
	AN2 (input)	PE4	○	○	○			
	AN3 (input)	PE5	○	○	○			
	AN4 (input)	PE6	○	○	×			
	AN5 (input)	PE7	○	○	×			
	AN6 (input)	PD6	○	○	×			
	AN7 (input)	PD7	○	○	×			
	ANEX0 (output)	PE0	○	○	○			
	ANEX1 (input)	PE1	○	○	○			
	ADTRG# (input)	P13	○	○	○			
		P17	○	○	○			
D/A converter or 12-Bit D/A converter	DA0 (output)	P03	○	×	×	○	○*2	○
	DA1 (output)	P05	○	○	○	○	○	○
Compare match timer W	TOC0 (output)	PC7				○	○	○
	TIC0 (input)	PC6				○	○	○
	TOC1 (output)	PE7				○	○	×
		PH2				○	○	○
	TIC1 (input)	PE6				○	○	×
		PH1				○	○	○
	TOC2 (output)	PB5				○	○	○
		PD3				○	○	×
	TIC2 (input)	PB3				○	○	○
		PD2				○	○	○
	TOC3 (output)	PE3				○	○	○
	TIC3 (input)	PE2				○	○	○
I²C bus interface	SCL0 (input/output)	P12				○	○	○
	SDA0 (input/output)	P13				○	○	○
	SCL2 (input/output)	P16				○	○	○
	SDA2 (input/output)	P17				○	○	○
Clock frequency accuracy measurement circuit	CACREF (input)	PA0				○	○	○
		PC7				○	○	○
		PH0				○	○	○
Remote control signal receiver	PMC0 (input)	P51				○	○	×
		P53				○	○	×
		PB3				○	○	○
		PC3				○	○	○
		PC4				○	○	○
		PC5				○	○	○

Module/ Function	Pin Function	Port Allocation	RX630			RX660		
			144-Pin	100-Pin	80-Pin	144-Pin	100-Pin	80-Pin
Comparator C	CMPC00 (input)	PE1				○	○	○
	CMPC10 (input)	PA3				○	○	○
	CMPC20 (input)	P15				○	○	○
	CMPC30 (input)	P26				○	○	○
	COMP0 (output)	PE5				○	○	○
	COMP1 (output)	PB1				○	○	○
	COMP2 (output)	P17				○	○	○
	COMP3 (output)	P30				○	○	○
	CVREFC0 (input)	PE2				○	○	○
	CVREFC1 (input)	PA4				○	○	○
	CVREFC2 (input)	P14				○	○	○
	CVREFC3 (input)	P27				○	○	○

Notes: 1. To use this pin function, set the relevant pin to general-purpose input (set the PORT.PDR.Bm bit and PORT.PMR.Bm bit to 0).
2. Not present on products provided with a JTAG.
3. Not available on products without a sub-clock oscillator.

Table 2.32 Comparison of P0n Pin Function Control Registers (P0nPFS)

Register	Bit	RX630 (n = 0 to 3, 5, 7)	RX660 (n = 0 to 3, 5, 7)
P0nPFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits	Pin function select bits
	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P00: IRQ8 (144-pin) P01: IRQ9 (144-pin) P02: IRQ10 (144-pin) P03: IRQ11 (144/100*1/80/64-pin) P05: IRQ13 (144/100/80-pin) P07: IRQ15 (144/100/80/64-pin)

Note: 1. Not present on products provided with a JTAG.

Table 2.33 Comparison of P1n Pin Function Control Registers (P1nPFS)

Register	Bit	RX630 (n = 0 to 7)	RX660 (n = 2 to 7)
P10PFS	PSEL[4:0]	Pin function select bits	—
P11PFS	PSEL[4:0]	Pin function select bits	—
P12PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIC5U 00101b: TMCI1 01010b: RXD2/SMISO2/SSCL2 01111b: SCL0[FM+]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000101b: TMCI1 001010b: RXD2/SMISO2/SSCL2*1 001111b: SCL0
P13PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0B 00011b: TIOCA5 00101b: TMO3 00110b: PO13 01001b: ADTRG# 01010b: TXD2/SMOSI2/SSDA2 01111b: SDA0[FM+]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000101b: TMO3 001010b: TXD2/SMOSI2/SSDA2*1 001111b: SDA0

Register	Bit	RX630 (n = 0 to 7)	RX660 (n = 2 to 7)
P14PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKA 00011b: TIOCB5 00100b: TCLKA 00101b: TMRI2 00110b: PO15 01011b: CTS1#/RTS1#/SS1# 10000b: CTX1 10001b: USB0_DPUPE	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKA 000101b: TMRI2 001011b: CTS1#/RTS1#/SS1# 010000b: CTX0
P15PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKB 00011b: TIOCB2 00100b: TCLKB 00101b: TMCI2 00110b: PO13 01010b: RXD1/SMISO1/SSCL1 01011b: SCK3 10000b: CRXD1-DS	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKB 000101b: TMCI2 001010b: RXD1/SMISO1/SSCL1 001011b: SCK3 010000b: CRX0
P16PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTIOC3D 00011b: TIOCB1 00100b: TCLKC 00101b: TMO2 00110b: PO14 00111b: RTCOUT 01001b: ADTRG0# 01010b: TXD1/SMOSI1/SSDA1 01011b: RXD3/SMISO3/SSCL3 01101b: MOSIA 01111b: SCL2-DS 10000b: IERXD 10001b: USB0_VBUS	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTIOC3D 000101b: TMO2 000111b: RTCOUT*1 001001b: ADTRG0# 001010b: TXD1/SMOSI1/SSDA1 001011b: RXD3/SMISO3/SSCL3 001101b: MOSIA 001111b: SCL2

Register	Bit	RX630 (n = 0 to 7)	RX660 (n = 2 to 7)
P17PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTIOC3B 00011b: TIOCB0 00100b: TCLKD 00101b: TMO1 00110b: PO15 00111b: POE8# 01001b: ADTRG# 01010b: SCK1 01011b: TXD3/SMOSI3/SSDA3 01101b: MISOA 01111b: SDA2-DS 10000b: IETXD	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTIOC3B 000101b: TMO1 000111b: POE8# 001000b: MTIOC4B 001010b: SCK1 001011b: TXD3/SMOSI3/SSDA3 001101b: MISOA 001111b: SDA2 011110b: COMP2
P1nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P12: IRQ2 (144/100/80-pin) P13: IRQ3 (144/100/80-pin) P14: IRQ4 (144/100/80/64/48-pin) P15: IRQ5 (144/100/80/64/48-pin) P16: IRQ6 (144/100/80/64/48-pin) P17: IRQ7 (144/100/80/64/48-pin)
	ASEL	—	Analog function select bit

Note: 1. Not available on products without a sub-clock oscillator.

Table 2.34 Comparison of P2n Pin Function Control Registers (P2nPFS)

Register	Bit	RX630 (n = 0 to 7)	RX660 (n = 0 to 7)
P20PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC1A 00011b: TIOCB3 00101b: TMRI0 00110b: PO0 01010b: TXD0/SMOSI0/SSDA0 01111b: SDA1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC1A 000101b: TMRI0 001010b: TXD0/SMOSI0/SSDA0
P21PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC1B 00011b: TIOCA3 00101b: TMCI0 00110b: PO1 01010b: RXD0/SMISO0/SSCL0 01111b: SCL1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC1B 000101b: TMCI0 001000b: MTIOC4A 001010b: RXD0/SMISO0/SSCL0
P22PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3B 00010b: MTCLKC 00011b: TIOCC3 00101b: TMO0 00110b: PO2 01010b: SCK0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKC 000101b: TMO0 001010b: SCK0
P23PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3D 00010b: MTCLKD 00011b: TIOCD3 00110b: PO3 01010b: TXD3/SMOSI3/SSDA3 01011b: CTS0#/RTS0#/SS0#	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKD 001010b: TXD3/SMOSI3/SSDA3 001011b: CTS0#/RTS0#/SS0#
P24PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4A 00010b: MTCLKA 00011b: TIOCB4 00101b: TMRI1 00110b: PO4 01010b: SCK3	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000010b: MTCLKA 000101b: TMRI1 001010b: SCK3

Register	Bit	RX630 (n = 0 to 7)	RX660 (n = 0 to 7)
P25PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4C 00010b: MTCLKB 00011b: TIOCA4 00110b: PO5 01001b: ADTRG0# 01010b: RXD3/SMISO3/SSCL3	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000010b: MTCLKA 000101b: TMRI1 001001b: ADTRG0# 001010b: RXD3/SMISO3/SSCL3
P26PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC2A 00101b: TMO1 00110b: PO6 01010b: TXD1/SMOSI1/SSDA1 01011b: CTS3#/RTS3#/SS3# 01101b: MOSIB	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2A 000101b: TMO1 001010b: TXD1/SMOSI1/SSDA1 001011b: CTS3#/RTS3#/SS3#
P27PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC2B 00101b: TMCI3 00110b: PO7 01010b: SCK1 01101b: RSPCKB	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2B 000101b: TMCI3 001010b: SCK1
P2nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P20: IRQ8 (144/100/80-pin) P21: IRQ9 (144/100/80-pin) P22: IRQ15 (144/100-pin) P23: IRQ3 (144/100-pin) P24: IRQ12 (144/100-pin) P25: IRQ5 (144/100-pin) P26: IRQ6 (144/100/80/64/48-pin) P27: IRQ7 (144/100/80/64/48-pin)
	ASEL	—	Analog function select bit

Table 2.35 Comparison of P3n Pin Function Control Registers (P3nPFS)

Register	Bit	RX630 (n = 0 to 4)	RX660 (n = 0 to 4, 6, 7)
P30PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 00101b: TMRI3 00110b: PO8 00111b: POE8# 01010b: RXD1/SMISO1/SSCL1 01101b: MISOB	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000101b: TMRI3 000111b: POE8# 001010b: RXD1/SMISO1/SSCL1 011110b: COMP3
P31PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 00101b: TMCI2 00110b: PO9 01011b: CTS1#/RTS1#/SS1# 01101b: SSLB0 11001b: TS1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000101b: TMCI2 001010b: CTS1#/RTS1#/SS1#
P32PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0C 00011b: TIOCC0 00101b: TMO3 00110b: PO10 00111b: RTCOUT 01010b: TXD6/SMOSI6/SSDA6 01011b: TXD0/SMOSI0/SSDA0 10000b: CTX0*1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0C 000101b: TMO3 000111b: RTCOUT*1, *2 001000b: POE0# 001010b: TXD6/SMOSI6/SSDA6 001011b: TXD0/SMOSI0/SSDA0 010000b: CTX0 100001b: POE10#
P33PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0D 00011b: TIOCD0 00101b: TMRI3 00110b: PO11 00111b: POE3# 01010b: RXD6/SMISIO6/SSCL6 01011b: RXD0/SMISIO0/SSCL0 10000b: CRX0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0D 000101b: TMRI3 001000b: POE4# 001010b: RXD6/SMISIO6/SSCL6 001011b: RXD0/SMISIO0/SSCL0 010000b: CRX0 100001b: POE11#

Register	Bit	RX630 (n = 0 to 4)	RX660 (n = 0 to 4, 6, 7)
P34PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0A 00101b: TMCI3 00110b: PO12 00111b: POE2# 01010b: SCK6 01011b: SCK0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0A 000101b: TMCI3 000111b: POE10# 001010b: SCK6 001011b: SCK0
P3nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0-DS (144/100/80/64/48-pin) P31: IRQ1-DS (144/100/80/64/48-pin) P32: IRQ2-DS (144/100/80/64-pin) P33: IRQ3-DS (144/100-pin) P34: IRQ4 (144/100/80-pin) P36: IRQ5 (144/100/80/64/48-pin) P37: IRQ4 (144/100/80/64/48-pin)

Notes: 1. Not present on 100-pin products with a ROM capacity of 512 KB or less.
2. Not available on products without a sub-clock oscillator.

Table 2.36 Comparison of P4n Pin Function Control Registers (P4nPFS)

Register	Bit	RX630 (n = 0 to 7)	RX660 (n = 0 to 7)
P4nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P40: IRQ8-DS (144/100/80/64/48-pin) P41: IRQ9-DS (144/100/80/64/48-pin) P42: IRQ10-DS (144/100/80/64/48-pin) P43: IRQ11-DS (144/100/80/64-pin) P44: IRQ12-DS (144/100/80/64-pin) P45: IRQ13-DS (144/100/80/64/48-pin) P46: IRQ14-DS (144/100/80/64/48-pin) P47: IRQ15-DS (144/100/80/64/48-pin)

Register	Bit	RX630 (n = 0 to 7)	RX660 (n = 0 to 7)
P4nPFS	ASEL	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin P40: AN000 (144/100/80/64/48-pin) P41: AN001 (144/100/80/64/48-pin) P42: AN002 (144/100/80/64/48-pin) P43: AN003 (144/100/80/64-pin) P44: AN004 (144/100/80/64-pin) P45: AN005 (144/100/80/64/48-pin) P46: AN006 (144/100/80/64/48-pin) P47: AN007 (144/100/80/64/48-pin)

Table 2.37 Comparison of P5n Pin Function Control Registers (P5nPFS)

Register	Bit	RX630 (n = 0 to 2, 4 to 6)	RX660 (n = 0 to 6)
P50PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 01010b: TXD2/SMOSI2/SSDA2 01101b: SSLB1	Pin function select bits 000000b: Hi-Z 001010b: TXD2/SMOSI2/SSDA2
P51PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 01010b: SCK2 01101b: SSLB2	Pin function select bits 000000b: Hi-Z 001010b: SCK2 100110b: PMC0
P52PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 01010b: RXD2/SMISO2/SSCL2 01101b: SSLB3	Pin function select bits 000000b: Hi-Z 001010b: RXD2/SMISO2/SSCL2
P53PFS	PSEL[5:0]	—	P53 pin function select bits
P54PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 00101b: TMCI1 01011b: CTS2#/RTS2#/SS2# 10000b: CTX1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000101b: TMCI1 001011b: CTS2#/RTS2#/SS2# 010000b: CTX0

Register	Bit	RX630 (n = 0 to 2, 4 to 6)	RX660 (n = 0 to 6)
P55PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 00101b: TMO3 10000b: CRX1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000010b: MTIOC4A 000101b: TMO3 001010b: TXD7/SMOSI7/SSDA7 010000b: CRX0
P56PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3C 00011b: TIOCA1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 001010b: SCK7
P5nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P50: IRQ0 (144/100-pin) P51: IRQ1 (144/100-pin) P52: IRQ2 (144/100-pin) P53: IRQ3 (144/100-pin) P54: IRQ4 (144/100/80/64-pin) P55: IRQ10 (144/100/80/64-pin) P56: IRQ6 (144-pin)

Table 2.38 Comparison of P6n Pin Function Control Registers (P6nPFS)

Register	Bit	RX630 (n = 0, 1, 6, 7)	RX660 (n = 0 to 7)
P60PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	P60 pin function select bits	P60 pin function select bits
P61PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 01011b: CTS9#/RTS9#/SS9#	Pin function select bits 000000b: Hi-Z 001010b: CTS9#/RTS9#/SS9#
P66PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 10000b: CTX2*1	Pin function select bits 000000b: Hi-Z 001000b: MTIOC7D
P67PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 10000b: CRX2*1	Pin function select bits 000000b: Hi-Z 001000b: MTIOC7C
P6nPFS	ISEL	—	Interrupt input function select bit

Note: 1. Not present on products with a ROM capacity of 1 MB or less.

Table 2.39 Comparison of P7n Pin Function Control Registers (P7nPFS)

Register	Bit	RX630 (n = 0, 3 to 7)	RX660 (n = 0 to 7)
P70PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	P70 pin function select bits	P70 pin function select bits
P73PFS	PSEL[4:0]	P73 pin function select bits	—
P74PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00110b: PO19 01011b: CTS11#/RTS11/SS11#	Pin function select bits 000000b: Hi-Z 001011b: CTS11#/SS11# 101101b: CTS011#/SS011#
P75PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00110b: PO20 01010b: SCK11	Pin function select bits 000000b: Hi-Z 001010b: SCK11 001011b: RTS11# 101100b: SCK011 101101b: RTS011# 101110b: DE011
P76PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	P76 pin function select bits	P76 pin function select bits
P77PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	P77 pin function select bits	P77 pin function select bits
P7nPFS	—	—	Interrupt input function select bit

Table 2.40 Comparison of P8n Pin Function Control Registers (P8nPFS)

Register	Bit	RX630 (n = 0 to 3, 6, 7)	RX660(n = 0 to 3,6,7)
P80PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3B 00110b: PO26 01010b: SCK10	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 001010b: SCK10 001011b: RTS10# 101100b: SCK010 101101b: RTS010# 101110b: DE010
P81PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3D 00110b: PO27 01010b: RXD10/SMISO10/SSCL10	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 001010b: RXD10/SMISO10/SSCL10 101100b: RXD010/SMISO010/ SSCL010
P82PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4A 00110b: PO28 01010b: TXD10/SMOSI10/SSDA10	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 001010b: TXD10/SMOSI10/SSDA10 101100b: TXD010/SMOSI010/ SSDA010
P83PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4C 01011b: CTS10#/RTS10#/SS10#	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 001010b: SCK10 001011b: CTS10#/SS10# 101100b: SCK010 101101b: CTS010#/SS010#
P86PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00011b: TIOCA0	Pin function select bits 000000b: Hi-Z 001000b: MTIOC4D 001010b: RXD10/SMISO10/SSCL10 101100b: RXD010/SMISO010/ SSCL010
P87PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00011b: TIOCA2	Pin function select bits 000000b: Hi-Z 001000b: MTIOC4C 001010b: TXD10/SMOSI10/SSDA10 101100b: TXD010/SMOSI010/ SSDA010
P8nPFS	ISEL	—	Interrupt input function select bit

Table 2.41 Comparison of P9n Pin Function Control Registers (P9nPFS)

Register	Bit	RX630 (n = 0 to 3)	RX660 (n = 0 to 3)
P90PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	P90 pin function select bits	P90 pin function select bits
P91PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	P91 pin function select bits	P91 pin function select bits
P92PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 01010b: RXD7/SMISO7/SSCL7	Pin function select bits 000000b: Hi-Z 001000b: POE4# 001010b: RXD7/SMISO7/SSCL7
P93PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 01011b: CTS7#/RTS7#/SS7#	Pin function select bits 000000b: Hi-Z 001000b: POE0# 001011b: CTS7#/RTS7#/SS7#
P9nPFS	ASEL	Analog input function select bit	—
	ISEL	—	Interrupt input function select bit

Table 2.42 Comparison of PAn Pin Function Control Registers (PAnPFS)

Register	Bit	RX630 (n = 0 to 7)	RX660 (n = 0 to 7)
PA0PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4A 00011b: TIOCA0 00110b: PO16 01101b: SSLA1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000111b: CACREF 001000b: MTIOC6D 001101b: SSLA1
PA1PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKC 00011b: TIOCB0 00110b: PO17 01010b: SCK5 01101b: SSLA2	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKC 001000b: MTIOC7B 001001b: ADTRG0# 001010b: SCK5 001100b: SCK12 001101b: SSLA2 100111b: MTIOC3B

Register	Bit	RX630 (n = 0 to 7)	RX660 (n = 0 to 7)
PA2PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00110b: PO18 01010b: RXD5/SMISO5/SSCL5 01101b: SSLA3	Pin function select bits 000000b: Hi-Z 001000b: MTIOC7A 001010b: RXD5/SMISO5/SSCL5 001100b: RXD12/SMISO12/ SSCL12/RXDX12 001101b: SSLA3
PA3PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0D 00010b: MTCLKD 00011b: TIOCD0 00100b: TCLKB 00110b: PO19 01010b: RXD5/SMISO5/SSCL5	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0D 000010b: MTCLKD 001000b: MTIC5V 001010b: RXD5/SMISO5/SSCL5 100111b: MTIOC4D
PA4PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIC5U 00010b: MTCLKA 00011b: TIOCA1 00101b: TMRI0 00110b: PO20 01010b: TXD5/SMOSI5/SSDA5 01101b: SSLA0	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000010b: MTCLKA 000101b: TMRI0 001000b: MTIOC4C 001001b: ADST0 001010b: TXD5/SMOSI5/SSDA5 001100b: TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12 001101b: SSLA0 100111b: MTIOC7C
PA5PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00011b: TIOCB1 00110b: PO21 01101b: RSPCKA	Pin function select bits 000000b: Hi-Z 001000b: MTIOC6B 001101b: RSPCKA

Register	Bit	RX630 (n = 0 to 7)	RX660 (n = 0 to 7)
PA6PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIC5V 00010b: MTCLKB 00011b: TIOCA2 00101b: TMCI3 00110b: PO22 00111b: POE2# 01011b: CTS5#/RTS5#/SS5# 01101b: MOSIA	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000010b: MTCLKB 000101b: TMCI3 000111b: POE10# 001000b: MTIOC3D 001011b: CTS5#/RTS5#/SS5# 001100b: CTS12#/RTS12#/SS12# 001101b: MOSIA 100111b: MTIOC6B
PA7PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00011b: TIOCB2 00110b: PO23 01101b: MISOA	PA7 pin function select bits 000000b: Hi-Z 001101b: MISOA
PAnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA0: IRQ0 (144/100/80/64-pin) PA1: IRQ11 (144/100/80/64/48-pin) PA2: IRQ10 (144/100/80-pin) PA3: IRQ6-DS (144/100/80/64/48-pin) PA4: IRQ5-DS (144/100/80/64/48-pin) PA5: IRQ5 (144/100/80-pin) PA6: IRQ14 (144/100/80/64/48-pin) PA7: IRQ7 (144/100-pin)
	ASEL	—	Analog function select bit

Table 2.43 Comparison of PBn Pin Function Control Registers (PBnPFS)

Register	Bit	RX630 (n = 0 to 7)	RX660 (n = 0 to 7)
PB0PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIC5W 00011b: TIOCA3 00110b: PO24 01010b: RXD4/SMISO4/SSCL4 01011b: RXD6/SMISO6/SSCL6 01101b: RSPCKA	Pin function select bits 000000b: Hi-Z 000001b: MTIC5W 000010b: MTIOC3D 001010b: RXD4/SMISO4/SSCL4 001011b: RXD6/SMISO6/SSCL6 001101b: RSPCKA
PB1PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0C 00010b: MTIOC4C 00011b: TIOCB3 00101b: TMCI0 00110b: PO25 01010b: TXD4/SMOSI4/SSDA4 01011b: TXD6/SMOSI6/SSDA6	Pin function select bits 000000b: Hi-Z 000001b: MTIC0C 000010b: MTIOC4C 000101b: TMCI0 001010b: TXD4/SMOSI4/SSDA4 001011b: TXD6/SMOSI6/SSDA6 011110b: COMP1
PB2PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00011b: TIOCC3 00100b: TCLKC 00110b: PO26 01010b: CTS4#/RTS4#/SS4# 01011b: CTS6#/RTS6#/SS6#	Pin function select bits 000000b: Hi-Z 001010b: CTS4#/RTS4#/SS4# 001011b: CTS6#/RTS6#/SS6#
PB3PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0A 00010b: MTIOC4A 00011b: TIOCD3 00100b: TCLKD 00101b: TMO0 00110b: PO27 00111b: POE3# 01010b: SCK4 01011b: SCK6	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0A 000010b: MTIOC4A 000101b: TMO0 000111b: POE11# 001010b: SCK4 001011b: SCK6 011101b: TIC2 100110b: PMC0

Register	Bit	RX630 (n = 0 to 7)	RX660 (n = 0 to 7)
PB4PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00011b: TIOCA4 00110b: PO28 01011b: CTS9#/RTS9#/SS9#	Pin function select bits 000000b: Hi-Z 001011b: CTS9#/RTS9#/SS9# 100100b: CTS11#/RTS11#/SS11# 101100b: CTS011#/RTS011#/ SS011# 101110b: DE011
PB5PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC2A 00010b: MTIOC1B 00011b: TIOCB4 00101b: TMRI1 00110b: PO29 00111b: POE1# 01010b: SCK9	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2A 000010b: MTIOC1B 000101b: TMRI1 000111b: POE4# 001010b: SCK9 011101b: TOC2 100100b: SCK11 101100b: SCK011
PB6PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3D 00011b: TIOCA5 00110b: PO30 01010b: RXD9/SMISO9/SSCL9	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 001010b: RXD9/SMISO9/SSCL9 100100b: RXD11/SMISO11/ SSCL11 101100b: RXD011/SMISO011/ SSCL011
PB7PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3B 00011b: TIOCB5 00110b: PO31 01010b: TXD9/SMOSI9/SSDA9	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 001010b: TXD9/SMOSI9/SSDA9 100100b: TXD11/SMOSI11/ SSDA11 101100b: TXD011/SMOSI011/ SSDA011

Register	Bit	RX630 (n = 0 to 7)	RX660 (n = 0 to 7)
PBnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB0: IRQ12 (144/100/80/64/48-pin) PB1: IRQ4-DS (144/100/80/64/48-pin) PB2: IRQ2 (144/100/80-pin) PB3: IRQ3 (144/100/80/64/48-pin) PB4: IRQ4 (144/100/80-pin) PB5: IRQ13 (144/100/80/64/48-pin) PB6: IRQ6 (144/100/80/64-pin) PB7: IRQ15 (144/100/80/64-pin)

Table 2.44 Comparison of PCn Pin Function Control Registers (PCnPFS)

Register	Bit	RX630 (n = 0 to 7)	RX660 (n = 0 to 7)
PC0PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3C 00011b: TCLKC 00110b: PO17 01011b: CTS5#/RTS5#/SS5# 01101b: SSLA1 01111b: SCL3	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 001011b: CTS5#/RTS5#/SS5# 001101b: SSLA1 101110b: RXD011/SMISO011/SSCL011
PC1PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3A 00011b: TCLKD 00110b: PO18 01010b: SCK5 01101b: SSLA2 01111b: SDA3	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 001010b: SCK5 001101b: SSLA2 101100b: TXD011/SMOSI011/SSDA011/TXDA011
PC2PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 00011b: TCLKA 00110b: PO21 01010b: RXD5/SMISO5/SSCL5 01101b: SSLA3 10000b: IERXD	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 001010b: RXD5/SMISO5/SSCL5 001101b: SSLA3 101100b: TXDB011

Register	Bit	RX630 (n = 0 to 7)	RX660 (n = 0 to 7)
PC3PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 00011b: TCLKB 00110b: PO24 01010b: TXD5/SMOSI5/SSDA5 10000b: IETXD	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 001010b: TXD5/SMOSI5/SSDA5 100110b: PMC0
PC4PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3D 00010b: MTCLKC 00011b: TIOCC6 00100b: TCLKE 00101b: TMCI1 00110b: PO25 00111b: POE0# 01010b: SCK5 01011b: CTS8#/RTS8#/SS8# 01101b: SSLA0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKC 000101b: TMCI1 000111b: POE0# 001000b: MTIOC0A 001010b: SCK5 001011b: CTS8#/RTS8#/SS8# 001101b: SSLA0 100100b: CTS10#/RTS10#/SS10# 100110b: PMC0 101100b: CTS010#/RTS010#/ SS010# 101110b: DE010
PC5PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3B 00010b: MTCLKD 00011b: TIOCD6 00100b: TCLKF 00101b: TMRI2 00110b: PO29 01010b: SCK8 01101b: RSPCKA	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKD 000101b: TMRI2 001000b: MTIOC0C 001010b: SCK8 001101b: RSPCKA 100100b: SCK10 100110b: PMC0 101100b: SCK010

Register	Bit	RX630 (n = 0 to 7)	RX660 (n = 0 to 7)
PC6PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTCLKA 00011b: TIOCA6 00101b: TMCI2 00110b: PO30 01010b: RXD8/SMISO8/SSCL8 01101b: MOSIA	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTCLKA 000101b: TMCI2 001010b: RXD8/SMISO8/SSCL8 001101b: MOSIA 011101b: TIC0 100100b: RXD10/SMISO10/ SSCL10 101100b: RXD010/SMISO010/ SSCL010
PC7PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKB 00011b: TIOCB6 00101b: TMO2 00110b: PO31 01010b: TXD8/SMOSI8/SSDA8 01101b: MISOA	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKB 000101b: TMO2 000111b: CACREF 001010b: TXD8/SMOSI8/SSDA8 001101b: MISOA 011101b: TOC0 100100b: TXD10/SMOSI10/ SSDA10 101100b: TXD010/SMOSI010/ SSDA010
PCnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PC0: IRQ14 (144/100-pin) PC1: IRQ12 (144/100-pin) PC2: IRQ10 (144/100/80/64-pin) PC3: IRQ11 (144/100/80/64-pin) PC4: IRQ12 (144/100/80/64/48-pin) PC5: IRQ5 (144/100/80/64/48-pin) PC6: IRQ13 (144/100/80/64/48-pin) PC7: IRQ14 (144/100/80/64/48-pin)

Table 2.45 Comparison of PDn Pin Function Control Registers (PDnPFS)

Register	Bit	RX630 (n = 0 to 7)	RX660 (n = 0 to 7)
PD0PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00011b: TIOCA7	Pin function select bits 000000b: Hi-Z 001000b: POE4#
PD1PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 00011b: TIOCB7 00100b: TCLKG 01101b: MOSIC 10000b: CTX0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 001000b: POE0# 010000b: CTX0
PD2PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 00011b: TIOCA8 01101b: MISOC 10000b: CRX0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 010000b: CRX0 011101b: TIC2
PD3PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00011b: TIOCB8 00100b: TCLKH 00111b: POE8# 01101b: RSPCKC	Pin function select bits 000000b: Hi-Z 000111b: POE8# 001000b: MTIOC8D 011101b: TOC2
PD4PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00111b: POE3# 01101b: SSLC0	Pin function select bits 000000b: Hi-Z 000111b: POE11# 001000b: MTIOC8B
PD5PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIC5W 00111b: POE2# 01101b: SSLC1	Pin function select bits 000000b: Hi-Z 000001b: MTIC5W 000111b: POE10# 001000b: MTIOC8C
PD6PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIC5V 00111b: POE1# 01101b: SSLC2	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000111b: POE4# 001000b: MTIOC8A

Register	Bit	RX630 (n = 0 to 7)	RX660 (n = 0 to 7)
PD7PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIC5U 00111b: POE0# 01101b: SSLC3	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000111b: POE0#
PDnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PD0: IRQ0 (144/100/80-pin) PD1: IRQ1 (144/100/80-pin) PD2: IRQ2 (144/100/80-pin) PD3: IRQ3 (144/100-pin) PD4: IRQ4 (144/100-pin) PD5: IRQ5 (144/100-pin) PD6: IRQ6 (144/100-pin) PD7: IRQ7 (144/100-pin)
	ASEL	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin PD0: AN016 (144/100/80-pin) PD1: AN017 (144/100/80-pin) PD2: AN018 (144/100/80-pin) PD3: AN019 (144/100-pin) PD4: AN020 (144/100-pin) PD5: AN021 (144/100-pin) PD6: AN022 (144/100-pin) PD7: AN023 (144/100-pin)

Table 2.46 Comparison of PEn Pin Function Control Registers (PEnPFS)

Register	Bit	RX630 (n = 0 to 7)	RX660 (n = 0 to 7)
PE0PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00011b: TIOCC9 01100b: SCK12 01101b: SSLB1	Pin function select bits 000000b: Hi-Z 001000b: MTIOC3D 001100b: SCK12
PE1PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4C 00011b: TIOCD9 00110b: PO18 01100b: TXD12/SMOSI12/SSDA12 TXDX12/SIOX12 01101b: SSLB2 01110b: RSPCLKB	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 001000b: MTIOC3B 001100b: TXD12/TXDX12/SIOX12 SMOSI12/SSDA12

Register	Bit	RX630 (n = 0 to 7)	RX660 (n = 0 to 7)
PE2PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4A 00011b: TIOCA9 00110b: PO23 01100b: RXD12/SMISO12/SSCL12 RXDX12 01101b: SSLB3 01110b: MOSIB	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 001000b: MTIOC7A 001100b: RXD12/RXDX12/ SMISO12/SSCL12 011101b: TIC3
PE3PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 00011b: TIOCB9 00110b: PO26 00111b: POE8# 01100b: CTS12#/RTS12#/SS12# 01101b: MISOB	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000111b: POE8# 001000b: MTIOC1B 001100b: CTS12#/RTS12#/SS12# 011101b: TOC3
PE4PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 00010b: MTIOC1A 00011b: TIOCA10 00110b: PO28 01101b: SSLB0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000010b: MTIOC1A 001000b: MTIOC4A 100111b: MTIOC7D
PE5PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4C 00010b: MTIOC2B 00011b: TIOCB10 01101b: RSPCKB	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000010b: MTIOC2B 011110b: COMP0
PE6PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00011b: TIOCA11 01011b: CTS4#/RTS4#/SS4# 01101b: MOSIB	Pin function select bits 000000b: Hi-Z 001000b: MTIOC6C 001010b: CTS4#/RTS4#/SS4# 011101b: TIC1

Register	Bit	RX630 (n = 0 to 7)	RX660 (n = 0 to 7)
PE7PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00011b: TIOCB11 01101b: MISOB	Pin function select bits 000000b: Hi-Z 001000b: MTIOC6A 011101b: TOC1
PEnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE0: IRQ8 (144/100/80/64-pin) PE1: IRQ9 (144/100/80/64/48-pin) PE2: IRQ7-DS (144/100/80/64/48-pin) PE3: IRQ11 (144/100/80/64/48-pin) PE4: IRQ12 (144/100/80/64/48-pin) PE5: IRQ5 (144/100/80/64-pin) PE6: IRQ6 (144/100-pin) PE7: IRQ7 (144/100-pin)
	ASEL	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin PE0: AN008 (144/100/80/64-pin) PE1: AN009 (144/100/80/64/48-pin) PE2: AN010 (144/100/80/64/48-pin) PE3: AN011 (144/100/80/64/48-pin) PE4: AN012 (144/100/80/64/48-pin) PE5: AN013 (144/100/80/64-pin) PE6: AN014 (144/100-pin) PE7: AN015 (144/100-pin)

Table 2.47 Comparison of PF5 Pin Function Control Registers (PF5PFS)

Register	Bit	RX630 (n = 0 to 2, 5)	RX660 (PF5PFS)
PF0PFS	—	PF0 pin function control register	—
PF1PFS	—	PF1 pin function control register	—
PF2PFS	—	PF2 pin function control register	—
PFnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PF5: IRQ4 (144-pin)

Table 2.48 Comparison of PHn Pin Function Control Register (PHnPFS)

Register	Bit	RX630	RX660
PHnPFS	—	—	PHn pin function control register

Table 2.49 Comparison of PJn Pin Function Control Registers (PJnPFS)

Register	Bit	RX630 (PJ3PFS)	RX660 (n = 1, 3, 5)
PJ1PFS	PSEL[5:0]	—	PJ1 pin function select bits
PJ3PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits	Pin function select bits
PJ5PFS	PSEL[5:0]	—	PJ5 pin function select bits
PJnPFS	ISEL	—	Interrupt input function select bit

Table 2.50 Comparison of PKn Pin Function Control Registers (PKnPFS)

Register	Bit	RX630 (n = 2 to 5)	RX660 (n = 2 to 5)
PK2PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits	Pin function select bits
PK3PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits	Pin function select bits
PK4PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits	Pin function select bits
PK5PFS	PSEL[4:0] (RX630) PSEL[5:0] (RX660)	Pin function select bits	Pin function select bits

Table 2.51 Comparisons of Multi-Function Pin Controller Registers

Register	Bit	RX630	RX660
PFCSE	CS4E	CS4 enable bit	—
	CS5E	CS5 enable bit	—
	CS6E	CS6 enable bit	—
	CS7E	CS7 enable bit	—
PFCSS0	CS0S (RX630) CS0S[1:0]*1 (RX660)	CS0# output pin select bits 0: P60 is set as CS0# output pin. 1: PC7 is set as CS0# output pin.	CS0# output pin select bits b1 b0 0 0: P24 is set as CS0# output pin. 0 1: P60 is set as CS0# output pin. 1 x: PC7 is set as CS0# output pin.
	CS1S[1:0]*2	CS1# output pin select bits b3 b2 0 0: P61 is set as CS1# output pin. 0 1: P71 is set as CS1# output pin. 1 x: PC6 is set as CS1# output pin.	CS1# output pin select bits b3 b2 0 0: P25 is set as CS1# output pin. 0 1: P61 is set as CS1# output pin. 1 0: P71 is set as CS1# output pin. 1 1: PC6 is set as CS1# output pin.
	CS2S[1:0]*3	CS2# output pin select bits b5 b4 0 0: P62 is set as CS2# output pin. 0 1: P72 is set as CS2# output pin. 1 x: PC5 is set as CS2# output pin.	CS2# output pin select bits b5 b4 0 0: P26 is set as CS2# output pin. 0 1: P62 is set as CS2# output pin. 1 0: P72 is set as CS2# output pin. 1 1: PC5 is set as CS2# output pin.
PFCSS0	CS3S[1:0]*4	CS3# output pin select bits b7 b6 0 0: P63 is set as CS3# output pin. 0 1: P73 is set as CS3# output pin. 1 x: PC4 is set as CS3# output pin.	CS3# output pin select bits b7 b6 0 0: P27 is set as CS3# output pin. 0 1: P63 is set as CS3# output pin. 1 0: P73 is set as CS3# output pin. 1 1: PC4 is set as CS3# output pin.
PFCSS1	—	CS output pin select register 1	—
PFAOE1	A21E	Address A21 output enable bit	—
	A22E	Address A22 output enable bit	—
	A23E	Address A23 output enable bit	—
PFBCR0	ADRHMS	A16 to A23 output enable bit	A16 to A20 output enable bit
	ADRHMS2	—	A16 to A20 output enable 2 bit
	BCLKO	—	BCLK forced output bit
	DH32E	D16 to D31 output enable bit	—
	WR32BC32E	WR3#/BC3# output enable bit WR2#/BC2# output enable bit	—
PFBCR1	WAITS[1:0]	WAIT select bits b1 b0 0 0: P57 is set as WAIT# input pin. 0 1: P55 is set as WAIT# input pin. 1 0: PC5 is set as WAIT# input pin. 1 1: P51 is set as WAIT# input pin.	WAIT select bits b1 b0 0 0: Setting disabled*5 0 1: P55 is set as WAIT# input pin. 1 0: PC5 is set as WAIT# input pin. 1 1: P51 is set as WAIT# input pin.
PFBCR2	—	—	External bus control register 2

Register	Bit	RX630	RX660
PFBCR3	—	—	External bus control register 3
PFUSB0	—	USB0 control register	—

Notes: 1. Because P60 is not present in 100-pin products, do not set the CS0S[1:0] bits of those products to 01b.
2. Because P61 and P71 are not present in 100-pin products, do not set the CS1S[1:0] bits of those products to 01b or 10b.
3. Because P62 and P72 are not present in 100-pin products, do not set the CS2S[1:0] bits of those products to 01b or 10b.
4. Because P63 and P73 are not present in 100-pin products, do not set the CS3S[1:0] bits of those products to 01b or 10b.
5. Even if these pins are set to 00b in 144-pin and 100-pin products, P55 is set as WAIT# input pin.

2.17 Multi-Function Timer Pulse Unit 2 and Multi-Function Timer Pulse Unit 3

Table 2.52 is a Comparative Overview of Multi-function Timer Pulse Unit 2 and Multi-function Timer Pulse Unit 3, and Table 2.53 is a Comparison of Registers of Multi-function Timer Pulse Unit 2 and Multi-function Timer Pulse Unit 3.

Table 2.52 Comparative Overview of Multi-function Timer Pulse Unit 2 and Multi-function Timer Pulse Unit 3

Item	RX630 (MTU2a)	RX660 (MTU3a)
Pulse input/output	Max. 16 lines	Max. 28 lines
Pulse input	3 lines	3 lines
Count clocks	Eight or seven clocks for each channel (four clocks for MTU5)	11 clocks for each channel (14 clocks for MTU0, 12 clocks for MTU2, 10 clocks for MTU5, and 4 clocks for MTU1 and MTU2 (when LWA = 1))
Available operations	[MTU0 to MTU4] • Waveform output on compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing on compare match or input capture • Synchronous input/output on each register by synchronous counter operation • Up to 12-phase PWM output in combination with synchronous operation	[MTU0 to MTU4, MTU6, MTU7, MTU8] • Waveform output on compare match • Input capture function (noise filter setting available) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) (excluding MTU8) • Simultaneous clearing by compare match or input capture (excluding MTU8) • Synchronous input/output on each register by synchronous counter operation (excluding MTU8) • Up to 12-phase PWM output in combination with synchronous operation (excluding MTU8)
	[MTU0, MTU3, MTU4] • Buffer operation specifiable • A mode for driving AC synchronous motors (brushless DC motors) by using complementary PWM output or reset-synchronized PWM output can be set, and the waveform output is selectable from two types (chopping and level).	[MTU0, MTU3, MTU4, MTU6, MTU7, MTU8] • Buffer operation specifiable
	[MTU1, MTU2] • Phase counting mode can be specified independently. • Cascade connection operation	[MTU1, MTU2] • Phase counting mode can be specified independently. • 32-bit phase counting mode can be specified for interlocked operation of MTU1 and MTU2 (when TMDR3.LWA = 1). • Cascade connection operation available

Item	RX630 (MTU2a)	RX660 (MTU3a)
Available operations	—	[MTU3, MTU4, MTU6, MTU7] • Through interlocked operation of MTU3/MTU4 and MTU6/MTU7, the positive and negative signals in six phases (12-phases in total) can be output in complementary PWM and reset-synchronized PWM operation. • In complementary PWM mode, data can be transferred from buffer registers to temporary registers on crests or troughs of the timer-counter values or when writing to buffer registers (MTU4.TGRD and MTU7.TGRD). • Double buffering function can be specified in complementary PWM mode.
	[MTU3, MTU4] • A total of six-phase waveform output, which includes three phases each for positive and negative complementary PWM or reset PWM output, by interlocking operation	[MTU3, MTU4] • Through interlocking with MTU0, a mode for driving AC synchronous motors (brushless DC motors) by using complementary PWM output or reset-synchronized PWM output can be set, and waveform output is selectable from two types (chopping and level).
	[MTU5] • Dead time compensation counter function	[MTU5] • Capable of operation as a dead time compensation counter
	—	[MTU0/MTU5, MTU1, MTU2, MTU8] 32-bit phase counting mode can be specified by combining MTU1 and MTU2 and through interlocked operation with MTU0/MTU5 and MTU8.
Interrupt skipping function	In complementary PWM mode • Interrupts at counter peaks or troughs • Function for skipping A/D converter conversion start triggers	Interrupts on crests and troughs of counter values and triggers to start conversion by the A/D converter can be skipped in complementary PWM mode.
Interrupt sources	28 sources	43 sources
Buffer operation	Automatic transfer of register data	Automatic transfer of register data (from the buffer register to the timer register)
Trigger generation	• Triggers to start conversion by A/D converter can be generated.	• Triggers to start conversion by A/D converter can be generated. • The A/D conversion start request delaying function enables A/D conversion to be started with any desired timing. Synchronized operation with PWM output is also possible.
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Table 2.53 Comparison of Registers of Multi-function Timer Pulse Unit 2 and Multi-function Timer Pulse Unit 3

Register	Bit	RX630 (MTU2a)	RX660 (MTU3a)
TCR2	—	—	Timer control register 2
TMDR(RX630) TMDR1(RX660)	—	Timer mode register	Timer mode register 1
TMDR2m	—	—	Timer mode register 2 (m = A or B)
TMDR3	—	—	Timer mode register 3

Register	Bit	RX630 (MTU2a)	RX660 (MTU3a)
MTU0, TIORH	IOA[3:0]	I/O control A bits b3 b0 0 0 0 0: Output disabled 0 0 0 1: Initial output is low. Low output at compare match 0 0 1 0: Initial output is low. High output at compare match 0 0 1 1: Initial output is low. Output toggled at compare match 0 1 0 0: Output disabled 0 1 0 1: Initial output is high. Low output at compare match 0 1 1 0: Initial output is high. High output at compare match 0 1 1 1: Initial output is high. Output toggled at compare match 1 0 0 0: Input capture at rising edge 1 0 0 1: Input capture at falling edge 1 0 1 x: Input capture at both edges 1 1 x x: Capture input source is clock count in MTU1. Input capture on counting up or down by MTU1.TCNT	I/O control A bits b3 b0 0 0 0 0: Output disabled 0 0 0 1: Initial output is low. Low output at compare match 0 0 1 0: Initial output is low. High output at compare match 0 0 1 1: Initial output is low. Output toggled at compare match 0 1 0 0: Output disabled 0 1 0 1: Initial output is high. Low output at compare match 0 1 1 0: Initial output is high. High output at compare match 0 1 1 1: Initial output is high. Output toggled at compare match 1 0 0 0: Input capture at rising edge 1 0 0 1: Input capture at falling edge 1 0 1 x: Input capture at both edges 1 1 0 0: Capture input source is count clock in MTU1. Input capture on counting up or down by MTU1.TCNT (LWA = 0) or MTU1.TCNTLW (LWA = 1) 1 1 1 x: Input capture on generation of compare match with MTU8.TGRC

Register	Bit	RX630 (MTU2a)	RX660 (MTU3a)
MTU1, TIOR	IOB[3:0]	I/O control B bits b3 b0 0 0 0 0: Output disabled 0 0 0 1: Initial output is low. Low output at compare match 0 0 1 0: Initial output is low. High output at compare match 0 0 1 1: Initial output is low. Output toggled at compare match 0 1 0 0: Output disabled 0 1 0 1: Initial output is high. Low output at compare match 0 1 1 0: Initial output is high. High output at compare match 0 1 1 1: Initial output is high. Output toggled at compare match 1 0 0 0: Input capture at rising edge 1 0 0 1: Input capture at falling edge 1 0 1 x: Input capture at both edges 1 1 x x: Input capture on generation of compare match with MTU0.TGRC	I/O control B bits b3 b0 0 0 0 0: Output disabled 0 0 0 1: Initial output is low. Low output at compare match 0 0 1 0: Initial output is low. High output at compare match 0 0 1 1: Initial output is low. Output toggled at compare match 0 1 0 0: Output disabled 0 1 0 1: Initial output is high. Low output at compare match 0 1 1 0: Initial output is high. High output at compare match 0 1 1 1: Initial output is high. Output toggled at compare match 1 0 0 0: Input capture at rising edge 1 0 0 1: Input capture at falling edge 1 0 1 x: Input capture at both edges 1 1 0 0: Input capture on generation of compare match with MTU0.TGRC 1 1 1 x: Input capture on generation of compare match with MTU8.TGRC

Register	Bit	RX630 (MTU2a)	RX660 (MTU3a)
TIORU TIORV TIORW	IOC[4:0]	I/O control C bits b4 b0 0 0 0 0 0: Compare match 0 0 0 0 1: Setting prohibited. 0 0 0 1 x: Setting prohibited. 0 0 1 x x: Setting prohibited. 0 1 x x x: Setting prohibited. 1 0 0 0 0: Setting prohibited. 1 0 0 0 1: Input capture at rising edge 1 0 0 1 0: Input capture at falling edge 1 0 0 1 1: Input capture at both edges 1 0 1 x x: Setting prohibited. 1 1 0 0 0: Setting prohibited. 1 1 0 0 1: Measurement of low pulse width of external input signal. Capture at trough in complementary PWM mode. 1 1 0 1 0: Measurement of low pulse width of external input signal. Capture at crest of complementary PWM mode. 1 1 0 1 1: Measurement of low pulse width of external input signal. Capture at crest and trough of complementary PWM mode. 1 1 1 0 0: Setting prohibited. 1 1 1 0 1: Measurement of high pulse width of external input signal. Capture at trough in complementary PWM mode. 1 1 1 1 0: Measurement of high pulse width of external input signal. Capture at crest of complementary PWM mode. 1 1 1 1 1: Measurement of high pulse width of external input signal. Capture at crest and trough of complementary PWM mode.	I/O control C bits b4 b0 0 0 0 0 0: No function 0 0 0 0 1: Setting prohibited. 0 0 0 1 x: Setting prohibited. 0 0 1 x x: Setting prohibited. 0 1 x x x: Setting prohibited. 1 0 0 0 0: Setting prohibited. 1 0 0 0 1: Input capture at rising edge 1 0 0 1 0: Input capture at falling edge 1 0 0 1 1: Input capture at both edges 1 0 1 x x: Capture on generation of compare match with MTU8.TGRC 1 1 0 0 0: Setting prohibited. 1 1 0 0 1: Measurement of low pulse width of external input signal. Capture at trough in complementary PWM mode. 1 1 0 1 0: Measurement of low pulse width of external input signal. Capture at crest of complementary PWM mode. 1 1 0 1 1: Measurement of low pulse width of external input signal. Capture at crest and trough of complementary PWM mode. 1 1 1 0 0: Setting prohibited. 1 1 1 0 1: Measurement of high pulse width of external input signal. Capture at trough in complementary PWM mode. 1 1 1 1 0: Measurement of high pulse width of external input signal. Capture at crest of complementary PWM mode. 1 1 1 1 1: Measurement of high pulse width of external input signal. Capture at crest and trough of complementary PWM mode.

Register	Bit	RX630 (MTU2a)	RX660 (MTU3a)
TIER	TTGE2	A/D conversion start request enable 2 bit 0: Generation of A/D conversion start request by MTU4.TCNT disabled 1: Generation of A/D conversion start request by MTU4.TCNT enabled	A/D conversion start request enable 2 bit 0: Generation of A/D conversion start request by MTUn.TCNT (n = 4 or 7) underflow (trough) disabled 1: Generation of A/D conversion start request by MTUn.TCNT (n = 4 or 7) underflow (trough) enabled
TSYCR	—	—	Timer synchronization clear Register
TCNTLW	—	—	Timer longword counter
TGRALW/ TGRBLW	—	—	Timer longword general register
TSTR (RX630) TSTR/TSTRA/TSTRB (RX660)	CST8	—	Count start 8 bit
TSYR (RX630) TSYRm (RX660)	—	Timer synchronization register	Timer synchronization register m (m = A or B)
TCSYSTR	—	—	Timer counter synchronization start register
TRWER (RX630) TRWERm (RX660)	—	Timer read enable register	Timer read/write enable register m (m = A or B)
TOER (RX630) TOERm (RX660)	—	Timer output master enable register	Timer output master enable register m (m = A or B)
TOCR1 (RX630) TOCR1m (RX660)	—	Timer output control register 1	Port output control register 1m (m = A or B)
TOCR2 (RX630) TOCR2m (RX660)	—	Timer output control register 2	Port output control register 2m (m = A or B)
TOLBR TOLBRm (RX660)	—	Timer output level buffer register	Timer output level buffer register m (m = A or B)
TGCR (RX630) TGCRA (RX660)	—	Timer gate control register	Timer gate control register A
TCNTS (RX630) TCNTSm (RX660)	—	Timer sub-counter	Timer sub-counter m (m = A or B)
TCDR (RX630) TCDRm (RX660)	—	Timer period data register	Timer period data register m (m = A or B)
TCBR (RX630) TCBRm (RX660)	—	Timer period buffer register	Timer period buffer register m (m = A or B)
TDDR (RX630) TDDRm (RX660)	—	Timer dead time data register	Timer dead time data register m (m = A or B)
TITCR (RX630) TITCR1m (RX660)	—	Timer interrupt skipping setting register	Timer interrupt skipping setting register 1m (m = A or B)
TITCNT (RX630) TITCNT1m (RX660)	—	Timer interrupt skipping counter	Timer interrupt skipping counter 1m (m = A or B)
TBTER (RX630) TBTERm (RX660)	—	Timer buffer transfer setting register	Timer buffer transfer setting register m (m = A or B)
TDER (RX630) TDERm (RX660)	—	Timer dead time enable register	Timer dead time enable register m (m = A or B)
TWCR (RX630) TWCRm (RX660)	SCC	—	Synchronization clear control bit
NFCR (RX630) NFCRn (RX660)	—	Noise filter control register	Noise filter control register n (n = 0 to 4, 6, 7, 8, C)
NFCR5	—	—	Noise filter control register 5

Register	Bit	RX630 (MTU2a)	RX660 (MTU3a)
TITMRm	—	—	Timer interrupt skipping mode register (m = A or B)
TITCR2m	—	—	Timer interrupt skipping setting register 2 (m = A or B)
TITCNT2m	—	—	Timer interrupt skipping counter 2 (m = A or B)

2.18 Port Output Enable 2/Port Output Enable 3

Table 2.54 is a Comparative Overview of Port Output Enable 2 and Port Output Enable 3, and Table 2.55 is a Comparison of Port Output Enable 2 and Port Output Enable 3 Registers.

Table 2.54 Comparative Overview of Port Output Enable 2 and Port Output Enable 3

Item	RX630 (POE2a)	RX660 (POE3a)
Pin status while output is disabled	• High impedance	High impedance
Target pins for switching to high-impedance state	• MTU output pins — MTU0 pin (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) — MTU3 pin (MTIOC3B, MTIOC3D) — MTU4 pin (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D)	• MTU output pins — MTU0 pin (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) — MTU3 pin (MTIOC3B, MTIOC3D) — MTU4 pin (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) — MTU6 pin (MTIOC6B, MTIOC6D) — MTU7 pin (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D)
Generating conditions of request for switching to high-impedance state	• Input signal detection Detection of the POE0# to POE3# or POE8# signal level • Simultaneous conduction between output pins Levels output on pins for complementary PWM output from the MTU are compared, and when simultaneous output of the active level continues for one or more cycles, the pins can be placed in the high-impedance state. [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D • SPOER register setting • Detection that the clock generation circuit stopped oscillating	• Input signal detection Detection of the POE0#, POE4#, POE8#, POE10#, or POE11# signal level. • Simultaneous conduction between output pins A match (simultaneous conduction) between the output signal levels at the active level over one or more cycles on the following combination of pins: [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D — MTIOC6B and MTIOC6D — MTIOC7A and MTIOC7C — MTIOC7B and MTIOC7D • SPOER register setting • Detection that the main clock generation circuit stopped oscillating
Functions	• Falling-edge detection or sampling of the low level (16 times at PCLK/8, PCLK/16, or PCLK/128) can be set for each of the POE0# to POE3#, and POE8# input pins.	• Falling-edge detection or sampling of the low level (16 times at PCLK/8, PCLK/16, or PCLK/128) can be set for each of the POE0#, POE4#, POE8#, POE10#, and POE11# input pins.

Item	RX630 (POE2a)	RX660 (POE3a)
Functions	• Pins for complementary PWM output from the MTU can be placed in the high-impedance state on detection of falling edges or sampling of the low level of the POE0# to POE3# pins. • Pins for output from MTU0 can be placed in the high-impedance state on detection of the falling edges or sampling of the low level of the POE8# pin. • The MTU complementary PWM output pins and MTU0 output pin can be set to the high impedance state when the clock pulse generator stops oscillation. • Levels output on pins for complementary PWM output from the MTU are compared, and when simultaneous output of the active level continues for one or more cycles, the pins can be placed in the high-impedance state. • The MTU complementary PWM output pins and MTU0 output pin can be set to the high impedance state by writing to the POE registers. • Interrupts are generated in response to the results of input level detection of POE0# to POE3#, and POE8#, and output level comparison of MTU complementary PWM output pins.	• Output of all control target pins can be placed in the high-impedance state on detection of the falling edge or sampling of the low level of the POE0#, POE4#, POE8#, POE10#, and POE11# pins. • Output on all control target pins can be placed in the high-impedance state when oscillation stop is detected in the clock generation circuit. • The MTU complementary PWM outputs can be placed in the high-impedance state when output levels of the MTU complementary PWM output pins are compared and simultaneous active-level output continues for one cycle or more. • Output on all control target pins can be put in the high-impedance state by modifying settings of POE3 registers. • Interrupts can be generated in response to input-level sampling or output-level comparison results.

Table 2.55 Comparison of Port Output Enable 2 and Port Output Enable 3 Registers

Register	Bit	RX630 (POE2a)	RX660 (POE3a)
ICSR1	POE1M[1:0]	POE1 mode select bits	—
	POE2M[1:0]	POE2 mode select bits	—
	POE3M[1:0]	POE3 mode select bits	—
	POE1F	POE1 flag	—
	POE2F	POE2 flag	—
	POE3F	POE3 flag	—
ICSR2	POE8M[1:0]	POE8 mode select bits	—
	POE4M[1:0]	—	POE4 mode select bits
	POE8E	POE8 high-impedance enable bit	—
	POE8F	POE8 flag	—
	POE4F	—	POE4 flag
ICSR3	OSTSTE	OSTST high-impedance enable bit	—
	OSTSTF	OSTST high impedance flag	—
	POE8M[1:0]	—	POE8 mode select bits
	PIE3	—	Port interrupt enable 3 bit
	POE8E	—	POE8 high-impedance enable bit
	POE8F	—	POE8 flag
ICSR4	—	—	Input level control/status register 4
ICSR5	—	—	Input level control/status register 5
ICSR6	—	—	Input level control/status register 6

Register	Bit	RX630 (POE2a)	RX660 (POE3a)
OCSR2	—	—	Output level control/status register 2
ALR1	—	—	Active level register 1
SPOER	CH34HIZ (RX630) MTUCH34HIZ (RX660)	MTU3 and MTU4 output high-impedance enable bit	MTU3 and MTU4 pin high-impedance enable bit
	MTUCH67HIZ	—	MTU6 and MTU7 pin high-impedance enable bit
	CH0HIZ (RX630) MTUCH0HIZ (RX660)	MTU0 output high-impedance enable bit (b1)	MTU0 pin high-impedance enable bit (b2)
POECR1	PE0ZE (RX630) MTU0AZE (RX660)	MTIOC0A high-impedance enable bit	MTIOC0A pin high-impedance enable bit
	PE1ZE (RX630) MTU0BZE (RX660)	MTIOC0B high-impedance enable bit	MTIOC0B pin high-impedance enable bit
	PE2ZE (RX630) MTU0CZE (RX660)	MTIOC0C high-impedance enable bit	MTIOC0C pin high-impedance enable bit
	PE3ZE (RX630) MTU0DZE (RX660)	MTIOC0D high-impedance enable bit	MTIOC0D pin high-impedance enable bit
POECR2	—	Port output enable control register 2 POECR2 is an 8-bit register.	Port output enable control register 2 POECR2 is a 16-bit register.
	MTU7BDZE	—	MTIOC7B/MTIOC7D pin high-impedance enable bit
	MTU7ACZE	—	MTIOC7A/MTIOC7C pin high-impedance enable bit
	MTU6BDZE	—	MTIOC6B/MTIOC6D pin high-impedance enable bit
	P3CZEA (RX630) MTU4BDZE (RX660)	MTU port 3 high-impedance enable bit (b4)	MTIOC4B/MTIOC4D pin high-impedance enable bit (b8)
	P2CZEA (RX630) MTU4ACZE (RX660)	MTU port 2 high-impedance enable bit (b5)	MTIOC4A/MTIOC4C pin high-impedance enable bit (b9)
	P1CZEA (RX630) MTU3BDZE (RX660)	MTU port 1 high-impedance enable bit (b6)	MTIOC3B/MTIOC3D pin high-impedance enable bit (b10)
POECR4	—	—	Port output enable control register 4
POECR5	—	—	Port output enable control register 5
M0SELR1	—	—	MTU0 pin select register 1

Register	Bit	RX630 (POE2a)	RX660 (POE3a)
M0SELR2	—	—	MTU0 pin select register 2
M3SELR	—	—	MTU3 pin select register
M4SELR1	—	—	MTU4 pin select register 1
M4SELR2	—	—	MTU4 pin select register 2

2.19 8-Bit Timer

Table 2.56 is a Comparative Overview of 8-Bit Timers, and Table 2.57 is a Comparison of 8-Bit Timers.

Table 2.56 Comparative Overview of 8-Bit Timers

Item	RX630 (TMR)	RX660 (TMRb)
Count clocks	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock: External count clock
Number of channels	(8 bits × 2 channels) × 2 units	(8 bits × 2 channels) × 2 units
compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selectable among compare match A or B, or an external reset signal.	Selectable among compare match A or B, or an external counter reset signal.
Timer output	Output pulses with a user-defined duty cycle or PWM output	Output pulses with a user-defined duty cycle or PWM output
Cascading of two channels	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
Event link function (output)	—	Compare match A, compare match B, and overflow (TMR0 to TMR3)
Event link function (input)	—	Ability to perform one of three actions according to accepted event (1) Counter start (TMR0 to TMR3) (2) Event counter (TMR0 to TMR3) (3) Counter restart (TMR0 to TMR3)
DTC activation	The DTC can be activated by compare match A interrupts or compare match B interrupts.	The DTC can be activated by compare match A interrupts or compare match B interrupts.
Generation of trigger to start A/D converter	Compare match A of TMR0 or TMR2	Compare match A of TMR0 or TMR2
Generation of SCI basic clock	Generation of baud rate clock for SCI	Generation of SCI basic clock
Generation of REMC operation clock	—	Generation of REMC (remote control signal receiver) operation clock
Low power consumption function	Ability to transition each unit to the module stop state	Ability to transition each unit to the module stop state

Table 2.57 Comparison of 8-Bit Timers Registers

Register	Bit	RX630 (TMR)	RX660 (TMRb)
TCSTR	—	—	Timer counter start register

2.20 Compare Match Timer (CMT)

Table 2.58 is a Comparative Overview of Compare Match Timer.

Table 2.58 Comparative Overview of Compare Match Timer

Item	RX630 (CMT)	RX660 (CMT)
Number of channels	4 channel	4 channel
Count clocks	Four frequency dividing clocks One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.	Four frequency dividing clocks One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.
Interrupts	A compare match interrupt can be requested for each channel.	A compare match interrupt can be requested for each channel.
Event link function (output)	—	An event signal is output at a CMT1 compare match.
Event link function (input)	—	Linking operations for the specified module is possible. CMT1 count start, event counter, and count restart operations are possible.
Low power consumption function	Ability to transition each unit to the module stop state	Ability to transition each unit to the module stop state

2.21 Realtime Clock

Table 2.59 is a Comparative Overview of Realtime Clocks, and Table 2.60 is a Comparison of Realtime Clock Registers.

Table 2.59 Comparative Overview of Realtime Clocks

Item	RX630 (RTCa)	RX660 (RTCC)
Count modes	Calendar count mode	Calendar count mode/binary count mode
Count source	Sub-clock (XCIN) or main clock (EXTAL)	Sub-clock (XCIN)
Clock and calendar functions	• Year, month, date, day-of-week, hour, minute, second are counted and represented in BCD. • 12 hours/24 hours mode switching function • 30 seconds adjustment function (a number less than 30 is rounded down to 00 seconds, and 30 seconds or more are rounded up to one minute) • Automatic adjustment function for leap years • Start/stop function • Indicates the state of 1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, or 64 Hz in binary • Clock error correction function • 1 Hz clock output	• Calendar count mode Year, month, date, day-of-week, hour, minute, second are counted, BCD display 12 hours/24 hours mode switching function 30 seconds adjustment function (a number less than 30 is rounded down to 00 seconds, and 30 seconds or more are rounded up to one minute) Automatic adjustment function for leap years • Binary count mode Count seconds in 32 bits, binary display • Common to both modes Start/stop function The sub-second digit is displayed in binary units (1Hz, 2Hz, 4Hz, 8Hz, 16Hz, 32 Hz, or 64 Hz). • Clock error correction function • Clock (1 Hz/64 Hz) output

Item	RX630 (RTCa)	RX660 (RTCC)
Interrupts	• Alarm interrupt (ALM) As an alarm interrupt condition, selectable which of the year, month, date, day-of-week, hour, minute, or second is compared.	• Alarm interrupt (ALM) As an alarm interrupt condition, selectable which of the below is compared with: — Calendar count mode: Year, month, date, day-of-week, hour, minute, or second — Binary count mode: Each bit of the 32-bit binary counter
	• Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second,1/64second, 1/128 second, or 1/256 second can be selected as an interrupt period.	• Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second,1/64second, 1/128 second, or 1/256 second can be selected as an interrupt period.
	• Carry interrupt (CUP) An interrupt is generated when a carry to the second counter is generated or when the 64-Hz counter is changed and the 64-Hz register is read at the same time.	• Carry interrupt (CUP) An interrupt request is generated at either of the following timings: — When a carry from the 64 Hz counter to the second counter is generated. — When the 64-Hz counter is changed and the R64CNT register is read at the same time.
	• Recovery from software standby mode or deep software standby mode can be performed by an alarm interrupt or periodic interrupt.	• Recovery from software standby mode or deep software standby mode can be performed by an alarm interrupt or periodic interrupt.
Time-capture function	Times can be captured by three event inputs. For every event input, the month, date, hour, minute, and second are captured.	Times can be captured by detecting an edge of a signal on a time capture event input pin. For every event input, the month, date, hour, minute, and second or the 32-bit binary counter value is captured.
Event link function	—	Periodic event output

Table 2.60 Comparison of Realtime Clock Registers

Register	Bit	RX630 (RTCa)	RX660 (RTCC)
BCNT0*1	—	—	Binary counter 0
BCNT1*1	—	—	Binary counter 1
BCNT2*1	—	—	Binary counter 2
BCNT3*1	—	—	Binary counter 3
BCNT0AR*1	—	—	Binary counter 0 alarm register
BCNT1AR*1	—	—	Binary counter 1 alarm register
BCNT2AR*1	—	—	Binary counter 2 alarm register
BCNT3AR*1	—	—	Binary counter 3 alarm register
BCNT0AER*1	—	—	Binary counter 0 alarm enable register
BCNT1AER*1	—	—	Binary counter 1 alarm enable register

Register	Bit	RX630 (RTCa)	RX660 (RTCC)
BCNT2AER*1	—	—	Binary counter 2 alarm enable register
BCNT3AER*1	—	—	Binary counter 3 alarm enable register
RCR1	RTCOS	—	RTCOUT output select bit
RCR2	CNTMD	—	Count mode select bit
RCR3	RTCEN	Sub-clock oscillator control bit 0: Sub-clock oscillator is stopped. 1: Sub-clock oscillator is operating.	RTC enable bit 0: RTC is disabled. 1: RTC is enabled.
RCR4	RCKSEL	Count source select bit 0: Sub-clock is selected. 1: Main clock is selected.	Count source select bit 0: Sub-clock is selected. 1: Settings prohibited.
RFRH/L	—	Frequency register H/L	—
BCNT0CPn	—	—	BCNT0 capture register n (n = 0 to 2)
BCNT1CPn	—	—	BCNT1 capture register n (n = 0 to 2)
BCNT2CPn	—	—	BCNT2 capture register n (n = 0 to 2)
BCNT3CPn	—	—	BCNT3 capture register n (n = 0 to 2)

Note: 1. In binary count mode

2.22 Watchdog Timer

Table 2.61 is a Comparative Overview of Watch Dog Timers.

Table 2.61 Comparative Overview of Watch Dog Timers

Item	RX630 (WDTA)	RX660 (WDTA)
Count source	Peripheral clock (PCLK)	Peripheral module clock (PCLK)
Clock division ratio	Divided by 4, 64, 128, 512, 2048, or 8192	Divided by 4, 64, 128, 512, 2048, or 8192
Counter operation	Counting down by a 14-bit down-counter	Counting down by a 14-bit down-counter
Count start conditions	• Counting automatically starts after a reset (auto-start mode). • Counting is started by refreshing the counter (writing 00h and then FFh to the WDTRR register) (register start mode).	Auto-start mode: Counting automatically starts after a reset. • Register start mode: Counting is started by the refresh operation (writing 00h and then FFh to the WDTRR register).
Count stop conditions	• Reset (The down-counter and other registers return to their initial values.) • A counter underflows or a refresh error occurs. Counting restarts automatically in auto-start mode, or by refreshing the counter in register start mode.	• Reset (The down-counter and other registers return to their initial values.) • Low power consumption modes • A counter underflows or a refresh error occurs (only in register start mode).
Window function	Window start and end positions can be specified. (refresh-permitted and refresh-prohibited periods)	Window start and end positions can be specified. (refresh-permitted and refresh-prohibited periods)
Watchdog timer reset output sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt/interrupt sources	• A non-maskable interrupt (WUNI) occurs when a down-counter underflow occurs. • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	• The down-counter value can be read by reading the WDTSR register.	• The down-counter value can be read by reading the WDTSR register.

Table 2.62 Comparison of Watchdog Timer Registers

Register	Bit	RX630 (WDTA)	RX660 (WDTA)
WDTRCR	RSTIRQS	Reset interrupt request select bit 0: Enables non-maskable interrupt request output 1: Enables reset output	Reset interrupt request select bit 0: Enables non-maskable interrupt request or interrupt request output 1: Enables reset output

2.23 Independent Watchdog Timer

Table 2.63 is a Comparative Overview of Independent Watchdog Timers, and Table 2.64 is a Comparison of Independent Watchdog Timer Registers.

Table 2.63 Comparative Overview of Independent Watchdog Timers

Item	RX630 (IWDTa)	RX660 (IWDTa)
Count source	IWDT-dedicated clock (IWDTCLK)	IWDT-dedicated clock (IWDTCLK)
Clock division ratio	Divided by 1, 16, 32, 64, 128, or 256	Divided by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down by a 14-bit down-counter	Counting down by a 14-bit down-counter
Count start conditions	• Counting automatically starts after a reset. (auto-start mode) • Counting is started by refreshing the counter (writing 00h and then FFh to the IWDTRR register). (register start mode)	• Auto-start mode: Counting automatically starts after a reset. • Register start mode: Counting is started by the refresh operation (writing 00h and then FFh to the IWDTRR register).
Count stop conditions	• Reset (The down-counter and other registers return to their initial values.) • A counter underflows or a refresh error occurs. Counting restarts automatically in auto-start mode, or by refreshing the counter in register start mode.	• Reset (The down-counter and other registers return to their initial values.) • Low power consumption mode (depending on the register setting) • A counter underflows or a refresh error occurs (only in register start mode).
Window function	Window start and end positions can be specified. (refresh-permitted and refresh-prohibited periods)	Window start and end positions can be specified. (refresh-permitted and refresh-prohibited periods)
Reset output sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt/interrupt sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	• The down-counter value can be read by reading the IWDTSR register.	• The down-counter value can be read by reading the IWDTSR register.
Event link function (output)	—	• Down-counter underflow event output • Refresh error event output
Output signals (internal signals)	• Reset output • Interrupt request output • Sleep mode count stop control output	• Reset output • Interrupt request output • Sleep mode count stop control output

Item	RX630 (IWDTa)	RX660 (IWDTa)
Auto-start mode (controlled by option function select register 0 (OFS0))	• Selecting the clock division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position of the watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position of the watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)	• Selecting the clock division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position of the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position of the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)
Register start mode (controlled by the IWDT register)	• Selecting the clock frequency division ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position of the watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position of the watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)	• Selecting the clock frequency division ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position of the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position of the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)

Table 2.64 Comparison of Independent Watchdog Timer Registers

Register	Bit	RX630 (IWDTa)	RX660 (IWDTa)
IWDTRCR	RSTIRQS	Reset interrupt request select bit 0: Enables non-maskable interrupt request output 1: Enables reset output	Reset interrupt request select bit 0: Enables non-maskable interrupt request or interrupt request output 1: Enables reset output

2.24 Serial Communications Interface

Table 2.65 is a Comparative Overview of Serial Communications Interfaces, Table 2.66 is a Comparison of Serial Communications Interface Channel Specifications, and Table 2.67 is a Comparison of Serial Communications Interface Registers.

Table 2.65 Comparative Overview of Serial Communications Interfaces

Item		RX630 (SCIc, SCId)	RX660 (SCIk, SCIm, SCIh)
Number of channels		• SCIc: 12 channels • SCId: 1 channel	• SCIk: 10 channels • SCIm: 2 channels • SCIh: 1 channel
Serial communications modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I^2C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I^2C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator	Bit rate specifiable by on-chip baud rate generator
Full-duplex communication		• Transmitter: Continuous transmission possible using double-buffer structure • Receiver: Continuous reception possible using double-buffer structure	• Transmitter: Continuous transmission possible using double-buffer structure • Receiver: Continuous reception possible using double-buffer structure
Data transfer		Selectable as LSB first or MSB first transfer	Selectable as LSB first or MSB first transfer
I/O signal level inversion		—	The levels of input and output signals can be inverted independently.
Interrupt sources		• Transmit end, transmit data empty, receive data full, and receive error • Completion of generation of a start condition, restart condition, or stop condition (for simple I^2C mode)	• Transmit end, transmit data empty, receive data full, receive error, receive data ready (SCI10, SCI11) and data match • Completion of generation of a start condition, restart condition, or stop condition (for simple I^2C mode)
Low power consumption function		Individual channels can be transitioned to the module stop state.	Individual channels can be transitioned to the module stop state.
Asynchronous mode	Data length	7 or 8 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection function	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	CTSn and RTSn pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Transmit/receive FIFO	—	Ability to use 16-stage FIFOs for transmission and reception (SCI10 and SCI11)
	Data match detection	—	Compares receive data and the comparison data register, and generates interrupt when they match.
	Start-bit detection	—	Low level or falling edge is selectable.

Item		RX630 (SCIc, SCId)	RX660 (SCIk, SCIm, SCIh)
Asynchronous mode	Receive data sampling timing adjustment	—	The receive data sampling point can be shifted from the center of the data forward or backward to a base point (SCI0 and SCI11).
	Transmit signal change timing adjustment	—	Either the falling or rising edge of the transmit data can be delayed (SCI0 and SCI11).
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly or by reading the SPTR.RXDMON flag.
	Clock source	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5 and SCI6).	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5, SCI6, and SCI12).
	Double-speed mode	—	Baud rate generator double-speed mode is selectable.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Transmit/receive FIFO	—	Ability to use 16-stage FIFOs for transmission and reception (SCI10 and SCI11)
Smart card interface mode	Error processing	• An error signal can be automatically transmitted when detecting a parity error during reception. • Data can be automatically retransmitted when receiving an error signal during transmission.	• An error signal can be automatically transmitted when detecting a parity error during reception. • Data can be automatically retransmitted when receiving an error signal during transmission.
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	I^2C bus format	I^2C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer speed	Maximum of 384 kbps. Fast-mode is supported.	Fast mode is supported.
	Noise cancellation	• The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters. • The interval for noise cancellation is adjustable.	• The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters. • The interval for noise cancellation is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.

Item		RX630 (SCIc, SCId)	RX660 (SCIk, SCIm, SCIh)
Extended serial mode (supported by SCI12 only)	Start frame transmission	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection
	Start frame reception	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two kinds of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two kinds of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates
	I/O control function	• Ability to select polarity or TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select receive data sampling timing of RXDX12 pin • Signals received on RXDX12 can be passed through to SCIc when the expanded serial mode control section is off.	• Ability to select polarity or TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select receive data sampling timing of RXDX12 pin
	Timer function	Usable as reloading timer	Usable as reloading timer
Bit rate modulation function		—	Correction of outputs from the on-chip baud rate generator can reduce errors.
Event link function (supported by SCI5 only)		—	• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output

Table 2.66 Comparison of Serial Communications Interface Channel Specifications

Item	RX630 (SCIc, SCId)	RX660 (SCIk, SCIm, SCIh)
Asynchronous mode	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12
Clock synchronous mode	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12
Smart card interface mode	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12
Simple I^2C mode	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12
Simple SPI mode	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12
FIFO mode	—	SCI10, SCI11
Data match detection	—	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11
Extended serial mode	SCI12	SCI12
TMR clock input	SCI5, SCI6, SCI12	SCI5, SCI6, SCI12
Event link function	—	SCI5
Peripheral module clock	PCLKB: SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12	PCLKA: SCI10, SCI11 PCLKB: SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI12

Table 2.67 Comparison of Serial Communications Interface Registers

Register	Bit	RX630 (SCIc, SCId)	RX660 (SCIk, SCIm, SCIh)
RDRH, RDRL, RDRHL	—	—	Receive data registers H, L, and HL
FRDR	—	—	Receive FIFO data register
TDRH, TDRL, TDRHL	—	—	Transmit data registers H, L, and HL
FTDR	—	—	Transmission FIFO data register
SMR (SCMR.SMIF bit = 0)	CHR	Character length bit (Valid only in asynchronous mode) 0: Data length of 8 bits is used for transmission and reception. 1: Data length of 7 bits is used for transmission and reception.	Character length bit (Valid only in asynchronous mode) Selectable in combination with the SCMR.CHR1 bit CHR1 CHR 0 0: Transmit/receive in 9-bit data length 0 1: Transmit/receive in 9-bit data length 1 0: Transmit/receive in 8-bit data length (initial value) 1 1: Transmit/receive in 7-bit data length
	CM	Communication mode bit 0: Operation is performed in asynchronous mode. 1: Operation is performed in clock synchronous mode.	Communication mode bit 0: Operation is performed in asynchronous mode or simple I^2C mode. 1: Operation is performed in clock synchronous mode or simple I^2C mode.

Register	Bit	RX630 (SCIc, SCId)	RX660 (SCIk, SCIm, SCIh)
SCR (SCMR.SMIF bit = 0)	MPIE	Multi-processor interrupt enable bit (Valid when the SMR.MP bit = 1 in asynchronous mode) 0: Normal receive operation 1: When the data with the multi-processor bit set to 0 is received, the data is not read, and setting the status flags ORER and FER in SSR to 1 is disabled. When the data with the multiprocessor bit set to 1 is received, the MPIE bit is automatically cleared to 0, and normal reception is resumed.	Multi-processor interrupt enable bit (Valid when the SMR.MP bit = 1 in asynchronous mode) 0: Normal receive operation 1: When the data with the multi-processor bit set to 0 is received, the data is not read, and setting the status flags RDRF, ORER, and FER in SSR to 1 is disabled. When data with the multi-processor bit set to 1 is received, the MPIE bit is automatically set to 0 to resume the normal receive operation.
SSRFIFO	—	—	Serial status register
SCMR	CHR1	—	Character length bit 1
MDDR	—	—	Modulation duty register
SEMR	ITE	—	Immediate transmission enable bit
	BRME	—	Bit rate modulation enable bit
SEMR	ABCSE	—	Asynchronous mode base clock select extended bit
	BGDM	—	Baud rate generator double-speed mode select bit
	RXDESEL	—	Asynchronous start bit edge detection select bit
FCR	—	—	FIFO control register
FDR	—	—	FIFO data count register
LSR	—	—	Line status register
CDR	—	—	Comparison data register
DCCR	—	—	Data comparison control register
SPTR	—	—	Serial port register
TMGR	—	—	Transmit/receive timing select register
CR2	BCCS[1:0]	Bus collision detection clock select bit b5 b4 0 0: SCI base clock 0 1: 1/2 SCI base clock frequency 1 0: 1/4 SCI base clock frequency 1 1: Setting prohibited.	Bus collision detection clock select bit • When the SEMR.BGDM bit is 0, or when the SEMR.BGDM bit is 1 and the SMR.CKS[1:0] bits are not 00b. b5 b4 0 0: Base clock 0 1: Base clock frequency divided by 2 1 0: Base clock frequency divided by 4 1 1: Setting prohibited. • When the SEMR.BGDM bit is 1 and the SMR.CKS[1:0] bits are 00b. b5 b4 0 0: Base clock frequency divided by 2 0 1: Base clock frequency divided by 4 1 0: Setting prohibited. 1 1: Setting prohibited.

2.25 I²C Bus Interface

Table 2.69 is a Comparison of I2C Bus Interface Registers.

Table 2.68 Comparison of Serial Communications Interface Registers

Item	RX630 (RIIC)	RX660 (RIICa)
Communication format	• I²C bus format or SMBus format • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate	• I²C bus format or SMBus format • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate
Transfer speed	Up to 1 Mbps	Fast-mode is supported (up to 400 kbps).
SCL clock	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%.	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%.
Issuing and detecting conditions	• Start, restart, and stop conditions are automatically generated. • Start conditions (including restart conditions) and stop conditions are detectable.	• Start, restart, and stop conditions are automatically generated. • Start conditions (including restart conditions) and stop conditions are detectable.
Slave address	• Configurable for three sets of slave addresses • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.	• Configurable for up to three different slave addresses • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.
Acknowledgment	• For transmission, the acknowledge bit is automatically loaded. — Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. — If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.	• For transmission, the acknowledge bit is automatically loaded. — Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. — If a wait between the eighth and ninth clock cycles has been selected, software control of the acknowledge response according to the received data value is possible.
Wait function	• In reception, the following periods of waiting can be obtained by holding the SCL clock at the low level: — Waiting between the eighth and ninth clock cycles — Waiting between the ninth clock cycle and the first clock cycle of the next transfer (WAIT function)	• In reception, the following periods of waiting can be obtained by holding the SCL line at the low level: — Waiting between the eighth and ninth clock cycles — Waiting between the ninth clock cycle and the first clock cycle of the next transfer

Item	RX630 (RIIC)	RX660 (RIICa)
SDA output delay function	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.	Change timing of the output of transmitted data, including the acknowledge bit, can be delayed.
Arbitration	• For multi-master operation — Operation to synchronize the SCL clock in cases of conflict with the SCL signal from another master is possible. — When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration is detectable when start condition is issued while the bus is busy (to prevent the issuing of double start conditions). • When transmitting a not-acknowledge bit, loss of arbitration is detectable by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. • In slave transmission, loss of arbitration is detectable if data mismatch.	• For multi-master operation — Operation to synchronize the SCL in cases of conflict with the SCL signal from another master is possible. — When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration is detectable when start condition is issued while the bus is busy (to prevent the issuing of double start conditions). • When transmitting a not-acknowledge bit, loss of arbitration is detectable by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. • In slave transmission, loss of arbitration is detectable if data mismatch.
Timeout function	The internal timeout function is capable of detecting long-interval stop of the SCL clock.	The internal timeout function is capable of detecting long-interval stop of the SCL.
Noise cancellation	The interface incorporates digital noise filters for both the SCL and SDA inputs, and programmable adjustment of the interval for noise cancellation is possible.	The interface incorporates digital noise filters for both the SCL and SDA inputs, and the interval for noise cancellation is adjustable by software.

Item	RX630 (RIIC)	RX660 (RIICa)
Interrupt sources	4 sources • Transfer error or event occurrence — AL detection — NACK detection — Timeout detection — Detection of a start condition (including restart conditions) — Stop condition detection) • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmission complete	4 sources • Error in transfer or occurrence of events — Arbitration lost detection — NACK detection — Timeout detection — Detection of a start condition (including restart conditions) — Stop condition detection • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmission complete
Low Power Consumption	Ability to specify module stop state	Ability to transition to module stop state

Table 2.69 Comparison of I²C Bus Interface Registers

Register	Bit	RX630 (RIIC)	RX660 (RIICa)
ICMR2	TMWE	Timeout internal counter write enable bit	—
ICFER	FMPE	Fast mode plus enable bit	—
ICIER	RIE	Receive data full interrupt enable bit 0: Receive data full interrupts (ICRXI) disabled 1: Receive data full interrupts (ICRXI) enabled	Receive data full interrupt enable bit 0: Receive data full interrupt requests (RXI) disabled 1: Receive data full interrupt requests (RXI) enabled
	TEIE	Transmission complete interrupt enable bit 0: Transmission complete interrupts (ICTEI) disabled 1: Transmission complete interrupts (ICTEI) enabled	Transmission complete interrupt enable bit 0: Transmission complete interrupt requests (TEI) disabled 1: Transmission complete interrupt requests (TEI) enabled
	TIE	Transmit data empty interrupt enable bit 0: Transmit data empty interrupts (ICTXI) disabled 1: Transmit data empty interrupts (ICTXI) enabled	Transmit data empty interrupt enable bit 0: Transmit data empty interrupt requests (TXI) disabled 1: Transmit data empty interrupt requests (TXI) enabled
TMOCNT	—	Timeout internal counter	—

2.26 CAN Module and CANFD Module

Table 2.70 is a Comparative Overview of CAN Module and CANFD Module, and Table 2.71 is a Comparison of CAN Module and CANFD Module Registers.

Table 2.70 Comparative Overview of CAN Module and CANFD Module

Item	RX630 (CAN)	RX660 (CANFD-Lite)
Protocol	Conforming to the ISO 11898-1 standard (standard frame or extension frame)	Conforming to the ISO 11898-1:2015 specifications
Bit rate (RX630) Data transfer rate (RX660)	Programming is possible with a maximum bit rate of 1 Mbps (fCAN is equal to or larger than 8 MHz). — fCAN: CAN clock source	• Arbitration phase: Maximum of 1 Mbps • Data phase: Maximum 8 Mbps*1
Operating frequency	PCLKB: 60MHz (max) CANFDMCLK: 24 MHz (max)	Register block: Maximum of 60 MHz (PCLKB) • Message buffer RAM: Maximum of 120 MHz (PCLKA)
Operating clock for data link layer (DLL clock)	—	Maximum of 60 MHz (either CANFDMCLK or CANFDCLK can be selected)
Message box (RX630) Message buffer (RX660)	32 mailboxes: Two mail box modes can be selected. • Normal mailbox mode: 32 mailboxes can be configured for transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for transmission or reception. The remaining mailboxes can be configured as a 4-stage transmit FIFO and a 4-stage receive FIFO.	• 32 receive message buffers • Four transmit message buffers • One transmit queue Automatic transfer of messages to the transmit queue is supported.
Frame type	• Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID) • Remote frame in base format (11-bit ID) • Remote frame in extended format (29-bit ID)	Classic CAN (CAN 2.0) • Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID) • Remote frame in base format (11-bit ID) • Remote frame in extended format (29-bit ID) CAN FD*1 • Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID)

Item	RX630 (CAN)	RX660 (CANFD-Lite)
Reception	• Data frames and remote frames can be received. • The ID format to be received (base ID only, extended ID only, or both base ID and extended ID) can be selected. • The one-shot receive function can be selected. • Overwrite mode (message is overwritten) or overrun mode (message is discarded) can be selected. • Reception end interrupt can be enabled or disabled individually for each mailbox.	• Data frames and remote frames can be received. • The ID format to be received (base ID only, extended ID only, or both base ID and extended ID) can be selected. • Receive message buffer interrupt can be enabled or disabled individually for each message buffer.
Data length	0 to 8 bytes	Classic CAN: 0 to 8 bytes CAN FD: 0 to 8, 12, 16, 20, 24, 32, 48, or 64 bytes*1
Acceptance filter	• Eight acceptance masks (an individual mask for every four mailboxes) • Mailbox masks can be enabled or disabled individually.	Filtering is possible in the following fields: • IDE bit (base format, extended format, or both) • ID field • RTR bit (data frame or remote frame) (only for Classic CAN) • DLC field Data (data length) • The protection function when the payload size is exceeded is provided. • Acceptance filter list (AFL) entries can be updated during communication.
Transmission	• Data frames and remote frames can be sent. • The ID format to be sent (base ID only, extended ID only, or both base ID and extended ID) can be selected. • The one-shot transmission function can be selected. • Either ID priority transmission mode or mailbox number priority transmission mode can be selected. • Transmission requests can be aborted (completion of abort can be confirmed with a flag). • Transmission end interrupt can be enabled or disabled individually for each mailbox.	• Data frames and remote frames can be sent. • The ID format to be sent (base ID only or extended ID only) can be selected. • The one-shot transmission function can be selected. • Either ID priority transmission mode or message buffer number priority transmission mode can be selected. • Transmission requests can be aborted (completion of abort can be confirmed with a flag). • Channel transmission interrupt can be enabled and disabled.

Item	RX630 (CAN)	RX660 (CANFD-Lite)
FIFO	• 24 mailboxes can be configured for transmission or reception. • The remaining mailboxes can be configured as a 4-stage transmit FIFO and a 4-stage receive FIFO.	The FIFO size is programmable. • Two receive FIFOs • One common FIFO (Whether to use the FIFO as a receive FIFO or transmit FIFO can be selected.)
Automatic transmission interval adjustment	—	• Available when the common FIFO is configured as a transmit FIFO • The interval between messages sent from the FIFO can be adjusted.
Bus-off recovery method	How to recover from the bus-off state can be selected. • Conforming to the ISO 11898-1 standard • The mode automatically changes to CAN Halt mode when bus off starts. • The mode automatically changes to CAN Halt mode when bus off ends. • A program causes a transition to CAN Halt mode. • A program causes a transition to error active state.	How to recover from the bus-off state can be selected. • Normal mode (ISO 11898-1 compliant) • Automatically enters CH_HALT mode when bus off starts. • Automatically enters CAN Halt mode when bus off ends • Software causes a transition CH_HALT mode (during bus-off recovery period). • A program causes a transition to error active state.
Timestamp function	• Timestamp function with a 16-bit counter • The reference clock can be selected from 1, 2, 4, and 8 bit time.	Transmission and reception timestamp function
Interrupt function	• Five types of interrupt sources (reception end interrupt, transmission end interrupt, receive FIFO interrupt, transmit FIFO interrupt, and error interrupt)	Receive FIFO interrupt Global error interrupt Channel transmission interrupt Channel error interrupt Common FIFO reception interrupt Receive message buffer interrupt
CAN sleep mode	Current consumption can be reduced by stopping the CAN clock.	Module start/stop function for each CAN node (CH_SLEEP mode and GL_SLEEP mode)
Software support	—	Label information is automatically added to received messages.
Software support units	Three software support unis • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support	—

Item	RX630 (CAN)	RX660 (CANFD-Lite)
Test modes	Three test modes are provided for user evaluation: • Listen-only mode • Self test mode 0 (external loopback) • Self test mode 1 (internal loopback)	• Basic test mode • Listen-only mode • Self test mode 0 (external loopback) • Self test mode 1 (internal loopback)
Low power consumption function (RX630) Power down function (RX660)	Ability to specify module stop state	Module start/stop function for each CAN node (CH_SLEEP mode and GL_SLEEP mode) Ability to transition to module stop state
RAM	—	RAM with ECC protection

Note: 1. This is only available for products that support the CAN FD protocol.

Table 2.71 Comparison of CAN Module and CANFD Module Registers

Register	Bit	RX630 (CAN)	RX660 (CANFD-Lite)
CTLR	—	Control register	—
BCR	—	Bit configuration register	—
MKRk	—	Mask register k (k = 0 to 7)	—
FIDCR0 FIDCR1	—	FIFO receive ID comparison register	—
MKIVLR	—	Mask disable register	—
MBj	—	Mailbox register j (j = 0 to 31)	—
MIER	—	Mailbox interrupt enable register	—
MCTLj	—	Message control register j (j = 0 to 3)	—
RFCR	—	Receive FIFO control register	—
RFPCR	—	Receive FIFO pointer control register	—
TFCR	—	Transmit FIFO control register	—
TFPCR	—	Transmit FIFO pointer control register	—
STR	—	Status register	—
MSMR	—	Mailbox search mode register	—
MSSR	—	Mailbox search status register	—
CSSR	—	Channel search support register	—
AFSR	—	Acceptance filter support register	—
EIER	—	Error interrupt enable register	—
EIFR	—	Error interrupt source decision register	—
RECR	—	Receive error count register	—
TECR	—	Transmit error count register	—
ECSR	—	Error code storage register	—
TSR	—	Timestamp register	—
TCR	—	Test control register	—
NBCR	—	—	Nominal bit rate configuration register
CHCR	—	—	Channel control register
CHSR	—	—	Channel status register
CHESR	—	—	Channel error status register
DBCR	—	—	Data bit rate configuration register
FDCFG	—	—	CAN FD configuration register
FDCTR	—	—	CAN FD control register
FDSTS	—	—	CAN FD status register
FDCRC	—	—	CAN FD CRC register
GCFG	—	—	Global configuration register
GCR	—	—	Global control register
GSR	—	—	Global status register
GESR	—	—	Global error status register
TISR	—	—	Transmit interrupt status register
TSCR	—	—	Timestamp counter register
AFCR	—	—	Acceptance filter list control register
AFCFG	—	—	Acceptance filter list configuration register
AFLn.IDR	—	—	Acceptance filter list n ID register (n = 0 to 15)
AFLn.MASK	—	—	Acceptance filter list n (n = 0 to 15)
AFLn.PTR0	—	—	Acceptance filter list n pointer register 0 (n = 0 to 15)
AFLn.PTR1	—	—	Acceptance filter list n pointer register 1 (n = 0 to 15)

Register	Bit	RX630 (CAN)	RX660 (CANFD-Lite)
RMCR	—	—	Receive message buffer configuration register
RMNDR	—	—	Receive message buffer new data register
RFCRn	—	—	Receive FIFO n configuration register (n = 0 or 1)
RFSRn	—	—	Receive FIFO n status register (n = 0 or 1)
RFPCRn	—	—	Receive FIFO n pointer control register (n = 0 or 1)
CFCR0	—	—	Common FIFO 0 configuration register
CFSR0	—	—	Common FIFO 0 status register
CFPCR0	—	—	Common FIFO 0 pointer control register
FESR	—	—	FIFO empty status register
FFSR	—	—	FIFO full status register
FMLSR	—	—	FIFO message lost status register
RFISR	—	—	Receive FIFO interrupt status register
DTCR	—	—	DMA transfer control register
DTSR	—	—	DMA transfer status register
TMCRn	—	—	Transmit message buffer n control register (n = 0 to 3)
TMSRn	—	—	Transmit message buffer n status register (n = 0 to 3)
TMTRSR0	—	—	Transmit message buffer transmission request status register 0
TMARSR0	—	—	Transmit message buffer transmission abort request status register 0
TMTCSR0	—	—	Transmit message buffer transmission completion status register 0
TMTASR0	—	—	Transmit message buffer transmission abort status register 0
TMIER0	—	—	transmission message buffer interrupt enable register 0
TQCR0	—	—	Transmit queue 0 configuration register
TQSR0	—	—	Transmit queue 0 status register
TQPCR0	—	—	Transmit queue 0 pointer control register
THCR	—	—	Transmission history configuration register
THSR	—	—	Transmission history status register
THACR0	—	—	Transmission history access register 0
THACR1	—	—	Transmission history access register 1
THPCR	—	—	Transmission history pointer control register
GRCR	—	—	Global reset control register
GTMCR	—	—	Global test mode configuration register
GTMER	—	—	Global test mode enable register
GTMLKR	—	—	Global test mode lock key register
RTPARk	—	—	RAM test page access register k (k = 0 to 63)
AFIGSR	—	—	Acceptance filter list ignore entry setting register
AFIGER	—	—	Acceptance filter list ignore entry enable register
RMIER	—	—	Receive message buffer interrupt enable register
ECCSR	—	—	ECC control/status register
ECTMR	—	—	ECC test mode register

Register	Bit	RX630 (CAN)	RX660 (CANFD-Lite)
ECTDR	—	—	ECC decoder test data register
ECEAR	—	—	ECC error address register

2.27 Serial Peripheral Interface

Table 2.72 is a Comparative Overview of Serial Peripheral Interfaces, and Table 2.73 is a Comparison of Serial Peripheral Interface Registers.

Table 2.72 Comparative Overview of Serial Peripheral Interfaces

Item	RX630 (RSPI)	RX660 (RSPId)
Number of channels	3 channels	1 channel
RSPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is possible. • Serial communication is possible in master and slave modes. • Switching of the polarity of the serial transfer clock • Switching of the phase of the serial transfer clock	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Full-duplex or simplex (transmit-only or reception-only (in slave mode)) can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK
Data format	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits).	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits). • Byte swapping of transmit and receive data is possible. • Ability to invert the logic level of transmit/receive data
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, external input clock is used as a serial clock (the maximum frequency is the PCLK frequency divided by 8). — Width at high level: 4 cycles of PCLK — Width at low level: 4 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4). — Width at high level: 2 cycles of PCLK — Width at low level: 2 cycles of PCLK
Buffer configuration	Double buffer configuration for the transmit/receive buffers	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers

Item	RX630 (RSPI)	RX660 (RSPId)
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection
SSL control function	• Four SSL pins for each channel (SSLn0 to SSLn3) • In single-master mode, SSLn0 to SSLn3 pins are output. • In multi-master mode: SSLn0 pin for input, and SSLn1 to SSLn3 pins for either output or unused • In slave mode: SSLn0 pin for input, and SSLn1 to SSLn3 pins for unused • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity	• Four SSL pins for each channel (SSLA0 to SSLA3) • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for unused • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity
Control in master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • The following items can be specified for each command: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation	• A transfer of up to eight commands can be executed sequentially in looped execution. • The following items can be specified for each command: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function • The delay between data bytes can be shortened during burst transfers.

Item	RX630 (RSPI)	RX660 (RSPId)
Interrupt sources	• Maskable interrupt sources — RSPI reception interrupt (receive buffer full) — RSPI transmission interrupt (transmit buffer empty) — RSPI error interrupt (mode fault, overrun, or parity error) — RSPI idle interrupt (RSPI idle)	• Interrupt sources — Receive buffer full interrupt — Transmit buffer empty interrupt — Error interrupt (mode fault, overrun, underrun, or parity error) — Idle interrupt — Communication end interrupt
Event link function (output)	—	• Interrupt sources — Receive buffer full events — Transmit buffer empty events — Error event (mode fault, overrun, underrun, or parity error) — Idle events — Communication completion events
Other functions	• Function for initializing the RSPI • Loopback mode	• Function for initializing the RSPI • Loopback mode
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.73 Comparison of Serial Peripheral Interface Registers

Register	Bit	RX630 (RSPI)	RX660 (RSPId)
SPSR	UDRF	—	Underrun error flag
	SPCF	—	Communication completion flag
SPDCR	SPBYT	—	RSPI byte access setting bit
SPCR2	SCKASE	—	RSPCK auto-stop function enable bit*1
SPDCR2	—	—	RSPI data control register 2
SPCR3	—	—	RSPI control register 3

Note: 1. Do not change the settings of the SPPE, SPOE, and SCKASE bits when the SPCR.SPE bit is set to 1.

2.28 CRC Calculator

Table 2.74 is a Comparative Overview of CRC Calculators, and Table 2.75 is a Comparison of CRC Calculator Registers.

Table 2.74 Comparative Overview of CRC Calculators

Item	RX630 (CRC)	RX660 (CRCA)	
Data size	8 bits	8 bits	32 bits
Data for CRC calculation	CRC code generated for any desired data in 8n-bit units (where n is a whole number)	CRC code generated for any desired data in 8n-bit units (where n is a whole number)	CRC code generated for any desired data in 32n-bit units (where n is a whole number)
CRC processor unit	8-bit parallel processing	8-bit parallel processing	32-bit parallel processing
CRC generating polynomial	One of three generating polynomials is selectable. • 8-bit CRC — $X^8 + X^2 + X + 1$ • 16-bit CRC — $X^{16} + X^{15} + X^2 + 1$ — $X^{16} + X^{12} + X^5 + 1$	One of three generating polynomials is selectable. • 8-bit CRC — $X^8 + X^2 + X + 1$ • 16-bit CRC — $X^{16} + X^{15} + X^2 + 1$ — $X^{16} + X^{12} + X^5 + 1$	One of two generating polynomials is selectable. • 32-bit CRC — $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ — $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$
CRC calculation switching	Selectable from CRC code generation for LSB first and MSB first communication	The order of the bits produced by CRC calculation can be switched for LSB first or MSB first communication.	
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state	

Table 2.75 Comparison of CRC Calculator Registers

Register	Bit	RX630 (CRC)	RX660 (CRCA)
CRCCR	GPS[1:0]: (RX630) GPS[2:0]: (RX660)	CRC generating polynomial switching bits b1 b0 0 0: No calculation is executed. 0 1: $X^8 + X^2 + X + 1$ 1 0: $X^{16} + X^{15} + X^2 + 1$ 1 1: $X^{16} + X^{12} + X^5 + 1$	CRC generating polynomial switching bits b2 b0 0 0 0: No calculation is executed. 0 0 1: 8-bit CRC ($X^8 + X^2 + X + 1$) 0 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$) 0 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$) 1 0 0: 32-bit CRC ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1: 32-bit CRC ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) 1 1 0: No calculation is executed. 1 1 1: No calculation is executed.
	LMS	CRC calculation switching bit (b2)	CRC calculation switching bit (b6)
CRCDIR	—	CRC data input register Supported access size • Byte access	CRC data input register Supported access size • Longword access (when generating 32-bit CRC) • Byte access (when generating 16-bit or 8-bit CRC)
CRCDOR	—	CRC data output register Supported access size • Word access The lower byte (b7 to b0) is used when generating an 8-bit CRC.	CRC data output register Supported access size • Longword access (when generating 32-bit CRC) • Word access (when generating 16-bit CRC) • Byte access (when generating 8-bit CRC)

2.29 12-Bit A/D Converter

Table 2.76 is a Comparative Overview of 12-Bit A/D Converters, and Table 2.77 is a Comparison of 12-Bit A/D Converter Registers.

Table 2.76 Comparative Overview of 12-Bit A/D Converters

Item	RX630 (S12ADa)	RX660 (S12ADH)
Number of units	One unit	One unit (S12AD)
Input channels	Up to 21 channels	24 channels
Extended analog function	Temperature sensor output, internal reference voltage	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	1.0 µs per channel (when A/D conversion clock (ADCLK) = 50 MHz)	0.9 µs per channel (when A/D conversion clock (ADCLK) = 60 MHz)
A/D conversion clock	Four types: PCLK, PCLK/2, PCLK/4, and PCLK/8	Peripheral module clock PCLKB and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. — PCLKB to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1 ADCLK is set using the clock generation circuit. The A/D conversion clock (ADCLK) can operate at frequencies from a maximum of 60 MHz to a minimum of 8 MHz.

Item	RX630 (S12ADa)	RX660 (S12ADH)
Data registers	• 21 registers for analog input • One register for temperature sensor • One register for internal reference voltage • The results of A/D conversion are stored in 12-bit A/D data registers. • In A/D-converted value addition mode, the results of A/D conversion are stored in 14-bit A/D data registers.	• 24 registers for analog input • One register for duplication of A/D conversion in double trigger mode • Two registers for expanded operation in double trigger mode • One register for temperature sensor output • One register for internal reference • One register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable from single scan and group scan modes) — The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers) — A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.

Item	RX630 (S12ADa)	RX660 (S12ADH)
Operating mode	• Single scan mode: — A/D conversion is performed only once on arbitrarily selected analog inputs of up to 21 channels. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: — A/D conversion is performed repeatedly on arbitrarily selected analog inputs of up to 21 channels.	• Single scan mode: — A/D conversion is performed only once on arbitrarily selected analog inputs. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: — A/D conversion is performed repeatedly on arbitrarily selected analog inputs. • Group scan mode: — Two (groups A and B) or three (groups A, B, and C) can be selected as the number of groups to be used. (Only the combination of groups A and B can be selected when the number of groups is two.) Arbitrarily selected analog input channels, the temperature sensor output, and the internal reference voltage are divided into two groups (group A and B) or three groups (group A, B, and C), and A/D conversion of the analog input selected on a group basis is performed only once. — The scanning start condition for groups A, B, and C (synchronous trigger) can be independently selected, allowing A/D conversion of each group to be started independently. • Group scan mode: (Group priority control selected) If a higher-priority group trigger is input during scanning of a lower-priority group, scanning of the lower-priority group stops and scanning of the higher-priority group starts. The priority order is group A (highest) > group B > group C (lowest). Whether or not to restart scanning (rescan) of the lower-priority group after processing for the higher-priority group completes, is selectable. Rescan can also be set to start either from the first selected channel or from the channel on which A/D conversion did not complete.

Item	RX630 (S12ADa)	RX660 (S12ADH)
Conditions for A/D conversion start	• Software trigger • Synchronous trigger Trigger from the MTU, TPU, or TMR • Asynchronous trigger A/D conversion can be triggered by the ADTRG0# pin.	• Software trigger • Synchronous trigger Trigger by the multi-function timer pulse unit (MTU), 8-bit timer (TMR), or event link controller (ELC) • Asynchronous trigger A/D conversion can be triggered by the external trigger ADTRG0# pin.
Functions	• Sample-and-hold function • Variable sampling state count • A/D-converted value addition mode	• Variable sampling time (settable on a per-channel basis) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function for A/D data registers • Compare function (window A and window B) • Ability to specify the channel conversion priority

Item	RX630 (S12ADa)	RX660 (S12ADH)
Interrupt sources	• A scan end interrupt request (S12ADI0) is generated on completion of A/D conversion. • The S12ADI0 interrupt can activate the DMAC and DTC.	• In the modes except double trigger mode and group scan mode, a scan end interrupt request (S12ADI) is generated on completion of single scan. • In double trigger mode, a scan end interrupt request (S12ADI) is generated on completion of double scan. • In group scan mode, an A/D scan end interrupt request (S12ADI) can be generated on completion of group A scan, A scan end interrupt request (S12GBADI) dedicated to group B is generated on completion of group B scan, and an A/D scan end interrupt request (S12GCADI) for group C can be generated on completion of group C scan. • When double trigger mode is selected in group scan mode, a scan end interrupt request (S12ADI) is generated on completion of double scan of group A. A corresponding scan end interrupt request (S12GBADI or S12GCADI) can be generated on completion of a group B or group C scan. • A compare interrupt request (S12CMPAI or S12CMPBI) can be generated upon a match with the comparison condition for the digital compare function. • The S12ADI, S12GBADI, and S12GCADI interrupts can activate the DMA controller (DMAC) or data transfer controller (DTC).
Event link function	—	• An event can be output upon completion of all scans. • Scan can be started by a trigger output by the ELC. • In single scan mode, an event can be output when the compare function window condition is met.
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Note: 1. The number of extended bits during addition differs depending on the addition count.
2-bit extension: 1-time to 4-time conversion (no addition or 1-time to 3-time addition)
4-bit extension: 16 conversions (15-time addition)

Table 2.77 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX630 (S12ADa)	RX660 (S12ADH)
ADCSR	DBLANS[4:0]	—	Double trigger target channel select bits
	GBADIE	—	Group B scan end interrupt enable bit
	DBLE	—	Double trigger mode select bit
	CKS[1:0]	A/D conversion clock select bits	—
	ADCS (RX630) ADCS[1:0] (RX660)	Scan mode select bit 0: Single scan mode 1: Continuous scan mode	Scan mode select bits b14 b13 0 0: Single scan mode 0 1: Group scan mode 1 0: Continuous scan mode 1 1: Settings prohibited.
ADANS0	—	A/D channel select register 0	—
ADANS1	—	A/D channel select register 1	—
ADANSA0	—	—	A/D channel select register A0
ADANSA1	—	—	A/D channel select register A1
ADANSB0	—	—	A/D channel select register B0
ADANSB1	—	—	A/D channel select register B1
ADANSC0	—	—	A/D channel select register C0
ADANSC1	—	—	A/D channel select register C1
ADSCSn	—	—	A/D channel conversion order setting register n (n = 0 to 23)
ADADC	ADC[1:0] (RX630) ADC[2:0] (RX660)	Addition count select bits b1 b0 0 0: 1-time conversion (no addition, same as normal conversion) 0 1: 2-time conversion (addition once) 1 0: 3-time conversion (addition twice) 1 1: 4-time conversion (addition three times)	Addition count select bits b2 b0 0 0 0: 1-time conversion (no addition, same as normal conversion) 0 0 1: 2-time conversion (addition once) 0 1 0: 3-time conversion (addition twice)*1 0 1 1: 4-time conversion (addition three times) 1 0 1: 16-time conversion (addition 15 times)*1 Settings other than the above are prohibited.
	AVEE	—	Average mode enable bit
ADCER	DIAGVAL[1:0]	—	Self diagnosis conversion voltage select bits
	DIAGLD	—	Self diagnosis mode select bit
	DIAGM	—	Self-diagnosis enable bit
ADSTRGR	ADSTRS[3:0]	A/D conversion start trigger select bits	—
	TRSB[5:0]	—	Group B A/D conversion start trigger select bits
	TRSA[5:0]	—	A/D conversion start trigger select bits

Register	Bit	RX630 (S12ADa)	RX660 (S12ADH)
ADEXICR	TSS	Temperature sensor output A/D-converted value addition mode select bit	—
	OCS	Internal reference voltage A/D-converted value addition mode select bit	—
	TSSA	—	Temperature sensor output A/D conversion select bit
	OCSA	—	Internal reference voltage A/D conversion select bit
	TSSB	—	Group B temperature sensor output A/D conversion select bit
	OCSB	—	Group B internal reference voltage A/D conversion select bit
ADGCEXCR	—	—	A/D group C extended input control register
ADGCTRGR	—	—	A/D group C trigger select register
ADDRy	—	A/D data register y (y = 0 to 20)	A/D data register y (y = 0 to 23)
ADDBLDR	—	—	A/D data duplication register
ADDBLDRA	—	—	A/D data duplication register A
ADDBLDRB	—	—	A/D data duplication register B
ADRD	—	—	A/D self-diagnosis data register
ADSSTR01	—	A/D sampling state register 01	—
ADSSTR23	—	A/D sampling state register 23	—
ADSSTRn	—	—	A/D sampling state register n (n = 0 to 15, L, T, O)
ADDISCR	—	—	A/D disconnection detection control register
ADELCCR	—	—	A/D event link control register
ADGSPCR	—	—	A/D group scan priority control register
ADCMPCR	—	—	A/D compare function control register
ADCMPANSR0	—	—	A/D compare function window A channel select register 0
ADCMPANSR1	—	—	A/D compare function window A channel select register 1
ADCMPANSER	—	—	A/D compare function window A extended input select register
ADCMPLR0	—	—	A/D compare function window A compare condition setting register 0
ADCMPLR1	—	—	A/D compare function window A compare condition setting register 1
ADCMPLER	—	—	A/D compare function window A extended input compare condition setting register
ADCMPDR0	—	—	A/D compare function window A lower level setting register
ADCMPDR1	—	—	A/D compare function window A upper level setting register
ADCMPSR0	—	—	A/D compare function window A channel status register 0

Register	Bit	RX630 (S12ADa)	RX660 (S12ADH)
ADCMPSR1	—	—	A/D compare function window A channel status register 1
ADCMPSER	—	—	A/D compare function window A extended input channel status register
ADWINMON	—	—	A/D compare function window A/B status monitoring register
ADCMPBNSR	—	—	A/D compare function window B channel select register
ADWINLLB	—	—	A/D compare function window B lower level setting register
ADWINULB	—	—	A/D compare function window B upper level setting register
ADCMPBSR	—	—	A/D compare function window B channel status register
ADVMONCR	—	—	A/D internal reference voltage monitoring circuit enable register
ADVMONO	—	—	A/D internal reference voltage monitoring circuit output enable register
ADVREFCR	—	—	A/D reference voltage control register

Note: 1. The AVEE bit is valid only when 2-time or 4-time conversion is selected. When average mode is selected (AVEE bit = 1), do not specify 3-time conversion (ADC[2:0] bits = 010b) or 16-time conversion (ADC[2:0] bits = 101b).

2.30 D/A Converter and 12-Bit D/A Converter

Table 2.78 is a Comparative Overview of D/A Converter and 12-bit D/A Converter, and Table 2.79 is a Comparison of D/A Converter and 12-bit D/A Converter Registers.

Table 2.78 Comparative Overview of D/A Converter and 12-bit D/A Converter

Item	RX630 (DAa)	RX660 (R12DAb)
Resolution	10 bits	12 bits
Output channels	2 channel	2 channel
Measure against interference between analog modules	Measure against interference between D/A and A/D converters: D/A converted data update timing is controlled by the 10-bit A/D converter synchronous D/A conversion enable input signal output by the 10-bit A/D converter. This reduces degradation of A/D conversion accuracy due to interference by controlling the timing of the D/A converter inrush current with the enable signal.	Measure against interference between D/A and A/D converters: D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable signal output by the 12-bit A/D converter. This reduces degradation of A/D conversion accuracy due to interference by controlling the timing of the 12-bit /A converter inrush current with the enable signal.
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state
Event link function (input)	—	Ability to start D/A conversion on channel 0 when an event signal is input
Output destination selection	—	Output to external pins and to comparator C can be controlled independently.

Table 2.79 Comparison of D/A Converter and 12-bit D/A Converter Registers

Register	Bit	RX630 (DAa)	RX660 (R12DAb)
DADSELR	—	—	D/A destination select register

2.31 Temperature Sensor

Table 2.80 is a Comparative Overview of Temperature Sensors.

Table 2.80 Comparative Overview of Temperature Sensors

Item	RX630	RX660 (TEMPS)
Temperature sensor voltage output	Output to the 12-bit A/D converter	The temperature sensor outputs a voltage to the 12-bit A/D converter (unit 0).
Low Power Consumption	Ability to transition to module stop state	—
Temperature sensor calibration data	Reference data measured for each chip at the time of shipment from the factory is stored in a register.	Reference data measured for each chip at the time of shipment from the factory is stored in a register.

Table 2.81 Comparison of Temperature Sensor Registers

Register	Bit	RX630	RX660(TEMPS)
TSCR	—	Temperature sensor control register	—
TSCDRH, TSCDRL	—	Temperature sensor calibration data register	—
TSCDR	—	—	Temperature sensor calibration data register

2.32 RAM

Table 2.82 is a Comparative Overview of RAM.

Table 2.82 Comparative Overview of RAM

Item	RX630	RX660
RAM capacity	Up to 128 KB (RAM0: 64 KB, RAM1: 64 KB)	128 KB
RAM address	• 64 KB RAM0: 0000 0000h to 0000 FFFFh (64 KB) • 96 KB RAM0: 0000 0000h to 0000 FFFFh (64 KB) RAM1: 0001 0000h to 0001 7FFFh (32 KB) • 128 KB RAM0: 0000 0000h to 0000 FFFFh (64 KB) RAM1: 0001 0000h to 0001 FFFFh (64 KB)	• RAM: 0000 0000h to 0001 FFFFh
Memory buses	Memory bus 1	Memory bus 1
Access	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing.*1 • The RAM can be enabled or disabled.
Data retention function	RAM0 data can be retained in deep software standby mode.	Not available in deep software standby mode
Low power consumption function	RAM0 and RAM1 can be individually set to module stop state.	Transition to the module stop state is possible.
Error checking	—	• Parity check: Detection of 1-bit errors • A non-maskable interrupt or an interrupt is generated when an error occurs.

Note: 1. An access beyond an 8-byte boundary doubles the number of cycles.

Table 2.83 Comparison of RAM Registers

Register	Bit	RX630	RX660
RAMMODE	—	—	RAM operation mode control register
RAMSTS	—	—	RAM error status register
RAMECAD	—	—	RAM error address capture register
RAMPRCR	—	—	RAM protection register

2.33 Flash Memory

Table 2.84 is a Comparative Overview of Flash Memory, and Table 2.85 is a Comparison of Flash Memory Registers.

Table 2.84 Comparative Overview of Flash Memory

Item	RX630		RX660	
	ROM	E2 data flash	Code flash memory	Data flash memory
Memory capacity	• User area: Up to 2 MB • User boot area: 16 KB	• Data area: 32 KB	• User area: Up to 1 MB • User boot area: 32 KB	• Data area: 32 KB
Read cycles	High-speed read at one ICLK clock cycle	Word or byte access requires reading at 6 FCLK clock cycles.	One cycle	16-bit or 8-bit read access requires 8 FCLK clock cycles.
Programming/ erasing method	• The dedicated sequencer (ECU) that rewrites ROM or E2 data flash is incorporated. • P/E on the ROM or E2 data flash can be performed by issuing commands to the FCU.		• FACI commands specified in the FACI command issuing area (007E 0000h) can be used to program and erase the code flash memory and data flash memory. • A flash memory programmer can be used to program and erase the flash memory via a serial interface (serial programming). • A user program can be used to program and erase the flash memory (self-programming).	
Value after erasure	FFh	Undefined	FFh	Undefined
Background operation (BGO) function	The CPU is able to execute program code from the ROM while the E2 data flash memory is being programmed or erased.		The user area can be read while the data area is being programmed or erased.	
Suspension and resumption	• The CPU is able to execute program code from the ROM during suspension of programming or erasure. • The CPU is able to execute program code from the E2 data flash memory during suspension of programming or erasure. • Programming and erasure of the ROM or E2 data flash memory can be restarted (resumed) after suspension.		—	
Trusted Memory (TM) function	—		Protects against illicit reading of blocks 8 and 9 in the code flash memory.	

Item	RX630		RX660	
	ROM	E2 data flash	Code flash memory	Data flash memory
Units of programming and erasure	• Units of programming for the user area or user boot area: 128 bytes • Units of erasure for the user area: Blocks • Units of erasure for the user boot area: 16 KB	• Unit of programming for the data area: 2 bytes • Unit of erasure for the data area: 32 bytes	• Units of programming for the user area or user boot area: 256 bytes • Units of erasure for the user area: Block units	• Unit of programming for the data area: 4 bytes • Unit of erasure for the data area: Block units
Other functions	—		Interrupts can be accepted during self-programming.	
On-board programming	Rewriting by using boot mode — The asynchronous serial interface (SCI1) is used. — The communication speed is adjusted automatically. — The user boot area is also rewritable. Rewriting by using USB boot mode — USB0 is used. — PC can be directly connected. No special hardware is needed. Rewriting by using user boot mode — A user-specific boot program can be created. Rewriting by a ROM or E2 data flash rewrite routine within a user program — Rewriting of ROM or E2 data flash is possible without resetting the system.		Programming/erasure in boot mode (SCI interface) — The asynchronous serial interface (SCI1) is used. — The communication speed is adjusted automatically. — Programming and erasure of the user boot area is also possible. Programming/erasure in boot mode (FINE interface) — FINE is used. Programming/erasure in user boot mode — A user-specific boot program can be created. Programming/erasure in single-chip mode — Programming or erasure by a routine within a user program for writing to the code flash memory or data flash memory is possible.	
Off-board programming	Rewriting of the user area or user boot area is possible by using a parallel programmer.	The data area cannot be rewritten by using a flash writer.	Programming or erasure of the user area or user boot area by using a parallel programmer is possible.	Programming or erasure of the data area using a parallel programmer is not possible.
Security function and protection function	Unintended rewriting can be prevented by using register settings and lock bits.	• Unintended rewriting or read can be prevented by using register settings. • Protection can be specified in register settings in units of 2 KB.	• Protects against illicit tampering with or reading of data in flash memory. • Protects against erroneous programming of the flash memory.	

Item	RX630		RX660	
	ROM	E2 data flash	Code flash memory	Data flash memory
FCU command lock function	When abnormal operations are detected during programming/erasure, this function disables any further programming/erasure.		—	
Unique ID	A unique 16-byte ID code is provided for each MCU.		A unique 12-byte ID code is provided for each MCU.	

Table 2.85 Comparison of Flash Memory Registers

Register	Bit	RX630	RX660
FMODR	—	Flash mode register	—
FASTAT	DFLWPE	E2 data flash P/E protect error flag	—
	DFLRPE	E2 data flash read protection violation flag	—
	ROMAE	ROM access violation flag	—
	CFAE	—	Code flash memory access violation flag
FAEINT	DFLWPEIE	E2 data flash P/E protection violation interrupt enable bit	—
	DFLRPEIE	E2 data flash read protection violation enable bit	—
	ROMAEIE	ROM access violation interrupt enable bit	—
	CFAEIE	—	Code flash memory access violation interrupt enable bit
DFLRE0	—	E2 data flash read enable register 0	—
DFLRE1	—	E2 data flash read enable register 1	—
DFLWE0	—	E2 data flash P/E enable register 0	—
DFLWE1	—	E2 data flash P/E enable register 1	—
FCURAME	—	FCU RAM enable register	—
FSADDR	—	—	FACI command start address register
FEADDR	—	—	FACI command end address register
FSTATR0 (RX630) FSTATR (RX660)	FLWEERR	—	Flash write/erase protection error flag
	PRGSPD	Program suspend status flag (b0)	Program suspend status flag (b8)
	ERSSPD	Erase suspend status flag (b1)	Erase suspend status flag (b9)
	DBFULL	—	Data buffer full flag
	SUSRDY	Suspend ready flag (b3)	Suspend ready flag (b11)
	PRGERR	Program error flag (b4)	Program error flag (b12)
	ERSERR	Erase error bit (b5)	Erase error bit (b13)
	ILGLERR	Illegal command error flag (b6)	Illegal command error flag (b14)
	FRDY	Flash ready flag (b7) 0: During programming/erasure, during suspending programming/erasure, during the lock bit read 2 command processing, during the peripheral clock notification command processing, or during blank check processing of E2 data flash 1: The above processing is not performed.	Flash ready flag (b15) 0: During processing of a program, block erasure, suspension of programming/erasure, resumption of programming/erasure, forced termination, blank check, configuration setting, lock bit program, or lock bit read command 1: The above processing is not performed.
FSTATR1	—	Flash status register 1	—

Register	Bit	RX630	RX660
FENTRYR	FENTRY0	ROM P/E mode entry bit 0	—
	FENTRY1	ROM P/E mode entry bit 1	—
	FENTRY2	ROM P/E mode entry bit 2	—
	FENTRY3	ROM P/E mode entry bit 3	—
	FENTRYC	—	Code flash memory P/E mode entry bit
	FEKEY[7:0] (RX630) KEY[7:0] (RX660)	Key code	Key code bits
FPROTR	FPKEY[7:0] (RX630) KEY[7:0] (RX660)	Key code	Key code bits
FRESETR	—	Flash reset register	—
FCMDR	—	FCU command register	—
FCPSR	—	FCU processing switching register	—
DFLBCCNT	—	E2 data flash blank check control register	—
FSUINITR	—	—	Flash sequencer set-up initialization register
FLKSTAT	—	—	Lock bit status register
FCMDR	—	—	FACI command register
DFLBCSTAT	—	E2 data flash blank check status register	—
PCKAR	—	Peripheral clock notification register	—
FBCCNT	—	—	Data flash blank check control register
FBCSTAT	—	—	Data flash blank check status register
FPSADDR	—	—	Data flash programming start address register
FCPSR	—	—	Flash sequencer processing switching register
FPCKAR	—	—	Flash sequencer processing clock notification register
UIDRn	—	Unique ID register n (n = 0 to 3)	Unique ID register n (n = 0 to 2)

2.34 Packages

As indicated in Table 2.86, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage. For details, refer to Design Guide for Migration between RX Family Differences in Package External form (R01AN4591EJ).

Table 2.86 Packages

Package Type	RENESASCode	
	RX630	**RX660**
177-pin TFLGA	○	×
176-pin LFBGA	○	×
176-pin LQFP	○	×
145-pin TFLGA	×	○
144-pin LQFP/LFQFP	PLQP0144KA-A	PLQP0144KA-B
100-pin TFLGA	○	×
100-pin LQFP/LFQFP	PLQP0100KB-A	PLQP0100KB-B
80-pin LQFP/LFQFP	PLQP0080KB-A	PLQP0080KB-B
64-pin LFQFP	×	○
48-pin LFQFP	×	○

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by **blue text**. Items that exists on both groups with different specifications are indicated by **red text**. **Black text** indicates there is no differences in the item's specifications between groups.

3.1 144-Pin Package

Table 3.1 is a Comparative Listing of 144-Pin Package Pin Functions.

Table 3.1 Comparative Listing of 144-Pin Package Pin Functions

144-Pin LFQFP	RX630	RX660
1	AVSS0	AVSS0
2	P05/IRQ13/DA1	P05/IRQ13/DA1
3	VREFH	P06
4	P03/IRQ11/DA0	P03/IRQ11/DA0
5	VREFL	P04
6	P02/TMCI1/SCK6/IRQ10/AN020	P02/TMCI1/SCK6/IRQ10
7	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/ AN019	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9
8	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/ AN018	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8
9	PF5/IRQ4	PF5/IRQ4
10	EMLE	EMLE*3/PN7*4
11	PJ5	PJ5/POE8#/CTS2#/RTS2#/SS2#/IRQ13
12	VSS	PJ4
13	PJ3/MTIOC3C/CTS6#/RTS6#/CTS0#/RTS0#/ SS6#/SS0#	PJ3/MTIOC3C/CTS6#/RTS6#/SS6#/CTS0#/ RTS0#/SS0#/IRQ11
14	VCL	VCL
15	VBATT	PJ1/MTIOC3A
16	MD/FINED	MD/FINED/PN6
17	XCIN	XCIN*5/PH7*6
18	XCOUT	XCOUT*5/PH6*6
19	RES#	RES#
20	XTAL/P37	XTAL/P37/IRQ4
21	VSS	VSS
22	EXTAL/P36	EXTAL/P36/IRQ5
23	VCC	VCC
24	P35/NMI	P35/NMI
25	TRST#/P34/MTIOC0A/TMCI3/PO12/POE2#/ SCK6/SCK0/IRQ4	TRST#*3/P34/MTIOC0A/TMCI3/POE10#/ SCK6/SCK0/IRQ4
26	P33/MTIOC0D/TIOCD0/TMRI3/PO11/POE3#/ RXD6/RXD0/SMISO6/SMISO0/SSCL6/ SSCL0/CRX0/IRQ3-DS	P33/MTIOC0D/TMRI3/POE4#/POE11#/ RXD6/SMISO6/SSCL6/RXD0/SMISO0/ SSCL0/CRX0-A/IRQ3-DS
27	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCOUT/RTCIC2/TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/SSDA0/CTX0/IRQ2-DS	P32/MTIOC0C/TMO3/RTCIC2*7/ RTCOUT*7/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0-A/IRQ2-DS
28	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0/IRQ1-DS	TMS*3/P31/MTIOC4D/TMCI2/RTCIC1*7/ CTS1#/RTS1#/SS1#/IRQ1-DS

144-Pin LFQFP	RX630	RX660
29	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB/ IRQ0-DS	TD*3/P30/MTIOC4B/TMRI3/RTCIC0*7/ POE8#/RXD1/SMISO1/SSCL1/IRQ0-DS/ COMP3
30	TCK/FINEC/P27/CS7#/MTIOC2B/TMCI3/ PO7/SCK1/RSPCKB	TCK*3/P27/CS3#/MTIOC2B/TMCI3/ SCK1/IRQ7/CVREFC3
31	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/ MOSIB	TDO*3/P26/CS2#/MTIOC2A/TMO1/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/ IRQ6/CMPC30
32	P25/CS5#/MTIOC4C/MTCLKB/TIOCA4/ PO5/RXD3/SMISO3/SSCL3/ADTRG0#	P25/CS1#/MTIOC4C/MTCLKB/RXD3/ SMISO3/SSCL3/IRQ5/ADTRG0#
33	P24/CS4#/MTIOC4A/MTCLKA/TIOCB4/ TMRI1/PO4/SCK3	P24/CS0#/MTIOC4A/MTCLKA/TMRI1/SCK3/ IRQ12
34	P23/MTIOC3D/MTCLKD/TIOCD3/PO3/ TXD3/CTS0#/RTS0#/SMOSI3/SS0#/SSDA3	P23/MTIOC3D/MTCLKD/TXD3/SMOSI3/ SSDA3/CTS0#/RTS0#/SS0#/IRQ3
35	P22/MTIOC3B/MTCLKC/TIOCC3/TMO0/ PO2/SCK0	P22/MTIOC3B/MTCLKC/TMO0/SCK0/IRQ15
36	P21/MTIOC1B/TIOCA3/TMCI0/PO1/RXD0/ SMISO0/SSCL0/SCL1/IRQ9	P21/MTIOC1B/TMCI0/MTIOC4A/RXD0/ SMISO0/SSCL0/IRQ9
37	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/IRQ8	P20/MTIOC1A/TMRI0/TXD0/SMOSI0/SSDA0 /IRQ8
38	P17/MTIOC3A/MTIOC3B/TIOCB0/TCLKD/ TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/ SSDA3/MISOA/SDA2-DS/IETXD/IRQ7/ ADTRG#	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ MTIOC4B/SCK1/TXD3/SMOSI3/SSDA3/ MISOA-C/SDA2/IRQ7/COMP2
39	P87/TIOCA2	P87/MTIOC4C/SMOSI10/SSDA10/TXD10/ TXD010-B/SMOSI010-B/SSDA010-B/IRQ15
40	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/MOSIA/SCL2-DS/ IERXD/USB0_VBUS/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TMO2/RTCOUT/ TXD1/SMOSI1/SSDA1/RXD3/SMISO3/ SSCL3/MOSIA-C/SCL2/IRQ6/ADTRG0#
41	P86/TIOCA0	P86/MTIOC4D/SMISO10/SSCL10/RXD10/ RXD010-B/SMISO010-B/SSCL010-B/IRQ14
42	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/ CRX1-DS/IRQ5	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/SCK3/CRX0-C/IRQ5/ CMPC20
43	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_DPUPE/IRQ4	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/CTX0-C/IRQ4/CVREFC2
44	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG#	P13/MTIOC0B/TMO3/TXD2/SMOSI2/SSDA2 /SDA0/IRQ3
45	P12/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/IRQ2	P12/MTIC5U/TMCI1/RXD2/SMISO2/SSCL2/ SCL0/IRQ2
46	VCC_USB	PH3/MTIOC4D/TMCI0
47	USB0_DM	PH2/MTIOC4C/TMRI0/TOC1/IRQ1
48	USB0_DP	PH1/MTIOC3D/TMO0/TIC1/IRQ0/ADST0
49	VSS_USB	PH0/MTIOC3B/CACREF/ADTRG0#
50	P56/MTIOC3C/TIOCA1	P56/MTIOC3C/SCK7/IRQ6
51	TRDATA3/P55/WAIT#/MTIOC4D/TMO3/ CRX1/IRQ10	TRDATA3*3/P55/D0[A0/D0]/WAIT#/ MTIOC4D/MTIOC4A/TMO3/TXD7/SMOSI7/ SSDA7/CRX0-D/IRQ10

144-Pin LFQFP	RX630	RX660
52	TRDATA2/P54/ALE/MTIOC4B/TMCI1/CTS2#/ RTS2#/SS2#/CTX1	TRDATA2*3/P54/ALE/D1[A1/D1]/MTIOC4B/ TMCI1/CTS2#/RTS2#/SS2#/CTX0-D/IRQ4
53	BCLK/P53*1	P53/BCLK/PMC0/IRQ3
54	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3	P52/RD#/RXD2/SMISO2/SSCL2/IRQ2
55	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2	P51/WR1#/BC1#/WAIT#/SCK2/PMC0/IRQ1
56	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ IRQ0
57	VSS	VSS
58	TRCLK/P83/MTIOC4C/CTS10#/RTS10#/ SS10#	TRCLK*3/P83/MTIOC4C/SCK10/SS10#/ CTS10#/SCK010-B/CTS010#-A/SS010#-A/ IRQ3
59	VCC	VCC
60	PC7/A23/CS0#/MTIOC3A/MTCLKB/TIOCB6/ TMO2/PO31/TXD8/SMOSI8/SSDA8/MISOA/ IRQ14	UB/PC7/CS0#/MTIOC3A/MTCLKB/TMO2/ CACREF/TOC0/TXD8/SMOSI8/SSDA8/ SMOSI10/SSDA10/TXD10/TXD010-C/ SMOSI010-C/SSDA010-C/MISOA-A/IRQ14
61	PC6/A22/CS1#/MTIOC3C/MTCLKA/TIOCA6/ TMCI2/PO30/RXD8/SMISO8/SSCL8/MOSIA/ IRQ13	PC6/D2[A2/D2]/CS1#/MTIOC3C/MTCLKA/ TMCI2/TIC0/RXD8/SMISO8/SSCL8/ SMISO10/SSCL10/RXD10/RXD010-C/ SMISO010-C/SSCL010-C/MOSIA-A/IRQ13
62	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/ TIOCD6/TCLKF/TMRI2/PO29/SCK8/ RSPCKA	PC5/D3[A3/D3]/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/MTIOC0C/SCK8/SCK10/ SCK010-C/RSPCKA-A/PMC0/IRQ5
63	TRSYNC/P82/MTIOC4A/PO28/TXD10/ SMOSI10/SSDA10	TRSYNC*3/P82/MTIOC4A/SMOSI10/ SSDA10/TXD10/TXD010-A/SMOSI010-A/ SSDA010-A/IRQ2
64	TRDATA1/P81/MTIOC3D/PO27/RXD10/ SMISO10/SSCL10	TRDATA1*3/P81/MTIOC3D/SMISO10/ SSCL10/RXD10/RXD010-A/SMISO010-A/ SSCL010-A/IRQ9
65	TRDATA0/P80/MTIOC3B/PO26/SCK10	TRDATA0*3/P80/MTIOC3B/SCK10/RTS10#/ SCK010-A/RTS010#-A/DE010-A/IRQ8
66	PC4/A20/CS3#/MTIOC3D/MTCLKC/TIOCC6/ TCLKE/TMCI1/PO25/POE0#/SCK5/CTS8#/ RTS8#/SS8#/SSLA0	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ POE0#/MTIOC0A/SCK5/CTS8#/RTS8#/ SS8#/SS10#/CTS10#/RTS10#/CTS010#-B/ RTS010#-B/SS010#-B/DE010-B/SSLA0-A/ PMC0/IRQ12
67	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/ SMOSI5/SSDA5/IETXD	PC3/A19/MTIOC4D/TXD5/SMOSI5/SSDA5/ PMC0/IRQ11
68	P77/CS7#/PO23/TXD11/SMOSI11/SSDA11	TRDATA7*3/P77/SMOSI11/SSDA11/TXD11/ TXD011-A/SMOSI011-A/SSDA011-A/IRQ7
69	P76/CS6#/PO22/RXD11/SMISO11/SSCL11	TRDATA6*3/P76/SMISO11/SSCL11/RXD11/ RXD011-A/SMISO011-A/SSCL011-A/IRQ14
70	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/ SMISO5/SSCL5/SSLA3/IERXD	PC2/A18/MTIOC4B/RXD5/SMISO5/SSCL5/ TXDB011-A/SSLA3-A/IRQ10
71	P75/CS5#/PO20/SCK11	TRSYNC1*3/P75/SCK11/RTS11#/ SCK011-A/RTS011#-A/DE011-A/IRQ13
72	P74/CS4#/PO19/CTS11#/RTS11#/SS11#	TRDATA5*3/P74/A20/SS11#/CTS11#/ CTS011#-A/SS011#-A/IRQ12
73	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2/SDA3/IRQ12	PC1/A17/MTIOC3A/SCK5/TXD011-C/ SMOSI011-C/SSDA011-C/TXDA011-C/ SSLA2-A/IRQ12

144-Pin LFQFP	RX630	RX660
74	PL1	PL1
75	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1/SCL3/IRQ14	PC0/A16/MTIOC3C/CTS5#/RTS5#/SS5#/ RXD011-C/SMISO011-C/SSCL011-C/ SSLA1-A/IRQ14
76	PL0	PL0
77	P73/CS3#/PO16	TRDATA4*3/P73/CS3#/IRQ8
78	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9	PB7/A15/MTIOC3B/TXD9/SMOSI9/SSDA9/ SMOSI11/SSDA11/TXD11/TXD011-B/ SMOSI011-B/SSDA011-B/IRQ15
79	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9	PB6/A14/MTIOC3D/RXD9/SMISO9/SSCL9/ SMISO11/SSCL11/RXD11/RXD011-B/ SMISO011-B/SSCL011-B/IRQ6
80	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE1#/SCK9	PB5/A13/MTIOC2A/MTIOC1B/TMRI1/POE4# /TOC2/SCK9/SCK11/SCK011-B/IRQ13
81	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/SS9#	PB4/A12/CTS9#/RTS9#/SS9#/SS11#/ CTS11#/RTS11#/CTS011#-B/RTS011#-B/ SS011#-B/DE011-B/IRQ4
82	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE3#/SCK4/SCK6	PB3/A11/MTIOC0A/MTIOC4A/TMO0/ POE11#/TIC2/SCK4/SCK6/PMC0/IRQ3
83	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/ RTS4#/CTS6#/RTS6#/SS4#/SS6#	PB2/A10/CTS4#/RTS4#/SS4#/CTS6#/ RTS6#/SS6#/IRQ2
84	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/ PO25/TXD4/TXD6/SMOSI4/SMOSI6/SSDA4/ SSDA6/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TMCI0/TXD4/ SMOSI4/SSDA4/TXD6/SMOSI6/SSDA6/ IRQ4-DS/COMP1
85	P72/CS2#	P72/A19/CS2#/IRQ10
86	P71/CS1#	P71/A18/CS1#/IRQ1
87	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/RXD6/ SMISO4/SMISO6/SSCL4/SSCL6/RSPCKA/ IRQ12	PB0/A8/MTIC5W/MTIOC3D/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/RSPCKA-C/ IRQ12
88	PA7/A7/TIOCB2/PO23/MISOA	PA7/A7/MISOA-B/IRQ7
89	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE2#/CTS5#/RTS5#/SS5#/MOSIA	PA6/A6/MTIC5V/MTCLKB/TMCI3/POE10#/ MTIOC3D/MTIOC6B/CTS5#/RTS5#/SS5#/ CTS12#/RTS12#/SS12#/MOSIA-B/IRQ14
90	PA5/A5/TIOCB1/PO21/RSPCKA	PA5/A5/MTIOC6B/RSPCKA-B/IRQ5
91	VCC	VCC
92	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0/ IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TMRI0/MTIOC4C/ MTIOC7C/TXD5/SMOSI5/SSDA5/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLA0-B/IRQ5-DS/CVREFC1/ADST0
93	VSS	VSS
94	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/ PO19/RXD5/SMISO5/SSCL5/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/MTIC5V/ MTIOC4D/RXD5/SMISO5/SSCL5/IRQ6-DS/ CMPC10
95	PA2/A2/PO18/RXD5/SMISO5/SSCL5/SSLA3	PA2/A2/MTIOC7A/RXD5/SMISO5/SSCL5/ RXD12/SMISO12/SSCL12/RXDX12/ SSLA3-B/IRQ10
96	PA1/A1/MTIOC0B/MTCLKC/TIOCB0/PO17/ SCK5/SSLA2/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ MTIOC3B/SCK5/SCK12/SSLA2-B/IRQ11/ ADTRG0#
97	PA0/A0/BC0#/MTIOC4A/TIOCA0/PO16/ SSLA1	PA0/BC0#/A0/MTIOC4A/CACREF/MTIOC6D /SSLA1-B/IRQ0

144-Pin LFQFP	RX630	RX660
98	P67/CS7#/CRX2*2/IRQ15	P67/MTIOC7C/IRQ15
99	P66/CS6#/CTX2*2	P66/MTIOC7D/IRQ14
100	P65/CS5#	P65/IRQ13
101	PE7/D15[A15/D15]/TIOCB11/MISOB/IRQ7/AN5	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/TOC1/IRQ7/AN015
102	PE6/D14[A14/D14]/TIOCA11/CTS4#/RTS4#/SS4#/MOSIB/IRQ6/AN4	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/TIC1/CTS4#/RTS4#/SS4#/IRQ6/AN014
103	PK5/TXD4/SMOSI4/SSDA4	PK5/TXD4/SMOSI4/SSDA4
104	P70/SCK4	P70/SCK4/IRQ0
105	PK4/RXD4/SMISO4/SSCL4	PK4/RXD4/SMISO4/SSCL4
106	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/TIOCB10/RSPCKB/IRQ5/AN3	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/MTIOC2B/IRQ5/AN013/COMP0
107	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/TIOCA10/PO28/SSLB0/AN2	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/MTIOC1A/MTIOC4A/MTIOC7D/IRQ12/AN012
108	PE3/D11[A11/D11]/MTIOC4B/TIOCB9/PO26/POE8#/CTS12#/RTS12#/SS12#/MISOB/AN1	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/POE8#/MTIOC1B/TOC3/CTS12#/RTS12#/SS12#/IRQ11/AN011
109	PE2/D10[A10/D10]/MTIOC4A/TIOCA9/PO23/RXD12/SMISO12/SSCL12/RXDX12/SSLB3/MOSIB/IRQ7-DS/AN0	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/MTIOC7A/TIC3/RXD12/SMISO12/SSCL12/RXDX12/IRQ7-DS/AN010/CVREFC0
110	PE1/D9[A9/D9]/MTIOC4C/TIOCD9/PO18 TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2/RSPCKB/ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/MTIOC3B/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/IRQ9/AN009/CMPC00
111	PE0/D8[A8/D8]/TIOCC9/SCK12/SSLB1/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/SCK12/IRQ8/AN008
112	P64/CS4#	P64/D3[A3/D3]/IRQ4
113	P63/CS3#	P63/D2[A2/D2]/CS3#/IRQ3
114	P62/CS2#	P62/D1[A1/D1]/CS2#/IRQ2
115	P61/CS1#/CTS9#/RTS9#/SS9#	P61/D0[A0/D0]/CS1#/CTS9#/RTS9#/SS9#/IRQ1
116	PK3/RXD9/SMISO9/SSCL9	PK3/RXD9/SMISO9/SSCL9
117	P60/CS0#/SCK9	P60/CS0#/SCK9/IRQ0
118	PK2/TXD9/SMOSI9/SSDA9	PK2/TXD9/SMOSI9/SSDA9
119	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3/IRQ7/AN7	TRDATA3*3/PD7/D7[A7/D7]/MTIC5U/POE0#/IRQ7/AN023
120	PD6/D6[A6/D6]/MTIC5V/POE1#/SSLC2/IRQ6/AN6	TRDATA2*3/PD6/D6[A6/D6]/MTIC5V/POE4#/MTIOC8A/IRQ6/AN022
121	PD5/D5[A5/D5]/MTIC5W/POE2#/SSLC1/IRQ5/AN013	TRCLK*3/PD5/D5[A5/D5]/MTIC5W/POE10#/MTIOC8C/IRQ5/AN021
122	PD4/D4[A4/D4]/POE3#/SSLC0/IRQ4/AN012	TRSYNC*3/PD4/D4[A4/D4]/POE11#/MTIOC8B/IRQ4/AN020
123	PD3/D3[A3/D3]/TIOCB8/TCLKH/POE8#/RSPCKC/IRQ3/AN011	TRDATA1*3/PD3/D3[A3/D3]/POE8#/MTIOC8D/TOC2/IRQ3/AN019
124	PD2/D2[A2/D2]/MTIOC4D/TIOCA8/MISOC/CRX0/IRQ2/AN010	TRDATA0*3/PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0-B/IRQ2/AN018
125	PD1/D1[A1/D1]/MTIOC4B/TIOCB7/TCLKG/MOSIC/CTX0/IRQ1/AN009	TRDATA7*3/PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0-B/IRQ1/AN017
126	PD0/D0[A0/D0]/TIOCA7/IRQ0/AN008	TRDATA6*3/PD0/D0[A0/D0]/POE4#/IRQ0/AN016

144-Pin LFQFP	RX630	RX660
127	P93/A19/CTS7#/RTS7#/SS7#/AN017	TRSYNC1*3/P93/A19/POE0#/CTS7#/ RTS7#/SS7#/IRQ11
128	P92/A18/RXD7/SMISO7/SSCL7/AN016	TRDATA5*3/P92/A18/POE4#/RXD7/ SMISO7/SSCL7/IRQ10
129	P91/A17/SCK7/AN015	TRDATA4*3/P91/A17/SCK7/IRQ9
130	VSS	PF7
131	P90/A16/TXD7/SMOSI7/SSDA7/AN014	P90/A16/TXD7/SMOSI7/SSDA7/IRQ0
132	VCC	PF6
133	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
134	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
135	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
136	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
137	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
138	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
139	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
140	VREFL0	VREFL0/PJ7
141	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
142	VREFH0	VREFH0/PJ6
143	AVCC0	AVCC0
144	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#

Notes: 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.
2. Only available for products with a ROM capacity of 2 MB or 1.5 MB.
3. Not present on products without a JTAG.
4. Not present on products provided with a JTAG.
5. Not present on products without a sub-clock oscillator.
6. Not present on products provided with a sub-clock oscillator.
7. Not available on products without a sub-clock oscillator.

3.2 100-Pin Package

Table 3.2 is a Comparative Listing of 100-Pin Package Pin Functions.

Table 3.2 Comparative Listing of 100-Pin Package Pin Functions

100-Pin LFQFP	RX630	RX660
1	VREFH	P06
2	EMLE	EMLE*2/P03*3/IRQ11*3/DA0*3
3	VREFL	P04
4	PJ3/MTIOC3C/CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0#	PJ3/MTIOC3C/CTS6#/RTS6#/SS6#/CTS0#/RTS0#/SS0#/IRQ11
5	VCL	VCL
6	VBATT	PJ1/MTIOC3A
7	MD/FINED	MD/FINED/PN6
8	XCIN	XCIN*4/PH7*5
9	XCOUT	XCOUT*4/PH6*5
10	RES#	RES#
11	XTAL/P37	XTAL/P37/IRQ4
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36/IRQ5
14	VCC	VCC
15	P35/NMI	P35/NMI
16	TRST#/P34/MTIOC0A/TMCI3/PO12/POE2#/SCK6/SCK0/IRQ4	TRST#*2/P34/MTIOC0A/TMCI3/POE10#/SCK6/SCK0/IRQ4
17	P33/MTIOC0D/TIOCD0/TMRI3/PO11/POE3#/RXD6/RXD0/SMISO6/SMISO0/SSCL6/SSCL0/CRX0/IRQ3-DS	P33/MTIOC0D/TMRI3/POE4#/POE11#/RXD6/SMISO6/SSCL6/RXD0/SMISO0/SSCL0/CRX0-A/IRQ3-DS
18	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCOUT/RTCIC2/TXD6/TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/CTX0/IRQ2-DS	P32/MTIOC0C/TMO3/RTCIC2*6/RTCOUT*6/POE0#/POE10#/TXD6/SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/CTX0-A/IRQ2-DS
19	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0/IRQ1-DS	TMS*2/P31/MTIOC4D/TMCI2/RTCIC1*6/CTS1#/RTS1#/SS1#/IRQ1-DS
20	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB/IRQ0-DS	TDI*2/P30/MTIOC4B/TMRI3/RTCIC0*6/POE8#/RXD1/SMISO1/SSCL1/IRQ0-DS/COMP3
21	TCK/FINEC/P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB	TCK*2/P27/CS3#/MTIOC2B/TMCI3/SCK1/IRQ7/CVREFC3
22	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/MOSIB	TDO*2/P26/CS2#/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/IRQ6/CMPC30
23	P25/CS5#/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/ADTRG0#	P25/CS1#/MTIOC4C/MTCLKB/RXD3/SMISO3/SSCL3/IRQ5/ADTRG0#
24	P24/CS4#/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3	P24/CS0#/MTIOC4A/MTCLKA/TMRI1/SCK3/IRQ12
25	P23/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/SSDA3	P23/MTIOC3D/MTCLKD/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/SS0#/IRQ3
26	P22/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0	P22/MTIOC3B/MTCLKC/TMO0/SCK0/IRQ15
27	P21/MTIOC1B/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/IRQ9	P21/MTIOC1B/TMCI0/MTIOC4A/RXD0/SMISO0/SSCL0/IRQ9

100-Pin LFQFP	RX630	RX660
28	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/IRQ8	P20/MTIOC1A/TMRI0/TXD0/SMOSI0/SSDA0/ IRQ8
29	P17/MTIOC3A/MTIOC3B/TIOCB0/TCLKD/ TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/ SSDA3/MISOA/SDA2-DS/IETXD/IRQ7/ ADTRG#	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ MTIOC4B/SCK1/TXD3/SMOSI3/SSDA3/ MISOA-C/SDA2/IRQ7/COMP2
30	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/MOSIA/SCL2-DS/ IERXD/USB0_VBUS/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TMO2/RTCOUT*6/ TXD1/SMOSI1/SSDA1/RXD3/SMISO3/ SSCL3/MOSIA-C/SCL2/IRQ6/ADTRG0#
31	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/IRQ5	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/SCK3/CRX0-C/IRQ5/ CMPC20
32	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE/IRQ4	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/CTX0-C/IRQ4/CVREFC2
33	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG#	P13/MTIOC0B/TMO3/TXD2/SMOSI2/SSDA2/ SDA0/IRQ3
34	P12/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/IRQ2	P12/MTIC5U/TMCI1/RXD2/SMISO2/SSCL2/ SCL0/IRQ2
35	VCC_USB	PH3/MTIOC4D/TMCI0
36	USB0_DM	PH2/MTIOC4C/TMRI0/TOC1/IRQ1
37	USB0_DP	PH1/MTIOC3D/TMO0/TIC1/IRQ0/ADST0
38	VSS_USB	PH0/MTIOC3B/CACREF/ADTRG0#
39	P55/WAIT#/MTIOC4D/TMO3/CRX1/IRQ10	P55/D0[A0/D0]/WAIT#/MTIOC4D/MTIOC4A/ TMO3/CRX0-D/IRQ10
40	P54/ALE/MTIOC4B/TMCI1/CTS2#/RTS2#/ CTX1	P54/ALE/D1[A1/D1]/MTIOC4B/TMCI1/CTS2#/ RTS2#/SS2#/CTX0-D/IRQ4
41	BCLK/P53*1	P53/BCLK/PMC0/IRQ3
42	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3	P52/RD#/RXD2/SMISO2/SSCL2/IRQ2
43	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2	P51/WR1#/BC1#/WAIT#/SCK2/PMC0/IRQ1
44	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/IRQ0
45	PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/ PO31/TXD8/SMOSI8/SSDA8/MISOA/IRQ14	UB/PC7/CS0#/MTIOC3A/MTCLKB/TMO2/ CACREF/TOC0/TXD8/SMOSI8/SSDA8/ SMOSI10/SSDA10/TXD10/TXD010-C/ SMOSI010-C/SSDA010-C/MISOA-A/IRQ14
46	PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/ PO30/RXD8/SMISO8/SSCL8/MOSIA/IRQ13	PC6/D2[A2/D2]/CS1#/MTIOC3C/MTCLKA/ TMCI2/TIC0/RXD8/SMISO8/SSCL8/ SMISO10/SSCL10/RXD10/RXD010-C/ SMISO010-C/SSCL010-C/MOSIA-A/IRQ13
47	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/ TMRI2/PO29/SCK8/RSPCKA	PC5/D3[A3/D3]/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/MTIOC0C/SCK8/SCK10/ SCK010-C/RSPCKA-A/PMC0/IRQ5
48	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/ SSLA0	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ POE0#/MTIOC0A/SCK5/CTS8#/RTS8#/ SS8#/SS10#/CTS10#/RTS10#/CTS010#-B/ RTS010#-B/SS010#-B/DE010-B/SSLA0-A/ PMC0/IRQ12
49	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/ SMOSI5/SSDA5/IETXD	PC3/A19/MTIOC4D/TXD5/SMOSI5/SSDA5/ PMC0/IRQ11

100-Pin LFQFP	RX630	RX660
50	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/ SMISO5/SSCL5/SSLA3/IERXD	PC2/A18/MTIOC4B/RXD5/SMISO5/SSCL5/ TXDB011-A/SSLA3-A/IRQ10
51	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2/IRQ12	PC1/A17/MTIOC3A/SCK5/TXD011-C/ SMOSI011-C/SSDA011-C/TXDA011-C/ SSLA2-A/IRQ12
52	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1/IRQ14	PC0/A16/MTIOC3C/CTS5#/RTS5#/SS5#/ RXD011-C/SMISO011-C/SSCL011-C/ SSLA1-A/IRQ14
53	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9	PB7/A15/MTIOC3B/TXD9/SMOSI9/SSDA9/ SMOSI11/SSDA11/TXD11/TXD011-B/ SMOSI011-B/SSDA011-B/IRQ15
54	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9	PB6/A14/MTIOC3D/RXD9/SMISO9/SSCL9/ SMISO11/SSCL11/RXD11/RXD011-B/ SMISO011-B/SSCL011-B/IRQ6
55	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE1#/SCK9	PB5/A13/MTIOC2A/MTIOC1B/TMRI1/ POE4#/TOC2/SCK9/SCK11/SCK011-B/ IRQ13
56	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/ SS9#	PB4/A12/CTS9#/RTS9#/SS9#/SS11#/ CTS11#/RTS11#/CTS011#-B/RTS011#-B/ SS011#-B/DE011-B/IRQ4
57	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE3#/SCK6	PB3/A11/MTIOC0A/MTIOC4A/TMO0/ POE11#/TIC2/SCK4/SCK6/PMC0/IRQ3
58	PB2/A10/TIOCC3/TCLKC/PO26/CTS6#/ RTS6#/SS6#	PB2/A10/CTS4#/RTS4#/SS4#/CTS6#/ RTS6#/SS6#/IRQ2
59	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD6/SMOSI6/SSDA6/ IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TMCI0/TXD4/ SMOSI4/SSDA4/TXD6/SMOSI6/SSDA6/ IRQ4-DS/COMP1
60	VCC	VCC
61	PB0/A8/MTIC5W/TIOCA3/PO24/RXD6/ SMISO6/SSCL6/RSPCKA/IRQ12	PB0/A8/MTIC5W/MTIOC3D/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/RSPCKA-C/ IRQ12
62	VSS	VSS
63	PA7/A7/TIOCB2/PO23/MISOA	PA7/A7/MISOA-B/IRQ7
64	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE2#/CTS5#/RTS5#/SS5#/MOSIA	PA6/A6/MTIC5V/MTCLKB/TMCI3/POE10#/ MTIOC3D/MTIOC6B/CTS5#/RTS5#/SS5#/ CTS12#/RTS12#/SS12#/MOSIA-B/IRQ14
65	PA5/A5/TIOCB1/PO21/RSPCKA	PA5/A5/MTIOC6B/RSPCKA-B/IRQ5
66	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0/ IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TMRI0/MTIOC4C/ MTIOC7C/TXD5/SMOSI5/SSDA5/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLA0-B/IRQ5-DS/CVREFC1/ADST0
67	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/ PO19/RXD5/SMISO5/SSCL5/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/MTIC5V/ MTIOC4D/RXD5/SMISO5/SSCL5/IRQ6-DS/ CMPC10
68	PA2/A2/PO18/RXD5/SMISO5/SSCL5/SSLA3	PA2/A2/MTIOC7A/RXD5/SMISO5/SSCL5/ RXD12/SMISO12/SSCL12/RXDX12/ SSLA3-B/IRQ10
69	PA1/A1/MTIOC0B/MTCLKC/TIOCB0/PO17/ SCK5/SSLA2/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ MTIOC3B/SCK5/SCK12/SSLA2-B/IRQ11/ ADTRG0#

100-Pin LFQFP	RX630	RX660
70	PA0/A0/BC0#/MTIOC4A/TIOCA0/PO16/ SSLA1	PA0/BC0#/A0/MTIOC4A/CACREF/MTIOC6D/ SSLA1-B/IRQ0
71	PE7/D15[A15/D15]/MISOB/IRQ7/AN5	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/IRQ7/AN015
72	PE6/D14[A14/D14]/MOSIB/IRQ6/AN4	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/CTS4#/RTS4#/SS4#/IRQ6/AN014
73	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/ RSPCKB/IRQ5/AN3	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/IRQ5/AN013/COMP0
74	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/ PO28/SSLB0/AN2	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/MTIOC4A/MTIOC7D/IRQ12/ AN012
75	PE3/D11[A11/D11]/MTIOC4B/PO26/POE8#/ CTS12#/RTS12#/SS12#/MISOB/AN1	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ POE8#/MTIOC1B/TOC3/CTS12#/RTS12#/ SS12#/IRQ11/AN011
76	PE2/D10[A10/D10]/MTIOC4A/PO23/RXD12/ SMISO12/SSCL12/RXDX12/SSLB3/MOSIB/ IRQ7-DS/AN0	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ MTIOC7A/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/IRQ7-DS/AN010/CVREFC0
77	PE1/D9[A9/D9]/MTIOC4C/PO18/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2/ RSPCKB/ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/IRQ9/AN009/CMPC00
78	PE0/D8[A8/D8]/SCK12/SSLB1/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/ SCK12/IRQ8/AN008
79	PD7/D7[A7/D7]/MTIC5U/POE0#/IRQ7/AN7	PD7/D7[A7/D7]/MTIC5U/POE0#/IRQ7/AN023
80	PD6/D6[A6/D6]/MTIC5V/POE1#/IRQ6/AN6	PD6/D6[A6/D6]/MTIC5V/POE4#/MTIOC8A/ IRQ6/AN022
81	PD5/D5[A5/D5]/MTIC5W/POE2#/IRQ5/ AN013	PD5/D5[A5/D5]/MTIC5W/POE10#/MTIOC8C/ IRQ5/AN021
82	PD4/D4[A4/D4]/POE3#/IRQ4/AN012	PD4/D4[A4/D4]/POE11#/MTIOC8B/IRQ4/ AN020
83	PD3/D3[A3/D3]/POE8#/IRQ3/AN011	PD3/D3[A3/D3]/POE8#/MTIOC8D/TOC2/ IRQ3/AN019
84	PD2/D2[A2/D2]/MTIOC4D/CRX0*1/ IRQ2/AN010	PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0-B/ IRQ2/AN018
85	PD1/D1[A1/D1]/MTIOC4B/CTX0*1/IRQ1/ AN009	PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0-B/ IRQ1/AN017
86	PD0/D0[A0/D0]/IRQ0/AN008	PD0/D0[A0/D0]/POE4#/IRQ0/AN016
87	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
88	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
89	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
90	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
91	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
92	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
93	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
94	VREFL0	VREFL0/PJ7
95	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
96	VREFH0	VREFH0/PJ6
97	AVCC0	AVCC0
98	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
99	AVSS0	AVSS0
100	P05/IRQ13/DA1	P05/IRQ13/DA1

Notes: 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.
2. Not present on products without a JTAG.
3. Not present on products provided with a JTAG.
4. Not present on products without a sub-clock oscillator.
5. Not present on products provided with a sub-clock oscillator.
6. Not available on products without a sub-clock oscillator.

3.3 80-Pin Package

Table 3.3 is a Comparative Listing of 80-Pin Package Pin Functions.

Table 3.3 Comparative Listing of 80-Pin Package Pin Functions

80-Pin LFQFP	RX630	RX660
1	VREFH	P06
2	EMLE	P03/IRQ11/DA0
3	VREFL	P04
4	VCL	VCL
5	VBATT	PJ1/MTIOC3A
6	MD/FINED	MD/FINED/PN6
7	XCIN	XCIN*1/PH7*2
8	XCOUT	XCOUT*1/PH6*2
9	RES#	RES#
10	XTAL/P37	XTAL/P37/IRQ4
11	VSS	VSS
12	EXTAL/P36	EXTAL/P36/IRQ5
13	VCC	VCC
14	P35/NMI	P35/NMI
15	TRST#/P34/MTIOC0A/TMCI3/PO12/POE2#/SCK6/IRQ4	P34/MTIOC0A/TMCI3/POE10#/SCK6/SCK0/IRQ4
16	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCOUT/RTCIC2/TXD6/SMOSI6/SSDA6/IRQ2-DS	P32/MTIOC0C/TMO3/RTCIC2*3/RTCOUT*3/POE0#/POE10#/TXD6/SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/CTX0-A/IRQ2-DS
17	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0/IRQ1-DS	P31/MTIOC4D/TMCI2/RTCIC1*3/CTS1#/RTS1#/SS1#/IRQ1-DS
18	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB/IRQ0-DS	P30/MTIOC4B/TMRI3/RTCIC0*3/POE8#/RXD1/SMISO1/SSCL1/IRQ0-DS/COMP3
19	TCK/FINEC/P27/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB	P27/MTIOC2B/TMCI3/SCK1/IRQ7/CVREFC3
20	TDO/P26/MTIOC2A/TMO1/PO6/TXD1/SMOSI1/SSDA1/MOSIB	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/IRQ6/CMPC30
21	P21/MTIOC1B/TIOCA3/TMCI0/PO1/IRQ9	P21/MTIOC1B/TMCI0/MTIOC4A/RXD0/SMISO0/SSCL0/IRQ9
22	P20/MTIOC1A/TIOCB3/TMRI0/PO0/IRQ8	P20/MTIOC1A/TMRI0/TXD0/SMOSI0/SSDA0/IRQ8
23	P17/MTIOC3A/MTIOC3B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/MISOA/SDA2-DS/IETXD/IRQ7/ADTRG#	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/MTIOC4B/SCK1/TXD3/SMOSI3/SSDA3/MISOA-C/SDA2/IRQ7/COMP2
24	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/SMOSI1/SSDA1/MOSIA/SCL2-DS/IERXD/USB0_VBUS/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TMO2/RTCOUT*3/TXD1/SMOSI1/SSDA1/RXD3/SMISO3/SSCL3/MOSIA-C/SCL2/IRQ6/ADTRG0#
25	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SMISO1/SSCL1/CRX1-DS/IRQ5	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/SMISO1/SSCL1/SCK3/CRX0-C/IRQ5/CMPC20

80-Pin LFQFP	RX630	RX660
26	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_DPUPE/IRQ4	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/CTX0-C/IRQ4/CVREFC2
27	P13/MTIOC0B/TIOCA5/TMO3/PO13/ SDA0[FM+]/IRQ3/ADTRG#	P13/MTIOC0B/TMO3/SDA0/IRQ3
28	P12/TMCI1/SCL0[FM+]/IRQ2	P12/MTIC5U/TMCI1/SCL0/IRQ2
29	VCC_USB	PH3/MTIOC4D/TMCI0
30	USB0_DM	PH2/MTIOC4C/TMRI0/TOC1/IRQ1
31	USB0_DP	PH1/MTIOC3D/TMO0/TIC1/IRQ0/ADST0
32	VSS_USB	PH0/MTIOC3B/CACREF/ADTRG0#
33	P55/MTIOC4D/TMO3/CRX1/IRQ10	P55/MTIOC4D/MTIOC4A/TMO3/CRX0-D/ IRQ10
34	P54/MTIOC4B/TMCI1/CTX1	P54/MTIOC4B/TMCI1/CTX0-D/IRQ4
35	PC7/MTIOC3A/MTCLKB/TMO2/PO31/ TXD8/SMOSI8/SSDA8/MISOA/IRQ14	UB/PC7/MTIOC3A/MTCLKB/TMO2/ CACREF/TOC0/TXD8/SMOSI8/SSDA8/ SMOSI10/SSDA10/TXD10/TXD010-C/ SMOSI010-C/SSDA010-C/MISOA-A/IRQ14
36	PC6/MTIOC3C/MTCLKA/TMCI2/PO30/ RXD8/SMISO8/SSCL8/MOSIA/IRQ13	PC6/MTIOC3C/MTCLKA/TMCI2/TIC0/RXD8/ SMISO8/SSCL8/SMISO10/SSCL10/RXD10/ RXD010-C/SMISO010-C/SSCL010-C/ MOSIA-A/IRQ13
37	PC5/MTIOC3B/MTCLKD/TMRI2/PO29/ SCK8/RSPCKA	PC5/MTIOC3B/MTCLKD/TMRI2/MTIOC0C/ SCK8/SCK10/SCK010-C/RSPCKA-A/PMC0/ IRQ5
38	PC4/MTIOC3D/MTCLKC/TMCI1/PO25/ POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/ MTIOC0A/SCK5/CTS8#/RTS8#/SS8#/ SS10#/CTS10#/RTS10#/CTS010#-B/ RTS010#-B/SS010#-B/DE010-B/ SSLA0-A/PMC0/IRQ12
39	PC3/MTIOC4D/TCLKB/PO24/TXD5/ SMOSI5/SSDA5/IETXD	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5/ PMC0/IRQ11
40	PC2/MTIOC4B/TCLKA/PO21/RXD5/ SMISO5/SSCL5/SSLA3/IERXD	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/ TXDB011-A/SSLA3-A/IRQ10
41	PB7/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9	PB7/MTIOC3B/TXD9/SMOSI9/SSDA9/ SMOSI11/SSDA11/TXD11/TXD011-B/ SMOSI011-B/SSDA011-B/IRQ15
42	PB6/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9	PB6/MTIOC3D/RXD9/SMISO9/SSCL9/ SMISO11/SSCL11/RXD11/RXD011-B/ SMISO011-B/SSCL011-B/IRQ6
43	PB5/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/ PO29/POE1#/SCK9	PB5/MTIOC2A/MTIOC1B/TMRI1/POE4#/ TOC2/SCK9/SCK11/SCK011-B/IRQ13
44	PB4/TIOCA4/PO28/CTS9#/RTS9#/SS9#	PB4/CTS9#/RTS9#/SS9#/SS11#/CTS11#/ RTS11#/CTS011#-B/RTS011#-B/SS011#-B/ DE011-B/IRQ4
45	PB3/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/ TMO0/PO27/POE3#/SCK6	PB3/MTIOC0A/MTIOC4A/TMO0/POE11#/ TIC2/SCK4/SCK6/PMC0/IRQ3
46	PB2/TIOCC3/TCLKC/PO26/CTS6#/RTS6#/ SS6#	PB2/CTS4#/RTS4#/SS4#/CTS6#/RTS6#/ SS6#/IRQ2
47	PB1/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/ PO25/TXD6/SMOSI6/SSDA6/IRQ4-DS	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD4/ SMOSI4/SSDA4/TXD6/SMOSI6/SSDA6/ IRQ4-DS/COMP1

80-Pin LFQFP	RX630	RX660
48	VCC	VCC
49	PB0/MTIC5W/TIOCA3/PO24/RXD6/ SMISO6/SSCL6/RSPCKA/IRQ12	PB0/MTIC5W/MTIOC3D/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/RSPCKA-C/ IRQ12
50	VSS	VSS
51	PA6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE2#/CTS5#/RTS5#/SS5#/MOSIA	PA6/MTIC5V/MTCLKB/TMCI3/POE10#/ MTIOC3D/MTIOC6B/CTS5#/RTS5#/SS5#/ CTS12#/RTS12#/SS12#/MOSIA-B/IRQ14
52	PA5/TIOCB1/PO21/RSPCKA	PA5/MTIOC6B/RSPCKA-B/IRQ5
53	PA4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0/ IRQ5-DS	PA4/MTIC5U/MTCLKA/TMRI0/MTIOC4C/ MTIOC7C/TXD5/SMOSI5/SSDA5/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLA0-B/IRQ5-DS/CVREFC1/ADST0
54	PA3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/ PO19/RXD5/SMISO5/SSCL5/IRQ6-DS	PA3/MTIOC0D/MTCLKD/MTIC5V/MTIOC4D/ RXD5/SMISO5/SSCL5/IRQ6-DS/CMPC10
55	PA2/PO18/RXD5/SMISO5/SSCL5/SSLA3	PA2/MTIOC7A/RXD5/SMISO5/SSCL5/ RXD12/SMISO12/SSCL12/RXDX12/ SSLA3-B/IRQ10
56	PA1/MTIOC0B/MTCLKC/TIOCB0/PO17/ SCK5/SSLA2/IRQ11	PA1/MTIOC0B/MTCLKC/MTIOC7B/ MTIOC3B/SCK5/SCK12/SSLA2-B/ IRQ11/ADTRG0#
57	PA0/MTIOC4A/TIOCA0/PO16/SSLA1	PA0/MTIOC4A/CACREF/MTIOC6D/ SSLA1-B/IRQ0
58	PE5/MTIOC4C/MTIOC2B/RSPCKB/IRQ5/ AN3	PE5/MTIOC4C/MTIOC2B/IRQ5/AN013/ COMP0
59	PE4/MTIOC4D/MTIOC1A/PO28/SSLB0/AN2	PE4/MTIOC4D/MTIOC1A/MTIOC4A/ MTIOC7D/IRQ12/AN012
60	PE3/MTIOC4B/PO26/POE8#/CTS12#/ RTS12#/SS12#/MISOB/AN1	PE3/MTIOC4B/POE8#/MTIOC1B/TOC3/ CTS12#/RTS12#/SS12#/IRQ11/AN011
61	PE2/MTIOC4A/PO23/RXD12/SMISO12/ SSCL12/RXDX12/SSLB3/MOSIB/ IRQ7-DS/AN0	PE2/MTIOC4A/MTIOC7A/TIC3/RXD12/ SMISO12/SSCL12/RXDX12/IRQ7-DS/ AN010/CVREFC0
62	PE1/MTIOC4C/PO18/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/SSLB2/RSPCKB/ ANEX1	PE1/MTIOC4C/MTIOC3B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/IRQ9/AN009/ CMPC00
63	PE0/SCK12/SSLB1/ANEX0	PE0/MTIOC3D/SCK12/IRQ8/AN008
64	PD2/MTIOC4D/IRQ2/AN010	PD2/MTIOC4D/TIC2/CRX0-B/IRQ2/AN018
65	PD1/MTIOC4B/IRQ1/AN009	PD1/MTIOC4B/POE0#/CTX0-B/IRQ1/AN017
66	PD0/IRQ0/AN008	PD0/POE4#/IRQ0/AN016
67	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
68	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
69	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
70	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
71	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
72	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
73	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
74	VREFL0	VREFL0/PJ7
75	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
76	VREFH0	VREFH0/PJ6
77	AVCC0	AVCC0

80-Pin LFQFP	RX630	RX660
78	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
79	AVSS0	AVSS0
80	P05/IRQ13/DA1	P05/IRQ13/DA1

Notes: 1. Not present on products without a sub-clock oscillator.
2. Not present on products provided with a sub-clock oscillator.
3. Not available on products without a sub-clock oscillator.

4. Important Information when Migrating Between MCUs

This section presents important information on differences between the RX660 Group and the RX630 Group.

For notes regarding software, see section 4.1, Notes on Functional Design.

4.1 Notes on Functional Design

Some software that runs on the RX630 Group is compatible with the RX660 Group. Nevertheless, appropriate caution must be exercised due to differences in aspects such as operation timing and electrical characteristics.

Software-related considerations regarding function settings that differ between the RX660 Group and RX630 Group are as follows: For differences between modules and functions, refer to section 2, Comparative Overview of Specifications.

For further information, refer to the User's Manual: Hardware of each MCU group, listed in section 5, Reference Documents.

4.1.1 VCL Pin (External Capacitance)

When connecting a smoothing capacitor to the VCL pin of the RX660 Group to stabilize the internal power supply, select a capacitor rated at 0.47 µF.

4.1.2 Main Clock Oscillator

When connecting a resonator to the EXTAL pin or XTAL pin of the RX660 Group, select a resonator with the resonator frequency of 8 MHz to 24 MHz.

4.1.3 Software Configurable Interrupts

The software configurable interrupt has been added on the RX660 Group. Any of the interrupt sources for peripheral modules can be selected and assigned to interrupt vector numbers 128 to 255. These interrupts are categorized as software configurable interrupt A or software configurable interrupt B according to the operating clock of the peripheral module. For details on the configuration setting command, refer to the *RX660 Group User's Manual: Hardware* listed in section 5, Reference Documents.

4.1.4 Clock Frequency Settings

On the RX660 Group, the system clock (ICLK) and peripheral module clocks A, B, and D (PCLKA, PCLKB, and PCLKD) must be set within the following ranges:

- PCLKA ≥ PCLKB
- PCLKB:PCLKD = 1:1, 2:1, 4:1, or 1:2

4.1.5 Voltage Level Settings

On the RX660 Group, the values of the following registers must be changed appropriately according to the operating voltage: Operating-mode voltage level setting register (VOLSR), voltage detection level select register (LVDLVLR) for the voltage detection circuit, and option function select register 1 (OFS1) for option-setting memory. The values must be set by using a program.

4.1.6 RIIC Operating Voltage Setting

When using the RIIC on the RX660 Group, it is necessary to specify the power supply voltage range to preserve the slope characteristics. VCC is set to a value of 4.5 V or greater by default. If it is set to a value less than 4.5 V, make sure to change the voltage range before activating the RIIC. For details, refer to the description of the VOLSR.RICVLS bit in RX660 Group User's Manual: Hardware.

4.1.7 Option-Setting Memory

On the RX630 Group, the ID code protection codes and ID code protection codes for the on-chip debugger are located in the flash memory, but on the RX660 Group, they are located in the option-setting memory. Note that how to specify the settings differs between the groups.

4.1.8 PLL Circuit

The frequency multiplication factor of the PLL circuit can be set to 8, 10, 12, 16, 20, 24, 25, 50 on the RX630 Group and to 10 to 30 (in 0.5 increments) on the RX660 Group. To use the PLL circuit, change the setting of the PLLCR.STC bits to an appropriate value.

4.1.9 Exception Vector Table

On the RX630 Group, addresses allocated in a vector table are fixed. On the RX660 Group, addresses in the vector table can be relocated by using the value set in the exception table register (EXTB) as the start address.

4.1.10 Performing RAM Self-Diagnostics on Save Register Banks

On the RX660 Group save register banks are configured in the RAM. The save register banks are provided with a buffer, so when a SAVE instruction is used to write data to a register and then a RSTR instruction is used to read data from the same register, the data is actually read from the buffer and not from the RAM memory cells. When performing self-diagnostics on the RAM in a save register bank, use the following sequence of steps for checking the written data in order to prevent the data from being read from the buffer:

(1) Use the SAVE instruction to write data to the bank that is the target of the diagnostic test.
(2) Use the SAVE instruction to write data to a bank other than that written to in step 1.
(3) Use the RSTR instruction to read data from the bank written to in step 1.

4.1.11 Restrictions on Compare Function

The compare function of the 12-bit A/D converter on the RX660 Group is subject to the following restrictions.

1. The compare function cannot be used together with the self-diagnosis function or double trigger mode. (The compare function is not available for the ADRD, ADDBLDR, ADDBLDRA, and ADDBLDRB registers.)
2. It is necessary to specify single scan mode when using match or mismatch event outputs.
3. When the temperature sensor or internal reference voltage is selected for window A, window B operations are disabled.
4. When the temperature sensor or internal reference voltage is selected for window B, window A operations are disabled.
5. It is not possible to set the same channel for window A and window B.
6. It is necessary to set the reference voltage values such that the high-side reference voltage value is equal to or larger than the low-side reference voltage value.

4.1.12 I^2C Bus Interface Noise Elimination

The RX630 Group has integrated analog noise filters on the SCL and SDA lines, but the RX660 Group has no integrated analog noise filters.

4.1.13 Initialization of Port Direction Register (PDR)

The method of initializing the PDR register differs between the RX630 Group and RX660 Group, even on products with the same pin count.

4.1.14 MTIOC Pin Output Level when Counter Stops

While the MTIOC pin of the RX660 Group is operating in output state, writing 0 to the CSTn bit of TSTRA or TSTR causes the counter to stop. At this time, in complementary PWM mode or reset-synchronized PWM mode on the RX660 Group, the initial output level set in the TOCR1A or TOCR2A register is output by the MTIOC pin. In any mode other than the complementary PWM or reset-synchronized PWM mode, the output compare level of the MTIOC pin is retained. If data is written to the TIOR register with the CSTn bit set to 0, the pin output level is updated to the initial output value set in the register.

4.1.15 A/D Conversion Start Requests in Complementary PWM Mode

To generate PWM waveforms in complementary PWM mode on the RX660 Group, MTU4.TGRA (MTU7.TGRA) compare match detection is performed with not only MTU4.TCNT (MTU7.TCNT) but also with MTU3.TCNT (MTU6.TCNT) or TCNTSA (TCNTSB). Therefore, TRGA4N (TRGA7N) is also generated when a compare match with MTU3.TCNT (MTU6.TCNT) or TCNTSA (TCNTSB) occurs. When operating MTU3 and MTU4 (MTU6 and MTU7) in complementary PWM mode to generate A/D conversion start requests, use compare match between MTU4.TCNT (MTU7.TCNT) and MTU4.TADCORA or TADCORB (MTU7.TADCORA or TADCORB) as the A/D conversion start request.

4.1.16 High-Impedance Control of Unselected MTU Pins

On the RX660 Group, when high-impedance control is enabled for MTU pins in the POECR1 or POECR2 register and the control conditions are met, output on the pins multiplexed with the MTU function enters the high-impedance state regardless of whether or not the MTU function is selected. To prevent pin output from entering the high-impedance state unexpectedly, make settings such that the MTU pins selected in the PmnPFS register of the MPC and the MTU pins selected in the pin selection register of the POE3 match.

4.1.17 A/D Scan Conversion End Interrupt Generation

On the RX660 Group, when a scan is started by a software trigger and the ADIE bit has been set to 1, an A/D scan conversion end interrupt is generated when the scan ends, even if double trigger mode is selected.

4.1.18 Input Buffer Control by DIRQnE Bits (n = 0 to 15)

On the RX660 Group, setting, a DPSIERy.DIRQnE (y = 0 or 1, n = 0 to 15) bit to 1 enables the input buffer of the corresponding pin among IRQ0-DS to IRQ15-DS. Note that once the input buffer is enabled, inputs on these pins are sent to the corresponding DPSIFRy.DIRQnF (y = 0 or 1, n = 0 to 15) bits, but they are not sent to the interrupt controller, peripheral modules, and I/O ports.

4.1.19 Scan Conversion Time of 12-Bit A/D Converter

The scan conversion time differs between the RX630 Group and RX660 Group. The scan conversion time (t_{SCAN}) for each group of a single scan where the number of selected channels is n is expressed by the equations below.

For details, refer to the description of the 12-bit A/D converter analog input sampling time and scan conversion time in the User's Manual: Hardware of the RX630 Group and RX660 Group, listed in section 5, Reference Documents.

RX630: $t_{SCAN} = t_D + (t_{CONV} \times n) + t_{ED}$

RX660: $t_{SCAN} = t_D + (t_{DIS} \times n) + t_{DIAG} + (t_{CONV} \times n) + t_{ED}$

t_{SCAN} (when converting temperature sensor output or internal reference voltage) = $t_D + (t_{ADIS} \times m) + (t_{CONV} \times m) + t_{ED}$

t_D: Start-of-scanning-delay time
t_{SPL}: Sampling time
t_{DIS}: Disconnection detection assist processing time
t_{DIAG}: Self-diagnosis A/D conversion processing time
t_{CONV}: A/D conversion processing time
t_{ED}: End-of-scanning-delay time
t_{ADIS}: Auto-discharge processing time during A/D conversion of temperature sensor output and internal reference voltage

4.1.20 D/A Converter Settings

When configuring D/A converter settings on the RX660 Group, first set comparator C as the output destination in the D/A destination select register (DADSELR) and wait for the D/A converter output to stabilize before enabling comparator operation.

Similarly, stop the comparator temporarily before making changes to the settings of the D/A converter, then wait for the D/A converter output to stabilize before enabling comparator operation.

4.1.21 Comparator C Operation in Module Stop State

On the RX660 Group, the analog circuits of comparator C do not stop operating if a transition to the module stop state is made while comparator C is operating, so the analog power current associated with comparator C remains unchanged. If it is necessary to reduce analog power current consumption in the module stop state, stop operation of comparator C by clearing the CMPCTL.HCMPON bit to 0.

4.1.22 Comparator C Operation in Software Standby Mode

On the RX660 Group, the analog circuits of comparator C do not stop operating if a transition to software standby mode is made while comparator C is operating, so the analog power current associated with comparator C remains unchanged. If it is necessary to reduce analog power current consumption in software standby mode, stop operation of comparator C by clearing the CMPCTL.HCMPON bit to 0.

4.1.23 Interrupt Requests in Software Standby Mode

On the RX660 Group, if interrupt requests are generated in software standby mode due to interrupt sources not specified in the sources of recovery from software standby mode, these requests are retained in the interrupt controller. These interrupt requests are sequentially processed after recovery from software standby mode by another source. However, such interrupt requests are not retained for external pin interrupts.

4.1.24 Timer Mode Register Setting for ELC Event Input

To set the MTU to ELC action operation on the RX660 Group, set the timer mode register (TMDR) of the relevant channel to its initial value (00h).

5. Reference Documents

User's Manual: Hardware

RX630 Group User's Manual: Hardware Rev1.60 (R01UH0040EJ0160)
(The latest version can be downloaded from the Renesas Electronics website.)

RX660 Group User's Manual: Hardware Rev.1.00 (R01UH0937EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News
(The latest information can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This module reflects the content of the following technical updates:

TN-RX*-A099A/E
TN-RX*-A116A/E
TN-RX*-A115A/E
TN-RX*-A118A/E
TN-RX*-A120A/E
TN-RX*-A130B/E
TN-RX*-A138A/E
TN-RX*-A141A/E
TN-RX*-A147A/E
TN-RX*-A151A/E
TN-RX*-A152A/E
TN-RX*-A167A/E
TN-RX*-A177A/E
TN-RX*-A186A/E
TN-RX*-A193A/E
TN-RX*-A0147B/E
TN-RX*-A0226A/E
TN-RX*-A0226A/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jul.24.23	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (Max.) and VIH (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (Max.) and VIH (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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