RX660 Group, RX210 Group

Differences Between the RX660 Group and the RX210 Group

Introduction

This application note is intended as a reference to points of difference between the peripheral functions, I/O registers, and pin functions of the RX660 Group and RX210 Group, as well as a guide to key points to consider when migrating between the two groups.

Unless specifically otherwise noted, the information in this application note applies to the 144-pin package version of the RX660 Group and the 145-pin package version of the RX210 Group (chip version B) as the maximum specifications. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the User's Manual: Hardware of the products in question.

Target Devices

RX660 Group and RX210 Group

Contents

1. Comparison of Built-In Functions of RX660 Group and RX210 Group

A comparison of the built-in functions of the RX660 Group and RX210 Group is provided below. For details of the functions, see section 2, Comparative Overview of Specifications and section 5, Reference Documents.

Table 1.1 is a comparison of built-in functions of RX660 Group and RX210 Group.

Table 1.1 Comparison of Built-In Functions of RX660 Group and RX210 Group

Function	RX210	RX660
CPU	●	
Operating modes	●/▲	
Address space	▲	
Resets	○	
Option-setting memory (OFSM)	▲	
Voltage detection circuit (LVDAa): RX210, (LVDA): RX660	■/▲	
Clock generation circuit	●	
Clock frequency accuracy measurement circuit (CAC)	●	
Low power consumption	■	
Register write protection function	▲	
Exception handling	▲	
Interrupt controller (ICUb) RX210, (ICUF): RX660	●	
Buses	▲	
Memory-protection unit (MPU)	×	○
DMA controller	▲	
Data transfer controller (DTCa): RX210, (DTCb): RX660	●	
Event link controller (ELC)	●/▲	
I/O ports	●/▲	
Multi-function pin controller (MPC)	●	
Multi-function timer pulse unit 2 (MTU2a): RX210, Multi-function timer pulse unit 3 (MTU3a): RX660	●/▲	
Port output enable 2 (POE2a): RX210, Port output enable 3 (POE3a): RX660	▲	
16-bit timer pulse unit (TPUa)	○	×
8-bit timer (TMR): RX210, (TMRb): RX660	●/▲	
Compare match timer (CMT)	○	
Compare match timer W (CMTW)	×	○
Realtime clock (RTCb): RX210, (RTCC): RX660	●	
Watchdog timer (WDTA)	▲	
Independent watchdog timer (IWDTa)	▲	
Serial communications interface (SCIc, SCId): RX210, (SCIk, SCIm, SCIh): RX660	●/▲	
Serial communications interface (RSCI)	×	○
I²C bus interface (RIIC): RX210, (RIICa): RX660	▲	
CAN FD module (CANFD-Lite)	×	○
Serial peripheral interface (RSPI): RX210, (RSPId): RX660	▲	
CRC calculator (CRC): RX210, (CRCA): RX660	●	
Remote control signal receiver (REMCa)	×	○
12-bit A/D converter (S12ADb): RX210, (S12ADH): RX660	●	
D/A converter (DA): RX210, 12-bit D/A converter (R12DAb): RX660	●	
Temperature sensor (TEMPSa): RX210, (TEMPS): RX660	▲	

Function	RX210	RX660
Comparator A (CMPA): RX210	○	×
Comparator B (CMPB): RX210 Comparator C (CMPC): RX660	▲	
Data operation circuit (DOC): RX210, (DOCA): RX660	●	
RAM	▲	
ROM (flash memory for code storage): (RX210), E2 DataFlash (flash memory for data storage): (RX210), Flash memory (FLASH): RX660	▲	
Packages	▲	

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Differences in register specifications are not listed.

2.1 CPU

Table 2.1 is a comparative overview of CPU, and Table 2.2 is a comparison of CPU registers.

Table 2.1 Comparative Overview of CPU

Item	RX210	RX660
CPU	• Maximum operating frequency: 50 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Eight 32-bit registers — Accumulator: One 64-bit register • Basic instructions: 73 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits	• Maximum operating frequency: 120 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • 113 instructions — Standard provided instructions: 111 Basic instructions: 77, variable-length instruction format Single-precision floating point instructions: 11 DSP instructions: 23 — Instructions for register bank save function: 2 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits
FPU	—	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard
Register bank save function	—	• Fast collective saving and restoration of the values of CPU registers • 16 save register banks

Table 2.2 Comparison of CPU Registers

Register	Bit	RX210	RX660
FPSW	—	—	Single-precision floating-point status word
EXTB	—	—	Exception table register
ACC (RX210) ACC0, ACC1 (RX660)	—	Accumulator	Accumulator 0, accumulator 1

2.2 Operating Modes

Table 2.3 is a comparative overview of operating modes, and Table 2.4 is a comparison of operating mode registers.

Table 2.3 Comparative Overview of Operating Modes

Item	RX210	RX660
Operating modes specified by mode setting pins	Single-chip mode	Single-chip mode
	Boot mode	Boot mode (SCI interface)
	User boot mode	User boot mode
	—	Boot mode (FINE interface)
Operating modes selected by register settings	Single-chip mode, user boot mode On-chip ROM disabled extended mode On-chip ROM enabled extended mode	Single-chip mode, user boot mode On-chip ROM disabled extended mode On-chip ROM enabled extended mode

Table 2.4 Comparison of Operating Mode Registers

Register	Bit	RX210	RX660
SYSCR1	—	System control register 1	System control register 1
		Initial value after reset differs.	
VOLSR	—	—	Voltage level setting register

2.3 Address Space

Figure 2.1 is a comparative memory map of single-chip mode, Figure 2.2 is a comparative memory map of on-chip ROM enabled extended mode, and Figure 2.3 is a comparative memory map of on-chip ROM disabled extended mode.

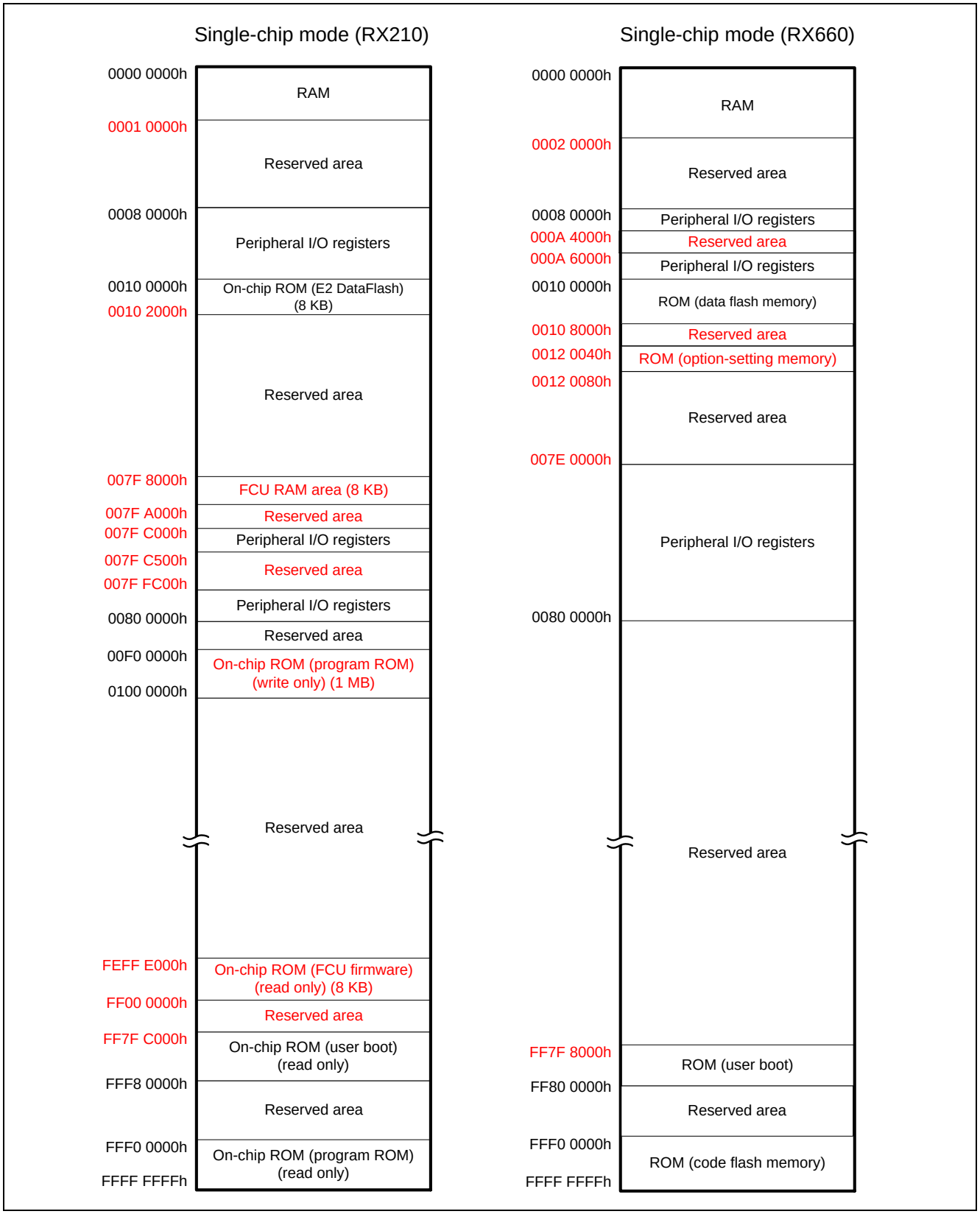

Figure 2.1 Comparative Memory Map of Single-Chip Mode

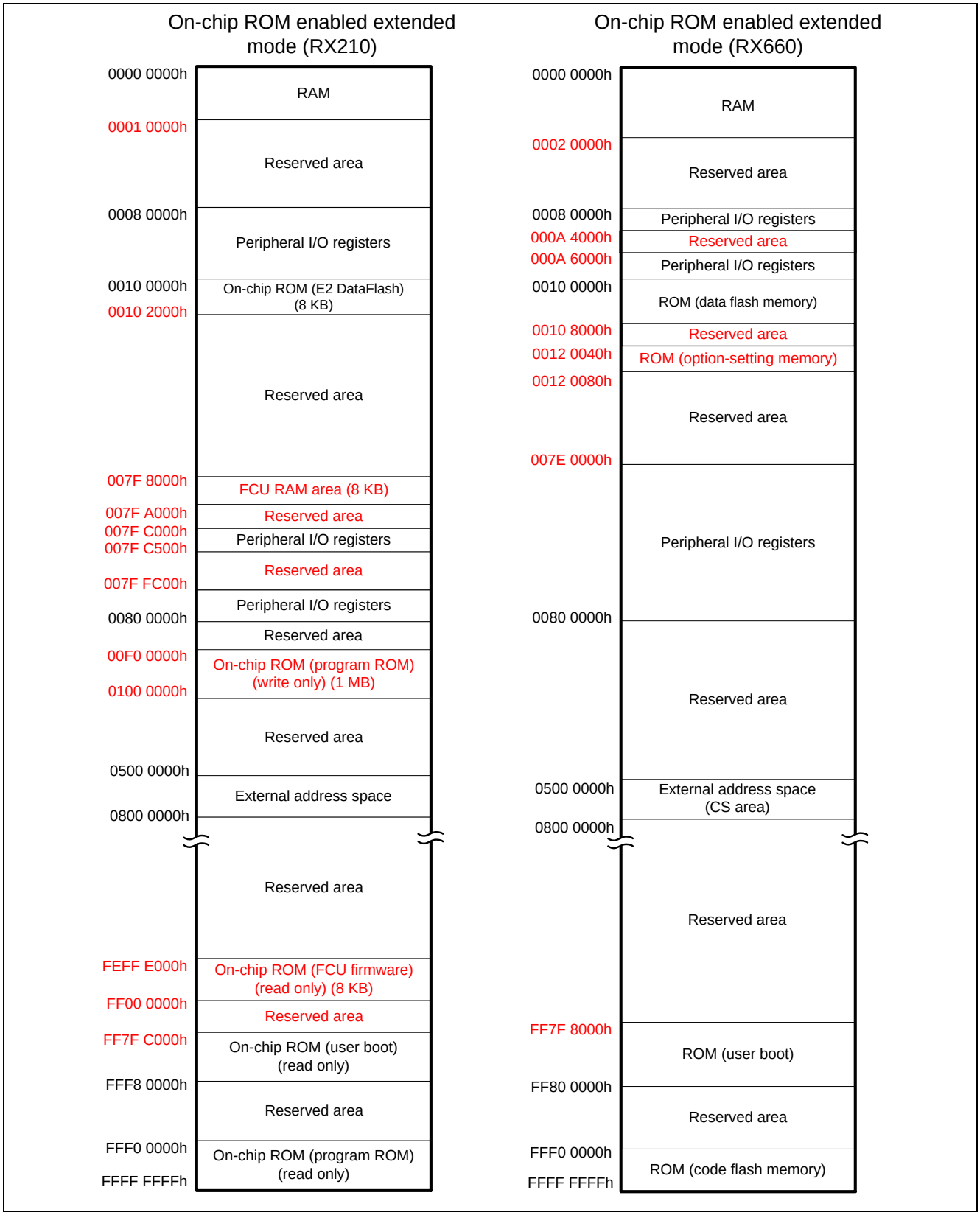

Figure 2.2 Comparative Memory Map of On-Chip ROM Enabled Extended Mode

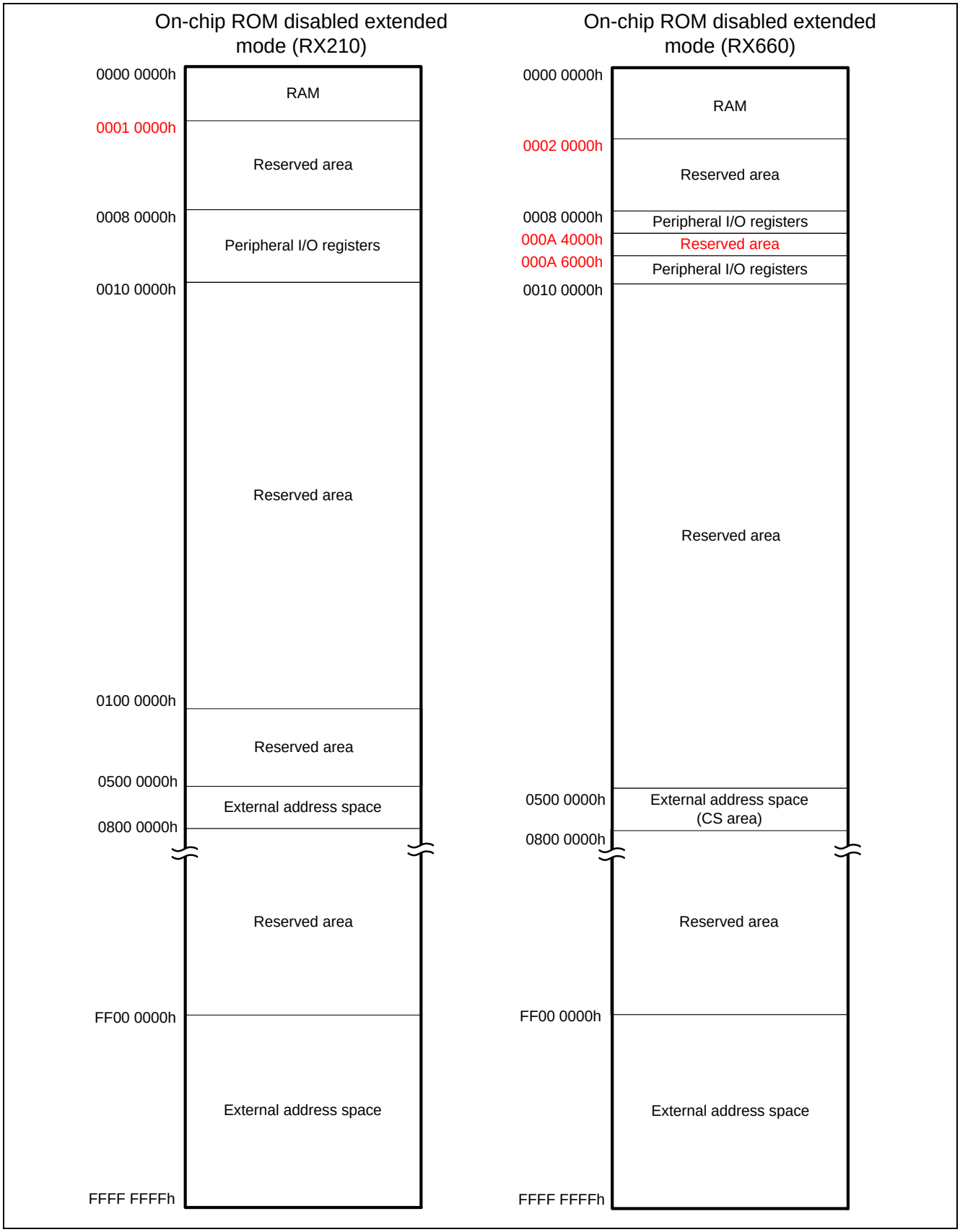

Figure 2.3 Comparative Memory Map of On-Chip ROM Disabled Extended Mode

2.4 Option-Setting Memory

Figure 2.4 is a comparison of option-setting memory areas, and Table 2.5 is a comparison of option-setting memory registers.

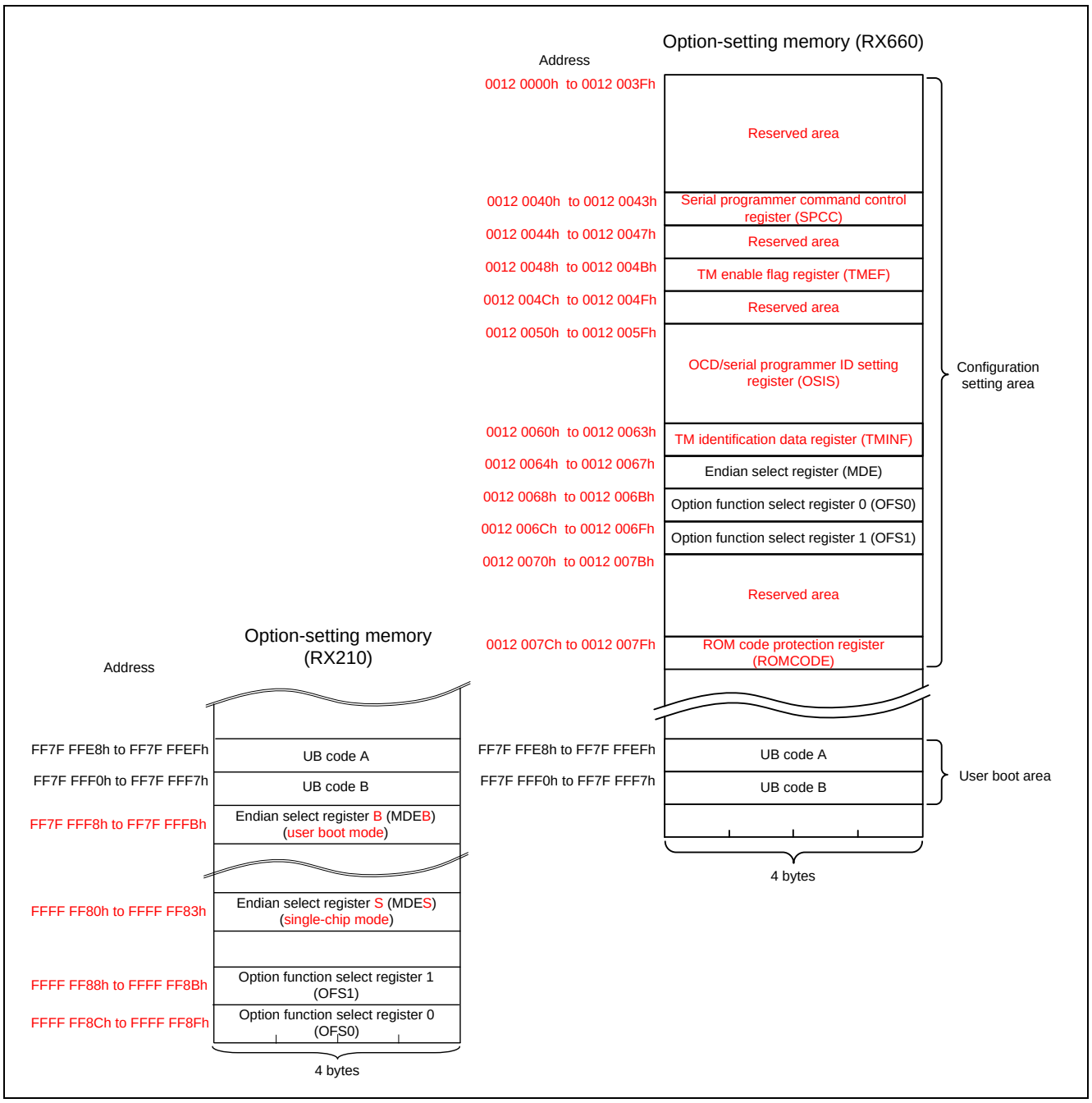

Figure 2.4 Comparison of Option-Setting Memory Areas

Table 2.5 Comparison of Option-Setting Memory Registers

Register	Bit Name	RX210 (OFSM)	RX660 (OFSM)
SPCC	—	—	Serial programmer command control register
OSIS	—	—	OCD/serial program ID setting register
OFS1	VDSEL	Voltage detection 0 level select bit b1 b0 0 0: 3.80 V is selected. 0 1: 2.80 V is selected. 1 0: 1.90 V is selected. 1 1: 1.72 V is selected.	Voltage detection 0 level select bit b1 b0 0 0: Reserved 0 1: Reserved 1 0: 2.83 V is selected. 1 1: 4.22 V is selected.
MDEB MDES (RX210) MDE (RX660)	—	Endian select register B Endian select register S	Endian select register
TMEF	—	—	TM enable flag register
TMINF	—	—	TM identification data register
ROMCODE	—	—	ROM code protection register

2.5 Voltage Detection Circuit

Table 2.6 is a comparative overview of the voltage detection circuits, and Table 2.7 is a comparison of voltage detection circuit registers.

Table 2.6 Comparative Overview of Voltage Detection Circuits

Item		RX210 (LVDAa)			RX660 (LVDA)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	When voltage drops below Vdet0	When voltage rises above or drops past Vdet1	When voltage rises above or drops past Vdet2 Switching between VCC and the voltage input on the CMPA2 pin can be accomplished using the LVCMPCR.EXVCCINP2 bit.	When voltage drops below Vdet0	When voltage rises above or drops past Vdet1	When voltage rises above or drops past Vdet2
	Detection voltage	Selectable from four levels using the OFS1 register	Selectable from 16 levels using LVDLVLR.LVD1LVL[3:0] bits	Varies according to whether VCC or the CMPA2 pin input voltage is selected. Selectable from 16 levels using LVDLVLR.LVD2LVL[3:0] bits	Selectable from two levels using OFS1.VDSEL[1:0] bits.	Selectable from five levels using LVDLVLR.LVD1LVL[3:0] bits	Selectable from five levels using LVDLVLR.LVD2LVL[3:0] bits
	Monitoring flags	—	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1 LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2 LVD2SR.LVD2DET flag: Vdet2 passage detection	—	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1 LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2 LVD2SR.LVD2DET flag: Vdet2 passage detection

Item		RX210 (LVDAa)			RX660 (LVDA)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
Voltage detection processing	Reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet0 > VCC: CPU restart timing after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable between after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC: CPU restart timing selectable between after specified time with VCC > Vdet2 or Vdet2 > VCC	Reset when Vdet0 > VCC: CPU restart timing after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable between after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC: CPU restart timing selectable between after specified time with VCC > Vdet2 or Vdet2 > VCC
	Interrupts	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
			Selectable between non-maskable or maskable interrupt	Selectable between non-maskable or maskable interrupt		Selectable between non-maskable or maskable interrupt	Selectable between non-maskable or maskable interrupt
			Interrupt request issued when Vdet1 > VCC, VCC > Vdet1, or both	Interrupt request issued when Vdet2 > VCC, VCC > Vdet2, or both		Interrupt request issued when Vdet1 > VCC, VCC > Vdet1, or both	Interrupt request issued when Vdet2 > VCC, VCC > Vdet2, or both
Digital filter	Enable/ disable switching	Digital filter function not available.	Available	Available	Digital filter function not available.	Available	Available
	Sampling time	—	1/n LOCO frequency × 2 (n: 1, 2, 4, 8)	1/n LOCO frequency × 2 (n: 1, 2, 4, 8)	—	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)
Event link function		—	Available: Event output at Vdet2 passage detection	Available: Event output at Vdet2 passage detection	—	Available: Event output at Vdet2 passage detection	Available: Event output at Vdet2 passage detection

Table 2.7 Comparison of Voltage Detection Circuit Registers

Register	Bit	RX210 (LVDAa)	RX660 (LVDA)
LVD2CR1	—	Voltage monitoring 2/comparator A2 interrupt/ELC event generation condition select bits	Voltage monitoring 2 interrupt generation condition select bits
LVD2SR	LVD2DET	Voltage monitoring 2/comparator A2 voltage change detection flag	Voltage monitoring 2 voltage change detection flag
	LVD2MON	Voltage monitoring 2/comparator A2 signal monitor flag	Voltage monitoring 2 signal monitor flag
LVCMPCR	EXVREFINP1	Comparator A1 reference voltage external input select bit	—
	EXVCCINP1	Comparator A1 comparison voltage external input select bit	—
	EXVREFINP2	Comparator A2 reference voltage external input select bit	—
	EXVCCINP2	Comparator A2 comparison voltage external input select bit	—
	LVD1E	Voltage detection 1/comparator A1 enable bit	Voltage detection 1 enable bit
	LVD2E	Voltage detection 2/comparator A2 enable bit	Voltage detection 2 enable bit
LVDLVLR	LVD1LVL[3:0]	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 0 0 0: 4.15 V 0 0 0 1: 4.00 V 0 0 1 0: 3.85 V 0 0 1 1: 3.70 V 0 1 0 0: 3.55 V 0 1 0 1: 3.40 V 0 1 1 0: 3.25 V 0 1 1 1: 3.10 V 1 0 0 0: 2.95 V 1 0 0 1: 2.80 V 1 0 1 0: 2.65 V 1 0 1 1: 2.50 V 1 1 0 0: 2.35 V 1 1 0 1: 2.20 V 1 1 1 0: 2.05 V 1 1 1 1: 1.90 V	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 1 0 0: 4.57 V (Vdet1_0) 0 1 0 1: 4.47 V (Vdet1_1) 0 1 1 0: 4.32 V (Vdet1_2) 1 0 1 0: 2.93 V (Vdet1_3) 1 0 1 1: 2.88 V (Vdet1_4) Settings other than the above are prohibited.

Register	Bit	RX210 (LVDAa)	RX660 (LVDA)
LVDLVLR	LVD2LVL[1:0] (RX210) LVD2LVL[3:0] (RX660)	Voltage detection 2 level select bits (Standard voltage during drop in voltage) (When LVCMPCR.EXVCCINP2 = 0 (VCC selected)) b7 b4 0 0 0 0: 4.15 V 0 0 0 1: 4.00 V 0 0 1 0: 3.85 V 0 0 1 1: 3.70 V 0 1 0 0: 3.55 V 0 1 0 1: 3.40 V 0 1 1 0: 3.25 V 0 1 1 1: 3.10 V 1 0 0 0: 2.95 V 1 0 0 1: 2.80 V 1 0 1 0: 2.65 V 1 0 1 1: 2.50 V 1 1 0 0: 2.35 V 1 1 0 1: 2.20 V 1 1 1 0: 2.05 V 1 1 1 1: 1.90 V (When LVCMPCR.EXVCCINP2 = 1 (CMPA2 pin selected)) b7 b4 0 0 0 1: 1.33 V Settings other than the above are prohibited.	Voltage detection 2 level select bits (Standard voltage during drop in voltage) b7 b4 0 1 0 0: 4.57 V (Vdet2_0) 0 1 0 1: 4.47 V (Vdet2_1) 0 1 1 0: 4.32 V (Vdet2_2) 1 0 1 0: 2.93 V (Vdet2_3) 1 0 1 1: 2.88 V (Vdet2_4) Settings other than the above are prohibited.
LVD1CR0	LVD1RIE	Voltage monitoring 1/comparator A1 interrupt/reset enable bit	Voltage monitoring 1 interrupt/reset enable bit
	LVD1DFDIS	Voltage monitoring 1/comparator A1 digital filter disable mode select bit	Voltage monitoring 1 digital filter disable mode select bit
	LVD1CMPE	Voltage monitoring 1 circuit/ comparator A1 comparison result output enable bit	Voltage monitoring 1 circuit comparison result output enable bit
	LVD1FSAMP [1:0]	Sampling clock select bits b5 b4 0 0: 1/1 LOCO frequency 0 1: 1/2 LOCO frequency 1 0: 1/4 LOCO frequency 1 1: 1/8 LOCO frequency	Sampling clock select bits b5 b4 0 0: 1/2 LOCO frequency 0 1: 1/4 LOCO frequency 1 0: 1/8 LOCO frequency 1 1: 1/16 LOCO frequency
	LVD1RI	Voltage monitoring 1 circuit/ comparator A1 mode select bit	Voltage monitoring 1 circuit mode select bit
	LVD1RN	Voltage monitoring 1/comparator A1 reset negation select bit	Voltage monitoring 1 reset negation select bit

Register	Bit	RX210 (LVDAa)	RX660 (LVDA)
LVD2CR0	LVD2RIE	Voltage monitoring 2/comparator A2 interrupt/reset enable bit	Voltage monitoring 2 interrupt/reset enable bit
	LVD2DFDIS	Voltage monitoring 2/comparator A2 digital filter disable mode select bit	Voltage monitoring 2 digital filter disable mode select bit
	LVD2CMPE	Voltage monitoring 2 circuit/ comparator A2 comparison result output enable bit	Voltage monitoring 2 circuit comparison result output enable bit
	LVD2FSAMP [1:0]	Sampling clock select bits b5 b4 0 0: 1/1 LOCO frequency 0 1: 1/2 LOCO frequency 1 0: 1/4 LOCO frequency 1 1: 1/8 LOCO frequency	Sampling clock select bits b5 b4 0 0: 1/2 LOCO frequency 0 1: 1/4 LOCO frequency 1 0: 1/8 LOCO frequency 1 1: 1/16 LOCO frequency
	LVD2RI	Voltage monitoring 2 circuit/ comparator A2 mode select bit	Voltage monitoring 2 circuit mode select bit
	LVD2RN	Voltage monitoring 2/comparator A2 reset negation select bit	Voltage monitoring 2 reset negation select bit

2.6 Clock Generation Circuit

Table 2.8 is a comparative overview of the clock generation circuits, and Table 2.9 is a comparison of clock generation circuit registers.

Table 2.8 Comparative Overview of Clock Generation Circuits

Item	RX210	RX660
Use	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, ROM, and RAM.	• Generates the system clock (ICLK) to be supplied to the CPU, TFU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the RSPI, SCIm, RSCI, MTU, and CANFD.
	• Of the peripheral module clocks (PCLKB and PCLKD) supplied to the peripheral modules. Peripheral module clocks (PCLKD) is the operating clock for the S12AD, and (PCLKB) is the operating clock for modules other than S12AD.	• Of the peripheral module clock (PCLKB) supplied to the peripheral modules. • Generates the peripheral module clock (for analog conversion) (PCLKD) to be supplied to the S12AD.
	• Generates the FlashIF clock (FCLK) to be supplied to the FlashIF.	• Generates the FlashIF clock (FCLK) to be supplied to the FlashIF.
	• Generates the external bus clock (BCLK) to be supplied to the external bus.	• Generates the external bus clock (BCLK) to be supplied to the external bus.
	• Generates the CAC clock (CACCLK) to be supplied to the CAC.	• Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CANFD clock (CANFDCLK) to be supplied to the CANFD. • Generates the CANFD main clock (CANFDMCLK) to be supplied to the CANFD.
	• Generates the RTC-dedicated sub-clock (RTCSCLK) to be supplied to the RTC.	• Generates the RTC sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the REMC sub-clock (REMSCLK) to be supplied to the REMC.
	• Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.	• Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT

Item	RX210	RX660
Operating frequency	• ICLK: 50 MHz (max.) • PCLKB: 32 MHz (max.) • PCLKD: 50 MHz (max.) • FCLK: — 4 MHz to 32 MHz (for programming and erasing the ROM and E2 DataFlash) — 32 MHz (max.) (for reading from the E2 DataFlash) • BCLK: 25 MHz (max.) • BCLK pin output: 12.5 MHz (max.) • CACCLK: Same as clock from respective oscillators • RTCSCLK: 32.768 kHz • IWDTCLK: 15 kHz	• ICLK: 120 MHz (max.) • PCLKA:120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKD: 8 MHz to 60 MHz (when 12-bit A/D converter is operating) • FCLK: — 4 MHz to 60 MHz (during programming or erasing of code flash memory or data flash memory) — 60 MHz (max.) (for reading from the data flash) • BCLK: 60 MHz (max.) • BCLK pin output: 40 MHz (max.) • CACCLK: Same as clock from respective oscillators • CANFDCLK: 60 MHz (max.) • CANFDMCLK: 24 MHz (max.) • RTCSCLK: 32.768 kHz • REMCLK: 32.768 kHz • IWDTCLK: 120 kHz
Main clock oscillator	• Resonator frequency: 1 MHz to 20 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: Crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and MTU pin can be forcedly driven to high-impedance. • Drive capacity switching function	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and MTU pin can be forcedly driven to high-impedance. • Drive capacity switching function
Sub-clock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: Crystal • Connection pin: XCIN, XCOUT • Drive capacity switching function	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: Crystal • Connection pins: XCIN and XCOUT • Drive capacity switching function
PLL frequency synthesizer	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 12.5 MHz • Frequency multiplication ratio: Selectable from 8, 10, 12, 16, 20, 24, and 25 • VCO oscillation frequency: 50 MHz to 100 MHz	• Input clock source: Main clock, HOCO • Input pulse frequency division ratio: Selectable from 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable from 10 to 30 (increments of 0.5) • Output clock frequency of PLL frequency synthesizer: 120 MHz to 240 MHz

Item	RX210	RX660
High-speed on-chip oscillator (HOCO)	• Oscillation frequency: 32 MHz/36.864 MHz/40 MHz/50 MHz • HOCO power supply control	• Oscillation frequency: 16 MHz/18 MHz/20 MHz • HOCO power supply control • FLL function (only present in products incorporating a sub-clock oscillator)
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 125 kHz	Oscillation frequency: 240 kHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 125 kHz	Oscillation frequency: 120 kHz
BCLK pin output control function	• Selectable between BCLK clock output or high-level output. • Output clock selectable between BCLK or BCLK/2.	• Selectable between BCLK clock output or high-level output. • Output clock selectable between BCLK or BCLK/2.
Event link function (output)	—	Detection of stopping of the main clock oscillator
Event link function (input)	—	Switching of the clock source to the low-speed on-chip oscillator

Table 2.9 Comparison of Clock Generation Circuit Registers

Register	Bit	RX210	RX660
SCKCR	PCKC[3:0]	—	The PCLKC is not implemented on this MCU. These bits should be set to 0001b.
	PCKA[3:0]	—	Peripheral module clock A (PCLKA) select bits
SCKCR2	—	—	System clock control register 2
SCKCR3	CKSEL[2:0]	Clock source select bits [Chip version A] b10 b8 0 0 0: LOCO 0 0 1: HOCO 0 1 1: Sub-clock oscillator 1 0 0: PLL circuit [Chip versions B and C] b10 b8 0 0 0: LOCO 0 0 1: HOCO 0 1 0: Main clock oscillator 0 1 1: Sub-clock oscillator 1 0 0: PLL circuit Settings other than the above are prohibited.	Clock source select bits b10 b8 0 0 0: LOCO 0 0 1: HOCO 0 1 0: Main clock oscillator 0 1 1: Sub-clock oscillator 1 0 0: PLL circuit Settings other than the above are prohibited.
VRCR	—	Voltage regulator control register	—
PLLCR	PLIDIV[1:0]	PLL input frequency division ratio select bits b1 b0 0 0: ×1/1 0 1: ×1/2 1 0: ×1/4 1 1: Setting prohibited.	PLL input frequency division ratio select bits b1 b0 0 0: ×1/1 0 1: ×1/2 1 0: ×1/3 1 1: Setting prohibited.
	STC[4:0] (RX210) STC[5:0] (RX660)	Frequency multiplication factor select bits b12 b8 0 0 1 1 1: ×8 0 1 0 0 1: ×10 0 1 0 1 1: ×12 0 1 1 1 1: ×16 1 0 0 1 1: ×20 1 0 1 1 1: ×24 1 1 0 0 0: ×25	Frequency multiplication factor select bits b13 b8 0 1 0 0 1 1: ×10.0 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11.0 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12.0 0 1 1 0 0 0: ×12.5 0 1 1 0 0 1: ×13.0

Register	Bit	RX210	RX660
PLLCR	STC[4:0] (RX210) STC[5:0] (RX660)	Settings other than the above are prohibited.	0 1 1 0 1 0: ×13.5 0 1 1 0 1 1: ×14.0 0 1 1 1 0 0: ×14.5 0 1 1 1 0 1: ×15.0 0 1 1 1 1 0: ×15.5 0 1 1 1 1 1: ×16.0 1 0 0 0 0 0: ×16.5 1 0 0 0 0 1: ×17.0 1 0 0 0 1 0: ×17.5 1 0 0 0 1 1: ×18.0 1 0 0 1 0 0: ×18.5 1 0 0 1 0 1: ×19.0 1 0 0 1 1 0: ×19.5 1 0 0 1 1 1: ×20.0 1 0 1 0 0 0: ×20.5 1 0 1 0 0 1: ×21.0 1 0 1 0 1 0: ×21.5 1 0 1 0 1 1: ×22.0 1 0 1 1 0 0: ×22.5 1 0 1 1 0 1: ×23.0 1 0 1 1 1 0: ×23.5 1 0 1 1 1 1: ×24.0 1 1 0 0 0 0: ×24.5 1 1 0 0 0 1: ×25.0 1 1 0 0 1 0: ×25.5 1 1 0 0 1 1: ×26.0 1 1 0 1 0 0: ×26.5 1 1 0 1 0 1: ×27.0 1 1 0 1 1 0: ×27.5 1 1 0 1 1 1: ×28.0 1 1 1 0 0 0: ×28.5 1 1 1 0 0 1: ×29.0 1 1 1 0 1 0: ×29.5 1 1 1 0 1 1: ×30.0 Settings other than the above are prohibited.
SOSCCR	SOSTP	Sub-clock oscillator stop bits	Sub-clock oscillator stop bits
		Initial value after a reset differs.	
HOCOCR2	HCFRQ [1:0]	HOCO frequency setting bits b1 b0 0 0: 32 MHz 0 1: 36.864 MHz 1 0: 40 MHz 1 1: 50 MHz	HOCO frequency setting bits b1 b0 0 0: 16 MHz 0 1: 18 MHz 1 0: 20 MHz Settings other than the above are prohibited.
HOCOTRRn	—	High-speed on-chip oscillator trimming register n (n = 0 to 3)	—
FLLCR1	—	—	FLL control register 1
FLLCR2	—	—	FLL control register 2
OSCOVFSR	—	—	Oscillation stabilization flag register

Register	Bit	RX210	RX660
MOSCWTCR	—	—	Main clock oscillator wait control register
SOSCWTCR	—	—	Sub-clock oscillator wait control register
SOFCR	—	—	Sub-clock oscillator forced oscillation control register
MOFCR	MODRV [2:0]	Main clock oscillator drive capability switch bits	—
	MODRV2 [1:0]	Main clock oscillator drive capability switch 2 bits b5 b4 0 1: 1 MHz to 8 MHz 1 0: 8.1 MHz to 15.9 MHz 1 1: 16 MHz to 20 MHz Settings other than the above are prohibited.	Main clock oscillator drive capability switch 2 bits b5 b4 0 0: 20.1 MHz to 24 MHz 0 1: 16.1 MHz to 20 MHz 1 0: 8.1 MHz to 16 MHz 1 1: 8 MHz
PLLPCR	—	PLL power control register	—

2.7 Clock Frequency Accuracy Measurement Circuit

Table 2.10 is a comparative overview of clock frequency accuracy measurement circuits, and Table 2.11 is a comparison of clock frequency accuracy measurement circuit registers.

Table 2.10 Comparative Overview of Clock Frequency Accuracy Measurement Circuits

Item	RX210 (CAC)	RX660 (CAC)
Measurement target clocks	The frequency of the following clocks can be measured. • Clock output from main clock oscillator (main clock) • Clock output from sub-clock oscillator (sub-clock) • Clock output from high-speed on-chip oscillator (HOCO clock) • Clock output from low-speed on-chip oscillator (LOCO clock) • Clock output from IWDT-dedicated on-chip oscillator (IWDTCLK clock)	The frequency of the following clocks can be measured. • Main clock • Sub-clock • HOCO clock • LOCO clock • IWDT-dedicated clock (IWDTCLK) • Peripheral module clock B (PCLKB)
Measurement reference clocks	—	• External clock input on CACREF pin • Main clock • Sub-clock • HOCO clock • LOCO clock • IWDT-dedicated clock (IWDTCLK) • Peripheral module clock B (PCLKB)
Selectable function	Digital filter function	Digital filter function
Interrupt sources	• Measurement end interrupt • Frequency error interrupt • Overflow interrupt	• Measurement end interrupt • Frequency error interrupt • Overflow interrupt
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Table 2.11 Comparison of Clock Frequency Accuracy Measurement Circuit Registers

Register	Bit	RX210 (CAC)	RX660 (CAC)
CACR1	FMCS[2:0]	Frequency measurement clock select bits [Chip version A] b3 b1 0 0 1: Clock output from sub-clock oscillator 0 1 0: Clock output from high-speed on-chip oscillator 0 1 1: Clock output from low-speed on-chip oscillator 1 0 0: Clock output from IWDT-dedicated on-chip oscillator [Chip versions B and C] b3 b1 0 0 0: Clock output from main clock oscillator 0 0 1: Clock output from sub-clock oscillator 0 1 0: Clock output from high-speed on-chip oscillator 0 1 1: Clock output from low-speed on-chip oscillator 1 0 0: Clock output from IWDT-dedicated on-chip oscillator Settings other than the above are prohibited.	Measurement target clock select bits b3 b1 0 0 0: Main clock 0 0 1: Sub-clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock B (PCLKB) Settings other than the above are prohibited.

Register	Bit	RX210 (CAC)	RX660 (CAC)
CACR2	RSCS[2:0]	Reference signal generation clock select bits [Chip version A] b3 b1 0 0 1: Clock output from sub-clock oscillator 0 1 0: Clock output from high-speed on-chip oscillator 0 1 1: Clock output from low-speed on-chip oscillator 1 0 0: Clock output from IWDT-dedicated on-chip oscillator [Chip versions B and C] b3 b1 0 0 0: Clock output from main clock oscillator 0 0 1: Clock output from sub-clock oscillator 0 1 0: Clock output from high-speed on-chip oscillator 0 1 1: Clock output from low-speed on-chip oscillator 1 0 0: Clock output from IWDT-dedicated on-chip oscillator Settings other than the above are prohibited.	Measurement reference clock select bits b3 b1 0 0 0: Main clock 0 0 1: Sub-clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock B (PCLKB) Settings other than the above are prohibited.

2.8 Low Power Consumption

Table 2.12 is a comparative overview of the low power consumption functions, Table 2.13 is a comparison of procedures for entering and exiting low power consumption modes and operating states in each mode, and Table 2.14 is a comparison of low power consumption registers.

Table 2.12 Comparative Overview of Low Power Consumption Functions

Item	RX210	RX660
Reducing power consumption by switching clock signals	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKB), S12AD clock (PCLKD), external bus clock (BCLK), and FlashIF clock (FCLK).	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, and PCLKD), external bus clock (BCLK), and flash interface clock (FCLK).
BCLK output control function	BCLK output or high-level output can be selected.	BCLK output or high-level output can be selected.
Module stop function	Each peripheral module can be stopped independently by the module stop control register.	Each peripheral module can be stopped independently by the module stop control register.
Function for transition to low power consumption mode	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.
Low power consumption modes	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode
Function for lower operating power consumption	Power consumption can be reduced in normal operation, sleep mode, and all-module clock stop mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. [Chip versions A and C] • Five operating power control modes are available — High-speed operating mode — Middle-speed operating mode 1A — Middle-speed operating mode 1B — Low-speed operating mode 1 — Low-speed operating mode 2 [Chip version B] • Seven operating power control modes are available — High-speed operating mode — Middle-speed operating mode 1A — Middle-speed operating mode 1B — Middle-speed operating mode 2A — Middle-speed operating mode 2B — Low-speed operating mode 1 — Low-speed operating mode 2	—

Table 2.13 Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX210	RX660
Sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM0 (RX210) (0000 0000h to 0000 FFFFh) RAM1 (RX210) (0001 0000h to 0001 7FFFh) RAM (RX660)	Operation possible (retained)	Operation possible (retained)
	Flash memory	Operation	Operation
	Watchdog timer (WDT)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Port output enable	—	Operation possible
	Remote control signal receiver (REMC)	—	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	8-bit timer (unit 0, unit1) (TMR)	Operation possible	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Operation possible	Operation possible
	I/O ports	Operation	Operation
All-module clock stop mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM0 (RX210) (0000 0000h to 0000 FFFFh) RAM1 (RX210) (0001 0000h to 0001 7FFFh) RAM (RX660)	Operation possible (retained)	Operation possible (retained)
	Flash memory	Stopped (retained)	Stopped (retained)

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX210	RX660
All-module clock stop mode	Watchdog timer (WDT)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Port output enable	—	Operation possible
	Remote control signal receiver (REMC)	—	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	8-bit timer (unit 0, unit1) (TMR)	Operation possible	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained
Software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Stopped	Stopped
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Stopped
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Stopped	Stopped
	CPU	Stopped (retained)	Stopped (retained)
	RAM0 (RX210) (0000 0000h to 0000 FFFFh) RAM1 (RX210) (0001 0000h to 0001 7FFFh) RAM (RX660)	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	Watchdog timer (WDT)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Port output enable	—	Stopped (retained)
	Remote control signal receiver (REMC)	—	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	8-bit timer (unit 0, unit1) (TMR)	Stopped (retained)	Stopped (retained)
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained
Deep software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Stopped	Stopped
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Stopped
	IWDT-dedicated on-chip oscillator	Stopped (undefined)	Stopped (undefined)

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX210	RX660
Deep software standby mode	PLL	Stopped	Stopped
	CPU	Stopped (undefined)	Stopped (undefined)
	RAM0 (RX210) (0000 0000h to 0000 FFFFh) RAM1 (RX210) (0001 0000h to 0001 7FFFh) RAM (RX660)	Stopped (undefined)	Stopped (undefined)
	Flash memory	Stopped (retained)	Stopped (retained)
	Watchdog timer (WDT)	Stopped (undefined)	Stopped (undefined)
	Independent watchdog timer (IWDT)	Stopped (undefined)	Stopped (undefined)
	Port output enable	—	Stopped (undefined)
	Remote control signal receiver (REMC)	—	Stopped (undefined)
	Realtime clock (RTC)	Operation possible	Operation possible
	8-bit timer (unit 0, unit1) (TMR)	Stopped (undefined)	Stopped (undefined)
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped	Stopped (undefined)
	I/O ports	Retained	Retained

Note: “Operation possible” means that whether the state is operating or stopped is controlled by the control register setting.
“Stopped (retained)” means that internal register values are retained and internal operations are suspended.
“Stopped (undefined)” means that internal register values are undefined and power is not supplied to the internal circuit.

Table 2.14 Comparison of Low Power Consumption Registers

Register	Bit	RX210	RX660
MSTPCRA	MSTPA0	—	Compare match timer W (unit 1) module stop bit
	MSTPA1	—	Compare match timer W (unit 0) module stop bit
	MSTPA9	Multifunction timer pulse unit module stop bit Target module: MTU0 to MTU5 0: Release from the module-stop state. 1: Transition to the module-stop state.	Multifunction timer pulse unit 3 module stop bit Target module: MTU3 0: Release from the module-stop state. 1: Transition to the module-stop state.
	MSTPA13	16-bit timer pulse unit module stop bit	—
	MSTPA19	D/A converter module stop bit	12-bit D/A converter module stop bit
MSTPCRB	MSTPB8	Temperature sensor module stop bit	—
	MSTPB10	Comparator B module stop bit	Comparator C module stop bit
MSTPCRC	MSTPC0	RAM0 module stop bit Target module: RAM0 (0000 0000h to 0000 FFFFh)	RAM module stop bit Target module: RAM (0000 0000h to 0001 FFFFh)
	MSTPC1	RAM1 module stop bit	—
	MSTPC17	—	I^2C bus interface 2 module stop bit

Register	Bit	RX210	RX660
MSTPCRD	—	—	Module stop control register D
OPCCR	—	Operating power control register	—
RSTCKCR	RSTCKSEL [2:0]	Sleep mode return clock source select bits [Chip version A] b2 b0 0 0 1: HOCO [Chip versions B and C] b2 b0 0 0 1: HOCO is selected. 0 1 0: Main clock oscillator is selected. Settings other than above are prohibited while the RSTCKEN bit is set to 1.	Sleep mode return clock source select bits b2 b0 0 0 1: HOCO is selected. 0 1 0: Main clock oscillator is selected. Settings other than above are prohibited while the RSTCKEN bit is set to 1.
MOSCWTCR	—	Main clock oscillator wait control register	—
SOSCWTCR	—	Sub-clock oscillator wait control register	—
PLLWTCR	—	PLL wait control register	—
HOCOWTCR2	—	HOCO wait control register 2	—
DPSBYCR	DEEPCUT1	Deep cut bit	—
DPSIER1	—	—	Deep standby interrupt enable register 1
DPSIER2	DRIICDIE	SDA-DS deep standby cancel signal enable bit	—
	DRIICCIE	SCL-DS deep standby cancel signal enable bit	—
DPSIFR1	—	—	Deep standby interrupt flag register 1
DPSIFR2	DRIICDIF	SDA-DS deep standby cancel flag	—
	DRIICCIF	SCL-DS deep standby cancel flag	—
DPSIEGR1	—	—	Deep standby interrupt edge register 1
DPSIEGR2	DRIICDEG	SDA-DS edge select bit	—
—	DRIICCEG	SCL-DS edge select bit	—
FHSSBYCR	—	Flash HOCO software standby control register	—

2.9 Register Write Protection Function

Table 2.15 is a comparative overview of the register write protection functions, and Table 2.16 is a comparison of register write protection function registers.

Table 2.15 Comparative Overview of Register Write Protection Functions

Item	RX210	RX660
PRC0 bit	Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, HOCOCR2	Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, FLLCR1, FLLCR2, OSTDCR, OSTDSR
PRC1 bit	• Register related to the operating modes: SYSCR0, SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR, RSTCKCR, MOSCWTCR, SOSCWTCR, PLLWTCR, DPSBYCR, DPSIER0, DPSIER2, DPSIFR0, DPSIFR2, DPSIEGR0, DPSIEGR2, FHSSBYCR, HOCOWTCR2 • Registers related to the clock generation circuit: MOFCR, HOCOPCR, PLLPCR (Chip version B) • Software reset register: SWRR	• Register related to the operating modes: SYSCR0, SYSCR1, VOLSR • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, RSTCKCR, DPSBYCR, DPSIER0 to DPSIER2, DPSIFR0 to DPSIFR2, DPSIEGR0 to DPSIEGR2 • Registers related to the clock generation circuit: MOSCWTCR, SOSCWTCR, MOFCR, SOFCR, HOCOPCR • Software reset register: SWRR
PRC2 bit	VRCR register	—
PRC3 bit	• Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	• Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

Table 2.16 Comparison of Register Write Protection Function Registers

Register	Bit	RX210	RX660
PRCR	PRC2	Protect bit 2	—

2.10 Exception Handling

Table 2.17 is a comparative overview of exception handling, Table 2.18 is a comparative listing of vectors, and Table 2.19 is a comparative listing of instructions for returning from exception handling routines.

Table 2.17 Comparative Overview of Exception Handling

Item	RX210	RX660
Exception events	• Undefined instruction exception • Privileged instruction exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap	• Undefined instruction exception • Privileged instruction exception • Access exception • Single-precision floating-point exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap

Table 2.18 Comparative Listing of Vectors

Item		RX210	RX660
Undefined instruction exception		Fixed vector table	Exception vector table (EXTB)
Privileged instruction exception		Fixed vector table	Exception vector table (EXTB)
Access exception		—	Exception vector table (EXTB)
Floating-point exception		—	Exception vector table (EXTB)
Reset		Fixed vector table	Exception vector table (EXTB)
Non-maskable interrupt		Fixed vector table	Exception vector table (EXTB)
Interrupt	Fast interrupt	FINTV	FINTV
	Other than fast interrupt	Relocatable vector table (INTB)	Interrupt vector table (INTB)
Unconditional trap		Relocatable vector table (INTB)	Interrupt vector table (INTB)

Table 2.19 Comparative Listing of Instructions for Returning from Exception Handling Routines

Item		RX210	RX660
Undefined instruction exception		RTE	RTE
Privileged instruction exception		RTE	RTE
Access exception		—	RTE
Floating-point exception		—	RTE
Reset		Return not possible	Return not possible
Non-maskable interrupt		Return not possible	Prohibited
Interrupt	Fast interrupt	RTFI	RTFI
	Other than fast interrupt	RTE	RTE
Unconditional trap		RTE	RTE

2.11 Interrupt Controller

Table 2.20 is a comparative overview of the interrupt controllers, and Table 2.21 is a comparison of interrupt controller registers.

Table 2.20 Comparative Overview of Interrupt Controllers

Item		RX210 (ICUb)	RX660 (ICUF)
Interrupts	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection The detection method is fixed for each connected peripheral module source.	• Interrupts from peripheral modules • Interrupt detection method: Edge detection/level detection (fixed for each interrupt source) • Group interrupt: Multiple interrupt sources are grouped together and treated as a single interrupt source.*1 — Group IE0 interrupt: Interrupt sources of coprocessors that use ICLK as the operating clock (edge detection) — Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) — Group BL0/BL1/BL2 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) — Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt B: Any of the interrupt sources for peripheral modules that use PCLKB as the operating clock can be assigned to interrupt vector numbers 128 to 207. • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.

Item		RX210 (ICUb)	RX660 (ICUF)
Interrupts	External pin interrupts	• Interrupts from pins IRQ0 to IRQ7 • Number of sources: 8 • Interrupt detection: Ability to set as source detection of low level, falling edge, rising edge, or rising and falling edges • Digital filter function: Supported	• Interrupts by input signals on IRQi pins (i = 0 to 15) • Interrupt detection: Ability to set as source detection of low level, falling edge, rising edge, or rising and falling edges • A digital filter can be used to remove noise.
	Software interrupts	• Interrupt generated by writing to a register • Number of sources: 1	• An interrupt request can be generated by writing to a register. • Number of sources: 2
	Event link interrupts	An ELSR18I or ELSR19I interrupt can be generated by an ELC event.	—
	Interrupt priority	Specified by registers.	Setting of priority level in interrupt source priority register r (IPRr) (r = 000 to 255)
	Fast interrupt function	Faster interrupt handling by the CPU can be specified for a single interrupt source only.	It is possible to reduce the CPU's interrupt response time. This setting can be used for one interrupt source only.
	DTC and DMAC control	The DTC and DMAC can be activated by an interrupt source.	The DTC and DMAC can be activated by an interrupt source.
Non-maskable interrupts	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection: Falling edge or rising edge • Digital filter function: Supported	• Interrupt by the input signal on the NMI pin • Interrupt detection: Falling edge or rising edge • Digital filter function: Supported
	Oscillation stop detection interrupt	Interrupt on detection of oscillation having stopped	Interrupt at detection of main clock oscillation stop
	WDT underflow/ refresh error interrupt	Interrupt on an underflow of the down counter or occurrence of a refresh error	Interrupt occurs when the watchdog timer underflows or a refresh error occurs.
	IWDT underflow/ refresh error interrupt	Interrupt on an underflow of the down counter or occurrence of a refresh error	Interrupt occurs when the independent watchdog timer underflows or a refresh error occurs.
	Voltage monitoring 1 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)	Interrupt from voltage detection circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)	Interrupt from voltage detection circuit 2 (LVD2)
	RAM error interrupt	—	Interrupt occurs when a parity check error is detected in the RAM.

Item		RX210 (ICUb)	RX660 (ICUF)
Return from low power consumption state	Sleep mode	Return is initiated by a non-maskable interrupt or any other interrupt source.	Exit sleep mode by any interrupt source.
	All-module clock stop mode	Return is initiated by non-maskable interrupts, IRQ0 to IRQ7 interrupts, TMR interrupts, or RTC alarm/ periodic interrupts.	Exit all-module clock stop mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection interrupt, RTC alarm, RTC period, IWDT, REMC interrupt, or software configurable interrupt 146 to 157).
	Software standby mode	Return is initiated by a non-maskable interrupt, interrupt IRQ0 to IRQ7, or an RTC alarm/periodic interrupt.	Exit software standby mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, RTC alarm, RTC period, IWDT, or REMC interrupt).
	Deep software standby mode	—	Exit deep software standby mode by NMI pin interrupt, any among a subset of external pin interrupts, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, RTC alarm, or RTC period).

Note: 1. Groups to which no interrupt source is assigned are reserved. There are no registers corresponding to such groups.

Table 2.21 Comparison of Interrupt Controller Registers

Register	Bit	RX210 (ICUb)	RX660 (ICUF)
IRn	—	Interrupt request register n (n = 016 to 253)	Interrupt request register n (n = 016 to 255)
IPRn	—	Interrupt source priority register n (n = 000 to 250)	Interrupt source priority register n (n = 000 to 255)
SWINTR2R	—	—	Software interrupt 2 generation register
DTCERn	DTCE	DTC activation enable bit (n = 027 to 252) 0: DTC activation is disabled 1: DTC activation is enabled	DTC transfer request enable bit (n = 026 to 255) 0: Set to an interrupt source to the CPU, or to the DMAC activation source. 1: Set to the DTC activation source.
IRQCRi	—	IRQ control register i (i = 0 to 7)	IRQ control register i (i = 0 to 15)
IRQFLTE1	—	—	IRQ pin digital filter enable register 1
IRQFLTC1	—	—	IRQ pin digital filter setting register 1
NMISR	RAMST	—	RAM error interrupt status flag
NMIER	RAMEN	—	RAM error interrupt enable bit
GRPBL0 GRPBL1 GRPBL2	—	—	Group BL0/BL1/BL2 interrupt request register
GRPAL0	—	—	Group AL0 interrupt request register
GENBL0 GENBL1 GENBL2	—	—	Group BL0/BL1/BL2 interrupt enable register
GENAL0	—	—	Group AL0 interrupt enable register
PIBRk	—	—	Software configurable interrupt B request register k (k = 0h, 1h, 5h, 6h, 8h to Ah, Ch, Dh)
PIARk	—	—	Software configurable interrupt A request register k (k = 0h to 5h, Bh, Ch)
SLIBXRn	—	—	Software configurable interrupt B source select register Xn (n = 128 to 143)
SLIBRn	—	—	Software configurable interrupt B source select register n (n = 144 to 207)
SLIARn	—	—	Software configurable interrupt A source select register n (n = 208 to 255)
SLIPRCR	—	—	Software configurable interrupt source select register Write protection register

2.12 Buses

Table 2.22 is a comparative overview of the buses, and Table 2.23 is a comparison of bus registers.

Table 2.22 Comparative Overview of Buses

Bus Type		RX210	RX660
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	Connected to RAM	Connected to RAM
	Memory bus 2	Connected to ROM	Connected to code flash memory
Internal main buses	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DTC and DMAC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the DTC and DMAC • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (TFU, DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral bus 1) • Operates in synchronization with the peripheral-module clock (PCLKB, PCLKD*1)	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 3	—	• Connected to peripheral modules (DOC, REMC, CANFD, CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)

Bus Type		RX210	RX660
Internal peripheral buses	Internal peripheral bus 4	—	• Connected to peripheral modules (MTU, RSPI, SCIi) • Operates in synchronization with the peripheral-module clock (PCLKA)
	Internal peripheral bus 5	—	• Connected to peripheral modules (RSCI, CANFD) • Operates in synchronization with the peripheral-module clock (PCLKA)
	Internal peripheral bus 6	• Connected to ROM (P/E) and E2 DataFlash • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to code flash memory (in P/E) and data flash memory • Operates in synchronization with the FlashIF clock (FCLK)
External bus	CS area	• Connected to the external devices • Operates in synchronization with the external-bus clock (BCLK)	• Connected to the external devices • Operates in synchronization with the external-bus clock (BCLK)

Note: 1. The peripheral module clock (PCLKD) is the operating clock of the S12AD.

Table 2.23 Comparison of Bus Registers

Register	Bit	RX210	RX660
BUSPRI	BPHB[1:0]	—	Internal peripheral bus 4 and 5 priority control bits

2.13 DMA Controller

Table 2.24 is a comparative overview of the DMA controllers, and Table 2.25 is a comparison of DMA controller registers.

Table 2.24 Comparative Overview of DMA Controllers

Item		RX210 (DMACA)	RX660 (DMACAa)
Number of channels		4 (DMACm (m = 0 to 3))	8 (DMACm (m = 0 to 7))
Transfer space		512 MB (00000000h to 0FFFFFFFh and F0000000h to FFFFFFFFh, excluding reserved areas)	512 MB (00000000h to 0FFFFFFFh and F0000000h to FFFFFFFFh, excluding reserved areas)
Maximum transfer volume		1 M data units (maximum number of transfers in block transfer mode: 1,024 data units × 1,024 blocks)	64 M data units (maximum number of transfers in block transfer mode: 1,024 data units × 65,536 blocks)
DMA request sources		• Activation source selectable for each channel • Software trigger • Interrupt requests from peripheral modules or trigger input to external interrupt input pins	• Activation source selectable for each channel • Software trigger • Interrupt requests from peripheral modules or trigger input to external interrupt input pins
Channel priority		Channel 0 > channel 1 > channel 2 > channel 3 (channel 0: highest)	Channel 0 > channel 1 > channel 2 > channel 3 ... > channel 7 (channel 0: highest)
Transfer data	Single data unit	Bit length: 8, 16, 32 bits	Bit length: 8, 16, 32 bits
	Block size	Number of data units: 1 to 1,024 data units	Number of data units: 1 to 1,024 data units
Transfer modes	Normal transfer mode	• Transfer of one data unit per DMA transfer request • Setting in which total number of data transfers is not specified (free running mode) is available.	• Transfer of one data unit per DMA transfer request • Setting in which total number of data transfers is not specified (free running mode) is available.
	Repeat transfer mode	• Transfer of one data unit per DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. • Maximum settable repeat size: 1,024 data units	• Transfer of one data unit per DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. • Maximum settable repeat size: 1,024 data units
	Block transfer mode	• Transfer of one data block per DMA transfer request • Maximum settable block size: 1,024 data units	• Transfer of one data block per DMA transfer request • Maximum settable block size: 1,024 data units
Selective functions	Extended repeat area function	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed • Area of 2 bytes to 128 MB separately settable as extended repeat area for transfer source or destination	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed • Area of 2 bytes to 128 MB separately settable as extended repeat area for transfer source or destination

Item		RX210 (DMACA)	RX660 (DMACAa)
Interrupt requests	Transfer end interrupt	Generated on completion of transferring data volume specified by the transfer counter.	• Generated when the specified number of transfers is completed in normal transfer mode • Generated when the specified repeat count of transfers is completed in repeat transfer mode • Generated when the specified block count of transfers is completed in block transfer mode
	Transfer escape end interrupt	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.
Event link function		Event link request generated after one data transfer (or after one block transfer in case of block transfer operation).	Event link request generated after one data transfer (or after one block transfer in case of block transfer operation).
Low power consumption function		Ability to specify module stop state	Ability to specify module stop state

Table 2.25 Comparison of DMA Controller Registers

Register	Bit	RX210 (DMACA)	RX660 (DMACAa)
DMCRB	—	DMA block transfer count register (b9 to b0)	DMA block transfer count register (b15 to b0)
DMIST	—	—	DMAC74 interrupt status monitor register

2.14 Data Transfer Controller

Table 2.26 is a comparative overview of the data transfer controllers, and Table 2.27 is a comparison of data transfer controller registers.

Table 2.26 Comparative Overview of Data Transfer Controllers

Item	RX210 (DTCa)	RX660 (DTCb)
Number of transfer channels	Equal to number of all interrupt sources that can start a DTC transfer.	Equal to number of all interrupt sources that can start a DTC transfer.
Transfer modes	• Normal transfer mode — A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address returns to the transfer start address when the number of data transfers equals the repeat size. — The maximum repeat size is 256 data units. • Block transfer mode — A single activation leads to the transfer of a single block of data. — The maximum block size is 256 data units.	• Normal transfer mode — A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address returns to the transfer start address when the number of data transfers equals the repeat size. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, or 1,024 bytes. • Block transfer mode — A single activation leads to the transfer of a single block of data. — The maximum block size is 256 × 32 bits = 1,024 bytes.
Chain transfer function	• Multiple data transfer types can be executed sequentially in response to a single transfer request. • Either “performed only when the transfer counter reaches 0” or “every time” can be selected.	• Multiple data transfer types can be executed sequentially in response to a single transfer request. • Either “performed only when the transfer counter reaches 0” or “every time” can be selected.
Sequence transfer	—	A complex series of transfers can be registered as a sequence. Any sequence can be selected by the transfer data and executed. • Only one sequence transfer trigger source can be selected at a time. • Up to 256 sequences can correspond to a single trigger source. • The data that is initially transferred in response to a transfer request determines the sequence. • The entire sequence can be executed on a single request, or the sequence can be suspended in the middle and resumed on the next transfer request (sequence division).

Item	RX210 (DTCa)	RX660 (DTCb)
Transfer space	• 16 MB in short-address mode (within 0000 0000h to 007F FFFFh or FF80 0000h to FFFF FFFFh, excluding reserved areas) • 4 GB in full-address mode (within 0000 0000h to FFFF FFFFh, excluding reserved areas)	• 16 MB in short-address mode (within 0000 0000h to 007F FFFFh or FF80 0000h to FFFF FFFFh, excluding reserved areas) • 4 GB in full-address mode (within 0000 0000h to FFFF FFFFh, excluding reserved areas)
Data transfer units	• Single data unit: 8 bits, 16 bits, or 32 bits • Single block size: 1 to 256 data units	• Single data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data units
CPU interrupt requests	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.
Event link function	An event link request is generated after one data transfer (for block transfers, after one block).	An event link request is generated after one data transfer (for block transfers, after one block).
Read skip	Transfer data read skip can be specified.	Reading of the transfer information can be skipped when the same transfer is repeated.
Write-back skip	Writeback skip can be enabled when “fixed” is selected for the transfer source address and/or transfer destination address.	Write-back of transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.
Write-back disable	—	Ability to disable write-back of transfer information
Displacement addition	—	Ability to add displacement to the transfer source address (selectable by each transfer information)
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Table 2.27 Comparison of Data Transfer Controller Registers

Register	Bit	RX210 (DTCa)	RX660 (DTCb)
MRA	WBDIS	—	Write-back disable bit*1
MRB	SQEND	—	Sequence transfer end bit
	INDX	—	Index table reference bit
MRC	—	—	DTC mode register C
DTCIBR	—	—	DTC index table base register
DTCOR	—	—	DTC operation register
DTCSQE	—	—	DTC sequence transfer enable register
DTCDISP	—	—	DTC address displacement register

Note: 1. Transfer information is usually allocated to a RAM area, but it can be allocated to a ROM area by setting the MRA.WBDIS bit to 1 (no write-back).

2.15 Event Link Controller

Table 2.28 is a comparative overview of the event link controllers, Table 2.29 is a comparison of event link controller registers, Table 2.30 lists correspondences between ELSRn registers and peripheral modules, and Table 2.31 shows correspondences between values set in ELSRn.ELS[7:0] and event signal names and numbers.

Table 2.28 Comparative Overview of Event Link Controllers

Item	RX210 (ELC)	RX660 (ELC)
Event link function	• 59 types of event signals can be directly connected to peripheral modules. • The operation of timer modules at event input is selectable. • Event link operation is possible for port B and port E. — Single port: Event link operation can be enabled for a single specified port. — Port group: Event link operation can be enabled for a group of specified bits within an 8-bit port.	• 83 types of event signals can be directly connected to peripheral modules. • The operation of peripheral timer modules at event signal input is selectable. • Event link operation is possible for port B and port E. — Single port: Event link operation can be enabled for a single specified port. — Port group: Event link operation can be enabled for multiple specified ports within a group of up to eight ports.
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Table 2.29 Comparison of Event Link Controller Registers

Register	Bit	RX210 (ELC)	RX660 (ELC)
ELSRn	—	Event link setting register n (n = 1 to 4, 7, 10, 12, 15, 16, 18 to 29)	Event link setting register n (n = 0, 3, 4, 7, 10 to 13, 15, 16, 18 to 28, 30, 31, 32, 56)
	ELS[7:0]	Event link select bits 00000000: Event output to the corresponding peripheral module is disabled. 00000001 to 01101001: Specifies the number of the event signal to be linked. Settings other than the above are prohibited.	Event link select bits 00h: Event signal output to the corresponding peripheral module is disabled. 01h to F1h: Specifies the number of the event signal to be linked. Settings other than the above are prohibited.
ELOPA	MTU0MD [1:0]	—	MTU0 operation select bits
	MTU1MD [1:0]	MTU1 operation select bits	—
	MTU2MD [1:0]	MTU2 operation select bits	—
ELOPD	TMR1MD [1:0]	—	TMR1 operation select bits
	TMR3MD [1:0]	—	TMR3 operation select bits
ELOPE	—	—	Event link option setting register E

Table 2.30 Correspondence between ELSRn Registers and Peripheral Modules

Register	RX210 (ELC)	RX660 (ELC)
ELSR0	—	MTU0
ELSR1	MTU1	—
ELSR2	MTU2	—
ELSR3	MTU3	MTU3
ELSR4	MTU4	MTU4
ELSR7	CMT1	CMT1
ELSR10	TMR0	TMR0
ELSR11	—	TMR1
ELSR12	TMR2	TMR2
ELSR13	—	TMR3
ELSR15	12-bit A/D converter	S12AD (ELCTRG00N)
ELSR16	DA0	DA0
ELSR18	Interrupt 1	ICU (interrupt 1)
ELSR19	Interrupt 2	ICU (interrupt 2)
ELSR20	Output port group 1	Output port group 1
ELSR21	Output port group 2	Output port group 2
ELSR22	Input port group 1	Input port group 1
ELSR23	Input port group 2	Input port group 2
ELSR24	Single port 0	Single port 0
ELSR25	Single port 1	Single port 1
ELSR26	Single port 2	Single port 2
ELSR27	Single port 3	Single port 3
ELSR28	Clock source switching to LOCO	Clock source switching to LOCO
ELSR29	POE	—
ELSR30	—	MTU6
ELSR31	—	MTU7
ELSR32	—	MTU8
ELSR56	—	S12AD (ELCTRG01N)

Table 2.31 Correspondence between Values Set in ELSRn.ELS[7:0] Bits and Event Signal Names and Numbers

Value of ELS[7:0] Bits	RX210 (ELC)	RX660 (ELC)
01h	—	MTU0 compare match 0A
02h	—	MTU0 compare match 0B
03h	—	MTU0 compare match 0C
04h	—	MTU0 compare match 0D
05h	—	MTU0 compare match 0E
06h	—	MTU0 compare match 0F
07h	—	MTU0 overflow
08h	MTU1 compare match 1A	—
09h	MTU1 compare match 1B	—
0Ah	MTU1 overflow	—
0Bh	MTU1 underflow	—
0Ch	MTU2 compare match 2A	—
0Dh	MTU2 compare match 2B	—
0Eh	MTU2 overflow	—
0Fh	MTU2 underflow	—
10h	MTU3 compare match 3A	MTU3 compare match 3A

Value of ELS[7:0] Bits	RX210 (ELC)	RX660 (ELC)
11h	MTU3 compare match 3B	MTU3 compare match 3B
12h	MTU3 compare match 3C	MTU3 compare match 3C
13h	MTU3 compare match 3D	MTU3 compare match 3D
14h	MTU3 overflow	MTU3 overflow
15h	MTU4 compare match 4A	MTU4 compare match 4A
16h	MTU4 compare match 4B	MTU4 compare match 4B
17h	MTU4 compare match 4C	MTU4 compare match 4C
18h	MTU4 compare match 4D	MTU4 compare match 4D
19h	MTU4 overflow	MTU4 overflow
1Ah	MTU4 underflow	MTU4 underflow
1Eh	—	MTU6 compare match 6A
1Fh	CMT1 compare match 1	MTU6 compare match 6B
20h	—	MTU6 compare match 6C
21h	—	MTU6 compare match 6D
22h	TMR0 compare match A0	MTU6 overflow
23h	TMR0 compare match B0	MTU7 compare match 7A
24h	TMR0 overflow	MTU7 compare match 7B
25h	—	MTU7 compare match 7C
26h	—	MTU7 compare match 7D
27h	—	MTU7 overflow
28h	TMR2 compare match A2	MTU7 underflow
29h	TMR2 compare match B2	MTU8 compare match 8A
2Ah	TMR2 overflow	MTU8 compare match 8B
2Bh	—	MTU8 compare match 8C
2Ch	—	MTU8 compare match 8D
2Dh	—	MTU8 overflow
2Eh	RTC cycle	—
31h	IWDT underflow or refresh error	—
37h	—	CMT1 compare match 1
3Ah	SCI5 error (receive error or error signal detection)	—
3Bh	SCI5 receive data full	—
3Ch	SCI5 transmit data empty	TMR0 compare match A0
3Dh	SCI5 transmit end	TMR0 compare match B0
3Eh	—	TMR0 overflow
3Fh	—	TMR1 compare match A1
40h	—	TMR1 compare match B1
41h	—	TMR1 overflow
42h	—	TMR2 compare match A2
43h	—	TMR2 compare match B2
44h	—	TMR2 overflow
45h	—	TMR3 compare match A3
46h	—	TMR3 compare match B3
47h	—	TMR3 overflow
4Eh	RIIC0 communication error or event generation	—
4Fh	RIIC0 receive data full	—
50h	RIIC0 transmit data empty	—
51h	RIIC0 transmit end	—

Value of ELS[7:0] Bits	RX210 (ELC)	RX660 (ELC)
52h	RSPI0 error (mode fault, overrun, or parity error)	—
53h	RSPI0 idle	—
54h	RSPI0 receive data full	—
55h	RSPI0 transmit data empty	—
56h	RSPI0 transmit end signal (except during clock synchronous operation in slave mode)	—
58h	A/D conversion end signal of 12-bit A/D converter	—
59h	Comparator B0 comparison result change signal	—
5Ah	Comparator B0, B1 common comparison result change signal	—
5Bh	LVD1 voltage detection	—
5Ch	LVD2 voltage detection	—
5Dh	DMAC0 transfer end	—
5Eh	DMAC1 transfer end	—
5Fh	DMAC2 transfer end	—
60h	DMAC3 transfer end	—
61h	DTC transfer end	—
62h	Oscillation stop detection of clock generation circuit	—
63h	Input edge detection of input port group 1	—
64h	Input edge detection of input port group 2	
65h	Input edge detection of single input port 0	—
66h	Input edge detection of single input port 1	—
67h	Input edge detection of single input port 2	
68h	Input edge detection of single input port 3	
69h	Software event	—
ACh	—	RTC periodic event (select 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, 1, or 2 seconds)
AFh	—	IWDT underflow or refresh error
B8h	—	SCI5 error (receive error or error signal detection)
B9h	—	SCI5 receive data full
BAh	—	SCI5 transmit data empty
BBh	—	SCI5 transmit end
CCh	—	RIIC0 communication error or event generation
CDh	—	RIIC0 receive data full
CEh	—	RIIC0 transmit data empty
CFh	—	RIIC0 transmit end
D0h	—	RSPI0 error (mode fault, overrun, underrun, or parity error)
D1h	—	RSPI0 idle
D2h	—	RSPI0 receive buffer full
D3h	—	RSPI0 transmit buffer empty
D4h	—	RSPI0 transmit end
D6h	—	S12AD A/D conversion end

Value of ELS[7:0] Bits	RX210 (ELC)	RX660 (ELC)
DCh	—	Comparator C0 comparison result change
DDh	—	Comparator C1 comparison result change
DEh	—	Comparator C2 comparison result change
DFh	—	Comparator C3 comparison result change
E2h	—	LVD1 voltage detection
E3h	—	LVD2 voltage detection
E4h	—	DMAC0 transfer end
E5h	—	DMAC1 transfer end
E6h	—	DMAC2 transfer end
E7h	—	DMAC3 transfer end
E8h	—	DTC transfer end
E9h	—	Oscillation stop detection of clock generation circuit
EAh	—	Input edge detection of input port group 1
EBh	—	Input edge detection of input port group 2
ECh	—	Input edge detection of single input port 0
EDh	—	Input edge detection of single input port 1
EEh	—	Input edge detection of single input port 2
EFh	—	Input edge detection of single input port 3
F0h	—	Software event
F1h	—	DOC data operation condition met

2.16 I/O Ports

Table 2.32 to Table 2.36 are comparative overviews of the I/O ports, Table 2.37 is a comparison of I/O port functions, Table 2.38 is a comparison of driving ability switching on I/O ports, and Table 2.39 is a comparison of I/O port registers.

Table 2.32 Comparative Overview of I/O Ports (144-Pin)

Port Symbol	RX210 (145, 144-Pin)	RX660 (144-Pin)
PORT0	P00 to P03, P05, P07	P00 to P07
PORT1	P12 to P17	P12 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P56	P50 to P56
PORT6	P60 to P67	P60 to P67
PORT7	P70 to P77	P70 to P77
PORT8	P80 to P83, P86, P87	P80 to P83, P86, P87
PORT9	P90 to P93	P90 to P93
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7
PORTF	PF5	PF5 to PF7
PORTH	PH0 to PH3	PH0 to PH3, PH6*1, PH7*1
PORTJ	PJ1, PJ3, PJ5	PJ1, PJ3 to PJ7
PORTK	PK2 to PK5	PK2 to PK5
PORTL	PL0, PL1	PL0, PL1
PORTN	—	PN6, PN7*2

Notes: 1. PH6 and PH7 are not present on products provided with a sub-clock oscillator.
2. PN7 is not present on products provided with a JTAG.

Table 2.33 Comparative Overview of I/O Ports (100-Pin)

Port Symbol	RX210 (100-Pin)	RX660 (100-Pin)
PORT0	P03, P05, P07	P03*1 to P07
PORT1	P12 to P17	P12 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P55	P50 to P55
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7
PORTH	PH0 to PH3	PH0 to PH3, PH6*2, PH7*2
PORTJ	PJ1, PJ3	PJ1, PJ3, PJ6, PJ7
PORTN	—	PN6

Notes: 1. P03 is not present on products provided with a JTAG.
2. PH6 and PH7 are not present on products provided with a sub-clock oscillator.

Table 2.34 Comparative Overview of I/O Ports (80-Pin)

Port Symbol	RX210 (80-Pin)	RX660 (80-Pin)
PORT0	P03, P05, P07	P03 to P07
PORT1	P12 to P17	P12 to P17
PORT2	P20, P21, P26, P27	P20, P21, P26, P27
PORT3	P30 to P32, P34 to P37	P30 to P32, P34 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P54, P55	P54, P55
PORTA	PA0 to PA6	PA0 to PA6
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC2 to PC7	PC2 to PC7
PORTD	PD0 to PD2	PD0 to PD2
PORTE	PE0 to PE5	PE0 to PE5
PORTH	PH0 to PH3	PH0 to PH3, PH6*1, PH7*1
PORTJ	PJ1	PJ1, PJ6, PJ7
PORTN	—	PN6

Note: 1. PH6 and PH7 are not present on products provided with a sub-clock oscillator.

Table 2.35 Comparative Overview of I/O Ports (64-Pin)

Port Symbol	RX210 (69, 64-Pin)	RX660 (64-Pin)
PORT0	P03, P05	P03, P07
PORT1	P14 to P17	P14 to P17
PORT2	P26, P27	P26, P27
PORT3	P30 to P32, P35 to P37	P30 to P32, P35 to P37
PORT4	P40 to P44, P46	P40 to P47
PORT5	P54, P55	P54, P55
PORTA	PA0, PA1, PA3, PA4, PA6	PA0, PA1, PA3, PA4, PA6
PORTB	PB0, PB1, PB3, PB5 to PB7	PB0, PB1, PB3, PB5 to PB7
PORTC	PC2 to PC7	PC2 to PC7
PORTE	PE0 to PE5	PE0 to PE5
PORTH	PH0 to PH3	PH0 to PH3, PH6*1, PH7*1
PORTJ	—	PJ6, PJ7
PORTN	—	PN6

Note: 1. PH6 and PH7 are not present on products provided with a sub-clock oscillator.

Table 2.36 Comparative Overview of I/O Ports (48-Pin)

Port Symbol	RX210 (48-Pin)	RX660 (48-Pin)
PORT1	P14 to P17	P14 to P17
PORT2	P26, P27	P26, P27
PORT3	P30, P31, P35 to P37	P30, P31, P35 to P37
PORT4	P40 to P42, P46	P40 to P42, P45 to P47
PORTA	PA1, PA3, PA4, PA6	PA1, PA3, PA4, PA6
PORTB	PB0, PB1, PB3, PB5	PB0, PB1, PB3, PB5
PORTC	PC4 to PC7	PC4 to PC7
PORTE	PE1 to PE4	PE1 to PE4
PORTH	PH0 to PH3	PH0 to PH3
PORTJ	—	PJ6, PJ7
PORTN	—	PN6

Table 2.37 Comparison of I/O Port Functions

Item	Port Symbol	RX210	RX660
Input pull-up function	PORT0	P00 to P03, P05, P07	P00 to P07
	PORT1	P12 to P17	P12 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P56	P50 to P56
	PORT6	P60 to P67	P60 to P67
	PORT7	P70 to P77	P70 to P77
	PORT8	P80 to P83, P86, P87	P80 to P83, P86, P87
	PORT9	P90 to P93	P90 to P93
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	PD0 to PD7	PD0 to PD7
	PORTE	PE0 to PE7	PE0 to PE7
	PORTF	PF5	PF5 to PF7
	PORTH	PH0 to PH3	PH0 to PH3, PH6, PH7
	PORTJ	PJ1, PJ3, PJ5	PJ1, PJ3 to PJ7
	PORTK	PK2 to PK5	PK2 to PK5
	PORTL	PL0, PL1	PL0, PL1
	PORTN	—	PN6, PN7
Open drain output function	PORT0	P00 to P02	P00 to P07
	PORT1	P12 to P17	P12 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT4	—	P40 to P47
	PORT5	P50 to P52, P54	P50 to P56
	PORT6	P60, P61	P60 to P67
	PORT7	P70, P74 to P77	P70 to P77
	PORT8	P80 to P83	P80 to P83, P86, P87
	PORT9	P90 to P93	P90 to P93
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	—	PD0 to PD7
	PORTE	PE0 to PE7	PE0 to PE7
	PORTF	—	PF5 to PF7
	PORTH	—	PH0 to PH3, PH6, PH7
	PORTJ	—	PJ1, PJ3 to PJ7
	PORTK	PK2 to PK5	PK2 to PK5
	PORTL	—	PL0, PL1
	PORTN	—	PN6, PN7
5 V tolerant	PORT1	P12, P13, P16, P17	P12, P13, P16, P17

Table 2.38 Comparison of Driving Ability Switching on I/O Ports

Port Symbol	Driving Ability Switching	RX210	RX660
PORT0	Fixed to normal	P03, P05, P07	P03, P05 to P07
	Normal/high	P00 to P02	P00 to P02, P04
PORT1	Fixed to normal	—	—
PORT1	Normal/high	P12 to P17	P12 to P17
PORT2	Fixed to normal	—	—
	Normal/high	P20 to P27	P20 to P27
PORT3	Fixed to normal	—	P36, P37
	Normal/high	P30 to P34, P36, P37	P30 to P34
PORT4	Fixed to normal	P40 to P47	P40 to P47
	Normal/high	—	—
PORT5	Fixed to normal	—	—
	Normal/high	P50 to P56	P50 to P56
PORT6	Fixed to normal	P62 to P67	—
	Normal/high	P60, P61	P60 to P67
PORT7	Fixed to normal	P71 to P73	—
	Normal/high	P70, P74 to P77	P70 to P77
PORT8	Fixed to normal	—	—
	Normal/high	P80 to P87	P80 to P83, P86, P87
PORT9	Fixed to normal	—	—
	Normal/high	P90 to P93	P90 to P93
PORTA	Fixed to normal	—	—
	Normal/high	PA0 to PA7	PA0 to PA7
PORTB	Fixed to normal	—	—
	Normal/high	PB0 to PB7	PB0 to PB7
PORTC	Fixed to normal	—	—
	Normal/high	PC0 to PC7	PC0 to PC7
PORTD	Fixed to normal	—	—
	Normal/high	PD0 to PD7	PD0 to PD7
PORTE	Fixed to normal	—	—
	Normal/high	PE0 to PE7	PE0 to PE7
PORTF	Fixed to normal	PF5	—
	Normal/high	—	PF5 to PF7
PORTH	Fixed to normal	—	—
	Normal/high	PH0 to PH3	PH0 to PH3, PH6, PH7
PORTJ	Fixed to normal	PJ5	PJ6, PJ7
	Normal/high	PJ1, PJ3	PJ1, PJ3 to PJ5
PORTK	Fixed to normal	—	—
	Normal/high	PK2 to PK5	PK2 to PK5
PORTL	Fixed to normal	PL0, PL1	—
	Normal/high	—	PL0, PL1
PORTN	Fixed to normal	—	—
	Normal/high	—	PN6, PN7

Table 2.39 Comparison of I/O Port Registers

Register	Bit	RX210	RX660
PDR	B0 to B7	Pm0 to Pm7 I/O select bits (m = 0 to 9, A to F, H, J to L)	Pm0 to Pm7 I/O select bits (m = 0 to 9, A to F, H, J to L, N)
PODR	B0 to B7	Pm0 to Pm7 output data store bits (m = 0 to 9, A to F, H, J to L)	Pm0 to Pm7 output data store bits (m = 0 to 9, A to F, H, J to L, N)
PIDR	B0 to B7	Pm0 to Pm7 bits (m = 0 to 9, A to F, H, J to L)	Pm0 to Pm7 bits (m = 0 to 9, A to F, H, J to L, N)
PMR	B0 to B7	Pm0 to Pm7 pin mode control bits (m = 0 to 9, A to F, H, J to L)	Pm0 to Pm7 pin mode control bits (m = 0 to 9, A to F, H, J to L, N)
ODR0	B2, B3 (RX210) B2 (RX660)	Pm1 output type select bits (m = 0 to 3, 6 to 9, A to C, E, K) • P01, P21, P31, P51, P61, P81, P91, PA1, PB1, and PC1 b2 0: CMOS output 1: N-channel open-drain b3 This bit is read as 0. The write value should be 0. • PE1 b3 b2 0 0: CMOS output 0 1: N-channel open-drain 1 0: P-channel open-drain 1 1: Hi-Z	Pm1 output type select bits (m = 0 to 9, A to E, H, J to L) 0: CMOS output 1: N-channel open-drain
ODR1	B0, B2, B4, B6	Pm4, Pm5, Pm6, and Pm7 output type select bits (m = 1 to 3, 7, A to C, E, K)	Pm4, Pm5, Pm6, and Pm7 output type select bits (m = 0 to 8, A to F, H, J, K, N)
PCR	B0 to B7	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A to F, H, J to L)	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A to F, H, J to L, N)
DSCR	—	Drive capacity control register (m = 0 to 3, 5 to 9, A to E, H, J, K)	Drive capacity control register (m = 0 to 3, 5 to 9, A to F, H, J to L, N)

2.17 Multi-Function Pin Controller

Table 2.40 is a comparison of the assignments of multiplexed pins, and Table 2.41 to Table 2.58 are comparisons of multi-function pin controller registers.

In the following comparison of the assignments of multiplexed pins, **orange text** pins that exist on the RX210 Group only and **blue text** designates pins that exist on the RX660 Group only. A circle (○) indicates that a function is assigned, a cross (×) that the pin does not exist or that no function is assigned, and grayed out items mean that the function is not implemented.

Table 2.40 Comparison of Multiplexed Pin Assignments

Module/ Function	Pin Function	Port Allocation	RX210					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Interrupt	NMI (input)	P35	○	○	○	○	○	○	○	○	○	○
	IRQ0-DS (input)	P30	○	○	○	○	○	○	○	○	○	○
	IRQ0 (input)	P50	×	×	×	×	×	○	○	×	×	×
		P60	×	×	×	×	×	○	×	×	×	×
		P70	×	×	×	×	×	○	×	×	×	×
		P90	×	×	×	×	×	○	×	×	×	×
		PA0	×	×	×	×	×	○	○	○	○	×
		PD0	○	○	○	×	×	○	○	○	×	×
		PH1	○	○	○	○	○	○	○	○	○	○
	IRQ1-DS (input)	P31	○	○	○	○	○	○	○	○	○	○
	IRQ1 (input)	P51	×	×	×	×	×	○	○	×	×	×
		P61	×	×	×	×	×	○	×	×	×	×
		P71	×	×	×	×	×	○	×	×	×	×
		PD1	○	○	○	×	×	○	○	○	×	×
		PH2	○	○	○	○	○	○	○	○	○	○
	IRQ2-DS (input)	P32	○	○	○	○	×	○	○	○	○	×
	IRQ2 (input)	P12	○	○	○	×	×	○	○	○	×	×
		P52	×	×	×	×	×	○	○	×	×	×
		P62	×	×	×	×	×	○	×	×	×	×
		P82	×	×	×	×	×	○	×	×	×	×
		PB2	×	×	×	×	×	○	○	○	×	×
		PD2	○	○	○	×	×	○	○	○	×	×
	IRQ3-DS (input)	P33	○	○	×	×	×	○	○	×	×	×
	IRQ3 (input)	P13	○	○	○	×	×	○	○	○	×	×
		P23	×	×	×	×	×	○	○	×	×	×
		P53	×	×	×	×	×	○	○	×	×	×
		P63	×	×	×	×	×	○	×	×	×	×
		P83	×	×	×	×	×	○	×	×	×	×
		PB3	×	×	×	×	×	○	○	○	○	○
		PD3	○	○	×	×	×	○	○	×	×	×
	IRQ4-DS (input)	PB1	○	○	○	○	○	○	○	○	○	○
	IRQ4 (input)	P14	○	○	○	○	○	○	○	○	○	○
		P34	○	○	○	×	×	○	○	○	×	×
		P37	×	×	×	×	×	○	○	○	○	○
		P54	×	×	×	×	×	○	○	○	○	×
		P64	×	×	×	×	×	○	×	×	×	×
		PB4	×	×	×	×	×	○	○	○	×	×
		PD4	○	○	×	×	×	○	○	×	×	×
		PF5	○	×	×	×	×	○	×	×	×	×

Module/ Function	Pin Function	Port Allocation	RX210					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Interrupt	IRQ5-DS (input)	PA4	○	○	○	○	○	○	○	○	○	○
	IRQ5 (input)	P15	○	○	○	○	○	○	○	○	○	○
		P25	×	×	×	×	×	○	○	×	×	×
		P36	×	×	×	×	×	○	○	○	○	○
		PA5	×	×	×	×	×	○	○	○	×	×
		PC5	×	×	×	×	×	○	○	○	○	○
		PD5	○	○	×	×	×	○	○	×	×	×
		PE5	○	○	○	○	×	○	○	○	○	×
	IRQ6-DS (input)	PA3	○	○	○	○	○	○	○	○	○	○
	IRQ6 (input)	P16	○	○	○	○	○	○	○	○	○	○
		P26	×	×	×	×	×	○	○	○	○	○
		P56	×	×	×	×	×	○	×	×	×	×
		PB6	×	×	×	×	×	○	○	○	○	×
		PD6	○	○	×	×	×	○	○	×	×	×
		PE6	○	○	×	×	×	○	○	×	×	×
	IRQ7-DS (input)	PE2	○	○	○	○	○	○	○	○	○	○
	IRQ7 (input)	P17	○	○	○	○	○	○	○	○	○	○
		P27	×	×	×	×	×	○	○	○	○	○
		P77	×	×	×	×	×	○	×	×	×	×
		PA7	×	×	×	×	×	○	○	×	×	×
		PD7	○	○	×	×	×	○	○	×	×	×
		PE7	○	○	×	×	×	○	○	×	×	×
	IRQ8-DS (input)	P40						○	○	○	○	○
	IRQ8 (input)	P00						○	×	×	×	×
		P20						○	○	○	×	×
		P73						○	×	×	×	×
		P80						○	×	×	×	×
		PE0						○	○	○	○	×
	IRQ9-DS (input)	P41						○	○	○	○	○
	IRQ9 (input)	P01						○	×	×	×	×
		P21						○	○	○	×	×
		P81						○	×	×	×	×
		P91						○	×	×	×	×
		PE1						○	○	○	○	○
	IRQ10-DS (input)	P42						○	○	○	○	○
	IRQ10 (input)	P02						○	×	×	×	×
		P55						○	○	○	○	×
		P72						○	×	×	×	×
		P92						○	×	×	×	×
		PA2						○	○	○	×	×
		PC2						○	○	○	○	×
	IRQ11-DS (input)	P43						○	○	○	○	×
	IRQ11 (input)	P03						○	○ *3	○	○	×
		P93						○	×	×	×	×
		PA1						○	○	○	○	○
		PC3						○	○	○	○	×
		PE3						○	○	○	○	○
		PJ3						○	○	×	×	×

Module/ Function	Pin Function	Port Allocation	RX210					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Interrupt	IRQ12-DS (input)	P44						○	○	○	○	×
	IRQ12 (input)	P24						○	○	×	×	×
		P74						○	×	×	×	×
		PB0						○	○	○	○	○
		PC1						○	○	×	×	×
		PC4						○	○	○	○	○
		PE4						○	○	○	○	○
	IRQ13-DS (input)	P45						○	○	○	○	○
	IRQ13 (input)	P05						○	○	○	×	×
		P65						○	×	×	×	×
		P75						○	×	×	×	×
		PB5						○	○	○	○	○
		PC6						○	○	○	○	○
		PJ5						○	×	×	×	×
	IRQ14-DS (input)	P46						○	○	○	○	○
	IRQ14 (input)	P66						○	×	×	×	×
		P76						○	×	×	×	×
		P86						○	×	×	×	×
		PA6						○	○	○	○	○
		PC0						○	○	×	×	×
		PC7						○	○	○	○	○
	IRQ15-DS (input)	P47						○	○	○	○	○
	IRQ15 (input)	P07						○	○	○	○	×
		P22						○	○	×	×	×
		P67						○	×	×	×	×
		P87						○	×	×	×	×
		PB7						○	○	○	○	×
Multi-function timer unit 2	MTIOC0A (input/output)	P34	○	○	○	×	×	○	○	○	×	×
		PB3	○	○	○	○	○	○	○	○	○	○
		PC4	×	×	×	×	×	○	○	○	○	○
	MTIOC0B (input/output)	P13	○	○	○	×	×	○	○	○	×	×
		P15	○	○	○	○	○	○	○	○	○	○
		PA1	○	○	○	○	○	○	○	○	○	○
	MTIOC0C (input/output)	P32	○	○	○	○	×	○	○	○	○	×
		PB1	○	○	○	○	○	○	○	○	○	○
		PC5	×	×	×	×	×	○	○	○	○	○
	MTIOC0D (input/output)	P33	○	○	×	×	×	○	○	×	×	×
		PA3	○	○	○	○	○	○	○	○	○	○
	MTIOC1A (input/output)	P20	○	○	○	×	×	○	○	○	×	×
		PE4	○	○	○	○	○	○	○	○	○	○
	MTIOC1B (input/output)	P21	○	○	○	×	×	○	○	○	×	×
		PB5	○	○	○	○	○	○	○	○	○	○
		PE3	×	×	×	×	×	○	○	○	○	○
	MTIOC2A (input/output)	P26	○	○	○	○	○	○	○	○	○	○
		PB5	○	○	○	○	○	○	○	○	○	○
	MTIOC2B (input/output)	P27	○	○	○	○	○	○	○	○	○	○
		PE5	○	○	○	○	×	○	○	○	○	×
	MTIOC3A (input/output)	P14	○	○	○	○	○	○	○	○	○	○
		P17	○	○	○	○	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX210					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Multi-function timer unit 2	MTIOC3A (input/output)	PC1	○	○	×	×	×	○	○	×	×	×
		PC7	○	○	○	○	○	○	○	○	○	○
		PJ1	○	○	○	×	×	○	○	○	×	×
	MTIOC3B (input/output)	P17	○	○	○	○	○	○	○	○	○	○
		P22	○	○	×	×	×	○	○	×	×	×
		P80	○	×	×	×	×	○	×	×	×	×
		PA1	×	×	×	×	×	○	○	○	○	○
		PB7	○	○	○	○	×	○	○	○	○	×
		PC5	○	○	○	○	○	○	○	○	○	○
		PE1	×	×	×	×	×	○	○	○	○	○
		PH0	×	×	×	×	×	○	○	○	○	○
	MTIOC3C (input/output)	P16	○	○	○	○	○	○	○	○	○	○
		P56	○	×	×	×	×	○	×	×	×	×
		PC0	○	○	×	×	×	○	○	×	×	×
		PC6	○	○	○	○	○	○	○	○	○	○
		PJ3	○	○	×	×	×	○	○	×	×	×
	MTIOC3D (input/output)	P16	○	○	○	○	○	○	○	○	○	○
		P23	○	○	×	×	×	○	○	×	×	×
		P81	○	×	×	×	×	○	×	×	×	×
		PA6	×	×	×	×	×	○	○	○	○	○
		PB0	×	×	×	×	×	○	○	○	○	○
		PB6	○	○	○	○	×	○	○	○	○	×
		PC4	○	○	○	○	○	○	○	○	○	○
		PE0	×	×	×	×	×	○	○	○	○	×
		PH1	×	×	×	×	×	○	○	○	○	○
	MTIOC4A (input/output)	P21	×	×	×	×	×	○	○	○	×	×
		P24	○	○	×	×	×	○	○	×	×	×
		P55	×	×	×	×	×	○	○	○	○	×
		P82	○	×	×	×	×	○	×	×	×	×
		PA0	○	○	○	○	×	○	○	○	○	×
		PB3	○	○	○	○	○	○	○	○	○	○
		PE2	○	○	○	○	○	○	○	○	○	○
		PE4	×	×	×	×	×	○	○	○	○	○
	MTIOC4B (input/output)	P17	×	×	×	×	×	○	○	○	○	○
		P30	○	○	○	○	○	○	○	○	○	○
		P54	○	○	○	○	×	○	○	○	○	×
		PC2	○	○	○	○	×	○	○	○	○	×
		PD1	○	○	○	×	×	○	○	○	×	×
		PE3	○	○	○	○	○	○	○	○	○	○
	MTIOC4C (input/output)	P25	○	○	×	×	×	○	○	×	×	×
		P83	○	×	×	×	×	○	×	×	×	×
		P87	×	×	×	×	×	○	×	×	×	×
		PA4	×	×	×	×	×	○	○	○	○	○
		PB1	○	○	○	○	○	○	○	○	○	○
		PE1	○	○	○	○	○	○	○	○	○	○
		PE5	○	○	○	○	×	○	○	○	○	×
		PH2	×	×	×	×	×	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX210					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Multi-function timer unit 2	MTIOC4D (input/output)	P31	○	○	○	○	○	○	○	○	○	○
		P55	○	○	○	○	×	○	○	○	○	×
		P86	×	×	×	×	×	○	×	×	×	×
		PA3	×	×	×	×	×	○	○	○	○	○
		PC3	○	○	○	○	×	○	○	○	○	×
		PD2	○	○	○	×	×	○	○	○	×	×
		PE4	○	○	○	○	○	○	○	○	○	○
		PH3	×	×	×	×	×	○	○	○	○	○
	MTIOC6A (input/output)	PE7						○	○	×	×	×
	MTIOC6B (input/output)	PA5						○	○	○	×	×
		PA6						○	○	○	○	×
	MTIOC6C (input/output)	PE6						○	○	×	×	×
	MTIOC6D (input/output)	PA0						○	○	○	○	×
	MTIOC7A (input/output)	PA2						○	○	○	×	×
		PE2						○	○	○	○	○
	MTIOC7B (input/output)	PA1						○	○	○	○	○
	MTIOC7C (input/output)	P67						○	×	×	×	×
		PA4						○	○	○	○	○
	MTIOC7D (input/output)	P66						○	×	×	×	×
		PE4						○	○	○	○	○
	MTIOC8A (input/output)	PD6						○	○	×	×	×
	MTIOC8B (input/output)	PD4						○	○	×	×	×
	MTIOC8C (input/output)	PD5						○	○	×	×	×
	MTIOC8D (input/output)	PD3						○	○	×	×	×
	MTIC5U (input)	P12	×	×	×	×	×	○	○	○	×	×
		PA4	○	○	○	○	○	○	○	○	○	○
		PD7	○	○	×	×	×	○	○	×	×	×
	MTIC5V (input)	PA3	×	×	×	×	×	○	○	○	○	○
		PA6	○	○	○	○	○	○	○	○	○	○
		PD6	○	○	×	×	×	○	○	×	×	×
	MTIC5W (input)	PB0	○	○	○	○	○	○	○	○	○	○
		PD5	○	○	×	×	×	○	○	×	×	×
	MTCLKA (input)	P14	○	○	○	○	○	○	○	○	○	○
		P24	○	○	×	×	×	○	○	×	×	×
		PA4	○	○	○	○	○	○	○	○	○	○
		PC6	○	○	○	○	○	○	○	○	○	○
	MTCLKB (input)	P15	○	○	○	○	○	○	○	○	○	○
		P25	○	○	×	×	×	○	○	×	×	×
		PA6	○	○	○	○	○	○	○	○	○	○
		PC7	○	○	○	○	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX210					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Multi-function timer unit 2	MTCLKC (input)	P22	○	○	×	×	×	○	○	×	×	×
		PA1	○	○	○	○	○	○	○	○	○	○
		PC4	○	○	○	○	○	○	○	○	○	○
	MTCLKD (input)	P23	○	○	×	×	×	○	○	×	×	×
		PA3	○	○	○	○	○	○	○	○	○	○
		PC5	○	○	○	○	○	○	○	○	○	○
Port output enable 2	POE0# (input)	P32	×	×	×	×	×	○	○	○	○	×
		P93	×	×	×	×	×	○	×	×	×	×
		PC4	○	○	○	○	○	○	○	○	○	○
		PD7	○	○	×	×	×	○	○	×	×	×
		PD1	×	×	×	×	×	○	○	○	×	×
	POE1# (input)	PB5	○	○	○	○	○					
		PD6	○	○	×	×	×					
	POE2# (input)	P34	○	○	○	×	×					
		PA6	○	○	○	○	○					
		PD5	○	○	×	×	×					
	POE3# (input)	P33	○	○	×	×	×					
		PB3	○	○	○	○	○					
		PD4	○	○	×	×	×					
	POE4# (input)	P33						○	○	×	×	×
		P92						○	×	×	×	×
		PB5						○	○	○	○	○
		PD0						○	○	○	×	×
		PD6						○	○	×	×	×
	POE8# (input)	P17	○	○	○	○	○	○	○	○	○	○
		P30	○	○	○	○	○	○	○	○	○	○
		PD3	○	○	×	×	×	○	○	×	×	×
		PE3	○	○	○	○	○	○	○	○	○	○
		PJ5	×	×	×	×	×	○	×	×	×	×
	POE10# (input)	P32						○	○	○	○	×
		P34						○	○	○	×	×
		PA6						○	○	○	○	○
		PD5						○	○	×	×	×
	POE11# (input)	P33						○	○	×	×	×
		PB3						○	○	○	○	○
		PD4						○	○	×	×	×
16-bit timer pulse unit	TIOCA0 (input/output)	P86	○	×	×	×	×					
		PA0	○	×	×	×	×					
	TIOCB0 (input/output)	P17	○	×	×	×	×					
		PA1	○	×	×	×	×					
	TIOCC0 (input/output)	P32	○	×	×	×	×					
	TIOCD0 (input/output)	P33	○	×	×	×	×					
		PA3	○	×	×	×	×					
	TIOCA1 (input/output)	P56	○	×	×	×	×					
		PA4	○	×	×	×	×					
	TIOCB1 (input/output)	P16	○	×	×	×	×					
		PA5	○	×	×	×	×					

Module/ Function	Pin Function	Port Allocation	RX210					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
16-bit timer pulse unit	TIOCA2 (input/output)	P87	○	×	×	×	×					
		PA6	○	×	×	×	×					
	TIOCB2 (input/output)	P15	○	×	×	×	×					
		PA7	○	×	×	×	×					
	TIOCA3 (input/output)	P21	○	×	×	×	×					
		PB0	○	×	×	×	×					
	TIOCB3 (input/output)	P20	○	×	×	×	×					
		PB1	○	×	×	×	×					
	TIOCC3 (input/output)	P22	○	×	×	×	×					
		PB2	○	×	×	×	×					
	TIOCD3 (input/output)	P23	○	×	×	×	×					
	TIOCD3 (input/output)	PB3	○	×	×	×	×					
	TIOCA4 (input/output)	P25	○	×	×	×	×					
	TIOCA4 (input/output)	PB4	○	×	×	×	×					
	TIOCB4 (input/output)	P24	○	×	×	×	×					
		PB5	○	×	×	×	×					
	TIOCA5 (input/output)	P13	○	×	×	×	×					
		PB6	○	×	×	×	×					
	TIOCB5 (input/output)	P14	○	×	×	×	×					
		PB7	○	×	×	×	×					
	TCLKA (input)	P14	○	×	×	×	×					
		PC2	○	×	×	×	×					
	TCLKB (input)	P15	○	×	×	×	×					
		PA3	○	×	×	×	×					
		PC3	○	×	×	×	×					
	TCLKC (input)	P16	○	×	×	×	×					
		PB2	○	×	×	×	×					
		PC0	○	×	×	×	×					
	TCLKD (input)	P17	○	×	×	×	×					
		PB3	○	×	×	×	×					
		PC1	○	×	×	×	×					
8-bit timer	TMO0 (output)	P22	○	○	×	×	×	○	○	×	×	×
		PB3	○	○	○	○	○	○	○	○	○	○
		PH1	○	○	○	○	○	○	○	○	○	○
	TMCI0 (input)	P01	○	×	×	×	×	○	×	×	×	×
		P21	○	○	○	×	×	○	○	○	×	×
		PB1	○	○	○	○	○	○	○	○	○	○
		PH3	○	○	○	○	○	○	○	○	○	○
	TMRI0 (input)	P00	○	×	×	×	×	○	×	×	×	×
		P20	○	○	○	×	×	○	○	○	×	×
		PA4	○	○	○	○	○	○	○	○	○	○
		PH2	○	○	○	○	○	○	○	○	○	○
	TMO1 (output)	P17	○	○	○	○	○	○	○	○	○	○
		P26	○	○	○	○	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX210					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
8-bit timer	TMCI1 (input)	P02	○	×	×	×	×	○	×	×	×	×
		P12	○	○	○	×	×	○	○	○	×	×
		P54	○	○	○	○	×	○	○	○	○	×
		PC4	○	○	○	○	○	○	○	○	○	○
	TMRI1 (input)	P24	○	○	×	×	×	○	○	×	×	×
		PB5	○	○	○	○	○	○	○	○	○	○
	TMO2 (output)	P16	○	○	○	○	○	○	○	○	○	○
		PC7	○	○	○	○	○	○	○	○	○	○
	TMCI2 (input)	P15	○	○	○	○	○	○	○	○	○	○
		P31	○	○	○	○	○	○	○	○	○	○
		PC6	○	○	○	○	○	○	○	○	○	○
	TMRI2 (input)	P14	○	○	○	○	○	○	○	○	○	○
		PC5	○	○	○	○	○	○	○	○	○	○
	TMO3 (output)	P13	○	○	○	×	×	○	○	○	×	×
		P32	○	○	○	○	×	○	○	○	○	×
		P55	○	○	○	○	×	○	○	○	○	×
	TMCI3 (input)	P27	○	○	○	○	○	○	○	○	○	×
		P34	○	○	○	×	×	○	○	○	×	×
		PA6	○	○	○	○	○	○	○	○	○	×
	TMRI3 (input)	P30	○	○	○	○	○	○	○	○	○	×
		P33	○	○	×	×	×	○	○	×	×	×
Serial communications interface	RXD0 (input) SMISO0 (input/output) SSCL0 (input/output)	P21	○	○	○ *3	×	×	○	○	○	×	×
		P33	○	×	×	×	×	○	○	×	×	×
	TXD0 (output) SMOSI0 (input/output) SSDA0 (input/output)	P20	○	○	○ *4	×	×	○	○	○	×	×
		P32	○	×	×	×	×	○	○	○	×	×
	SCK0 (input/output)	P22	○	○	×	×	×	○	○	×	×	×
		P34	○	×	×	×	×	○	○	○	×	×
	CTS0# (input) RTS0# (output) SS0# (input)	P23	○	○	×	×	×	○	○	×	×	×
		PJ3	○	×	×	×	×	○	○	×	×	×
	RXD1 (input) SMISO1 (input/output) SSCL1 (input/output)	P15	○	○	○	○	○	○	○	○	○	○
		P30	○	○	○	○	○	○	○	○	○	○
	TXD1 (output) SMOSI1 (input/output) SSDA1 (input/output)	P16	○	○	○	○	○	○	○	○	○	○
		P26	○	○	○	○	○	○	○	○	○	○
	SCK1 (input/output)	P17	○	○	○	○	○	○	○	○	○	○
		P27	○	○	○	○	○	○	○	○	○	○
	CTS1# (input) RTS1# (output) SS1# (input)	P14	○	○	○	○	○	○	○	○	○	○
		P31	○	○	○	○	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX210					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial communications interface	RXD2 (input) SMISO2 (input/output) SSCL2 (input/output)	P12	○	×	×	×	×	○	○	×	×	×
		P52	○	×	×	×	×	○	○	×	×	×
	TXD2 (output) SMOSI2 (input/output) SSDA2 (input/output)	P13	○	×	×	×	×	○	○	×	×	×
		P50	○	×	×	×	×	○	○	×	×	×
	SCK2 (input/output)	P51	○	×	×	×	×	○	○	×	×	×
	CTS2# (input) RTS2# (output) SS2# (input)	P54	○	×	×	×	×	○	○	×	×	×
		PJ5	×	×	×	×	×	○	×	×	×	×
	RXD3 (input) SMISO3 (input/output) SSCL3 (input/output)	P16	○	×	×	×	×	○	○	○	○	○
		P25	○	×	×	×	×	○	○	×	×	×
	TXD3 (output) SMOSI3 (input/output) SSDA3 (input/output)	P17	○	×	×	×	×	○	○	○	○	○
		P23	○	×	×	×	×	○	○	×	×	×
	SCK3 (input/output)	P15	○	×	×	×	×	○	○	○	○	○
		P24	○	×	×	×	×	○	○	×	×	×
	CTS3# (input) RTS3# (output) SS3# (input)	P26	○	×	×	×	×	○	○	○	○	○
	RXD4 (input) SMISO4 (input/output) SSCL4 (input/output)	PB0	○	×	×	×	×	○	○	○	○	○
		PK4	○	×	×	×	×	○	×	×	×	×
	TXD4 (output) SMOSI4 (input/output) SSDA4 (input/output)	PB1	○	×	×	×	×	○	○	○	○	○
		PK5	○	×	×	×	×	○	×	×	×	×
	SCK4 (input/output)	P70	○	×	×	×	×	○	×	×	×	×
		PB3	○	×	×	×	×	○	○	○	○	○
	CTS4# (input) RTS4# (output) SS4# (input)	PB2	○	×	×	×	×	○	○	○	×	×
		PE6	○	×	×	×	×	○	○	×	×	×
	RXD5 (input) SMISO5 (input/output) SSCL5 (input/output)	PA2	○	○	○	×	×	○	○	○	×	×
		PA3	○	○	○	○	○	○	○	○	○	○
		PC2	○	○	○	○	×	○	○	○	○	×

Module/ Function	Pin Function	Port Allocation	RX210					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial communications interface	TXD5 (output) SMOSI5 (input/output) SSDA5 (input/output)	PA4	○	○	○	○	○	○	○	○	○	○
		PC3	○	○	○	○	×	○	○	○	○	×
	SCK5 (input/output)	PA1	○	○	○	○	○	○	○	○	○	○
		PC1	○	○	×	×	×	○	○	×	×	×
		PC4	○	○	○	○	○	○	○	○	○	○
	CTS5# (input) RTS5# (output) SS5# (input)	PA6	○	○	○	○	○	○	○	○	○	○
		PC0	○	○	×	×	×	○	○	×	×	×
	RXD6 (input) SMISO6 (input/output) SSCL6 (input/output)	P01	○	×	×	×	×	○	×	×	×	×
		P33	○	○	×	×	×	○	○	×	×	×
		PB0	○	○	○	○	○	○	○	○	○	○
	TXD6 (output) SMOSI6 (input/output) SSDA6 (input/output)	P00	○	×	×	×	×	○	×	×	×	×
		P32	○	○	○	○	×	○	○	○	○	×
		PB1	○	○	○	○	○	○	○	○	○	○
	SCK6 (input/output)	P02	○	×	×	×	×	○	×	×	×	×
		P34	○	○	○	×	×	○	○	○	×	×
		PB3	○	○	○	○	○	○	○	○	○	○
	CTS6# (input) RTS6# (output) SS6# (input)	PB2	○	○	○	×	×	○	○	○	×	×
		PJ3	○	○	×	×	×	○	○	×	×	×
	RXD7 (input) SMISO7 (input/output) SSCL7 (input/output)	P92	○	×	×	×	×	○	×	×	×	×
	TXD7 (output) SMOSI7 (input/output) SSDA7 (input/output)	P55	×	×	×	×	×	○	×	×	×	×
		P90	○	×	×	×	×	○	×	×	×	×
	SCK7 (input/output)	P56	×	×	×	×	×	○	×	×	×	×
		P91	○	×	×	×	×	○	×	×	×	×
	CTS7# (input) RTS7# (output) SS7# (input)	P93	○	×	×	×	×	○	×	×	×	×
	RXD8 (input) SMISO8 (input/output) SSCL8 (input/output)	PC6	○	○	○	○	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX210					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial communications interface	TXD8 (output) SMOSI8 (input/output) SSDA8 (input/output)	PC7	○	○	○	○	○	○	○	○	○	○
	SCK8 (input/output)	PC5	○	○	○	○	○	○	○	○	○	○
	CTS8# (input) RTS8# (output) SS8# (input)	PC4	○	○	○	○	○	○	○	○	○	○
	RXD9 (input) SMISO9 (input/output) SSCL9 (input/output)	PB6	○	○	○	○	×	○	○	○	○	×
		PK3	○	×	×	×	×	○	×	×	×	×
	TXD9 (output) SMOSI9 (input/output) SSDA9 (input/output)	PB7	○	○	○	○	×	○	○	○	○	×
		PK2	○	×	×	×	×	○	×	×	×	×
	SCK9 (input/output)	P60	○	×	×	×	×	○	×	×	×	×
		PB5	○	○	○	○	×	○	○	○	○	×
	CTS9# (input) RTS9# (output) SS9# (input)	P61	○	×	×	×	×	○	×	×	×	×
		PB4	○	○	○	×	×	○	○	○	×	×
	RXD10 (input) SMISO10 (input/output) SSCL10 (input/output)	P81	○	×	×	×	×	○	×	×	×	×
		P86	×	×	×	×	×	○	×	×	×	×
		PC6	×	×	×	×	×	○	○	○	○	○
	RXD010 (input) SMISO010 (input/output) SSCL010 (input/output)	P81						○	×	×	×	×
		P86						○	×	×	×	×
		PC6						○	○	○	○	○
	TXD10 (output) SMOSI10 (input/output) SSDA10 (input/output)	P82	○	×	×	×	×	○	×	×	×	×
		P87	×	×	×	×	×	○	×	×	×	×
		PC7	×	×	×	×	×	○	○	○	○	○
	TXD010 (output) SMOSI010 (input/output) SSDA010 (input/output)	P82						○	×	×	×	×
		P87						○	×	×	×	×
		PC7						○	○	○	○	○
	SCK10 (input/output)	P80	○	×	×	×	×	○	×	×	×	×
		P83	×	×	×	×	×	○	×	×	×	×
		PC5	×	×	×	×	×	○	○	○	○	○
	SCK010 (input/output) RTS010# (output) DE010 (output)	P80						○	×	×	×	×

Module/ Function	Pin Function	Port Allocation	RX210					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial communications interface	SCK010 (input/output) CTS010# (input) SS010# (input)	P83						○	×	×	×	×
	SCK010 (input/output)	PC5						○	○	○	○	○
	CTS10# (input) RTS10# (output) SS10# (input)	P83	○	×	×	×	×	×	×	×	×	×
		PC4	×	×	×	×	×	○	○	○	○	○
	RTS10# (output)	P80						○	×	×	×	×
	CTS10# (input) SS10# (input)	P83						○	×	×	×	×
	CTS010# (input) RTS010# (output) SS010# (input) DE010 (output)	PC4						○	○	○	○	○
	RXD11 (input) SMISO11 (input/output) SSCL11 (input/output)	P76	○	×	×	×	×	○	×	×	×	×
		PB6	×	×	×	×	×	○	○	○	○	×
	RXD011 (input) SMISO011 (input/output) SSCL011 (input/output)	P76						○	×	×	×	×
		PB6						○	○	○	○	×
		PC0						○	○	×	×	×
	TXD11 (output) SMOSI11 (input/output) SSDA11 (input/output)	P77	○	×	×	×	×	○	×	×	×	×
		PB7	×	×	×	×	×	○	○	○	○	×
	TXD011 (output) SMOSI011 (input/output) SSDA011 (input/output)	P77						○	×	×	×	×
		PB7						○	○	○	○	×
		PC1						○	○	×	×	×
	SCK11 (input/output)	P75	○	×	×	×	×	○	×	×	×	×
		PB5	×	×	×	×	×	○	○	○	○	×
	SCK011 (input/output) RTS011# (output) DE011 (output)	P75						○	×	×	×	×
	SCK011 (input/output)	PB5						○	○	○	○	×
	TXDA011 (output)	PC1						○	○	×	×	×
	TXDB011 (output)	PC2						○	○	○	○	×
	CTS11# (input) RTS11# (output) SS11# (input)	P74	○	×	×	×	×	×	×	×	×	×
		PB4	×	×	×	×	×	○	○	○	×	×
	CTS011# (input) SS011# (input)	P74						○	×	×	×	×

Module/ Function	Pin Function	Port Allocation	RX210					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial communications interface	CTS011# (input) RTS011# (output) SS011# (input) DE011 (output)	PB4						○	○	○	×	×
	RTS11# (output)	P75						○	×	×	×	×
	CTS11# (input) SS11# (input)	P74						○	×	×	×	×
	RXD12 (input) SMISO12 (input/output) SSCL12 (input/output) RXDX12 (input)	PA2	×	×	×	×	×	○	○	○	×	×
		PE2	○	○	○	○	○ *5	○	○	○	○	○
	TXD12 (output) SMOSI12 (input/output) SSDA12 (input/output) TXDX12 (output) SIOX12 (input/output)	PA4	×	×	×	×	×	○	○	○	○	○
		PE1	○	○	○	○	○ *6	○	○	○	○	○
	SCK12 (input/output)	PA1	×	×	×	×	×	○	○	○	○	○
		PE0	○	○	○	○	×	○	○	○	○	×
	CTS12# (input) RTS12# (output) SS12# (input)	PA6	×	×	×	×	×	○	○	○	○	○
		PE3	○	○	○	○	○ *7	○	○	○	○	○
I^2C bus interface	SCL-DS (input/output)	P16	○	○	○	○	○					
	SCL (input/output)	P12	○	○	○	×	×					
	SDA-DS (input/output)	P17	○	○	○	○	○					
	SDA (input/output)	P13	○	○	○	×	×					
	SCL0 (input/output)	P12						○	○	○	×	×
	SDA0 (input/output)	P13						○	○	○	×	×
	SCL2 (input/output)	P16						○	○	○	○	○
	SDA2 (input/output)	P17						○	○	○	○	○
Serial peripheral interface	RSPCKA (input/output)	PA5	○	○	○	×	×	○	○	○	×	×
		PB0	○	○	○	○	○	○	○	○	○	○
		PC5	○	○	○	○	○	○	○	○	○	○
	MOSIA (input/output)	P16	○	○	○	○	○	○	○	○	○	○
		PA6	○	○	○	○	○	○	○	○	○	○
		PC6	○	○	○	○	○	○	○	○	○	○
	MISOA (input/output)	P17	○	○	○	○	○	○	○	○	○	○
		PA7	○	○	×	×	×	○	○	×	×	×
		PC7	○	○	○	○	○	○	○	○	○	○
	SSLA0 (input/output)	PA4	○	○	○	○	○	○	○	○	○	○
		PC4	○	○	○	○	○	○	○	○	○	○
	SSLA1 (output)	PA0	○	○	○	○	×	○	○	○	○	×
		PC0	○	○	×	×	×	○	○	×	×	×

Module/ Function	Pin Function	Port Allocation	RX210					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial peripheral interface	SSLA2 (output)	PA1	○	○	○	○	○	○	○	○	○	○
		PC1	○	○	×	×	×	○	○	×	×	×
	SSLA3 (output)	PA2	○	○	○	×	×	○	○	○	×	×
		PC2	○	○	○	○	×	○	○	○	○	×
Realtime clock*8	RTCOUT (output)	P16	○	○	○	○	×	○	○	○	○	×
		P32	○	○	○	○	×	○	○	○	○	×
	RTCIC0 (input)*1	P30	○	○	○	○	×	○	○	○	○	×
	RTCIC1 (input)*1	P31	○	○	○	○	×	○	○	○	○	×
	RTCIC2 (input)*1	P32	○	○	○	○	×	○	○	○	○	×
12-bit A/D converter	AN000 (input)*1	P40	○	○	○	○	○	○	○	○	○	○
	AN001 (input)*1	P41	○	○	○	○	○	○	○	○	○	○
	AN002 (input)*1	P42	○	○	○	○	○	○	○	○	○	○
	AN003 (input)*1	P43	○	○	○	○	×	○	○	○	○	×
	AN004 (input)*1	P44	○	○	○	○	×	○	○	○	○	×
	AN005 (input)*1	P45	○	○	○	×	×	○	○	○	○	○
	AN006 (input)*1	P46	○	○	○	○	○	○	○	○	○	○
	AN007 (input)*1	P47	○	○	○	×	×	○	○	○	○	○
	AN008 (input)*1	PE0	○	○	○	○	×	○	○	○	○	×
	AN009 (input)*1	PE1	○	○	○	○	○	○	○	○	○	○
	AN010 (input)*1	PE2	○	○	○	○	○	○	○	○	○	○
	AN011 (input)*1	PE3	○	○	○	○	○	○	○	○	○	○
	AN012 (input)*1	PE4	○	○	○	○	○	○	○	○	○	○
	AN013 (input)*1	PE5	○	○	○	○	×	○	○	○	○	×
	AN014 (input)*1	PE6	○	○	×	×	×	○	○	×	×	×
	AN015 (input)*1	PE7	○	○	×	×	×	○	○	×	×	×
	AN016 (input)	PD0						○	○	○	×	×
	AN017 (input)	PD1						○	○	○	×	×
	AN018 (input)	PD2						○	○	○	×	×
	AN019 (input)	PD3						○	○	×	×	×
	AN020 (input)	PD4						○	○	×	×	×
	AN021 (input)	PD5						○	○	×	×	×
	AN022 (input)	PD6						○	○	×	×	×
	AN023 (input)	PD7						○	○	×	×	×
	ADST0 (output)	PA4						○	○	○	○	○
		PH1						○	○	○	○	○
	ADTRG0# (input)	P07	○	○	○	×	×	○	○	○	○	×
		P16	○	○	○	○	○	○	○	○	○	○
		P25	○	○	×	×	×	○	○	×	×	×
		PA1	×	×	×	×	×	○	○	○	○	○
		PH0	×	×	×	×	×	○	○	○	○	○
D/A converter	DA0 (output)*1	P03	○	○	○	○	×					
	DA1 (output)*1	P05	○	○	○	○	×					
12-bit D/A converter	DA0 (output)	P03						○	○	○	○	×
	DA1 (output)	P05						○	○	○	×	×
Clock frequency accuracy measurement circuit	CACREF (input)	PA0	○	○	○	○	×	○	○	○	○	×
		PC7	○	○	○	○	○	○	○	○	○	○
		PH0	○	○	○	○	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX210					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Comparator A	CMPA1 (input)*1	PE3	○	○	○	○	○					
	CMPA2 (input)*1	PE4	○	○	○	○	○					
	CVREFA (input)*1	PA1	○	○	○	○	○					
Comparator B	CMPB0 (input)*1	PE1	○	○	○	○	○					
	CVREFB0 (input)*1	PE2	○	○	○	○	○					
	CMPB1 (input*1	PA3	○	○	○	○	○					
	CVREFB1 (input)*1	PA4	○	○	○	○	○					
External bus	CS0# (output)	P24	○	○	×	×	×					
		PC7	○	○	×	×	×					
	CS1# (output)	P25	○	○	×	×	×					
		PC6	○	○	×	×	×					
	CS2# (output)	P26	○	○	×	×	×					
		PC5	○	○	×	×	×					
	CS3# (output)	P27	○	○	×	×	×					
		PC4	○	○	×	×	×					
	A0 to A7 (output)	PA0 to PA7	○	○	×	×	×					
	A8 to A15 (output)	PB0 to PB7	○	○	×	×	×					
	A16 to A23 (output)	PC0 to PC7	○	○	×	×	×					
	D0 to D7 (input/output)	PD0 to PD7	○	○	×	×	×					
	D8 to D15 (input/output)	PE0 to PE7	○	○	×	×	×					
	BCLK (output)	P53	○	○	×	×	×					
	RD# (output)	P52	○	○	×	×	×					
	WR# (output)	P50	○	○	×	×	×					
	WR0# (output)	P50	○	○	×	×	×					
	WR1# (output)	P51	○	○	×	×	×					
	BC0# (output)	PA0	○	○	×	×	×					
	BC1# (output)	P51	○	○	×	×	×					
	WAIT# (input)	P51	○	○	×	×	×					
	WAIT# (input)	P55	○	○	×	×	×					
		PC5	○	○	×	×	×					
	ALE (output)	P54	○	○	×	×	×					
Compare match timer W	TOC0 (output)	PC7						○	○	○	○	○
	TIC0 (input)	PC6						○	○	○	○	○
	TOC1 (output)	PE7						○	○	×	×	×
		PH2						○	○	○	○	○
	TIC1 (input)	PE6						○	○	×	×	×
		PH1						○	○	○	○	○
	TOC2 (output)	PB5						○	○	○	○	○
		PD3						○	○	×	×	×
	TIC2 (input)	PB3						○	○	○	○	○
		PD2						○	○	○	×	×
	TOC3 (output)	PE3						○	○	○	○	○
	TIC3 (input)	PE2						○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX210					RX660				
			144-Pin	100-Pin	80-Pin	64-Pin	48-Pin	144-Pin	100-Pin	80-Pin	64-Pin	48-Pin
CAN FD module	CRX0 (input)	P15						○	○	○	○	○
		P33						○	○	×	×	×
		P55						○	○	○	○	×
		PD2						○	○	○	×	×
	CTX0 (output)	P14						○	○	○	○	○
		P32						○	○	○	○	×
		P54						○	○	○	○	×
		PD1						○	○	○	×	×
Remote control signal receiver	PMC0 (input)	P51						○	○	×	×	×
		P53						○	○	×	×	×
		PB3						○	○	○	○	○
		PC3						○	○	○	○	×
		PC4						○	○	○	○	○
		PC5						○	○	○	○	○
Comparator C	CMPC00 (input)	PE1						○	○	○	○	○
	CMPC10 (input)	PA3						○	○	○	○	○
	CMPC20 (input)	P15						○	○	○	○	○
	CMPC30 (input)	P26						○	○	○	○	○
	COMP0 (output)	PE5						○	○	○	○	×
	COMP1 (output)	PB1						○	○	○	○	○
	COMP2 (output)	P17						○	○	○	○	○
	COMP3 (output)	P30						○	○	○	○	○
	CVREFC0 (input)	PE2						○	○	○	○	○
	CVREFC1 (input)	PA4						○	○	○	○	○
	CVREFC2 (input)	P14						○	○	○	○	○
	CVREFC3 (input)	P27						○	○	○	○	○

Notes: 1. To use this pin function, set the corresponding pin as general input (clear the PORT.PDR.Bm and PORT.PMR.Bm bits to 0).
2. Not present on products provided with a JTAG.
3. SMISO0 function not implemented.
4. SMOSI0 function not implemented.
5. SMISO12 function not implemented.
6. SMOSI12 function not implemented.
7. SS12# function not implemented.
8. Only present in products incorporating a sub-clock oscillator.

Table 2.41 Comparison of P0n Pin Function Control Register (P0nPFS)

Register	Bit	RX210 (n = 0 to 3, 5, 7)	RX660 (n = 0 to 3, 5, 7)
P03PFS	PSEL[3:0] (RX210)	P03 pin function select bits	—
P05PFS	PSEL[3:0] (RX210)	P05 pin function select bits	—
P0nPFS	ISEL	—	Interrupt input function select bit

Table 2.42 Comparison of P1n Pin Function Control Register (P1nPFS)

Register	Bit	RX210 (n = 2 to 7)	RX660 (n = 2 to 7)
P12PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0101b: TMCI1 1010b: RXD2/SMISO2/SSCL2 1111b: SCL	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000101b: TMCI1 001010b: RXD2/SMISO2/SSCL2 001111b: SCL0
P13PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC0B 0011b: TIOCA5 0101b: TMO3 1010b: TXD2/SMOSI2/SSDA2 1111b: SDA	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000101b: TMO3 001010b: TXD2/SMOSI2/SSDA2 001111b: SDA0
P14PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC3A 0010b: MTCLKA 0011b: TIOCB5 0100b: TCLKA 0101b: TMRI2 1011b: CTS1#/RTS1#/SS1#	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKA 000101b: TMRI2 001011b: CTS1#/RTS1#/SS1# 010000b: CTX0
P15PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC0B 0010b: MTCLKB 0011b: TIOCB2 0100b: TCLKB 0101b: TMCI2 1010b: RXD1/SMISO1/SSCL1 1011b: SCK3	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKB 000101b: TMCI2 001010b: RXD1/SMISO1/SSCL1 001011b: SCK3 010000b: CRX0
P16PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC3C 0010b: MTIOC3D 0011b: TIOCB1 0100b: TCLKC 0101b: TMO2 0111b: RTCOUT 1001b: ADTRG0# 1010b: TXD1/SMOSI1/SSDA1 1011b: RXD3/SMISO3/SSCL3 1101b: MOSIA 1111b: SCL-DS	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTIOC3D 000101b: TMO2 000111b: RTCOUT*1 001001b: ADTRG0# 001010b: TXD1/SMOSI1/SSDA1 001011b: RXD3/SMISO3/SSCL3 001101b: MOSIA 001111b: SCL2

Register	Bit	RX210 (n = 2 to 7)	RX660 (n = 2 to 7)
P17PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC3A 0010b: MTIOC3B 0011b: TIOCB0 0100b: TCLKD 0101b: TMO1 0111b: POE8# 1010b: SCK1 1011b: TXD3/SMOSI3/SSDA3 1101b: MISOA 1111b: SDA-DS	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTIOC3B 000101b: TMO1 000111b: POE8# 001000b: MTIOC4B 001010b: SCK1 001011b: TXD3/SMOSI3/SSDA3 001101b: MISOA 001111b: SDA2 011110b: COMP2
P1nPFS	ASEL	—	Analog function select bit

Note: 1. Only present in products incorporating a sub-clock oscillator.

Table 2.43 Comparison of P2n Pin Function Control Register (P2nPFS)

Register	Bit	RX210 (n = 0 to 7)	RX660 (n = 0 to 7)
P20PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC1A 0011b: TIOCB3 0101b: TMRI0 1010b: TXD0/SMOSI0/SSDA0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC1A 000101b: TMRI0 001010b: RXD0/SMISO0/SSCL0
P21PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC1B 0011b: TIOCA3 0101b: TMCI0 1010b: RXD0/SMISO0/SSCL0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC1B 000101b: TMCI0 001000b: MTIOC4A 001010b: RXD0/SMISO0/SSCL0
P22PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC3B 0010b: MTCLKC 0011b: TIOCC3 0101b: TMO0 1010b: SCK0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKC 000101b: TMO0 001010b: SCK0
P23PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC3D 0010b: MTCLKD 0011b: TIOCD3 1010b: TXD3/SMOSI3/SSDA3 1011b: CTS0#/RTS0#/SS0#	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKD 001010b: TXD3/SMOSI3/SSDA3 001011b: CTS0#/RTS0#/SS0#
P24PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC4A 0010b: MTCLKA 0011b: TIOCB4 0101b: TMRI1 1010b: SCK3	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000010b: MTCLKA 000101b: TMRI1 001010b: SCK3
P25PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC4C 0010b: MTCLKB 0011b: TIOCA4 1001b: ADTRG0# 1010b: RXD3/SMISO3/SSCL3	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000010b: MTCLKB 001001b: ADTRG0# 001010b: RXD3/SMISO3/SSCL3
P2nPFS	ISEL	—	Interrupt input function select bit
P2nPFS	ASEL	—	Analog function select bit

Table 2.44 Comparison of P3n Pin Function Control Register (P3nPFS)

Register	Bit	RX210 (n = 0 to 4)	RX660 (n = 0 to 4, 6, 7)
P30PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC4B 0101b: TMRI3 0111b: POE8# 1010b: RXD1/SMISO1/SSCL1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000101b: TMRI3 000111b: POE8# 001010b: RXD1/SMISO1/SSCL1 011110b: COMP3
P32PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC0C 0011b: TIOCC0 0101b: TMO3 0111b: RTCOUT 1010b: TXD0/SMOSI0/SSDA0 1011b: TXD6/SMOSI6/SSDA6	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0C 000101b: TMO3 000111b: RTCOUT*1 001000b: POE0# 001010b: TXD6/SMOSI6/SSDA6 001011b: TXD0/SMOSI0/SSDA0 010000b: CTX0 100001b: POE10#
P33PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC0D 0011b: TIOCD0 0101b: TMRI3 0111b: POE3# 1010b: RXD0/SMISO0/SSCL0 1011b: RXD6/SMISO6/SSCL6	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0D 000101b: TMRI3 001000b: POE4# 001010b: RXD6/SMISO6/SSCL6 001011b: RXD0/SMISO0/SSCL0 010000b: CRX0 100001b: POE11#
P34PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC0A 0101b: TMCI3 0111b: POE2# 1010b: SCK0 1011b: SCK6	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0A 000101b: TMCI3 000111b: POE10# 001010b: SCK6 001011b: SCK0

Register	Bit	RX210 (n = 0 to 4)	RX660 (n = 0 to 4, 6, 7)
P3nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0-DS (145/144/100/80/69/64/48-pin) P31: IRQ1-DS (145/144/100/80/69/64/48-pin) P32: IRQ2-DS (145/144/100/80/69/64/48-pin) P33: IRQ3-DS (145/144/100-pin) P34: IRQ4 (145/144/100/80-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0-DS (144/100/80/64/48-pin) P31: IRQ1-DS (144/100/80/64/48-pin) P32: IRQ2-DS (144/100/80/64-pin) P33: IRQ3-DS (144/100-pin) P34: IRQ4 (144/100/80-pin) P36: IRQ5 (144/100/80/64/48-pin) P37: IRQ4 (144/100/80/64/48-pin)

Note: 1. Only present in products incorporating a sub-clock oscillator.

Table 2.45 Comparison of P4n Pin Function Control Register (P4nPFS)

Register	Bit	RX210 (n = 0 to 7)	RX660 (n = 0 to 7)
P4nPFS	ISEL	—	Interrupt input function select bit

Table 2.46 Comparison of P5n Pin Function Control Register (P5nPFS)

Register	Bit	RX210 (n = 0 to 2, 4 to 6)	RX660 (n = 0 to 6)
P51PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 1010b: SCK2	Pin function select bits 000000b: Hi-Z 001010b: SCK2 100110b: PMC0
P53PFS	—	—	P53 pin function control register
P54PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC4B 0101b: TMCI1 1011b: CTS2#/RTS2#/SS2#	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000101b: TMCI1 001011b: CTS2#/RTS2#/SS2# 010000b: CTX0
P55PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC4D 0101b: TMO3	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000010b: MTIOC4A 000101b: TMO3 001010b: TXD7/SMOSI7/SSDA7 010000b: CRX0
P56PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC3C 0011b: TIOCA1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 001010b: SCK7
P5nPFS	ISEL	—	Interrupt input function select bit

Table 2.47 Comparison of P6n Pin Function Control Register (P6nPFS)

Register	Bit	RX210 (n = 0, 1)	RX660 (n = 0 to 7)
P66PFS	PSEL[5:0]	—	P66 pin function control register
P67PFS	PSEL[5:0]	—	P67 pin function control register
P6nPFS	ISEL	—	Interrupt input function select bit

Table 2.48 Comparison of P7n Pin Function Control Register (P7nPFS)

Register	Bit	RX210	RX660 (n = 0 to 7)
P74PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 1011b: CTS11#/RTS11#/SS11#	Pin function select bits 000000b: Hi-Z 001011b: CTS11#/SS11# 101101b: CTS011#/SS011#
P75PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 1010b: SCK11	Pin function select bits 000000b: Hi-Z 001010b: SCK11 001011b: RTS11# 101100b: SCK011 101101b: RTS011# 101110b: DE011
P76PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 1010b: RXD11/SMISO11/SSCL11	Pin function select bits 000000b: Hi-Z 001010b: RXD11/SMISO11/ SSCL11 101100b: RXD011/SMISO011/ SSCL011
P77PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 1011b: TXD11/SMOSI11/SSDA11	Pin function select bits 000000b: Hi-Z 001010b: TXD11/SMOSI11/ SSDA11 101100b: TXD011/SMOSI011/ SSDA011
P7nPFS	ISEL	—	Interrupt input function select bit

Table 2.49 Comparison of P8n Pin Function Control Register (P8nPFS)

Register	Bit	RX210 (n = 0 to 3, 6, 7)	RX660 (n = 0 to 3, 6, 7)
P80PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC3B 1010b: SCK10	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 001010b: SCK10 001011b: RTS10# 101100b: SCK010 101101b: RTS010# 101110b: DE010

Register	Bit	RX210 (n = 0 to 3, 6, 7)	RX660 (n = 0 to 3, 6, 7)
P81PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC3D 1010b: RXD10/SMISO10/SSCL10	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 001010b: RXD10/SMISO10/ SSCL10 101100b: RXD010/SMISO010/ SSCL010
P82PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC4A 1010b: TXD10/SMOSI10/SSDA10	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 001010b: TXD10/SMOSI10/ SSDA10 101100b: TXD010/SMOSI010/ SSDA010
P83PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC4C 1011b: CTS10#/RTS10#/SS10#	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 001010b: SCK10 001011b: CTS10#/SS10# 101100b: SCK010 101101b: CTS010#/SS010#
P86PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0011b: TIOCA0	Pin function select bits 000000b: Hi-Z 001000b: MTIOC4D 001010b: RXD10/SMISO10/ SSCL10 101100b: RXD010/SMISO010/ SSCL010
P87PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0011b: TIOCA2	Pin function select bits 000000b: Hi-Z 001000b: MTIOC4C 001010b: TXD10/SMOSI10/ SSDA10 101100b: TXD010/SMOSI010/ SSDA010
P8nPFS	—	—	P8n pin function control register

Table 2.50 Comparison of P9n Pin Function Control Register (P9nPFS)

Register	Bit	RX210	RX660 (n = 0 to 3)
P92PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 1010b: RXD7/SMISO7/SSCL7	Pin function select bits 000000b: Hi-Z 001000b: POE4# 001010b: RXD7/SMISO7/SSCL7
P93PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 1011b: CTS7#/RTS7#/SS7#	Pin function select bits 000000b: Hi-Z 001000b: POE0# 001011b: CTS7#/RTS7#/SS7#
P9nPFS	—	—	P9n pin function control register

Table 2.51 Comparison of PAn Pin Function Control Register (PAnPFS)

Register	Bit	RX210 (n = 0 to 7)	RX660 (n = 0 to 7)
PA0PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC4A 0011b: TIOCA0 0111b: CACREF 1101b: SSLA1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000111b: CACREF 001000b: MTIOC6D 001101b: SSLA1
PA1PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC0B 0010b: MTCLKC 0011b: TIOCB0 1010b: SCK5 1101b: SSLA2	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKC 001000b: MTIOC7B 001001b: ADTRG0# 001010b: SCK5 001100b: SCK12 001101b: SSLA2 100111b: MTIOC3B
PA2PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 1010b: RXD5/SMISO5/SSCL5 1101b: SSLA3	Pin function select bits 000000b: Hi-Z 001000b: MTIOC7A 001010b: RXD5/SMISO5/SSCL5 001100b: RXD12/SMISO12/ SSCL12/RXDX12 001101b: SSLA3

Register	Bit	RX210 (n = 0 to 7)	RX660 (n = 0 to 7)
PA3PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC0D 0010b: MTCLKD 0011b: TIOCD0 0100b: TCLKB 1010b: RXD5/SMISO5/SSCL5	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0D 000010b: MTCLKD 001000b: MTIC5V 001010b: RXD5/SMISO5/SSCL5 100111b: MTIOC4D
PA4PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIC5U 0010b: MTCLKA 0011b: TIOCA1 0101b: TMRI0 1010b: TXD5/SMOSI5/SSDA5 1101b: SSLA0	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000010b: MTCLKA 000101b: TMRI0 001000b: MTIOC4C 001001b: ADST0 001010b: TXD5/SMOSI5/SSDA5 001100b: TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12 001101b: SSLA0 100111b: MTIOC7C
PA5PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0011b: TIOCB1 1101b: RSPCKA	Pin function select bits 000000b: Hi-Z 001000b: MTIOC6B 001101b: RSPCKA
PA6PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIC5V 0010b: MTCLKB 0011b: TIOCA2 0101b: TMCI3 0111b: POE2# 1011b: CTS5#/RTS5#/SS5# 1101b: MOSIA	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000010b: MTCLKB 000101b: TMCI3 000111b: POE10# 001000b: MTIOC3D 001011b: CTS5#/RTS5#/SS5# 001100b: CTS12#/RTS12#/SS12# 001101b: MOSIA 100111b: MTIOC6B
PA7PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0011b: TIOCB2 1101b: MISOA	Pin function select bits 000000b: Hi-Z 001101b: MISOA

Register	Bit	RX210 (n = 0 to 7)	RX660 (n = 0 to 7)
PAnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA3: IRQ6-DS (145/144/100/80/69/64/48-pin) PA4: IRQ5-DS (145/144/100/80/69/64/48-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA0: IRQ0 (144/100/80/64-pin) PA1: IRQ11 (144/100/80/64/48-pin) PA2: IRQ10 (144/100/80-pin) PA3: IRQ6-DS (144/100/80/64/48-pin) PA4: IRQ5-DS (144/100/80/64/48-pin) PA5: IRQ5 (144/100/80-pin) PA6: IRQ14 (144/100/80/64/48-pin) PA7: IRQ7 (144/100-pin)
PAnPFS	ASEL	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin PA1: CVREFA (145/144/100/80/69/64/48-pin) PA3: CMPB1 (145/144/100/80/69/64/48-pin) PA4: CVREFB1 (145/144/100/80/69/64/48-pin)	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin PA3: CMPC10 (144/100/80/64/48-pin) PA4: CVREFC1 (144/100/80/64/48-pin)

Table 2.52 Comparison of PBn Pin Function Control Register (PBnPFS)

Register	Bit	RX210 (n = 0 to 7)	RX660 (n = 0 to 7)
PB0PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIC5W 0011b: TIOCA3 1010b: RXD4/SMISO4/SSCL4 1011b: RXD6/SMISO6/SSCL6 1101b: RSPCKA	Pin function select bits 000000b: Hi-Z 000001b: MTIC5W 000010b: MTIOC3D 001010b: RXD4/SMISO4/SSCL4 001011b: RXD6/SMISO6/SSCL6 001101b: RSPCKA
PB1PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIC0C 0010b: MTIOC4C 0011b: TIOCB3 0101b: TMCI0 1010b: TXD4/SMOSI4/SSDA4 1011b: TXD6/SMOSI6/SSDA6	Pin function select bits 000000b: Hi-Z 000001b: MTIC0C 000010b: MTIOC4C 000101b: TMCI0 001010b: TXD4/SMOSI4/SSDA4 001011b: TXD6/SMOSI6/SSDA6 011110b: COMP1

Register	Bit	RX210 (n = 0 to 7)	RX660 (n = 0 to 7)
PB2PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0011b: TIOCC3 0100b: TCLKC 1010b: CTS4#/RTS4#/SS4# 1011b: CTS6#/RTS6#/SS6#	Pin function select bits 000000b: Hi-Z 001010b: CTS4#/RTS4#/SS4# 001011b: CTS6#/RTS6#/SS6#
PB3PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC0A 0010b: MTIOC4A 0011b: TIOCD3 0100b: TCLKD 0101b: TMO0 0111b: POE3# 1010b: SCK4 1011b: SCK6	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0A 000010b: MTIOC4A 000101b: TMO0 000111b: POE11# 001010b: SCK4 001011b: SCK6 011101b: TIC2 100110b: PMC0
PB4PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0011b: TIOCA4 1011b: CTS9#/RTS9#/SS9#	Pin function select bits 000000b: Hi-Z 001011b: CTS9#/RTS9#/SS9# 100100b: CTS11#/RTS11#/SS11# 101100b: CTS011#/RTS011#/ SS011# 101110b: DE011
PB5PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC2A 0010b: MTIOC1B 0011b: TIOCB4 0101b: TMRI1 0111b: POE1# 1010b: SCK9	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2A 000010b: MTIOC1B 000101b: TMRI1 000111b: POE4# 001010b: SCK9 011101b: TOC2 100100b: SCK11 101100b: SCK011
PB6PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC3D 0011b: TIOCA5 1010b: RXD9/SMISO9/SSCL9	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 001010b: RXD9/SMISO9/SSCL9 100100b: RXD11/SMISO11/ SSCL11 101100b: RXD011/SMISO011/ SSCL011

Register	Bit	RX210 (n = 0 to 7)	RX660 (n = 0 to 7)
PB7PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC3B 0011b: TIOCB5 1010b: TXD9/SMOSI9/SSDA9	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 001010b: TXD9/SMOSI9/SSDA9 100100b: TXD11/SMOSI11/ SSDA11 101100b: TXD011/SMOSI011/ SSDA011
PBnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB1: IRQ4-DS (145/144/100/80/69/64/48-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB0: IRQ12 (144/100/80/64/48-pin) PB1: IRQ4-DS (144/100/80/64/48-pin) PB2: IRQ2 (144/100/80-pin) PB3: IRQ3 (144/100/80/64/48-pin) PB4: IRQ4 (144/100/80-pin) PB5: IRQ13 (144/100/80/64/48-pin) PB6: IRQ6 (144/100/80/64-pin) PB7: IRQ15 (144/100/80/64-pin)

Table 2.53 Comparison of PCn Pin Function Control Register (PCnPFS)

Register	Bit	RX210 (n = 0 to 7)	RX660 (n = 0 to 7)
PC0PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC3C 0011b: TCLKC 1011b: CTS5#/RTS5#/SS5# 1101b: SSLA1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 001011b: CTS5#/RTS5#/SS5# 001101b: SSLA1 101100b: RXD011/SMISO011/ SSCL011
PC1PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC3A 0011b: TCLKD 1010b: SCK5 1101b: SSLA2	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 001010b: SCK5 001101b: SSLA2 101100b: TXD011/SMOSI011/ SSDA011/TXDA011
PC2PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC4B 0011b: TCLKA 1010b: RXD5/SMISO5/SSCL5 1101b: SSLA3	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 001010b: RXD5/SMISO5/SSCL5 001101b: SSLA3 101100b: TXDB011

Register	Bit	RX210 (n = 0 to 7)	RX660 (n = 0 to 7)
PC3PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 01010b: TXD5/SMOSI5/SSDA5	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 001010b: TXD5/SMOSI5/SSDA5 100110b: PMC0
PC4PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC3D 0010b: MTCLKC 0101b: TMCI1 0111b: POE0# 1010b: SCK5 1011b: CTS8#/RTS8#/SS8# 1101b: SSLA0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKC 000101b: TMCI1 000111b: POE0# 001000b: MTIOC0A 001010b: SCK5 001011b: CTS8#/RTS8#/SS8# 001101b: SSLA0 100100b: CTS10#/RTS10#/SS10# 100110b: PMC0 101100b: CTS010#/RTS010#/ SS010# 101110b: DE010
PC5PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC3B 0010b: MTCLKD 0101b: TMRI2 1010b: SCK8 1101b: RSPCKA	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKD 000101b: TMRI2 001000b: MTIOC0C 001010b: SCK8 001101b: RSPCKA 100100b: SCK10 100110b: PMC0 101100b: SCK010
PC6PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC3C 0010b: MTCLKA 0101b: TMCI2 1010b: RXD8/SMISO8/SSCL8 1101b: MOSIA	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTCLKA 000101b: TMCI2 001010b: RXD8/SMISO8/SSCL8 001101b: MOSIA 011101b: TIC0 100100b: RXD10/SMISO10/ SSCL10 101100b: RXD010/SMISO010/ SSCL010

Register	Bit	RX210 (n = 0 to 7)	RX660 (n = 0 to 7)
PC7PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC3A 0010b: MTCLKB 0101b: TMO2 0111b: CACREF 1010b: TXD8/SMOSI8/SSDA8 1101b: MISOA	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKB 000101b: TMO2 000111b: CACREF 001010b: TXD8/SMOSI8/SSDA8 001101b: MISOA 011101b: TOC0 100100b: TXD10/SMOSI10/ SSDA10 101100b: TXD010/SMOSI010/ SSDA010
PCnPFS	ISEL	—	Interrupt input function select bit

Table 2.54 Comparison of PDn Pin Function Control Register (PDnPFS)

Register	Bit	RX210 (n = 0 to 7)	RX660 (n = 0 to 7)
PD0PFS	—	—	PD0 pin function select bits
PD1PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC4B	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 001000b: POE0# 010000b: CTX0
PD2PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC4D	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 010000b: CRX0 011101b: TIC2
PD3PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0111b: POE8#	Pin function select bits 000000b: Hi-Z 000111b: POE8# 001000b: MTIOC8D 011101b: TOC2
PD4PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0111b: POE3#	Pin function select bits 000000b: Hi-Z 000111b: POE11# 001000b: MTIOC8B
PD5PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIC5W 0111b: POE2#	Pin function select bits 000000b: Hi-Z 000001b: MTIC5W 000111b: POE10# 001000b: MTIOC8C

Register	Bit	RX210 (n = 0 to 7)	RX660 (n = 0 to 7)
PD6PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIC5V 0111b: POE1#	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000111b: POE4# 001000b: MTIOC8A
PDnPFS	ASEL	—	Analog function select bit

Table 2.55 Comparison of PEn Pin Function Control Register (PEnPFS)

Register	Bit	RX210 (n = 0 to 7)	RX660 (n = 0 to 7)
PE0PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 1100b: SCK12	Pin function select bits 000000b: Hi-Z 001000b: MTIOC3D 001100b: SCK12
PE1PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC4C 1100b: TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 001000b: MTIOC3B 001100b: TXD12/TXDX12/ SIOX12S/MOSI12/ SSDA12
PE2PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC4A 1100b: RXD12/RXDX12/ SMISO12/SSCL12	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 001000b: MTIOC7A 001100b: RXD12/RXDX12/ SMISO12/SSCL12 011101b: TIC3
PE3PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC4B 0111b: POE8# 1100b: CTS12#/RTS12#/SS12#	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000111b: POE8# 001000b: MTIOC1B 001100b: CTS12#/RTS12#/SS12# 011101b: TOC3
PE4PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC4D 0010b: MTIOC1A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000010b: MTIOC1A 001000b: MTIOC4A 100111b: MTIOC7D
PE5PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC4C 0010b: MTIOC2B	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000010b: MTIOC2B 011110b: COMP0

Register	Bit	RX210 (n = 0 to 7)	RX660 (n = 0 to 7)
PE6PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 1011b: CTS4#/RTS4#/SS4#	Pin function select bits 000000b: Hi-Z 001000b: MTIOC6C 001011b: CTS4#/RTS4#/SS4# 011101b: TIC1
PE7PFS	PSEL[5:0]	—	PE7 pin function select bits
PEnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE2: IRQ7-DS (145/144/100/80/69/64/48-pin) PE5: IRQ5 (145/144/100/80/69/64-pin) PE6: IRQ6 (145/144/100-pin) PE7: IRQ7 (145/144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE0: IRQ8 (144/100/80/64-pin) PE1: IRQ9 (144/100/80/64/48-pin) PE2: IRQ7-DS (144/100/80/64/48-pin) PE3: IRQ11 (144/100/80/64/48-pin) PE4: IRQ12 (144/100/80/64/48-pin) PE5: IRQ5 (100/80/64-pin) PE6: IRQ6 (144/100-pin) PE7: IRQ7 (144/100-pin)
	ASEL	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin PE0: AN008 (145/144/100/80/69/64-pin) PE1: AN009, CMPB0 (145/144/100/80/69/64/48-pin) PE2: AN010, CVREFB0 (145/144/100/80/69/64/48-pin) PE3: AN011, CMPA1 (145/144/100/80/69/64/48-pin) PE4: AN012, CMPA2 (145/144/100/80/69/64/48-pin) PE5: AN013 (145/144/100/80/69/64-pin) PE6: AN014 (145/144/100-pin) PE7: AN015 (145/144/100-pin)	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin PE0: AN008 (144/100/80/64-pin) PE1: AN009 (144/100/80/64/48-pin) PE2: AN010 (144/100/80/64/48-pin) PE3: AN011 (144/100/80/64/48-pin) PE4: AN012 (144/100/80/64/48-pin) PE5: AN013 (144/100/80/64-pin) PE6: AN014 (144/100-pin) PE7: AN015 (144/100-pin)

Table 2.56 Comparison of PHn Pin Function Control Register (PHnPFS)

Register	Bit	RX210 (n = 0 to 3)	RX660 (n = 0 to 3)
PH0PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0111b: CACREF	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000111b: CACREF 001001b: ADTRG0#
PH1PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0101b: TMO0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000101b: TMO0 001001b: ADST0 011101b: TIC1
PH2PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0101b: TMRI0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000101b: TMRI0 011001b: TOC1
PH3PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0101b: TMCI0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000101b: TMCI0

Table 2.57 Comparison of PJn Pin Function Control Register (PJnPFS)

Register	Bit	RX210 (n = 1, 3)	RX660 (n = 1, 3, 5)
PJ3PFS	PSEL[3:0] (RX210) PSEL[5:0] (RX660)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC3C 1010b: CTS0#/RTS0#/SS0# 1011b: CTS6#/RTS6#/SS6#	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 001010b: CTS6#/RTS6#/SS6# 001011b: CTS0#/RTS0#/SS0#
PJ5PFS	PSEL[5:0]	—	PJ5 pin function select bits
PJnPFS	ISEL	—	Interrupt input function select bit

Table 2.58 Comparisons of Multi-Function Pin Controller Registers

Register	Bit	RX210	RX660
PFCSE	CS0E	CS0 enable bit of PC7 0: Configures PC7 as an I/O port. 1: Configures PC7 as the CS0# signal.	CS0 enable bit 0: Disables CS0# output. 1: Enables CS0# output.
	CS1E	CS1 enable bit of PC6 0: Configures PC6 as an I/O port. 1: Configures PC6 as the CS1# signal.	CS1 enable bit 0: Disables CS1# output. 1: Enables CS1# output.
	CS2E	CS2 enable bit of P26 0: Configures P26 as an I/O port. 1: Configures P26 as the CS2# signal.	CS2 enable bit 0: Disables CS2# output. 1: Enables CS2# output.
	CS3E	CS3 enable bit of P27 0: Configures P27 as an I/O port. 1: Configures P27 as the CS3# signal.	CS3 enable bit 0: Disables CS3# output. 1: Enables CS3# output.
	CS4E	CS0 enable bit of P24	—
	CS5E	CS1 enable bit of P25	—
	CS6E	CS2 enable bit of PC5	—
	CS7E	CS3 enable bit of PC4	—
PFCSS0	—	—	CS output pin select register 0
PFAOE1	A21E	Address A21 output enable bit	—
	A22E	Address A22 output enable bit	—
	A23E	Address A23 output enable bit	—
PFBCR0	ADRHMS	—	A16 to A20 output enable bit
	ADRHMS2	—	A16 to A20 output enable 2 bit
	BCLKO	—	BCLK forced output bit
PFBCR1	ALEOE	ALE output enable bit 0: Configures P54 as an I/O port. 1: Configures P54 as the ALE pin.	ALE output enable bit 0: Disables ALE pin output. 1: Enables ALE pin output.
PFBCR2	—	—	External bus control register 2
PFBCR3	—	—	External bus control register 3

2.18 Multi-Function Timer Pulse Unit 2 and Multi-Function Timer Pulse Unit 3

Table 2.59 is a comparative overview of multi-function timer pulse unit 2 and multi-function timer pulse unit 3, and Table 2.60 is a comparison of multi-function timer pulse unit 2 and multi-function timer pulse unit 3 registers.

Table 2.59 Comparative Overview of Multi-Function Timer Pulse Unit 2 and Multi-Function Timer Pulse Unit 3

Item	RX210 (MTU2a)	RX660 (MTU3a)
Pulse input/output	Max. 16 lines	Max. 28 lines
Pulse input	3 lines	3 lines
Count clocks	Seven or eight clocks for each channel (four clocks for MTU5)	11 clocks for each channel (14 for MTU0, 12 for MTU2, 10 for MTU5, and four each for MTU1 and MTU2 (when LWA = 1))
Available operations	[MTU0 to MTU4] • Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Simultaneous register input/output by synchronous counter operation • Up to 12-phase PWM output in combination with synchronous operation	[MTU0 to MTU4, MTU6, MTU7, MTU8] • Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) (excluding MTU8) • Simultaneous clearing by compare match or input capture (excluding MTU8) • Simultaneous register input/output by synchronous counter operation (excluding MTU8) • Up to 12-phase PWM output in combination with synchronous operation (excluding MTU8)
	[MTU0, MTU3, MTU4] • Ability to specify buffer operation • AC synchronous motor (brushless DC motor) drive mode using complementary PWM output or reset-synchronized PWM output can be specified, and two types of waveform output (chopping and level) can be selected.	[MTU0, MTU3, MTU4, MTU6, MTU7, MTU8] • Ability to specify buffer operation
	[MTU1, MTU2] • Independent specification of phase counting mode • Cascade connection operation	[MTU1, MTU2] • Independent specification of phase counting mode • Ability to specify 32-bit phase counting mode linked to MTU1 or MTU2 (when TMDR3.LWA = 1) • Cascade connection operation

Item	RX210 (MTU2a)	RX660 (MTU3a)
Available operations	—	[MTU3, MTU4, MTU6, MTU7] • Ability to produce 12-phase waveform output, comprising six phases each of positive and negative output, in complementary PWM or reset PWM mode, through linked operation of MTU3 or MTU4 and MTU6 or MTU7 • In complementary PWM mode, ability to transfer data from the buffer register to a temporary register at peaks or troughs of the timer counter or when writes to the buffer register (MTU4.TGRD or MTU7.TGRD) occur • Ability to specify double buffer function in complementary PWM mode
	[MTU3, MTU4] Ability to produce six-phase waveform output, including three phases each for positive and negative complementary PWM or reset PWM output, by interlocking operation	[MTU3, MTU4] Through linked operation with MTU0, ability to specify the AC synchronous motor (brushless DC motor) drive mode using complementary PWM or reset PWM and to select two types (chopping or level) of waveform output
	[MTU5] Dead time compensation counter	[MTU5] Can be used as a dead time compensation counter.
	—	[MTU0/MTU5, MTU1, MTU2, MTU8] Ability to use the MTU1 and MTU2 in combination and specify 32-bit phase counting mode linked to the MTU0 or MTU5 and MTU8
Interrupt skipping function	Complementary PWM mode • Interrupts at counter peak or trough • A/D converter conversion start trigger skipping function	Ability to skip interrupts at counter peak or trough and A/D converter conversion start triggers in complementary PWM mode
Interrupt sources	28 sources	43 sources
Buffer operation	Automatic transfer of register data	Automatic transfer of register data (transfer from buffer register to timer register)
Trigger generation	Ability to generate A/D converter start trigger	• Ability to generate A/D converter start trigger • Ability to start A/D conversion at user-specified timing using A/D conversion start request delay function, and ability to synchronize operation with PWM output
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Table 2.60 Comparison of Multi-Function Timer Pulse Unit 2 and 3 Registers

Register	Bit	RX210 (MTU2a)	RX660 (MTU3a)
TCR2	—	—	Timer control register 2
TMDR (RX210) TMDR1 (RX660)	—	Timer mode register	Timer mode register 1
TMDR2A TMDR2B	—	—	Timer mode register 2
TMDR3	—	—	Timer mode register 3
TIER	TTGE2	A/D converter start request enable 2 bit 0: A/D converter start request generation by MTU4.TCNT underflow (trough) is disabled. 1: A/D converter start request generation by MTU4.TCNT underflow (trough) is enabled.	A/D converter start request enable 2 bit 0: A/D converter start request generation by MTUn.TCNT underflow (trough) is disabled. 1: A/D converter start request generation by MTUn.TCNT underflow (trough) is enabled.
TSYCR	—	—	Timer synchronous clear register
TADCR	—	Timer A/D converter start request control register	—
TADCORA/ TADCORB	—	Timer A/D converter start request cycle set registers A and B	—
TADCOBRA/ TADCOBRB	—	Timer A/D converter start request cycle set buffer registers A and B	—
TCNTLW	—	—	Timer longword counter
TGRALW/TGRBLW	—	—	Timer longword general registers
TSTR (RX210) TSTR/TSTRA/ TSTRB (RX660)	CST8	—	Counter start 8 bit
TSYR (RX210) TSYRm (RX660)	—	Timer synchronous register	Timer synchronous register m (m = A, B)
TCSYSTR	—	—	Timer counter synchronous start register
TRWER (RX210) TRWERm (RX660)	—	Timer read/write enable register	Timer read/write enable register m (m = A, B)
TOER (RX210) TOERm (RX660)	—	Timer output master enable register	Timer output master enable register m (m = A, B)
TOCR1 (RX210) TOCR1m (RX660)	—	Timer output control register 1	Timer output control register 1 m (m = A, B)
TOCR2 (RX210) TOCR2m (RX660)	—	Timer output control register 2	Timer output control register 2 m (m = A, B)
TOLBR TOLBRm (RX660)	—	Timer output level buffer register	Timer output level buffer register m (m = A, B)
TGCR (RX210) TGCRA(RX660)	—	Timer gate control register	Timer gate control register A
TCNTS (RX210) TCNTSm (RX660)	—	Timer subcounter	Timer subcounter m (m = A, B)
TCDR (RX210) TCDRm (RX660)	—	Timer cycle data register	Timer cycle data register m (m = A, B)
TCBR (RX210) TCBRm (RX660)	—	Timer cycle buffer register	Timer cycle buffer register m (m = A, B)
TDDR (RX210) TDDRm (RX660)	—	Timer dead time data register	Timer dead time data register m (m = A, B)

Register	Bit	RX210 (MTU2a)	RX660 (MTU3a)
TITCR (RX210) TITCR1m (RX660)	—	Timer interrupt skipping set register	Timer interrupt skipping set register 1 m (m = A, B)
TITCNT (RX210) TITCNT1m (RX660)	—	Timer interrupt skipping counter	Timer interrupt skipping counter 1 m (m = A, B)
TBTER (RX210) TBTERm (RX660)	—	Timer buffer transfer set register	Timer buffer transfer set register m (m = A, B)
TDER (RX210) TDERm (RX660)	—	Timer dead time enable register	Timer dead time enable register m (m = A, B)
TWCR (RX210) TWCRB (RX660)	SCC	—	Synchronous clearing control bit
NFCR (RX210) NFCRn (RX660)	—	Noise filter control register	Noise filter control register n (n = 0 to 4, 6, 7, 8, C)
NFCR5	—	—	Noise filter control register 5
TITMRA/TITMRB	—	—	Timer interrupt skipping mode registers
TITCR2A/TITCR2B	—	—	Timer interrupt skipping set registers 2
TITCNT2A/ TITCNT2B	—	—	Timer interrupt skipping counters 2

2.19 Port Output Enable 2 and Port Output Enable 3

Table 2.61 is a comparative overview of port output enable 2 and port output enable 3, and Table 2.62 is a comparison of port output enable 2 and port output enable 3 registers.

Table 2.61 Comparative Overview of Port Output Enable 2 and Port Output Enable 3

Item	RX210 (POE2a)	RX660 (POE3a)
Pin status while output is disabled	High-impedance	High-impedance
High-impedance control target pins	• MTU output pins — MTU0 pin (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) — MTU3 pin (MTIOC3B, MTIOC3D) — MTU4 pin (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D)	• MTU output pins — MTU0 pin (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) — MTU3 pin (MTIOC3B, MTIOC3D) — MTU4 pin (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) — MTU6 pin (MTIOC6B, MTIOC6D) — MTU7 pin (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D)
Conditions for generating high-impedance request	• Input pin changes When signal input occurs on pin POE0# to POE3# and POE8#. • Short circuit of output pins: A match (short circuit) of output signal levels (active level) lasting one or more cycles on one of the combinations of pins listed below [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D • Making of SPOER register setting • Detection of stopped oscillation on main clock oscillator	• Input pin changes When signal input occurs on pin POE0#, POE4#, POE8#, POE10#, or POE11# • Short circuit of output pins: A match (short circuit) of output signal levels (active level) lasting one or more cycles on one of the combinations of pins listed below [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D — MTIOC6B and MTIOC6D — MTIOC7A and MTIOC7C — MTIOC7B and MTIOC7D • Making of SPOER register setting • Detection of stopped oscillation on main clock oscillator

Item	RX210 (POE2a)	RX660 (POE3a)
Functions	• Each of the POE0# to POE3# and POE8# input pins can be set for falling edge, PCLK/8 × 16, PCLK/16 × 16, or PCLK/128 × 16 low-level sampling. • The MTU complementary PWM output pins can be put in the high-impedance state by the falling edge or low-level sampling of the POE0# to POE3# pins. • The MTU0 output pins can be put in the high-impedance state by the falling edge or low-level sampling of the POE8# pin. • The MTU complementary PWM output pins and MTU0 output pins can be put in the high-impedance state by detection of clock generator oscillation stop. • The MTU complementary PWM output pins can be put in the high-impedance state when the output levels of MTU complementary PWM output pins are compared and simultaneous active-level output continues for one PCLK clock cycle or more. • The MTU complementary PWM output pins and MTU0 output pins can be put in the high-impedance state each time a write to the POE register occurs. • Interrupts can be generated by input-level sampling of the POE0# to POE3# and POE8# input pins or the results of output-level comparison with the MTU complementary PWM output pins.	• Falling-edge detection or sampling of the low level 16 times at PCLK/8, PCLK/16, or PCLK/128 can be set for each of the POE0#, POE4#, POE8#, POE10#, and POE11# input pins. • Output on all control target pins can be placed in the high-impedance state on detection of falling edges or sampling of the low level on the POE0#, POE4#, POE8#, POE10#, and POE11# pins. • Output on all control target pins can be placed in the high-impedance state when oscillation by the clock generation circuit stops. • It is possible to compare levels output on pins for complementary PWM output from the MTU, and when simultaneous output of the active level continues for one or more cycles, output on the pins can be placed in the high-impedance state. • Output on all control target pins can be placed in the high-impedance state by modifying settings of POE3 registers. • Interrupts can be generated in response to the results of input level sampling or output-level comparison.

Table 2.62 Comparison of Port Output Enable 2 and Port Output Enable 3 Registers

Register	Bit	RX210 (POE2a)	RX660 (POE3a)
ICSR1	POE1M[1:0]	POE1 mode select bits	—
	POE2M[1:0]	POE2 mode select bits	—
	POE3M[1:0]	POE3 mode select bits	—
	POE1F	POE1 flag	—
	POE2F	POE2 flag	—
	POE3F	POE3 flag	—
ICSR2	POE8M[1:0]	POE8 mode select bits	—
	POE4M[1:0]	—	POE4 mode select bits
	POE8E	POE8 high-impedance enable bit	—
	POE8F	POE8 flag	—
	POE4F	—	POE4 flag
ICSR3	OSTSTE	OSTST high-impedance enable bit	—
	OSTSTF	OSTST high-impedance flag	—
	POE8M[1:0]	—	POE8 mode select bits
	PIE3	—	Port interrupt enable 3 bit
	POE8E	—	POE8 high-impedance enable bit
	POE8F	—	POE8 flag
ICSR4	—	—	Input level control/status register 4
ICSR5	—	—	Input level control/status register 5
ICSR6	—	—	Input level control/status register 6
OCSR2	—	—	Output level control/status register 2
ALR1	—	—	Active level register 1
SPOER	CH34HIZ (RX210) MTUCH34HIZ (RX660)	MTU3 and MTU4 output high-impedance enable bit	MTU3 and MTU4 pin high-impedance enable bit
	MTUCH67HIZ	—	MTU6 and MTU7 pin high-impedance enable bit
	CH0HIZ (RX210) MTUCH0HIZ (RX660)	MTU0 output high-impedance enable bit (b1)	MTU0 pin high-impedance enable bit (b2)
POECR1	PE0ZE (RX210) MTU0AZE (RX660)	MTIOC0A high-impedance enable bit	MTIOC0A pin high-impedance enable bit
	PE1ZE MTU0BZE (RX660)	MTIOC0B high-impedance enable bit	MTIOC0B pin high-impedance enable bit
	PE2ZE MTU0CZE (RX660)	MTIOC0C high-impedance enable bit	MTIOC0C pin high-impedance enable bit
	PE3ZE MTU0DZE (RX660)	MTIOC0D high-impedance enable bit	MTIOC0D pin high-impedance enable bit

Register	Bit	RX210 (POE2a)	RX660 (POE3a)
POECR2	—	Port output enable control register 2 POECR2 is an 8-bit register.	Port output enable control register 2 POECR2 is a 16-bit register.
	MTU7BDZE	—	MTIOC7B/MTIOC7D pin high-impedance enable bit
	MTU7ACZE	—	MTIOC7A/MTIOC7C pin high-impedance enable bit
	MTU6BDZE	—	MTIOC6B/MTIOC6D pin high-impedance enable bit
	P3CZEA (RX210) MTU4BDZE (RX660)	MTU port 3 high-impedance enable bit (b4)	MTIOC4B/MTIOC4D pin high-impedance enable bit (b8)
	P2CZEA (RX210) MTU4ACZE (RX660)	MTU port 2 high-impedance enable bit (b5)	MTIOC4A/MTIOC4C pin high-impedance enable bit (b9)
	P1CZEA (RX210) MTU3BDZE (RX660)	MTU port 1 high-impedance enable bit (b6)	MTIOC3B/MTIOC3D pin high-impedance enable bit (b10)
POECR4	—	—	Port output enable control register 4
POECR5	—	—	Port output enable control register 5
ICSR3	—	Input level control/status register 3	—
M0SELR1	—	—	MTU0 pin select register 1
M0SELR2	—	—	MTU0 pin select register 2
M3SELR	—	—	MTU3 pin select register
M4SELR1	—	—	MTU4 pin select register 1
M4SELR2	—	—	MTU4 pin select register 2

2.20 8-Bit Timer

Table 2.63 is a comparative overview of 8-bit timers, and Table 2.64 is a comparison of 8-bit timer registers.

Table 2.63 Comparative Overview of 8-Bit Timers

Item	RX210 (TMR)	RX660 (TMRb)
Count clocks	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External count clock	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock: External count clock
Number of channels	(8 bits × 2 channels) × 2 units	(8 bits × 2 channels) × 2 units
Compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selectable among compare match A or B, or an external reset signal.	Selectable among compare match A or B, or an external counter reset signal.
Timer output	Output pulses with a user-defined duty cycle or PWM output	Output pulses with a user-defined duty cycle or PWM output
Cascading of two channels	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
Event link function (output)	Compare match A, compare match B, and overflow (TMR0, TMR2)	Compare match A, compare match B, and overflow (TMR0 to TMR3)
Event link function (input)	Ability to perform one of three actions according to accepted event (1) Counter start (TMR0, TMR2) (2) Event counter (TMR0, TMR2) (3) Counter restart (TMR0, TMR2)	Ability to perform one of three actions according to accepted event (1) Counter start (TMR0 to TMR3) (2) Event counter (TMR0 to TMR3) (3) Counter restart (TMR0 to TMR3)
Generation of trigger to start A/D converter	—	Compare match A of TMR0 or TMR2
DTC activation	The DTC can be activated by compare match A interrupts or compare match B interrupts.	The DTC can be activated by compare match A interrupts or compare match B interrupts.
Generation of baud rate clock for SCI	Generation of baud rate clock for SCI	Generation of SCI basic clock
Generation of REMC operation clock	—	Generation of REMC (remote control signal receiver) operation clock
Low power consumption function	Ability to transition each unit to the module stop state	Ability to transition each unit to the module stop state

Table 2.64 Comparison of 8-Bit Timer Registers

Register	Bit	RX210 (TMR)	RX660 (TMRb)
TCSR	ADTE	—	A/D trigger enable bit

2.21 Realtime Clock

Table 2.65 is a comparative overview of realtime clocks, and Table 2.66 is a comparison of realtime clock registers.

Table 2.65 Comparative Overview of Realtime Clocks

Item	RX210 (RTCb)	RX660 (RTCC)
Count modes	Calendar count mode	Calendar count mode/binary count mode
Count source	Sub-clock (XCIN)	Sub-clock (XCIN)
Clock and calendar functions	• Year, month, date, day-of-week, hour, minute, second are counted, BCD display • 12 hours/24 hours mode switching function • 30-second adjustment function (Fewer than 30 seconds is rounded down to 00 seconds, and 30 seconds or more is rounded up to one minute.) • Automatic leap year adjustment function • Start/stop function • The status (1 Hz, 2 Hz, 4Hz, 8Hz, 16Hz, 32Hz, or 64Hz) is displayed in binary units. • Time error adjustment function • 1 Hz clock output	• Calendar count mode — Year, month, date, day-of-week, hour, minute, second are counted, BCD display — 12 hours/24 hours mode switching function — 30 seconds adjustment function (a number less than 30 is rounded down to 00 seconds, and 30 seconds or more are rounded up to one minute) — Automatic adjustment function for leap years • Binary count mode Count seconds in 32 bits, binary display • Common to both modes — Start/stop function — The sub-second digit is displayed in binary units (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, or 64 Hz). — Clock error correction function — Clock (1 Hz/64 Hz) output
Interrupts	• Alarm interrupt (ALM) Year, month, date, day of the week, hour, minute, or second can be selected as the condition for the alarm interrupt. • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second can be selected as an interrupt period.	• Alarm interrupt (ALM) As an alarm interrupt condition, selectable which of the below is compared with: — Calendar count mode: Year, month, date, day-of-week, hour, minute, or second — Binary count mode: Each bit of the 32-bit binary counter • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second can be selected as an interrupt period.

Item	RX210 (RTCb)	RX660 (RTCC)
Interrupt	• Carry interrupt (CUP) Indicates occurrence of a carry to the seconds counter or a carry to the 64 Hz counter during reading of the 64 Hz counter. • Recovery from software standby mode or deep software standby mode can be performed by an alarm interrupt or periodic interrupt.	• Carry interrupt (CUP) An interrupt is generated at either of the following timings: — When a carry from the 64 Hz counter to the second counter is generated. — When the 64-Hz counter is changed and the R64CNT register is read at the same time. • Recovery from software standby mode or deep software standby mode can be performed by an alarm interrupt or periodic interrupt
Time-capture function	The times when any of three event signals are input can be captured. The month, date, hour, minute, and second are captured for each event.	Times when the edge of the time capture event input pin is detected can be captured. For every event input, the month, date, hour, minute, and second, or the 32-bit binary counter value, is captured.
Event link function	Periodic event output	Periodic event output

Table 2.66 Comparison of Realtime Clock Registers

Register	Bit	RX210 (RTCb)	RX660 (RTCBa)
RCR1	RTCOS	—	RTCOUT output select bit
RCR2	CNTMD	—	Count mode select bit
RCR3	RTCEN	Sub-Clock Oscillator Control bit 0: Sub-clock oscillator is stopped. 1: Sub-clock oscillator is operating..	RTC Enable bit 0: RTC disabled 1: RTC enabled
	RTCDV[2:0]	Sub-Clock Oscillator Drive Capacity Control bit	—
RCR4	—		RTC control register 4
BCNT0*1	—	—	Binary counter 0
BCNT1*1	—	—	Binary counter 1
BCNT2*1	—	—	Binary counter 2
BCNT3*1	—	—	Binary counter 3
BCNT0AR*1	—	—	Binary counter 0 alarm register
BCNT1AR*1	—	—	Binary counter 1 alarm register
BCNT2AR*1	—	—	Binary counter 2 alarm register
BCNT3AR*1	—	—	Binary counter 3 alarm register
BCNT0AER*1	—	—	Binary counter 0 alarm enable register
BCNT1AER*1	—	—	Binary counter 1 alarm enable register
BCNT2AER*1	—	—	Binary counter 2 alarm enable register
BCNT3AER*1	—	—	Binary counter 3 alarm enable register

Note: 1. In binary count mode.

2.22 Watchdog Timer

Table 2.67 is a comparative overview of the watchdog timers, and Table 2.68 is a comparison of watchdog timer registers.

Table 2.67 Comparative Overview of Watchdog Timers

Item	RX210 (WDTA)	RX660 (WDTA)
Count source	Peripheral clock (PCLK)	Peripheral clock (PCLK)
Clock division ratio	Divide by 4, 64, 128, 512, 2048, or 8192	Divide by 4, 64, 128, 512, 2048, or 8192
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Counting automatically starts after a reset (auto-start mode) • Counting is started by refreshing the WDTRR register (writing 00h and then FFh) (register start mode)	• Auto-start mode: Counting starts automatically after a reset. • Register start mode: Counting is started by refreshing the counter (writing 00h and then FFh to the WDTRR register).
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error is generated Counting restarts (in auto-start mode, counting automatically restarts after a reset or after a non-maskable interrupt request is output. In register start mode, counting restarts after refreshing.)	• Reset (the down-counter and other registers return to their initial values) • Low power consumption state (by means of register setting) • Underflow or refresh error (register start mode only)
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Reset output sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read by the WDTSR register.	The down-counter value can be read by the WDTSR register.

Table 2.68 Comparison of Watchdog Timer Registers

Register	Bit	RX210 (WDTA)	RX660 (WDTA)
WDTRCR	RSTIRQS	Reset interrupt request selection bit 0: Non-maskable interrupt request output is enabled 1: Reset output is enabled	Reset interrupt request selection bit 0: Non-maskable interrupt request output or interrupt request output is enabled 1: Reset output is enabled

2.23 Independent Watchdog Timer

Table 2.69 is a comparative overview of the independent watchdog timers, and Table 2.70 is a comparison of independent watchdog timer registers.

Table 2.69 Comparative Overview of Independent Watchdog Timers

Item	RX210 (IWDTa)	RX660 (IWDTa)
Count source	IWDT-dedicated clock (IWDTCLK)	IWDT-dedicated clock (IWDTCLK)
Clock division ratio	Divide by 1, 16, 32, 64, 128, or 256	Divide by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Counting automatically starts after a reset (auto-start mode) • Counting is started by refreshing the IWDTRR register (writing 00h and then FFh) (register start mode)	• Auto-start mode: Counting starts automatically after a reset. • Register start mode: Counting is started by refreshing the counter (writing 00h and then FFh to the IWDTRR register).
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error is generated Counting restarts (in auto-start mode, counting automatically restarts after a reset or after a non-maskable interrupt request is output. In register start mode, counting restarts after refreshing.)	• Reset (the down-counter and other registers return to their initial values) • Low power consumption state (by means of register setting) • Underflow or refresh error (register start mode only)
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Reset output sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt/interrupt sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read by the IWDTSR register.	The down-counter value can be read by the IWDTSR register.
Event link function (output)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflow event output • Refresh error event output
Output signals (internal signals)	• Reset output • Interrupt request output • Sleep mode count stop control output	• Reset output • Interrupt request output • Sleep mode count stop control output

Item	RX210 (IWDTa)	RX660 (IWDTa)
Auto-start mode (controlled by option function select register 0 (OFS0))	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the watchdog timer (OFS0.IWDTRPSS[1:0]bits) • Selecting the window end position in the watchdog timer (OFS0.IWDTRPES[1:0]bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0]bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0]bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)
Register start mode (controlled by the IWDT registers)	• Selecting the clock frequency division ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)	• Selecting the clock frequency division ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)

Table 2.70 Comparison of Independent Watchdog Timer Registers

Register	Bit	RX210 (IWDTa)	RX660 (IWDTa)
IWDTRCR	RSTIRQS	Reset interrupt request select bit 0: Non-maskable interrupt request output is enabled. 1: Reset output is enabled.	Reset interrupt request select bit 0: Non-maskable interrupt request or interrupt request output is enabled. 1: Reset output is enabled.

2.24 Serial Communications Interface

Table 2.71 is a comparative overview of the serial communications interfaces, and Table 2.72 is a comparison of serial communications interface channel specifications, and Table 2.73 is a comparison of serial communications interface registers.

Table 2.71 Comparative Overview of Serial Communications Interfaces

Item		RX210 (SCIc, SCId)	RX660 (SCIk, SCIm, SCIh)
Number of channels		• SCIc: 12 channels • SCId: 1 channel	• SCIk: 10 channels • SCIm: 2 channels • SCIh: 1 channel
Serial communications modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable as LSB first or MSB first transfer.	Selectable as LSB first or MSB first transfer.
I/O signal level inversion		—	The levels of input and output signals can be inverted independently.
Interrupt sources		• Transmit end, transmit data empty, receive data full, and receive error • Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)	• Transmit end, transmit data empty, receive data full, receive error, receive data ready (SCI10 and SCI11), and data match • Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)
Low power consumption function		Individual channels can be transitioned to the module stop state.	Individual channels can be transitioned to the module stop state.
Asynchronous mode	Data length	7 or 8 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection function	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.

Item		RX210 (SCIc, SCId)	RX660 (SCIk, SCIm, SCIh)
Asynchronous mode	Transmit/receive FIFO	—	Ability to use 16-stage FIFOs for transmission and reception (SCI10 and SCI11)
	Data match detection	—	Compares receive data and comparison data, and generates interrupt when they are matched
	Start-bit detection	—	Low level or falling edge is selectable.
	Receive data sampling timing adjustment	—	The receive data sampling point can be shifted from the center of the data forward or backward to a base point (SCI0 to SCI11).
	Transmit signal change timing adjustment	—	Either the falling or rising edge of the transmit data can be delayed (SCI0 to SCI11).
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly or by reading the SPTR.RXDMON flag.
	Clock source	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5, SCI6, and SCI12).	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5, SCI6, and SCI12).
	Double-speed mode	—	Baud rate generator double-speed mode is selectable.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	CTSn and RTSn pins can be used in controlling transmission/ reception.	CTSn# and RTSn# pins can be used in controlling transmission/ reception.
	Transmit/receive FIFO	—	Ability to use 16-stage FIFOs for transmission and reception (SCI10 and SCI11)
Smart card interface mode	Error processing	• An error signal can be automatically transmitted when detecting a parity error during reception • Data can be automatically retransmitted when receiving an error signal during transmission	• An error signal can be automatically transmitted when detecting a parity error during reception • Data can be automatically retransmitted when receiving an error signal during transmission
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.

Item		RX210 (SCIc, SCId)	RX660 (SCIk, SCIm, SCIh)
Simple I²C mode	Communication format	I²C bus format (MSB-first transfer only)	I²C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer rate	Up to 384 kbps	Fast mode is supported.
	Noise cancellation	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.
Extended serial mode (supported by SCI12 only)	Start frame transmission	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection
	Start frame reception	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two kinds of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two kinds of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates

Item		RX210 (SCIc, SCId)	RX660 (SCIk, SCIm, SCIh)
Extended serial mode (supported by SCI12 only)	I/O control function	• Ability to select polarity or TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select receive data sampling timing of RXDX12 pin • Signals received on RXDX12 can be passed through to SCIc when the extended serial mode control section is turned off.	• Ability to select polarity or TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select receive data sampling timing of RXDX12 pin
	Timer function	Usable as reloading timer	Usable as reloading timer
Bit rate modulation function			Correction of outputs from the on-chip baud rate generator can reduce errors.
Event link function (supported by SCI5 only)		• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output	• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output

Table 2.72 Comparison of Serial Communications Interface Channel Specifications

Item	RX210 (SCIc, SCId)	RX660 (SCIk, SCIm, SCIh)
Asynchronous mode	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6 SCI7, SCI8, SCI9, SCI10, SCI11, SCI12	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6 SCI7, SCI8, SCI9, SCI10, SCI11, SCI12
Clock synchronous mode	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6 SCI7, SCI8, SCI9, SCI10, SCI11, SCI12	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6 SCI7, SCI8, SCI9, SCI10, SCI11, SCI12
Smart card interface mode	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6 SCI7, SCI8, SCI9, SCI10, SCI11, SCI12	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6 SCI7, SCI8, SCI9, SCI10, SCI11, SCI12
Simple I^2C mode	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6 SCI7, SCI8, SCI9, SCI10, SCI11, SCI12	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6 SCI7, SCI8, SCI9, SCI10, SCI11, SCI12
Simple SPI mode	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6 SCI7, SCI8, SCI9, SCI10, SCI11, SCI12	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6 SCI7, SCI8, SCI9, SCI10, SCI11, SCI12
FIFO mode	—	SCI10, SCI11
Data match detection	—	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6 SCI7, SCI8, SCI9, SCI10, SCI11
Extended serial mode	SCI12	SCI12
TMR clock input	SCI5, SCI6, SCI12	SCI5, SCI6, SCI12
Event link function	SCI5	SCI5
Peripheral module clock	PCLKB: SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6 SCI7, SCI8, SCI9, SCI10, SCI11, SCI12	PCLKA: SCI10, SCI11 PCLKB: SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6 SCI7, SCI8, SCI9, SCI12

Table 2.73 Comparison of Serial Communications Interface Registers

Register	Bit	RX210 (SCIc, SCId)	RX660 (SCIk, SCIm, SCIh)
RDRH RDRL RDRHL	—	—	Receive data registers H, L, and HL
FRDR	—	—	Receive FIFO data register
TDRH TDRL TDRL	—	—	Transmit data registers H, L, and HL
FTDR	—	—	Transmit FIFO data register
SMR	CHR	Character length bit (Valid only in asynchronous mode.) 0: Transmit/receive in 8-bit data length 1: Transmit/receive in 7-bit data length	Character length bit (Valid only in asynchronous mode.) Selects in combination with the SCMR.CHR1 bit. CHR1 CHR 0 0: Transmit/receive in 9-bit data length 0 1: Transmit/receive in 9-bit data length 1 0: Transmit/receive in 8-bit data length (initial value) 1 1: Transmit/receive in 7-bit data length
	CM	Communications mode bit 0: Asynchronous mode 1: Clock synchronous mode	Communications mode bit 0: Asynchronous mode or simple I^2C mode 1: Clock synchronous mode or simple SPI mode
SCR	MPIE	Multi-processor interrupt enable bit (Valid in asynchronous mode when the SMR.MP bit is set to 1.) 0: Normal reception 1: When data with the multi-processor bit set to 0 is received, the data is not read, and setting the status flags ORER and FER in SSR to 1 is disabled. When data with the multiprocessor bit set to 1 is received, the MPIE bit is automatically cleared to 0, and normal reception resumes.	Multi-processor interrupt enable bit (Valid in asynchronous mode when the SMR.MP bit is set to 1.) 0: Normal reception 1: When data with the multi-processor bit set to 0 is received, the data is not read, and setting the status flags RDRF, ORER, and FER in the SSR register to 1 is disabled. When data with the multi-processor bit set to 1 is received, the MPIE bit is automatically cleared to 0, and normal reception resumes.
SSR (RX210) SSR/SSRFIFO (RX660)	—	Serial status register	Serial status register Non-smart card interface mode and FIFO mode (SCMR.SMIF = 0 and FCR.FM = 1)
	DR	—	Receive data ready flag
	RDF	—	Receive FIFO full flag
	TDFE	—	Transmit FIFO empty flag

Register	Bit	RX210 (SCIc, SCId)	RX660 (SCIk, SCIm, SCIh)
SCMR	CHR1	—	Character length bit 1
MDDR	—	—	Modulation duty register
SEMR	ITE	—	Immediate transmission enable bit
	BRME	—	Bit rate modulation enable bit
	ABCSE	—	Asynchronous mode base clock select extended bit
	BGDM	—	Baud rate generator double-speed mode select bit
	RXDESEL	—	Asynchronous start bit edge detection select bit
SPMR	MSS	Master slave select bit 0: TXDn pin: transmission, RXDn pin: reception (master mode) 1: TXDn pin: reception, RXDn pin: transmission (slave mode)	Master slave select bit 0: SMOSIn pin: transmission, SMISOn pin: reception (master mode) 1: SMOSIn pin: reception, SMISOn pin: transmission (slave mode)
FCR	—	—	FIFO control register
FDR	—	—	FIFO data count register
LSR	—	—	Line status register
CDR	—	—	Comparison data register
DCCR	—	—	Data comparison control register
SPTR	—	—	Serial port register
TMGR	—	—	Transmit/receive timing select register
CR2	BCCS[1:0]	Bus collision detection clock select bits b5 b4 0 0: SCI base clock 0 1: SCI base clock frequency divided by 2 1 0: SCI base clock frequency divided by 4 1 1: Setting prohibited.	Bus collision detection clock select bits • When SEMR.BGDM = 0, or SEMR.BGDM = 1 and SMR.CKS[1:0] = other than 00b b5 b4 0 0: Base clock 0 1: Base clock frequency divided by 2 1 0: Base clock frequency divided by 4 1 1: Setting prohibited. • When SEMR.BGDM = 1 and SMR.CKS[1:0] = 00b b5 b4 0 0: Base clock frequency divided by 2 0 1: Base clock frequency divided by 4 1 0: Setting prohibited. 1 1: Setting prohibited.

2.25 I²C bus Interface

Table 2.74 is a comparison of I²C bus interface registers.

Table 2.74 Comparison of I²C Bus Interface Registers

Register	Bit	RX210 (RIIC)	RX660 (RIICa)
ICCR1	SDAI	SDA line monitor bit 0: SDA0 line is low. 1: SDA0 line is high.	SDA line monitor bit (n = 0 or 2) 0: SDAn line is low. 1: SDAn line is high.
	SCLI	SCL line monitor bit 0: SCL0 line is low. 1: SCL0 line is high.	SCL line monitor bit (n = 0 or 2) 0: SCLn line is low. 1: SCLn line is high.
	SDAO	SDA output control/monitor bit Read 0: SDA0 pin driven low. 1: SDA0 pin released. Write 0: SDA0 pin driven low. 1: SDA0 pin released.	SDA output control/monitor bit (n = 0 or 2) Read 0: SDAn pin driven low. 1: SDAn pin released. Write 0: SDAn pin driven low. 1: SDAn pin released. (High-level output is achieved through an external pull-up resistor.)
	SCLO	SCL output control/monitor bit Read 0: SCL0 pin driven low. 1: SCL0 pin released. Write 0: SCL0 pin driven low. 1: SCL0 pin released. (High-level output is achieved through an external pull-up resistor.)	SCL output control/monitor bit (n = 0 or 2) Read 0: SCLn pin driven low. 1: SCLn pin released. Write 0: SCLn pin driven low. 1: SCLn pin released. (High-level output is achieved through an external pull-up resistor.)
	IICRST	I²C-bus interface internal reset bit 0: Releases RIIC reset or internal reset. 1: Initiates RIIC reset or internal reset. (Clears the bit counter and the SCL0/SDA0 output latch.)	I²C-bus interface internal reset bit (n = 0 or 2) 0: Releases RIIC reset or internal reset. 1: Initiates RIIC reset or internal reset. (Clears the bit counter and the SCLn/SDAn output latch.)

Register	Bit	RX210 (RIIC)	RX660 (RIICa)
ICCR1	ICE	I²C-bus interface enable bit 0: Disabled (SCL0 and SDA0 pins in inactive state). 1: Enabled (SCL0 and SDA0 pins in active state). (Combined with the IICRST bit to select either RIIC or internal reset.)	I²C-bus interface enable bit (n = 0 or 2) 0: Disabled (SCLn and SDAn pins in inactive state). 1: Enabled (SCLn and SDAn pins in active state). (Combined with the IICRST bit to select either RIIC or internal reset.)
ICMR2	TMOL	Timeout L count control bit 0: Count-up is disabled while the SCL0 line is low. 1: Count-up is enabled while the SCL0 line is low.	Timeout L count control bit (n = 0 or 2) 0: Count-up is disabled while the SCLn line is low. 1: Count-up is enabled while the SCLn line is low.
	TMOH	Timeout H count control bit 0: Count-up is disabled while the SCL0 line is high. 1: Count-up is enabled while the SCL0 line is high.	Timeout H count control bit (n = 0 or 2) 0: Count-up is disabled while the SCLn line is high. 1: Count-up is enabled while the SCLn line is high.
ICMR3	RDRFS	RDRF flag set timing selection bit 0: The RDRF flag is set to 1 at the rising edge of the ninth SCL clock cycle. (The SCL0 line is not held low at the falling edge of the eighth clock cycle.) 1: The RDRF flag is set to 1 at the rising edge of the eighth SCL clock cycle. (The SCL0 line is held low at the falling edge of the eighth clock cycle.) Low-hold is released by writing a value to the ACKBT bit.	RDRF flag set timing selection bit 0: The RDRF flag is set to 1 at the rising edge of the ninth SCL clock cycle. (The SCLn line is not held low at the falling edge of the eighth clock pulse.) 1: The RDRF flag is set to 1 at the rising edge of the eighth SCL clock cycle. (The SCLn line is held low at the falling edge of the eighth clock pulse.) Low-hold is released by writing a value to the ACKBT bit.
TMOCNT	—	Timeout internal counter	—

2.26 Serial Peripheral Interface

Table 2.75 is a comparative overview of serial peripheral interfaces, and Table 2.76 is a comparison of serial peripheral interface registers.

Table 2.75 Comparative Overview of Serial Peripheral Interfaces

Item	RX210 (RSPI)	RX660 (RSPId)
Number of channels	1 channel	1 channel
RSPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Capable of serial communication in master/slave mode. • Communication modes: Full-duplex or simplex (transmit-only) can be selected. • Capable of switching the polarity of the serial transfer clock. • Capable of switching the phase of the serial transfer clock.	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Communication modes: Full-duplex or simplex (transmit-only) can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK
Data format	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits).	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits). • Byte swapping of transmit and receive data is selectable • Ability to invert the logic level of transmit/receive data
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the maximum divisor is 4096). • In slave mode, the externally input clock is used as the serial clock (the maximum frequency is that of PCLK divided by 8). — Width at high level: 4 cycles of PCLK — Width at low level: 4 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4). — Width at high level: 2 cycles of PCLK — Width at low level: 2 cycles of PCLK

Item	RX210 (RSPI)	RX660 (RSPId)
Buffer configuration	• Double buffer configuration for the transmit/receive buffers	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection
SSL control function	• Four SSL signals (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 signals are output. • In multi-master mode: SSLA0 signal for input, and SSLA1 to SSLA3 signals for either output or unused. • In slave mode: SSLA0 signal for input, and SSLA1 to SSLA3 signals for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) — Range:1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) — Range:1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity
Control in master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function • The delay between data bytes can be shortened during burst transfers.

Item	RX210 (RSPI)	RX660 (RSPId)
Interrupt sources	Maskable interrupt sources • RSPI receive interrupt (receive buffer full) • RSPI transmit interrupt (transmit buffer empty) • RSPI error interrupt (mode fault, overrun, or parity error) • RSPI idle interrupt (RSPI idle)	Interrupt sources • Receive buffer full interrupt • Transmit buffer empty interrupt • Error interrupt (mode fault, overrun, underrun, or parity error) • Idle interrupt • Communication end interrupt
Event link function (output)	The following five types of events can be output to the event link controller. • Reception buffer full event output • Transmission buffer empty event output • Mode fault, overrun, or parity error event output • RSPI idle event output • Transmission-completed event output	Interrupt sources: • Receive buffer full events • Transmit buffer empty events • Error events (mode fault, overrun, underrun, parity error) • Idle events • Communication completion events
Other functions	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode	• Function for initializing the RSPI • Loopback mode
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.76 Comparison of Serial Peripheral Interface Registers

Register	Bit	RX210 (RSPI)	RX660 (RSPId)
SPSR	MODF	Mode fault error flag 0: No mode fault error occurs 1: A mode fault error occurs	Mode fault error flag 0: Neither a mode fault error nor an underrun error occurs. 1: A mode fault error or an underrun error occurs.
	UDRF	—	Underrun error flag
	SPTEF	—	Transmit buffer empty flag
	SPCF	—	Communication completion flag
	SPRF	—	Receive buffer full flag
SPDR	—	RSPI data register Supported access sizes • Longword access (SPDCR.SPLW = 1) • Word access (SPDCR.SPLW = 0)	RSPI data register Supported access sizes • Longword access (SPDCR.SPLW = 1, SPBYTE = 0) • Word access (SPDCR.SPLW = 0, SPBYTE = 0) • Byte access (SPDCR.SPBYT = 1)
SPDCR	SPBYT	—	RSPI byte access specification bit
SPCR2	SPPE	Parity enable bit 0: A parity bit is not added to transmit data, and no parity checking of receive data is performed. 1: A parity bit is added to transmit data, and parity checking of receive data is performed (when SPCR.TXMD = 0). A parity bit is added to transmit data, but no parity checking of receive data is performed (when SPCR.TXMD = 1).	Parity enable bit 0: A parity bit is not added to transmit data, and no parity checking of receive data is performed. 1: A parity bit is added to transmit data, and parity checking of receive data is performed.
	SCKASE	—	RSPCK auto-stop function enable
SPDCR2	—	—	RSPI data control register 2
SPCR3	—	—	RSPI control register 3

2.27 CRC Calculator

Table 2.77 is a comparative overview of the CRC calculators, and Table 2.78 is a comparison of CRC calculator registers.

Table 2.77 Comparative Overview of CRC Calculators

Item	RX210 (CRC)	RX660 (CRCA)	
Data size	8 bits	8 bits	32 bits
Data for CRC calculation	CRC code generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 32n-bit units (where n is a whole number)
CRC processor unit	Operation executed on eight bits in parallel	8-bit parallel processing	32-bit parallel processing
CRC generating polynomial	One of three generating polynomials is selectable • 8-bit CRC: $X^8 + X^2 + X + 1$ • 16-bit CRC: — $X^{16} + X^{15} + X^2 + 1$ — $X^{16} + X^{12} + X^5 + 1$	One of three generating polynomials is selectable • 8-bit CRC: $X^8 + X^2 + X + 1$ • 16-bit CRC: — $X^{16} + X^{15} + X^2 + 1$ — $X^{16} + X^{12} + X^5 + 1$	One of two generating polynomials is selectable • 32-bit CRC: — $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ — $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$
CRC calculation switching	CRC code generation for LSB-first or MSB-first communication selectable	The order of the bits produced by CRC calculation can be switched for LSB first or MSB first communication	
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state	

Table 2.78 Comparison of CRC Calculator Registers

Register	Bit	RX210 (CRC)	RX660 (CRCA)
CRCCR	GPS[1:0] (RX210) GPS[2:0] (RX660)	CRC generating polynomial switching bits b1 b0 0 0: No calculation is executed. 0 1: 8-bit CRC ($X^8 + X^2 + X + 1$) 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$) 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$)	CRC generating polynomial switching bits b2 b0 0 0 0: No calculation is executed. 0 0 1: 8-bit CRC ($X^8 + X^2 + X + 1$) 0 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$) 0 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$) 1 0 0: 32-bit CRC ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1: 32-bit CRC ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) 1 1 0: No calculation is executed. 1 1 1: No calculation is executed.
	LMS	CRC calculation switching bit (b2)	CRC calculation switching bit (b6)
CRCDIR	—	CRC data input register Supported access sizes • Byte access	CRC data input register Supported access sizes • Longword access (32-bit CRC selected) • Byte access (16-bit or 8-bit CRC selected)
CRCDOR	—	CRC data output register Supported access sizes • Word access The bottom byte (b7 to b0) is used when generating 8-bit CRCs.	CRC data output register Supported access sizes • Longword access (32-bit CRC selected) • Word access (16-bit CRC selected) • Byte access (8-bit CRC selected)

2.28 12-Bit A/D Converter

Table 2.79 is a comparative overview of the 12-bit A/D converters, and Table 2.80 is a comparison of 12-bit A/D converter registers.

Table 2.79 Comparative Overview of 12-Bit A/D Converters

Item	RX210 (S12ADb)	RX660 (S12ADH)
Number of units	1 unit	1 unit (S12AD)
Input channels	16 channels	24 channels
Extended analog function	Temperature sensor output, internal reference voltage	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	1.0 µs per channel (when A/D conversion clock ADCLK = 50 MHz)	0.9 µs per channel (when A/D conversion clock (ADCLK) = 60 MHz)
A/D conversion clock	Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency division ratio should be one of the following. PCLK to ADCLK frequency division ratio = 1:1, 1:2, 1:4, 1:8, 2:1, 4:1 ADCLK is set using the clock generation circuit.	Peripheral module clock PCLKB and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. PCLKB to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1 ADCLK is set using the clock generation circuit. The A/D conversion clock (ADCLK) can operate at frequencies from a maximum of 60 MHz to a minimum of 8 MHz.
Data registers	• 16 registers for analog input and one for A/D-converted data duplication in double trigger mode • One register for temperature sensor output • One register for internal reference • The results of A/D conversion are stored in 12-bit A/D data registers. • In addition mode, A/D conversion results are added and stored in A/D data registers as 14-bit data.	• 24 registers for analog input, one for A/D-converted data duplication in double trigger mode • Two registers for A/D-converted data duplication during extended operation in double trigger mode • One register for temperature sensor output • One register for internal reference • One register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode.

Item	RX210 (S12ADb)	RX660 (S12ADH)
Data registers	• Duplication of A/D conversion data A/D conversion data of one selected analog input channel is stored in A/D data register y when conversion is started by the first trigger and in the duplication register when started by the second trigger. Duplication is available only when double trigger mode is selected in single scan mode or group scan mode.	• Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers) A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.
Operating modes	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 16 channels arbitrarily selected. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of up to 16 channels arbitrarily selected. • Group scan mode: — Up to 16 analog input channels are divided between group A and group B, and A/D conversion is performed only once on all channels in the selected group. — The scanning start condition for groups A and B (synchronous trigger) can be independently selected, allowing A/D conversion of each group to be started independently.	• Single scan mode: — A/D conversion is performed only once on arbitrarily selected analog inputs. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: A/D conversion is performed repeatedly on arbitrarily selected analog inputs. • Group scan mode: — Two (groups A and B) or three (groups A, B, and C) can be selected as the number of groups to be used. (Only the combination of groups A and B can be selected when the number of groups is two.) — Arbitrarily selected analog input channels, the temperature sensor output, and the internal reference voltage are divided into two groups (group A and B) or three groups (group A, B, and C), and A/D conversion of the analog input selected on a group basis is performed only once. — The scanning start condition for groups A, B, and C (synchronous trigger) can be independently selected, allowing A/D conversion of each group to be started independently.

Item	RX210 (S12ADb)	RX660 (S12ADH)
Operating modes		• Group scan mode (Group priority control selected) If a higher-priority group trigger is input during scanning of a lower-priority group, scanning of the lower-priority group stops and scanning of the higher-priority group starts. The priority order is group A (highest) > group B > group C (lowest). Whether or not to restart scanning (rescan) of the lower-priority group after processing for the higher-priority group completes, is selectable. Rescan can also be set to start either from the first selected channel or from the channel on which A/D conversion did not complete.
Conditions for A/D conversion start	• Software trigger • Synchronous trigger Trigger by MTU, ELC, or temperature sensor. • Asynchronous trigger A/D conversion can be triggered from the ADTRG0# pin.	• Software trigger • Synchronous trigger Trigger by the multi-function timer pulse unit (MTU), 8-bit timer (TMR), or event link controller (ELC) • Asynchronous trigger A/D conversion can be triggered by the external trigger ADTRG0# pin.
Functions	• Sample-and-hold function • Channel-dedicated sample-and-hold function (0.25 V ≤ analog voltage input ≤ AVCC0 to 0.25 V) • Variable sampling state count • Self-diagnosis of 12-bit A/D converter • A/D-converted value addition mode • Analog input disconnection detection assist • Double trigger mode (duplication of A/D conversion data)	• Variable sampling time (settable on a per-channel basis) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers • Compare function (window A and window B) Ability to specify the channel conversion priority

Item	RX210 (S12ADb)	RX660 (S12ADH)
Interrupt sources	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan. • In group scan mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of group A scan, whereas an A/D scan end interrupt request (GBADI) for group B can be generated on completion of group B scan. • When double trigger mode is selected in group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan of group A, whereas A/D scan end interrupt request (GBADI) specially for group B can be generated on completion of group B scan. • The S12ADI0 or GBADI interrupts can activate the DMA controller (DMAC) or the data transfer controller (DTC).	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI) can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt request (S12ADI) can be generated on completion of double scan. • In group scan mode, an A/D scan end interrupt request (S12ADI) can be generated on completion of group A scan, an A/D scan end interrupt request (S12GBADI) for group B can be generated on completion of group B scan, and an A/D scan end interrupt request (S12GCADI) for group C can be generated on completion of group C scan. • When double trigger mode is selected in group scan mode, A/D scan end interrupt request (S12ADI) can be generated on completion of double scan of group A. A corresponding scan end interrupt request (S12GBADI or S12GCADI) can be generated on completion of a group B or group C scan. • A compare interrupt request (S12CMPAI or S12CMPBI) can be generated upon a match with the comparison condition for the digital compare function. • The S12ADI, S12GBADI, and S12GCADI interrupts can activate the DMA controller (DMAC) or data transfer controller (DTC).
Event link function	• An ELC event can be generated on completion of scans other than group B scan in group scan mode. • A/D conversion can be started by a trigger from the ELC.	• An event can be output upon completion of all scans. • In single scan mode, an event can be output when the compare function window condition is met. • Scan can be started by a trigger output by the ELC.
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.80 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX210 (S12ADb)	RX660 (S12ADH)
ADDRy	—	A/D data register y (y = 0 to 15)	A/D data register y (y = 0 to 23)
ADDBLDRA	—	—	A/D data duplication register A
ADDBLDRB	—	—	A/D data duplication register B
ADANSA (RX210) ADANSA0 (RX660)	—	A/D channel select register A	A/D channel select register A0
ADANSA1	—	—	A/D channel select register A1
ADANSB (RX210) ADANSB0 (RX660)	—	A/D channel select register B	A/D channel select register B0
ADANSB1	—	—	A/D channel select register B1
ADANSC0	—	—	A/D channel select register C0
ADANSC1	—	—	A/D channel select register C1
ADSCSn	—	—	A/D channel conversion order setting register n (n = 0 to 23)
ADADS (RX210) ADADS0 (RX660)	—	A/D-converted value addition mode select register	A/D-converted value addition/ average function select register 0
ADADS1	—	—	A/D-converted value addition/ average function select register 1
ADADC	ADC[1:0] (RX210) ADC[2:0] (RX660)	Addition count select bits b1 b0 0 0: 1-time conversion (no addition, same as normal conversion) 0 1: 2-time conversion (addition one time) 1 0: 3-time conversion (addition two times) 1 1: 4-time conversion (addition 3 times)	Addition count select bits b2 b0 0 0 0: 1-time conversion (no addition, same as normal conversion) 0 0 1: 2-time conversion (addition one time) 0 1 0: 3-time conversion (addition two times) 0 1 1: 4-time conversion (addition three times) 1 0 1: 16-time conversion (addition 15 times) Settings other than the above are prohibited.
	AVEE	—	Average mode enable bit

Register	Bit	RX210 (S12ADb)	RX660 (S12ADH)
ADEXICR	TSSAD	—	Temperature sensor output A/D converted value addition/ average mode select bit
	OCSAD	Internal reference voltage A/D converted value addition mode select 0: Internal reference voltage A/D converted value addition mode is not selected 1: Internal reference voltage A/D converted value addition mode is selected	Internal reference voltage A/D-converted value addition/average mode select bit 0: Internal reference voltage A/D-converted value addition/average mode is disabled. 1: Internal reference voltage A/D-converted value addition/average mode is enabled.
	TSS (RX210) TSSA (RX660)	Temperature sensor output A/D conversion select bits	Temperature sensor output A/D conversion select bits
	OCS (RX210) OCSA (RX660)	Internal reference voltage A/D conversion select bits	Internal reference voltage A/D conversion select bits
	TSSB	—	Group B temperature sensor output A/D conversion select bit
	OCSB	—	Group B internal reference voltage A/D conversion select bit
ADGCEXCR	—	—	A/D group C extended input control register
ADGCTRGR	—	—	A/D group C trigger select register
ADSSTRn	—	A/D sampling state register n (n = 0 to 7, L, T, O)	A/D sampling state register n (n = 0 to 15, L, T, O)
ADSHCR	—	A/D sample and hold circuit control register	—

Register	Bit	RX210 (S12ADb)	RX660 (S12ADH)
ADDISCR	ADNDIS[4:0]	Disconnection detection assist setting bit b3-b0 ADNDIS[3:0]: Discharge or precharge duration b4 ADNDIS[4]: Discharge or precharge selection 0: Discharge 1: Precharge	A/D disconnection detection assist setting bits Specifies the discharge or precharge duration in ADCLK clock cycles. b3 b0 0 0 0 0: No charging (disconnection detection assist function disabled) 0 0 1 1: Charge duration of 3 clock cycles 0 1 1 0: Charge duration of 6 clock cycles 1 0 0 1: Charge duration of 9 clock cycles 1 1 0 0: Charge duration of 12 clock cycles 1 1 1 1: Charge duration of 15 clock cycles Settings other than the above are prohibited. b4 0: Discharge 1: Precharge
ADELCCR	—	—	A/D event link control register
ADGSPCR	—	—	A/D group scan priority control register
ADCMPCR	—	—	A/D compare function control register
ADCMPANSR0	—	—	A/D compare function window A channel select register 0
ADCMPANSR1	—	—	A/D compare function window A channel select register 1
ADCMPANSER	—	—	A/D compare function window A extended input select register
ADCMPLR0	—	—	A/D compare function window A comparison condition setting register 0
ADCMPLR1	—	—	A/D compare function window A comparison condition setting register 1
ADCMPLER	—	—	A/D compare function window A extended input comparison condition setting register
ADCMPDR0	—	—	A/D compare function window A lower-side level setting register
ADCMPDR1	—	—	A/D compare function window A upper-side level setting register
ADCMPSR0	—	—	A/D compare function window A channel status register 0

Register	Bit	RX210 (S12ADb)	RX660 (S12ADH)
ADCMPSR1	—	—	A/D compare function window A channel status register 1
ADCMPSER	—	—	A/D compare function window A extended input channel status register
ADWINMON	—	—	A/D compare function window A/B status monitor register
ADCMPBNSR	—	—	A/D compare function window B channel select register
ADWINLLB	—	—	A/D compare function window B lower-side level setting register
ADWINULB	—	—	A/D compare function window B upper-side level setting register
ADCMPBSR	—	—	A/D compare function window B channel status register
ADVMONCR	—	—	A/D internal reference voltage monitoring circuit enable register
ADVMONO	—	—	A/D internal reference voltage monitoring circuit output enable register
ADVREFCR	—	—	A/D reference voltage control register

2.29 D/A Converter and 12-Bit D/A Converter

Table 2.81 is a comparative overview of the D/A converter and 12-bit D/A converter, and Table 2.82 is a comparison of D/A converter and 12-bit D/A converter registers.

Table 2.81 Comparative Overview of D/A Converter and 12-bit D/A Converter

Item	RX210 (DA)	RX660 (R12DAb)
Resolution	10 bits	12 bits
Output channels	2 channels	2 channels
Measure against interference between analog modules	—	Measure against interference between D/A and A/D converters: D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable signal output by the 12-bit A/D converter. This reduces degradation of A/D conversion accuracy due to interference by controlling the timing of the 12-bit D/A converter inrush current with the enable signal.
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state
Event link function (input)	D/A0 conversion can be started when an event signal is input.	Ability to start D/A conversion on channel 0 when an event signal is input
Output destination selection	—	Output to external pins and to comparator C can be controlled independently.

Table 2.82 Comparison of D/A Converter and 12-bit D/A Converter Registers

Register	Bit	RX210 (DA)	RX660 (R12DAb)
DAADSCR	—	—	D/A A/D synchronous start control register
DADSELR	—	—	D/A destination select register

2.30 Temperature Sensor

Table 2.83 is a comparative overview of the temperature sensors, and Table 2.84 is a comparison of temperature sensor registers.

Table 2.83 Comparative Overview of Temperature Sensors

Item	RX210 (TEMPSa)	RX660 (TEMPS)
Temperature sensor voltage output	The temperature sensor outputs a voltage to the 12-bit A/D converter via a programmable gain amplifier (PGA).	The temperature sensor outputs a voltage to the 12-bit A/D converter (unit 0).
Power consumption reduction function	Ability to specify module stop state	—
Temperature sensor calibration data	—	Reference data measured for each chip at the time of shipment from the factory is stored in a register.

Table 2.84 Comparison of Temperature Sensor Registers

Register	Bit	RX210 (TEMPSa)	RX660 (TEMPS)
TSCR	—	Temperature sensor control register	—
TSCDR	—	—	Temperature sensor calibration data register

2.31 Comparator B and Comparator C

Table 2.85 is a comparative overview of comparator B and comparator C, and Table 2.86 is a comparison of comparator B and comparator C registers.

Table 2.85 Comparative Overview of Comparator B and Comparator C

Item	RX210 (CMPB)	RX660 (CMPC)
Number of channels	2 channels (comparator B0, comparator B1)	4 channels (comparator C0 to comparator C3)
Analog input voltage	Voltage input to CMPBn pin (n = 0 or 1)	Input voltage on CMPCn0 pin (n = channel number)
Reference input voltage	Voltage input to CVREFBn pin (n = 0 or 1) or internal reference voltage	Input voltage on CVREFC0 to CVREFC3 pins or output voltage of on-chip D/A converter 0 or on-chip D/A converter 1
Comparison result	Read from the CPBFLG.CPBnOUT flag (n = 0 or 1)	The comparison result can be output externally.
Digital filter function	Whether the digital filter is applied or not, and the sampling frequency, can be selected.	• One of three sampling periods can be selected. • The filter function can also be disabled. • A noise-filtered signal can be used to generate interrupt request output and event output to the ELC, and comparison results can be read from registers.
Interrupt request	• When the comparator B0 comparison result changes • When the comparator B1 comparison result changes	• An interrupt request is generated upon detection of a valid edge of the comparison result. • The rising edge, falling edge, or both edges of the comparison result can be selected as valid edges.
Timing of event generation to ELC	• When the comparator B0 comparison result changes • When the comparator B0 or comparator B1 comparison result changes	• When the comparator C0 comparison result changes • When the comparator C1 comparison result changes • When the comparator C2 comparison result changes • When the comparator C3 comparison result changes
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Table 2.86 Comparison of Comparator B and Comparator C Registers

Register	Bit	RX210 (CMPB)	RX660 (CMPC)
CPBCNT1	—	Comparator B control register 1	—
CPBFLG	—	Comparator B flag register	—
CPBINT	—	Comparator B interrupt control register	—
CPBF	—	Comparator B filter select register	—
CMPCTL	—	—	Comparator control register
CMPSEL0	—	—	Comparator input select register
CMPSEL1	—	—	Comparator reference voltage select register
CMPMON	—	—	Comparator output monitor register
CMPIOC	—	—	Comparator external output enable register

2.32 Data Operation Circuit

Table 2.87 is a comparative overview of data operation circuit, and Table 2.88 is a comparison of data operation circuit registers.

Table 2.87 Comparative Overview of Data Operation Circuit

Item	RX210 (DOC)	RX660 (DOCA)
Data operation functions	16-bit data comparison, addition, and subtraction	• Comparison of 16- or 32-bit data (match/mismatch, greater/less, in/out of range) • Addition or subtraction of 16- or 32-bit data
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state
Interrupts	• The compared values either match or mismatch • The result of data addition is greater than FFFFh • The result of data subtraction is less than 0000h	• When data comparison result matches detection condition • When data addition result is greater than FFFFh (when DOCR.DOPSZ = 0) or FFFF FFFFh (when DOCR.DOPSZ = 1) (overflow) • When data subtraction result is less than 0000h (when DOCR.DOPSZ = 0) or 0000 0000h (when DOCR.DOPSZ = 1) (underflow)
Event link function (output)	—	• When data comparison result matches detection condition • When data addition result is greater than FFFFh (when DOCR.DOPSZ = 0) or FFFF FFFFh (when DOCR.DOPSZ = 1) (overflow) • When data subtraction result is less than 0000h (when DOCR.DOPSZ = 0) or 0000 0000h (when DOCR.DOPSZ = 1) (underflow)

Table 2.88 Comparison of Data Operation Circuit Registers

Register	Bit	RX210 (DOC)	RX660 (DOCA)
DOCR	DOPSZ	—	Data operation size select bit
	DCSEL (RX210) DCSEL[2:0] (RX660)	Detection condition select bit 0: Detect mismatches as a result of data comparison 1: Detect matches as a result of data comparison	Detection condition select bits b6 b4 0 0 0: Mismatch (DODIR ≠ DODSR0) 0 0 1: Match (DODIR = DODSR0) 0 1 0: Less (DODIR < DODSR0) 0 1 1: Greater (DODIR > DODSR0) 1 0 0: In range (DODSR0 < DODIR < DODSR1) 1 0 1: Out of range (DODIR < DODSR0, DODSR1 < DODIR) Other than above: Setting prohibited.
	DOPCIE	Data operation circuit interrupt enable bit (b4)	Data operation circuit interrupt enable bit (b7)
	DOPCF	Data operation circuit flag	—
	DOPCFCL	DOPCF clear bit	—
DOSR	—	—	DOC status register
DOSCR	—	—	DOC status clear register
DODIR	—	DOC data input register DODIR is a 16-bit readable/writable register.	DOC data input register DODIR is a 32-bit readable/writable register.
DODSR (RX210) DODSR0/ DODSR1 (RX660)	—	DOC data setting register DODSR is a 16-bit readable/writable register.	DOC data setting registers 0 and 1 DODSR0 and DODSR1 are 32-bit readable/writable register.

2.33 RAM

Table 2.89 is a comparative overview of the RAM, and Table 2.90 is a comparison of RAM registers.

Table 2.89 Comparative Overview of RAM

Item	RX210	RX660
RAM capacity	Max. 96 KB (RAM0: 64 KB, RAM1: 32KB)	128 KB
RAM address	• RAM capacity 96 KB RAM0: 0000 0000h to 0000 FFFFh RAM1: 0001 0000h to 0001 7FFFh • RAM capacity 64 KB RAM0: 0000 0000h to 0000 FFFFh • RAM capacity 32 KB RAM0: 0000 0000h to 0000 7FFFh • RAM capacity 20 KB RAM0: 0000 0000h to 0000 4FFFh • RAM capacity 16 KB RAM0: 0000 0000h to 0000 3FFFh • RAM capacity 12 KB RAM0: 0000 0000h to 0000 2FFFh	RAM0: 0000 0000h to 0001 FFFFh
Memory bus	Memory bus 1	Memory bus 1
Access	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing.*1 • The RAM can be enabled or disabled.
Data retention function	Not available in deep software standby mode	Not available in deep software standby mode
Low power consumption function	Ability to specify module stop state independently for RAM0 and RAM1.	Ability to specify module stop state
Error checking function	—	• Parity check: Detection of 1-bit errors • Generation of non-maskable interrupt or interrupt when an error occurs

Note: 1. When accessing across an 8-byte boundary, the number of cycles is doubled.

Table 2.90 Comparison of RAM Registers

Register	Bit	RX210	RX660
RAMMODE	—	—	RAM operating mode control register
RAMSTS	—	—	RAM error status register
RAMECAD	—	—	RAM error address capture register
RAMPRCR	—	—	RAM protection register

2.34 Flash Memory

Table 2.91 is a comparative overview of flash memory, and Table 2.92 is a comparison of flash memory registers.

Table 2.91 Comparative Overview of Flash Memory

Item	RX210	RX660	
	—	Code Flash Memory	Data Flash Memory
Memory capacity	• User area: Up to 1 MB • Data area: 8 KB • User boot area: 16 KB	• User area: Up to 1 MB • User boot area: 32 KB	Data area: 32 KB
Addresses	• Products with capacity of 1 MB FFF0 0000h to FFFF FFFFh • Products with capacity of 768 KB FFF4 0000h to FFFF FFFFh • Products with capacity of 512 KB FFF8 0000h to FFFF FFFFh • Products with capacity of 384 KB FFFA 0000h to FFFF FFFFh • Products with capacity of 256 KB FFFC 0000h to FFFF FFFFh • Products with capacity of 128 KB FFFE 0000h to FFFF FFFFh • Products with capacity of 96 KB FFFE 8000h to FFFF FFFFh • Products with capacity of 64 KB FFFF 0000h to FFFF FFFFh • Data area: 0100 0000h to 0100 2000h	• 1 MB FFF0 0000h to FFFF FFFFh • 512 KB FFF8 0000h to FFFF FFFFh • Data flash memory 0100 0000h to 0100 7FFFh	

Item	RX210	RX660	
	—	Code Flash Memory	Data Flash Memory
FCU command (RX210) Software commands (RX660)	The following FCU commands are implemented • P/E normal mode transition • Status read mode transition • Lock bit read mode transition (lock bit read 1) • Peripheral clock notification • Programming • Block erase • P/E suspend • P/E resume • Status register clear • Lock bit read 2/blank check	FACI commands • Program (user area): 256-byte programming • Program (data area): 4-byte programming • Block erase • P/E suspend • P/E resume • Status clear • Forced stop • Blank check • Configuration set • Program lock bit • Read lock bit	
Read cycles	One cycle Data area: Word or byte read access requires 4 FCLK clock cycles.	One cycle	16-bit or 8-bit read access requires 8 FCLK clock cycles.
Value after erasure	• ROM: FFh • E2 DataFlash: undefined	FFh	Undefined
Programming/ erasing method	• Software commands can be used to program and erase the code flash memory and data flash memory. • A flash memory programmer can be used to program and erase the flash memory via a serial interface (serial programming). • A user program can be used to program and erase the flash memory (self-programming).	• FACI commands specified in the FACI command issuing area (007E 0000h) can be used to program and erase the code flash memory and data flash memory. • A flash memory programmer can be used to program and erase the flash memory via a serial interface (serial programming). • A user program can be used to program and erase the flash memory (self-programming).	

Item	RX210	RX660	
	—	Code Flash Memory	Data Flash Memory
Interrupts	An interrupt (FRDYI) is generated upon completion of FCU command execution.	• Data flash memory access violation interrupt • Command lock interrupt • Code flash memory access violation interrupt • Flash ready interrupt	
Security function	Protects against illicit tampering with or reading of data in flash memory.	Protects against illicit tampering with or reading of data in flash memory.	
Trusted Memory (TM) function	—	Protects against illicit reading of blocks 8 and 9 in the code flash memory.	
Units of programming and erasure	Programming the code flash (4 bytes) Programming the E2 DataFlash (1 byte) Erasure of both types of flash memory is in block units.	Programming the user area and user boot area: 256 bytes Erasure of user area: Block units	Programming the data area: 4 bytes Erasure of data area: Block units
Other functions	Interrupts can be accepted during self-programming.	Interrupts can be accepted during self-programming.	
On-board programming (serial programming and self-programming)	• Programming in boot mode — The clock synchronous serial interface (SCI1) is used. — The communication speed is adjusted automatically. — The user boot area is also programmable. • Programming in user boot mode — A user-specific boot program can be created. • Programming using a ROM programming routine in a user program — The ROM/E2 DataFlash can be programmed without resetting the system.	• Programming/erasure in boot mode (SCI interface) — The clock synchronous serial interface (SCI1) is used. — The communication speed is adjusted automatically. — Programming and erasure of the user boot area is also possible. • Programming/erasure in boot mode (FINE interface) — FINE is used. • Programming/erasure in user boot mode — A user-specific boot program can be created. • Programming/erasure in single-chip mode — Programming or erasure by a routine within a user program for writing to the code flash memory or data flash memory is possible.	
Off-board programming (programming and erasure using a parallel programmer)	A PROM programmer can be used to program the user area and user boot area.	Programming and erasure of the code flash memory and option-setting memory using a parallel programmer is possible.	Programming or erasure of the data area using a parallel programmer is not possible.
Protection function	It is possible to designate a specific range within the user area that may be programmed and prohibit programming outside that range during self-programming.	Protects against erroneous programming of the flash memory.	

Item	RX210	RX660	
	—	Code Flash Memory	Data Flash Memory
Background operation (BGO) function	• Programs in the ROM area can run while the E2 DataFlash is being programmed or erased. • The CPU can run programs in areas other than the ROM or E2 DataFlash while the ROM is being programmed or erased.	The user area can be read while the data area is being programmed or erased.	
Unique ID	—	A unique 12-byte ID code is provided for each MCU.	

Table 2.92 Comparison of Flash Memory Registers

Register	Bit	RX210	RX660 (FLASH)
FMODR	—	Flash mode register	—
FCURAME	—	FCU RAM enable register	—
FSTATR0	—	Flash status register 0	—
FSTATR1	—	Flash status register 1	—
FRDYIE	—	Flash ready interrupt enable register	—
FENTRYR	—	Flash P/E mode entry register	—
FPROTR	—	Flash protection register	—
FRESETR	—	Flash reset register	—
FCMDR	—	FCU command register	—
FCPSR	—	FCU processing switching register	—
FPESTAT	—	Flash P/E status register	—
PCKAR	—	Peripheral clock notification register	—
DFLRE0	—	E2 DataFlash read enable register 0	—
DFLWE0	—	E2 DataFlash programming/ erasure enable register 0	—
FENTRYR	—	Flash P/E mode entry register	—
DFLBCCNT	—	E2 DataFlash blank check control register	—
DFLBCSTAT	—	E2 DataFlash blank check status register	—
FEAMH	—	Flash error address monitor register H	—
FEAML	—	Flash error address monitor register L	—
FSCMR	—	Flash start-up setting monitor register	—
FAWSMR	—	Flash access window start address monitor register	—
FAWEMR	—	Flash access window end address monitor register	—

Register	Bit	RX210	RX660 (FLASH)
FASTAT	DFLWPE	E2 DataFlash programming/erasure protection violation bit	—
	DFLRPE	E2 DataFlash read protection violation bit	—
	DFLAE	E2 DataFlash access violation bit	—
	ROMAE	ROM access violation bit	—
	DFAE	—	Data flash memory access violation flag
	CFAE	—	Code flash memory access violation flag
FAEINT	DFLWPEIE	E2 DataFlash programming/ erasure protection violation interrupt enable bit	Flash access error interrupt enable register
	DFLRPEIE	E2 DataFlash read protection violation interrupt enable bit	—
	DFLAEIE	E2 DataFlash access violation interrupt enable bit	—
	ROMAEIE	ROM access violation interrupt enable bit	—
	DFAEIE	—	Data flash memory access violation interrupt enable bit
	CMDLKIE	—	Command lock interrupt enable bit
	CFAEIE	—	Code flash memory access violation interrupt enable bit
FRDYIE	—	—	Flash ready interrupt enable register
FSADDR	—	—	FACI command start address register
FEADDR	—	—	FACI command end address register
FSTATR	—	—	Flash status register
FENTRYR	—	—	Flash P/E mode entry register
FPROTR	—	—	Flash protection register
FSUINITR	—	—	Flash sequencer set-up initialization register
FLKSTAT	—	—	Lock bit status register
FCMDR	—	—	FACI command register
FPESTAT	—	—	Flash P/E status register
FBCCNT	—	—	Data flash blank check control register
FBCSTAT	—	—	Data flash blank check status register
FPSADDR	—	—	Data flash programming start address register
FCPSR	—	—	Flash sequencer processing switching register
FPCKAR	—	—	Flash sequencer processing clock notification register
UIDRn	—	—	Unique ID register n (n = 0 to 2)

2.35 Packages

As indicated in Table 2.93, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage.

Table 2.93 Packages

	Renesas Code			
	RX210			RX660
Package Type	Chip Version A	Chip Version B	Chip Version C	—
145-pin TFLGA	×	○	×	×
144-pin LFQFP	×	×	×	○
144-pin LQFP	×	○	×	×
100-pin TFLGA	PTLG0100JA-A	PTLG0100JA-A PTLG0100KA-A	PTLG0100JA-A	×
100-pin LFQFP	×	×	×	○
100-pin LQFP	PLQP0100KB-A	PLQP0100KB-A	PLQP0100KB-A	×
80-pin LFQFP	×	×	×	○
80-pin LQFP	PLQP0080KB-A	PLQP0080KB-A PLQP0080JA-A	PLQP0080KB-A PLQP0080JA-A	×
69-pin WLBGA	×	○	×	×
64-pin TFLGA	×	○	×	×
64-pin LFQFP	×	×	×	○
64-pin LQFP	PLQP0064KB-A	PLQP0064KB-A PLQP0064GA-A	PLQP0064KB-A PLQP0064GA-A	×
48-pin LQFP	×	○	×	×
48-pin LFQFP	×	×	×	○

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by **blue text**. Items that exists on both groups with different specifications are indicated by **red text**. **Black text** indicates there is no differences in the item's specifications between groups.

3.1 144-Pin Package

Table 3.1 is a comparative listing of the pin functions of 144-pin package products.

Table 3.1 Comparative Listing of 144-Pin Package Pin Functions

144-Pin LFQFP/ LQFP	RX210	RX660
1	AVSS0	AVSS0
2	P05/DA1	P05/IRQ13/DA1
3	VREFH	P06
4	P03/DA0	P03/IRQ11/DA0
5	VREFL	P04
6	P02/TMCI1/SCK6	P02/TMCI1/SCK6/IRQ10
7	P01/TMCI0/RXD6/SMISO6/SSCL6	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9
8	P00/TMRI0/TXD6/SMOSI6/SSDA6	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8
9	PF5/IRQ4	PF5/IRQ4
10	NC	EMLE*2/PN7*3
11	PJ5	PJ5/POE8#/CTS2#/RTS2#/SS2#/IRQ13
12	VSS	PJ4
13	PJ3/MTIOC3C/CTS6#/RTS6#/SS6#/CTS0#/ RTS0#/SS0#	PJ3/MTIOC3C/CTS6#/RTS6#/SS6#/CTS0#/ RTS0#/SS0#/IRQ11
14	VCL	VCL
15	PJ1/MTIOC3A	PJ1/MTIOC3A
16	MD/FINED	MD/FINED/PN6
17	XCIN	XCIN*4/PH7*5
18	XCOUT	XCOUT*4/PH6*5
19	RES#	RES#
20	XTAL/P37	XTAL/P37/IRQ4
21	VSS	VSS
22	EXTAL/P36	EXTAL/P36/IRQ5
23	VCC	VCC
24	P35/NMI	P35/NMI
25	P34/MTIOC0A/TMCI3/POE2#/SCK6/SCK0/ IRQ4	TRST#*2/P34/MTIOC0A/TMCI3/POE10#/ SCK6/SCK0/IRQ4
26	P33/MTIOC0D/TMRI3/POE3#/TIOCD0/ RXD6/SMISO6/SSCL6/RXD0/SMISO0/ SSCL0/IRQ3-DS	P33/MTIOC0D/TMRI3/POE4#/POE11#/ RXD6/SMISO6/SSCL6/RXD0/SMISO0/ SSCL0/CRX0-A/IRQ3-DS
27	P32/MTIOC0C/TMO3/TIOCC0/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ IRQ2-DS/RTCOUT/RTCIC2	P32/MTIOC0C/TMO3/RTCIC2/RTCOUT/ POE0#/POE10#/TXD6/SMOSI6/SSDA6/ TXD0/SMOSI0/SSDA0/CTX0-A/IRQ2-DS
28	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/ SS1#/IRQ1-DS/RTCIC1	TMS*2/P31/MTIOC4D/TMCI2/RTCIC1/ CTS1#/RTS1#/SS1#/IRQ1-DS
29	P30/MTIOC4B/TMRI3/POE8#/RXD1/ SMISO1/SSCL1/IRQ0-DS/RTCIC0	TDI*2/P30/MTIOC4B/TMRI3/RTCIC0/POE8#/ RXD1/SMISO1/SSCL1/IRQ0-DS/COMP3

144-Pin LFQFP/ LQFP	RX210	RX660
30	P27/CS3#/MTIOC2B/TMCI3/SCK1	TCK*2/P27/CS3#/MTIOC2B/TMCI3/SCK1/ IRQ7/CVREFC3
31	P26/CS2#/MTIOC2A/TMO1/TXD1/SMOSI1/ SSDA1/CTS3#/RTS3#/SS3#	TDO*2/P26/CS2#/MTIOC2A/TMO1/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/IRQ6/ CMPC30
32	P25/CS1#/MTIOC4C/MTCLKB/TIOCA4/ RXD3/SMISO3/SSCL3/ADTRG0#	P25/CS1#/MTIOC4C/MTCLKB/RXD3/ SMISO3/SSCL3/IRQ5/ADTRG0#
33	P24/CS0#/MTIOC4A/MTCLKA/TMRI1/ TIOCB4/SCK3	P24/CS0#/MTIOC4A/MTCLKA/TMRI1/SCK3/ IRQ12
34	P23/MTIOC3D/MTCLKD/TIOCD3/CTS0#/ RTS0#/SS0#/TXD3/SMOSI3/SSDA3	P23/MTIOC3D/MTCLKD/TXD3/SMOSI3/ SSDA3/CTS0#/RTS0#/SS0#/IRQ3
35	P22/MTIOC3B/MTCLKC/TMO0/TIOCC3/ SCK0	P22/MTIOC3B/MTCLKC/TMO0/SCK0/IRQ15
36	P21/MTIOC1B/TMCI0/TIOCA3/RXD0/ SMISO0/SSCL0	P21/MTIOC1B/TMCI0/MTIOC4A/RXD0/ SMISO0/SSCL0/IRQ9
37	P20/MTIOC1A/TMRI0/TIOCB3/TXD0/ SMOSI0/SSDA0	P20/MTIOC1A/TMRI0/TXD0/SMOSI0/ SSDA0/IRQ8
38	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ TIOCB0/TCLKD/SCK1/MISOA/SDA-DS/ TXD3/SMOSI3/SSDA3/IRQ7	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ MTIOC4B/SCK1/TXD3/SMOSI3/SSDA3/ MISOA-C/SDA2/IRQ7/COMP2
39	P87/TIOCA2	P87/MTIOC4C/SMOSI10/SSDA10/TXD10/ TXD010-B/SMOSI010-B/SSDA010-B/IRQ15
40	P16/MTIOC3C/MTIOC3D/TMO2/TIOCB1/ TCLKC/TXD1/SMOSI1/SSDA1/MOSIA/ SCL-DS/RXD3/SMISO3/SSCL3/IRQ6/ RTCOUT/ADTRG0#	P16/MTIOC3C/MTIOC3D/TMO2/RTCOUT/ TXD1/SMOSI1/SSDA1/RXD3/SMISO3/ SSCL3/MOSIA-C/SCL2/IRQ6/ADTRG0#
41	P86/TIOCA0	P86/MTIOC4D/SMISO10/SSCL10/RXD10/ RXD010-B/SMISO010-B/SSCL010-B/IRQ14
42	P15/MTIOC0B/MTCLKB/TMCI2/TIOCB2/ TCLKB/RXD1/SMISO1/SSCL1/SCK3/IRQ5	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/SCK3/CRX0-C/IRQ5/ CMPC20
43	P14/MTIOC3A/MTCLKA/TMRI2/TIOCB5/ TCLKA/CTS1#/RTS1#/SS1#/IRQ4	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/CTX0-C/IRQ4/CVREFC2
44	P13/MTIOC0B/TMO3/TIOCA5/SDA/ TXD2/SMOSI2/SSDA2/IRQ3	P13/MTIOC0B/TMO3/TXD2/SMOSI2/SSDA2/ SDA0/IRQ3
45	P12/TMCI1/SCL/RXD2/SMISO2/SSCL2/IRQ2	P12/MTIC5U/TMCI1/RXD2/SMISO2/SSCL2/ SCL0/IRQ2
46	PH3/TMCI0	PH3/MTIOC4D/TMCI0
47	PH2/TMRI0/IRQ1	PH2/MTIOC4C/TMRI0/TOC1/IRQ1
48	PH1/TMO0/IRQ0	PH1/MTIOC3D/TMO0/TIC1/IRQ0/ADST0
49	PH0/CACREF	PH0/MTIOC3B/CACREF/ADTRG0#
50	P56/MTIOC3C/TIOCA1	P56/MTIOC3C/SCK7/IRQ6
51	P55/WAIT#/MTIOC4D/TMO3	TRDATA3/P55/D0[A0/D0]/WAIT#/MTIOC4D/ MTIOC4A/TMO3/TXD7/SMOSI7/SSDA7/ CRX0-D/IRQ10
52	P54/ALE/MTIOC4B/TMCI1/CTS2#/RTS2#/ SS2#	TRDATA2/P54/ALE/D1[A1/D1]/MTIOC4B/ TMCI1/CTS2#/RTS2#/SS2#/CTX0-D/IRQ4
53	BCLK/P53	P53/BCLK/PMC0/IRQ3
54	P52/RD#/RXD2/SMISO2/SSCL2	P52/RD#/RXD2/SMISO2/SSCL2/IRQ2
55	P51/WR1#/BC1#/WAIT#/SCK2	P51/WR1#/BC1#/WAIT#/SCK2/PMC0/IRQ1
56	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ IRQ0

144-Pin LFQFP/ LQFP	RX210	RX660
57	VSS	VSS
58	P83/MTIOC4C/CTS10#/RTS10#	TRCLK*2/P83/MTIOC4C/SCK10/SS10#/ CTS10#/SCK010-B/CTS010#-A/SS010#-A/ IRQ3
59	VCC	VCC
60	PC7/A23/CS0#/MTIOC3A/TMO2/MTCLKB/ TXD8/SMOSI8/SSDA8/MISOA/CACREF	UB/PC7/CS0#/MTIOC3A/MTCLKB/TMO2/ CACREF/TOC0/TXD8/SMOSI8/SSDA8/ SMOSI10/SSDA10/TXD10/TXD010-C/ SMOSI010-C/SSDA010-C/MISOA-A/IRQ14
61	PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/ RXD8/SMISO8/SSCL8/MOSIA	PC6/D2[A2/D2]/CS1#/MTIOC3C/MTCLKA/ TMCI2/TIC0/RXD8/SMISO8/SSCL8/ SMISO10/SSCL10/RXD10/RXD010-C/ SMISO010-C/SSCL010-C/MOSIA-A/IRQ13
62	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/ TMRI2/SCK8/RSPCKA	PC5/D3[A3/D3]/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/MTIOC0C/SCK8/SCK10/ SCK010-C/RSPCKA-A/PMC0/IRQ5
63	P82/MTIOC4A/TXD10/SMOSI10/SSDA10	TRSYNC*2/P82/MTIOC4A/SMOSI10/ SSDA10/TXD10/TXD010-A/SMOSI010-A/ SSDA010-A/IRQ2
64	P81/MTIOC3D/RXD10/SMISO10/ SSCL10	TRDATA1/P81/MTIOC3D/SMISO10/SSCL10/ RXD10/RXD010-A/SMISO010-A/SSCL010-A/ IRQ9
65	P80/MTIOC3B/SCK10	TRDATA0/P80/MTIOC3B/SCK10/RTS10#/ SCK010-A/RTS010#-A/DE010-A/IRQ8
66	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ POE0#/MTIOC0A/SCK5/CTS8#/RTS8#/ SS8#/SS10#/CTS10#/RTS10#/CTS010#-B/ RTS010#-B/SS010#-B/DE010-B/SSLA0-A/ PMC0/IRQ12
67	PC3/A19/MTIOC4D/TCLKB/TXD5/SMOSI5/ SSDA5	PC3/A19/MTIOC4D/TXD5/SMOSI5/SSDA5/ PMC0/IRQ11
68	P77/TXD11/SMOSI11/SSDA11	TRDATA7/P77/SMOSI11/SSDA11/TXD11/ TXD011-A/SMOSI011-A/SSDA011-A/IRQ7
69	P76/RXD11/SMISO11/SSCL11	TRDATA6/P76/SMISO11/SSCL11/RXD11/ RXD011-A/SMISO011-A/SSCL011-A/IRQ14
70	PC2/A18/MTIOC4B/TCLKA/RXD5/SMISO5/ SSCL5/SSLA3	PC2/A18/MTIOC4B/RXD5/SMISO5/ SSCL5/TXDB011-A/SSLA3-A/IRQ10
71	P75/SCK11	TRSYNC1/P75/SCK11/RTS11#/ SCK011-A/RTS011#-A/DE011-A/IRQ13
72	P74/CTS11#/RTS11#/SS11#	TRDATA5/P74/A20/SS11#/CTS11#/ CTS011#-A/SS011#-A/IRQ12
73	PC1/A17/MTIOC3A/TCLKD/SCK5/SSLA2	PC1/A17/MTIOC3A/SCK5/TXD011-C/ SMOSI011-C/SSDA011-C/TXDA011-C/ SSLA2-A/IRQ12
74	PL1	PL1
75	PC0/A16/MTIOC3C/TCLKC/CTS5#/RTS5#/ SS5#/SSLA1	PC0/A16/MTIOC3C/CTS5#/RTS5#/SS5#/ SMISO011-C/SSCL011-C/RXD011-C/ SSLA1-A/IRQ14
76	PL0	PL0
77	P73	TRDATA4/P73/CS3#/IRQ8

144-Pin LFQFP/ LQFP	RX210	RX660
78	PB7/A15/MTIOC3B/TIOCB5/TXD9/SMOSI9/ SSDA9	PB7/A15/MTIOC3B/TXD9/SMOSI9/SSDA9/ SMOSI11/SSDA11/TXD11/TXD011-B/ SMOSI011-B/SSDA011-B/IRQ15
79	PB6/A14/MTIOC3D/TIOCA5/RXD9/SMISO9/ SSCL9	PB6/A14/MTIOC3D/RXD9/SMISO9/SSCL9/ SMISO11/SSCL11/RXD11/RXD011-B/ SMISO011-B/SSCL011-B/IRQ6
80	PB5/A13/MTIOC2A/MTIOC1B/TMRI1/ POE1#/TIOCB4/SCK9	PB5/A13/MTIOC2A/MTIOC1B/TMRI1/ POE4#/TOC2/SCK9/SCK11/SCK011-B/ IRQ13
81	PB4/A12/TIOCA4/CTS9#/RTS9#/SS9#	PB4/A12/CTS9#/RTS9#/SS9#/SS11#/ CTS11#/RTS11#/CTS011#-B/RTS011#-B/ SS011#-B/DE011-B/IRQ4
82	PB3/A11/MTIOC0A/MTIOC4A/TMO0/ POE3#/TIOCD3/TCLKD/SCK4/SCK6	PB3/A11/MTIOC0A/MTIOC4A/TMO0/ POE11#/TIC2/SCK4/SCK6/PMC0/IRQ3
83	PB2/A10/TIOCC3/TCLKC/CTS4#/ RTS4#/SS4#/CTS6#/RTS6#/SS6#	PB2/A10/CTS4#/RTS4#/SS4#/CTS6#/ RTS6#/SS6#/IRQ2
84	PB1/A9/MTIOC0C/MTIOC4C/TMCI0/ TIOCB3/TXD4/SMOSI4/SSDA4/TXD6/ SMOSI6/SSDA6/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TMCI0/TXD4/ SMOSI4/SSDA4/TXD6/SMOSI6/SSDA6/ IRQ4-DS/COMP1
85	P72	P72/A19/CS2#/IRQ10
86	P71	P71/A18/CS1#/IRQ1
87	PB0/A8/MTIC5W/TIOCA3/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/RSPCKA	PB0/A8/MTIC5W/MTIOC3D/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/RSPCKA-C/ IRQ12
88	PA7/A7/TIOCB2/MISOA	PA7/A7/MISOA-B/IRQ7
89	PA6/A6/MTIC5V/MTCLKB/TMCI3/POE2#/ TIOCA2/CTS5#/RTS5#/SS5#/MOSIA	PA6/A6/MTIC5V/MTCLKB/TMCI3/POE10#/ MTIOC3D/MTIOC6B/CTS5#/RTS5#/SS5#/ CTS12#/RTS12#/SS12#/MOSIA-B/IRQ14
90	PA5/A5/TIOCB1/RSPCKA	PA5/A5/MTIOC6B/RSPCKA-B/IRQ5
91	VCC	VCC
92	PA4/A4/MTIC5U/MTCLKA/TMRI0/TIOCA1/ TXD5/SMOSI5/SSDA5/SSLA0/IRQ5-DS/ CVREFB1	PA4/A4/MTIC5U/MTCLKA/TMRI0/MTIOC4C/ MTIOC7C/TXD5/SMOSI5/SSDA5/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLA0-B/IRQ5-DS/CVREFC1/ADST0
93	VSS	VSS
94	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/ RXD5/SMISO5/SSCL5/IRQ6-DS/CMPB1	PA3/A3/MTIOC0D/MTCLKD/MTIC5V/ MTIOC4D/RXD5/SMISO5/SSCL5/IRQ6-DS/ CMPC10
95	PA2/A2/RXD5/SMISO5/SSCL5/SSLA3	PA2/A2/MTIOC7A/RXD5/SMISO5/SSCL5/ RXD12/SMISO12/SSCL12/RXDX12/ SSLA3-B/IRQ10
96	PA1/A1/MTIOC0B/MTCLKC/TIOCB0/SCK5/ SSLA2/CVREFA	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ MTIOC3B/SCK5/SCK12/SSLA2-B/IRQ11/ ADTRG0#
97	PA0/A0/BC0#/MTIOC4A/TIOCA0/ SSLA1/CACREF	PA0/BC0#/A0/MTIOC4A/CACREF/MTIOC6D/ SSLA1-B/IRQ0
98	P67	P67/MTIOC7C/IRQ15
99	P66	P66/MTIOC7D/IRQ14
100	P65	P65/IRQ13
101	PE7/D15[A15/D15]/IRQ7/AN015	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/IRQ7/AN015

144-Pin LFQFP/ LQFP	RX210	RX660
102	PE6/D14[A14/D14]/CTS4#/RTS4#/SS4#/ IRQ6/AN014	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/CTS4#/RTS4#/SS4#/IRQ6/AN014
103	PK5/TXD4/SMOSI4/SSDA4	PK5/TXD4/SMOSI4/SSDA4
104	P70/SCK4	P70/SCK4/IRQ0
105	PK4/RXD4/SMISO4/SSCL4	PK4/RXD4/SMISO4/SSCL4
106	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/ IRQ5/AN013	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/IRQ5/AN013/COMP0
107	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/ AN012/CMPA2	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/MTIOC4A/MTIOC7D/IRQ12/ AN012
108	PE3/D11[A11/D11]/MTIOC4B/POE8#/ CTS12#/RTS12#/SS12#/AN011/CMPA1	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ POE8#/MTIOC1B/TOC3/CTS12#/RTS12#/ SS12#/IRQ11/AN011
109	PE2/D10[A10/D10]/MTIOC4A/RXD12/ RXDX12/SMISO12/SSCL12/IRQ7-DS/ AN010/CVREFB0	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ MTIOC7A/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/IRQ7-DS/AN010/CVREFC0
110	PE1/D9[A9/D9]/MTIOC4C/TXD12/TXDX12/ SIOX12/SMOSI12/SSDA12/AN009/CMPB0	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/IRQ9/AN009/CMPC00
111	PE0/D8[A8/D8]/SCK12/AN008	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/SCK12/ IRQ8/AN008
112	P64	P64/D3[A3/D3]/IRQ4
113	P63	P63/D2[A2/D2]/CS3#/IRQ3
114	P62	P62/D1[A1/D1]/CS2#/IRQ2
115	P61/CTS9#/RTS9#/SS9#	P61/D0[A0/D0]/CS1#/CTS9#/RTS9#/SS9#/ IRQ1
116	PK3/RXD9/SMISO9/SSCL9	PK3/RXD9/SMISO9/SSCL9
117	P60/SCK9	P60/CS0#/SCK9/IRQ0
118	PK2/TXD9/SMOSI9/SSDA9	PK2/TXD9/SMOSI9/SSDA9
119	PD7/D7[A7/D7]/MTIC5U/POE0#/IRQ7	TRDATA3*2/PD7/D7[A7/D7]/MTIC5U/POE0#/ IRQ7/AN023
120	PD6/D6[A6/D6]/MTIC5V/POE1#/IRQ6	TRDATA2*2/PD6/D6[A6/D6]/MTIC5V/POE4#/ MTIOC8A/IRQ6/AN022
121	PD5/D5[A5/D5]/MTIC5W/POE2#/IRQ5	TRCLK*2/PD5/D5[A5/D5]/MTIC5W/POE10#/ MTIOC8C/IRQ5/AN021
122	PD4/D4[A4/D4]/POE3#/IRQ4	TRSYNC*2/PD4/D4[A4/D4]/POE11#/ MTIOC8B/IRQ4/AN020
123	PD3/D3[A3/D3]/POE8#/IRQ3	TRDATA1/PD3/D3[A3/D3]/POE8#/MTIOC8D/ TOC2/IRQ3/AN019
124	PD2/D2[A2/D2]/MTIOC4D/IRQ2	TRDATA0/PD2/D2[A2/D2]/MTIOC4D/TIC2/ CRX0-B/IRQ2/AN018
125	PD1/D1[A1/D1]/MTIOC4B/IRQ1	TRDATA7/PD1/D1[A1/D1]/MTIOC4B/POE0#/ CTX0-B/IRQ1/AN017
126	PD0/D0[A0/D0]/IRQ0	TRDATA6/PD0/D0[A0/D0]/POE4#/IRQ0/ AN016
127	P93/CTS7#/RTS7#/SS7#	TRSYNC1/P93/A19/POE0#/CTS7#/RTS7#/ SS7#/IRQ11
128	P92/RXD7/SMISO7/SSCL7	TRDATA5/P92/A18/POE4#/RXD7/SMISO7/ SSCL7/IRQ10
129	P91/SCK7	TRDATA4/P91/A17/SCK7/IRQ9
130	VSS	PF7

144-Pin LFQFP/ LQFP	RX210	RX660
131	P90/TXD7/SMOSI7/SSDA7	P90/A16/TXD7/SMOSI7/SSDA7/IRQ0
132	VCC	PF6
133	P47/AN007	P47/IRQ15-DS/AN007
134	P46/AN006	P46/IRQ14-DS/AN006
135	P45/AN005	P45/IRQ13-DS/AN005
136	P44/AN004	P44/IRQ12-DS/AN004
137	P43/AN003	P43/IRQ11-DS/AN003
138	P42/AN002	P42/IRQ10-DS/AN002
139	P41/AN001	P41/IRQ9-DS/AN001
140	VREFL0	VREFL0/PJ7
141	P40/AN000	P40/IRQ8-DS/AN000
142	VREFH0	VREFH0/PJ6
143	AVCC0	AVCC0
144	P07/ADTRG0#	P07/IRQ15/ADTRG0#

Notes: 1. The I/O buffer power supply for these pins is AVCC0.
2. Not present on products not provided with a JTAG.
3. Not present on products provided with a JTAG.
4. Not present on products not provided with a sub-clock oscillator.
5. Not present on products provided with a sub-clock oscillator.

3.2 100-Pin Package

Table 3.2 is a comparative listing of the pin functions of 100-pin package products.

Table 3.2 Comparative Listing of 100-Pin Package Pin Functions

100-Pin LFQFP	RX210	RX660
1	VREFH	P06
2	P03/DA0	EMLE*2/P03*3/IRQ11*2/DA0*3
3	VREFL	P04
4	PJ3/MTIOC3C/CTS6#/RTS6#/SS6#	PJ3/MTIOC3C/CTS6#/RTS6#/SS6#/CTS0#/RTS0#/SS0#/IRQ11
5	VCL	VCL
6	PJ1/MTIOC3A	PJ1/MTIOC3A
7	MD/FINED	MD/FINED/PN6
8	XCIN	XCIN*4/PH7*5
9	XCOUT	XCOUT*4/PH6*5
10	RES#	RES#
11	XTAL/P37	XTAL/P37/IRQ4
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36/IRQ5
14	VCC	VCC
15	P35/NMI	P35/NMI
16	P34/MTIOC0A/TMCI3/POE2#/SCK6/IRQ4	TRST#*2/P34/MTIOC0A/TMCI3/POE10#/SCK6/SCK0/IRQ4
17	P33/MTIOC0D/TMRI3/POE3#/RXD6/SMISO6/SSCL6/IRQ3-DS	P33/MTIOC0D/TMRI3/POE4#/POE11#/RXD6/SMISO6/SSCL6/RXD0/SMISO0/SSCL0/CRX0-A/IRQ3-DS
18	P32/MTIOC0C/TMO3/TXD6/SMOSI6/SSDA6/IRQ2-DS/RTCOUT/RTCIC2	P32/MTIOC0C/TMO3/RTCIC2/RTCOUT/POE0#/POE10#/TXD6/SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/CTX0-A/IRQ2-DS
19	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/IRQ1-DS/RTCIC1	TMS*2/P31/MTIOC4D/TMCI2/RTCIC1/CTS1#/RTS1#/SS1#/IRQ1-DS
20	P30/MTIOC4B/TMRI3/POE8#/RXD1/SMISO1/SSCL1/IRQ0-DS/RTCIC0	TDI*2/P30/MTIOC4B/TMRI3/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/IRQ0-DS/COMP3
21	P27/CS3#/MTIOC2B/TMCI3/SCK1	TCK*2/P27/CS3#/MTIOC2B/TMCI3/SCK1/IRQ7/CVREFC3
22	P26/CS2#/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1	TDO*2/P26/CS2#/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/IRQ6/CMPC30
23	P25/CS1#/MTIOC4C/MTCLKB/ADTRG0#	P25/CS1#/MTIOC4C/MTCLKB/RXD3/SMISO3/SSCL3/IRQ5/ADTRG0#
24	P24/CS0#/MTIOC4A/MTCLKA/TMRI1	P24/CS0#/MTIOC4A/MTCLKA/TMRI1/SCK3/IRQ12
25	P23/MTIOC3D/MTCLKD/CTS0#/RTS0#/SS0#	P23/MTIOC3D/MTCLKD/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/SS0#/IRQ3
26	P22/MTIOC3B/MTCLKC/TMO0/SCK0	P22/MTIOC3B/MTCLKC/TMO0/SCK0/IRQ15
27	P21/MTIOC1B/TMCI0/RXD0/SMISO0/SSCL0	P21/MTIOC1B/TMCI0/MTIOC4A/RXD0/SMISO0/SSCL0/IRQ9
28	P20/MTIOC1A/TMRI0/TXD0/SMOSI0/SSDA0	P20/MTIOC1A/TMRI0/TXD0/SMOSI0/SSDA0/IRQ8
29	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/SCK1/MISOA/SDA-DS/IRQ7	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/MTIOC4B/SCK1/TXD3/SMOSI3/SSDA3/MISOA-C/SDA2/IRQ7/COMP2

100-Pin LFQFP	RX210	RX660
30	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/ SMOSI1/SSDA1/MOSIA/SCL-DS/IRQ6/ RTCOUT/ADTRG0#	P16/MTIOC3C/MTIOC3D/TMO2/RTCOUT/ TXD1/SMOSI1/SSDA1/RXD3/SMISO3/ SSCL3/MOSIA-C/SCL2/IRQ6/ADTRG0#
31	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/IRQ5	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/SCK3/CRX0-C/IRQ5/ CMPC20
32	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/IRQ4	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/CTX0-C/IRQ4/CVREFC2
33	P13/MTIOC0B/TMO3/SDA/IRQ3	P13/MTIOC0B/TMO3/TXD2/SMOSI2/SSDA2/ SDA0/IRQ3
34	P12/TMCI1/SCL/IRQ2	P12/MTIC5U/TMCI1/RXD2/SMISO2/SSCL2/ SCL0/IRQ2
35	PH3/TMCI0	PH3/MTIOC4D/TMCI0
36	PH2/TMRI0/IRQ1	PH2/MTIOC4C/TMRI0/TOC1/IRQ1
37	PH1/TMO0/IRQ0	PH1/MTIOC3D/TMO0/TIC1/IRQ0/ADST0
38	PH0/CACREF	PH0/MTIOC3B/CACREF/ADTRG0#
39	P55/WAIT#/MTIOC4D/TMO3	P55/D0[A0/D0]/WAIT#/MTIOC4D/MTIOC4A/ TMO3/CRX0-D/IRQ10
40	P54/ALE/MTIOC4B/TMCI1	P54/ALE/D1[A1/D1]/MTIOC4B/TMCI1/ CTS2#/RTS2#/SS2#/CTX0-D/IRQ4
41	BCLK/P53	P53/BCLK/PMC0/IRQ3
42	P52/RD#	P52/RD#/RXD2/SMISO2/SSCL2/IRQ2
43	P51/WR1#/BC1#/WAIT#	P51/WR1#/BC1#/WAIT#/SCK2/PMC0/IRQ1
44	P50/WR0#/WR#	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ IRQ0
45	PC7/A23/CS0#/MTIOC3A/TMO2/MTCLKB/ TXD8/SMOSI8/SSDA8/MISOA/CACREF	UB/PC7/CS0#/MTIOC3A/MTCLKB/TMO2/ CACREF/TOC0/TXD8/SMOSI8/SSDA8/ SMOSI10/SSDA10/TXD10/TXD010-C/ SMOSI010-C/SSDA010-C/MISOA-A/IRQ14
46	PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/ RXD8/SMISO8/SSCL8/MOSIA	PC6/D2[A2/D2]/CS1#/MTIOC3C/MTCLKA/ TMCI2/TIC0/RXD8/SMISO8/SSCL8/ SMISO10/SSCL10/RXD10/RXD010-C/ SMISO010-C/SSCL010-C/MOSIA-A/IRQ13
47	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/ TMRI2/SCK8/RSPCKA	PC5/D3[A3/D3]/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/MTIOC0C/SCK8/SCK10/ SCK010-C/RSPCKA-A/PMC0/IRQ5
48	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ POE0#/MTIOC0A/SCK5/CTS8#/RTS8#/ SS8#/SS10#/CTS10#/RTS10#/CTS010#-B/ RTS010#-B/SS010#-B/DE010-B/SSLA0-A/ PMC0/IRQ12
49	PC3/A19/MTIOC4D/TXD5/SMOSI5/SSDA5	PC3/A19/MTIOC4D/TXD5/SMOSI5/SSDA5/ PMC0/IRQ11
50	PC2/A18/MTIOC4B/RXD5/SMISO5/SSCL5/ SSLA3	PC2/A18/MTIOC4B/RXD5/SMISO5/SSCL5/ TXDB011-A/SSLA3-A/IRQ10
51	PC1/A17/MTIOC3A/SCK5/SSLA2	PC1/A17/MTIOC3A/SCK5/TXD011-C/ SMOSI011-C/SSDA011-C/TXDA011-C/ SSLA2-A/IRQ12
52	PC0/A16/MTIOC3C/CTS5#/RTS5#/SS5#/ SSLA1	PC0/A16/MTIOC3C/CTS5#/RTS5#/SS5#/ SMISO011-C/SSCL011-C/RXD011-C/ SSLA1-A/IRQ14

100-Pin LFQFP	RX210	RX660
53	PB7/A15/MTIOC3B/TXD9/SMOSI9/SSDA9	PB7/A15/MTIOC3B/TXD9/SMOSI9/SSDA9/ SMOSI11/SSDA11/TXD11/TXD011-B/ SMOSI011-B/SSDA011-B/IRQ15
54	PB6/A14/MTIOC3D/RXD9/SMISO9/SSCL9	PB6/A14/MTIOC3D/RXD9/SMISO9/SSCL9/ SMISO11/SSCL11/RXD11/RXD011-B/ SMISO011-B/SSCL011-B/IRQ6
55	PB5/A13/MTIOC2A/MTIOC1B/TMRI1/ POE1#/SCK9	PB5/A13/MTIOC2A/MTIOC1B/TMRI1/ POE4#/TOC2/SCK9/SCK11/SCK011-B/ IRQ13
56	PB4/A12/CTS9#/RTS9#/SS9#	PB4/A12/CTS9#/RTS9#/SS9#/SS11#/ CTS11#/RTS11#/CTS011#-B/RTS011#-B/ SS011#-B/DE011-B/IRQ4
57	PB3/A11/MTIOC0A/MTIOC4A/TMO0/POE3#/ SCK6	PB3/A11/MTIOC0A/MTIOC4A/TMO0/ POE11#/TIC2/SCK4/SCK6/PMC0/IRQ3
58	PB2/A10/CTS6#/RTS6#/SS6#	PB2/A10/CTS4#/RTS4#/SS4#/CTS6#/ RTS6#/SS6#/IRQ2
59	PB1/A9/MTIOC0C/MTIOC4C/TMCI0/TXD6/ SMOSI6/SSDA6/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TMCI0/TXD4/ SMOSI4/SSDA4/TXD6/SMOSI6/SSDA6/ IRQ4-DS/COMP1
60	VCC	VCC
61	PB0/A8/MTIC5W/RXD6/SMISO6/SSCL6/ RSPCKA	PB0/A8/MTIC5W/MTIOC3D/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/RSPCKA-C/ IRQ12
62	VSS	VSS
63	PA7/A7/MISOA	PA7/A7/MISOA-B/IRQ7
64	PA6/A6/MTIC5V/MTCLKB/TMCI3/POE2#/ CTS5#/RTS5#/SS5#/MOSIA	PA6/A6/MTIC5V/MTCLKB/TMCI3/POE10#/ MTIOC3D/MTIOC6B/CTS5#/RTS5#/SS5#/ CTS12#/RTS12#/SS12#/MOSIA-B/IRQ14
65	PA5/A5/RSPCKA	PA5/A5/MTIOC6B/RSPCKA-B/IRQ5
66	PA4/A4/MTIC5U/MTCLKA/TMRI0/TXD5/ SMOSI5/SSDA5/SSLA0/IRQ5-DS/CVREFB1	PA4/A4/MTIC5U/MTCLKA/TMRI0/MTIOC4C/ MTIOC7C/TXD5/SMOSI5/SSDA5/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLA0-B/IRQ5-DS/CVREFC1/ADST0
67	PA3/A3/MTIOC0D/MTCLKD/RXD5/SMISO5/ SSCL5/IRQ6-DS/CMPB1	PA3/A3/MTIOC0D/MTCLKD/MTIC5V/ MTIOC4D/RXD5/SMISO5/SSCL5/IRQ6-DS/ CMPC10
68	PA2/A2/RXD5/SMISO5/SSCL5/SSLA3	PA2/A2/MTIOC7A/RXD5/SMISO5/SSCL5/ RXD12/SMISO12/SSCL12/RXDX12/ SSLA3-B/IRQ10
69	PA1/A1/MTIOC0B/MTCLKC/SCK5/SSLA2/ CVREFA	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ MTIOC3B/SCK5/SCK12/SSLA2-B/IRQ11/ ADTRG0#
70	PA0/A0/BC0#/MTIOC4A/SSLA1/CACREF	PA0/BC0#/A0/MTIOC4A/CACREF/MTIOC6D/ SSLA1-B/IRQ0
71	PE7/D15[A15/D15]/IRQ7/AN015	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/IRQ7/AN015
72	PE6/D14[A14/D14]/IRQ6/AN014	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/CTS4#/RTS4#/SS4#/IRQ6/AN014
73	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/ IRQ5/AN013	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/IRQ5/AN013/COMP0
74	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/ AN012/CMPA2	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/MTIOC4A/MTIOC7D/IRQ12/ AN012

100-Pin LFQFP	RX210	RX660
75	PE3/D11[A11/D11]/MTIOC4B/POE8#/ CTS12#/RTS12#/SS12#/AN011/CMPA1	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ POE8#/MTIOC1B/TOC3/CTS12#/RTS12#/ SS12#/IRQ11/AN011
76	PE2/D10[A10/D10]/MTIOC4A/RXD12/ RXDX12/SMISO12/SSCL12/IRQ7-DS/ AN010/CVREFB0	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ MTIOC7A/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/IRQ7-DS/AN010/CVREFC0
77	PE1/D9[A9/D9]/MTIOC4C/TXD12/TXDX12/ SIOX12/SMOSI12/SSDA12/AN009/CMPB0	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/IRQ9/AN009/CMPC00
78	PE0/D8[A8/D8]/SCK12/AN008	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/SCK12/ IRQ8/AN008
79	PD7/D7[A7/D7]/MTIC5U/POE0#/IRQ7	PD7/D7[A7/D7]/MTIC5U/POE0#/IRQ7/AN023
80	PD6/D6[A6/D6]/MTIC5V/POE1#/IRQ6	PD6/D6[A6/D6]/MTIC5V/POE4#/MTIOC8A/ IRQ6/AN022
81	PD5/D5[A5/D5]/MTIC5W/POE2#/IRQ5	PD5/D5[A5/D5]/MTIC5W/POE10#/MTIOC8C/ IRQ5/AN021
82	PD4/D4[A4/D4]/POE3#/IRQ4	PD4/D4[A4/D4]/POE11#/MTIOC8B/IRQ4/ AN020
83	PD3/D3[A3/D3]/POE8#/IRQ3	PD3/D3[A3/D3]/POE8#/MTIOC8D/TOC2/ IRQ3/AN019
84	PD2/D2[A2/D2]/MTIOC4D/IRQ2	PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0-B/ IRQ2/AN018
85	PD1/D1[A1/D1]/MTIOC4B/IRQ1	PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0-B/ IRQ1/AN017
86	PD0/D0[A0/D0]/IRQ0	PD0/D0[A0/D0]/POE4#/IRQ0/AN016
87	P47/AN007	P47/IRQ15-DS/AN007
88	P46/AN006	P46/IRQ14-DS/AN006
89	P45/AN005	P45/IRQ13-DS/AN005
90	P44/AN004	P44/IRQ12-DS/AN004
91	P43/AN003	P43/IRQ11-DS/AN003
92	P42/AN002	P42/IRQ10-DS/AN002
93	P41/AN001	P41/IRQ9-DS/AN001
94	VREFL0	VREFL0/PJ7
95	P40/AN000	P40/IRQ8-DS/AN000
96	VREFH0	VREFH0/PJ6
97	AVCC0	AVCC0
98	P07/ADTRG0#	P07/IRQ15/ADTRG0#
99	AVSS0	AVSS0
100	P05/DA1	P05/IRQ13/DA1

Notes: 1. The I/O buffer power supply for these pins is AVCC0.
2. Not present on products not provided with a JTAG.
3. Not present on products provided with a JTAG.
4. Not present on products not provided with a sub-clock oscillator.
5. Not present on products provided with a sub-clock oscillator.

3.3 80-Pin Package

Table 3.3 is a comparative listing of the pin functions of 80-pin package products.

Table 3.3 Comparative Listing of 80-Pin Package Pin Functions

80-Pin LFQFP	RX210	RX660
1	VREFH	P06
2	P03/DA0	P03/IRQ11/DA0
3	VREFL	P04
4	VCL	VCL
5	PJ1/MTIOC3A	PJ1/MTIOC3A
6	MD/FINED	MD/FINED/PN6
7	XCIN	XCIN*2/PH7*3
8	XCOUT	XCOUT*2/PH6*3
9	RES#	RES#
10	XTAL/P37	XTAL/P37/IRQ4
11	VSS	VSS
12	EXTAL/P36	EXTAL/P36/IRQ5
13	VCC	VCC
14	P35/NMI	P35/NMI
15	P34/MTIOC0A/TMCI3/POE2#/SCK6/IRQ4	P34/MTIOC0A/TMCI3/POE10#/SCK6/SCK0/IRQ4
16	P32/MTIOC0C/TMO3/TXD6/SMOSI6/SSDA6/IRQ2-DS/RTCOUT/RTCIC2	P32/MTIOC0C/TMO3/RTCIC2/RTCOUT/POE0#/POE10#/TXD6/SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/CTX0-A/IRQ2-DS
17	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/IRQ1-DS/RTCIC1	P31/MTIOC4D/TMCI2/RTCIC1/CTS1#/RTS1#/SS1#/IRQ1-DS
18	P30/MTIOC4B/TMRI3/POE8#/RXD1/SMISO1/SSCL1/IRQ0-DS/RTCIC0	P30/MTIOC4B/TMRI3/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/IRQ0-DS/COMP3
19	P27/MTIOC2B/TMCI3/SCK1	P27/MTIOC2B/TMCI3/SCK1/IRQ7/CVREFC3
20	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/IRQ6/CMPC30
21	P21/MTIOC1B/TMCI0/RXD0/SSCL0	P21/MTIOC1B/TMCI0/MTIOC4A/RXD0/SMISO0/SSCL0/IRQ9
22	P20/MTIOC1A/TMRI0/TXD0/SSDA0	P20/MTIOC1A/TMRI0/TXD0/SMOSI0/SSDA0/IRQ8
23	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/SCK1/MISOA/SDA-DS/IRQ7	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/MTIOC4B/SCK1/TXD3/SMOSI3/SSDA3/MISOA-C/SDA2/IRQ7/COMP2
24	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/SMOSI1/SSDA1/MOSIA/SCL-DS/IRQ6/RTCOUT/ADTRG0#	P16/MTIOC3C/MTIOC3D/TMO2/RTCOUT/TXD1/SMOSI1/SSDA1/RXD3/SMISO3/SSCL3/MOSIA-C/SCL2/IRQ6/ADTRG0#
25	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/SMISO1/SSCL1/IRQ5	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/SMISO1/SSCL1/SCK3/CRX0-C/IRQ5/CMPC20
26	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/RTS1#/SS1#/IRQ4	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/RTS1#/SS1#/CTX0-C/IRQ4/CVREFC2
27	P13/MTIOC0B/TMO3/SDA/IRQ3	P13/MTIOC0B/TMO3SDA0/IRQ3
28	P12/TMCI1/SCL/IRQ2	P12/MTIC5U/TMCI1/SCL0/IRQ2
29	PH3/TMCI0	PH3/MTIOC4D/TMCI0
30	PH2/TMRI0/IRQ1	PH2/MTIOC4C/TMRI0/TOC1/IRQ1
31	PH1/TMO0/IRQ0	PH1/MTIOC3D/TMO0/TIC1/IRQ0/ADST0

80-Pin LFQFP	RX210	RX660
32	PH0/CACREF	PH0/MTIOC3B/CACREF/ADTRG0#
33	P55/MTIOC4D/TMO3	P55/MTIOC4D/MTIOC4A/TMO3/CRX0-D/ IRQ10
34	P54/MTIOC4B/TMCI1	P54/MTIOC4B/TMCI1/CTX0-D/IRQ4
35	PC7/MTIOC3A/TMO2/MTCLKB/TXD8/ SMOSI8/SSDA8/MISOA/CACREF	UB/PC7/MTIOC3A/MTCLKB/TMO2/ CACREF/TOC0/TXD8/SMOSI8/SSDA8/ SMOSI10/SSDA10/TXD10/TXD010-C/ SMOSI010-C/SSDA010-C/MISOA-A/IRQ14
36	PC6/MTIOC3C/MTCLKA/TMCI2/RXD8/ SMISO8/SSCL8/MOSIA	PC6/MTIOC3C/MTCLKA/TMCI2/TIC0/RXD8/ SMISO8/SSCL8/SMISO10/SSCL10/RXD10/ RXD010-C/SMISO010-C/SSCL010-C/ MOSIA-A/IRQ13
37	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/ RSPCKA	PC5/MTIOC3B/MTCLKD/TMRI2/MTIOC0C/ SCK8/SCK10/SCK010-C/RSPCKA-A/PMC0/ IRQ5
38	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/ SCK5/CTS8#/RTS8#/SS8#/SSLA0	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/ MTIOC0A/SCK5/CTS8#/RTS8#/SS8#/ SS10#/CTS10#/RTS10#/CTS010#-B/ RTS010#-B/SS010#-B/DE010-B/SSLA0-A/ PMC0/IRQ12
39	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5/ PMC0/IRQ11
40	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/ SSLA3	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/ TXDB011-A/SSLA3-A/IRQ10
41	PB7/MTIOC3B/TXD9/SMOSI9/SSDA9	PB7/MTIOC3B/TXD9/SMOSI9/SSDA9/ SMOSI11/SSDA11/TXD11/TXD011-B/ SMOSI011-B/SSDA011-B/IRQ15
42	PB6/MTIOC3D/RXD9/SMISO9/SSCL9	PB6/MTIOC3D/RXD9/SMISO9/SSCL9/ SMISO11/SSCL11/RXD11/RXD011-B/ SMISO011-B/SSCL011-B/IRQ6
43	PB5/MTIOC2A/MTIOC1B/TMRI1/POE1#/ SCK9	PB5/MTIOC2A/MTIOC1B/TMRI1/POE4#/ TOC2/SCK9/SCK11/SCK011-B/IRQ13
44	PB4/CTS9#/RTS9#/SS9#	PB4/CTS9#/RTS9#/SS9#/SS11#/CTS11#/ RTS11#/CTS011#-B/RTS011#-B/SS011#-B/ DE011-B/IRQ4
45	PB3/MTIOC0A/MTIOC4A/TMO0/POE3#/ SCK6	PB3/MTIOC0A/MTIOC4A/TMO0/POE11#/ TIC2/SCK4/SCK6/PMC0/IRQ3
46	PB2/CTS6#/RTS6#/SS6#	PB2/CTS4#/RTS4#/SS4#/CTS6#/RTS6#/ SS6#/IRQ2
47	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD6/ SMOSI6/SSDA6/IRQ4-DS	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD4/ SMOSI4/SSDA4/TXD6/SMOSI6/SSDA6/ IRQ4-DS/COMP1
48	VCC	VCC
49	PB0/MTIC5W/RXD6/SMISO6/SSCL6/ RSPCKA	PB0/MTIC5W/MTIOC3D/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/RSPCKA-C/ IRQ12
50	VSS	VSS
51	PA6/MTIC5V/MTCLKB/TMCI3/POE2#/ CTS5#/RTS5#/SS5#/MOSIA	PA6/MTIC5V/MTCLKB/TMCI3/POE10#/ MTIOC3D/MTIOC6B/CTS5#/RTS5#/SS5#/ CTS12#/RTS12#/SS12#/MOSIA-B/IRQ14
52	PA5/RSPCKA	PA5/MTIOC6B/RSPCKA-B/IRQ5

80-Pin LFQFP	RX210	RX660
53	PA4/MTIC5U/MTCLKA/TMRI0/TXD5/ SMOSI5/SSDA5/SSLA0/IRQ5-DS/CVREFB1	PA4/MTIC5U/MTCLKA/TMRI0/MTIOC4C/ MTIOC7C/TXD5/SMOSI5/SSDA5/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLA0-B/IRQ5-DS/CVREFC1/ADST0
54	PA3/MTIOC0D/MTCLKD/RXD5/SMISO5/ SSCL5/IRQ6-DS/CMPB1	PA3/MTIOC0D/MTCLKD/MTIC5V/MTIOC4D/ RXD5/SMISO5/SSCL5/IRQ6-DS/CMPC10
55	PA2/RXD5/SMISO5/SSCL5/SSLA3	PA2/MTIOC7A/RXD5/SMISO5/SSCL5/ RXD12/SMISO12/SSCL12/RXDX12/ SSLA3-B/IRQ10
56	PA1/MTIOC0B/MTCLKC/SCK5/SSLA2/ CVREFA	PA1/MTIOC0B/MTCLKC/MTIOC7B/ MTIOC3B/SCK5/SCK12/SSLA2-B/IRQ11/ ADTRG0#
57	PA0/MTIOC4A/SSLA1/CACREF	PA0/MTIOC4A/CACREF/MTIOC6D/ SSLA1-B/IRQ0
58	PE5/MTIOC4C/MTIOC2B/IRQ5/AN013	PE5/MTIOC4C/MTIOC2B/IRQ5/AN013/ COMP0
59	PE4/MTIOC4D/MTIOC1A/AN012/CMPA2	PE4/MTIOC4D/MTIOC1A/MTIOC4A/ MTIOC7D/IRQ12/AN012
60	PE3/MTIOC4B/POE8#/CTS12#/RTS12#/ SS12#/AN011/CMPA1	PE3/MTIOC4B/POE8#/MTIOC1B/TOC3/ CTS12#/RTS12#/SS12#/IRQ11/AN011
61	PE2/MTIOC4A/RXD12/RXDX12/SMISO12/ SSCL12/IRQ7-DS/AN010/CVREFB0	PE2/MTIOC4A/MTIOC7A/TIC3/RXD12/ SMISO12/SSCL12/RXDX12/IRQ7-DS/ AN010/CVREFC0
62	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12/AN009/CMPB0	PE1/MTIOC4C/MTIOC3B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/IRQ9/AN009/ CMPC00
63	PE0/SCK12/AN008	PE0/MTIOC3D/SCK12/IRQ8/AN008
64	PD2/MTIOC4D/IRQ2	PD2/MTIOC4D/TIC2/CRX0-B/IRQ2/AN018
65	PD1/MTIOC4B/IRQ1	PD1/MTIOC4B/POE0#/CTX0-B/IRQ1/AN017
66	PD0/IRQ0	PD0/POE4#/IRQ0/AN016
67	P47/AN007	P47/IRQ15-DS/AN007
68	P46/AN006	P46/IRQ14-DS/AN006
69	P45/AN005	P45/IRQ13-DS/AN005
70	P44/AN004	P44/IRQ12-DS/AN004
71	P43/AN003	P43/IRQ11-DS/AN003
72	P42/AN002	P42/IRQ10-DS/AN002
73	P41/AN001	P41/IRQ9-DS/AN001
74	VREFL0	VREFL0/PJ7
75	P40/AN000	P40/IRQ8-DS/AN000
76	VREFH0	VREFH0/PJ6
77	AVCC0	AVCC0
78	P07/ADTRG0#	P07/IRQ15/ADTRG0#
79	AVSS0	AVSS0
80	P05/DA1	P05/IRQ13/DA1

Notes: 1. The I/O buffer power supply for these pins is AVCC0.
2. Not present on products not provided with a sub-clock oscillator.
3. Not present on products provided with a sub-clock oscillator.

3.4 64-Pin Package

Table 3.4 is a comparative listing of the pin functions of 64-pin package products.

Table 3.4 Comparative Listing of 64-Pin Package Pin Functions

64-Pin LFQFP/ LQFP	RX210	RX660
1	P03/DA0	P03/IRQ11/DA0
2	VCL	VCL
3	MD/FINED	MD/FINED/PN6
4	XCIN	XCIN*2/PH7*3
5	XCOUT	XCOUT*2/PH6*3
6	RES#	RES#
7	XTAL/P37	XTAL/P37/IRQ4
8	VSS	VSS
9	EXTAL/P36	EXTAL/P36/IRQ5
10	VCC	VCC
11	P35/NMI	P35/NMI
12	P32/MTIOC0C/TMO3/TXD6/SMOSI6/SSDA6/ IRQ2-DS/RTCOUT/RTCIC2	P32/MTIOC0C/TMO3/RTCIC2/RTCOUT/ POE0#/POE10#/TXD6/SMOSI6/SSDA6/ CTX0-A/IRQ2-DS
13	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/ IRQ1-DS/RTCIC1	P31/MTIOC4D/TMCI2/RTCIC1/CTS1#/ RTS1#/SS1#/IRQ1-DS
14	P30/MTIOC4B/TMRI3/POE8#/RXD1/ SMISO1/SSCL1/IRQ0-DS/RTCIC0	P30/MTIOC4B/TMRI3/RTCIC0/POE8#/ RXD1/SMISO1/SSCL1/IRQ0-DS/COMP3
15	P27/MTIOC2B/TMCI3/SCK1	P27/MTIOC2B/TMCI3/SCK1/IRQ7/CVREFC3
16	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/ CTS3#/RTS3#/SS3#/IRQ6/CMPC30
17	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ SCK1/MISOA/SDA-DS/IRQ7	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ MTIOC4B/SCK1/TXD3/SMOSI3/SSDA3/ MISOA-C/SDA2/IRQ7/COMP2
18	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/ SMOSI1/SSDA1/MOSIA/SCL-DS/IRQ6/ RTCOUT/ADTRG0#	P16/MTIOC3C/MTIOC3D/TMO2/RTCOUT/ TXD1/SMOSI1/SSDA1/RXD3/SMISO3/ SSCL3/MOSIA-C/SCL2/IRQ6/ADTRG0#
19	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/IRQ5	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/SCK3/CRX0-C/IRQ5/ CMPC20
20	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/IRQ4	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/CTX0-C/IRQ4/CVREFC2
21	PH3/TMCI0	PH3/MTIOC4D/TMCI0
22	PH2/TMRI0/IRQ1	PH2/MTIOC4C/TMRI0/TOC1/IRQ1
23	PH1/TMO0/IRQ0	PH1/MTIOC3D/TMO0/TIC1/IRQ0/ADST0
24	PH0/CACREF	PH0/MTIOC3B/CACREF/ADTRG0#
25	P55/MTIOC4D/TMO3	P55/MTIOC4D/MTIOC4A/TMO3/CRX0-D/ IRQ10
26	P54/MTIOC4B/TMCI1	P54/MTIOC4B/TMCI1/CTX0-D/IRQ4
27	PC7/MTIOC3A/TMO2/MTCLKB/TXD8/ SMOSI8/SSDA8/MISOA/CACREF	UB/PC7/MTIOC3A/MTCLKB/TMO2/ CACREF/TOC0/TXD8/SMOSI8/SSDA8/ SMOSI10/SSDA10/TXD10/TXD010-C/ SMOSI010-C/SSDA010-C/MISOA-A/IRQ14

64-Pin LFQFP/ LQFP	RX210	RX660
28	PC6/MTIOC3C/MTCLKA/TMCI2/RXD8/ SMISO8/SSCL8/MOSIA	PC6/MTIOC3C/MTCLKA/TMCI2/TIC0/RXD8/ SMISO8/SSCL8/SMISO10/SSCL10/RXD10/ RXD010-C/SMISO010-C/SSCL010-C/ MOSIA-A/IRQ13
29	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/ RSPCKA	PC5/MTIOC3B/MTCLKD/TMRI2/MTIOC0C/ SCK8/SCK10/SCK010-C/RSPCKA-A/PMC0/ IRQ5
30	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/ SCK5/CTS8#/RTS8#/SS8#/SSLA0	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/ MTIOC0A/SCK5/CTS8#/RTS8#/SS8#/ SS10#/CTS10#/RTS10#/CTS010#-B/ RTS010#-B/SS010#-B/DE010-B/SSLA0-A/ PMC0/IRQ12
31	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5/ PMC0/IRQ11
32	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/ SSLA3	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/ TXDB011-A/SSLA3-A/IRQ10
33	PB7/MTIOC3B/TXD9/SMOSI9/SSDA9	PB7/MTIOC3B/TXD9/SMOSI9/SSDA9/ SMOSI11/SSDA11/TXD11/TXD011-B/ SMOSI011-B/SSDA011-B/IRQ15
34	PB6/MTIOC3D/RXD9/SMISO9/SSCL9	PB6/MTIOC3D/RXD9/SMISO9/SSCL9/ SMISO11/SSCL11/RXD11/RXD011-B/ SMISO011-B/SSCL011-B/IRQ6
35	PB5/MTIOC2A/MTIOC1B/TMRI1/POE1#/ SCK9	PB5/MTIOC2A/MTIOC1B/TMRI1/POE4#/ TOC2/SCK9/SCK11/SCK011-B/IRQ13
36	PB3/MTIOC0A/MTIOC4A/TMO0/POE3#/ SCK6	PB3/MTIOC0A/MTIOC4A/TMO0/POE11#/ TIC2/SCK4/SCK6/PMC0/IRQ3
37	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD6/ SMOSI6/SSDA6/IRQ4-DS	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD4/ SMOSI4/SSDA4/TXD6/SMOSI6/SSDA6/ IRQ4-DS/COMP1
38	VCC	VCC
39	PB0/MTIC5W/RXD6/SMISO6/SSCL6/ RSPCKA	PB0/MTIC5W/MTIOC3D/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/RSPCKA-C/ IRQ12
40	VSS	VSS
41	PA6/MTIC5V/MTCLKB/TMCI3/POE2#/ CTS5#/RTS5#/SS5#/MOSIA	PA6/MTIC5V/MTCLKB/TMCI3/POE10#/ MTIOC3D/MTIOC6B/CTS5#/RTS5#/SS5#/ CTS12#/RTS12#/SS12#/MOSIA-B/IRQ14
42	PA4/MTIC5U/MTCLKA/TMRI0/TXD5/ SMOSI5/SSDA5/SSLA0/IRQ5-DS/CVREFB1	PA4/MTIC5U/MTCLKA/TMRI0/MTIOC4C/ MTIOC7C/TXD5/SMOSI5/SSDA5/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLA0-B/IRQ5-DS/CVREFC1/ADST0
43	PA3/MTIOC0D/MTCLKD/RXD5/SMISO5/ SSCL5/IRQ6-DS/CMPB1	PA3/MTIOC0D/MTCLKD/MTIC5V/MTIOC4D/ RXD5/SMISO5/SSCL5/IRQ6-DS/CMPC10
44	PA1/MTIOC0B/MTCLKC/SCK5/SSLA2/ CVREFA	PA1/MTIOC0B/MTCLKC/MTIOC7B/ MTIOC3B/SCK5/SCK12/SSLA2-B/IRQ11/ ADTRG0#
45	PA0/MTIOC4A/SSLA1/CACREF	PA0/MTIOC4A/CACREF/MTIOC6D/ SSLA1-B/IRQ0
46	PE5/MTIOC4C/MTIOC2B/IRQ5/AN013	PE5/MTIOC4C/MTIOC2B/IRQ5/AN013/ COMP0
47	PE4/MTIOC4D/MTIOC1A/AN012/CMPA2	PE4/MTIOC4D/MTIOC1A/MTIOC4A/ MTIOC7D/IRQ12/AN012

64-Pin LFQFP/ LQFP	RX210	RX660
48	PE3/MTIOC4B/POE8#/CTS12#/RTS12#/ SS12#/AN011/CMPA1	PE3/MTIOC4B/POE8#/MTIOC1B/TOC3/ CTS12#/RTS12#/SS12#/IRQ11/AN011
49	PE2/MTIOC4A/RXD12/RXDX12/SMISO12/ SSCL12/IRQ7-DS/AN010/CVREFB0	PE2/MTIOC4A/MTIOC7A/TIC3/RXD12/ SMISO12/SSCL12/RXDX12/IRQ7-DS/ AN010/CVREFC0
50	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12/AN009/CMPB0	PE1/MTIOC4C/MTIOC3B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/IRQ9/AN009/ CMPC00
51	PE0/SCK12/AN008	PE0/MTIOC3D/SCK12/IRQ8/AN008
52	VREFL	P47/IRQ15-DS/AN007
53	P46/AN006	P46/IRQ14-DS/AN006
54	VREFH	P45/IRQ13-DS/AN005
55	P44/AN004	P44/IRQ12-DS/AN004
56	P43/AN003	P43/IRQ11-DS/AN003
57	P42/AN002	P42/IRQ10-DS/AN002
58	P41/AN001	P41/IRQ9-DS/AN001
59	VREFL0	VREFL0/PJ7
60	P40/AN000	P40/IRQ8-DS/AN000
61	VREFH0	VREFH0/PJ6
62	AVCC0	AVCC0
63	P05/DA1	P07/IRQ15/ADTRG0#
64	AVSS0	AVSS0

Notes: 1. The I/O buffer power supply for these pins is AVCC0.
2. Not present on products not provided with a sub-clock oscillator.
3. Not present on products provided with a sub-clock oscillator.
4. PC0 and PC1 are valid only when the port switching function is selected.

3.5 48-Pin Package

Table 3.5 is a comparative listing of the pin functions of 48-pin package products.

Table 3.5 Comparative Listing of 48-Pin Package Pin Functions

48-Pin LFQFP/ HWQFN	RX210	RX660
1	VCL	VCL
2	MD/FINED	MD/FINED/PN6
3	RES#	RES#
4	XTAL/P37	XTAL/P37/IRQ4
5	VSS	VSS
6	EXTAL/P36	EXTAL/P36/IRQ5
7	VCC	VCC
8	P35/NMI	P35/NMI
9	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/ IRQ1-DS	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/ IRQ1-DS
10	P30/MTIOC4B/TMRI3/POE8#/RXD1/ SMISO1/SSCL1/IRQ0-DS	P30/MTIOC4B/POE8#/RXD1/SMISO1/ SSCL1/IRQ0-DS/COMP3
11	P27/MTIOC2B/TMCI3/SCK1	P27/MTIOC2B/SCK1/IRQ7/CVREFC3
12	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/ CTS3#/RTS3#/SS3#/IRQ6/CMPC30
13	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ SCK1/MISOA/SDA-DS/IRQ7	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ MTIOC4B/SCK1/TXD3/SMOSI3/SSDA3/ MISOA-C/SDA2/IRQ7/COMP2
14	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/ SMOSI1/SSDA1/MOSIA/SCL-DS/IRQ6/ ADTRG0#	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/ SMOSI1/SSDA1/RXD3/SMISO3/SSCL3/ MOSIA-C/SCL2/IRQ6/ADTRG0#
15	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/IRQ5	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/SCK3/CRX0-C/IRQ5/ CMPC20
16	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/IRQ4	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/CTX0-C/IRQ4/CVREFC2
17	PH3/TMCI0	PH3/MTIOC4D/TMCI0
18	PH2/TMRI0/IRQ1	PH2/MTIOC4C/TMRI0/TOC1/IRQ1
19	PH1/TMO0/IRQ0	PH1/MTIOC3D/TMO0/TIC1/IRQ0/ADST0
20	PH0/CACREF	PH0/MTIOC3B/CACREF/ADTRG0#
21	PC7/MTIOC3A/TMO2/MTCLKB/TXD8/ SMOSI8/SSDA8/MISOA/CACREF	UB/PC7/MTIOC3A/MTCLKB/TMO2/ CACREF/TOC0/TXD8/SMOSI8/SSDA8/ SMOSI10/SSDA10/TXD10/TXD010-C/ SMOSI010-C/SSDA010-C/MISOA-A/IRQ14
22	PC6/MTIOC3C/MTCLKA/TMCI2/RXD8/ SMISO8/SSCL8/MOSIA	PC6/MTIOC3C/MTCLKA/TMCI2/TIC0/RXD8/ SMISO8/SSCL8/SMISO10/SSCL10/RXD10/ RXD010-C/SMISO010-C/SSCL010-C/ MOSIA-A/IRQ13
23	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/ RSPCKA	PC5/MTIOC3B/MTCLKD/TMRI2/MTIOC0C/ SCK8/SCK10/SCK010-C/RSPCKA-A/PMC0/ IRQ5
24	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/ SCK5/CTS8#/RTS8#/SS8#/SSLA0	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/ MTIOC0A/SCK5/CTS8#/RTS8#/SS8#/ SS10#/CTS10#/RTS10#/CTS010#-B/ RTS010#-B/SS010#-B/DE010-B/SSLA0-A/ PMC0/IRQ12

48-Pin LFQFP/ HWQFN	RX210	RX660
25	PB5/MTIOC2A/MTIOC1B/TMRI1/POE1#	PB5/MTIOC2A/MTIOC1B/TMRI1/POE4#/ TOC2/IRQ13
26	PB3/MTIOC0A/MTIOC4A/TMO0/POE3#/ SCK6	PB3/MTIOC0A/MTIOC4A/TMO0/POE11#/ TIC2/SCK4/SCK6/PMC0/IRQ3
27	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD6/ SMOSI6/SSDA6/IRQ4-DS	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD4/ SMOSI4/SSDA4/TXD6/SMOSI6/SSDA6/ IRQ4-DS/COMP1
28	VCC	VCC
29	PB0/MTIC5W/RXD6/SMISO6/SSCL6/ RSPCKA	PB0/MTIC5W/MTIOC3D/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/RSPCKA-C/ IRQ12
30	VSS	VSS
31	PA6/MTIC5V/MTCLKB/TMCI3/POE2#/ CTS5#/RTS5#/SS5#/MOSIA	PA6/MTIC5V/MTCLKB/POE10#/MTIOC3D/ CTS5#/RTS5#/SS5#/CTS12#/RTS12#/ SS12#/MOSIA-B/IRQ14
32	PA4/MTIC5U/MTCLKA/TMRI0/TXD5/ SMOSI5/SSDA5/SSLA0/IRQ5-DS/CVREFB1	PA4/MTIC5U/MTCLKA/TMRI0/MTIOC4C/ MTIOC7C/TXD5/SMOSI5/SSDA5/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLA0-B/IRQ5-DS/CVREFC1/ADST0
33	PA3/MTIOC0D/MTCLKD/RXD5/SMISO5/ SSCL5/IRQ6-DS/CMPB1	PA3/MTIOC0D/MTCLKD/MTIC5V/MTIOC4D/ RXD5/SMISO5/SSCL5/IRQ6-DS/CMPC10
34	PA1/MTIOC0B/MTCLKC/SCK5/SSLA2/ CVREFA	PA1/MTIOC0B/MTCLKC/MTIOC7B/ MTIOC3B/SCK5/SCK12/SSLA2-B/IRQ11/ ADTRG0#
35	PE4/MTIOC4D/MTIOC1A/AN012/CMPA2	PE4/MTIOC4D/MTIOC1A/MTIOC4A/ MTIOC7D/IRQ12/AN012
36	PE3/MTIOC4B/POE8#/CTS12#/RTS12#/ AN011/CMPA1	PE3/MTIOC4B/POE8#/MTIOC1B/TOC3/ CTS12#/RTS12#/SS12#/IRQ11/AN011
37	PE2/MTIOC4A/RXD12/RXDX12/SSCL12/ IRQ7-DS/AN010/CVREFB0	PE2/MTIOC4A/MTIOC7A/TIC3/RXD12/ SMISO12/SSCL12/RXDX12/IRQ7-DS/ AN010/CVREFC0
38	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/ SSDA12/AN009/CMPB0	PE1/MTIOC4C/MTIOC3B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/IRQ9/AN009/ CMPC00
39	VREFL	P47/IRQ15-DS/AN007
40	P46/AN006	P46/IRQ14-DS/AN006
41	VREFH	P45/IRQ13-DS/AN005
42	P42/AN002	P42/IRQ10-DS/AN002
43	P41/AN001	P41/IRQ9-DS/AN001
44	VREFL0	VREFL0/PJ7
45	P40/AN000	P40/IRQ8-DS/AN000
46	VREFH0	VREFH0/PJ6
47	AVCC0	AVCC0
48	AVSS0	AVSS0

4. Important Information when Migrating Between MCUs

This section presents important information on differences between the RX660 Group and the RX210 Group. 4.1, Notes on Functional Design, presents information regarding the software.

4.1 Notes on Functional Design

Some software that runs on the RX210 Group is compatible with the RX660 Group. Nevertheless, appropriate caution must be exercised due to differences in aspects such as operation timing and electrical characteristics.

Software-related considerations regarding function settings that differ between the RX660 Group and RX210 Group are as follows:

For differences between modules and functions, refer to 2, Comparative Overview of Specifications. For further information, refer to the User's Manual: Hardware of each MCU group, listed in 5, Reference Documents.

4.1.1 VCL Pin (External Capacitor)

Connect a smoothing capacitor rated at 0.47 µF to the VCL pin of the RX660 Group for stabilization of the internal power supply.

4.1.2 Main Clock Oscillator

When connecting an oscillator to the EXTAL or XTAL pin on the RX660 Group, select an oscillator with an oscillation frequency of 8 MHz to 24 MHz.

4.1.3 Transition to Boot Mode (FINE Interface)

On the RX660 Group a transition to boot mode (FINE interface) occurs when the MD pin is low-level at the time of release from a reset and is then switched to high-level within 20 to 100 msec. For details on operating modes, refer to RX660 Group User's Manual: Hardware, listed in section 5, Reference Documents.

4.1.4 RTS2# Pin of Serial Communications Interface

The RTS2# pin of the serial communications interface is multiplexed with P54 on the RX210 Group and with P54 and PJ5 on the RX660 Group. Keep this in mind when designing systems.

4.1.5 RTS10# Pin of Serial Communications Interface

The RTS10# pin of the serial communications interface is multiplexed with P83 on the RX210 Group and with PC4 on the RX660 Group. Keep this in mind when designing systems.

4.1.6 RTS11# Pin of Serial Communications Interface

The RTS11# pin of the serial communications interface is multiplexed with P74 on the RX210 Group and with PB4 on the RX660 Group. Keep this in mind when designing systems.

4.1.7 RTS12# Pin of Serial Communications Interface

The RTS12# pin of the serial communications interface is multiplexed with PE3 on the RX210 Group and with PA6 and PE3 on the RX660 Group. Keep this in mind when designing systems.

4.1.8 Mode Setting Pins

The mode setting pins when a reset is canceled are the MD and PC7 pins on the RX210 Group and the MD and UB pins on the RX660 Group.

4.1.9 Software Configurable Interrupts

Software configurable interrupt functionality has been added to the RX660 Group. This allows selection of a single interrupt source from among multiple peripheral module interrupt sources for assignment to each interrupt vector number from 128 to 255. These interrupts are classified as either software configurable interrupt B or software configurable interrupt A according to the operating clock of the corresponding peripheral modules. For details of the software configurable interrupt functionality, refer to RX660 Group User's Manual: Hardware, listed in section 5, Reference Documents.

4.1.10 Usage of Flash Memory Commands

On the RX210 Group the flash memory is programmed and erased by issuing FCU commands to the FCU. On the RX660 Group the flash memory is programmed, erased, etc., by first transitioning to a dedicated sequencer mode for programming and erasing the ROM and then issuing FACI commands.

Table 4.1 is a comparison of the specifications of the FCU and FACI commands.

Table 4.1 Specification Comparison of FCU and FACI Commands

Item	FCU Command (RX210)	FACI Command (RX660)
Command issuance area	Programming/erasure address (00F8 0000h to 00FF FFFFh)	—
Usable commands	• P/E normal mode transition • Status read mode transition • Lock bit read mode transition (lock bit read 1) • Peripheral clock notification • Programming • Block erase • P/E suspend • P/E resume • Status register clear • Lock bit read 2/blank checking	• Programming • Block erase • Forced end • Blank checking • Configuration settings • Lock bit program • P/E suspend • P/E resume • Status clear

4.1.11 Clock Frequency Settings

On the RX660 Group the frequencies of the system clock (ICLK) and peripheral module clocks A, B, and D (PCLKA, PCLKB, and PCLKD) must be set so that they fall within the ranges indicated below.

- PCLKA ≥ PCLKB
- PCLKB:PCLKD = 1:1, 2:1, 4:1, or 1:2

4.1.12 Voltage Level Settings

On the RX660 Group the settings of the voltage level setting register (VOLSR) associated with the operating mode, the voltage detection level select register (LVDLVLR) of the voltage detection circuit, and option function select register 1 (OFS1) of the option-setting memory must be changed to appropriate values according to the operating voltage. Make sure to set these values using a program.

4.1.13 RIIC Operating Voltage Setting

When using the RIIC on the RX660 Group, it is necessary to specify the power supply voltage range to preserve the slope characteristics. VCC is set to a value of 4.5 V or greater by default. If it is set to a value less than 4.5 V, make sure to change the voltage range before activating the RIIC. For details, refer to the description of the VOLSR.RICVLS bit in RX660 Group User's Manual: Hardware.

4.1.14 Option-Setting Memory

On the RX210 Group the ID code protection codes and ID code protection codes for the on-chip debugger are located in the ROM, but on the RX660 Group they are located in the option-setting memory. Note that the setting configuration procedures are different.

4.1.15 PLL Circuit

The frequency multiplication factor of the PLL circuit can be set to ×8 to ×25 on the RX210 Group and to ×10 or ×30 (in ×0.5 increments) on the RX660 Group. To use the PLL circuit, change the setting of the PLLCR.STC bits to an appropriate value.

4.1.16 Exception Vector Table

The address of the vector table is fixed on the RX210 Group, but on the RX660 Group the vector table is relocatable using the value set in the exception table register (EXTB) as the start address.

4.1.17 Performing RAM Self-Diagnostics on Save Register Banks

On the RX660 Group save register banks are configured in the RAM. The save register banks are provided with a buffer, so when a SAVE instruction is used to write data to a register and then a RSTR instruction is used to read data from the same register, the data is actually read from the buffer and not from the RAM memory cells. When performing self-diagnostics on the RAM in a save register bank, use the following sequence of steps for checking the written data in order to prevent the data from being read from the buffer:

1. Use the SAVE instruction to write data to the bank that is the target of the diagnostic test.
2. Use the SAVE instruction to write data to a bank other than that written to in step 1.
3. Use the RSTR instruction to read data from the bank written to in step 1.

4.1.18 Restrictions on Compare Function

The compare function of the 12-bit A/D converter on the RX660 Group is subject to the following restrictions.

1. The compare function cannot be used together with the self-diagnosis function or double trigger mode. (The compare function is not available for the ADRD, ADDBLDR, ADDBLDRA, and ADDBLDRB registers.)
2. It is necessary to specify single scan mode when using match or mismatch event outputs.
3. When the temperature sensor or internal reference voltage is selected for window A, window B operations are disabled.
4. When the temperature sensor or internal reference voltage is selected for window B, window A operations are disabled.
5. It is not possible to set the same channel for window A and window B.
6. It is necessary to set the reference voltage values such that the high-side reference voltage value is equal to or larger than the low-side reference voltage value.

4.1.19 MOSCWTCR Register

On the RX210 Group this register counts cycles of the main clock, but on the RX660 Group it counts cycles of the LOCO clock.

4.1.20 Eliminating I²C Bus Interface Noise

The RX210 Group has integrated analog noise filters on the SCL and SDA lines, but the RX660 Group has no integrated analog noise filters.

4.1.21 Initialization of Port Direction Register (PDR)

The method of initializing the PDR register differs between the RX210 Group and RX660 Group, even on products with the same pin count.

4.1.22 MTIOC Pin Output Level when Counter Stops

During operation with the MTIOC pin set to output, writing 0 to a CSTn bit in TSTRA or TSTR causes the corresponding counter to stop. At this point, in complementary PWM mode or reset-synchronized PWM mode on the RX660 Group, the output on the MTIOC pin is at the initial output level set in the TOCR1A or TOCR2A register. In other than complementary PWM mode or reset-synchronized PWM mode, the output compare output level of the MTIOC pin is maintained. The specified initial output level is changed if a write to the TIOR register is performed when the value of the CSTn bit is 0.

4.1.23 A/D Conversion Start Requests in Complementary PWM Mode

To generate PWM waveforms in complementary PWM mode on the RX660 Group, MTU4.TGRA (MTU7.TGRA) compare match detection is performed with not only MTU4.TCNT (MTU7.TCNT) but also with MTU3.TCNT (MTU6.TCNT) or TCNTSA (TCNTSB).

Therefore, TRGA4N (TRGA7N) is also generated when a compare match with MTU3.TCNT (MTU6.TCNT) or TCNTSA (TCNTSB) occurs. When operating MTU3 and MTU4 (MTU6 and MTU7) in complementary PWM mode to generate A/D conversion start requests, use compare match between MTU4.TCNT (MTU7.TCNT) and MTU4.TADCORA or TADCORB (MTU7.TADCORA or TADCORB) as the A/D conversion start request.

4.1.24 High-Impedance Control of Unselected MTU Pins

On the RX660 Group, when high-impedance control is enabled for MTU pins in the POECR1 or POECR2 register and the control conditions are met, output on the pins multiplexed with the MTU function enters the high-impedance state regardless of whether or not the MTU function is selected. To prevent pin output from entering the high-impedance state unexpectedly, make settings such that the MTU pins selected in the PmnPFS register of the MPC and the MTU pins selected in the pin selection register of the POE3 match.

4.1.25 A/D Scan Conversion End Interrupt Generation

On the RX660 Group, when a scan is started by a software trigger and the ADIE bit has been set to 1, an A/D scan conversion end interrupt is generated when the scan ends, even if double trigger mode is selected.

4.1.26 Input Buffer Control by DIRQnE Bits (n = 0 to 15)

On the RX660 Group, setting a DPSIERy.DIRQnE (y = 0 or 1, n = 0 to 15) bit to 1 enables the input buffer of the corresponding pin among IRQ0-DS to IRQ15-DS. Note that once the input buffer is enabled, inputs on these pins are sent to the corresponding DPSIFRy.DIRQnF (y = 0 or 1, n = 0 to 15) bits, but they are not sent to the interrupt controller, peripheral modules, and I/O ports.

4.1.27 Scan Conversion Time of 12-Bit A/D Converter

The scan conversion time differs between the RX210 Group and RX660 Group. The scan conversion time (t_{SCAN}) for each group of a single scan where the number of selected channels is n is expressed by the equations below. For details, refer to the description of the 12-bit A/D converter analog input sampling time and scan conversion time in the User's Manual: Hardware of the RX210 Group and RX660 Group, listed in section 5, Reference Documents.

RX210: $t_{SCAN} = t_D + (t_{DIS} \times n) + t_{DIAG} + (t_{CONV} \times n) + t_{ED}$

RX660: $t_{SCAN} = t_D + (t_{DIS} \times n) + t_{DIAG} + (t_{CONV} \times n) + t_{ED}$

t_{SCAN} (when converting temperature sensor output or internal reference voltage) $= t_D + (t_{ADIS} \times m) + (t_{CONV} \times m) + t_{ED}$

t_D	Start-of-scanning-delay time
t_{SPL}	Sampling time
t_{DIS}	Disconnection detection assist processing time
t_{DIAG}	Self-diagnosis A/D conversion processing time
t_{CONV}	A/D conversion processing time
t_{ED}	End-of-scanning-delay time
t_{ADIS}	Auto-discharge processing time during A/D conversion of temperature sensor output and internal reference voltage

4.1.28 D/A Converter Settings

When configuring D/A converter settings on the RX660 Group, first set comparator C as the output destination in the D/A destination select register (DADSELR) and wait for the D/A converter output to stabilize before enabling comparator operation.

Similarly, stop the comparator temporarily before making changes to the settings of the D/A converter, then wait for the D/A converter output to stabilize before enabling comparator operation.

4.1.29 Comparator C Operation in Module Stop State

On the RX660 Group the analog circuits of comparator C do not stop operating if a transition to the module stop state is made while comparator C is operating, so the analog power current associated with comparator C remains unchanged. If it is necessary to reduce analog power current consumption in the module stop state, stop operation of comparator C by clearing the CMPCTL.HCMPON bit to 0.

4.1.30 Comparator C Operation in Software Standby Mode

On the RX660 Group the analog circuits of comparator C do not stop operating if a transition to software standby mode is made while comparator C is operating, so the analog power current associated with comparator C remains unchanged. If it is necessary to reduce analog power current consumption in software standby mode, stop operation of comparator C by clearing the CMPCTL.HCMPON bit to 0.

4.1.31 Interrupt Requests in Software Standby Mode

When an interrupt request occurs in software standby mode but the interrupt source is not set as a source for exiting software standby mode, the request is held in the interrupt controller. The request is handled after exiting by another interrupt source. Note that interrupt requests for external pin interrupts are not held.

4.1.32 Timer Mode Register Setting for ELC Event Input

To set the MTU to ELC action operation on the RX660 Group, set the timer mode register (TMDR) of the relevant channel to its initial value (00h).

4.1.33 Differences Among Chip Versions

There are differences in functionality among the different chip versions of RX210 Group MCUs. Refer to the table below for details.

Section		Specification Differences		
		Chip Version A	**Chip Version C**	**Chip Version B**
9. Clock Generation Circuit	9.2.2 System Clock Control Register 3 (SCKCR3)	The main clock oscillator cannot be selected as the clock source.	The main clock oscillator can be selected as the clock source.	← (Same as at left)
	9.2.17 PLL Power Control Register (PLLPCR)	There is no PLLPCR register. Therefore, there is no functionality for powering off the PLL to reduce power consumption.	← (Same as at left)	The PLLPCR register has been added. This provides functionality to power off the PLL to reduce power consumption when the PLL will not be used.
10. Clock Frequency Accuracy Measurement Circuit (CAC)	10.2.2 CAC Control Register 1 (CACR1)	The output clock of the main clock oscillator cannot be selected as the frequency measurement clock.	The output clock of the main clock oscillator can be selected as the frequency measurement clock.	← (Same as at left)
	10.2.3 CAC Control Register 2 (CACR2)	The output clock of the main clock oscillator cannot be selected as the reference signal generation clock.	The output clock of the main clock oscillator can be selected as the reference signal generation clock.	← (Same as at left)
11. Low Power Consumption	11.2.5 Operating Power Control Register (OPCCR)	Middle-speed operating modes 2A and 2B are not implemented.	← (Same as at left)	Middle-speed operating modes 2A and 2B have been added to reduce current consumption during operation.
	11.2.6 Sleep Mode Return Clock Source Switching Register (RSTCKCR)	The main clock oscillator cannot be selected as the sleep mode return clock source.	The main clock oscillator can be selected as the sleep mode return clock source.	← (Same as at left)
	11.2.18 Flash HOCO Software Standby Control Register (FHSSBYCR)	It is necessary to control the power supply for the flash memory in software standby mode.	← (Same as at left)	It is not necessary to control the power supply for the flash memory in software standby mode.
19. I/O Ports	Table 19.2 Port Functions	Port 17 is not 5 V tolerant.	Port 17 is 5 V tolerant.	← (Same as at left)

5. Reference Documents

User's Manual: Hardware

RX210 Group User's Manual: Hardware Rev.1.50 (R01UH0037EJ0150)
(The latest version can be downloaded from the Renesas Electronics website.)

RX660 Group User's Manual: Hardware Rev.1.00 (R01UH0937EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This module reflects the content of the following technical updates:

TN-RX*-A035B/E

TN-RX*-A080A/E

TN-RX*-A087A/E

TN-RX*-A094A/E

TN-RX*-A096A/E

TN-RX*-A097A/E

TN-RX*-A099A/E

TN-RX*-A107A/E

TN-RX*-A118A/E

TN-RX*-A138A/E

TN-RX*-A141A/E

TN-RX*-A147A/E

TN-RX*-A151A/E

TN-RX*-A177A/E

TN-RX*-A188A/E

TN-RX*-A193A/E

TN-RX*-A0147B/E

TN-RX*-A0231A/E

TN-RX*-A0224B/E

TN-RX*-A0239B/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jun. 23, 2022	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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