RX660 Group, RX140 Group

Differences Between the RX660 Group and the RX140 Group

Introduction

This application note is intended as a reference to points of difference in the peripheral functions, I/O registers, and pin functions between the RX660 Group and RX140 Group, as well as a guide to key points to consider when migrating between the two groups.

Unless specifically otherwise noted, the information in this application note applies to the 144-pin package version of the RX660 Group and the 80-pin package version of the RX140 Group as the maximum specifications. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the User's Manual: Hardware for the products in question.

Target Devices

RX660 Group, RX140 Group

Contents

1. Comparison of Built-In Functions of RX660 Group and RX140 Group

A comparison of the built-in functions of the RX660 Group and RX140 Group is provided below. For details of the functions, see section 2, Comparative Overview of Specifications and section 5, Reference Documents.

Table 1.1 is Comparison of Built-In Functions of RX140 Group and RX660 Group.

Table 1.1 Comparison of Built-In Functions of RX140 Group and RX660 Group

Function	RX140	RX660
CPU	●/▲	
Operating modes	▲	
Address space	●/▲	
Resets	●/▲	
Option-setting memory (OFSM)	●/▲	
Voltage detection circuit (LVDAb for RX140, and LVDA for RX660)	▲	
Clock generation circuit	▲	
Clock frequency accuracy measurement circuit (CAC)	○	
Low power consumption function	■/●/▲	
Register write protection function	▲	
Exception handling	○	
Interrupt controller (ICUb for RX140, and ICUF for RX660)	●/▲	
Buses	▲	
Memory-protection unit (MPU)	×	○
DMA controller (DMACAa)	×	○
Data transfer controller (DTCb)	○	
Event link controller (ELC)	▲	
I/O ports	■/●/▲	
Multi-function pin controller (MPC)	■/●/▲	
Multi-function timer pulse unit 2 (MTU2a for RX140) Multi-function timer pulse unit 3 (MTU3a for RX660)	●/▲	
Port Output Enable 2 (POE2a for RX140) Port Output Enable 3 (POE3a for RX660)	●/▲	
8-bit timer (TMRa for /RX140, and TMRb for RX660)	▲	
Compare match timer (CMT)	○	
Compare match timer W (CMTW)	×	○
Realtime clock (RTCB for RX140, and RTCC for RX660)	●/▲	
Low-power timer (LPTa)	○	×
Watchdog timer (WDTA)	×	○
Independent watchdog timer (IWDTa)	▲	
Serial communications interface (SCIg, SCIk, and SCIh for RX140, and SCIk, SCIm, and SCIh for RX660)	●/▲	
Serial communications interface (RSCI)	×	○
I^2C bus interface (RIICa)	▲	
CAN module (RSCAN for RX140) CAN FD module (CANFD-Lite for RX660)	●/▲	
Serial peripheral interface (RSPIc for RX140, and RSPId for RX660)	●/▲	
CRC calculator (CRC for RX140, and CRCA for RX660)	●/▲	
Capacitance-type touch sensor (CTSU2SL, CTSU2L)	○	×
Remote controller signal receiver (REMCa)	×	○
Trigonometric function calculator (TFU)	×	○
AESA	○	×

Function	RX140	RX660
RNGA	○	×
12-bit A/D converter (S12ADE for RX140, and S12ADH for RX660)	▲	
D/A converter (DAa for RX140) 12-bit D/A converter (R12DAb for RX660)	●/▲	
Temperature sensor (TEMPSA for RX140, and TEMPS for RX660)	○	
Comparator B (CMPBa for RX140) Comparator C (CMPC for RX660)	■/●/▲	
Data operation circuit (DOC for RX140, and DOCA for RX660)	▲	
RAM	■/▲	
Flash memory (FLASH)	■/●/▲	
Packages	▲	

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Register specification items that have no differences between the groups are not indicated.

2.1 CPU

Table 2.1 is Comparative Overview of CPUs.

Table 2.1 Comparative Overview of CPUs

Item	RX140	RX660
CPU	• Maximum operating frequency: 48 MHz • 32-bit RX CPU (RXv2) • Minimum instruction execution time: One instruction per clock cycle • Address space: — 4 GB, linear • Register — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • Basic instructions: 75, variable-length instruction format • Floating point instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian and big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits	• Maximum operating frequency: 120 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per clock cycle • Address space: — 4 GB, linear • Register — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • 113 instructions — Standard provided instructions: 111 Basic instructions: 77, variable-length instruction format Single-precision floating point instructions: 11 DSP instructions: 23 — Instructions for register bank save function: 2 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian and big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits
FPU	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard
Register bank save function	—	• Fast collective saving and restoration of the values of CPU registers • 16 save register banks

2.2 Operating Modes

Table 2.2 is Comparative Overview of Operating Modes, and Table 2.3 is Comparison of Operating Mode Registers.

Table 2.2 Comparative Overview of Operating Modes

Item	RX140	RX660
Operating mode by mode setting pins	Single-chip mode	Single-chip mode
	Boot mode (SCI interface)	Boot mode (SCI interface)
	—	User boot mode
	Boot mode (FINE interface)	Boot mode (FINE interface)
Operating mode by registers	—	Single-chip mode User boot mode Extended mode with on-chip ROM disabled Extended mode with on-chip ROM enabled

Table 2.3 Comparison of Operating Mode Registers

Register	Bit	RX140	RX660
MDSR	—	—	Mode status register
SYSCR0	—	—	System control register 0
SYSCR1	—	System control register 1	System control register 1
		Initial value after a reset differs.	
VOLSR	—	—	Voltage level setting register

2.3 Address Space

Figure 2.1 is Comparison of Memory Maps in Single-Chip Mode.

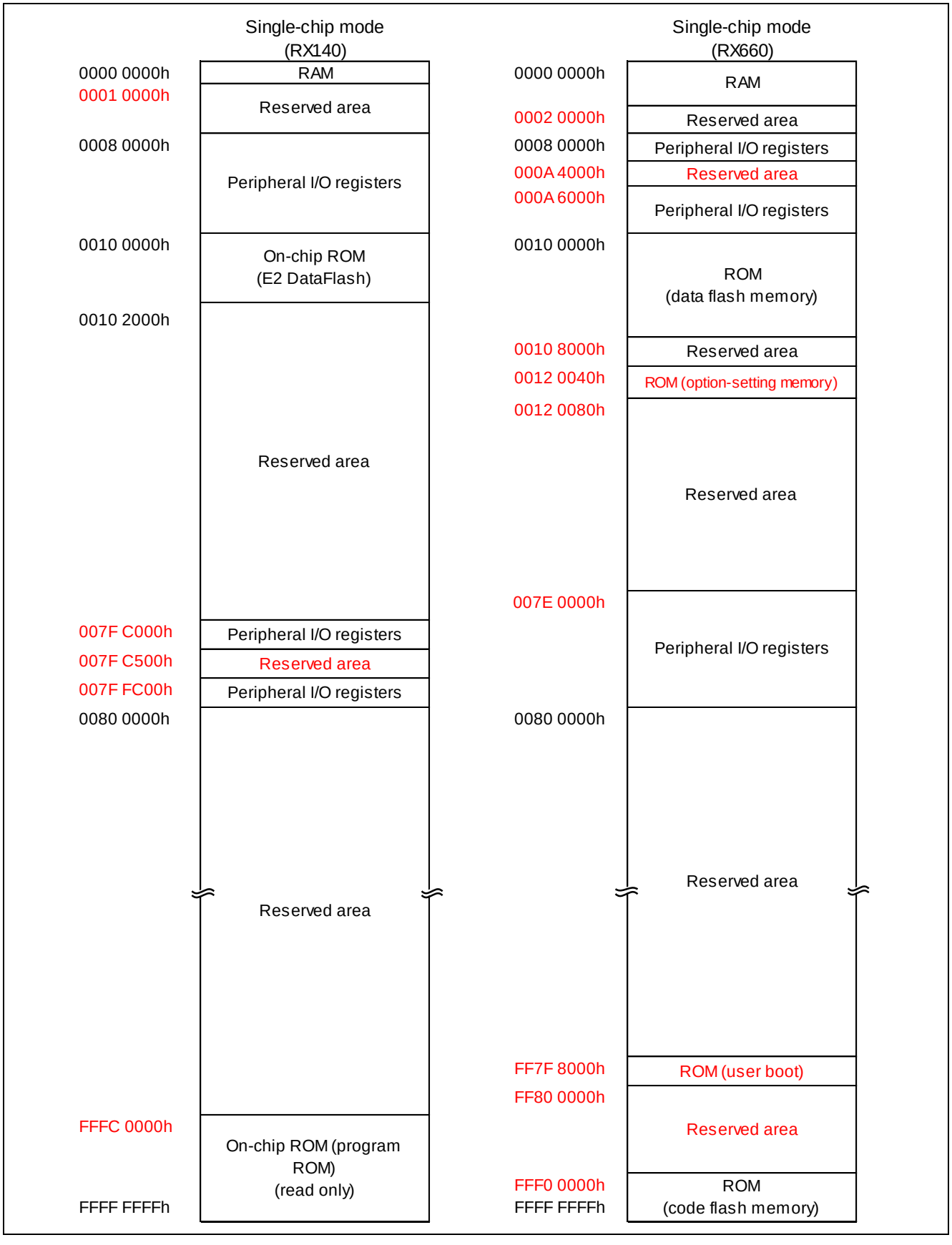

Figure 2.1 Comparison of Memory Maps in Single-Chip Mode

2.4 Reset

Table 2.4 is Comparative Overview of Resets, and Table 2.5 is Comparison of Reset-Related Registers.

Table 2.4 Comparative Overview of Resets

Item	RX140	RX660
RES# pin reset	Voltage input to the RES# pin is driven low.	Voltage input to the RES# pin is driven low.
Power-on reset	VCC rises (voltage monitored: VPOR)	VCC rises (voltage monitored: VPOR)
Voltage monitoring 0 reset	VCC falls (voltage monitored: Vdet0)	VCC falls (voltage monitored: Vdet0)
Voltage monitoring 1 reset	VCC falls (voltage monitored: Vdet1)	VCC falls (voltage monitored: Vdet1)
Voltage monitoring 2 reset	VCC falls (voltage monitored: Vdet2)	VCC falls (voltage monitored: Vdet2)
Deep software standby reset	—	Exiting deep software standby mode by interrupt
Independent watchdog timer reset	Independent watchdog timer underflow or refresh error	Independent watchdog timer underflow or refresh error
Watchdog timer reset	—	Watchdog timer underflow or refresh error
Software reset	Register setting	Register setting

Table 2.5 Comparison of Reset-Related Registers

Register	Bit	RX140	RX660
RSTSR0	DPSRSTF	—	Deep software standby reset flag
RSTSR2	WDTRF	—	Watchdog timer reset detect flag

2.5 Option-Setting Memory

Figure 2.2 is Comparison of Option-Setting Memory Areas, and Table 2.6 is Comparison of Option-Setting Memory Registers.

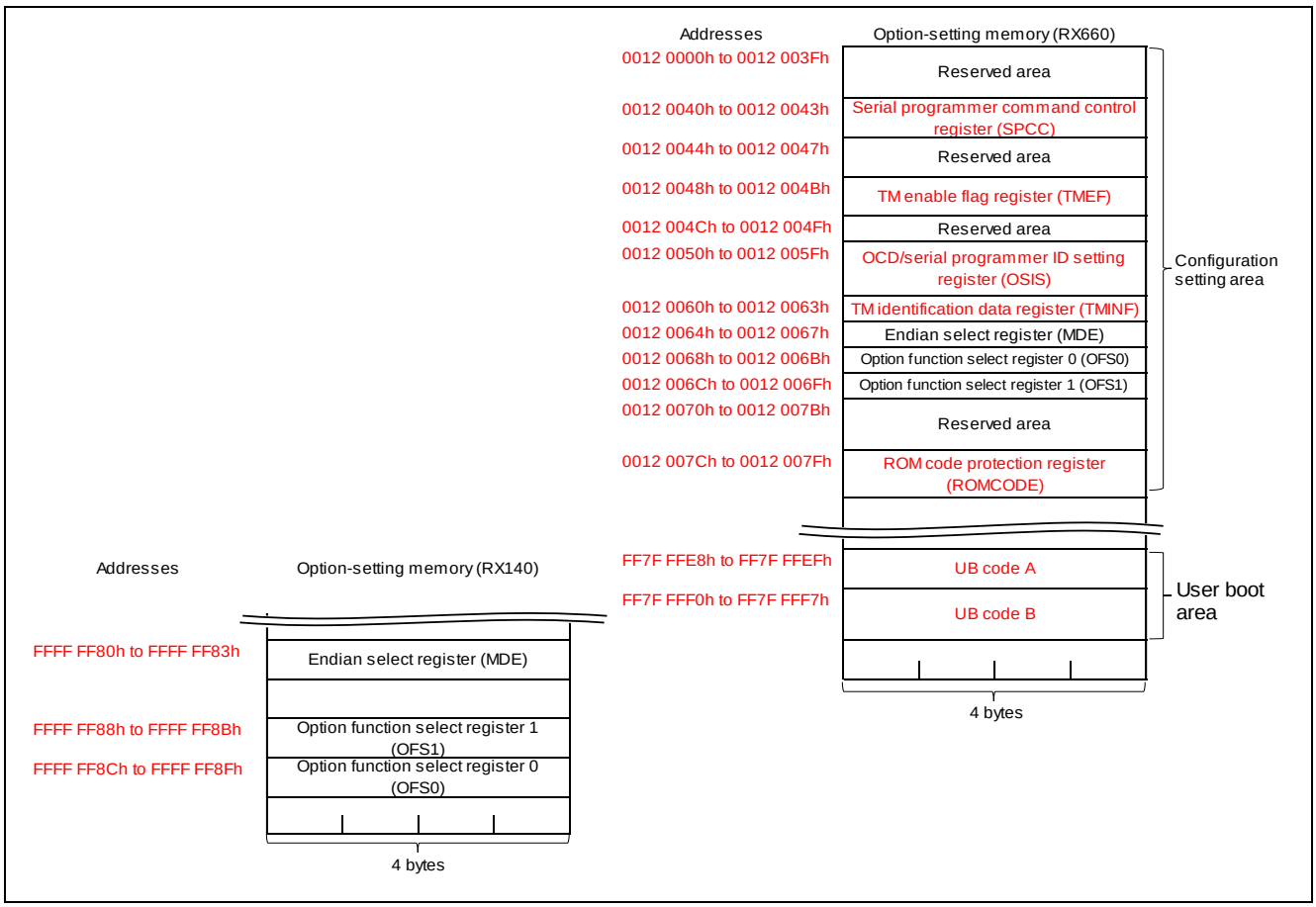

Figure 2.2 Comparison of Option-Setting Memory Areas

Table 2.6 Comparison of Option-Setting Memory Registers

Register	Bit	RX140 (OFSM)	RX660 (OFSM)
SPCC	—	—	Serial programmer command control register
OSIS	—	—	OCD/serial programmer ID setting register
OFS0	IWDTTOPS[1:0]	IWDT timeout period select bits b3 b2 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1,024 cycles (03FFh) 1 1: 2,048 cycles (07FFh)	IWDT timeout period select bits b3 b2 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh)
	IWDTRSTIRQS	IWDT reset interrupt request select bit 0: Non-maskable interrupt request is enabled 1: Reset is enabled	IWDT reset interrupt request select bit 0: Non-maskable interrupt request or plain interrupt request is enabled 1: Reset is enabled
	IWDTSLCSTP	IWDT sleep mode count stop control bit 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, or deep sleep mode	IWDT sleep mode count stop control bit 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, deep software standby, or all-module clock stop mode.
	WDTSTRT	—	WDT start mode select bit
	WDTTOPS[1:0]	—	WDT timeout period select bits
	WDTCKS[3:0]	—	WDT clock frequency division ratio select bits
	WDTRPES[1:0]	—	WDT window end position select bits
	WDTRPSS[1:0]	—	WDT window start position select bits
	WDTRSTIRQS	—	WDT reset interrupt request select bit
OFS1	VDSEL	Voltage detection 0 level select bits b1 b0 0 0: 3.84 V is selected 0 1: 2.82 V is selected 1 0: 2.51 V is selected 1 1: 1.90 V is selected	Voltage detection 0 level select bits b1 b0 0 0: Reserved 0 1: Reserved 1 0: 2.83 V is selected 1 1: 4.22 V is selected
	HOCOFRQ[1:0]	HOCO frequency selection bits	—
TMEF	—	—	TM enable flag register
TMINF	—	—	TM identification data register
ROMCODE	—	—	ROM code protection register

2.6 Voltage Detection Circuit

Table 2.7 is Comparative Overview of Voltage Detection Circuits, and Table 2.8 is Comparison of Voltage Detection Circuit Registers.

Table 2.7 Comparative Overview of Voltage Detection Circuits

Item		RX140 (LVDAb)			RX660 (LVDA)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	When voltage drops below Vdet0	When voltage rises above or drops below Vdet1	When voltage rises above or drops below Vdet2 Input voltage can be switched to VCC or CMPA2 pins using the LVCMPCR. EXVCCINP2 bit.	When voltage drops below Vdet0	When voltage rises above or drops below Vdet1	When voltage rises above or drops below Vdet2
	Detection voltage	Selectable from 4 levels using the OFS1 register	Selectable from 14 levels using LVDLVLR. LVD1LVL[3:0] bits	Selectable from 4 levels using LVDLVLR. LVD2LVL[3:0] bits	Selectable from 2 levels using OFS1. VDSE[1:0] bits	Selectable from 5 levels using LVDLVLR. LVD1LVL[3:0] bits	Selectable from 5 levels using LVDLVLR. LVD2LVL[3:0] bits
	Monitoring flag	Not available	LVD1SR. LVD1MON Flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR. LVD2MON Flag: Monitors whether voltage is higher or lower than Vdet2	Not available	LVD1SR. LVD1MON Flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR. LVD2MON Flag: Monitors whether voltage is higher or lower than Vdet2
			LVD1SR. LVD1DET Flag: Vdet1 passage detection	LVD2SR. LVD2DET Flag: Vdet2 passage detection		LVD1SR. LVD1DET Flag: Vdet1 passage detection	LVD2SR. LVD2DET Flag: Vdet2 passage detection
Process upon voltage detection	Reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet0 > VCC: CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC or CMPA2: CPU restart timing selectable: after specified time with VCC or CMPA2 > Vdet2 or after specified time with Vdet2 > VCC or CMPA2	Reset when Vdet0 > VCC: CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet2 or Vdet2 > VCC

Item		RX140 (LVDAb) Voltage Monitoring 0	RX140 (LVDAb) Voltage Monitoring 1	RX140 (LVDAb) Voltage Monitoring 2	RX660 (LVDA) Voltage Monitoring 0	RX660 (LVDA) Voltage Monitoring 1	RX660 (LVDA) Voltage Monitoring 2
Process upon voltage detection	Interrupt	Not available	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	Not available	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
			Selectable between non-maskable or maskable interrupt	Selectable between non-maskable or maskable interrupt		Selectable between non-maskable or maskable interrupt	Selectable between non-maskable or maskable interrupt
			Interrupt request issued when Vdet1 >VCC and/or VCC > Vdet1	Interrupt request issued when Vdet2 > VCC or CMPA2, and/or VCC or CMPA2 > Vdet2		Interrupt request issued when Vdet1 >VCC and/or VCC > Vdet1	Interrupt request issued when Vdet2 >VCC and/or VCC > Vdet2
Digital filter	Enable/ disable switching	—	—	—	Digital filter not available	Available	Available
	Sampling time	—	—	—	—	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)
Event link function		Not available	Available Output of event signals on detection of Vdet1 crossings	Not available	Not available	Available Output of event signals on detection of Vdet1 crossings	Available Output of event signals on detection of Vdet2 crossings

Table 2.8 Comparison of Voltage Detection Circuit Registers

Register	Bit	RX140 (LVDAb)	RX660 (LVDA)
LVD2CR1	LVD2IDTSEL [1:0]	Voltage monitoring 2 interrupt occurrence condition select bits b1 b0 0 0: When VCC or CMPA2 ≥ Vdet2 (rise) detected 0 1: When VCC or CMPA2 < Vdet2 (fall) detected 1 0: When rise and fall detected 1 1: Setting prohibited	Voltage monitoring 2 interrupt occurrence condition select bits b1 b0 0 0: When VCC ≥ Vdet2 (rise) detected 0 1: When VCC < Vdet2 (fall) detected 1 0: When rise and fall detected 1 1: Setting prohibited
LVD2SR	LVD2MON	Voltage monitoring 2 signal monitoring flag 0: VCC or CMPA2 < Vdet2 1: VCC or CMPA2 ≥ Vdet2, or LVD2MON disabled	Voltage monitoring 2 signal monitoring flag 0: VCC < Vdet2 1: VCC ≥ Vdet2 or LVD2MON disabled
LVCMPCR	EXVCCINP2	Voltage detection 2 comparison voltage external input select bit*1	—
LVDLVLR	LVD1LVL [3:0]	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 0 0 0: 4.29 V 0 0 0 1: 4.16 V 0 0 1 0: 4.03 V 0 0 1 1: 3.86 V 0 1 0 0: 3.10 V 0 1 0 1: 3.00 V 0 1 1 0: 2.90 V 0 1 1 1: 2.80 V 1 0 0 0: 2.68 V 1 0 0 1: 2.59 V 1 0 1 0: 2.48 V 1 0 1 1: 2.20 V 1 1 0 0: 1.96 V 1 1 0 1: 1.86 V Settings other than the above are prohibited.	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 1 0 0: 4.57 V (Vdet1_0) 0 1 0 1: 4.47 V (Vdet1_1) 0 1 1 0: 4.32 V (Vdet1_2) 1 0 1 0: 2.93 V (Vdet1_3) 1 0 1 1: 2.88 V (Vdet1_4) Settings other than the above are prohibited.

Register	Bit	RX140 (LVDAb)	RX660 (LVDA)
LVDLVLR	LVD2LVL [1:0] (RX140) LVD2LVL [3:0] (RX660)	Voltage detection 2 level select bits (Standard voltage during drop in voltage) b5 b4 0 0: 4.32 V 0 1: 4.17 V 1 0: 4.03 V 1 1: 3.84 V	Voltage detection 2 level select bits (Standard voltage during drop in voltage) b7 b4 0 1 0 0: 4.57 V (Vdet2_0) 0 1 0 1: 4.47 V (Vdet2_1) 0 1 1 0: 4.32 V (Vdet2_2) 1 0 1 0: 2.93 V (Vdet2_3) 1 0 1 1: 2.88 V (Vdet2_4) Settings other than the above are prohibited.
LVD1CR0	LVD1DFDIS	—	Voltage monitoring 1 digital filter disable mode select bit
	LVD1FSAMP [1:0]	—	Sampling clock select bits
LVD2CR0	LVD2DFDIS	—	Voltage monitoring 2 digital filter disable mode select bit
	LVD2FSAMP [1:0]	—	Sampling clock select bits
	LVD2RN	Voltage monitoring 2 reset negate select bit 0: Negate when specified time (tLVD2) elapsed after detection of VCC or CMPA2 > Vdet2 1: Negate when specified time (tLVD2) elapsed after assertion of voltage monitoring 2 reset	Voltage monitoring 2 reset negate select bit 0: Negate when specified time (tLVD2) elapsed after detection of VCC > Vdet2 1: Negate when specified time (tLVD2) elapsed after assertion of LVD2 reset

Note: 1. The EXVCCINP2 can be changed only when LVD1E and LVD2E bits are "0" (voltage detection 1 circuit and voltage detection 2 circuit disabled).

2.7 Clock Generation Circuit

Table 2.9 is Comparative Overview of Clock Generation Circuits, and Table 2.10 is Comparison of Clock Generation Circuit Registers.

Table 2.9 Comparative Overview of Clock Generation Circuits

Item	RX140	RX660
Use	• Generates the system clock (ICLK) to be supplied to CPU, DTC, ROM, and RAM.	• Generates the system clock (ICLK) to be supplied to the CPU, TFU, DMAC, DTC, code flash memory and RAM. • Generates the peripheral module clock (PCLKA) supplied to RSPI, SCIm, RSCI, MTU, and CANFD.
	• Generates the peripheral module clocks (PCLKB, PCLKD) supplied to the peripheral modules The peripheral module clock PCLKD is the operating clock for S12AD, and peripheral module clock PCLKB is the operating clock for peripheral modules other than S12AD.	• Generates the peripheral module clock (PCLKB) supplied to the peripheral modules. • Generates the peripheral module clock (for analog conversion) (PCLKD) to be supplied to the S12AD.
	• Generates the FlashIF clock (FCLK) to be supplied to the FlashIF.	• Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the external-bus clock (BCLK) to be supplied to the external bus.
	• Generates the CAC clock (CACCLK) to be supplied to the CAC.	• Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CANFD clock (CANFDCLK) to be supplied to the CANFD.
	• Generates the CAN clock (CANMCLK) to be supplied to the CAN.	• Generates the CANFD main clock (CANFDMCLK) to be supplied to the CANFD.
	• Generates the RTC-dedicated sub-clock (RTCSCLK) to be supplied to the RTC.	• Generates the RTC sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the REMC sub-clock (REMSCLK) to be supplied to the REMC.
	• Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the LPT clock (LPTCLK) to be supplied to the LPT.	• Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.

Item	RX140	RX660
Operating frequency	• ICLK: 48 MHz (max.) • PCLKB: 32 MHz (max.) • PCLKD: 48 MHz (max.) • FCLK: — 1 MHz to 48 MHz (for programing and erasing ROM or E2 DataFlash) — 48 MHz (max.) (when reading from the E2 DataFlash) • CACCLK: Same as the clock from respective oscillators • CANMCLK: 20 MHz (max.) • RTCSCLK: 32.768 kHz • IWDTCLK: 15 kHz • LPTCLK: Same as the clock from selected oscillator	• ICLK: 120 MHz (max.) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKD: 8 MHz to 60 MHz (for conversion with the 12-bit A/D converter) • FCLK: — 4 MHz to 60 MHz (for programming and erasing the cold flash memory or data flash memory) — 60 MHz (max.) (for reading from the data flash memory) • BCLK: 60 MHz (max.) • BCLK pin output: 40 MHz (max.) • CACCLK: Same as the clock from respective oscillators • CANFDCLK: 60 MHz (max.) • CANFDMCLK: 24 MHz (max.) • RTCSCLK: 32.768 kHz • REMCLK: 32.768 kHz • IWDTCLK: 120 kHz
Main clock oscillator	• Oscillation frequency: 1 MHz to 20 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal • Connection pins: EXTAL and XTAL • Oscillation stop detection function: • When a main clock oscillation stop is detected, the system clock source is switched to LOCO, and the MTU pin is driven to high-impedance state. • Drive capacity switching function	• Oscillation frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal • Connection pins: EXTAL and XTAL • Oscillation stop detection function: • When a main clock oscillation stop is detected, the system clock source is switched to LOCO, and the MTU pin is driven to high-impedance state. • Drive capacity switching function
Sub-clock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: Crystal resonator • Connection pins: XCIN and XCOUT • Drive capacity switching function	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: Crystal resonator • Connection pins: XCIN and XCOUT • Drive capacity switching function

Item	RX140	RX660
PLL circuit (RX140) PLL frequency synthesizer (RX660)	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 12 MHz • Frequency multiplication ratio: Selectable from 4 to 12 (increments of 0.5) • Oscillation frequency: 24 MHz to 48 MHz	• Input clock source: Main clock, HOCO • Input pulse frequency division ratio: Selectable from 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable from 10 to 30 (increments of 0.5) • Output clock frequency of frequency synthesizer: 120 MHz to 240 MHz
High-speed on-chip oscillator (HOCO)	• Oscillation frequency: 24 MHz, 32 MHz, and 48 MHz	• Oscillation frequency: Selectable from 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control • FLL function (Cannot be used for products that do not have sub-clock oscillator)
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 4 MHz	Oscillation frequency: 240 kHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 15 kHz	Oscillation frequency: 120 kHz
BCLK pin output control function	—	• Selectable from BCLK clock output and high output • Output clock can be selected from BCLK or 1/2 frequency of BCLK
Event link function (output)	—	Detection of stopping of the main clock oscillator
Event link function (input)	—	Switching of the clock source to the low-speed on-chip oscillator

Table 2.10 Comparison of Clock Generation Circuit Registers

Register	Bit	RX140	RX660
SCKCR	PCKC[3:0]	—	This MCU does not have PCLKC. Set it to 0001b.
	PCKA[3:0]	—	Peripheral module clock A (PCLKA) select bits
	BCK[3:0]	—	External bus clock (BCLK) select bits
	PSTOP1	—	BCLK pin output control bit
SCKCR2	—	—	System clock control register 2
PLLCR	PLIDIV[1:0]	PLL input frequency division ratio select bits b1 b0 0 0: 1 0 1: 2 1 0: 4 1 1: Setting prohibited	PLL input frequency division ratio select bits b1 b0 0 0: 1 0 1: 2 1 0: 3 1 1: Setting prohibited
	PLLSRCSEL	—	PLL clock source select bit
	STC[5:0]	Frequency multiplication factor select bits b13 b8 0 0 0 1 1 1: ×4 0 0 1 0 0 0: ×4.5 0 0 1 0 0 1: ×5 0 0 1 0 1 0: ×5.5 0 0 1 0 1 1: ×6 0 0 1 1 0 0: ×6.5 0 0 1 1 0 1: ×7 0 0 1 1 1 0: ×7.5 0 0 1 1 1 1: ×8 0 1 0 0 0 0: ×8.5 0 1 0 0 0 1: ×9 0 1 0 0 1 0: ×9.5 0 1 0 0 1 1: ×10 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12	Frequency multiplication factor select bits b13 b8 0 1 0 0 1 1: ×10.0 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11.0 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12.0 0 1 1 0 0 0: ×12.5 0 1 1 0 0 1: ×13.0 0 1 1 0 1 0: ×13.5 0 1 1 0 1 1: ×14.0 0 1 1 1 0 0: ×14.5 0 1 1 1 0 1: ×15.0 0 1 1 1 1 0: ×15.5 0 1 1 1 1 1: ×16.0 1 0 0 0 0 0: ×16.5 1 0 0 0 0 1: ×17.0 1 0 0 0 1 0: ×17.5 1 0 0 0 1 1: ×18.0 1 0 0 1 0 0: ×18.5

Register	Bit	RX140	RX660
PLLCR	STC[5:0]	Settings other than the above are prohibited.	1 0 0 1 0 1: ×19.0 1 0 0 1 1 0: ×19.5 1 0 0 1 1 1: ×20.0 1 0 1 0 0 0: ×20.5 1 0 1 0 0 1: ×21.0 1 0 1 0 1 0: ×21.5 1 0 1 0 1 1: ×22.0 1 0 1 1 0 0: ×22.5 1 0 1 1 0 1: ×23.0 1 0 1 1 1 0: ×23.5 1 0 1 1 1 1: ×24.0 1 1 0 0 0 0: ×24.5 1 1 0 0 0 1: ×25.0 1 1 0 0 1 0: ×25.5 1 1 0 0 1 1: ×26.0 1 1 0 1 0 0: ×26.5 1 1 0 1 0 1: ×27.0 1 1 0 1 1 0: ×27.5 1 1 0 1 1 1: ×28.0 1 1 1 0 0 0: ×28.5 1 1 1 0 0 1: ×29.0 1 1 1 0 1 0: ×29.5 1 1 1 0 1 1: ×30.0 Settings other than the above are prohibited.
BCKCR	—	—	External bus clock control register
HOCOCR2	—	—	High-speed on-chip oscillator control register 2
FLLCR1	—	—	FLL control register 1
FLLCR2	—	—	FLL control register 2
OSCOVFSR	SOOVF	—	Sub-clock oscillation stabilization flag
	ILCOVF	—	IWDT-dedicated clock oscillation stabilization flag

Register	Bit	RX140	RX660
MOSCWTCR	MSTS[4:0] (RX140) MSTS[7:0] (RX660)	Main clock oscillator wait time setting bits b4 b0 0 0 0 0 0: Wait time = 0 cycles (0.5 µs) 0 0 0 0 1: Wait time = 1,024 cycles (256 µs) 0 0 0 1 0: Wait time = 2,048 cycles (512 µs) 0 0 0 1 1: Wait time = 4,096 cycles (1.024 ms) 0 0 1 0 0: Wait time = 8,192 cycles (2.048 ms) 0 0 1 0 1: Wait time = 16,384 cycles (4.096 ms) 0 0 1 1 0: Wait time = 32,768 cycles (8.192 ms) 0 0 1 1 1: Wait time = 65,536 cycles (16.384 ms) 0 1 0 0 0: Wait time = 131,072 cycles (32.768ms) Settings other than the above are prohibited. Wait time when LOCO = 4.0 MHz (0.25 µs, TYP)	Main clock oscillator wait time setting bits The setting value of the MSTS[7:0] bits are obtained by the following formula using the maximum frequency of fLOCO so that the waiting time always becomes equal to or larger than the oscillation stabilization time of the main clock. MSTS[7:0] > [tMAINOSC × (fLOCO_max) + 16] / 32 (tMAINOSC: main clock oscillation stabilization time; fLOCO_max: maximum fLOCO frequency)
LOFCR	—	Low-speed on-chip oscillator forced oscillation control register	—
CKOCR	—	CLKOUT output control register	—
SOSCWTCR	—	—	Sub-clock oscillator wait control register
SOFCR	—	—	Sub-clock oscillator forced oscillation control register
MOFCR	MODRV21 (RX140) MODRV2 [1:0] (RX660)	Main clock oscillator driving ability switching bit 0: 1 MHz to 10 MHz 1: 10 MHz to 20 MHz	Main clock oscillator driving ability 2 switching bits b5 b4 0 0: 20.1 to 24 MHz 0 1: 16.1 to 20 MHz 1 0: 8.1 to 16 MHz 1 1: 8 MHz
LOCOTRR2	—	Low-speed on-chip oscillator trimming register 2	—
ILOCOTRR	—	IWDT-dedicated on-chip oscillator trimming register	—
HOCOTRRn	—	High-speed on-chip oscillator trimming register n (n = 0)	—
HOCOPCR	—	—	High-speed on-chip oscillator power supply control register
SOMCR	—	Sub-clock oscillator mode control register	—

2.8 Low Power Consumption Function

Table 2.11 is Comparative Overview of Low Power Consumption Functions, Table 2.12 is Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode, and Table 2.13 is Comparison of Low Power Consumption Registers.

Table 2.11 Comparative Overview of Low Power Consumption Functions

Item	RX140	RX660
Reducing power consumption by switching clock signals	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKB), S12AD clock (PCLKD), and FlashIF clock (FCLK).	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, and PCLKD), external-bus clock (BCLK), and FlashIF clock (FCLK).
BCLK output control function	—	Selectable from BCLK output and high output
Module stop function	Each peripheral module can be stopped independently.	Each peripheral module can be stopped independently.
Function for transition to low power consumption mode	Can be transitioned to a low power consumption mode, in which the CPU, peripheral module, and oscillators are stopped.	Can be transitioned to a low power consumption mode, in which the CPU, peripheral module, and oscillators are stopped.
Low power consumption modes	• Sleep mode • Deep sleep mode • Software standby mode • Snooze mode	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode
Function for lower operating power consumption	• Power consumption can be reduced in normal operation, sleep mode, deep sleep mode, and snooze mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Four operating power control modes are available: — High-speed operating mode — Middle-speed operating mode — Middle-speed operating mode 2 — Low-speed operating mode	—

Table 2.12 Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX140	RX660
Sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM	Operation possible (retained)	Operation possible (retained)
	DTC	Operation possible	—
	Flash memory	Operation	Operation
	Watchdog timer (WDT)	—	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	Port output enable (POE)	—	Operation possible
	Low-power timer (LPT)	Operation possible	—
	Remote controller signal receiver (REMC)	—	Operation possible
	8-bit timer (unit 0, unit1)	—	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Operation possible	Operation possible
	I/O ports	Operation	Operation
	RTCOUT output	Operation possible	—
	CLKOUT output	Operation possible	—
	Comparator B	Operation possible	—
Deep sleep mode	Transition method	Control register + instruction	—
	Method of cancellation other than reset	Interrupt	—
	State after cancellation	Program execution state (interrupt processing)	—
	Main clock oscillator	Operation possible	—
	Sub-clock oscillator	Operation possible	—
	High-speed on-chip oscillator	Operation possible	—
	Low-speed on-chip oscillator	Operation possible	—
	IWDT-dedicated on-chip oscillator	Operation possible	—
	PLL	Operation possible	—
	CPU	Stopped (retained)	—
	RAM	Stopped (retained)	—
	DTC	Stopped (retained)	—

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX140	RX660
Deep sleep mode	Flash memory	Stopped (retained)	—
	Independent watchdog timer (IWDT)	Operation possible	—
	Realtime clock (RTC)	Operation possible	—
	Low-power timer (LPT)	Operation possible	—
	Voltage detection circuit (LVD)	Operation possible	—
	Power-on reset circuit	Operation	—
	Peripheral modules	Operation possible	—
	I/O ports	Operation	—
	RTCOUT output	Operation possible	—
	CLKOUT output	Operation possible	—
	Comparator B	Operation possible	—
All-module clock stop mode	Transition method	—	Control register + instruction
	Method of cancellation other than reset	—	Interrupt
	State after cancellation	—	Program execution state (interrupt processing)
	Main clock oscillator	—	Operation possible
	Sub-clock oscillator	—	Operation possible
	High-speed on-chip oscillator	—	Operation possible
	Low-speed on-chip oscillator	—	Operation possible
	IWDT-dedicated on-chip oscillator	—	Operation possible
	PLL	—	Operation possible
	CPU	—	Stopped (retained)
	RAM	—	Stopped (retained)
	Flash memory	—	Stopped (retained)
	Watchdog timer (WDT)	—	Stopped (retained)
	Independent watchdog timer (IWDT)	—	Operation possible
	Realtime clock (RTC)	—	Operation possible
	Port output enable (POE)	—	Operation possible
	Remote controller signal receiver (REMC)	—	Operation possible
	8-bit timer (unit 0, unit1)	—	Operation possible
	Voltage detection circuit (LVD)	—	Operation possible
	Power-on reset circuit	—	Operation
	Peripheral modules	—	Stopped (retained)
	I/O ports	—	Operation
Software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Stopped	Stopped
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Operation possible	Stopped
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Stopped	Stopped
	CPU	Stopped (retained)	Stopped (retained)

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX140	RX660
Software standby mode	RAM	Stopped (retained)	Stopped (retained)
	DTC	Stopped (retained)	—
	Flash memory	Stopped (retained)	Stopped (retained)
	Watchdog timer (WDT)	—	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	Port output enable (POE)	—	Stopped (retained)
	Low-power timer (LPT)	Operation possible	—
	Remote controller signal receiver (REMC)	—	Operation possible
	8-bit timer (unit 0, unit1)	—	Stopped (retained)
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained
	RTCOUT output	Operation possible	—
	CLKOUT output	Operation possible	—
	Comparator B	Operation possible	—
Deep software standby mode	Transition method	—	Control register + instruction
	Method of cancellation other than reset	—	Interrupt
	State after cancellation	—	Program execution state (interrupt processing)
	Main clock oscillator	—	Stopped
	Sub-clock oscillator	—	Operation possible
	High-speed on-chip oscillator	—	Stopped
	Low-speed on-chip oscillator	—	Stopped
	IWDT-dedicated on-chip oscillator	—	Stopped (undefined)
	PLL	—	Stopped
	CPU	—	Stopped (undefined)
	RAM	—	Stopped (undefined)
	Flash memory	—	Stopped (retained)
	Watchdog timer (WDT)	—	Stopped (undefined)
	Independent watchdog timer (IWDT)	—	Stopped (undefined)
	Realtime clock (RTC)	—	Operation possible
	Port output enable (POE)	—	Stopped (undefined)
	Remote controller signal receiver (REMC)	—	Stopped (undefined)
	8-bit timer (unit 0, unit1)	—	Stopped (undefined)
	Voltage detection circuit (LVD)	—	Operation possible
	Power-on reset circuit	—	Operation
	Peripheral modules	—	Stopped (undefined)
	I/O ports	—	Retained

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX140	RX660
Snooze mode	Transition method	Condition for snooze transition occurring in software standby mode	—
	Method of cancellation other than reset	Occurrence of an interrupt or a snooze completion condition	—
	State after cancellation	A program being executed (interrupt processing) or software standby mode taking place	—
	Main clock oscillator	Operation possible	—
	Sub-clock oscillator	Operation possible	—
	High-speed on-chip oscillator	Operation possible	—
	Low-speed on-chip oscillator	Operation possible	—
	IWDT-dedicated on-chip oscillator	Operation possible	—
	PLL	Operation possible	—
	CPU	Stopped (retained)	—
	RAM	Operation possible (retained)	—
	DTC	Operation possible	—
	Flash memory	Stopped (retained)	—
	Independent watchdog timer (IWDT)	Operation possible	—
	Realtime clock (RTC)	Operation possible	—
	Low-power timer (LPT)	Operation possible	—
	Voltage detection circuit (LVD)	Operation possible	—
	Power-on reset circuit	Operation	—
	Peripheral modules	Operation possible	—
	I/O ports	Operation	—
	RTCOUT output	Operation possible	—
	CLKOUT output	Operation possible	—
	Comparator B	Operation possible	—

“Operation possible” means that whether the state is operating or stopped is controlled by the control register setting.
“Stopped (retained)” means that internal register values are retained and internal operations are suspended.
“Stopped (undefined)” means that the internal register values are undefined and the internal operation state is power-off.

Table 2.13 Comparison of Low Power Consumption Registers

Register	Bit	RX140	RX660
SBYCR	OPE	—	Output port enable bit
	SSBY	Software standby bit 0: Transitions to sleep mode or deep sleep mode after executing the WAIT instruction 1: Transitions to software standby mode after executing the WAIT instruction	Software standby bit 0: Transitions to sleep mode or all-module clock stop mode after executing the WAIT instruction 1: Transitions to software standby mode after executing the WAIT instruction
MSTPCRA	MSTPA0	—	Compare match timer W (Unit 1) module stop bit
	MSTPA1	—	Compare match timer W (Unit 0) module stop bit
	MSTPA9	Multi-function timer pulse unit module stop bit Target modules: MTU0 to MTU5 0: Release from module-stop state 1: Transition to module-stop state	Multi-function timer pulse unit 3 module stop bit Target module: MTU3 0: Release from module-stop state 1: Transition to module-stop state
	MSTPA14	—	Compare match timer (Unit 1) module stop bit
	MSTPA24	—	Module stop A24 setting bit
	MSTPA27	—	Module stop A27 setting bit
	MSTPA28	Data transfer controller module stop bit Target module: DTC 0: Release from module-stop state 1: Transition to module-stop state	DMA controller/data transfer controller module stop bit Target module: DMAC/DTC 0: Release from module-stop state 1: Transition to module-stop state
	MSTPA29	—	Module stop A29 setting bit
	ACSE	—	All-module clock stop mode enable bit
MSTPCRB	MSTPB0	CAN module stop bit	—
	MSTPB8	ELC module stop bit	—
	MSTPB10	Comparator B module stop bit	Comparator C module stop bit
	MSTPB24	—	Serial communications interface 7 module stop bit
	MSTPB27	—	Serial communications interface 4 module stop bit
	MSTPB28	—	Serial communications interface 3 module stop bit
	MSTPB29	—	Serial communications interface 2 module stop bit
	MSTPB31	—	Serial communications interface 0 module stop bit
MSTPCRC	MSTPC0	RAM module stop bit Target module: RAM (0000 0000h to 0000 FFFFh)	RAM module stop bit Target module: RAM (0000 0000h to 0001 FFFFh)
	MSTPC17	—	I^2C bus interface 2 module stop bit
	MSTPC24	—	Serial communications interface 11 module stop bit

Register	Bit	RX140	RX660
MSTPCRC	MSTPC25	—	Serial communications interface 10 module stop bit
	DSLPE	Deep sleep mode enable bit	—
MSTPCRD	MSTPD2	—	Serial communications interface 11 module stop bit
	MSTPD3	—	Serial communications interface 10 module stop bit
	MSTPD7	—	Remote controller signal receiver module stop bit
	MSTPD10	Touch sensor control unit module stop bit	CANFD module stop bit
	MSTPD29	Genuine random number generation module stop bit	—
	MSTPD30	AES hardware accelerator module stop bit	—
OPCCR	—	Operating power control register	—
SOPCCR	—	Sub-operating power control register	—
RSTCKCR	RSTCKSEL [2:0]	Sleep mode return clock source select bits b2 b0 0 0 0: LOCO is selected. 0 0 1: HOCO is selected*1. 0 1 0: Main clock oscillator is selected. Settings other than the above are prohibited when the RSTCKEN bit is 1.	Sleep mode return clock source select bits b2 b0 0 0 1: HOCO is selected. 0 1 0: Main clock oscillator is selected. Settings other than the above are prohibited when the RSTCKEN bit is 1.
SNZCR	—	Snooze control register	—
SNZCR2	—	Snooze control register 2	—
DPSBYCR	—	—	Deep standby control register
DPSIER0	—	—	Deep standby interrupt enable register 0
DPSIER1	—	—	Deep standby interrupt enable register 1
DPSIER2	—	—	Deep standby interrupt enable register 2
DPSIFR0	—	—	Deep standby interrupt flag register 0
DPSIFR1	—	—	Deep standby interrupt flag register 1
DPSIFR2	—	—	Deep standby interrupt flag register 2
DPSIEGR0	—	—	Deep standby interrupt edge register 0
DPSIEGR1	—	—	Deep standby interrupt edge register 1
DPSIEGR2	—	—	Deep standby interrupt edge register 2
DPSBKRy	—	—	Deep standby backup register y (y = 0 to 31)

Note: 1. Rewrite this register after setting the PRCR.PRC1 bit to 1 (write enabled).

2.9 Register Write Protection Function

Table 2.14 is Comparative Overview of Register Write Protection Functions, and Table 2.15 is Comparison of Register Write Protection Function Registers.

Table 2.14 Comparative Overview of Register Write Protection Functions

Item	RX140	RX660
PRC0 bit	• Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, LOFCR, OSTDCR, OSTDSR, CKOCR, LOCOTRR2, ILOCOTRR, HOCOTRR0, SOMCR	• Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, FLLCR1, FLLCR2, OSTDCR, OSTDSR
PRC1 bit	• Registers related to the operating modes: SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, SOPCCR, SNZCR, SNZCR2 • Registers related to the clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR	• Registers related to the operating modes: SYSCR0, SYSCR1, VOLSR • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, RSTCKCR, DPSBYCR, DPSIER0 to DPSIER2, DPSIFR0 to DPSIFR2, DPSIEGR0 to DPSIEGR2 • Registers related to the clock generation circuit: MOSCWTCR, SOSCWTCR, MOFCR, SOFCR, HOCOPCR • Software reset register: SWRR
PRC2 bit	• Registers related to low-power timer: LPTCR1, LPTCR2, LPTCR3, LPTPRD, LPCMR0, LPCMR1, LPWUCR	—
PRC3 bit	• Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	• Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

Table 2.15 Comparison of Register Write Protection Function Registers

Register	Bit	RX140	RX660
PRCR	PRC2	Protect bit 2	—

2.10 Interrupt Controller

Table 2.16 is Comparative Overview of Interrupt Controllers, and Table 2.17 is Comparison of Interrupt Controller Registers.

Table 2.16 Comparative Overview of Interrupt Controllers

Item		RX140 (ICUb)	RX660 (ICUF)
Interrupt	Peripheral interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection — The detection method is fixed for each source of connected peripheral modules.	• Interrupts from peripheral modules • Interrupt detection method: Edge detection or level detection (The interrupt detection method is fixed for each interrupt source.) • Group interrupt: Multiple interrupt sources are grouped together and treated as a single interrupt source*1. — Group IE0 interrupt: Interrupt sources of coprocessors that use ICLK as the operating clock (edge detection) — Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) — Group BL0/BL1/BL2 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) — Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt B: Any of the interrupt sources for peripheral modules that use PCLKB as the operating clock can be assigned to interrupt vector numbers 128 to 207. • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.

Item		RX140 (ICUb)	RX660 (ICUF)
Interrupt	External pin interrupts	• Interrupts from pins IRQ0 to IRQ7 • Number of sources: 8 • Interrupt detection: Detection of low level, falling edge, rising edge, or rising and falling edges can be set for each detection source. • Digital filter function: Supported	• Interrupts by input signals on IRQi pins (i = 0 to 15) • Interrupt detection: Detection of low level, falling edge, rising edge, or rising and falling edges can be set for each detection source. • A digital filter can be used to remove noise.
	Software interrupts	• Interrupt generated by writing to a register • Number of sources: 1	• An interrupt request can be generated by writing to a register. • Number of sources: 2
	Event link interrupt	ELSR8I and ELSR18I interrupts are generated by an ELC event.	—
	Interrupt priority level	Specified by registers.	The priority level is set with the interrupt source priority register r (IPRr) (r = 000 to 255).
	Fast interrupt function	Faster interrupt handling by the CPU can be specified for a single interrupt source only.	It is possible to reduce the CPU's interrupt response time. This setting can be used for one interrupt source only.
	DTC and DMAC control	The DTC can be activated by an interrupt source.	The DTC and DMAC can be activated by an interrupt source.
Non-maskable interrupts	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection: — Falling edge — Rising edge • Digital filter function: Supported	• Interrupt by the input signal on the NMI pin • Interrupt detection: — Falling edge — Rising edge • A digital filter can be used to remove noise.
	Oscillation stop interrupt	Interrupt on detection of oscillation having stopped	Interrupt occurs when the main clock oscillator stop is detected.
	WDT underflow/ refresh error interrupt	—	Interrupt occurs when the watchdog timer underflows or a refresh error occurs.
	IWDT underflow/ refresh error interrupt	Interrupt on an underflow of the down counter or occurrence of a refresh error	Interrupt occurs when the independent watchdog timer underflows or a refresh error occurs.
	Voltage monitoring 1 interrupt	Voltage monitoring interrupt of voltage detection circuit 1 (LVD1)	Interrupt from voltage detection circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Voltage monitoring interrupt of voltage detection circuit 2 (LVD2)	Interrupt from voltage detection circuit 2 (LVD2)
	RAM error interrupt	—	Interrupt occurs when a parity check error is detected in RAM.

Item		RX140 (ICUb)	RX660 (ICUF)
Return from low power consumption state	Sleep mode	Exit this mode by any non-maskable interrupt or any interrupt source.	Exit this mode by any interrupt source.
	Deep sleep mode	Exit this mode by any non-maskable interrupt or any interrupt source.	—
	All-module clock stop mode	—	Exit this mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection, RTC alarm, RTC cycle, IWDT, REMC interrupt, or software configurable interrupts 146 to 157).
	Software standby mode	Exit this mode by non-maskable interrupt other than oscillation stop detection interrupt, external pin interrupt (IRQ0 to IRQ7), peripheral interrupt (voltage monitoring 1, voltage monitoring 2, RTC alarm/cycle), or ELSR8I interrupt (LPT-dedicated interrupt).	Exit this mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, RTC alarm, RTC cycle, IWDT, or REMC interrupt).
	Deep software standby mode	—	Exit this mode by NMI pin interrupt, specific external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, RTC alarm, or TRC cycle).
	Snooze mode	Exit this mode by non-maskable interrupt other than oscillation stop detection interrupt, external pin interrupt (IRQ0 to IRQ7), peripheral interrupt (voltage monitoring 1, voltage monitoring 2, RTC alarm/cycle), or SNZI interrupt (snooze exit interrupt).	—

Note: 1. Groups without an assigned interrupt are reserved. There are no registers for such a group.

Table 2.17 Comparison of Interrupt Controller Registers

Register	Bit	RX140 (ICUb)	RX660 (ICUF)
SWINTR2R	—	—	Software interrupt 2 generation register
DTCERn	DTCE	DTC transfer request enable bit (n = 027 to 255) 0: Set to an interrupt source to the CPU. 1: Set to the DTC activation source.	DTC transfer request enable bit (n = 026 to 255) 0: Set to an interrupt source to the CPU, or DMAC activation source. 1: Set to the DTC activation source.
DMRSRm	—	—	DMAC activation source select register m
IRQCRi	—	IRQ control register i (i = 0 to 7)	IRQ control register i (i = 0 to 15)
IRQFLTE1	—	—	IRQ pin digital filter enable register 1
IRQFLTC1	—	—	IRQ pin digital filter setting register 1
NMISR	WDTST	—	WDT underflow/refresh error status flag
	RAMST	—	RAM error interrupt status flag
NMIER	WDTEN	—	WDT underflow/refresh error enable bit
	RAMEN	—	RAM error interrupt enable bit
NMICLR	WDTCLR	—	WDT clear bit
GRPBL0 GRPBL1 GRPBL2	—	—	Group BL0/BL1/BL2 interrupt request register
GRPAL0	—	—	Group AL0 interrupt request register
GENBL0 GENBL1 GENBL2	—	—	Group BL0/BL1/BL2 interrupt request enable register
GENAL0	—	—	Group AL0 interrupt request enable register
PIBRk	—	—	Software configurable interrupt B request register k (k = 0h, 1h, 5h, 6h, 8h to Ah, Ch, Dh)
PIARk	—	—	Software configurable interrupt A request register k (k = 0h to 5h, Bh, Ch)
SLIBXRn	—	—	Software configurable interrupt B source select register Xn (n = 128 to 143)
SLIBRn	—	—	Software configurable interrupt B source select register n (n = 144 to 207)
SLIARn	—	—	Software configurable interrupt A source select register n (n = 208 to 255)
SLIPRCR	—	—	Software configurable interrupt source select register write protect register

2.11 Buses

Table 2.18 is Comparative Overview of Buses, and Table 2.19 is Comparison of Bus Registers.

Table 2.18 Comparative Overview of Buses

Item		RX140	RX660
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	• Connected to RAM	• Connected to RAM
	Memory bus 2	• Connected to ROM	• Connected to code flash memory
Internal main buses	Internal main bus 1	• Connected to CPU • Operates in synchronization with the system clock (ICLK)	• Connected to CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the DTC and DMAC • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (TFU, DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules • Operates in synchronization with the peripheral module clock (PCLKB)	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral module clock (PCLKB)
	Internal peripheral bus 3	• Connected to peripheral modules (CTSU, RSCAN) • Operates in synchronization with the peripheral module clock (PCLKB)	• Connected to peripheral modules (DOC, REMC, CANFD, and CMPC) • Operates in synchronization with the peripheral module clock (PCLKB)
	Internal peripheral bus 4	—	• Connected to peripheral modules (MTU, RSPI, and SCIi) • Operates in synchronization with the peripheral module clock (PCLKA)

Item		RX140	RX660
Internal peripheral buses	Internal peripheral bus 5	—	• Connected to peripheral modules (RSCI and CANFD) • Operates in synchronization with the peripheral module clock (PCLKA)
	Internal peripheral bus 6	• Connected to ROM (in P/E) and E2 DataFlash • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to code flash memory (in P/E) and data flash memory • Operates in synchronization with the FlashIF clock (FCLK)
External bus	CS area	—	• Connected to external devices • Operates in synchronization with the external-bus clock (BCLK)

Table 2.19 Comparison of Bus Registers

Register	Bit	RX140	RX660
CSnCR	—	—	CSn control register (n = 0 to 3)
CSnREC	—	—	CSn recovery cycle setting register (n = 0 to 3)
CSRECEN	—	—	CSn recovery cycle insertion enable register
CSnMOD	—	—	CSn mode register (n = 0 to 3)
CSnWCR1	—	—	CSn wait control register 1 (n = 0 to 3)
CSnWCR2	—	—	CSn wait control register 2 (n = 0 to 3)
BERSR1	MST[2:0]	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved
BUSPRI	BPHB[1:0]	—	Internal peripheral bus 4 and 5 priority control bits
	BPEB[1:0]	—	External bus priority control bits

2.12 Event Link Controller

Table 2.20 is Comparative Overview of Event Link Controllers, Table 2.21 is Comparison of Event Link Controller Registers, Table 2.22 is Correspondence between the ELSRn Registers and Peripheral Modules, and Table 2.23 is Correspondence between Event Signal Names and Signal Numbers set in ELSRn.ELS[7:0].

Table 2.20 Comparative Overview of Event Link Controllers

Item	RX140 (ELC)	RX660 (ELC)
Event link ALEOE function	• Event signals of 48 types can be directly linked to peripheral modules. • An operation to be executed at event signal input can be selected for timer peripheral modules. • Event link operation is possible for port B. — Single port: An event link operation can be set for a specified single port. — Port group: An event link operation can be specified for a group of ports selected from a maximum of 8 ports.	• Event signals of 83 types can be directly linked to peripheral modules. • An operation to be executed at event signal input can be selected for timer peripheral modules. • Event link operation is possible for port B and port E. — Single port: An event link operation can be set for a specified single port. — Port group: An event link operation can be specified for a group of ports selected from a maximum of 8 ports.
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Table 2.21 Comparison of Event Link Controller Registers

Register	Bit	RX140 (ELC)	RX660 (ELC)
ELSRn	—	Event link setting register n (n = 1 to 4, 7, 8, 10, 12, 14 to 16, 18 to 20, 22, 24, 25)	Event link setting register n (n = 0, 3, 4, 7, 10 to 13, 15, 16, 18 to 28, 30, 31, 32, 56)
	ELS[7:0]	Event link select bits 00h: Event output to the target peripheral module is disabled. 08h to 6Ah: Specify the number for the event signal to be linked. Settings other than the above are prohibited.	Event link select bits 00h: Event signal output to the target peripheral module is disabled. 01h to F1h: Specify the number for the event signal to be linked. Settings other than the above are prohibited.
ELOPA	MTU0MD [1:0]	—	MTU0 operation select bits
	MTU1MD [1:0]	MTU1 operation select bits	—
	MTU2MD [1:0]	MTU2 operation select bits	—
ELOPC	LPTMD[1:0]	LPT operation select bits	—

Register	Bit	RX140 (ELC)	RX660 (ELC)
ELOPD	TMR1MD [1:0]	—	TMR1 operation select bits
	TMR3MD [1:0]	—	TMR3 operation select bits
ELOPE	—	—	Event link option setting register E
PGR1 (RX140) PGRn (RX660)	—	Port group setting register 1	Port group setting register n (n = 1, 2)
PGC1 (RX140) PGCn (RX660)	—	Port group control register 1	Port group control register n (n = 1, 2)
PDBF1 (RX140) PDBFn (RX660)	—	Port buffer register 1	Port buffer register n (n = 1, 2)
PELm	—	Event link port setting register m (m = 0, 1)	Event link port setting register m (m = 0 to 3)
	PSP[1:0]	Port number specification bits b4 b3 0 0: Setting disabled 0 1: Port B (for register PGR1) 1 0: Setting prohibited 1 1: Setting prohibited	Port number specification bits b4 b3 0 0: Setting disabled 0 1: Port B (for register PGR1) 1 0: Port E (for register PGR2) 1 1: Setting prohibited

Table 2.22 Correspondence between the ELSRn Registers and Peripheral Modules

Register	RX140 (ELC)	RX660 (ELC)
ELSR0	—	MTU0
ELSR1	MTU1	—
ELSR2	MTU2	—
ELSR3	MTU3	MTU3
ELSR4	MTU4	MTU4
ELSR7	CMT1	CMT1
ELSR8	ICU (LPT-dedicated interrupt)	—
ELSR10	TMR0	TMR0
ELSR11	—	TMR1
ELSR12	TMR2	TMR2
ELSR13	—	TMR3
ELSR14	CTSU	—
ELSR15	S12AD	S12AD (ELCTRG00N)
ELSR16	DA0	DA0
ELSR18	ICU (interrupt 1)	ICU (interrupt 1)
ELSR19	—	ICU (interrupt 2)
ELSR20	Output port group 1	Output port group 1
ELSR21	—	Output port group 2
ELSR22	Input port group 1	Input port group 1
ELSR23	—	Input port group 2
ELSR24	Single port 0	Single port 0
ELSR25	Single port 1	Single port 1

Register	RX140 (ELC)	RX660 (ELC)
ELSR26	—	Single port 2
ELSR27	—	Single port 3
ELSR28	—	Clock source is switched to LOCO.
ELSR30	—	MTU6
ELSR31	—	MTU7
ELSR32	—	MTU8
ELSR56	—	S12AD (ELCTRG01N)

Table 2.23 Correspondence between Event Signal Names and Signal Numbers set in ELSRn.ELS[7:0]

ELS[7:0] Bit Value	RX140 (ELC)	RX660 (ELC)
01h	—	MTU0 compare match 0A
02h	—	MTU0 compare match 0B
03h	—	MTU0 compare match 0C
04h	—	MTU0 compare match 0D
05h	—	MTU0 compare match 0E
06h	—	MTU0 compare match 0F
07h	—	MTU0 overflow
08h	MTU1 compare match 1A	—
09h	MTU1 compare match 1B	—
0Ah	MTU1 overflow	—
0Bh	MTU1 underflow	—
0Ch	MTU2 compare match 2A	—
0Dh	MTU2 compare match 2B	—
0Eh	MTU2 overflow	—
0Fh	MTU2 underflow	—
10h	MTU3 compare match 3A	MTU3 compare match 3A
11h	MTU3 compare match 3B	MTU3 compare match 3B
12h	MTU3 compare match 3C	MTU3 compare match 3C
13h	MTU3 compare match 3D	MTU3 compare match 3D
14h	MTU3 overflow	MTU3 overflow
15h	MTU4 compare match 4A	MTU4 compare match 4A
16h	MTU4 compare match 4B	MTU4 compare match 4B
17h	MTU4 compare match 4C	MTU4 compare match 4C
18h	MTU4 compare match 4D	MTU4 compare match 4D
19h	MTU4 overflow	MTU4 overflow
1Ah	MTU4 underflow	MTU4 underflow
1Eh	—	MTU6 compare match 6A
1Fh	CMT1 compare match 1	MTU6 compare match 6B
20h	—	MTU6 compare match 6C
21h	—	MTU6 compare match 6D
22h	TMR0 compare match A0	MTU6 overflow
23h	TMR0 compare match B0	MTU7 compare match 7A
24h	TMR0 overflow	MTU7 compare match 7B
25h	—	MTU7 compare match 7C
26h	—	MTU7 compare match 7D
27h	—	MTU7 overflow
28h	TMR2 compare match A2	MTU7 underflow
29h	TMR2 compare match B2	MTU8 compare match 8A
2Ah	TMR2 overflow	MTU8 compare match 8B
2Bh	—	MTU8 compare match 8C

ELS[7:0] Bit Value	RX140 (ELC)	RX660 (ELC)
2Ch	—	MTU8 compare match 8D
2Dh	—	MTU8 overflow
32h	LPT compare match 0	—
33h	LPT compare match 1	—
34h	S12AD compare condition match	—
35h	S12AD compare condition mismatch	—
37h	—	CMT1 compare match 1
3Ah	SCI5 error (reception error or error signal detected)	—
3Bh	SCI5 receive data full	—
3Ch	SCI5 transmit data empty	TMR0 compare match A0
3Dh	SCI5 transmit end	TMR0 compare match B0
3Eh	—	TMR0 overflow
3Fh	—	TMR1 compare match A1
40h	—	TMR1 compare match B1
41h	—	TMR1 overflow
42h	—	TMR2 compare match A2
43h	—	TMR2 compare match B2
44h	—	TMR2 overflow
45h	—	TMR3 compare match A3
46h	—	TMR3 compare match B3
47h	—	TMR3 overflow
4Eh	RIIC0 communication error, event occurrence	—
4Fh	RIIC0 receive data full	—
50h	RIIC0 transmit data empty	—
51h	RIIC0 transmit end	—
58h	S12AD A/D conversion enf	—
59h	Comparison result change of comparator B0	—
5Ah	Comparison result change of comparator B0/B1	—
5Bh	LVD1 voltage detection	—
61h	DTC transfer completion	—
63h	Input edge detection on input port group 1	—
65h	Input edge detection on single input port 0	—
66h	Input edge detection on single input port 1	—
69h	Software event	—
6Ah	DOC data calculation condition match	—
ACh	—	RTC periodic event (select 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, 1, or 2 seconds)
AFh	—	IWDT underflow or refresh error
B8h	—	SCI5 error (reception error or error signal detected)
B9h	—	SCI5 receive data full

ELS[7:0] Bit Value	RX140 (ELC)	RX660 (ELC)
BAh	—	SCI5 transmit data empty
BBh	—	SCI5 transmit end
CCh	—	RIIC0 communication error, event occurrence
CDh	—	RIIC0 receive data full
CEh	—	RIIC0 transmit data empty
CFh	—	RIIC0 transmit end
D0h	—	RSPI0 error (mode fault, overrun, underrun, or parity error)
D1h	—	RSPI0 idle
D2h	—	RSPI0 receive buffer full
D3h	—	RSPI0 transmit buffer empty
D4h	—	RSPI0 transmit end
D6h	—	S12AD A/D conversion end
DCh	—	Comparison result change on comparator C0
DDh	—	Comparison result change on comparator C1
DEh	—	Comparison result change on comparator C2
DFh	—	Comparison result change on comparator C3
E2h	—	LVD1 voltage detection
E3h	—	LVD2 voltage detection
E4h	—	DMAC0 transfer completion
E5h	—	DMAC1 transfer completion
E6h	—	DMAC2 transfer completion
E7h	—	DMAC3 transfer completion
E8h	—	DTC transfer completion
E9h	—	Oscillation stop detection of clock generation circuit
EAh	—	Input edge detection on input port group 1
EBh	—	Input edge detection on input port group 2
ECh	—	Input edge detection on single input port 0
EDh	—	Input edge detection on single input port 1
EEh	—	Input edge detection on single input port 2
EFh	—	Input edge detection on single input port 3
F0h	—	Software event
F1h	—	DOC data calculation condition match

2.13 I/O Port

Table 2.24 to Table 2.26 are a comparative overview of I/O ports, Table 2.27 is Comparison of I/O Port Functions, and Table 2.29 is Comparison of I/O Port Registers.

Table 2.24 Comparative Overview of I/O Ports (80-Pin)

Port Symbol	RX140 (80-Pin)	RX660 (80-Pin)
PORT0	P03 to P07	P03*1 to P07
PORT1	P12 to P17	P12 to P17
PORT2	P20, P21, P26, P27	P20, P21, P26, P27
PORT3	P30 to P32, P34 to P37	P30 to P32, P34 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P54, P55	P54, P55
PORTA	PA0 to PA6	PA0 to PA6
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC2 to PC7
PORTD	PD0 to PD2	PD0 to PD2
PORTE	PE0 to PE5	PE0 to PE5
PORTG	PG7	Not available
PORTH	PH0 to PH3, PH6, PH7	PH0 to PH3*2, PH6, PH7*2
PORTJ	PJ1, PJ6, PJ7	PJ1, PJ6, PJ7
PORTN	Not available	PN6

Notes: 1. A product that has JTAG does not have P03.
2. A product that has a sub-clock oscillator does not have PH6 or PH7.

Table 2.25 Comparative Overview of I/O Ports (64-Pin)

Port Symbol	RX140 (64-Pin)	RX660 (64-Pin)
PORT0	P03, P05	P03, P07
PORT1	P14 to P17	P14 to P17
PORT2	P26, P27	P26, P27
PORT3	P30 to P32, P35 to P37	P30 to P32, P35 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P54, P55	P54, P55
PORTA	PA0, PA1, PA3, PA4, PA6	PA0, PA1, PA3, PA4, PA6
PORTB	PB0, PB1, PB3, PB5 to PB7	PB0, PB1, PB3, PB5 to PB7
PORTC	PC0 to PC7	PC2 to PC7
PORTE	PE0 to PE5	PE0 to PE5
PORTG	PG7	Not available
PORTH	PH0 to PH3*2, PH6, PH7*2	PH0 to PH3*1, PH6, PH7*1
PORTJ	Not available	PJ6, PJ7
PORTN	Not available	PN6

Notes: 1. A product that has a sub-clock oscillator does not have PH6 or PH7.
2. Not available for a product whose ROM capacity is 64 KB.

Table 2.26 Comparative Overview of I/O Ports (48-Pin)

Port Symbol	RX140 (48-Pin)	RX660 (48-Pin)
PORT1	P14 to P17	P14 to P17
PORT2	P26 ,P27	P26, P27
PORT3	P30, P31, P35 to P37	P30, P31, P35 to P37
PORT4	P40 to P42, P45 to P47	P40 to P42, P45 to P47
PORTA	PA1, PA3, PA4, PA6	PA1, PA3, PA4, PA6
PORTB	PB0, PB1, PB3, PB5	PB0, PB1, PB3, PB5
PORTC	PC0 to PC7*1	PC4 to PC7
PORTE	PE1 to PE4	PE1 to PE4
PORTG	PG7	Not available
PORTH	PH0 to PH3	PH0 to PH3
PORTJ	PJ6, PJ7	PJ6, PJ7
PORTN	Not available	PN6

Note: 1. PC0 to PC3 are effective only when switching is made by port switch register B.

Table 2.27 Comparison of I/O Port Functions

Item	Port Symbol	RX140	RX660
Input pull-up function	PORT0	P03 to P07	P00 to P07
	PORT1	P12 to P17	P12 to P17
	PORT2	P20, P21, P26, P27	P20 to P27
	PORT3	P30 to P32, P34, P36, P37	P30 to P34, P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P54, P55	P50 to P56
	PORT6	—	P60 to P67
	PORT7	—	P70 to P77
	PORT8	—	P80 to P83, P86, P87
	PORT9	—	P90 to P93
	PORTA	PA0 to PA6	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC2 to PC7	PC0 to PC7
	PORTD	PD0 to PD2	PD0 to PD7
	PORTE	PE0 to PE5	PE0 to PE7
	PORTF	—	PF5 to PF7
	PORTG	PG7	—
	PORTH	PH0 to PH3	PH0 to PH3, PH6, PH7
	PORTJ	PJ1, PJ6, PJ7	PJ1, PJ3 to PJ7
	PORTK	—	PK2 to PK5
	PORTL	—	PL0, PL1
	PORTN	—	PN6, PN7
Open drain output function	PORT0	—	P00 to P07
	PORT1	P12 to P17	P12 to P17
	PORT2	P20, P21, P26, P27	P20 to P27
	PORT3	P30 to P32, P34, P36, P37	P30 to P34, P36, P37
	PORT4	—	P40 to P47
	PORT5	—	P50 to P56
	PORT6	—	P60 to P67
	PORT7	—	P70 to P77
	PORT8	—	P80 to P83, P86, P87
	PORT9	—	P90 to P93
	PORTA	PA0 to PA6	PA0 to PA7

Item	Port Symbol	RX140	RX660
Open drain output function	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC2 to PC7	PC0 to PC7
	PORTD	PD0 to PD2	PD0 to PD7
	PORTE	PE0 to PE3	PE0 to PE7
	PORTF	—	PF5 to PF7
	PORTG	PG7	—
	PORTH	—	PH0 to PH3, PH6, PH7
	PORTJ	—	PJ1, PJ3 to PJ7
	PORTK	—	PK2 to PK5
	PORTL	—	PL0, PL1
	PORTN	—	PN6, PN7
5 V tolerant	PORT1	P12, P13, P16, P17	P12, P13, P16, P17

Table 2.28 Comparison of Driving Ability Switching on I/O Ports

Port Symbol	Driving Ability Switching	RX140	RX660
PORT0	Normally fixed	—	P03, P05 to P07
	Normal/high	—	P00 to P02, P04
PORT1	Normally fixed	—	—
	Normal/high	—	P12 to P17
PORT2	Normally fixed	—	—
	Normal/high	—	P20 to P27
PORT3	Normally fixed	—	P36, P37
	Normal/high	—	P30 to P34
PORT4	Normally fixed	—	P40 to P47
	Normal/high	—	—
PORT5	Normally fixed	—	—
	Normal/high	—	P50 to P56
PORT6	Normally fixed	—	—
	Normal/high	—	P60 to P67
PORT7	Normally fixed	—	—
	Normal/high	—	P70 to P77
PORT8	Normally fixed	—	—
	Normal/high	—	P80 to P83, P86, P87
PORT9	Normally fixed	—	—
	Normal/high	—	P90 to P93
PORTA	Normally fixed	—	—
	Normal/high	—	PA0 to PA7
PORTB	Normally fixed	—	—
	Normal/high	—	PB0 to PB7
PORTC	Normally fixed	—	—
	Normal/high	—	PC0 to PC7
PORTD	Normally fixed	—	—
	Normal/high	—	PD0 to PD7
PORTE	Normally fixed	—	—
	Normal/high	—	PE0 to PE7
PORTF	Normally fixed	—	—
	Normal/high	—	PF5 to PF7
PORTH	Normally fixed	—	—
	Normal/high	—	PH0 to PH3, PH6, PH7

Port Symbol	Driving Ability Switching	RX140	RX660
PORTJ	Normally fixed	—	PJ6, PJ7
	Normal/high	—	PJ1, PJ3 to PJ5
PORTK	Normally fixed	—	—
	Normal/high	—	PK2 to PK5
PORTL	Normally fixed	—	—
	Normal/high	—	PL0, PL1
PORTN	Normally fixed	—	—
	Normal/high	—	PN6, PN7

Table 2.29 Comparison of I/O Port Registers

Register	Bit	RX140	RX660
PDR	B0 to B7	Pm0 to Pm7 I/O select bits (m = 0 to 5, A to E, G, H, J)	Pm0 to Pm7 I/O select bits (m = 0 to 9, A to F, H, J to L, N)
PODR	B0 to B7	Pm0 to Pm7 output data store bits (m = 0 to 5, A to E, G, H, J)	Pm0 to Pm7 output data store bits (m = 0 to 9, A to F, H, J to L, N)
PIDR	B0 to B7	Pm0 to Pm7 bits (m = 0 to 5, A to E, G, H, J)	Pm0 to Pm7 bits (m = 0 to 9, A to F, H, J to L, N)
PMR	B7	Pm7 pin mode control bit (m = 0 to 5, A to E, G, H, J) PG7 0: Used as general I/O port 1: Used for MD function (initial value) Others 0: Used as general I/O port (initial value) 1: Used for peripheral function	Pm7 pin mode control bit (m = 0 to 9, A to F, H, J to L, N) 0: Used as general I/O port 1: Used for peripheral module
ODR0	B2, B3, (RX140) B2 (RX660)	Pm1 output type select bit (m = 1 to 3, A to E, J) • P21, P31, PA1, PB1, PD1 b2 0: CMOS output 1: N-channel open drain b3 This bit is read as 0. The write value should be 0. • PE1 b3 b2 0 0: CMOS output 0 1: N-channel open drain 1 0: P-channel open drain 1 1: Hi-Z	Pm1 output type select bit (m = 0 to 9, A to E, H, J to L) 0: CMOS output 1: N-channel open drain
ODR1	B0, B2, B4, B6	Pm4, Pm5, Pm6, and Pm7 output type select bits (m = 1 to 3, A to C, G)	Pm4, Pm5, Pm6, and Pm7 output type select bits (m = 0 to 8, A to F, H, J, K, N)
PCR	B0 to B7	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 5, A to E, G, H, J)	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A to F, H, J to L, N)
PSRA	—	Port switch register A	—
PSRB	—	Port switch register B	—

Register	Bit	RX140	RX660
PRWCNTR	—	Port read wait control register	—
DSCR	—	—	Drive capacity control register (m = 0 to 3, 5 to 9, A to F, H, J to L, N)

2.14 Multi-Function Pin Controller

Table 2.30 is Comparison of Multiplexed Pin Assignments, and Table 2.31 to Table 2.50 are Comparisons of Multi-Function Pin Controller Registers.

In the following comparison of the assignments of multiplexed pins, **orange text** designates pins that exist on the RX140 Group only, and **blue text** designates pins that exist on the RX660 Groups only. A circle (○) indicates that a function is assigned, a cross (×) that the pin does not exist or that no function is assigned, and grayed out items mean that the function is not implemented.

Table 2.30 Comparison of Multiplexed Pin Assignments

Module/Function	Pin Function	Port Allocation	RX140			RX660		
			80-Pin	64-Pin	48-Pin	80-Pin	64-Pin	48-Pin
Interrupt	NMI (input)	P35	○	○	○	○	○	○
	IRQ0 (input)	P30	○	○	○	×	×	×
		PA0	×	×	×	○	○	×
		PD0	○	×	×	○	×	×
		PH1	○	○	○	○	○	○
	IRQ0-DS (input)	P30				○	○	○
	IRQ1 (input)	P31	○	○	○	×	×	×
		PD1	○	×	×	○	×	×
		PH2	○	○	○	○	○	○
	IRQ1-DS (input)	P31				○	○	○
	IRQ2 (input)	P12	○	×	×	○	×	×
		P32	○	○	×	×	×	×
		P36	○	○	○	×	×	×
		PB2	×	×	×	○	×	×
		PD2	○	×	×	○	×	×
	IRQ2-DS (input)	P32				○	○	×
	IRQ3 (input)	P13	○	×	×	○	×	×
		PB3	×	×	×	○	○	○
	IRQ4 (input)	P14	○	○	○	○	○	○
		P34	○	×	×	○	×	×
		P37	○	○	○	○	○	○
		P54	×	×	×	○	○	×
		PB1	○	○	○	×	×	×
		PB4	×	×	×	○	×	×
	IRQ4-DS (input)	PB1				○	○	○
	IRQ5 (input)	P15	○	○	○	○	○	○
		P36	×	×	×	○	○	○
		PA4	○	○	○	×	×	×
		PA5	×	×	×	○	×	×
		PC5	×	×	×	○	○	○
		PE5	○	○	×	○	○	×
	IRQ5-DS (input)	PA4				○	○	○
	IRQ6 (input)	P16	○	○	○	○	○	○
		PA3	○	○	○	×	×	×
		P26	×	×	×	○	○	○
		PB6	×	×	×	○	○	×
	IRQ6-DS (input)	PA3				○	○	○
	IRQ7 (input)	P17	○	○	○	○	○	○
		PE2	○	○	○	×	×	×
		P27	×	×	×	○	○	○

Module/Function	Pin Function	Port Allocation	RX140			RX660		
			80-Pin	64-Pin	48-Pin	80-Pin	64-Pin	48-Pin
Interrupt	IRQ7-DS (input)	PE2				○	○	○
	IRQ8 (input)	P20				○	×	×
		PE0				○	○	×
	IRQ8-DS (input)	P40				○	○	○
	IRQ9 (input)	P21				○	×	×
		PE1				○	○	○
	IRQ9-DS (input)	P41				○	○	○
	IRQ10 (input)	P55				○	○	×
		PA2				○	×	×
		PC2				○	○	×
	IRQ10-DS (input)	P42				○	○	○
	IRQ11 (input)	P03				○	○	×
		PA1				○	○	○
		PC3				○	○	×
		PE3				○	○	○
	IRQ11-DS (input)	P43				○	○	×
	IRQ12 (input)	PB0				○	○	○
		PC4				○	○	○
		PE4				○	○	○
	IRQ12-DS (input)	P44				○	○	×
	IRQ13 (input)	P05				○	×	×
		PB5				○	○	○
		PC6				○	○	○
	IRQ13-DS (input)	P45				○	○	○
	IRQ14 (input)	PA6				○	○	○
		PC7				○	○	○
	IRQ14-DS (input)	P46				○	○	○
	IRQ15 (input)	P07				○	○	×
		PB7				○	×	×
	IRQ15-DS (input)	P47				○	○	○
Clock generation circuit	CLKOUT (output)	PE3	○	○	○			
		PE4	○	○	○			
Multi-function timer unit 2	MTIOC0A (input/output)	P34	○	×	×	○	×	×
		PB3	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	MTIOC0B (input/output)	P13	○	×	×	○	×	×
		P15	○	○	○	○	○	○
		PA1	○	○	○	○	○	○
	MTIOC0C (input/output)	P32	○	○	×	○	○	×
		PB1	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
	MTIOC0D (input/output)	PA3	○	○	○	○	○	○
	MTIOC1A (input/output)	P20	○	×	×	○	×	×
		PE4	○	○	○	○	○	○
	MTIOC1B (input/output)	P21	○	×	×	○	×	×
		PB5	○	○	○	○	○	○
		PE3	○	○	○	○	○	○
	MTIOC2A (input/output)	P26	○	○	○	○	○	○
		PB5	○	○	○	○	○	○

Module/Function	Pin Function	Port Allocation	RX140			RX660		
			80-Pin	64-Pin	48-Pin	80-Pin	64-Pin	48-Pin
Multi-function timer unit 2	MTIOC2B (input/output)	P27	○	○	○	○	○	○
		PE5	○	○	×	○	○	×
	MTIOC3A (input/output)	P14	○	○	○	○	○	○
		P17	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
		PJ1	○	×	×	○	×	×
	MTIOC3B (input/output)	P17	○	○	○	○	○	○
		PA1	○	○	○	○	○	○
		PB7	○	○	×	○	○	×
		PC5	○	○	○	○	○	○
		PE1	×	×	×	○	○	○
		PH0	○	○	○	○	○	○
	MTIOC3C (input/output)	P16	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	MTIOC3D (input/output)	P16	○	○	○	○	○	○
		PA6	○	○	○	○	○	○
		PB0	○	○	○	○	○	○
		PB6	○	○	×	○	○	×
		PC4	○	○	○	○	○	○
		PE0	×	×	×	○	○	×
		PH1	○	○	○	○	○	○
	MTIOC4A (input/output)	P55	○	○	×	○	○	×
		PA0	○	○	×	○	○	×
		PB3	○	○	○	○	○	○
		PE2	○	○	○	○	○	○
		PE4	○	○	○	○	○	○
		P21	×	×	×	○	×	×
	MTIOC4B (input/output)	P30	○	○	○	○	○	○
		P54	○	○	×	○	○	×
		PC2	○	○	×	○	○	×
		PD1	○	×	×	○	○	○
		PE3	○	○	○	○	○	×
	MTIOC4C (input/output)	PA4	○	○	○	○	○	○
		PB1	○	○	○	○	○	○
		PE1	○	○	○	○	○	○
		PE5	○	○	×	○	○	×
		PH2	○	○	○	○	○	○
	MTIOC4D (input/output)	P31	○	○	○	○	○	○
		P55	○	○	×	○	○	×
		PA3	○	○	○	○	○	○
		PC3	○	○	×	○	○	×
		PD2	○	×	×	○	×	×
		PE4	○	○	○	○	○	○
		PH3	○	○	○	○	○	○
	MTIC5U (input)	PA4	○	○	○	○	○	○
		P12	×	×	×	○	×	×
	MTIC5V (input)	PA3	○	○	○	○	○	○
		PA6	○	○	○	○	○	○
	MTIC5W (input)	PB0	○	○	○	○	○	○

Module/Function	Pin Function	Port Allocation	RX140			RX660		
			80-Pin	64-Pin	48-Pin	80-Pin	64-Pin	48-Pin
Multi-function timer unit 2	MTIOC6B (input/output)	PA5				○	×	×
		PA6				○	○	×
	MTIOC6D (input/output)	PA0				○	○	×
	MTIOC7A (input/output)	PA2				○	×	×
		PE2				○	○	○
	MTIOC7B (input/output)	PA1				○	○	○
	MTIOC7C (input/output)	PA4				○	○	○
	MTIOC7D (input/output)	PE4				○	○	○
	MTCLKA (input)	P14	○	○	○	○	○	○
		PA4	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	MTCLKB (input)	P15	○	○	○	○	○	○
		PA6	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	MTCLKC (input)	PA1	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	MTCLKD (input)	PA3	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
Port output enable 2	POE0# (input)	P32	×	×	×	○	○	×
		PC4	○	○	○	○	○	○
		PD1	×	×	×	○	×	×
	POE1# (input)	PB5	○	○	○			
	POE2# (input)	P34	○	×	×			
		PA6	○	○	○			
	POE3# (input)	PB3	○	○	○			
	POE4# (input)	PB5				○	○	○
		PD0				○	×	×
	POE8# (input)	P17	○	○	○	○	○	○
		P30	○	○	○	○	○	○
		PE3	○	○	○	○	○	○
	POE10# (input)	P32				○	○	×
		P34				○	×	×
		PA6				○	○	○
	POE11# (input)	PB3				○	○	○
8-bit timer	TMO0 (output)	PB3	○	○	○	○	○	○
		PH1	○	○	○	○	○	○
	TMCI0 (input)	P21	○	×	×	○	×	×
		PB1	○	○	○	○	○	○
		PH3	○	○	○	○	○	○
	TMRI0 (input)	P20	○	×	×	○	×	×
		PA4	○	○	○	○	○	○
		PH2	○	○	○	○	○	○
	TMO1 (output)	P17	○	○	○	○	○	○
		P26	○	○	○	○	○	○
	TMCI1 (input)	P12	○	×	×	○	×	×
		P54	○	○	×	○	○	×
		PC4	○	○	○	○	○	○
	TMRI1 (input)	PB5	○	○	○	○	○	○
	TMO2 (output)	P16	○	○	○	○	○	○
		PC7	○	○	○	○	○	○

Module/Function	Pin Function	Port Allocation	RX140			RX660		
			80-Pin	64-Pin	48-Pin	80-Pin	64-Pin	48-Pin
8-bit timer	TMCI2 (input)	P15	○	○	○	○	○	○
		P31	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	TMRI2 (input)	P14	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
	TMO3 (output)	P13	○	×	×	○	×	×
		P32	○	○	×	○	○	×
		P55	○	○	×	○	○	×
	TMCI3 (input)	P27	○	○	○	○	○	×
		P34	○	×	×	○	×	×
		PA6	○	○	○	○	○	×
	TMRI3 (input)	P30	○	○	○	○	○	×
Serial communications interface	RXD0 (input)/ SMISO0 (input/output)/ SSCL0 (input/output)	P21				○	×	×
	TXD0 (output)/ SMOSI0 (input/output)/ SSDA0 (input/output)	P20				○	×	×
		P32				○	×	×
	SCK0 (input/output)	P34				○	×	×
	RXD1 (input)/ SMISO1 (input/output)/ SSCL1 (input/output)	P15	○	○	○	○	○	○
		P30	○	○	○	○	○	○
	TXD1 (output)/ SMOSI1 (input/output)/ SSDA1 (input/output)	P16	○	○	○	○	○	○
		P26	○	○	○	○	○	○
	SCK1 (input/output)	P17	○	○	○	○	○	○
		P27	○	○	○	○	○	○
	CTS1# (input)/ RTS1# (output)/ SS1# (input)	P14	○	○	○	○	○	○
		P31	○	○	○	○	○	○
	RXD3 (input)/ SMISO3 (input/output)/ SSCL3 (input/output)	P16				○	○	○
	TXD3 (output)/ SMOSI3 (input/output)/ SSDA3 (input/output)	P17				○	○	○
	SCK3 (input/output)	P15				○	○	○
	CTS3# (input)/ RTS3# (output)/ SS3# (input)	P26				○	○	○
	RXD4 (input)/ SMISO4 (input/output)/ SSCL4 (input/output)	PB0				○	○	○
	TXD4 (output)/ SMOSI4 (input/output)/ SSDA4 (input/output)	PB1				○	○	○
	SCK4 (input/output)	PB3				○	○	○
	CTS4# (input)/ RTS4# (output)/ SS4# (input)	PB2				○	×	×

Module/Function	Pin Function	Port Allocation	RX140			RX660		
			80-Pin	64-Pin	48-Pin	80-Pin	64-Pin	48-Pin
Serial communications interface	RXD5 (input)/ SMISO5 (input/output)/ SSCL5 (input/output)	PA2	○	×	×	○	×	×
		PA3	○	○	○	○	○	○
		PC2	○	○	×	○	○	×
	TXD5 (output)/ SMOSI5 (input/output)/ SSDA5 (input/output)	PA4	○	○	○	○	○	○
		PC3	○	○	×	○	○	×
	SCK5 (input/output)	PA1	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	CTS5# (input)/ RTS5# (output)/ SS5# (input)	PA6	○	○	○	○	○	○
	RXD6 (input)/ SMISO6 (input/output)/ SSCL6 (input/output)	PB0	○	○	○	○	○	○
		PD1	○	×	×	×	×	×
	TXD6 (output)/ SMOSI6 (input/output)/ SSDA6 (input/output)	P32	○	○	×	○	○	×
		PB1	○	○	○	○	○	○
		PD0	○	×	×	×	×	×
	SCK6 (input/output)	P34	○	×	×	○	×	×
		PB3	○	○	○	○	○	○
		PD2	○	×	×	×	×	×
	CTS6# (input)/ RTS6# (output)/ SS6# (input)	PB2	○	×	×	○	×	×
	RXD8 (input)/ SMISO8 (input/output)/ SSCL8 (input/output)	PC6	○	○	○	○	○	○
	TXD8 (output)/ SMOSI8 (input/output)/ SSDA8 (input/output)	PC7	○	○	○	○	○	○
	SCK8 (input/output)	PC5	○	○	○	○	○	○
	CTS8# (input)/ RTS8# (output)/ SS8# (input)	PC4	○	○	○	○	○	○
	RXD9 (input)/ SMISO9 (input/output)/ SSCL9 (input/output)	PB6	○	○	×	○	○	×
	TXD9 (output)/ SMOSI9 (input/output)/ SSDA9 (input/output)	PB7	○	○	×	○	○	×
	SCK9 (input/output)	PB5	○	○	×	○	○	×
	CTS9# (input)/ RTS9# (output)/ SS9# (input)	PB4	○	○	×	○	×	×
	RXD10 (input)/ SMISO10 (input/output)/ SSCL10 (input/output)	PC6				○	○	○
	TXD10 (output)/ SMOSI10 (input/output)/ SSDA10 (input/output)	PC7				○	○	○
	SCK10 (input/output)	PC5				○	○	○

Module/Function	Pin Function	Port Allocation	RX140			RX660		
			80-Pin	64-Pin	48-Pin	80-Pin	64-Pin	48-Pin
Serial communications interface	CTS10# (input)/ RTS10# (output)/ SS10# (input)	PC4				○	○	○
	RXD11 (input)/ SMISO11 (input/output)/ SSCL11 (input/output)	PB6				○	○	×
	TXD11 (output)/ SMOSI11 (input/output)/ SSDA11 (input/output)	PB7				○	○	×
	SCK11 (input/output)	PB5				○	○	×
	CTS11# (input)/ RTS11# (output)/ SS11# (input)	PB4				○	×	×
	RXD12 (input)/ SMISO12 (input/output)/ SSCL12 (input/output)/ RXDX12 (input)	PE2	○	○	○*4	○	○	○
		PA2	×	×	×	○	×	×
	TXD12 (output)/ SMOSI12 (input/output)/ SSDA12 (input/output)/ SIOX12 (input/output)/ TXDX12 (output)	PE1	○	○	○*4			
	TXD12 (output)/ SMOSI12 (input/output)/ SSDA12 (input/output)/ TXDX12 (output)/ SIOX12 (input/output)	PA4				○	○	○
		PE1				○	○	○
	SCK12 (input/output)	PE0	○	○	×	○	○	×
		PA1	×	×	×	○	○	○
	CTS12# (input)/ RTS12# (output)/ SS12# (input)	PE3	○	○	○*4	○	○	○
		PA6	×	×	×	○	○	○
	RXD010 (input)/ SMISO010 (input/output)/ SSCL010 (input/output)	PC6				○	○	○
	TXD010 (output)/ SMOSI010 (input/output)/ SSDA010 (input/output)	PC7				○	○	○
	SCK010 (input/output)	PC5				○	○	○
	CTS010# (input)/ RTS010# (output)/ SS010# (input)/ DE010 (output)	PC4				○	○	○
	RXD011 (input)/ SMISO011 (input/output)/ SSCL011 (input/output)	PB6				○	○	×
	TXD011 (output)/ SMOSI011 (input/output)/ SSDA011 (input/output)	PB7				○	○	×
	SCK011 (input/output)	PB5				○	○	×
	TXDB011 (output)	PC2				○	○	×

Module/Function	Pin Function	Port Allocation	RX140 80-Pin	RX140 64-Pin	RX140 48-Pin	RX660 80-Pin	RX660 64-Pin	RX660 48-Pin
Serial communications interface	CTS011# (input)/ RTS011# (output)/ SS011# (input)/ DE011 (output)	PB4				○	×	×
I2C bus interface	SCL0 (input/output)	P12	○	×	×	○	×	×
		P16	○	○	○	×	×	×
	SDA0 (input/output)	P13	○	×	×	○	×	×
		P17	○	○	○	×	×	×
	SCL2 (input/output)	P16				○	○	○
	SDA2 (input/output)	P17				○	○	○
Serial peripheral interface	RSPCKA (input/output)	PA5	○	×	×	○	×	×
		PB0	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
	MOSIA (input/output)	P16	○	○	○	○	○	○
		PA6	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	MISOA (input/output)	P17	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	SSLA0 (input/output)	PA4	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	SSLA1 (output)	PA0	○	○	×	○	○	×
	SSLA2 (output)	PA1	○	○	○	○	○	○
	SSLA3 (output)	PA2	○	×	×	○	×	×
		PC2	○	○	×	○	○	×
Realtime clock	RTCOUT output	P16	○	○	○	○	○	×
		P32	○	○	×	○	○	×
	RTCIC0 (input)*3, *1	P30				○	○	×
	RTCIC1 (input)*3, *1	P31				○	○	×
	RTCIC2 (input)*3, *1	P32				○	○	×
Low-power timer	LPTO (output)	P26	○	○	○			
		PB3	○	○	○			
		PC7	○	○	○			
CAN module	CTXD0 (output)	P14	○	○	○			
		P54	○	○	×			
	CRXD0 (input)	P15	○	○	○			
		P55	○	○	×			
CANFD module	CRX0 (input)	P15				○	○	○
		P55				○	○	×
		PD2				○	×	×
	CTX0 (output)	P14				○	○	○
		P32				○	○	×
		P54				○	○	×
		PD1				○	×	×
12-bit A/D converter	AN000 (input)*1	P40	○	○	○	○	○	○
	AN001 (input)*1	P41	○	○	○	○	○	○
	AN002 (input)*1	P42	○	○	○	○	○	○
	AN003 (input)*1	P43	○	○	×	○	○	×
	AN004 (input)*1	P44	○	○	×	○	○	×
	AN005 (input)*1	P45	○	○	○	○	○	○

Module/Function	Pin Function	Port Allocation	RX140			RX660		
			80-Pin	64-Pin	48-Pin	80-Pin	64-Pin	48-Pin
12-bit A/D converter	AN006 (input)*1	P46	○	○	○	○	○	○
	AN007 (input)*1	P47	○	○	○	○	○	○
	AN008 (input)*1	PE0				○	○	×
	AN009 (input)*1	PE1				○	○	○
	AN010 (input)*1	PE2				○	○	○
	AN011 (input)*1	PE3				○	○	○
	AN012 (input)*1	PE4				○	○	○
	AN013 (input)*1	PE5				○	○	×
	AN016 (input)*1	PE0	○	○	×	×	×	×
		PD0	×	×	×	○	×	×
	AN017 (input)*1	PE1	○	○	○	×	×	×
		PD1	×	×	×	○	×	×
	AN018 (input)*1	PE2	○	○	○	×	×	×
		PD2	×	×	×	○	×	×
	AN019 (input)*1	PE3	○	○	○	×	×	×
	AN020 (input)*1	PE4	○	○	○	×	×	×
	AN021 (input)*1	PE5	○	○	×	×	×	×
	AN024 (input)*1	PD0	○	×	×			
	AN025 (input)*1	PD1	○	×	×			
	AN026 (input)*1	PD2	○	×	×			
	ADTRG0# (input)	P07	○	×	×	○	○	○
		P16	○	○	○	○	○	○
		P25	×	×	×	×	○	○
		PA1	×	×	×	○	○	×
		PH0	×	×	×	○	○	×
	ADST0 (output)	PA4				○	○	○
		PH1				○	○	○
D/A comparator	DA0 (output)	P03	○	○	×	○	○	×
	DA1 (output)	P05	○	○	×	○	×	×
Clock frequency accuracy measurement circuit	CACREF (input)	PA0	○	○	×	○	○	×
		PC7	○	○	○	○	○	○
		PH0	○	○	○	○	○	○
LVD voltage detection input	CMPA2 (input)	PE4	○	○	○			
Comparator B	CMPB0 (input)	PE1	○	○	○			
	CVREFB0 (input)	PE2	○	○	○			
	CMPOB0 (output)	PE5	○	○	×			
	CMPB1 (input)	PA3	○	○	○			
	CVREFB1 (input)	PA4	○	○	○			
	CMPOB1 (output)	PB1	○	○	○			
Comparator C	CMPC00 (input)	PE1				○	○	○
	CMPC10 (input)	PA3				○	○	○
	CMPC20 (input)	P15				○	○	○
	CMPC30 (input)	P26				○	○	○
	COMP0 (output)	PE5				○	○	×
	COMP1 (output)	PB1				○	○	○
	COMP2 (output)	P17				○	○	○
	COMP3 (output)	P30				○	○	○
	CVREFC0 (input)	PE2				○	○	○

Module/Function	Pin Function	Port Allocation	RX140			RX660		
			80-Pin	64-Pin	48-Pin	80-Pin	64-Pin	48-Pin
Comparator C	CVREFC1 (input)	PA4				○	○	○
	CVREFC2 (input)	P14				○	○	○
	CVREFC3 (input)	P27				○	○	○
CTSU	TS0 (input/output)	P32	○	○	×			
	TS1 (input/output)	P31	○	○	○			
	TS2 (input/output)	P30	○	○	○			
	TS3 (input/output)	P27	○	○	○			
	TS4 (input/output)	P26	○	○	○			
	TS5 (input/output)	P15	○	○	○			
	TS6 (input/output)	P14	○	○	○			
	TS7 (input/output)	PH3	○	○	○			
	TS8 (input/output)	PH2	○	○	○			
	TS9 (input/output)	PH1	○	○	○			
	TS10 (input/output)	PH0	○	○	○			
	TS11 (input/output)	P55	○	○	×			
	TS12 (input/output)	P54	○	○	×			
	TS13 (input/output)	PC7	○	○	○			
	TS14 (input/output)	PC6	○	○	○			
	TS15 (input/output)	PC5	○	○	○			
	TS16 (input/output)	PC3	○	○	×			
	TS17 (input/output)	PC2	○	○	×			
	TS18 (input/output)	PB7	○	○	×			
	TS19 (input/output)	PB6	○	○	×			
	TS20 (input/output)	PB5	○	○	○			
	TS21 (input/output)	PB4	○	×	×			
	TS22 (input/output)	PB3	○	○	○			
	TS23 (input/output)	PB2	○	×	×			
	TS24 (input/output)	PB1	○	○	○			
	TS25 (input/output)	PB0	○	○	○			
	TS26 (input/output)	PA6	○	○	○			
	TS27 (input/output)	PA5	○	×	×			
	TS28 (input/output)	PA4	○	○	○			
	TS29 (input/output)	PA3	○	○	○			
	TS30 (input/output)	PA2	○	×	×			
	TS31 (input/output)	PA1	○	○	×			
	TS32 (input/output)	PA0	○	○	×			
	TS33 (input/output)	PE4	○	○	○			
	TS34 (input/output)	PE3	○	○	○			
	TS35 (input/output)	PE2	○	○	○			
	TSCAP (-)	PC4	○	○	○			
Remote controller signal receiver	PMC0 (input)	PB3				○	○	○
		PC3				○	○	×
		PC4				○	○	○
		PC5				○	○	○
Compare match timer W	TOC0 (output)	PC7				○	○	○
	TIC0 (input)	PC6				○	○	○
	TOC1 (output)	PH2				○	○	○
	TIC1 (input)	PH1				○	○	○
	TOC2 (output)	PB5				○	○	○

Module/Function	Pin Function	Port Allocation	RX140			RX660		
			80-Pin	64-Pin	48-Pin	80-Pin	64-Pin	48-Pin
Compare match timer W	TIC2 (input)	PB3				○	○	○
		PD2				○	×	×
	TOC3 (output)	PE3				○	○	○
	TIC3 (input)	PE2				○	○	○

Notes: 1. When using this pin function, configure the pin setting to general input. (Set the PORT.PDR.Bm and PORT.PMR.Bm bits to 0.)
2. Not available for products that have JTAG.
3. Not available for products that do not have a sub-clock oscillator.
4. However, the SMISO12 function is not available.

Table 2.31 Comparison of P0n Pin Function Control Registers (P0nPFS)

Register	Bit	RX140 (n = 3,5,7)	RX660 (n = 0 to 3, 5, 7)
P00PFS	PSEL[5:0]	—	P00 pin function select bits
P01PFS	PSEL[5:0]	—	P01 pin function select bits
P02PFS	PSEL[5:0]	—	P02 pin function select bits
P03PFS	PSEL[4:0]	P03 pin function select bits	—
P05PFS	PSEL[4:0]	P05 pin function select bits	—
P0nPFS	ISEL	—	Interrupt input function select bit

Table 2.32 Comparison of P1n Pin Function Control Registers (P1nPFS)

Register	Bit	RX140 (n = 2 to 7)	RX660 (n = 2 to 7)
P12PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00101b: TMCI1 01111b: SCL	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000101b: TMCI1 001010b: RXD2/SMISO2/SSCL2*1 001111b: SCL0
P13PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0B 00101b: TMO3 01111b: SDA	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000101b: TMO3 001010b: TXD2/SMOSI2/SSDA2*1 001111b: SDA0
P14PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKA 00101b: TMRI2 01011b: CTS1#/RTS1#/SS1# 10000b: CTXD0 11001b: TS6	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKA 000101b: TMRI2 001011b: CTS1#/RTS1#/SS1# 010000b: CTX0

Register	Bit	RX140 (n = 2 to 7)	RX660 (n = 2 to 7)
P15PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKB 00101b: TMCI2 01010b: RXD1/SMISO1/SSCL1 10000b: CRXD0 11001b: TS5	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKB 000101b: TMCI2 001010b: RXD1/SMISO1/SSCL1 001011b: SCK3 010000b: CRX0
P16PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTIOC3D 00101b: TMO2 00111b: RTCOUT 01001b: ADTRG0# 01010b: TXD1/SMOSI1/SSDA1 01101b: MOSIA 01111b: SCL	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTIOC3D 000101b: TMO2 000111b: RTCOUT*1 001001b: ADTRG0# 001010b: TXD1/SMOSI1/SSDA1 001011b: RXD3/SMISO3/SSCL3 001101b: MOSIA 001111b: SCL2
P17PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTIOC3B 00101b: TMO1 00111b: POE8# 01010b: SCK1 01101b: MISOA 01111b: SDA	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTIOC3B 000101b: TMO1 000111b: POE8# 001000b: MTIOC4B 001010b: SCK1 001011b: TXD3/SMOSI3/SSDA3 001101b: MISOA 001111b: SDA2 011110b: COMP2
P1nPFS	ASEL	—	Analog function select bit

Note: 1. Not available for products that do not have a sub-clock oscillator.

Table 2.33 Comparison of P2n Pin Function Control Registers (P2nPFS)

Register	Bit	RX140 (n = 0, 1, 6, 7)	RX660 (n = 0 to 7)
P20PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC1A 00101b: TMRI0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC1A 000101b: TMRI0 001010b: TXD0/SMOSI0/SSDA0
P21PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC1B 00101b: TMCI0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC1B 000101b: TMCI0 001000b: MTIOC4A 001010b: RXD0/SMISO0/SSCL0
P22PFS	PSEL[5:0]	—	P22 pin function select bits
P23PFS	PSEL[5:0]	—	P23 pin function select bits
P24PFS	PSEL[5:0]	—	P24 pin function select bits
P25PFS	PSEL[5:0]	—	P25 pin function select bits
P26PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC2A 00101b: TMO1 01010b: TXD1/SMOSI1/SSDA1 11001b: TS4 11011b: LPTO	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2A 000101b: TMO1 001010b: TXD1/SMOSI1/SSDA1 001011b: CTS3#/RTS3#/SS3#
P27PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC2B 00101b: TMCI3 01010b: SCK1 11001b: TS3	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2B 000101b: TMCI3 001010b: SCK1
P2nPFS	ISEL	—	Interrupt input function select bit
P2nPFS	ASEL	—	Analog function select bit

Table 2.34 Comparison of P3n Pin Function Control Registers (P3nPFS)

Register	Bit	RX140 (n = 0 to 2, 4, 6, 7)	RX660 (n = 0 to 4, 6, 7)
P30PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 00101b: TMRI3 00111b: POE8# 01010b: RXD1/SMISO1/SSCL1 11001b: TS2	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000101b: TMRI3 000111b: POE8# 001010b: RXD1/SMISO1/SSCL1 011110b: COMP3
P31PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 00101b: TMCI2 01011b: CTS1#/RTS1#/SS1# 11001b: TS1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000101b: TMCI2 001010b: CTS1#/RTS1#/SS1#
P32PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0C 00101b: TMO3 00111b: RTCOUT 01011b: TXD6/SMOSI6/SSDA6 11001b: TS0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0C 000101b: TMO3 000111b: RTCOUT*1 001000b: POE0# 001010b: TXD6/SMOSI6/SSDA6 001011b: TXD0/SMOSI0/SSDA0 010000b: CTX0 100001b: POE10#
P33PFS	PSEL[5:0]	—	P33 pin function select bits
P34PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0A 00101b: TMCI3 00111b: POE2# 01011b: SCK6	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0A 000101b: TMCI3 000111b: POE10# 001010b: SCK6 001011b: SCK0
P3nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0 (80/64/48/32-pin) P31: IRQ1 (80/64/48/32-pin) P32: IRQ2 (80/64-pin) P34: IRQ4 (80-pin) P36: IRQ2 (80/64/48/32-pin) P37: IRQ4 (80/64/48-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0-DS (144/100/80/64/48- pin) P31: IRQ1-DS (144/100/80/64/48- pin) P32: IRQ2-DS (144/100/80/64-pin) P33: IRQ3-DS (144/100-pin) P34: IRQ4 (144/100/80-pin) P36: IRQ5 (144/100/80/64/48-pin) P37: IRQ4 (144/100/80/64/48-pin)

Note: 1. Not available for products that do not have a sub-clock oscillator.

Table 2.35 Comparison of P4n Pin Function Control Registers (P4nPFS)

Register	Bit	RX140 (n = 0 to 7)	RX660 (n = 0 to 7)
P4nPFS	ISEL	—	Interrupt input function select bit

Table 2.36 Comparison of P5n Pin Function Control Registers (P5nPFS)

Register	Bit	RX140 (n = 4, 5)	RX660 (n = 0 to 6)
P50PFS	PSEL[5:0]	—	P50 pin function select bits
P51PFS	PSEL[5:0]	—	P51 pin function select bits
P52PFS	PSEL[5:0]	—	P52 pin function select bits
P53PFS	PSEL[5:0]	—	P53 pin function select bits
P54PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 00101b: TMCI1 10000b: CTXD0 11001b: TS12	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000101b: TMCI1 001011b: CTS2#/RTS2#/SS2# 010000b: CTX0
P55PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 00010b: MTIOC4A 00101b: TMO3 10000b: CRXD0 11001b: TS11	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000010b: MTIOC4A 000101b: TMO3 001010b: TXD7/SMOSI7/SSDA7 010000b: CRX0
P56PFS	PSEL[5:0]	—	P56 pin function select bits
P5nPFS	ISEL	—	Interrupt input function select bit

Table 2.37 Comparison of P6n Pin Function Control Registers (P6nPFS)

Register	Bit	RX140	RX660 (n = 0 to 7)
P6nPFS	—	—	P6n pin function control register

Table 2.38 Comparison of P7n Pin Function Control Registers (P7nPFS)

Register	Bit	RX140	RX660 (n = 0 to 7)
P7nPFS	—	—	P7n pin function control register

Table 2.39 Comparison of P8n Pin Function Control Registers (P8nPFS)

Register	Bit	RX140	RX660 (n = 0 to 3, 6, 7)
P8nPFS	—	—	P8n pin function control register

Table 2.40 Comparison of P9n Pin Function Control Registers (P9nPFS)

Register	Bit	RX140	RX660 (n = 0 to 3)
P9nPFS	—	—	P9n pin function control register

Table 2.41 Comparison of PAn Pin Function Control Registers (PAnPFS)

Register	Bit	RX140 (n = 0 to 6)	RX660 (n = 0 to 7)
PA0PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4A 00111b: CACREF 01101b: SSLA1 11001b: TS32	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000111b: CACREF 001000b: MTIOC6D 001101b: SSLA1
PA1PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKC 00011b: MTIOC3B 01010b: SCK5 01101b: SSLA2 11001b: TS31	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKC 001000b: MTIOC7B 001001b: ADTRG0# 001010b: SCK5 001100b: SCK12 001101b: SSLA2 100111b: MTIOC3B
PA2PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 01010b: RXD5/SMISO5/SSCL5 01101b: SSLA3 11001b: TS30	Pin function select bits 000000b: Hi-Z 001000b: MTIOC7A 001010b: RXD5/SMISO5/SSCL5 001100b: RXD12/SMISO12/ SSCL12/RXDX12 001101b: SSLA3
PA3PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0D 00010b: MTCLKD 00011b: MTIOC4D 00100b: MTIC5V 01010b: RXD5/SMISO5/SSCL5 11001b: TS29	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0D 000010b: MTCLKD 001000b: MTIC5V 001010b: RXD5/SMISO5/SSCL5 100111b: MTIOC4D

Register	Bit	RX140 (n = 0 to 6)	RX660 (n = 0 to 7)
PA4PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIC5U 00010b: MTCLKA 00011b: MTIOC4C 00101b: TMRI0 01010b: TXD5/SMOSI5/SSDA5 01101b: SSLA0 11001b: TS28	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000010b: MTCLKA 000101b: TMRI0 001000b: MTIOC4C 001001b: ADST0 001010b: TXD5/SMOSI5/SSDA5 001100b: TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12 001101b: SSLA0 100111b: MTIOC7C
PA5PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 01101b: RSPCKA 11001b: TS27	Pin function select bits 000000b: Hi-Z 001000b: MTIOC6B 001101b: RSPCKA
PA6PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIC5V 00010b: MTCLKB 00011b: MTIOC3D 00101b: TMCI3 00111b: POE2# 01011b: CTS5#/RTS5#/SS5# 01101b: MOSIA 11001b: TS26	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000010b: MTCLKB 000101b: TMCI3 000111b: POE10# 001000b: MTIOC3D 001011b: CTS5#/RTS5#/SS5# 001100b: CTS12#/RTS12#/SS12# 001101b: MOSIA 100111b: MTIOC6B
PA7PFS	PSEL[5:0]	—	PA7 pin function select bits
PAnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA3: IRQ6 (80/64/48/32-pin) PA4: IRQ5 (80/64/48/32-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA0: IRQ0 (144/100/80/64-pin) PA1: IRQ11 (144/100/80/64/48-pin) PA2: IRQ10 (144/100/80-pin) PA3: IRQ6-DS (144/100/80/64/48-pin) PA4: IRQ5-DS (144/100/80/64/48-pin) PA5: IRQ5 (144/100/80-pin) PA6: IRQ14 (144/100/80/64/48-pin) PA7: IRQ7 (144/100-pin)

Register	Bit	RX140 (n = 0 to 6)	RX660 (n = 0 to 7)
PAnPFS	ASEL	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin PA3: CMPB1 (80/64/48/32-pin) PA4: CVREFB1 (80/64/48/32-pin)	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin PA3: CMPC10 (144/100/80/64/48-pin) PA4: CVREFC1 (144/100/80/64/48-pin)

Table 2.42 Comparison of PBn Pin Function Control Registers (PBnPFS)

Register	Bit	RX140 (n = 0 to 7)	RX660 (n = 0 to 7)
PB0PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIC5W 00010b: MTIOC3D 01011b: RXD6/SMISO6/SSCL6 01101b: RSPCKA 11001b: TS25	Pin function select bits 000000b: Hi-Z 000001b: MTIC5W 000010b: MTIOC3D 001010b: RXD4/SMISO4/SSCL4 001011b: RXD6/SMISO6/SSCL6 001101b: RSPCKA
PB1PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0C 00010b: MTIOC4C 00101b: TMCI0 01011b: TXD6/SMOSI6/SSDA6 10000b: CMPOB1 11001b: TS24	Pin function select bits 000000b: Hi-Z 000001b: MTIC0C 000010b: MTIOC4C 000101b: TMCI0 001010b: TXD4/SMOSI4/SSDA4 001011b: TXD6/SMOSI6/SSDA6 011110b: COMP1
PB2PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 01011b: CTS6#/RTS6#/SS6# 11001b: TS23	Pin function select bits 000000b: Hi-Z 001010b: CTS4#/RTS4#/SS4# 001011b: CTS6#/RTS6#/SS6#
PB3PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0A 00010b: MTIOC4A 00101b: TMO0 00111b: POE3# 01011b: SCK6 11001b: TS22 11011b: LPTO	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0A 000010b: MTIOC4A 000101b: TMO0 000111b: POE11# 001010b: SCK4 001011b: SCK6 011101b: TIC2 100110b: PMC0

Register	Bit	RX140 (n = 0 to 7)	RX660 (n = 0 to 7)
PB4PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 01011b: CTS9#/RTS9#/SS9# 11001b: TS21	Pin function select bits 000000b: Hi-Z 001011b: CTS9#/RTS9#/SS9# 100100b: CTS11#/RTS11#/SS11# 101100b: CTS011#/RTS011#/ SS011# 101110b: DE011
PB5PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC2A 00010b: MTIOC1B 00101b: TMRI1 00111b: POE1# 01010b: SCK9 11001b: TS20	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2A 000010b: MTIOC1B 000101b: TMRI1 000111b: POE4# 001010b: SCK9 011101b: TOC2 100100b: SCK11 101100b: SCK011
PB6PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3D 01010b: RXD9/SMISO9/SSCL9 11001b: TS19	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 001010b: RXD9/SMISO9/SSCL9 100100b: RXD11/SMISO11/SSCL11 101100b: RXD011/SMISO011/ SSCL011
PB7PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3B 01010b: TXD9/SMOSI9/SSDA9 11001b: TS18	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 001010b: TXD9/SMOSI9/SSDA9 100100b: TXD11/SMOSI11/SSDA11 101100b: TXD011/SMOSI011/ SSDA011
PBnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB1: IRQ4 (80/64/48-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB0: IRQ12 (144/100/80/64/48-pin) PB1: IRQ4-DS (144/100/80/64/48-pin) PB2: IRQ2 (144/100/80-pin) PB3: IRQ3 (144/100/80/64/48-pin) PB4: IRQ4 (144/100/80-pin) PB5: IRQ13 (144/100/80/64/48-pin) PB6: IRQ6 (144/100/80/64-pin) PB7: IRQ15 (144/100/80/64-pin)

Table 2.43 Comparison of PCn Pin Function Control Registers (PCnPFS)

Register	Bit	RX140 (n = 2 to 7)	RX660 (n = 0 to 7)
PC0PFS	PSEL[5:0]	—	PC0 pin function select bits
PC1PFS	PSEL[5:0]	—	PC1 pin function select bits
PC2PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 01010b: RXD5/SMISO5/SSCL5 01101b: SSLA3 11001b: TS17	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 001010b: RXD5/SMISO5/SSCL5 001101b: SSLA3 101100b: TXDB011
PC3PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 01010b: TXD5/SMOSI5/SSDA5 11001b: TS16	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 001010b: TXD5/SMOSI5/SSDA5 100110b: PMC0
PC4PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3D 00010b: MTCLKC 00011b: MTIOC0A 00101b: TMCI1 00111b: POE0# 01010b: SCK5 01011b: CTS8#/RTS8#/SS8# 01101b: SSLA0 11001b: TSCAP	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKC 000101b: TMCI1 000111b: POE0# 001000b: MTIOC0A 001010b: SCK5 001011b: CTS8#/RTS8#/SS8# 001101b: SSLA0 100100b: CTS10#/RTS10#/SS10# 100110b: PMC0 101100b: CTS010#/RTS010#/ SS010# 101110b: DE010
PC5PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3B 00010b: MTCLKD 00011b: MTIOC0C 00101b: TMRI2 01010b: SCK8 01101b: RSPCKA 11001b: TS15	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKD 000101b: TMRI2 001000b: MTIOC0C 001010b: SCK8 001101b: RSPCKA 100100b: SCK10 100110b: PMC0 101100b: SCK010

Register	Bit	RX140 (n = 2 to 7)	RX660 (n = 0 to 7)
PC6PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTCLKA 00101b: TMCI2 01010b: RXD8/SMISO8/SSCL8 01101b: MOSIA 11001b: TS14	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTCLKA 000101b: TMCI2 001010b: RXD8/SMISO8/SSCL8 001101b: MOSIA 011101b: TIC0 100100b: RXD10/SMISO10/SSCL10 101100b: RXD010/SMISO010/ SSCL010
PC7PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKB 00101b: TMO2 00111b: CACREF 01010b: TXD8/SMOSI8/SSDA8 01101b: MISOA 11001b: TS13 11011b: LPTO	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKB 000101b: TMO2 000111b: CACREF 001010b: TXD8/SMOSI8/SSDA8 001101b: MISOA 011101b: TOC0 100100b: TXD10/SMOSI10/SSDA10 101100b: TXD010/SMOSI010/ SSDA010
PCnPFS	ISEL	—	Interrupt input function select bit

Table 2.44 Comparison of PDn Pin Function Control Registers (PDnPFS)

Register	Bit	RX140 (n = 0 to 2)	RX660 (n = 0 to 7)
PD0PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 01011b: TXD6/SMOSI6/SSDA6	Pin function select bits 000000b: Hi-Z 001000b: POE4#
PD1PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 01011b: RXD6/SMISO6/SSCL6	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 001000b: POE0# 010000b: CTX0
PD2PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 01011b: SCK6	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 010000b: CRX0 011101b: TIC2
PD3PFS	PSEL[5:0]	—	PD3 pin function select bits

Register	Bit	RX140 (n = 0 to 2)	RX660 (n = 0 to 7)
PD4PFS	PSEL[5:0]	—	PD4 pin function select bits
PD5PFS	PSEL[5:0]	—	PD5 pin function select bits
PD6PFS	PSEL[5:0]	—	PD6 pin function select bits
PD7PFS	PSEL[5:0]	—	PD7 pin function select bits
PDnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PD0: IRQ0 (80-pin) PD1: IRQ1 (80-pin) PD2: IRQ2 (80-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PD0: IRQ0 (144/100/80-pin) PD1: IRQ1 (144/100/80-pin) PD2: IRQ2 (144/100/80-pin) PD3: IRQ3 (144/100-pin) PD4: IRQ4 (144/100-pin) PD5: IRQ5 (144/100-pin) PD6: IRQ6 (144/100-pin) PD7: IRQ7 (144/100-pin)
	ASEL	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin PD0: AN024 (100-pin) PD1: AN025 (100-pin) PD2: AN026 (100-pin)	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin PD0: AN016 (144/100/80-pin) PD1: AN017 (144/100/80-pin) PD2: AN018 (144/100/80-pin) PD3: AN019 (144/100-pin) PD4: AN020 (144/100-pin) PD5: AN021 (144/100-pin) PD6: AN022 (144/100-pin) PD7: AN023 (144/100-pin)

Table 2.45 Comparison of PEn Pin Function Control Registers (PEnPFS)

Register	Bit	RX140 (n = 0 to 5)	RX660 (n = 0 to 7)
PE0PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 01100b: SCK12	Pin function select bits 000000b: Hi-Z 001000b: MTIOC3D 001100b: SCK12
PE1PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4C 01100b: TXD12/TXDX12/SIOX12 SMOSI12/SSDA12	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 001000b: MTIOC3B 001100b: TXD12/TXDX12/SIOX12 SMOSI12/SSDA12
PE2PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4A 01100b: RXD12/RXDX12/ SMISO12/SSCL12 11001b: TS35	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 001000b: MTIOC7A 001100b: RXD12/RXDX12/ SMISO12/SSCL12 011101b: TIC3

Register	Bit	RX140 (n = 0 to 5)	RX660 (n = 0 to 7)
PE3PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 00010b: MTIOC1B 00111b: POE8# 01001b: CLKOUT 01100b: CTS12#/RTS12#/SS12# 11001b: TS34	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000111b: POE8# 001000b: MTIOC1B 001100b: CTS12#/RTS12#/SS12# 011101b: TOC3
PE4PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 00010b: MTIOC1A 00011b: MTIOC4A 01001b: CLKOUT 11001b: TS33	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000010b: MTIOC1A 001000b: MTIOC4A 100111b: MTIOC7D
PE5PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4C 00010b: MTIOC2B 10000b: CMPOB0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000010b: MTIOC2B 011110b: COMP0
PE6PFS	PSEL[5:0]	—	PE6 pin function select bits
PE7PFS	PSEL[5:0]	—	PE7 pin function select bits
PEnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE2: IRQ7 (80/64/48/32-pin) PE5: IRQ5 (80/64-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE0: IRQ8 (144/100/80/64-pin) PE1: IRQ9 (144/100/80/64/48-pin) PE2: IRQ7-DS (144/100/80/64/48-pin) PE3: IRQ11 (144/100/80/64/48-pin) PE4: IRQ12 (144/100/80/64/48-pin) PE5: IRQ5 (100/80/64-pin) PE6: IRQ6 (144/100-pin) PE7: IRQ7 (144/100-pin)

Register	Bit	RX140 (n = 0 to 5)	RX660 (n = 0 to 7)
PEnPFS	ASEL	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin PE0: AN016 (80/64-pin) PE1: AN017, CMPB0 (80/64/48/32-pin) PE2: AN018, CVREFB0 (80/64/48/32-pin) PE3: AN019, CMPA1 (80/64/48/32-pin) PE4: AN020, CMPA2 (80/64/48/32-pin) PE5: AN021 (80/64-pin)	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin PE0: AN008 (144/100/80/64-pin) PE1: AN009 (144/100/80/64/48-pin) PE2: AN010 (144/100/80/64/48-pin) PE3: AN011 (144/100/80/64/48-pin) PE4: AN012 (144/100/80/64/48-pin) PE5: AN013 (144/100/80/64-pin) PE6: AN014 (144/100-pin) PE7: AN015 (144/100-pin)

Table 2.46 Comparison of PF5 Pin Function Control Registers (PF5PFS)

Register	Bit	RX140	RX660
PF5PFS	—	—	PF5 pin function control register

Table 2.47 Comparison of PHn Pin Function Control Registers (PHnPFS)

Register	Bit	RX140 (n = 0 to 3)	RX660 (n = 0 to 3)
PH0PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3B 00111b: CACREF 11001b: TS10	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000111b: CACREF 001001b: ADTRG0#
PH1PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3D 00101b: TMO0 11001b: TS9	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000101b: TMO0 001001b: ADST0 011101b: TIC1
PH2PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000101b: TMRI0 011001b: TS8	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000101b: TMRI0 011001b: TOC1
PH3PFS	PSEL[4:0] (RX140) PSEL[5:0] (RX660)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 00101b: TMCI0 11001b: TS7	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000101b: TMCI0

Table 2.48 Comparison of PJn Pin Function Control Register (PJnPFS)

Register	Bit	RX140 (n = 1, 6, 7)	RX660 (n = 1, 3, 5)
PJ3PFS	PSEL[5:0]	—	PJ3 pin function select bits
PJ5PFS	PSEL[5:0]	—	PJ5 pin function select bits
PJnPFS	ISEL	—	Interrupt input function select bit
	ASEL	Analog function select bit	—

Table 2.49 Comparison of PKn Pin Function Control Registers (PKnPFS)

Register	Bit	RX140	RX660 (n = 2 to 5)
PKnPFS	—	—	PKn pin function control register

Table 2.50 Comparisons of Multi-Function Pin Controller Registers

Register	Bit	RX140	RX660
PFCSE	—	—	CS output enable register
PFCSS0	—	—	CS output pin select register 0
PFAOE0	—	—	Address output enable register 0
PFAOE1	—	—	Address output enable register 1
PFBCR0	—	—	External bus control register 0
PFBCR1	—	—	External bus control register 1
PFBCR2	—	—	External bus control register 2
PFBCR3	—	—	External bus control register 3

2.15 Multi-Function Timer Pulse Unit 2/Multi-Function Timer Pulse Unit 3

Table 2.51 is Comparative Overview of Multi-Function Timer Pulse Unit 2 and Multi-Function Timer Pulse Unit 3, and Table 2.52 is Register Comparison of Multi-Function Timer Pulse Unit 2 and Multi-Function Timer Pulse Unit 3.

Table 2.51 Comparative Overview of Multi-Function Timer Pulse Unit 2 and Multi-Function Timer Pulse Unit 3

Item	RX140 (MTU2a)	RX660 (MTU3a)
Pulse input/output	Max. 16 lines	Max. 28 lines
Pulse input	3 lines	3 lines
Count clocks	8 or 7 clocks for each channel (4 clocks for MTU5)	11 clocks for each channel (MTU0: 14, MTU2: 12, MTU5: 10, MTU1 & MTU2: (when LWA = 1) 4)
Available operations	[MTU0 to MTU4] • Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Simultaneous register input/output by synchronous counter operation • Up to 12-phase PWM output in combination with synchronous operation	[MTU0 to MTU4, MTU6, MTU7, MTU8] • Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) (excluding MTU8) • Simultaneous clearing by compare match or input capture (excluding MTU8) • Simultaneous register input/output by synchronous counter operation (excluding MTU8) • Up to 12-phase PWM output in combination with synchronous operation (excluding MTU8)
	[MTU0, MTU3, MTU4] • Ability to specify buffer operation • Ability to specify the AC synchronous motor (brushless DC motor) drive mode using complementary PWM or reset-synchronized PWM and to select two types (chopping or level) of waveform output	[MTU0, MTU3, MTU4, MTU6, MTU7, MTU8] • Ability to specify buffer operation
	[MTU1, MTU2] • Independent specification of phase counting mode • Cascade connection operation	[MTU1, MTU2] • Independent specification of phase counting mode • Ability to specify 32-bit phase counting mode linked to MTU1 or MTU2 (when TMDR3.LWA = 1) • Cascade connection operation

Item	RX140 (MTU2a)	RX660 (MTU3a)
Available operations	—	[MTU3, MTU4, MTU6, MTU7] • Ability to produce 12-phase waveform output, comprising six phases each of positive and negative output, in complementary PWM or reset-synchronized PWM mode, through linked operation of MTU3 or MTU4 and MTU6 or MTU7 • In complementary PWM mode, ability to transfer data from the buffer register to a temporary register at peaks or troughs of the timer counter or when writes to the buffer register (MTU4.TGRD or MTU7.TGRD) occur • Ability to specify double buffer function in complementary PWM mode
	[MTU3, MTU4] • Through linked operation, complementary PWM and 6-phase output of positive and negative 3-phase reset PWM are possible.	[MTU3, MTU4] • Through linked operation with MTU0, ability to specify the AC synchronous motor (brushless DC motor) drive mode using complementary PWM or reset-synchronized PWM and to select two types (chopping or level) of waveform output
	[MTU5] • Dead time compensation counter function • Input capture function (Noise filter setting is possible.) • Counter clear operation	[MTU5] • Can be used as a dead time compensation counter.
	—	[MTU0/MTU5, MTU1, MTU2, MTU8] Combining MTU1 and MTU2, and with linked operation with MTU0/MTU5 and MTU8, 32-bit phase counting mode can be configured.
Interrupt skipping function	In Complementary PWM mode • Interrupt at peak or trough of counter • A/D conversion start trigger skipping function	Ability to skip interrupts at counter peak or trough and A/D conversion start triggers in complementary PWM mode
Interrupt sources	28 sources	43 sources
Buffer operation	Automatic transfer of register data	Automatic transfer of register data (transfer from buffer register to timer register)
Trigger generation	• Ability to generate A/D conversion start trigger	• Ability to generate A/D conversion start trigger • Ability to start A/D conversion at user-specified timing using A/D conversion start request delaying function Ability to synchronize operation with PWM output
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Table 2.52 Register Comparison of Multi-Function Timer Pulse Unit 2 and Multi-Function Timer Pulse Unit 3

Register	Bit	RX140 (MTU2a)	RX660 (MTU3a)
TCR2	—	—	Timer control register 2
TMDR (RX140) TMDR1 (RX660)	—	Timer mode register	Timer mode register 1
TMDR2m	—	—	Timer mode register 2 (m = A, B)
TMDR3	—	—	Timer mode register 3
MTU0, TIORH	IOA[3:0]	I/O control A bits b3 b0 0 0 0 0: Output disabled 0 0 0 1: Initial output is Low Low output at compare match 0 0 1 0: Initial output is Low High output at compare match 0 0 1 1: Initial output is Low Toggle output at compare match 0 1 0 0: Output disabled 0 1 0 1: Initial output is High Low output at compare match 0 1 1 0: Initial output is High High output at compare match 0 1 1 1: Initial output is High Toggle output at compare match 1 0 0 0: Input capture at rising edge 1 0 0 1: Input capture at falling edge 1 0 1 x: Input capture at both edges 1 1 x x: Capture input source is the clock source for counting in MTU1. Input capture at count-up/down of MTU1.TCNT	I/O control A bits b3 b0 0 0 0 0: Output disabled 0 0 0 1: Initial output is Low Low output at compare match 0 0 1 0: Initial output is Low High output at compare match 0 0 1 1: Initial output is Low Toggle output at compare match 0 1 0 0: Output disabled 0 1 0 1: Initial output is High Low output at compare match 0 1 1 0: Initial output is High High output at compare match 0 1 1 1: Initial output is High Toggle output at compare match 1 0 0 0: Input capture at rising edge 1 0 0 1: Input capture at falling edge 1 0 1 x: Input capture at both edges 1 1 0 0: Capture input source is the clock source for counting in MTU1. Input capture at count-up/down of MTU1.TCNT (LWA = 0) or MTU1.TCNTLW (LWA = 1) 1 1 1 x: Input capture at compare match of MTU8.TGRC

Register	Bit	RX140 (MTU2a)	RX660 (MTU3a)
MTU1, TIOR	IOB[3:0]	I/O control B bits b3 b0 0 0 0 0: Output disabled 0 0 0 1: Initial output is Low Low output at compare match 0 0 1 0: Initial output is Low High output at compare match 0 0 1 1: Initial output is Low Toggle output at compare match 0 1 0 0: Output disabled 0 1 0 1: Initial output is High Low output at compare match 0 1 1 0: Initial output is High High output at compare match 0 1 1 1: Initial output is High Toggle output at compare match 1 0 0 0: Input capture at rising edge 1 0 0 1: Input capture at falling edge 1 0 1 x: Input capture at both edges 1 1 x x: Input capture at compare match or input capture of MTU0.TGRC	I/O control B bits b3 b0 0 0 0 0: Output disabled 0 0 0 1: Initial output is Low Low output at compare match 0 0 1 0: Initial output is Low High output at compare match 0 0 1 1: Initial output is Low Toggle output at compare match 0 1 0 0: Output disabled 0 1 0 1: Initial output is High Low output at compare match 0 1 1 0: Initial output is High High output at compare match 0 1 1 1: Initial output is High Toggle output at compare match 1 0 0 0: Input capture at rising edge 1 0 0 1: Input capture at falling edge 1 0 1 x: Input capture at both edges 1 1 0 0: Input capture at compare match or input capture of MTU0.TGRC 1 1 1 x: Input capture at compare match of MTU8.TGRC
TIORU TIORV TIORW	IOC[4:0]	I/O control C bits b4 b0 0 0 0 0 0: Compare match 0 0 0 0 1: Setting prohibited 0 0 0 1 x: Setting prohibited 0 0 1 x x: Setting prohibited 0 1 x x x: Setting prohibited 1 0 0 0 0: Setting prohibited 1 0 0 0 1: Input capture at rising edge 1 0 0 1 0: Input capture at falling edge 1 0 0 1 1: Input capture at both edges 1 0 1 x x: Setting prohibited 1 1 0 0 0: Setting prohibited	I/O control C bits b4 b0 0 0 0 0 0: No function 0 0 0 0 1: Setting prohibited 0 0 0 1 x: Setting prohibited 0 0 1 x x: Setting prohibited 0 1 x x x: Setting prohibited 1 0 0 0 0: Setting prohibited 1 0 0 0 1: Input capture at rising edge 1 0 0 1 0: Input capture at falling edge 1 0 0 1 1: Input capture at both edges 1 0 1 x x: Capture at compare match of MTU8.TGRC 1 1 0 0 0: Setting prohibited

Register	Bit	RX140 (MTU2a)	RX660 (MTU3a)
TIORU TIORV TIORW	IOC[4:0]	1 1 0 0 1: Capture at troughs of complementary PWM mode for measuring the width of Low pulses of external input signal 1 1 0 0 1: Capture at peaks of complementary PWM mode for measuring the width of Low pulses of external input signal 1 1 0 1 1: Capture at peaks and troughs of complementary PWM mode for measuring the width of Low pulses of external input signal 1 1 1 0 0: Setting prohibited 1 1 1 0 1: Capture at troughs of complementary PWM mode for measuring the width of High pulses of external input signal 1 1 1 1 0: Capture at peaks of complementary PWM mode for measuring the width of High pulses of external input signal 1 1 1 1 1: Capture at peaks and troughs of complementary PWM mode for measuring the width of High pulses of external input signal	1 1 0 0 1: Capture at troughs of complementary PWM mode for measuring the width of Low pulses of external input signal 1 1 0 0 1: Capture at peaks of complementary PWM mode for measuring the width of Low pulses of external input signal 1 1 0 1 1: Capture at peaks and troughs of complementary PWM mode for measuring the width of Low pulses of external input signal 1 1 1 0 0: Setting prohibited 1 1 1 0 1: Capture at troughs of complementary PWM mode for measuring the width of High pulses of external input signal 1 1 1 1 0: Capture at peaks of complementary PWM mode for measuring the width of High pulses of external input signal 1 1 1 1 1: Capture at peaks and troughs of complementary PWM mode for measuring the width of High pulses of external input signal
TIER	TTGE2	A/D conversion start request enable 2 bit 0: A/D conversion at MTU4.TCNT underflow (trough) is disabled 1: A/D conversion at MTU4.TCNT underflow (trough) is enabled	A/D conversion start request enable 2 bit 0: A/D conversion at MTUn.TCNT underflow (trough) is disabled (n = 4, 7) 1: A/D conversion at MTUn.TCNT underflow (trough) is enabled (n = 4, 7)
TSYCR	—	—	Timer synchronous clear register
TCNTLW	—	—	Timer longword counter
TGRALW/ TGRBLW	—	—	Timer longword general register

Register	Bit	RX140 (MTU2a)	RX660 (MTU3a)
TSTR (RX140) TSTR/TSTRA/TSTRB (RX660)	CST8	—	Counter start 8 bit
TSYR (RX140) TSYRm (RX660)	—	Timer synchronous register	Timer synchronous register m (m = A, B)
TCSYSTR	—	—	Timer counter synchronous start register
TRWER (RX140) TRWERm (RX660)	—	Timer read/write enable register	Timer read/write enable register m (m = A, B)
TOER (RX140) TOERm (RX660)	—	Timer output master enable register	Timer output master enable register m (m = A, B)
TOCR1 (RX140) TOCR1m (RX660)	—	Timer output control register 1	Timer output control register 1m (m = A, B)
TOCR2 (RX140) TOCR2m (RX660)	—	Timer output control register 2	Timer output control register 2m (m = A, B)
TOLBR TOLBRm (RX660)	—	Timer output level buffer register	Timer output level buffer register m (m = A, B)
TGCR (RX140) TGCRA (RX660)	—	Timer gate control register	Timer gate control register A
TCNTS (RX140) TCNTSm (RX660)	—	Timer subcounter	Timer subcounter m (m = A, B)
TCDR (RX140) TCDRm (RX660)	—	Timer period data register	Timer period data register m (m = A,B)
TCBR (RX140) TCBRm (RX660)	—	Timer period buffer register	Timer period buffer register m (m = A, B)
TDDR (RX140) TDDRm (RX660)	—	Timer dead time data register	Timer dead time data register m (m = A, B)
TITCR (RX140) TITCR1m (RX660)	—	Timer interrupt skipping set register	Timer interrupt skipping set register 1m (m = A, B)
TITCNT (RX140) TITCNT1m (RX660)	—	Timer interrupt skipping counter	Timer interrupt skipping counter 1m (m = A, B)
TBTER (RX140) TBTERm (RX660)	—	Timer buffer transfer set register	Timer buffer transfer set register m (m = A, B)
TDER (RX140) TDERm (RX660)	—	Timer dead time enable register	Timer dead time enable register m (m = A, B)
TWCR (RX140) TWCRm (RX660)	SCC	—	Synchronous clearing control bit
NFCR (RX140) NFCRn (RX660)	—	Noise filter control register	Noise filter control register n (n = 0 to 4, 6, 7, 8, C)
NFCR5	—	—	Noise filter control register 5
TITMRm	—	—	Timer interrupt skipping mode register (m = A, B)
TITCR2m	—	—	Timer interrupt skipping set register 2 (m = A, B)
TITCNT2m	—	—	Timer interrupt skipping counter 2 (m = A, B)

2.16 Port Output Enable 2/Port Output Enable 3

Table 2.53 is Comparative Overview of Port Output Enable 2 and Port Output Enable 3, and Table 2.54 is Register Comparison of Port Output Enable 2 and Port Output Enable 3.

Table 2.53 Comparative Overview of Port Output Enable 2 and Port Output Enable 3

Item	RX140 (POE2a)	RX660 (POE3a)
Pin status while output is disabled	High-impedance	High-impedance
High-impedance control target pins	• MTU output pins — MTU0 pin (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) — MTU3 pin (MTIOC3B, MTIOC3D) — MTU4 pin (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D)	• MTU output pins — MTU0 pin (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) — MTU3 pin (MTIOC3B, MTIOC3D) — MTU4 pin (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) — MTU6 pin (MTIOC6B, MTIOC6D) — MTU7 pin (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D)
High-impedance request occurrence condition	• Input pin changes When signal input occurs on pin POE0# to POE3#, or POE8# • Short circuit of output pins Comparing the output levels of the MTU complementary PWM output pins, the pins can be set to high-impedance when simultaneous output of the active level continues for one or more PCLK clocks. [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D • SPOER register settings are specified.	• Input pin changes When signal input occurs on pin POE0#, POE4#, POE8#, POE10#, or POE11# • Short circuit of output pins A match (short circuit) of output signal levels (active level) lasting one or more cycles on one of the combinations of pins listed below [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D — MTIOC6B and MTIOC6D — MTIOC7A and MTIOC7C — MTIOC7B and MTIOC7D • SPOER register settings are specified. • Detection of stopped oscillation on main clock oscillator

Item	RX140 (POE2a)	RX660 (POE3a)
Functions	• Falling-edge detection or sampling of the low level 16 times at PCLK/8, PCLK/16, or PCLK/128 clock can be set for each of the POE0# to POE3#, POE8# input pins. • The MTU complementary PWM output pins can be set to high impedance by falling-edge detection or sampling of the low level on POE0# to POE3# pins. • The MTU0 output pin can be set to high impedance by falling-edge detection or sampling of the low level on the POE8# pin. • The MTU complementary PWM output pins and the MTU0 output pin can be set to high-impedance when the clock generation circuit stops oscillation. • Comparing the output levels of the MTU complementary PWM output pins, the pins can be set to high-impedance when simultaneous output of the active level continues for one or more PCLK clocks. • The MTU complementary PWM output pins and the MTU0 output pin can be set to high-impedance by writing in the POE register. • Interrupt is generated according to the input level detection result of POE0# to POE3# and POE8# and the output level comparison result of the MTU complementary PWM output pins.	• Falling-edge detection or sampling of the low level 16 times at PCLK/8, PCLK/16, or PCLK/128 can be set for each of the POE0#, POE4#, POE8#, POE10#, and POE11# input pins. • Output on all control target pins can be set to high-impedance by falling-edge detection or sampling of the low level on the POE0#, POE4#, POE8#, POE10#, and POE11# pins. • Output on all control target pins can be set to high-impedance when oscillation stop is detected on the clock generation circuit. • Comparing the output levels of the MTU complementary PWM output pins, the pins can be set to high-impedance when simultaneous output of the active level continues for one or more cycles. • Output on all control target pins can be set to high-impedance by setting the POE3 register. • Interrupts can be generated in response to the results of input level sampling or output-level comparison.

Table 2.54 Register Comparison of Port Output Enable 2 and Port Output Enable 3

Register	Bit	RX140 (POE2a)	RX660 (POE3a)
ICSR1	POE1M[1:0]	POE1 mode select bits	—
	POE2M[1:0]	POE2 mode select bits	—
	POE3M[1:0]	POE3 mode select bits	—
	POE1F	POE1 flag	—
	POE2F	POE2 flag	—
	POE3F	POE3 flag	—
ICSR2	POE8M[1:0]	POE8 mode select bits	—
	POE4M[1:0]	—	POE4 mode select bits
	POE8E	POE8 high-impedance enable bit	—
	POE8F	POE8 flag	—
	POE4F	—	POE4 flag
ICSR3	OSTSTE	OSTST high-impedance enable bit	—
	OSTSTF	OSTST high-impedance flag	—
	POE8M[1:0]	—	POE8 mode select bits
	PIE3	—	Port interrupt enable 3 bit
	POE8E	—	POE8 high-impedance enable bit
	POE8F	—	POE8 flag
ICSR4	—	—	Input level control/status register 4
ICSR5	—	—	Input level control/status register 5

Register	Bit	RX140 (POE2a)	RX660 (POE3a)
ICSR6	—	—	Input level control/status register 6
OCSR2	—	—	Output level control/status register 2
ALR1	—	—	Active level register 1
SPOER	CH34HIZ (RX140) MTUCH34HIZ (RX660)	MTU3/MTU4 output high-impedance enable bit	MTU3 and MTU4 pin high-impedance enable bit
	MTUCH67HIZ	—	MTU6 and MTU7 pin high-impedance enable bit
	CH0HIZ (RX140) MTUCH0HIZ (RX660)	MTU0 output high-impedance enable bit (b1)	MTU0 pin high-impedance enable bit (b2)
POECR1	PE0ZE (RX140) MTU0AZE (RX660)	MTIOC0A high-impedance enable bit	MTIOC0A pin high-impedance enable bit
	PE1ZE (RX140) MTU0BZE (RX660)	MTIOC0B high-impedance enable bit	MTIOC0B pin high-impedance enable bit
	PE2ZE (RX140) MTU0CZE (RX660)	MTIOC0C high-impedance enable bit	MTIOC0C pin high-impedance enable bit
	PE3ZE (RX140) MTU0DZE (RX660)	MTIOC0D high-impedance enable bit	MTIOC0D pin high-impedance enable bit
POECR2	—	Port output enable control register 2 POECR2 is an 8-bit register.	Port output enable control register 2 POECR2 is a 16-bit register.
	MTU7BDZE	—	MTIOC7B/MTIOC7D pin high-impedance enable bit
	MTU7ACZE	—	MTIOC7A/MTIOC7C pin high-impedance enable bit
	MTU6BDZE	—	MTIOC6B/MTIOC6D pin high-impedance enable bit
	P3CZEA (RX140) MTU4BDZE (RX660)	MTU port 3 high-impedance enable bit (b4)	MTIOC4B/MTIOC4D pin high-impedance enable bit (b8)
	P2CZEA (RX140) MTU4ACZE (RX660)	MTU port 2 high-impedance enable bit (b5)	MTIOC4A/MTIOC4C pin high-impedance enable bit (b9)
	P1CZEA (RX140) MTU3BDZE (RX660)	MTU port 1 high-impedance enable bit (b6)	MTIOC3B/MTIOC3D pin high-impedance enable bit (b10)
POECR4	—	—	Port output enable control register 4
POECR5	—	—	Port output enable control register 5
ICSR3	—	Input level control/status register 3	—

Register	Bit	RX140 (POE2a)	RX660 (POE3a)
M0SELR1	—	—	MTU0 pin select register 1
M0SELR2	—	—	MTU0 pin select register 2
M3SELR	—	—	MTU3 pin select register
M4SELR1	—	—	MTU4 pin select register 1
M4SELR2	—	—	MTU4 pin select register 2

2.17 8-Bit Timer

Table 2.55 is Comparative Overview of 8-Bit Timers, and Table 2.56 is Comparison of 8-Bit Timer Registers.

Table 2.55 Comparative Overview of 8-Bit Timers

Item	RX140 (TMRa)	RX660 (TMRb)
Count clocks	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock: External count clock	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock: External count clock
Number of channels	(8 bits × 2 channels) × 2 units	(8 bits × 2 channels) × 2 units
Compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selectable among compare match A or B, or an external counter reset signal	Selectable among compare match A or B, or an external counter reset signal
Timer output	Output pulses with a user-defined duty cycle or PWM output	Output pulses with a user-defined duty cycle or PWM output
Cascading of two channels	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
Event link function (output)	Compare match A, compare match B, and overflow (TMR0 and TMR2)	Compare match A, compare match B, and overflow (TMR0 to TMR3)
Event link function (input)	Ability to perform one of three actions according to accepted event (1) Counter start (TMR0 and TMR2) (2) Event counter (TMR0 and TMR2) (3) Counter restart (TMR0 and TMR2)	Ability to perform one of three actions according to accepted event (1) Counter start (TMR0 to TMR3) (2) Event counter (TMR0 to TMR3) (3) Counter restart (TMR0 to TMR3)
DTC activation	The DTC can be activated by compare match A interrupts or compare match B interrupts.	The DTC can be activated by compare match A interrupts or compare match B interrupts.
Generation of trigger to start A/D converter	—	Compare match A of TMR0 or TMR2
Generation of SCI basic clock	Generation of SCI basic clock	Generation of SCI basic clock
Generation of REMC reception clock	—	Generation of operating clock of REMC (remote controller signal receiver)

Item	RX140 (TMRa)	RX660 (TMRb)
Low power consumption function	Ability to transition each unit to the module stop state	Ability to transition each unit to the module stop state

Table 2.56 Comparison of 8-Bit Timer Registers

Register	Bit	RX140 (TMRa)	RX660 (TMRb)
TCSR	ADTE	—	A/D trigger enable bit

2.18 Compare Match Timer (CMT)

Table 2.57 is Comparative Overview of Compare Match Timers, and Table 2.58 is Register Comparison of Compare Match Timers.

Table 2.57 Comparative Overview of Compare Match Timers

Item	RX140 (CMT)	RX660 (CMT)
Number of channels	2 channels	4 channels
Count clocks	Four frequency dividing clocks: One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.	Four frequency dividing clocks: One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.
Interrupt	A compare match interrupt can be requested for each channel.	A compare match interrupt can be requested for each channel.
Event link function (output)	An event signal is output upon a CMT1 compare match.	An event signal is output upon a CMT1 compare match.
Event link function (input)	Linking to the specified module is possible. CMT1 count start, event counter, or count restart operation is possible.	Linking to the specified module is possible. CMT1 count start, event counter, or count restart operation is possible.
Low power consumption function	Ability to specify module stop state	Ability to transition each unit to the module stop state

Table 2.58 Register Comparison of Compare Match Timers

Register	Bit	RX140 (CMT)	RX660 (CMT)
CMSTR1	—	—	Compare match timer start register 1

2.19 Realtime Clock

Table 2.59 is Comparative Overview of Realtime Clocks, and Table 2.60 is Register Comparison of Realtime Clocks.

Table 2.59 Comparative Overview of Realtime Clocks

Item	RX140 (RTCB)	RX660 (RTCC)
Count mode	Calendar count mode/binary count mode	Calendar count mode/binary count mode
Count source	Sub-clock (XCIN)	Sub-clock (XCIN)
Clock and calendar functions	• Calendar count mode Year, month, day, day of the week, hour, minute, and second are counted and displayed in BCD. 12/24 hour modes switching function 30-seconds rounding function (Seconds less than 30 are rounded down to 00 second, seconds equal to or larger than 30 are rounded up to 1 minute.) Leap year auto correction • Binary count mode Seconds are counted by 32 bits, and displayed in binary. • Common in both modes Start/stop function Binary display of digits of second and lower (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, 64 Hz) Clock error correction function Clock (1 Hz/64 Hz) output	• Calendar count mode Year, month, day, day of the week, hour, minute, and second are counted and displayed in BCD. 12/24 hour modes switching function 30-seconds rounding function (Seconds less than 30 are rounded down to 00 second, seconds equal to or larger than 30 are rounded up to 1 minute.) Leap year auto correction • Binary count mode Seconds are counted by 32 bits, and displayed in binary. • Common in both modes Start/stop function Binary display of digits of second and lower (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, 64 Hz) Clock error correction function Clock (1 Hz/64 Hz) output

Item	RX140 (RTCB)	RX660 (RTCC)
Interrupt	• Alarm interrupt (ALM) One of the following can be selected as the comparison condition for alarm interrupt. — Calendar count mode Year, month, day, day of the week, hour, minute, and second — Binary count mode Each bit of the 32-bit binary counter • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second can be selected as an interrupt period. • Carry interrupt (CUP) Interrupt request occurs at one of the following timings. — When a carry from the 64Hz counter to the second counter occurs. — When change of the 64Hz counter and read of the R64CNT register occurs at the same time • Exit from software standby mode is possible by an alarm interrupt or a periodic interrupt.	• Alarm interrupt (ALM) One of the following can be selected as the comparison condition for alarm interrupt. — Calendar count mode Year, month, day, day of the week, hour, minute, and second — Binary count mode Each bit of the 32-bit binary counter • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second can be selected as an interrupt period. • Carry interrupt (CUP) Interrupt request occurs at one of the following timings. — When a carry from the 64Hz counter to the second counter occurs. — When change of the 64Hz counter and read of the R64CNT register occurs at the same time • Exit from software standby mode or deep software standby mode is possible by an alarm interrupt or a periodic interrupt.
Time capture function	—	Time can be captured by the edge detection of the time capture event input pin. For each event input, month, day, hour, minute, and second is captured or the 32-bit binary counter value is captured.
Event link function	—	Periodic event output

Table 2.60 Register Comparison of Realtime Clocks

Register	Bit	RX140 (RTCB)	RX660 (RTCC)
RCR3	—	—	RTC control register 3
RCR4	—	—	RTC control register 4
RTCCRn	—	—	Time capture control register n (n = 0 to 2)
RSECCPn/ BCNT0CPn	—	—	Second capture register n (n = 0 to 2)/ BCNT0 capture register n (n = 0 to 2)
RMINCPn/ BCNT1CPn	—	—	Minute capture register n (n = 0 to 2)/ BCNT1 capture register n (n = 0 to 2)
RHRCPn/ BCNT2CPn	—	—	Hour capture register n (n = 0 to 2)/ BCNT2 capture register n (n = 0 to 2)
RDAYCPn/ BCNT3CPn	—	—	Day capture register n (n = 0 to 2)/ BCNT3 capture register n (n = 0 to 2)
RMONCPn	—	—	Month capture register n (n = 0 to 2)

2.20 Independent Watchdog Timer

Table 2.61 is Comparative Overview of Independent Watchdog Timers, and Table 2.62 is Comparison of Independent Watchdog Timer Registers.

Table 2.61 Comparative Overview of Independent Watchdog Timers

Item	RX140 (IWDTa)	RX660 (IWDTa)
Count source	IWDT-dedicated clock (IWDTCLK)	IWDT-dedicated clock (IWDTCLK)
Clock division ratio	Divide by 1, 16, 32, 64, 128, or 256	Divide by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Auto-start mode: Counting starts automatically after a reset. • Register start mode: Counting starts by refreshing the counter (writing 00h and then FFh to the IWDTRR register).	• Auto-start mode: Counting starts automatically after a reset. • Register start mode: Counting starts by refreshing the counter (writing 00h and then FFh to the IWDTRR register).
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • Low power consumption state (by means of register setting) • Underflow or refresh error (register start mode only)	• Reset (the down-counter and other registers return to their initial values) • Low power consumption state (by means of register setting) • Underflow or refresh error (register start mode only)
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Reset output sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt/ interrupt sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	• The down-counter value can be read by the IWDTSR register.	• The down-counter value can be read by the IWDTSR register.
Event link function (output)	—	• Down-counter underflow event output • Refresh error event output
Output signals (internal signals)	• Reset output • Interrupt request output • Sleep mode count stop control output	• Reset output • Interrupt request output • Sleep mode count stop control output

Item	RX140 (IWDTa)	RX660 (IWDTa)
Auto-start mode (controlled by option function select register 0 (OFS0))	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (OFS0.IWDTSLCSTP bit)	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)
Register start mode (controlled by the IWDT registers)	• Selecting the clock frequency division ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (IWDTCSTPR.SLCSTP bit)	• Selecting the clock frequency division ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bit) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)

Table 2.62 Comparison of Independent Watchdog Timer Registers

Register	Bit	RX140 (IWDTa)	RX660 (IWDTa)
IWDTCR	TOPS[1:0]	Timeout period select bits b1 b0 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1,024 cycles (03FFh) 1 1: 2,048 cycles (07FFh)	Timeout period select bits b1 b0 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh)
IWDTRCR	RSTIRQS	Reset interrupt request select bit 0: Non-maskable interrupt request output is enabled. 1: Reset output is enabled.	Reset interrupt request select bit 0: Non-maskable interrupt request or interrupt request output is enabled. 1: Reset output is enabled.
IWDTCSTPR	SLCSTP	Sleep mode count stop control bit 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, and deep sleep mode.	Sleep mode count stop control bit 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, deep software standby, or all-module clock stop mode.

2.21 Serial Communication Interface

Table 2.63 is Comparative Overview of Serial Communications Interfaces, Table 2.64 is Comparison of Serial Communications Interface Channel Specifications, and Table 2.65 is Comparison of Serial Communications Interface Registers.

Table 2.63 Comparative Overview of Serial Communications Interfaces

Item		RX140 (SCIg, SCIk, SCIh)	RX660 (SCIk, SCIm, SCIh)
Number of channels		• SCIg: 2 channels • SCIk: 3 channels • SCIh: 1 channel	• SCIk: 10 channels • SCIm: 2 channels • SCIh: 1 channel
Serial communications modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I^2C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I^2C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		LSB first or MSB first can be selected.	LSB first or MSB first can be selected.
I/O signal level inversion		The levels of input and output signals can be inverted independently (SCI1 and SCI5).	The levels of input and output signals can be inverted independently.
Interrupt sources		• Transmit end, transmit data empty, receive data full, receive error, and data match • Completion of generation of a start condition, restart condition, or stop condition (for simple I^2C mode)	• Transmit end, transmit data empty, receive data full, receive error, receive data ready (SCI10 and SCI11), and data match • Completion of generation of a start condition, restart condition, or stop condition (for simple I^2C mode)
Low power consumption function		Individual channels can be transitioned to the module stop state.	Individual channels can be transitioned to the module stop state.
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity function	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection function	Parity error, overrun error, and framing error	Parity error, overrun error, and framing error
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Transmit/ receive FIFO	—	FIFO of 16 lines is available for transmission and FIFO of 16 lines is available for reception (SCI10 and SCI11).
	Data match detection	Compares receive data and comparison data register, and generates interrupt when they match (SCI1 and SCI5).	Compares receive data and comparison data register, and generates interrupt when they match.
	Start-bit detection	Low level or falling edge is selectable.	Low level or falling edge is selectable.

Item		RX140 (SCIg, SCIk, SCIh)	RX660 (SCIk, SCIm, SCIh)
Asynchronous mode	Receive data sampling timing adjustment	The receive data sampling point can be shifted from the center of the data forward or backward to a base point (SCI1, SCI5).	The receive data sampling point can be shifted from the center of the data forward or backward to a base point (SCI0 to SCI11).
	Transmit signal change timing adjustment	Either the falling or rising edge of the transmit data can be delayed (SCI1, SCI5).	Either the falling or rising edge of the transmit data can be delayed (SCI0 to SCI11).
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly or by reading the SPTR.RXDMON flag.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly or by reading the SPTR.RXDMON flag.
	Clock source	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5, SCI6).	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5, SCI6, and SCI12).
	Double-speed mode	Baud rate generator double-speed mode can be selected.	Baud rate generator double-speed mode can be selected.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Transmit/ receive FIFO	—	FIFO of 16 lines is available for transmission and FIFO of 16 lines is available for reception (SCI10 and SCI11).
Smart card interface mode	Error processing	• An error signal can be automatically transmitted when detecting a parity error during reception. • Data can be automatically retransmitted when receiving an error signal during transmission.	• An error signal can be automatically transmitted when detecting a parity error during reception. • Data can be automatically retransmitted when receiving an error signal during transmission.
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	I^2C bus format	I^2C bus format
	Operation mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer speed	Fast mode supported	Fast mode supported
	Noise cancellation	• The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters. • The interval for noise cancellation is adjustable.	• The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters. • The interval for noise cancellation is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.

Item		RX140 (SCIg, SCIk, SCIh)	RX660 (SCIk, SCIm, SCIh)
Extended serial mode (supported by SCI12 only)	Start frame transmission	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection
	Start frame reception	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two kinds of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two kinds of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates
	I/O control function	• Ability to select polarity for TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select receive data sampling timing of RXDX12 pin	• Ability to select polarity for TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select receive data sampling timing of RXDX12 pin
	Timer function	Usable as reloading timer	Usable as reloading timer
Bit rate modulation function		Correction of outputs from the on-chip baud rate generator can reduce errors.	Correction of outputs from the on-chip baud rate generator can reduce errors.
Event link function (supported by SCI5 only)		• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output	• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output

Table 2.64 Comparison of Serial Communications Interface Channel Specifications

Item	RX140 (SCIg, SCIk, SCIh)	RX660 (SCIk, SCIm, SCIh)
Asynchronous mode	SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12
Clock synchronous mode	SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12
Smart card interface mode	SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12
Simple I^2C mode	SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12
Simple SPI mode	SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12
FIFO mode	—	SCI10, SCI11
Data match detection	SCI1, SCI5	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11
Extended serial mode	SCI12	SCI12
TMR clock input	SCI5, SCI6, SCI12	SCI5, SCI6, SCI12
Event link function	SCI5	SCI5
Peripheral module clock	PCLKB: SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	PCLKA: SCI10, SCI11 PCLKB: SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI12

Table 2.65 Comparison of Serial Communications Interface Registers

Register	Bit	RX140 (SCIg, SCIk, SCIh)	RX660 (SCIk, SCIm, SCIh)
FRDR	—	—	Receive FIFO data register
FTDR	—	—	Transmit FIFO data register
TSR	—	—	Transmit shift register
SSR (RX140) SSR/ SSRFIFO (RX660)	—	Serial status register	Serial status register When not in smart card interface mode and in FIFO mode (SCMR.SMIF bit = 0, and FCR.FM bit = 1)
	DR	—	Receive data ready flag
	RDF	—	Receive FIFO full flag
	TDFE	—	Transmit FIFO empty flag
SEMR	ITE	—	Immediate transmission enable bit
	ABCSE	—	Asynchronous mode base clock select extended bit
FCR	—	—	FIFO control register
FDR	—	—	FIFO data count register
LSR	—	—	Line status register

2.22 I²C Bus Interface

Table 2.66 is Register Comparison of I²C Bus Interfaces.

Table 2.66 Register Comparison of I²C Bus Interfaces

Register	Bit	RX140 (RIICa)	RX660 (RIICa)
ICCR1	SDAI	SDA line monitor bit 0: SDA0 line is Low 1: SDA0 line is High	SDA line monitor bit (n = 0, 2) 0: SDAn line is Low 1: SDAn line is High
	SCLI	SCL line monitor bit 0: SCL0 line is Low 1: SCL0 line is High	SCL line monitor bit (n = 0, 2) 0: SCLn line is Low 1: SCLn line is High
	SDAO	SDA output control/monitor bit • When reading 0: SDA0 pin is set to Low 1: SDA0 pin is opened • When writing 0: Sets the SDA0 pin to Low 1: Opens the SDA0 pin (High is output by external pull-up resistance.)	SDA output control/monitor bit (n = 0, 2) • When reading 0: SDAn pin is set to Low 1: SCLn pin is opened • When writing 0: Sets the SCLn pin to Low 1: Opens the SCLn pin (High is output by external pull-up resistance.)
	SCLO	SCL output control/monitor bit • When reading 0: SCL0 pin is set to Low 1: SCL0 pin is opened • When writing 0: Sets the SCL0 pin to Low 1: Opens the SCL0 pin (High is output by external pull-up resistance.)	SCL output control/monitor bit (n = 0, 2) • When reading 0: SCLn pin is set to Low 1: SCLn pin is opened • When writing 0: Sets the SCLn pin to Low 1: Opens the SCLn pin (High is output by external pull-up resistance.)
	IICRST	I²C bus interface internal reset bit 0: Releases the RIIC reset or internal reset 1: Initiates the RIIC reset or internal reset (The bit counter is cleared, and the SCL0/SDA0 output latch is released.)	I²C bus interface internal reset bit (n = 0, 2) 0: Releases the RIIC reset or internal reset 1: Initiates the RIIC reset or internal reset (The bit counter is cleared, and the SCLn/SDAn output latch is released.)
	ICE	I²C bus interface enable bit 0: Disabled (SCL0 and SDA0 pins inactive) 1: Enabled (SCL0 and SDA0 pins active) (RIIC reset or internal reset is selected by the combination with the IICRST bit.)	I²C bus interface enable bit (n = 0,2) 0: Disabled (SCLn and SDAn pins inactive) 1: Enabled (SCLn and SDAn pins active) (RIIC reset or internal reset is selected by the combination with the IICRST bit.)

Register	Bit	RX140 (RIICa)	RX660 (RIICa)
ICMR2	TMOL	Timeout L count control bit 0: Counting-up is disabled when the SCL0 line is Low 1: Counting-up is enabled when the SCL0 line is Low	Timeout L count control bit 0: Counting-up is disabled when the SCLn line is Low 1: Counting-up is enabled when the SCLn line is Low
	TMOH	Timeout H count control bit 0: Counting-up is disabled when the SCL0 line is High 1: Counting-up is enabled when the SCL0 line is High	Timeout H count control bit 0: Counting-up is disabled when the SCLn line is High 1: Counting-up is enabled when the SCLn line is High
ICMR3	RDRFS	RDRF flag set timing select bit 0: Becomes 1 at the rising edge of the 9th clock of the SCL clock (The SCL0 line is not held Low at the falling edge of the 8th clock.) 1: Becomes 1 at the rising edge of the 8th clock of the SCL clock (The SCL0 line is held Low at the falling edge of the 8th clock.) Holding of Low is released by writing in the ACKBT bit.	RDRF flag set timing select bit 0: Becomes 1 at the 9th rising edge of the SCL (The SCLn line is not held Low at the falling edge of the 8th clock.) 1: Becomes 1 at the 8th rising edge of the SCL (The SCLn line is held Low at the falling edge of the 8th clock.) Holding of Low is released by writing in the ACKBT bit.

2.23 CAN Module and CAN FD Module

Table 2.67 is Comparative Overview of CAN Module and CAN FD Module, and Table 2.68 is Comparison of CAN Module/CANFD Module Registers.

Table 2.67 Comparative Overview of CAN Module and CAN FD Module

Item	RX140 (RSCAN)	RX660 (CANFD-Lite)
Protocol	Conforming to the ISO 11898-1 specifications	Conforming to the ISO 11898-1:2015 specifications
Bit rate (RX140) Data transfer rate (RX660)	Maximum of 1 Mbps	Arbitration phase: Maximum of 1 Mbps Data phase: Maximum of 8 Mbps*1
Operating frequency	PCLKB: 40 MHz (max.) CANMCLK: 20 MHz (max.)	Register block: Maximum of 60 MHz (PCLKB) Message buffer RAM: Maximum of 120 MHz (PCLKA)
Operating clock for data link layer (DLL clock)	—	Maximum of 60 MHz (either CANFDMCLK or CANFDCLK can be selected)
Buffer (RX140) Message buffer (RX660)	A total of 20 buffers • Individual buffers: 4 buffers (4 buffers for one channel) Transmit buffer: 4 buffers per channel • Shared buffers: 16 buffers Receive buffer: 0 to 16 buffers Receive FIFO buffer: 2 FIFO buffers (up to 16 buffers allocatable to each) Transmit/receive FIFO buffer: A FIFO buffer per channel (up to 16 buffers allocatable to each)	• Four transmit message buffers • One transmit queue Automatic transfer of messages to the transmit queue is supported. • 32 receive message buffers
Frame type	• Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID) • Remote frame in base format (11-bit ID) • Remote frame in extended format (29-bit ID)	ClassicCAN (CAN2.0) • Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID) • Remote frame in base format (11-bit ID) • Remote frame in extended format (29-bit ID) CANFD*1 • Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID)
Reception	• Data frames and remote frames can be received. • The ID format to be received (base ID only, extended ID only, or both base ID and extended ID) can be selected. • Interrupts can be enabled or disabled for each FIFO. • Mirror function (to receive messages transmitted from the own CAN node) • Timestamp function (recording of 16-bit timer value indicating time message received)	• Data frames and remote frames can be received. • The ID format to be received (base ID only, extended ID only, or both base ID and extended ID) can be selected. • Receive message buffer interrupt can be enabled or disabled individually for each message buffer.
Data length	0 to 8 bytes	Classic CAN: 0 to 8 bytes CANFD: 0 to 8, 12, 16, 20, 24, 32, 48, and 64 bytes*1

Item	RX140 (RSCAN)	RX660 (CANFD-Lite)
Receive filter function (RX140) Acceptance filter (RX660)	• Receive messages can be selected according to 16 receive rules. • The number of receive rules (0 to 16) can be set for each channel. • Acceptance filter processing: ID and mask can be set for each receive rule. • DLC filter processing: A DLC check value can be set for each receive rule.	Filtering is possible in the following fields: • IDE bit (base format, extended format, or both) • ID field • RTR bit (data frame or remote frame) (only for Classic CAN) • DLC field Data (data length) The protection function when the payload size is exceeded is provided. Acceptance filter list (AFL) entries can be updated during communication.
Receive message transfer function	• Routing function to transfer receive messages to arbitrary destinations (can be transferred to up to two buffers). Transfer destination: Receive buffer, receive FIFO buffer, and transmit/receive FIFO buffer • Label addition function Label information can be stored together when storing a message in a receive buffer and FIFO buffer.	—
Transmission	• Data frames and remote frames can be sent. • The ID format to be sent (base ID only, extended ID only, or both base ID and extended ID) can be selected. • The one-shot transmission function can be selected. • Either ID priority transmission mode or transmit buffer priority transmission mode can be selected. • Transmission can be aborted (completion of abort can be confirmed with a flag). • Interrupt can be enabled or disabled individually for each transmit buffer, or transmit/receive FIFO buffer.	• Data frames and remote frames can be sent. • The ID format to be sent (base ID only or extended ID only) can be selected. • The one-shot transmission function can be selected. • Either ID priority transmission mode or message buffer number priority transmission mode can be selected. • Transmission requests can be aborted (completion of abort can be confirmed with a flag). • Channel transmission interrupt can be enabled and disabled.
FIFO	• Receive FIFO buffer: 2 FIFO buffers (up to 16 buffers allocatable to each) • Transmit/receive FIFO buffer: A FIFO buffer per channel (up to 16 buffers allocatable to each)	The FIFO size is programmable. • Two receive FIFOs • One common FIFO (Whether to use the FIFO as a receive FIFO or transmit FIFO can be selected.)
Interval transmission function (RX140) Automatic transmission interval adjustment (RX660)	The message transmission interval time can be set. (transmit mode of transmit/receive FIFO buffers)	Available when the common FIFO is configured as a transmit FIFO The interval between messages sent from the FIFO can be adjusted.
Transmit history function	Stores the history information of transmitted messages.	—

Item	RX140 (RSCAN)	RX660 (CANFD-Lite)
Bus-off recovery method	How to recover from the bus-off state can be selected. • Conforming to the ISO 11898-1 specifications • The mode automatically changes to channel halt mode when bus off starts. • The mode automatically changes to channel halt mode when bus off ends. • A program causes a transition to channel halt mode. • A program causes a transition to error active state (forcible return from the bus off state).	How to recover from the bus-off state can be selected. • Normal mode (ISO 11898-1 compliant) • Automatically enters CH_HALT mode when bus off starts. • Automatically enters CH_Halt mode when bus off ends. • Software causes a transition to CH_HALT mode (during bus-off recovery period). • A program causes a transition to error active state.
Timer	Timestamp function (recording of 16-bit timer value indicating time message received)	Transmission and reception timestamp function
Interrupt function	• Global (2 sources) — Global receive FIFO interrupt — Global error interrupt • Channel (3 sources/channel) — Channel transmission interrupt Transmit complete interrupt Transmit abort interrupt Transmit/receive FIFO transmit complete interrupt Transmit history interrupt — Channel error interrupt — Transmit/receive FIFO receive interrupt	Receive FIFO interrupt Global error interrupt Channel transmission interrupt Channel error interrupt Common FIFO reception interrupt Receive message buffer interrupt
Software support	—	Label information is automatically added to received messages.
Test modes	Test function for user evaluation • Listen-only mode • Self test mode 0 (external loopback) • Self test mode 1 (internal loopback) • RAM test (read/write test)	• Basic test mode • Listen-only mode • Self test mode 0 (external loopback mode) • Self test mode 1 (internal loopback mode)
Low power consumption function (RX140) Power down function (RX660)	Ability to specify module stop state	Module start/stop function for each CAN node (CH_SLEEP mode and GL_SLEEP mode) Ability to transition to module stop state
RAM	—	RAMECC protection

Note: 1. This is only available for products that support the CANFD protocol.

Table 2.68 Comparison of CAN Module/CANFD Module Registers

Register	Bit	RX140 (RSCAN)	RX660 (CANFD-Lite)
NBCR	—	—	Nominal bit rate configuration register
CHCR	—	—	Channel control register
CHSR	—	—	Channel status register
CHESR	—	—	Channel error status register
DBCR	—	—	Data bit rate configuration register
FDCFG	—	—	CANFD configuration register
FDCTR	—	—	CANFD control register
FDSTS	—	—	CANFD status register
FDCRC	—	—	CANFDCRC register
GCFG	—	—	Global configuration register
GCR	—	—	Global control register
GSR	—	—	Global status register
GESR	—	—	Global error status register
TISR	—	—	Transmit interrupt status register
TSCR	—	—	Timestamp counter register
AFCR	—	—	Acceptance filter list control register
AFCFG	—	—	Acceptance filter list configuration register
AFLn.IDR	—	—	Acceptance filter list n ID register (n = 0 to 15)
AFLn.MASK	—	—	Acceptance filter list n mask register (n = 0 to 15)
AFLn.PTR0	—	—	Acceptance filter list n pointer register 0 (n = 0 to 15)
AFLn.PTR1	—	—	Acceptance filter list n pointer register 1 (n = 0 to 15)
RMCR	—	—	Receive message buffer configuration register
RMNDR	—	—	Receive message buffer new data register
RFCRn	—	—	Receive FIFOn configuration register (n = 0, 1)
RFSRn	—	—	Receive FIFOn status register (n = 0, 1)
RFPCRn	—	—	Receive FIFOn pointer control register (n = 0, 1)
CFCR0	—	—	Common FIFO 0 configuration register
CFSR0	—	—	Common FIFO 0 status register
CFPCR0	—	—	Common FIFO 0 pointer control register
FESR	—	—	FIFO empty status register
FFSR	—	—	FIFO full status register
FMLSR	—	—	FIFO message lost status register
RFISR	—	—	Receive FIFO interrupt status register
DTCR	—	—	DMA transfer control register
DTSR	—	—	DMA transfer status register
TMCRn	—	—	Transmit message buffer n control register (n = 0 to 3)

Register	Bit	RX140 (RSCAN)	RX660 (CANFD-Lite)
TMSRn	—	—	Transmit message buffer n status register (n = 0 to 3)
TMTRSR0	—	—	Transmit message buffer transmission request status register 0
TMARSR0	—	—	Transmit message buffer transmission abort request status register 0
TMTCSR0	—	—	Transmit message buffer transmission completion status register 0
TMTASR0	—	—	Transmit message buffer transmission abort status register 0
TMIER0	—	—	Transmit message buffer interrupt enable register 0
TQCR0	—	—	Transmit queue 0 configuration register
TQSR0	—	—	Transmit queue 0 status register
TQPCR0	—	—	Transmit queue 0 pointer control register
THCR	—	—	Transmission history configuration register
THSR	—	—	Transmission history status register
THACR0	—	—	Transmission history access register 0
THACR1	—	—	Transmission history access register 1
THPCR	—	—	Transmission history pointer control register
GRCR	—	—	Global reset control register
GTMCR	—	—	Global test mode configuration register
GTMER	—	—	Global test mode enable register
GFDCFG	—	—	Global CANFD configuration register
GTMLKR	—	—	Global test mode lock key register
RTPARk	—	—	RAM test page access register k (k = 0 to 63)
AFIGSR	—	—	Acceptance filter list ignore entry setting register
AFIGER	—	—	Acceptance filter list ignore entry enable register
RMIER	—	—	Receive message buffer interrupt enable register
ECCSR	—	—	ECC control/status register
ECTMR	—	—	ECC test mode register
ECTDR	—	—	ECC decoder test data register
ECEAR	—	—	ECC error address register
CFGL	—	Bit configuration register L	—
CFGH	—	Bit configuration register H	—
CTRL	—	Control register L	—
CTRH	—	Control register H	—
STSL	—	Status register L	—
STSH	—	Status register H	—

Register	Bit	RX140 (RSCAN)	RX660 (CANFD-Lite)
ERFLL	—	Error flag register L	—
ERFLH	—	Error flag register H	—
GCFGL	—	Global configuration register L	—
GCFGH	—	Global configuration register H	—
GCTRL	—	Global control register L	—
GCTRH	—	Global control register H	—
GSTS	—	Global status register	—
GERFLL	—	Global error flag register	—
GTINTSTS	—	Global transmit interrupt status register	—
GTSC	—	Timestamp register	—
GAFLCFG	—	Receive rule number configuration register	—
GAFLIDLj	—	Receive rule entry register jAL (j = 0 to 15)	—
GAFLIDHj	—	Receive rule entry register jAH (j = 0 to 15)	—
GAFLMLj	—	Receive rule entry register jBL (j = 0 to 15)	—
GAFLMHj	—	Receive rule entry register jBH (j = 0 to 15)	—
GAFLPLj	—	Receive rule entry register jCL (j = 0 to 15)	—
GAFLPHj	—	Receive rule entry register jCH (j = 0 to 15)	—
RMNB	—	Receive buffer number configuration register	—
RMND0	—	Receive buffer receive complete flag register	—
RMIDLn	—	Receive buffer register nAL (n = 0 to 15)	—
RMIDHn	—	Receive buffer register nAH (n = 0 to 15)	—
RMTSn	—	Receive buffer register nBL (n = 0 to 15)	—
RMPTRn	—	Receive buffer register nBH (n = 0 to 15)	—
RMDF0n	—	Receive buffer register nCL (n = 0 to 15)	—
RMDF1n	—	Receive buffer register nCH (n = 0 to 15)	—
RMDF2n	—	Receive buffer register nDL (n = 0 to 15)	—
RMDF3n	—	Receive buffer register nDH (n = 0 to 15)	—
RFCCm	—	Receive FIFO control register m (m = 0, 1)	—
RFSTSm	—	Receive FIFO status register m (m = 0, 1)	—
RFPCTRm	—	Receive FIFO pointer control register m (m = 0, 1)	—
RFIDLm	—	Receive FIFO access register mAL (m = 0, 1)	—

Register	Bit	RX140 (RSCAN)	RX660 (CANFD-Lite)
RFIDHm	—	Receive FIFO access register mAH (m = 0, 1)	—
RFTSm	—	Receive FIFO access register mBL (m = 0,1)	—
RFPTRm	—	Receive FIFO access register mBH (m = 0,1)	—
RFDF0m	—	Receive FIFO access register mCL (m = 0,1)	—
RFDF1m	—	Receive FIFO access register mCH (m = 0,1)	—
RFDF2m	—	Receive FIFO access register mDL (m = 0,1)	—
RFDF3m	—	Receive FIFO access register mDH (m = 0,1)	—
CFCCL0	—	Transmit/receive FIFO control register 0L	—
CFCCH0	—	Transmit/receive FIFO control register 0H	—
CFSTS0	—	Transmit/receive FIFO status register 0	—
CFPCTR0	—	Transmit/receive FIFO pointer control register 0	—
CFIDL0	—	Transmit/receive FIFO access register 0AL	—
CFIDH0	—	Transmit/receive FIFO access register 0AH	—
CFTS0	—	Transmit/receive FIFO access register 0BL	—
CFPTR0	—	Transmit/receive FIFO access register 0BH	—
CFDF00	—	Transmit/receive FIFO access register 0CL	—
CFDF10	—	Transmit/receive FIFO access register 0CH	—
CFDF20	—	Transmit/receive FIFO access register 0DL	—
CFDF30	—	Transmit/receive FIFO access register 0DH	—
RFMSTS	—	Receive FIFO message lost status register	—
CFMSTS	—	Transmit/receive FIFO message lost status register	—
RFISTS	—	Receive FIFO interrupt status register	—
CFISTS	—	Transmit/receive FIFO receive interrupt status register	—
TMCp	—	Transmit buffer control register p (p = 0 to 3)	—
TMSTSp	—	Transmit buffer status register p (p = 0 to 3)	—
TMTRSTS	—	Transmit buffer transmit request status register	—
TMTCSTS	—	Transmit buffer transmit complete status register	—

Register	Bit	RX140 (RSCAN)	RX660 (CANFD-Lite)
TMTASTS	—	Transmit buffer transmit abort status register	—
TMIEC	—	Transmit buffer interrupt enable register	—
TMIDLp	—	Transmit buffer register pAL (p = 0 to 3)	—
TMIDHp	—	Transmit buffer register pAH (p = 0 to 3)	—
TMPTRp	—	Transmit buffer register pBH (p = 0 to 3)	—
TMDF0p	—	Transmit buffer register pCL (p = 0 to 3)	—
TMDF1p	—	Transmit buffer register pCH (p = 0 to 3)	—
TMDF2p	—	Transmit buffer register pDL (p = 0 to 3)	—
TMDF3p	—	Transmit buffer register pDH (p = 0 to 3)	—
THLCC0	—	Transmit history buffer control register	—
THLSTS0	—	Transmit history buffer status register	—
THLACC0	—	Transmit history buffer access register	—
THLPCTR0	—	Transmit history buffer pointer control register	—
GRWCR	—	Global RAM window control register	—
GTSTCFG	—	Global test configuration register	—
GTSTCTRL	—	Global test control register	—
GLOCKK	—	Global test protection unlock register	—
RPGACCr	—	RAM test register r (r = 0 to 127)	—

2.24 Serial Peripheral Interface

Table 2.69 is Comparative Overview of Serial Peripheral Interfaces, and Table 2.70 is Comparison of Serial Peripheral Interface Registers.

Table 2.69 Comparative Overview of Serial Peripheral Interfaces

Item	RX140 (RSPIc)	RX660 (RSPId)
Number of channels	1 channel	1 channel
RSPI transfer functions	• Use of MOSI (Master out/slave in), MISO (Master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Communication modes: Full-duplex or simplex (transmit-only) can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK	• Use of MOSI (Master out/slave in), MISO (Master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Communication modes: Full-duplex or simplex (transmit-only) can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK
Data format	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits). • Byte swapping of transmit and receive data is selectable	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits). • Byte swapping of transmit and receive data is selectable • Ability to invert the logic level of transmit/receive data
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from division by 2 to division by 4096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4). — Width at high level: 2 cycles of PCLK — Width at low level: 2 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from division by 2 to division by 4096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4). — Width at high level: 2 cycles of PCLK — Width at low level: 2 cycles of PCLK
Buffer configuration	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection

Item	RX140 (RSPIc)	RX660 (RSPId)
SSL control function	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Range: 1 to 8 RSPCK cycles — Setting unit: 1 RSPCK cycle • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Range: 1 to 8 RSPCK cycles — Setting unit: 1 RSPCK cycle • Controllable wait for next-access SSL output assertion (next-access delay) — Range: 1 to 8 RSPCK cycles — Setting unit: 1 RSPCK cycle • Function for changing SSL polarity	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Range: 1 to 8 RSPCK cycles — Setting unit: 1 RSPCK cycle • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Range: 1 to 8 RSPCK cycles — Setting unit: 1 RSPCK cycle • Controllable wait for next-access SSL output assertion (next-access delay) — Range: 1 to 8 RSPCK cycles — Setting unit: 1 RSPCK cycle • Function for changing SSL polarity
Control in master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function • The delay between data bytes can be shortened during burst transfers.
Interrupt sources	• Interrupt sources — Receive buffer full interrupt — Transmit buffer empty interrupt — Error interrupt (mode fault, overrun, underrun, or parity error) — Idle interrupt	• Interrupt sources — Receive buffer full interrupt — Transmit buffer empty interrupt — Error interrupt (mode fault, overrun, underrun, or parity error) — Idle interrupt — Communication end interrupt

Item	RX140 (RSPIc)	RX660 (RSPId)
Event link function (output)	—	• Interrupt sources — Receive buffer full events — Transmit buffer empty events — Error events (mode fault, overrun, underrun, or parity error) — Idle events — Communication completion events
Other functions	• Function for initializing the RSPI • Loop-back mode function	• Function for initializing the RSPI • Loop-back mode function
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.70 Comparison of Serial Peripheral Interface Registers

Register	Bit	RX140 (RSPIc)	RX660 (RSPId)
SPSR	SPCF	—	Communication completion flag
SPDCR2	DINV	—	Transferred data invert bit
SPCR3	—	—	RSPI control register 3

2.25 CRC Calculator

Table 2.71 is Comparative Overview of CRC Calculators, and Table 2.72 is Comparison of CRC Calculator Registers.

Table 2.71 Comparative Overview of CRC Calculators

Item	RX140 (CRC)	RX660 (CRCA)	
Data size	8 bits	8 bits	32 bits
Data for CRC calculation	CRC codes are generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 32n-bit units (where n is a whole number)
CRC processor unit	8-bit parallel processing	8-bit parallel processing	32-bit parallel processing
CRC generating polynomial	One of three generating polynomials is selectable • 8-bit CRC: — $X^8 + X^2 + X + 1$ • 16-bit CRC: — $X^{16} + X^{15} + X^2 + 1$ — $X^{16} + X^{12} + X^5 + 1$	One of three generating polynomials is selectable • 8-bit CRC: — $X^8 + X^2 + X + 1$ • 16-bit CRC: — $X^{16} + X^{15} + X^2 + 1$ — $X^{16} + X^{12} + X^5 + 1$	One of two generating polynomials is selectable • 32-bit CRC: — $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ — $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$
CRC calculation switching	The order of the bits produced by CRC calculation can be switched for LSB first or MSB first communication	The order of the bits produced by CRC calculation can be switched for LSB first or MSB first communication	
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state	

Table 2.72 Comparison of CRC Calculator Registers

Register	Bit	RX140 (CRC)	RX660 (CRCA)
CRCCR	GPS[1:0]: (RX140) GPS[2:0]: (RX660)	CRC generating polynomial switching bits b1 b0 0 0: No calculation is executed. 0 1: 8-bit CRC ($X^8 + X^2 + X + 1$) 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$) 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$)	CRC generating polynomial switching bits b2 b0 0 0 0: No calculation is executed. 0 0 1: 8-bit CRC ($X^8 + X^2 + X + 1$) 0 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$) 0 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$) 1 0 0: 32-bit CRC ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1: 32-bit CRC ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) 1 1 0: No calculation is executed. 1 1 1: No calculation is executed.
	LMS	CRC calculation switching bit (b2)	CRC calculation switching bit (b6)
CRCDIR	—	CRC data input register Supported access sizes • Byte access	CRC data input register Supported access sizes • Longword access (32-bit CRC selected) • Byte access (16-bit or 8-bit CRC selected)
CRCDOR	—	CRC data output register Supported access sizes • Word access The lower byte (b7 to b0) is used when generating 8-bit CRC.	CRC data output register Supported access sizes • Longword access (32-bit CRC selected) • Word access (16-bit CRC selected) • Byte access (8-bit CRC selected)

2.26 12-Bit A/D Converter

Table 2.73 is Comparative Overview of 12-Bit A/D Converters, and Table 2.74 is Comparison of 12-Bit A/D Converter Registers.

Table 2.73 Comparative Overview of 12-Bit A/D Converters

Item	RX140 (S12ADE)	RX660 (S12ADH)
Number of units	1 unit	1 unit (S12AD)
Input channels	18 channels	24 channels
Extended analog function	Temperature sensor output, internal reference voltage	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	0.88 µs (ADCCR.CCS bit = 0) or 0.67 µs (ADCCR.CCS bit = 1) per channel (when A/D conversion clock (ADCLK) = 48 MHz)	0.9 µs per channel (when A/D conversion clock (ADCLK) = 60 MHz)
A/D conversion clock	Peripheral module clock PCLKB and A/D conversion clock ADCLK can be set so that the frequency division ratio should be one of the following. — PCLK to ADCLK frequency division ratio = 1:1, 1:2, 2:1, 4:1, 8:1 ADCLK is set by using the clock generation circuit.	Peripheral module clock PCLKB and A/D conversion clock ADCLK can be set so that the frequency division ratio should be one of the following. — PCLKB to ADCLK frequency division ratio = 1:1, 1:2, 2:1, 4:1 ADCLK is set by using the clock generation circuit. The A/D conversion clock (ADCLK) can operate at frequencies from a maximum of 60 MHz to a minimum of 8 MHz.
Data register	• 18 registers for analog input • 1 register for A/D-converted data duplication in double trigger mode • 1 register for temperature sensor • 1 register for internal reference voltage • 1 register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • 12-bit accuracy output for the results of A/D conversion • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits*1 in the A/D data registers in A/D-converted value addition mode.	• 24 registers for analog input • 1 register for A/D-converted data duplication in double trigger mode • 2 registers for duplication of A/D conversion data for extended operation in double trigger mode • 1 register for temperature sensor • 1 register for internal reference voltage • 1 register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode.

Item	RX140 (S12ADE)	RX660 (S12ADH)
Data register	• Double trigger mode (selectable in single scan and group scan modes) — The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.	• Double trigger mode (selectable in single scan and group scan modes) — The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers) — A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.
Operation mode	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 18 channels arbitrarily selected. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs of up to 18 channels arbitrarily selected. • Group scan mode: — Analog inputs of up to 18 channels arbitrarily selected, are divided into group A and group B, and A/D conversion of the analog inputs selected on a group basis is performed only once. — The scanning start condition for groups A and B (synchronous trigger) can be independently selected, allowing A/D conversion of each group to be started independently.	• Single scan mode: — A/D conversion is performed only once on arbitrarily selected analog inputs. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: — A/D conversion is performed repeatedly on arbitrarily selected analog inputs. • Group scan mode: — Two (groups A and B) or three (groups A, B, and C) can be selected as the number of groups to be used. (Only the combination of groups A and B can be selected when the number of groups is two.) Arbitrarily selected analog input channels, the temperature sensor output, and the internal reference voltage are divided into two groups (group A and B) or three groups (group A, B, and C), and A/D conversion of the analog input selected on a group basis is performed only once. — The scanning start condition for groups A, B, and C (synchronous trigger) can be independently selected, allowing A/D conversion of each group to be started independently.

Item	RX140 (S12ADE)	RX660 (S12ADH)
Operation mode	• Group scan mode (When group A priority control selected) — At a trigger input on group A during A/D conversion of group B, the A/D conversion of group B is suspended and the A/D conversion of group A is performed. — Restart (re-scan) setting is possible to restart the A/D conversion of group B at the completion of the A/D conversion of group A.	• Group scan mode (When group priority control selected) If a higher-priority group trigger is input during scanning of a lower-priority group, scanning of the lower-priority group stops and scanning of the higher-priority group starts. The priority order is group A (highest) > group B > group C (lowest). Whether or not to restart scanning (rescan) of the lower-priority group after processing for the higher-priority group completes, is selectable. Rescan can also be set to start either from the first selected channel or from the channel on which A/D conversion did not complete.
Conditions for A/D conversion start	• Software trigger • Synchronous trigger Trigger by the multi-function timer pulse unit (MTU) or event link controller (ELC) • Asynchronous trigger A/D conversion can be started by the external trigger ADTRG0# pin.	• Software trigger • Synchronous trigger Trigger by the multi-function timer pulse unit (MTU), 8-bit timer (TMR), or event link controller (ELC) • Asynchronous trigger A/D conversion can be started by the external trigger ADTRG0# pin.
Functions	• Variable sampling state count • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers • Compare function (window A and window B) • 16 ring buffers when the compare function is used	• Variable sampling time (can be set per channel) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers • Compare function (window A and window B) • Ability to specify the channel conversion priority
Interrupt sources	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan.	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI) can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt request (S12ADI) can be generated on completion of double scan.

Item	RX140 (S12ADE)	RX660 (S12ADH)
Interrupt sources	• In group scan mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of group A scan. An A/D scan end interrupt request (GBADI) only for group B can be generated on completion of group B scan.	• In group scan mode, an A/D scan end interrupt request (S12ADI) can be generated on completion of group A scan. An A/D scan end interrupt request (S12GBADI) only for group B can be generated on completion of group B scan. An A/D scan end interrupt request (S12GCADI) for group C can be generated on completion of group C scan.
	• When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of a double scan of group A. An A/D scan end interrupt request (GBADI) only for group B can be generated on completion of group B scan.	• When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI) can be generated on completion of a double scan of group A. A corresponding scan end interrupt request (S12GBADI or S12GCADI) can be generated on completion of a group B or group C scan. • A compare interrupt request (S12CMPAI or S12CMPBI) can be generated upon a match with the comparison condition for the digital compare function.
	• The S12ADI0 and GBADI interrupts can activate the data transfer controller (DTC).	• The S12ADI, S12GBADI, and S12GCADI interrupts can activate the DMA controller (DMAC) and the data transfer controller (DTC).
Event link function	• In group scan mode, an ELC event occurs at the completion of an A/D scan end interrupt of a group other than group B. • In group scan mode, an ELC event occurs at the completion of an A/D scan end interrupt of group B. • An ELC event occurs at the completion of all scans. • Scan can be started by a trigger output by the ELC. • In single scan mode, an ELC event occurs when the event condition of the window compare function is satisfied.	• An event can be output upon completion of all scans. • Scan can be started by a trigger output by the ELC. • In single scan mode, an event can be output when the compare function window condition is met.
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Note: 1. The number of extended bits at the time of addition differs depending on the number of times of addition.
2-bit extension: 1-time to 4-time conversion (0-time to 3-time addition)
4-bit extension: 16-time conversion (15-time addition)

Table 2.74 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX140 (S12ADE)	RX660 (S12ADH)
ADDRy	—	A/D data register y (y = 0 to 8, 16 to 21, 24 to 26)	A/D data register y (y = 0 to 23)
ADDBLDRA	—	—	A/D data duplication register A
ADDBLDRB	—	—	A/D data duplication register B
ADCSR	ADHSC	A/D conversion operation select bit	—
ADANSA0	ANSA009 to ANSA015	—	A/D conversion channel select bits
ADANSA1	ANSA106, ANSA107	—	A/D conversion channel select bits
	ANSA108 to ANSA110	A/D conversion channel select bits	—
ADANSB0	ANSB009 to ANSB015	—	A/D conversion channel select bits
ADANSB1	ANSB106, ANSB107	—	A/D conversion channel select bits
	ANSB108 to ANSB110	A/D conversion channel select bits	—
ADANSC0	—	—	A/D channel select register C0
ADANSC1	—	—	A/D channel select register C1
ADSCSn	—	—	A/D channel conversion order setting register n (n = 0 to 23)
ADADS0	ADS009 to ADS015	—	A/D-converted value addition/average channel select bits
ADADS1	ADS106, ADS107	—	A/D-converted value addition/average channel select bits
	ADS108 to ADS110	A/D-converted value addition/average channel select bits	—
ADEXICR	TSSB	—	Group B temperature sensor output A/D conversion select bit
	OCSB	—	Group B internal reference voltage A/D conversion select bit
ADGCEXCR	—	—	A/D group C extended input control register
ADGCTRGR	—	—	A/D group C trigger select register
ADSSTRn	—	A/D sampling state register n (n = 0 to 8, L, T, O)	A/D sampling state register n (n = 0 to 15, L, T, O)
		Initial value after a reset differs.	

Register	Bit	RX140 (S12ADE)	RX660 (S12ADH)
ADDISCR	ADNDIS[4:0]	A/D disconnection detection assist setting bits b4 ADNDIS[4]: Discharge or precharge selection 0: Discharge 1: Precharge b3-b0 ADNDIS[3:0]: Discharge or precharge period	A/D disconnection detection assist setting bits b4 ADNDIS[4]: 0: Discharge 1: Precharge The discharge/precharge period is specified by the number of ADCLK clock cycles. b3 b0 0 0 0 0: No charging (disconnection detection assist function disabled) 0 0 1 1: Charge period of 3 clock cycles 0 1 1 0: Charge period of 6 clock cycles 1 0 0 1: Charge period of 9 clock cycles 1 1 0 0: Charge period of 12 clock cycles 1 1 1 1: Charge period of 15 clock cycles Settings other than the above are prohibited.
ADELCCR	ELCC[1:0] (RX140) ELCC[2:0] (RX660)	Event link control bits b1 b0 0 0: In group scan mode, an event occurs at the completion of an A/D scan end interrupt of a group other than group B. 0 1: In group scan mode, an event occurs at the completion of an A/D scan end interrupt of group B. 1 x: An event occurs at the completion of all scans.	Event link control bits b2 b0 0 0 0: An event is output upon completion of the scan of group A. 0 0 1: An event is output upon completion of the scan of group B. 0 1 0: An event is output upon completion of the scan of group A, group B, or group C. 1 0 0: An event is output upon completion of the scan of group C. Settings other than the above are prohibited.
ADGSPCR	PGS	Group A priority control setting bit 0: Priority control of group A is not performed. 1: Priority control of group A is performed.	Group priority control setting bit 0: Priority control of a group is not performed. 1: Priority control of a group is performed.

Register	Bit	RX140 (S12ADE)	RX660 (S12ADH)
ADGSPCR	GBRSCN	Group B restart setting bit (Effective only when PGS = 1. This bit is reserved when PGS = 0.) 0: In group A priority control, the A/D conversion of group B is not restarted after suspension. 1: In group A priority control, the A/D conversion of group B is restarted after suspension.	Low priority group restart setting bit (Effective only when PGS = 1. This bit is reserved when PGS = 0.) 0: Restart is not made for the group suspended by group priority control. 1: Restart is made for the group suspended by group priority control.
	LGRRS	—	Restart channel select bit
	GBRP	Single scan consecutive start setting bit for group B (Effective only when PGS = 1. This bit is reserved when PGS = 0.) 0: Single scan consecutive operation is not made for group B. 1: Single scan consecutive operation is started for group B.	Single scan consecutive start setting bit (Effective only when PGS = 1. This bit is reserved when PGS = 0.) 0: Single scan consecutive operation is not made 1: Single scan consecutive operation is started for the group of the lowest priority.
ADCMPCR	CMPAB[1:0]	Window A/B complex conditions setting bits b1 b0 0 0: S12ADWMELC is output when window A comparison conditions are met OR window B comparison conditions are met. S12ADWUMELC is output in other cases. 0 1: S12ADWMELC is output when window A comparison conditions are met EXOR window B comparison conditions are met. S12ADWUMELC is output in other cases. 1 0: S12ADWMELC is output when window A comparison conditions are met AND window B comparison conditions are met. S12ADWUMELC is output in other cases. 1 1: Setting prohibited.	Window A/B complex conditions setting bits b1 b0 0 0: Window A comparison conditions are met OR window B comparison conditions are met. 0 1: Window A comparison conditions are met XOR window B comparison conditions are met. 1 0: Window A comparison conditions are met AND window B comparison conditions are met. 1 1: Setting prohibited

Register	Bit	RX140 (S12ADE)	RX660 (S12ADH)
ADCMPCR	CMPBE	Compare window B operation enable bit 0: Compare window B operation is disabled, and S12ADWMELC and S12ADWUMELC outputs are disabled. 1: Compare window B operation is enabled.	Compare window B operation enable bit 0: Compare window B operation is disabled. 1: Compare window B operation is enabled.
	CMPAE	Compare window A operation enable bit 0: Compare window A operation is disabled, and S12ADWMELC and S12ADWUMELC outputs are disabled. 1: Compare window A operation is enabled.	Compare window A operation enable bit 0: Compare window A operation is disabled. 1: Compare window A operation is enabled.
	CMPBIE	—	Compare B interrupt enable bit
	CMPAIE	—	Compare A interrupt enable bit
ADCMPANSR0	CMPCHA009 to CMPCHA015	—	Compare window A channel select bits
ADCMPANSR1	CMPCHA106, CMPCHA107	—	Compare window A channel select bits
	CMPCHA108 to CMPCHA110	Compare window A channel select bits	—
ADCMPLR0	CMPLCHA009 to CMPCHA015	—	Compare window A compare condition select bit
ADCMPLR1	CMPLCHA106, CMPLCHA107	—	Compare window A compare condition select bit
	CMPLCHA108 to CMPLCHA110	Compare window A compare condition select bit	—
ADCMPLER	CMPLTSA (RX140) CMPLTS (RX660)	Compare window A temperature sensor output compare condition select bit	Compare window A temperature sensor output compare condition select bit
ADCMPLER	CMPLOCA (RX140) CMPLOC (RX660)	Compare window A internal reference voltage compare condition select bit	Compare window A internal reference voltage compare condition select bit
ADCMPSR0	CMPSTCHA009 to CMPSTCHA015	—	Compare window A flag
ADCMPSR1	CMPSTCHA106, CMPSTCHA107	—	Compare window A flag
	CMPSTCHA108 to CMPSTCHA110	Compare window A flag	—
ADCMPSER	CMPSTTSA (RX140) CMPFTS (RX660)	Compare window A temperature sensor output compare flag	Compare window A temperature sensor output compare flag

Register	Bit	RX140 (S12ADE)	RX660 (S12ADH)
ADCMPSER	CMPSTOCA (RX140) CMPFOC (RX660)	Compare window A internal reference voltage compare flag	Compare window A internal reference voltage compare flag
ADHVREFCNT	—	A/D high/low reference voltage control register	—
ADCMPBNSR	CMPCHB[5:0]	Compare window B channel select bits Selects a channel to be compared by the compare window B condition. b5 b0 0 0 0 0 0 0: AN000 0 0 0 0 0 1: AN001 0 0 0 0 1 0: AN002 : : 0 0 0 1 1 0: AN006 0 0 0 1 1 1: AN007 0 1 0 0 0 0: AN016 0 1 0 0 0 1: AN017 : : 0 1 0 1 0 1: AN021 0 1 1 0 0 0: AN024 0 1 1 0 0 1: AN025 0 1 1 0 1 0: AN026 1 0 0 0 0 0: Temperature sensor 1 0 0 0 0 1: Internal reference voltage Settings other than the above are prohibited.	Compare window B channel select bits Selects a channel to be compared by the compare window B condition. b5 b0 0 0 0 0 0 0: AN000 0 0 0 0 0 1: AN001 0 0 0 0 1 0: AN002 : : 0 1 0 1 1 0: AN022 0 1 0 1 1 1: AN023 1 0 0 0 0 0: Temperature sensor 1 0 0 0 0 1: Internal reference voltage Settings other than the above are prohibited.
ADBUFn	—	A/D data storage buffer register n (n = 0 to 15)	—
ADBUFEN	—	A/D data storage buffer enable register	—
ADBUFPTR	—	A/D data storage buffer pointer register	—
ADCCR	—	A/D conversion cycle control register	—
ADVMONCR	—	—	A/D internal reference voltage monitoring circuit enable register
ADVMONO	—	—	A/D internal reference voltage monitoring circuit output enable register
ADVREFCR	—	—	A/D reference voltage control register

2.27 D/A Converter and 12-Bit D/A Converter

Table 2.75 is Comparative Overview of D/A Converters and 12-Bit D/A Converters, and Table 2.76 is Register Comparison of D/A Converters and 12-Bit D/A Converters.

Table 2.75 Comparative Overview of D/A Converters and 12-Bit D/A Converters

Item	RX140 (DAa)	RX660 (R12DAb)
Resolution	8 bits	12 bits
Output channels	2 channels	2 channels
Measure against interference between analog modules	Measure against interference between D/A and A/D converters: D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable signal output by the 12-bit A/D converter. This reduces degradation of A/D conversion accuracy due to interference by controlling the timing of the 8-bit D/A converter inrush current with the enable signal.	Measure against interference between D/A and A/D converters: D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable signal output by the 12-bit A/D converter. This reduces degradation of A/D conversion accuracy due to interference by controlling the timing of the 12-bit D/A converter inrush current with the enable signal.
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state
Event link function (input)	Ability to start D/A conversion on channel 0 when an event signal is input	Ability to start D/A conversion on channel 0 when an event signal is input
Output destination selection	—	Output to external pins and to comparator C can be controlled independently.

Table 2.76 Register Comparison of D/A Converters and 12-Bit D/A Converters

Register	Bit	RX140 (DAa)	RX660 (R12DAb)
DACR	DAE	—	D/A enable bit
DADSELR	—	—	D/A destination select register

2.28 Comparator B/Comparator C

Table 2.77 is Comparative Overview of Comparator B/C Modules, and Table 2.78 is Comparison of Comparator B and Comparator C Registers.

Table 2.77 Comparative Overview of Comparator B/C Modules

Item	RX140 (CMPBa)	RX660 (CMPC)
Number of channels	2 channels (comparator B0, comparator B1)	4 channels (comparator C0 to comparator C3)
Analog input voltage	• Input voltage to the CMPBn pin (n=0, 1)	• Input voltage from the CMPCn0 pin (n = channel number)
Reference input voltage	Input voltage to the CVREFBn pin (n = 0, 1) or internal reference voltage	Input voltage from the CVREFC0 to CVREFC3 pins, output voltage from on-chip D/A converter 0 or on-chip D/A converter 1
Comparison result	Read from the CPBFLG.CPBnOUT flag The comparison result can be output to the CMPOBn pins	The comparison result can be output externally.
Digital filter function	Presence/Absence of a digital filter can be set, and a sampling frequency can be selected.	• One of three sampling periods can be selected. • The filter function can also be disabled. • A noise-filtered signal can be used to generate interrupt request output and event output to the ELC, and comparison results can be read from registers.
Interrupt request signal	• When the comparison result of comparator B0 changes • When the comparison result of comparator B1 changes	• An interrupt request is generated upon detection of a valid edge of the comparison result. • The rising edge, falling edge, or both edges of the comparison result can be selected as valid edges.
Occurrence timing of event to ELC	• When the comparison result of comparator B0 changes • When the comparison result of comparator B1 changes	—
Optional functions	• Window function The window function (low-voltage reference (VRFL) < CMPBn < VRFH) can be enabled/disabled. • Reference input voltage The CVREFBn pin input or the internal reference voltage (generated internally) can be selected. • High-speed mode or low-speed mode can be selected for comparator B response speed.	—
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Table 2.78 Comparison of Comparator B and Comparator C Registers

Register	Bit	RX140 (CMPBa)	RX660 (CMPC)
CPBCNT1	—	Comparator B control register 1	—
CPBCNT2	—	Comparator B control register 2	
CPBFLG	—	Comparator B flag register	—
CPBINT	—	Comparator B interrupt control register	—
CPBF	—	Comparator B filter select register	—
CPBMD	—	Comparator B mode select register	—
CPBREF	—	Comparator B reference input voltage select register	—
CPBOCR	—	Comparator B output control register	—
CMPCTL	—	—	Comparator control register
CMPSEL0	—	—	Comparator input switch register
CMPSEL1	—	—	Comparator reference voltage select register
CMPMON	—	—	Comparator output monitor register
CMPIOC	—	—	Comparator external output enable register

2.29 Data Operation Circuit

Table 2.79 is Comparative Overview of Data Operation Circuits, and Table 2.80 is Comparison of Data Operation Circuit Registers.

Table 2.79 Comparative Overview of Data Operation Circuits

Item	RX140 (DOC)	RX660 (DOCA)
Data operation functions	16-bit data comparison, addition, and subtraction	• Comparison of 16- or 32-bit data (match/mismatch, greater/less, in/out of range) • Addition or subtraction of 16- or 32-bit data
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state
Interrupt	• When data comparison result matches detection condition • The result of data addition is greater than FFFFh (overflow) • The result of data subtraction is less than 0000h (underflow)	• When data comparison result matches detection condition • When data addition result is greater than FFFFh (when DOCR.DOPSZ = 0) or FFFF FFFFh (when DOCR.DOPSZ = 1) (overflow) • When data subtraction result is less than 0000h (when DOCR.DOPSZ = 0) or 0000 0000h (when DOCR.DOPSZ = 1) (underflow)
Event link function (output)	• When data comparison result matches detection condition • The result of data addition is greater than FFFFh (overflow) • The result of data subtraction is less than 0000h (underflow)	• When data comparison result matches detection condition • When data addition result is greater than FFFFh (when DOCR.DOPSZ = 0) or FFFF FFFFh (when DOCR.DOPSZ = 1) (overflow) • When data subtraction result is less than 0000h (when DOCR.DOPSZ = 0) or 0000 0000h (when DOCR.DOPSZ = 1) (underflow)

Table 2.80 Comparison of Data Operation Circuit Registers

Register	Bit	RX140 (DOC)	RX660 (DOCA)
DOCR	DOPSZ	—	Data operation size select bit
	DCSEL (RX140) DCSEL[2:0] (RX660)	Detection condition select bit 0: Data mismatches are detected. 1: Data matches are detected.	Detection condition select bits b6 b4 0 0 0: Mismatch (DODIR ≠ DODSR0) 0 0 1: Match (DODIR = DODSR0) 0 1 0: Less (DODIR < DODSR0) 0 1 1: Greater (DODIR > DODSR0) 1 0 0: In range (DODSR0 < DODIR < DODSR1) 1 0 1: Out of range (DODIR < DODSR0, DODSR1 < DODIR) Other than above: Setting prohibited.
	DOPCIE	Data operation circuit interrupt enable bit (b4)	Data operation circuit interrupt enable bit (b7)
	DOPCF	Data operation circuit flag	—
	DOPCFCL	DOPCF clear bit	—
DOSR	—	—	DOC status register
DOSCR	—	—	DOC status clear register
DODIR	—	DOC data input register	DOC data input register
		16-bit read/write register	32-bit read/write register
DODSR (RX140) DODSR0/ DODSR1 (RX660)	—	DOC data setting register	DOC data setting register 0 DOC data setting register 1
		16-bit read/write register	32-bit read/write register

2.30 RAM

Table 2.81 is Comparative Overview of RAM.

Table 2.81 Comparative Overview of RAM

Item	RX140	RX660
RAM capacity	Max. 64 KB	128 KB
RAM address	• RAM capacity: 64 KB RAM0: 0000 0000h to 0000 FFFFh • RAM capacity: 32 KB RAM0: 0000 0000h to 0000 7FFFh • RAM capacity: 16 KB RAM0: 0000 0000h to 0000 3FFFh	• RAM: 0000 0000h to 0001 FFFFh
Memory buses	Memory bus 1	Memory bus 1
Access	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing*1. • The RAM can be enabled or disabled.
Data retention function	—	The data retention function is not available for deep software standby mode.
Low power consumption function	Ability to transition to module stop state	Ability to specify module stop state
Error checking function	—	• Parity check: Detection of 1-bit errors • A non-maskable interrupt or an interrupt is generated when an error occurs.

Note: 1. For access that crosses a 8-byte boundary, the number of cycles is doubled.

Table 2.82 Comparison of RAM Registers

Register	Bit	RX140	RX660
RAMMODE	—	—	RAM operating mode control register
RAMSTS	—	—	RAM error status register
RAMECAD	—	—	RAM error address capture register
RAMPRCR	—	—	RAM protection register

2.31 Flash Memory

Table 2.83 is Comparative Overview of Flash Memories, and Table 2.84 is Comparison of Flash Memory Registers.

Table 2.83 Comparative Overview of Flash Memories

Item	RX140	RX660	
	—	Code flash memory	Data flash memory
Memory space	• User area: Max. 256 KB • Data area: 8 KB • Extra area: Startup area information, access window information, and unique IDs are stored	• User area: Max. 1 MB • User boot area: 32 KB	• Data area: 32 KB
Operating clock	• FCLK: 1 to 48 MHz (in ROM P/E mode, in E2 DataFlash P/E mode) 1 to 48 MHz (in E2 DataFlash mode) • HOCO clock: 24 MHz, 32 MHz, or 48 MHz (in ROM P/E mode, in E2 DataFlash P/E mode)	• FCLK: 4 MHz to 60 MHz (when code flash memory P/E) • HOCO clock: 16 MHz, 18 MHz, or 20 MHz	• FCLK: 4 MHz to 60 MHz (when data flash memory P/E) 60 MHz (max.) (for reading from the data flash memory) • HOCO clock: 16 MHz, 18 MHz, or 20 MHz
Address	• Products with capacity of 256 KB: — FFFC 0000h to FFFF FFFFh • Products with capacity of 128 KB: — FFFE 0000h to FFFF FFFFh • Data area — 0100 0000h to 0010 1FFFh	• 1 MB — FFF0 0000h to FFFF FFFFh • 512 KB — FFF8 0000h to FFFF FFFFh • Data flash memory — 0100 0000h to 0100 7FFFh	

Item	RX140	RX660	
	—	Code flash memory	Data flash memory
Software commands	• The following software commands are implemented: — Program, blank check, block erasure, and all-block erasure • The following commands are implemented for programs in the extra area. — Start-up area information program — Access window protection — Access window information program	• FACI command — Program (user area) 256-byte program — Program (data area) 4-byte program — Block erase — P/E suspend — P/E resume — Status clear — Forced stop — Blank check — Configuration setting — Lock bit program — Lock bit read	
Read cycle	One cycle	One cycle	16-bit or 8-bit read access requires 8 FCLK clock cycles.
Value after erasure	• ROM: FFh • E2 DataFlash: FFh	FFh	Undefined
Programming/ erasing method	—	• FACI commands specified in the FACI command issuing area (007E 0000h) can be used to program and erase the code flash memory and data flash memory. • A flash memory programmer can be used to program and erase the flash memory via a serial interface (serial programming). • A user program can be used to program and erase the flash memory (self-programming).	
Interrupt	Interrupt (FRDYI) occurs at the completion of the software command or forcible termination processing	• Data flash memory access violation interrupt • Command lock interrupt • Code flash memory access violation interrupt • Flash ready interrupt	
Security function	—	Protects against illicit tampering with or reading of data in flash memory.	
Trusted Memory (TM) function	—	Protects against illicit reading of code flash memory block 8 or block 9.	
Units of programming and erasure	Programming the code flash (4 bytes) Programming the E2 DataFlash (1byte) Erasure of both types of flash memory is in block units.	Programming the user area and user boot area: 256 bytes Erasure of user area: Block units	Programming the data area: 4 bytes Erasure of data area: Block units
Other functions	Interrupts can be accepted during self-programming.	Interrupts can be accepted during self-programming.	

Item	RX140	RX660	
	—	Code flash memory	Data flash memory
On-board programming (serial programming and self-programming)	• Boot mode (SCI interface) — Channel 1 of the serial communications interface (SCI1) is used for asynchronous serial communication. — The user area and data area are programmable. • Boot mode (FINE interface) — FINE is used. — The user area and data area are programmable. • Self-programming (single-chip mode) — The user area and data area are programmable using a flash programming routine in a user program.	• Programming/erasure in boot mode (SCI interface) — The asynchronous serial interface (SCI1) is used. — The communication speed is adjusted automatically. — Programming/erasure is possible in user boot area. • Programming/erasure in boot mode (FINE interface) — FINE is used. • Programming/erasure in user boot mode — User's own boot programs can be created. • Programming/erasure in single-chip mode — Programming or erasure by a routine within a user program for writing to the code flash memory or data flash memory is possible.	
Off-board programming	The user area and data area are rewritable using a flash programmer compatible with this MCU.	Programming/erasure of the user area and user boot area is possible using a parallel programmer	Programming/erasure of the data area is not possible using a parallel programmer.
ID code protection	• In boot mode, connection to a serial programmer can be enabled or disabled using an ID code. • When connected to an on-chip debugging emulator, control is possible by an ID code. • When connected to a parallel programmer, control is possible by a ROM code.	—	—
Start-up program protection function	This function enables the safe rewriting of block 0 to block 7.	—	—
Protection function	In self-programming, rewrite can be enabled for a specified area in the user area and disabled for other areas.	Protects against erroneous programming of the flash memory.	
Background operation (BGO) function	• Programs in the ROM area can run while programing/erasure is executed in the E2 DataFlash.	Reading from the user area is possible during programming/erasure in the data area.	
Unique ID	A unique 16-byte ID code is provided for each MCU.	A unique 12-byte ID code is provided for each MCU.	

Table 2.84 Comparison of Flash Memory Registers

Register	Bit	RX140	RX660
DFLCTL	—	E2 DataFlash control register	—
MEMWAITR	—	Memory wait cycle setting register	
DFLWAITR	—	Data flash wait cycle setting register	
FPR	—	Protection unlock register	—
FPSR	—	Protection unlock status register	—
FPMCR	—	Flash P/E mode control register	—
FISR	—	Flash initial setting register	—
FRESETR	—	Flash reset register	—

Register	Bit	RX140	RX660
FASR	—	Flash area select register	—
FCR	—	Flash control register	—
FEXCR	—	Flash extra area control register	—
FSARH	—	Flash processing start address register H	—
FSARL	—	Flash processing start address register L	—
FEARH	—	Flash processing end address register H	—
FEARL	—	Flash processing end address register L	—
FWBn	—	Flash write buffer n register (n = 0 to 3)	—
FSTATR0	—	Flash status register 0	—
FSTATR1	—	Flash status register 1	—
FEAMH	—	Flash error address monitor register H	—
FEAMH	—	Flash error address monitor register H	—
FEAML	—	Flash error address monitor register L	—
FSCMR	—	Flash start-up setting monitor register	—
FAWSMR	—	Flash access window start address monitor register	—
FAWEMR	—	Flash access window end address monitor register	—
FWEPROR	—	—	Flash P/E protect register
FASTAT	—	—	Flash access status register
FAEINT	—	—	Flash access error interrupt enable register
FRDYIE	—	—	Flash ready interrupt enable register
FSADDR	—	—	FACI command start address register
FEADDR	—	—	FACI command end address register
FSTATR	—	—	Flash status register
FPROTR	—	—	Flash protect register
FSUINITR	—	—	Flash sequencer set-up initialization register
FLKSTAT	—	—	Lock bit status register
FCMDR	—	—	FACI command register
FPESTAT	—	—	Flash P/E status register
FBCCNT	—	—	Data flash blank check control register
FBCSTAT	—	—	Data flash blank check status register
FPSADDR	—	—	Data flash programming start address register
FCPSR	—	—	Flash sequencer processing switching register
FPCKAR	—	—	Flash sequencer processing clock frequency notification register
UIDRn	—	Unique ID register n (n = 0 to 3)	Unique ID register n (n = 0 to 2)

2.32 Package

As indicated in Table 2.85, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage.

Table 2.85 Packages

Package Type	RENESASCode	
	RX140	RX660
144-pin LFQFP	×	○
100-pin LFQFP	×	○
64-pin LQFP	○	×
48-pin HWQFN	○	×
32-pin LQFP	○	×
32-pin HWQFN	○	×

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by **blue text**. Items that exists on both groups with different specifications are indicated by **red text**. Black text indicates there is no differences in the item's specifications between groups.

3.1 80-Pin Package

Table 3.1 is Comparative Listing of 80-Pin Package Pin Functions.

Table 3.1 Comparative Listing of 80-Pin Package Pin Functions

80-Pin LFQFP	RX140	RX660
1	P06	P06
2	P03/DA0	P03/IRQ11/DA0
3	P04	P04
4	VCL	VCL
5	PJ1/MTIOC3A	PJ1/MTIOC3A
6	MD/PG7/FINED	MD/FINED/PN6
7	XCIN/PH7	XCIN*3/PH7*4
8	XCOUT/PH6	XCOUT*3/PH6*4
9	RES#	RES#
10	XTAL/P37/IRQ4	XTAL/P37/IRQ4
11	VSS	VSS
12	EXTAL/P36/IRQ2	EXTAL/P36/IRQ5
13	VCC	VCC
14	P35/NMI	P35/NMI
15	P34/MTIOC0A/TMCI3/POE2#/SCK6/IRQ4	P34/MTIOC0A/TMCI3/POE10#/SCK6/SCK0/IRQ4
16	P32/MTIOC0C/TMO3/TXD6/SMOSI6/SSDA6/TS0/IRQ2/RTCOUT	P32/MTIOC0C/TMO3/RTCIC2*5/RTCOUT*5/POE0#/POE10#/TXD6/SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/CTX0-A/IRQ2-DS
17	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/TS1/IRQ1	P31/MTIOC4D/TMCI2/RTCIC1*5/CTS1#/RTS1#/SS1#/IRQ1-DS
18	P30/MTIOC4B/TMRI3/POE8#/RXD1/SMISO1/SSCL1/TS2/IRQ0	P30/MTIOC4B/TMRI3/RTCIC0*5/POE8#/RXD1/SMISO1/SSCL1/IRQ0-DS/COMP3
19	P27/MTIOC2B/TMCI3/SCK1/TS3	P27/MTIOC2B/TMCI3/SCK1/IRQ7/CVREFC3
20	P26/MTIOC2A/TMO1/LPTO/TXD1/SMOSI1/SSDA1/TS4	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/IRQ6/CMPC30
21	P21/MTIOC1B/TMCI0	P21/MTIOC1B/TMCI0/MTIOC4A/RXD0/SMISO0/SSCL0/IRQ9
22	P20/MTIOC1A/TMRI0	P20/MTIOC1A/TMRI0/TXD0/SMOSI0/SSDA0/IRQ8
23	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/SCK1/MISOA/SDA0/IRQ7	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/MTIOC4B/SCK1/TXD3/SMOSI3/SSDA3/MISOA-C/SDA2/IRQ7/COMP2
24	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/SMOSI1/SSDA1/MOSIA/SCL0/IRQ6/RTCOUT/ADTRG0#	P16/MTIOC3C/MTIOC3D/TMO2/RTCOUT*5/TXD1/SMOSI1/SSDA1/RXD3/SMISO3/SSCL3/MOSIA-C/SCL2/IRQ6/ADTRG0#
25	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/SMISO1/SSCL1/CRXD0/TS5/IRQ5	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/SMISO1/SSCL1/SCK3/CRX0-C/IRQ5/CMPC20

80-Pin LFQFP	RX140	RX660
26	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/CTXD0/TS6/IRQ4	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/CTX0-C/IRQ4/CVREFC2
27	P13/MTIOC0B/TMO3/SDA0/IRQ3	P13/MTIOC0B/TMO3/SDA0/IRQ3
28	P12/TMCI1/SCL0/IRQ2	P12/MTIC5U/TMCI1/SCL0/IRQ2
29	PH3/MTIOC4D/TMCI0/TS7	PH3/MTIOC4D/TMCI0
30	PH2/MTIOC4C/TMRI0/TS8/IRQ1	PH2/MTIOC4C/TMRI0/TOC1/IRQ1
31	PH1/MTIOC3D/TMO0/TS9/IRQ0	PH1/MTIOC3D/TMO0/TIC1/IRQ0/ADST0
32	PH0/MTIOC3B/TS10/CACREF	PH0/MTIOC3B/CACREF/ADTRG0#
33	P55/MTIOC4A/MTIOC4D/TMO3/CRXD0/ TS11	P55/MTIOC4D/MTIOC4A/TMO3/CRX0-D/ IRQ10
34	P54/MTIOC4B/TMCI1/CTXD0/TS12	P54/MTIOC4B/TMCI1/CTX0-D/IRQ4
35	PC7/MTCLKB/MTIOC3A/TMO2/LPTO/ MISOA/TXD8/SMOSI8/SSDA8/TS13/ CACREF	UB/PC7/MTIOC3A/MTCLKB/TMO2/ CACREF/TOC0/TXD8/SMOSI8/SSDA8/ SMOSI10/SSDA10/TXD10/TXD010-C/ SMOSI010-C/SSDA010-C/MISOA-A/IRQ14
36	PC6/MTIOC3C/MTCLKA/TMCI2/MOSIA/ RXD8/SMISO8/SSCL8/TS14	PC6/MTIOC3C/MTCLKA/TMCI2/TIC0/RXD8/ SMISO8/SSCL8/SMISO10/SSCL10/RXD10/ RXD010-C/SMISO010-C/SSCL010-C/ MOSIA-A/IRQ13
37	PC5/MTIOC0C/MTIOC3B/MTCLKD/TMRI2/ RSPCKA/SCK8/TS15	PC5/MTIOC3B/MTCLKD/TMRI2/MTIOC0C/ SCK8/SCK10/SCK010-C/RSPCKA-A/PMC0/ IRQ5
38	PC4/MTIOC0A/MTIOC3D/MTCLKC/TMCI1/ POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0/ TSCAP	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/ MTIOC0A/SCK5/CTS8#/RTS8#/SS8#/ SS10#/CTS10#/RTS10#/CTS010#-B/ RTS010#-B/SS010#-B/DE010-B/SSLA0-A/ PMC0/IRQ12
39	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5/TS16	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5/ PMC0/IRQ11
40	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/ SSLA3/TS17	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/ TXDB011-A/SSLA3-A/IRQ10
41	PB7/PC1*2/MTIOC3B/TXD9/SMOSI9/ SSDA9/TS18	PB7/MTIOC3B/TXD9/SMOSI9/SSDA9/ SMOSI11/SSDA11/TXD11/TXD011-B/ SMOSI011-B/SSDA011-B/IRQ15
42	PB6/PC0*2/MTIOC3D/RXD9/SMISO9/ SSCL9/TS19	PB6/MTIOC3D/RXD9/SMISO9/SSCL9/ SMISO11/SSCL11/RXD11/RXD011-B/ SMISO011-B/SSCL011-B/IRQ6
43	PB5/MTIOC2A/MTIOC1B/TMRI1/POE1#/ SCK9/TS20	PB5/MTIOC2A/MTIOC1B/TMRI1/POE4#/ TOC2/SCK9/SCK11/SCK011-B/IRQ13
44	PB4/CTS9#/RTS9#/SS9#/TS21	PB4/CTS9#/RTS9#/SS9#/SS11#/CTS11#/ RTS11#/CTS011#-B/RTS011#-B/SS011#-B/ DE011-B/IRQ4
45	PB3/MTIOC0A/MTIOC4A/TMO0/POE3#/ LPTO/SCK6/TS22	PB3/MTIOC0A/MTIOC4A/TMO0/POE11#/ TIC2/SCK4/SCK6/PMC0/IRQ3
46	PB2/CTS6#/RTS6#/SS6#/TS23	PB2/CTS4#/RTS4#/SS4#/CTS6#/RTS6#/ SS6#/IRQ2
47	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD6/ SMOSI6/SSDA6/TS24/IRQ4/CMPOB1	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD4/ SMOSI4/SSDA4/TXD6/SMOSI6/SSDA6/ IRQ4-DS/COMP1
48	VCC	VCC
49	PB0/MTIOC3D/MTIC5W/RXD6/SMISO6/ SSCL6/RSPCKA/TS25	PB0/MTIC5W/MTIOC3D/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/RSPCKA-C/ IRQ12

80-Pin LFQFP	RX140	RX660
50	VSS	VSS
51	PA6/MTIOC3D/MTIC5V/MTCLKB/TMCI3/ POE2#/CTS5#/RTS5#/SS5#/MOSIA/TS26	PA6/MTIC5V/MTCLKB/TMCI3/POE10#/ MTIOC3D/MTIOC6B/CTS5#/RTS5#/SS5#/ CTS12#/RTS12#/SS12#/MOSIA-B/IRQ14
52	PA5/RSPCKA/TS27	PA5/MTIOC6B/RSPCKA-B/IRQ5
53	PA4/MTIOC4C/MTIC5U/MTCLKA/TMRI0/ TXD5/SMOSI5/SSDA5/SSLA0/TS28/IRQ5/ CVREFB1	PA4/MTIC5U/MTCLKA/TMRI0/MTIOC4C/ MTIOC7C/TXD5/SMOSI5/SSDA5/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLA0-B/IRQ5-DS/CVREFC1/ADST0
54	PA3/MTIOC0D/MTIOC4D/MTIC5V/MTCLKD/ RXD5/SMISO5/SSCL5/TS29/IRQ6/CMPB1	PA3/MTIOC0D/MTCLKD/MTIC5V/MTIOC4D/ RXD5/SMISO5/SSCL5/IRQ6-DS/CMPC10
55	PA2/RXD5/SMISO5/SSCL5/SSLA3/TS30	PA2/MTIOC7A/RXD5/SMISO5/SSCL5/ RXD12/SMISO12/SSCL12/RXDX12/ SSLA3-B/IRQ10
56	PA1/MTIOC0B/MTIOC3B/MTCLKC/SCK5/ SSLA2/TS31	PA1/MTIOC0B/MTCLKC/MTIOC7B/ MTIOC3B/SCK5/SCK12/SSLA2-B/IRQ11/ ADTRG0#
57	PA0/MTIOC4A/SSLA1/TS32/CACREF	PA0/MTIOC4A/CACREF/MTIOC6D/ SSLA1-B/IRQ0
58	PE5/MTIOC4C/MTIOC2B/IRQ5/AN021/ CMPOB0	PE5/MTIOC4C/MTIOC2B/IRQ5/AN013/ COMP0
59	PE4/MTIOC4D/MTIOC1A/MTIOC4A/TS33/ AN020/CMPA2/CLKOUT	PE4/MTIOC4D/MTIOC1A/MTIOC4A/ MTIOC7D/IRQ12/AN012
60	PE3/MTIOC1B/MTIOC4B/POE8#/CTS12#/ RTS12#/SS12#/TS34/AN019/CLKOUT	PE3/MTIOC4B/POE8#/MTIOC1B/TOC3/ CTS12#/RTS12#/SS12#/IRQ11/AN011
61	PE2/MTIOC4A/RXD12/RXDX12/SMISO12/ SSCL12/TS35/IRQ7/AN018/CVREFB0	PE2/MTIOC4A/MTIOC7A/TIC3/RXD12/ SMISO12/SSCL12/RXDX12/IRQ7-DS/ AN010/CVREFC0
62	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12/AN017/CMPB0	PE1/MTIOC4C/MTIOC3B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/IRQ9/AN009/ CMPC00
63	PE0/SCK12/AN016	PE0/MTIOC3D/SCK12/IRQ8/AN008
64	PD2/MTIOC4D/SCK6/IRQ2/AN026	PD2/MTIOC4D/TIC2/CRX0-B/IRQ2/AN018
65	PD1/MTIOC4B/RXD6/SMISO6/SSCL6/IRQ1/ AN025	PD1/MTIOC4B/POE0#/CTX0-B/IRQ1/AN017
66	PD0/TXD6/SMOSI6/SSDA6/IRQ0/AN024	PD0/POE4#/IRQ0/AN016
67	P47*1/AN007	P47/IRQ15-DS/AN007
68	P46*1/AN006	P46/IRQ14-DS/AN006
69	P45*1/AN005	P45/IRQ13-DS/AN005
70	P44*1AN004	P44/IRQ12-DS/AN004
71	P43*1/AN003	P43/IRQ11-DS/AN003
72	P42*1/AN002	P42/IRQ10-DS/AN002
73	P41*1/AN001	P41/IRQ9-DS/AN001
74	VREFL0/PJ7*1	VREFL0/PJ7
75	P40*1/AN000	P40/IRQ8-DS/AN000
76	VREFH0/PJ6*1	VREFH0/PJ6
77	AVCC0	AVCC0
78	P07*1/ADTRG0#	P07/IRQ15/ADTRG0#
79	AVSS0	AVSS0
80	P05*1/DA1	P05/IRQ13/DA1

Notes: 1. The I/O buffer power supply for these pins is AVCC0.
2. PC0 and PC1 are effective only when the port switching function is selected.

3. Not available for products that do not have a sub-clock oscillator.
4. Not available for products that have a sub-clock oscillator.
5. Not available for products that do not have a sub-clock oscillator.

3.2 64-Pin Package

Table 3.2 is Comparative Listing of 64-Pin Package Pin Functions.

Table 3.2 Comparative Listing of 64-Pin Package Pin Functions

64-Pin LFQFP	RX140	RX660
1	P03*1/DA0	P03/IRQ11/DA0
2	VCL	VCL
3	MD/PG7/FINED	MD/FINED/PN6
4	XCIN/PH7*6	XCIN*2/PH7*3
5	XCOUT/PH6*6	XCOUT*2/PH6*3
6	RES#	RES#
7	XTAL/P37/IRQ4	XTAL/P37/IRQ4
8	VSS	VSS
9	EXTAL/P36/IRQ2	EXTAL/P36/IRQ5
10	VCC	VCC
11	P35/NMI	P35/NMI
12	P32/MTIOC0C/TMO3/TXD6*6/SMOSI6*6/ SSDA6*6/TS0*6/IRQ2/RTCOUT	P32/MTIOC0C/TMO3/RTCIC2*5/RTCOUT*5/ POE0#/POE10#/TXD6/SMOSI6/SSDA6/ CTX0-A/IRQ2-DS
13	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/ TS1*6/IRQ1	P31/MTIOC4D/TMCI2/RTCIC1*5/CTS1#/ RTS1#/SS1#/IRQ1-DS
14	P30/MTIOC4B/TMRI3/POE8#/RXD1/ SMISO1/SSCL1/TS2*6/IRQ0	P30/MTIOC4B/TMRI3/RTCIC0*5/POE8#/ RXD1/SMISO1/SSCL1/IRQ0-DS/COMP3
15	P27/MTIOC2B/TMCI3/SCK1/TS3	P27/MTIOC2B/TMCI3/SCK1/IRQ7/CVREFC3
16	P26/MTIOC2A/TMO1/LPTO/TXD1/SMOSI1/ SSDA1/TS4	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/ CTS3#/RTS3#/SS3#/IRQ6/CMPC30
17	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ SCK1/MISOA/SDA0/IRQ7	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ MTIOC4B/SCK1/TXD3/SMOSI3/SSDA3/ MISOA-C/SDA2/IRQ7/COMP2
18	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/ SMOSI1/SSDA1/MOSIA/SCL0/IRQ6/ RTCOUT/ADTRG0#	P16/MTIOC3C/MTIOC3D/TMO2/RTCOUT*5/ TXD1/SMOSI1/SSDA1/RXD3/SMISO3/ SSCL3/MOSIA-C/SCL2/IRQ6/ADTRG0#
19	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/CRXD0/TS5*6/IRQ5	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/SCK3/CRX0-C/IRQ5/ CMPC20
20	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/CTXD0/TS6*6/IRQ4	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/CTX0-C/IRQ4/CVREFC2
21	PH3/MTIOC4D/TMCI0/TS7*6	PH3/MTIOC4D/TMCI0
22	PH2/MTIOC4C/TMRI0/TS8*6/IRQ1	PH2/MTIOC4C/TMRI0/TOC1/IRQ1
23	PH1/MTIOC3D/TMO0/TS9*6/IRQ0	PH1/MTIOC3D/TMO0/TIC1/IRQ0/ADST0
24	PH0/MTIOC3B/TS10*6/CACREF	PH0/MTIOC3B/CACREF/ADTRG0#
25	P55/MTIOC4A/MTIOC4D/TMO3/CRXD0*6/ TS11*6	P55/MTIOC4D/MTIOC4A/TMO3/CRX0-D/ IRQ10
26	P54/MTIOC4B/TMCI1/CTXD0*6/TS12*6	P54/MTIOC4B/TMCI1/CTX0-D/IRQ4
27	PC7/MTIOC3A/MTCLKB/TMO2/LPTO/ TXD8*6/SMOSI8*6/SSDA8*6/MISOA/TS13/ CACREF	UB/PC7/MTIOC3A/MTCLKB/TMO2/ CACREF/TOC0/TXD8/SMOSI8/SSDA8/ SMOSI10/SSDA10/TXD10/TXD010-C/ SMOSI010-C/SSDA010-C/MISOA-A/IRQ14
28	PC6/MTIOC3C/MTCLKA/TMCI2/RXD8*6/ SMISO8*6/SSCL8*6/MOSIA/TS14	PC6/MTIOC3C/MTCLKA/TMCI2/TIC0/RXD8/ SMISO8/SSCL8/SMISO10/SSCL10/RXD10/ RXD010-C/SMISO010-C/SSCL010-C/ MOSIA-A/IRQ13

64-Pin LFQFP	RX140	RX660
29	PC5/MTIOC0C/MTIOC3B/MTCLKD/TMRI2/SCK8*6/RSPCKA/TS15	PC5/MTIOC3B/MTCLKD/TMRI2/MTIOC0C/SCK8/SCK10/SCK010-C/RSPCKA-A/PMC0/IRQ5
30	PC4/MTIOC0A/MTIOC3D/MTCLKC/TMCI1/POE0#/SCK5/CTS8#*6/RTS8#*6/SS8#*6/SSLA0/TSCAP	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/MTIOC0A/SCK5/CTS8#/RTS8#/SS8#/SS10#/CTS10#/RTS10#/CTS010#-B/RTS010#-B/SS010#-B/DE010-B/SSLA0-A/PMC0/IRQ12
31	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5/TS16*6	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5/PMC0/IRQ11
32	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/SSLA3/TS17*6	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/TXDB011-A/SSLA3-A/IRQ10
33	PB7/PC1*4/MTIOC3B/TXD9*6/SMOSI9*6/SSDA9*6/TS18*6	PB7/MTIOC3B/TXD9/SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/TXD011-B/SMOSI011-B/SSDA011-B/IRQ15
34	PB6/PC0*4/MTIOC3D/RXD9*6/SMISO9*6/SSCL9*6/TS19*6	PB6/MTIOC3D/RXD9/SMISO9/SSCL9/SMISO11/SSCL11/RXD11/RXD011-B/SMISO011-B/SSCL011-B/IRQ6
35	PB5/MTIOC2A/MTIOC1B/TMRI1/POE1#/SCK9*6/TS20*6	PB5/MTIOC2A/MTIOC1B/TMRI1/POE4#/TOC2/SCK9/SCK11/SCK011-B/IRQ13
36	PB3/MTIOC0A/MTIOC4A/TMO0/POE3#/LPTO/SCK6*6/TS22*6	PB3/MTIOC0A/MTIOC4A/TMO0/POE11#/TIC2/SCK4/SCK6/PMC0/IRQ3
37	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD6*6/SMOSI6*6/SSDA6*6/TS24*6/IRQ4/CMPOB1	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD4/SMOSI4/SSDA4/TXD6/SMOSI6/SSDA6/IRQ4-DS/COMP1
38	VCC	VCC
39	PB0/MTIOC3D/MTIC5W/RXD6*6/SMISO6*6/SSCL6*6/RSPCKA/TS25	PB0/MTIC5W/MTIOC3D/RXD4/SMISO4/SSCL4/RXD6/SMISO6/SSCL6/RSPCKA-C/IRQ12
40	VSS	VSS
41	PA6/MTIOC3D/MTIC5V/MTCLKB/TMCI3/POE2#/CTS5#/RTS5#/SS5#/MOSIA/TS26*6	PA6/MTIC5V/MTCLKB/TMCI3/POE10#/MTIOC3D/MTIOC6B/CTS5#/RTS5#/SS5#/CTS12#/RTS12#/SS12#/MOSIA-B/IRQ14
42	PA4/MTIOC4C/MTIC5U/MTCLKA/TMRI0/TXD5/SMOSI5/SSDA5/SSLA0/TS28/IRQ5/CVREFB1	PA4/MTIC5U/MTCLKA/TMRI0/MTIOC4C/MTIOC7C/TXD5/SMOSI5/SSDA5/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLA0-B/IRQ5-DS/CVREFC1/ADST0
43	PA3/MTIOC0D/MTIOC4D/MTIC5V/MTCLKD/RXD5/SMISO5/SSCL5/TS29/IRQ6/CMPB1	PA3/MTIOC0D/MTCLKD/MTIC5V/MTIOC4D/RXD5/SMISO5/SSCL5/IRQ6-DS/CMPC10
44	PA1/MTIOC0B/MTIOC3B/MTCLKC/SCK5/SSLA2/TS31	PA1/MTIOC0B/MTCLKC/MTIOC7B/MTIOC3B/SCK5/SCK12/SSLA2-B/IRQ11/ADTRG0#
45	PA0/MTIOC4A/SSLA1/TS32*6/CACREF	PA0/MTIOC4A/CACREF/MTIOC6D/SSLA1-B/IRQ0
46	PE5/MTIOC4C/MTIOC2B/IRQ5/AN021/CMPOB0	PE5/MTIOC4C/MTIOC2B/IRQ5/AN013/COMP0
47	PE4/MTIOC4D/MTIOC1A/MTIOC4A/TS33/AN020/CMPA2/CLKOUT	PE4/MTIOC4D/MTIOC1A/MTIOC4A/MTIOC7D/IRQ12/AN012
48	PE3/MTIOC1B/MTIOC4B/POE8#/CTS12#/RTS12#/SS12#/TS34/AN019/CLKOUT	PE3/MTIOC4B/POE8#/MTIOC1B/TOC3/CTS12#/RTS12#/SS12#/IRQ11/AN011
49	PE2/MTIOC4A/RXD12/RXDX12/SMISO12/SSCL12/TS35/IRQ7/AN018/CVREFB0	PE2/MTIOC4A/MTIOC7A/TIC3/RXD12/SMISO12/SSCL12/RXDX12/IRQ7-DS/AN010/CVREFC0

64-Pin LFQFP	RX140	RX660
50	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12/AN017/CMPB0	PE1/MTIOC4C/MTIOC3B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/IRQ9/AN009/ CMPC00
51	PE0/SCK12/AN016	PE0/MTIOC3D/SCK12/IRQ8/AN008
52	P47*1/AN007	P47/IRQ15-DS/AN007
53	P46*1/AN006	P46/IRQ14-DS/AN006
54	P45*1/AN005	P45/IRQ13-DS/AN005
55	P44*1/AN004	P44/IRQ12-DS/AN004
56	P43*1/AN003	P43/IRQ11-DS/AN003
57	P42*1/AN002	P42/IRQ10-DS/AN002
58	P41*1/AN001	P41/IRQ9-DS/AN001
59	VREFL0/PJ7*1	VREFL0/PJ7
60	P40*1/AN000	P40/IRQ8-DS/AN000
61	VREFH0/PJ6*1	VREFH0/PJ6
62	AVCC0	AVCC0
63	P05*1/DA1	P07/IRQ15/ADTRG0#
64	AVSS0	AVSS0

Notes: 1. The I/O buffer power supply for these pins is AVCC0.
2. Not available for products that do not have a sub-clock oscillator.
3. Not available for products that have a sub-clock oscillator.
4. PC0 and PC1 are effective only when the port switching function is selected.
5. Not available for products that do not have a sub-clock oscillator.
6. Not available for a product whose ROM capacity is 64 KB.

3.3 48-Pin Package

Table 3.3 is Comparative Listing of 48-Pin Package Pin Functions.

Table 3.3 Comparative Listing of 48-Pin Package Pin Functions

48-Pin LFQFP/ HWQFN	RX140	RX660
1	VCL	VCL
2	MD/PG7/FINED	MD/FINED/PN6
3	RES#	RES#
4	XTAL/P37/IRQ4	XTAL/P37/IRQ4
5	VSS	VSS
6	EXTAL/P36/IRQ2	EXTAL/P36/IRQ5
7	VCC	VCC
8	P35/NMI	P35/NMI
9	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/ TS1*3/IRQ1	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/ IRQ1-DS
10	P30/MTIOC4B/TMRI3/POE8#/RXD1/ SMISO1/SSCL1/TS2*3/IRQ0	P30/MTIOC4B/POE8#/RXD1/SMISO1/ SSCL1/IRQ0-DS/COMP3
11	P27/MTIOC2B/TMCI3/SCK1/TS3	P27/MTIOC2B/SCK1/IRQ7/CVREFC3
12	P26/MTIOC2A/TMO1/LPTO/TXD1/SMOSI1/ SSDA1/TS4	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/ CTS3#/RTS3#/SS3#/IRQ6/CMPC30
13	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ SCK1/MISOA/SDA0/IRQ7	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ MTIOC4B/SCK1/TXD3/SMOSI3/SSDA3/ MISOA-C/SDA2/IRQ7/COMP2
14	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/ SMOSI1/SSDA1/MOSIA/SCL0/IRQ6/ ADTRG0#/RTCOUT	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/ SMOSI1/SSDA1/RXD3/SMISO3/SSCL3/ MOSIA-C/SCL2/IRQ6/ADTRG0#
15	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/CRXD0*3/TS5*3/IRQ5	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/SCK3/CRX0-C/IRQ5/ CMPC20
16	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/CTXD0*3/TS6*3/IRQ4	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/CTX0-C/IRQ4/CVREFC2
17	PH3/MTIOC4D/TMCI0/TS7*3	PH3/MTIOC4D/TMCI0
18	PH2/MTIOC4C/TMRI0/TS8*3/IRQ1	PH2/MTIOC4C/TMRI0/TOC1/IRQ1
19	PH1/MTIOC3D/TMO0/TS9*3/IRQ0	PH1/MTIOC3D/TMO0/TIC1/IRQ0/ADST0
20	PH0/MTIOC3B/TS10*3/CACREF	PH0/MTIOC3B/CACREF/ADTRG0#
21	PC7/MTIOC3A/TMO2/MTCLKB/LPTO/ TXD8*3/SMOSI8*3/SSDA8*3/MISOA/TS13/ CACREF	UB/PC7/MTIOC3A/MTCLKB/TMO2/ CACREF/TOC0/TXD8/SMOSI8/SSDA8/ SMOSI10/SSDA10/TXD10/TXD010-C/ SMOSI010-C/SSDA010-C/MISOA-A/IRQ14
22	PC6/MTIOC3C/MTCLKA/TMCI2/RXD8*3/ SMISO8*3/SSCL8*3/MOSIA/TS14	PC6/MTIOC3C/MTCLKA/TMCI2/TIC0/RXD8/ SMISO8/SSCL8/SMISO10/SSCL10/RXD10/ RXD010-C/SMISO010-C/SSCL010-C/ MOSIA-A/IRQ13
23	PC5/MTIOC0C/MTIOC3B/MTCLKD/TMRI2/ SCK8*3/RSPCKA/TS15	PC5/MTIOC3B/MTCLKD/TMRI2/MTIOC0C/ SCK8/SCK10/SCK010-C/RSPCKA-A/PMC0/ IRQ5
24	PC4/MTIOC0A/MTIOC3D/MTCLKC/TMCI1/ POE0#/SCK5/CTS8#*3/RTS8#*3/SS8#*3/ SSLA0/TSCAP	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/ MTIOC0A/SCK5/CTS8#/RTS8#/SS8#/ SS10#/CTS10#/RTS10#/CTS010#-B/ RTS010#-B/SS010#-B/DE010-B/SSLA0-A/ PMC0/IRQ12

48-Pin LFQFP/ HWQFN	RX140	RX660
25	PB5/PC3*1/MTIOC2A/MTIOC1B/TMRI1/ POE1#/TS20*3	PB5/MTIOC2A/MTIOC1B/TMRI1/POE4#/ TOC2/IRQ13
26	PB3/PC2*1/MTIOC0A/MTIOC4A/TMO0/ POE3#/LPTO/SCK6*3/TS22*3	PB3/MTIOC0A/MTIOC4A/TMO0/POE11#/ TIC2/SCK4/SCK6/PMC0/IRQ3
27	PB1/PC1*1/MTIOC0C/MTIOC4C/TMCI0/ TXD6*3/SMOSI6*3/SSDA6*3/TS24*3/IRQ4/ CMPOB1	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD4/ SMOSI4/SSDA4/TXD6/SMOSI6/SSDA6/ IRQ4-DS/COMP1
28	VCC	VCC
29	PB0/PC0*1/MTIOC3D/MTIC5W/RXD6*3/ SMISO6*3/SSCL6*3/RSPCKA/TS25	PB0/MTIC5W/MTIOC3D/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/RSPCKA-C/ IRQ12
30	VSS	VSS
31	PA6/MTIOC3D/MTIC5V/MTCLKB/TMCI3/ POE2#/CTS5#/RTS5#/SS5#/MOSIA/TS26*3	PA6/MTIC5V/MTCLKB/POE10#/MTIOC3D/ CTS5#/RTS5#/SS5#/CTS12#/RTS12#/ SS12#/MOSIA-B/IRQ14
32	PA4/MTIOC4C/MTIC5U/MTCLKA/TMRI0/ TXD5/SMOSI5/SSDA5/SSLA0/TS28/IRQ5/ CVREFB1	PA4/MTIC5U/MTCLKA/TMRI0/MTIOC4C/ MTIOC7C/TXD5/SMOSI5/SSDA5/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLA0-B/IRQ5-DS/CVREFC1/ADST0
33	PA3/MTIOC0D/MTIOC4D/MTIC5V/MTCLKD/ RXD5/SMISO5/SSCL5/TS29/IRQ6/CMPB1	PA3/MTIOC0D/MTCLKD/MTIC5V/MTIOC4D/ RXD5/SMISO5/SSCL5/IRQ6-DS/CMPC10
34	PA1/MTIOC0B/MTIOC3B/MTCLKC/SCK5/ SSLA2/TS31	PA1/MTIOC0B/MTCLKC/MTIOC7B/ MTIOC3B/SCK5/SCK12/SSLA2-B/IRQ11/ ADTRG0#
35	PE4/MTIOC4D/MTIOC1A/MTIOC4A/TS33/ AN020/CMPA2/CLKOUT	PE4/MTIOC4D/MTIOC1A/MTIOC4A/ MTIOC7D/IRQ12/AN012
36	PE3/MTIOC1B/MTIOC4B/POE8#/CTS12#/ RTS12#/TS34/AN019/CLKOUT	PE3/MTIOC4B/POE8#/MTIOC1B/TOC3/ CTS12#/RTS12#/SS12#/IRQ11/AN011
37	PE2/MTIOC4A/RXD12/RXDX12/SSCL12/ TS35/IRQ7/AN018/CVREFB0	PE2/MTIOC4A/MTIOC7A/TIC3/RXD12/ SMISO12/SSCL12/RXDX12/IRQ7-DS/ AN010/CVREFC0
38	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/ SSDA12/AN017/CMPB0	PE1/MTIOC4C/MTIOC3B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/IRQ9/AN009/ CMPC00
39	P47*2/AN007	P47/IRQ15-DS/AN007
40	P46*2/AN006	P46/IRQ14-DS/AN006
41	P45*2/AN005	P45/IRQ13-DS/AN005
42	P42*2/AN002	P42/IRQ10-DS/AN002
43	P41*2/AN001	P41/IRQ9-DS/AN001
44	VREFL0/PJ7*2	VREFL0/PJ7
45	P40*2/AN000	P40/IRQ8-DS/AN000
46	VREFH0/PJ6*2	VREFH0/PJ6
47	AVCC0	AVCC0
48	AVSS0	AVSS0

Notes: 1. PC0 to PC3 are effective only when the port switching function is selected.
2. The I/O buffer power supply for these pins is AVCC0.
3. Not available for a product whose ROM capacity is 64 KB.

4. Important Information when Migrating Between MCUs

This section describes important information on differences between the RX660 Group and the RX140 Group.

For notes regarding software, see section 4.1, Notes on Functional Design.

4.1 Notes on Functional Design

Software operating on the RX140 Groups is compatible with some software written for the RX660 Group. Nevertheless, appropriate caution must be exercised due to differences in aspects such as operation timing and electrical characteristics.

This section describes software-related considerations regarding function settings that differ between the RX660 Group and RX140 Group. For differences between modules and functions, see section 2, Comparative Overview of Specifications.

For further information, refer to the User's Manual: Hardware of each MCU group, listed in section 5, Reference Documents.

4.1.1 VCL Pin (External Capacitor)

When connecting a smoothing capacitor to the VCL pin to stabilize the internal power supply, select a capacitor rated at 0.47 µF for the RX660 Group.

4.1.2 Main Clock Oscillator

When connecting an oscillator to the EXTAL or XTAL pin of the RX660 Group, use an oscillator whose resonator frequency is 8 MHz to 24 MHz.

4.1.3 Software Configurable Interrupt

In the RX660 Group, the software configurable interrupt function is added. Any of the interrupt sources of multiple peripheral modules can be selected and assigned to interrupt vector numbers 128 to 255. Software configurable interrupts are categorized into software configurable interrupt B and software configurable interrupt A by operating clocks of peripheral modules. For details of software configurable interrupt functions, refer to the RX660 Group User's Manual: Hardware listed in section 5, Reference Documents.

4.1.4 Clock Frequency Settings

For the RX660 Group, the system clock (ICLK) and peripheral module clock A, B, and D (PCLKA, PCLKB, and PCLKD) must be configured to satisfy the following conditions:

- PCLKA ≥ PCLKB
- PCLKB:PCLKD = 1:1, 2:1, 4:1, or 1:2

4.1.5 Voltage Level Setting

On the RX660 Group, the operating mode setting in the voltage level setting register (VOLSR), the voltage detection circuit setting in the voltage detection level select register (LVDLVLR), and the option-setting memory setting in the option function select register 1 (OFS1) need to be changed as appropriate to match the operating voltage. Use a program to set these values.

4.1.6 RIIC Operating Voltage Setting

When using the RIIC on the RX660 Group, it is necessary to specify the power supply voltage range to preserve the slope characteristics. VCC is set to a value of 4.5 V or greater by default. If it is set to a value less than 4.5 V, make sure to change the voltage range before activating the RIIC. For details, refer to the description of the VOLSR.RICVLS bit in RX660 Group User's Manual: Hardware.

4.1.7 Option-Setting Memory

On the RX140 Group, the ID code protection codes and ID code protection codes for the on-chip debugger are located in the ROM, but on the RX660 Group, they are located in the option-setting memory. Note that the setting configuration procedures are different.

4.1.8 PLL Circuit

The frequency multiplication factor of the PLL circuit can be set to 4 to 12 (in 0.5 increments) on the RX140 Group and to 10 or 30 (in 0.5 increments) on the RX660 Group. To use the PLL circuit, change the setting of the PLLCR.STC bits to an appropriate value.

4.1.9 Exception Vector Table

In the RX140 Group, the vector table is allocated at a fixed address. In the RX660 Group, however, the vector table can be allocated variably with its start address being the value specified in the exception table register (EXTB).

4.1.10 Performing RAM Self-Diagnostics on Save Register Banks

On the RX660 Group save register banks are configured in the RAM. The save register banks are provided with a buffer, so when a SAVE instruction is used to write data to a register and then a RSTR instruction is used to read data from the same register, the data is actually read from the buffer and not from the RAM memory cells. When performing self-diagnostics on the RAM in a save register bank, use the following sequence of steps for checking the written data in order to prevent the data from being read from the buffer:

(1) Use the SAVE instruction to write data to the bank that is the target of the diagnostic test.
(2) Use the SAVE instruction to write data to a bank other than that written to in step 1.
(3) Use the RSTR instruction to read data from the bank written to in step 1.

4.1.11 Restrictions on Compare Function

The compare function of the 12-bit A/D converter on the RX660 Group is subject to the following restrictions.

1. The compare function cannot be used together with the self-diagnosis function or double trigger mode. (The compare function is not available for the ADRD, ADDBLDR, ADDBLDRA, and ADDBLDRB registers.)
2. It is necessary to specify single scan mode when using match or mismatch event outputs.
3. When the temperature sensor or internal reference voltage is selected for window A, window B operations are disabled.
4. When the temperature sensor or internal reference voltage is selected for window B, window A operations are disabled.
5. It is not possible to set the same channel for window A and window B.
6. It is necessary to set the reference voltage values such that the high-side reference voltage value is equal to or larger than the low-side reference voltage value.

4.1.12 Eliminating I^2C Bus Interface Noise

The RX140 Group has integrated analog noise filters on the SCL and SDA lines, but the RX660 Group has no integrated analog noise filters.

4.1.13 Initialization of Port Direction Register (PDR)

The method of initializing the PDR register differs between the RX140 Group and RX660 Group, even on products with the same pin count.

4.1.14 MTIOC Pin Output Level when Counter Is Stopped

When the MTIOC pin of the RX660 Group is operating in output mode, writing 0 in the CSTn bit of TSTRA or TSTR stops the counter. At this time, in complementary PWM mode or reset-synchronized PWM mode of the RX660 Group, the initial output level specified by the TOCR1A register or the TOCR2A register is output from the MTIOC pin. In a mode other than the complementary PWM mode or the reset-synchronized PWM mode, the output compare output level of the MTIOC pin is retained. When the CSTn bit = 0, when a value is written in the TIOR register, the output level is updated to the initial output value being written.

4.1.15 A/D Conversion Start Request in Complementary PWM Mode

In complementary PWM mode of the RX660 Group, compare match is made not only with MTU4.TGRA (MTU7.TGRA) and MTU4.TCN (MTU7.TCNT) but also with MTU3.TCNT (MTU6.TCNT) and TCNTSA (TCNTSB) to generate the PWM waveform.

Therefore, TRGA4N (TRGA7N) is also generated at a compare match with MTU3.TCNT (MTU6.TCNT) or TCNTSA (TCNTSB). When making an A/D conversion start request while MTU3 and MTU4 (MTU6 and MTU7) are operating in complementary PWM mode, make an A/D conversion start request by compare match with MTU4.TCNT (MTU7.TCNT) or MTU4.TADCORA/TADCORB (MTU7.TADCORA/TADCORB).

4.1.16 High-impedance Control when MTU Pin Is not Selected

In the RX660 Group, if the high impedance control of the MTU pin is enabled by the POECR1 or POECR2 register, the output of a pin that is multiplexed with the MTU function becomes high-impedance when the control condition is satisfied, even if the MTU function is not selected. To prevent unintended high-impedance output from a pin, make setting so that the MTU pin selected by the PmnPFS register of MPC and the MTU pin selected by the pin select register of POE3 coincide.

4.1.17 Generation of Interrupt upon Completion of A/D Scan Conversion

In the RX660 Group, if a scan is started by a software trigger, an A/D scan conversion end interrupt is generated if the ADIE bit is 1 when the scan finishes, even if double trigger mode is selected.

4.1.18 Input Buffer Control by DIRQnE Bit (n = 0 to 15)

In the RX660 Group, setting the DPSIERy.DIRQnE (y = 0 or 1, n = 0 to 15) bit to 1 enables the input buffer of pins IRQ0-DS to IRQ15-DS. By this, the input on the pin is reflected to the DPSIFRy.DIRQnF (y = 0 or 1, n = 0 to 15) bit, but note that it is not reflected to input controllers, peripheral modules, or I/O ports.

4.1.19 Scan Conversion Time of 12-Bit A/D Converter

The scan conversion time differs between the RX140 Group and the RX660 Group. The scan conversion time (t_{SCAN}) for each group of a single scan where the number of selected channels is n is expressed by the equations below.

For details, refer to the description of the 12-bit A/D converter analog input sampling time and scan conversion time in RX140 Group User's Manual: Hardware and RX660 Group User's Manual: Hardware, listed in section 5, Reference Documents.

RX140: $t_{SCAN} = t_D + (t_{DIS} \times n) + t_{DIAG} + (t_{CONV} \times n) + t_{ED}$

RX660: $t_{SCAN} = t_D + (t_{DIS} \times n) + t_{DIAG} + (t_{CONV} \times n) + t_{ED}$

t_{SCAN} (for temperature sensor output and internal reference voltage conversion)

$= t_D + (t_{ADIS} \times m) + (t_{CONV} \times m) + t_{ED}$

t_D: Start-of-scanning-delay time

t_{SPL}: Sampling time

t_{DIS}: Disconnection detection assistance processing time

t_{DIAG}: Self-diagnosis A/D conversion processing time

t_{CONV}: A/D conversion processing time

t_{ED}: End-of-scanning-delay time

t_{ADIS}: Auto-discharging processing time when A/D converting the temperature sensor output and the internal reference voltage

4.1.20 Setting of D/A Converter

When making a setting of the D/A converter of the RX660 Group, make output setting to comparator C by the D/A destination select register (DADSELR), wait for a while until the output of the D/A converter stabilizes, and then enable the operation of the comparator.

When changing the setting of the D/A converter, change the setting after stopping the comparator. Then, wait for a while until the output of the D/A converter stabilizes, and then enable the operation of the comparator.

4.1.21 Comparator C Operation in Module Stop Mode

In the RX660 Group, if the module transitions to the module stop mode while comparator C is operating, the analog circuit of the comparator C keeps operating, so that the analog power supply current is kept equivalent to the condition when comparator C is busy. If the analog power supply current needs to be lowered in module stop mode, set the CMPCTL.HCMPON bit to 0 to stop comparator C.

4.1.22 Comparator C Operation in Software Standby Mode

In the RX660 Group, if the module transitions to the software standby mode while comparator C is operating, the analog circuit of the comparator C keeps operating, so that the analog power supply current is kept equivalent to the condition when comparator C is busy. If the analog power supply current needs to be lowered in software standby mode, set the CMPCTL.HCMPON bit to 0 to stop comparator C.

4.1.23 Interrupt Request in Software Standby Mode

In the RX660 Group, if interrupt requests not configured for exiting software standby mode are generated during software standby mode, they are retained in the interrupt controller. Then, they are processed after the software standby mode is released by some other interrupt source. However, interrupt requests from external pins are not retained.

4.1.24 Timer Mode Register Setting for ELC Event Input

To set the MTU to ELC action operation on the RX660 Group, set the timer mode register (TMDR) of the relevant channel to its initial value (00h).

5. Reference Documents

User’s Manual: Hardware

RX140 Group User's Manual: Hardware Rev1.10 (R01UH0905EJ0110)
(The latest version can be downloaded from the Renesas Electronics website.)

RX660 Group User's Manual: Hardware Rev.1.00 (R01UH0937EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This application note reflects the content of the following technical updates:

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Dec. 23, 2022	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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