RX65N/RX651 Group, RX63N/RX631 Group

Differences Between the RX65N Group and the RX63N Group

Summary

This application note is intended principally as a reference providing an overview of the peripheral functions of the RX65N Group and RX63N Group, to enable checking of the points of difference between the I/O registers and pin functions of the two groups, and to allow confirmation of key points related to migration.

Unless specifically indicated otherwise, the information listed in this application note applies to the 176/177-pin package version of the RX65N Group and to the 176/177-pin package version of the RX63N Group. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the user's manuals of the products in question.

Target Devices

RX65N Group and RX63N Group

Contents

1. Comparison of Functions of RX65N Group and RX63N Group

A comparison of the functions of the RX65N Group and RX63N Group is provided below. For details of the functions, see 2, Comparative Overview of Functions, and 5, Reference Documents.

Table 1.1 is a comparative listing of the functions of the RX65N and RX63N.

Table 1.1 Comparison of Functions of RX65N and RX63N

Function	RX63N	RX65N Code Flash 1.0 MB or less	RX65N Code Flash more than 1.5 MB
CPU	▲		
Operating mode	●/■		
Address space	▲		
Resets	○		
Option-setting memory	●/▲		
Voltage detection circuit (LVDA)	●/▲		
Clock generation circuit	●/▲/■		
Frequency measurement circuit (MCK)	○	×	
Clock frequency accuracy measurement circuit (CAC)	×	○	
Low power consumption function	●		
Battery backup function	○		
Register write protection function	▲		
Exception handling	○		
Interrupt controller (ICUb): RX63N, (ICUB): RX65N	●/▲		
Buses	▲		
Memory-protection unit (MPU)	▲		
DMA controller (DMACA): RX63N, (DMACAa): RX65N	●/▲		
EXDMA controller (EXDMACa):	▲*2		
Data transfer controller (DTCa): RX63N, (DTCb): RX65N	●		
Event link controller (ELC)	×	○	
I/O ports	●/▲		
Multi-function pin controller (MPC)	●/▲/■		
Multi-function timer pulse unit 2 (MTU2a)	○	×	
Multi-function timer pulse unit 3 (MTU3a)	×	○	
Port output enable 2 (POE2a)	○	×	
Port output enable 3 (POE3a)	×	○	
16-bit timer pulse unit (TPUa)	●/▲		
Programmable pulse generator (PPG)	●*2		
8-bit timer (TMR)	●		
Compare match timer (CMT)	●		
Compare match timer W (CMTW)	×	○	
Realtime clock (RTCa): RX63N, (RTCd): RX65N	●		
Watchdog timer (WDTA)	●		
Independent watchdog timer (IWDTa)	●		
Ethernet controller (ETHERC)	○*2		
DMA controller for the ethernet controller (EDMAC): RX63N, (EDMACa): RX65N	▲/■*2		

Function	RX63N	RX65N Code Flash 1.0 MB or less	RX65N Code Flash more than 1.5 MB
USB 2.0 Host/Function module (USBa): RX63N USB 2.0 FS Host/Function module (USBb): RX65N	●/■		
Serial communications interface (SCIc, SCId): RX63N, (SCIg, SCIi, SCIh): RX65N	●/▲		
I²C bus interface (RIIC): RX63N, (RIICa): RX65N	●/▲		
CAN module (CAN)	▲*2		
Serial peripheral interface (RSPI): RX63N, (RSPIc): RX65N	●/▲		
Quad serial peripheral interface (QSPI)	×	○	
IEbus controller (IEB)	○	×	
CRC calculator (CRC): RX63N, (CRCA): RX65N	●		
SD host interface (SDHI)	×	○	
SD slave interface (SDSI)	×	○*2	
Multimedia card interface (MMCIF)	×	○*2	
Parallel data capture unit (PDC)	▲*3		
Boundary scan	○		
AESa	×	○	○*1
RNGa	×	○	○*1
12-bit A/D converter (S12ADa): RX63N, (S12ADFa): RX65N	●/▲		
10-bit A/D converter (ADb)	○	×	
D/A converter (DAa): RX63N 12-bit D/A converter (R12DAa): RX65N	●/▲		
Temperature sensor	▲		
Data operation circuit (DOC)	×	○	
RAM	▲		
Standby RAM	×	○	
Flash memory (code flash)	●/▲		
Flash memory (E2 data flash)	○		×
Flash memory (data flash)	×		○
Trusted Secure IP (TSIP)	×		○
Package	▲/■		

Notes: ○: Function implemented, ×: Function not implemented, ●: Differences exist due to added functionality, ▲: Differences exist due to change in functionality, ■: Differences exist due to removal of functionality.

1. Implemented within Trusted Secure IP (TSIP) module.
2. Not implemented on 64-pin version.
3. The parallel data capture unit (PDC) is implemented on the RX631 but not on the RX63N.

2. Comparative Overview of Functions

2.1 CPU

Table 2.1 is a comparative overview of CPU features, and Table 2.2 is a comparative listing of the CPU registers.

Table 2.1 Comparative Overview of CPU Features

Item	RX63N	RX65N
CPU	• Max. operating frequency: 100 MHz • 32-bit RX CPU • Min. instruction execution time: 1 clock cycle per instruction • Address space: 4 GB, linear addresses • Registers General purpose registers: 32-bit × 16 Control registers: 32-bit × 9 Accumulator: 64-bit × 1 • Basic instructions: 73 • Floating-point operation instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement Instructions: Little-endian Data: Selectable between little-endian and big-endian • 32-bit multiplier: 32-bit × 32-bit → 64-bit • Divider: 32-bit ÷ 32-bit → 32-bit • Barrel shifter: 32-bit • Memory protection unit (MPU)	• Max. operating frequency: 120 MHz • 32-bit RX CPU (RXv2) • Min. instruction execution time: 1 clock cycle per instruction • Address space: 4 GB, linear addresses • Registers General purpose registers: 32-bit × 16 Control registers: 32-bit × 10 Accumulator: 72-bit × 2 • Basic instructions: 75 • Floating-point operation instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement Instructions: Little-endian Data: Selectable between little-endian and big-endian • 32-bit multiplier: 32-bit × 32-bit → 64-bit • Divider: 32-bit ÷ 32-bit → 32-bit • Barrel shifter: 32-bit • Memory protection unit (MPU)
FPU	• Single-precision floating-point numbers (32-bit) • Data types and exceptions in conformance with IEEE 754 standard	• Single-precision floating-point numbers (32-bit) • Data types and exceptions in conformance with IEEE 754 standard

Table 2.2 Comparison of CPU Registers

Register	Bit	RX63N	RX65N
EXTB	—	—	Exception table register
ACC (RX63N) ACC0, ACC1 (RX65N)	—	Accumulator	Accumulator 0, accumulator 1

2.2 Operating Modes

Table 2.3 shows a comparative overview of the operating mode specifications, and Table 2.4 shows a comparative listing of the operating mode registers.

Table 2.3 Comparative Overview of Operating Modes Specifications

Item	RX63N	RX65N
Operating modes specified by mode setting pins	Single-chip mode	Single-chip mode
	Boot mode (SCI interface)	Boot mode (SCI interface)
	Boot mode (USB interface)	Boot mode (USB interface)
	User boot mode	—
	—	Boot mode (FINE interface)
Operating modes specified by register settings	Single-chip mode	Single-chip mode
	User boot mode	—
	On-chip ROM disabled extended mode	On-chip ROM disabled extended mode
	On-chip ROM enabled extended mode	On-chip ROM enabled extended mode

Table 2.4 Comparative Listing of Operating Mode Registers

Register	Bit	RX63N	RX65N
MDSR	—	Mode status register	—
SYSCR1	SBYRAME	—	Standby RAM enable bit

2.3 Address Space

Table 2.5 is a comparative memory map of single-chip mode, Table 2.6 a comparative memory map of on-chip ROM enabled extended mode, and Table 2.7 a comparative memory map of on-chip ROM disabled extended mode.

Table 2.5 Comparative Memory Map of Single-Chip Mode

Start Address	RX63N	RX65N
0000 0000h	RAM	On-chip RAM
0004 0000h	Reserved area	Reserved area
0008 0000h	Peripheral I/O registers	Peripheral I/O registers
000A 4000h		Standby RAM
000A 6000h		Peripheral I/O registers
0010 0000h	On-chip ROM (E2 data flash)	On-chip ROM (data flash memory)
0010 8000h	Reserved area	Reserved area
007E 0000h		FACI command issuing area
007F 0004h		Reserved area
007F 8000h	FCU-RAM area	
007F A000h	Reserved area	
007F C000h	Peripheral I/O registers	Peripheral I/O registers
007F C500h	Reserved area	
007F FC00h	Peripheral I/O registers	
0080 0000h	Reserved area	On-chip expansion RAM
0086 0000h		Reserved area
00E0 0000h	On-chip ROM (program ROM) (write only)	
0100 0000h	Reserved area	
FE7F 5D00h		On-chip ROM (option-setting memory)
FE7F 5D80h		Reserved area
FE7F 7D70h		On-chip ROM (read only)
FE7F 7DA0h		Reserved area
FEFF E000h	On-chip ROM (FCU firmware) (read only)	
FF00 0000h	Reserved area	
FF7F C000h	On-chip ROM (user boot) (read only)	
FF80 0000h	Reserved area	
FFE0 0000h	On-chip ROM (program ROM) (read only)	On-chip ROM (code flash memory)

Table 2.6 Comparative Memory Map of On-Chip ROM Enabled Extended Mode

Start Address	RX63N	RX65N
0000 0000h	RAM	On-chip RAM
0004 0000h	Reserved area	Reserved area
0008 0000h	Peripheral I/O registers	Peripheral I/O registers
000A 4000h		Standby RAM
000A 6000h		Peripheral I/O registers
0010 0000h	On-chip ROM (E2 data flash)	On-chip ROM (data flash memory)
0010 2000h		
0010 8000h	Reserved area	Reserved area
007E 0000h		FACI command issuing area
007F 0004h		Reserved area
007F 8000h	FCU-RAM area	
007F A000h	Reserved area	
007F C000h	Peripheral I/O registers	Peripheral I/O registers
007F C500h	Reserved area	
007F FC00h	Peripheral I/O registers	
0080 0000h	Reserved area	On-chip expansion RAM
0086 0000h		Reserved area
00E0 0000h	On-chip ROM (program ROM) (write only)	
0100 0000h	CS7 (16 MB)	CS7 (16 MB)
0200 0000h	CS6 (16 MB)	CS6 (16 MB)
0300 0000h	CS5 (16 MB)	CS5 (16 MB)
0400 0000h	CS4 (16 MB)	CS4 (16 MB)
0500 0000h	CS3 (16 MB)	CS3 (16 MB)
0600 0000h	CS2 (16 MB)	CS2 (16 MB)
0700 0000h	CS1 (16 MB)	CS1 (16 MB)
0800 0000h	SDCS (128 MB)	SDCS (128 MB)
1000 0000h	Reserved area	Reserved area
FE7F 5D00h		On-chip ROM (option-setting memory)
FE7F 5D80h		Reserved area
FE7F 7D70h		On-chip ROM (read only)
FE7F 7DA0h		Reserved area
FEFF E000h	On-chip ROM (FCU firmware) (read only)	
FF00 0000h	Reserved area	
FF7F C000h	On-chip ROM (user boot) (read only)	
FF80 0000h	Reserved area	
FFE0 0000h	On-chip ROM (program ROM) (read only)	On-chip ROM (code flash memory)

Note: Areas enclosed in thick-bordered boxes are in the external address space (CS area and SDRAM area).

Table 2.7 Comparative Memory Map of On-Chip ROM Disabled Extended Mode

Start Address	RX63N	RX65N
0000 0000h	RAM	On-chip RAM
0004 0000h	Reserved area	Reserved area
0008 0000h	Peripheral I/O registers	Peripheral I/O registers
000A 4000h		Standby RAM
000A 6000h		Peripheral I/O registers
0010 0000h	Reserved area	Reserved area
0080 0000h		On-chip expansion RAM
0086 0000h		Reserved area
0100 0000h	CS7 (16 MB)	CS7 (16 MB)
0200 0000h	CS6 (16 MB)	CS6 (16 MB)
0300 0000h	CS5 (16 MB)	CS5 (16 MB)
0400 0000h	CS4 (16 MB)	CS4 (16 MB)
0500 0000h	CS3 (16 MB)	CS3 (16 MB)
0600 0000h	CS2 (16 MB)	CS2 (16 MB)
0700 0000h	CS1 (16 MB)	CS1 (16 MB)
0800 0000h	SDCS (128 MB)	SDCS (128 MB)
1000 0000h	Reserved area	Reserved area
FF00 0000h	CS0 (16 MB)	CS0 (16 MB)

Note: Areas enclosed in thick-bordered boxes are in the external address space (CS area and SDRAM area).

2.4 Option-Setting Memory

Table 2.8 shows a comparative overview of the option-setting memory registers.

Table 2.8 Comparative Overview of Option-Setting Memory Registers

Register	Bit	RX63N	RX65N
SPCC	—	—	Serial command control register
OSIS	—	—	OCD/serial program ID setting register
OFS0	IWDTRSTIRQS	IWDT reset interrupt request select bit 0: Non-maskable interrupt request is enabled. 1: Reset is enabled.	IWDT reset interrupt request select bit 0: Non-maskable interrupt request or interrupt request is enabled. 1: Reset is enabled.
	WDTRSTIRQS	IWDT reset interrupt request select bit 0: Non-maskable interrupt request is enabled. 1: Reset is enabled.	IWDT reset interrupt request select bit 0: Non-maskable interrupt request or interrupt request is enabled. 1: Reset is enabled.
OFS1	VDSEL[1:0]	—	Voltage detection 0 level select bits
MDEB	—	Endian select register B	—
MDES	—	Endian select register S	—
MDE	MDE[2:0]	—	Endian select
	BANKMD[2:0]	—	Bank Mode Select*1
TMEF	TMEF[2:0]	—	TM enable
	TMEFDB[2:0]	—	Dual-Bank TM Enable*1
TMINF	—	—	TM identification data register
BANKSEL	—	—	Bank Select Register*1
FAW	—	—	Flash access window setting register
ROMCODE	—	—	ROM code protection register

Note: 1. Can be used for products with at least 1.5 MB of code flash memory.

2.5 Voltage Detection Circuit

Table 2.9 shows a comparative overview of the voltage detection circuit specifications, and Table 2.10 shows a comparative listing of the voltage detection circuit registers.

Table 2.9 Comparative overview of Voltage Detection Circuit Specifications

Item		RX63N (LVDA)			RX65N (LVDA)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	Voltage falls lower than Vdet0.	Voltage rises or falls past Vdet1.	Voltage rises or falls past Vdet2.	Voltage falls lower than Vdet0.	Voltage rises or falls past Vdet1.	Voltage rises or falls past Vdet2.
	Detection voltage	One level fixed	Specify voltage using LVDLVLR.LVD1LVL[3:0] bits	Specify voltage using LVDLVLR.LVD2LVL[3:0] bits	Selectable from three levels using OFS1.VDSEL[1:0] bits.	Selectable from three levels using LVDLVLR.LVD1LVL[3:0] bits.	Selectable from three levels using LVDLVLR.LVD2LVL[3:0] bits.
	Monitor flag	—	LVD1SR.LVD1MON flag: Monitors if higher or lower than Vdet1.	LVD2SR.LVD2MON flag: Monitors if higher or lower than Vdet2.	—	LVD1SR.LVD1MON flag: Monitors if higher or lower than Vdet1.	LVD2SR.LVD2MON flag: Monitors if higher or lower than Vdet2.
			LVD1SR.LVD1DET flag: Detects rise or fall past Vdet1.	LVD2SR.LVD2DET flag: Detects rise or fall past Vdet2.		LVD1SR.LVD1DET flag: Detects rise or fall past Vdet1.	LVD2SR.LVD2DET flag: Detects rise or fall past Vdet2.
Voltage detection processing	Reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet0 > VCC: CPU operation restarts a fixed period of time after VCC > Vdet0.	Reset when Vdet1 > VCC: Selectable between CPU operation restarts a fixed period of time after VCC > Vdet1 and CPU operation restarts a fixed period of time after Vdet1 > VCC.	Reset when Vdet2 > VCC: Selectable between CPU operation restarts a fixed period of time after VCC > Vdet2 and CPU operation restarts a fixed period of time after Vdet2 > VCC.	Reset when Vdet0 > VCC: CPU operation restarts a fixed period of time after VCC > Vdet0.	Reset when Vdet1 > VCC: Selectable between CPU operation restarts a fixed period of time after VCC > Vdet1 and CPU operation restarts a fixed period of time after Vdet1 > VCC.	Reset when Vdet2 > VCC: Selectable between CPU operation restarts a fixed period of time after VCC > Vdet2 and CPU operation restarts a fixed period of time after Vdet2 > VCC.
	Interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
			Non-maskable interrupt	Non-maskable interrupt		Selectable between non-maskable interrupt and interrupt.	Selectable between non-maskable interrupt and interrupt.
			Interrupt request generated both when Vdet1 > VCC and when VCC > Vdet1, or one or the other.	Interrupt request generated both when Vdet2 > VCC and when VCC > Vdet2, or one or the other.		Interrupt request generated both when Vdet1 > VCC and when VCC > Vdet1, or one or the other.	Interrupt request generated both when Vdet2 > VCC and when VCC > Vdet2, or one or the other.

Item		RX63N (LVDA)			RX65N (LVDA)		
		Voltage Monitoring 0	Voltage Monitoring 1	Voltage Monitoring 2	Voltage Monitoring 0	Voltage Monitoring 1	Voltage Monitoring 2
Digital filter	Enable/ disable switching	—	Available	Available	—	Available	Available
	Sampling time	—	1/n LOCO frequency × 2 (n: 1, 2, 4, 8)	1/n LOCO frequency × 2 (n: 1, 2, 4, 8)	—	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)
Event link function		—	—	—	—	Available: Vdet pass-through detection event output	Available: Vdet pass-through detection event output

Table 2.10 Comparative Listing of Voltage Detection Circuit Registers

Register	Bit	RX63N (LVDA)	RX65N (LVDA)
LVD1CR1	LVD1IRQSEL	—	Voltage monitoring 1 interrupt type select bit
LVD2CR1	LVD2IRQSEL	—	Voltage monitoring 2 interrupt type select bit
LVDLVLR	LVD1LVL[3:0]	Voltage detection 1 level select bits (standard voltage during drop in voltage) b3 b0 1 0 1 0: 2.95 V Do not set to values other than the above.	Voltage detection 1 level select bits (standard voltage during drop in voltage) b3 b0 1 0 0 1: 2.99 V (Vdet1_1) 1 0 1 0: 2.92 V (Vdet1_2) 1 0 1 1: 2.85 V (Vdet1_3) Do not set to values other than the above.
	LVD2LVL[3:0]	Voltage detection 2 level select bits (standard voltage during drop in voltage) b7 b4 1 0 1 0: 2.95 V Do not set to values other than the above.	Voltage detection 2 level select bits (standard voltage during drop in voltage) b7 b4 1 0 0 1: 2.99 V (Vdet2_1) 1 0 1 0: 2.92 V (Vdet2_2) 1 0 1 1: 2.85 V (Vdet2_3) Do not set to values other than the above.
LVD1CR0	LVD1FSAMP[1:0]	Sampling clock select bits b5 b4 0 0: 1/1 LOCO frequency 0 1: 1/2 LOCO frequency 1 0: 1/4 LOCO frequency 1 1: 1/8 LOCO frequency	Sampling clock select bits b5 b4 0 0: 1/2 LOCO frequency 0 1: 1/4 LOCO frequency 1 0: 1/8 LOCO frequency 1 1: 1/16 LOCO frequency
LVD2CR0	LVD2FSAMP[1:0]	Sampling clock select bits b5 b4 0 0: 1/1 LOCO frequency 0 1: 1/2 LOCO frequency 1 0: 1/4 LOCO frequency 1 1: 1/8 LOCO frequency	Sampling clock select bits b5 b4 0 0: 1/2 LOCO frequency 0 1: 1/4 LOCO frequency 1 0: 1/8 LOCO frequency 1 1: 1/16 LOCO frequency

2.6 Clock Generation Circuit

Table 2.11 shows a comparative overview of the clock generation circuit specifications, and Table 2.12 shows a comparative listing of the clock generation circuit registers.

Table 2.11 Comparative Overview of Clock Generation Circuit Specifications

Item	RX63N	RX65N
Uses	• Generates the system clock (ICLK) supplied to the CPU, DMAC, DTC, ROM, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the ETHERC, EDMAC, and DEU. • Generates the peripheral module clock (PCLKB) supplied to the peripheral modules. • Generates the FlashIF clock (FCLK) supplied to the FlashIF. • Generates the external bus clock (BCLK) supplied to the external bus. • Generates the SDRAM clock (SDCLK) supplied to the SDRAM. • Generates the USB clock (UCLK) supplied to the USB. • Generates the CAN clock (CANMCLK) supplied to the CAN. • Generates the IEBUS clock (IECLK) supplied to the IEBUS. • Generates the RTC-dedicated sub clock (RTCSCLK) supplied to the RTC. • Generates the RTC-dedicated main clock (RTCMCLK) supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) supplied to the IWDT. • Generates the JTAG clock (JTAGTCK) supplied to the JTAG.	• Generates the system clock (ICLK) supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the ETHERC, EDMAC, RSPI, SCIi, MTU3, and AES. • Generates the peripheral module clock (PCLKB) supplied to the peripheral modules. • Generates the peripheral module (analog conversion) clocks (PCLKC: unit 0, PCLKD: unit 1) to be supplied to the S12ADC. • Generates the FlashIF clock (FCLK) supplied to the FlashIF. • Generates the external bus clock (BCLK) supplied to the external bus. • Generates the SDRAM clock (SDCLK) supplied to the SDRAM. • Generates the USB clock (UCLK) supplied to the USBb. • Generates the CAC clock (CACCLK) supplied to the CAC. • Generates the CAN clock (CANMCLK) supplied to the CAN. • Generates the RTC sub clock (RTCSCLK) supplied to the RTC. • Generates the RTC main clock (RTCMCLK) supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) supplied to the IWDT. • Generates the JTAG clock (JTAGTCK) supplied to the JTAG.

Item	RX63N	RX65N
Operating frequencies	• ICLK: 100 MHz (max.) • PCLKA: 100 MHz (max.) • PCLKB: 50 MHz (max.) • FCLK: 4 MHz to 50 MHz (when programming or erasing the ROM or E2 data flash) 50 MHz (max.) (for reading from the E2 data flash) • BCLK: 100 MHz (max.) • BCLK pin output: 50 MHz (max.) • SDCLK pin output: 50 MHz (max.) • UCLK: 48 MHz (max.) • CANMCLK: 20 MHz (max.) • IECLK: 50 MHz (max.) • RTCSCLK: 32.768 kHz • RTCMCLK: 4 MHz to 16 MHz • IWDTCLK: 125 kHz • JTAGTCK: 10 MHz (max.)	• ICLK: 120 MHz (max.) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKC: 60 MHz (max.) • PCLKD: 60 MHz (max.) • FCLK: 4 MHz to 60 MHz (when programming or erasing the code flash memory or data flash memory)*1 60 MHz (max.) (for reading from the data flash)*1 • BCLK: 120 MHz (max.) • BCLK pin output: 60 MHz (max.) • SDCLK pin output: 60 MHz (max.) • UCLK: 48 MHz (max.) • CACCLK: Same frequency as each oscillator • CANMCLK: 24 MHz (max.) • RTCSCLK: 32.768 kHz • RTCMCLK: 8 MHz to 16 MHz • IWDTCLK: 120 kHz • JTAGTCK: 10 MHz (max.)
Main clock oscillator	• Resonator frequency: 4 MHz to 16 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop of the main clock is detected, the system clock source is switched to LOCO, and MTU output can be forcedly driven to high-impedance.	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop of the main clock is detected, the system clock source is switched to LOCO, and MTU output can be forcedly driven to high-impedance.
Sub-clock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pins: XCIN, XCOUT	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pins: XCIN, XCOUT
PLL frequency synthesizer	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 16 MHz • Frequency multiplication ratio: Selectable within range from 8, 10, 12, 16, 20, 24, 25, 50 • VCO oscillation frequency: 104 MHz to 200 MHz	• Input clock source: Main clock, HOCO • Input pulse frequency division ratio: Selectable from 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable within range from 10 to 30 • PLL frequency synthesizer output clock frequency: 120 MHz to 240 MHz
High-speed on-chip oscillator (HOCO)	• Oscillation frequency: 50 MHz • HOCO power supply control	• Oscillation frequency: Selectable from 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control

Item	RX63N	RX65N
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 125 kHz	Oscillation frequency: 240 kHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 125 kHz	Oscillation frequency: 120 kHz
External clock input (TCK) for JTAG	Input clock frequency: 10 MHz (max.)	Input clock frequency: 10 MHz (max.)
Control of output on BCLK pin	• BCLK clock output or high output is selectable • BCLK or BCLK/2 is selectable as the output clock	• BCLK clock output or high output is selectable • BCLK or BCLK/2 is selectable as the output clock
Control of output on SDCLK pin	SDCLK clock output or high output is selectable	SDCLK clock output or high output is selectable
Event link function (output)	—	Main clock oscillator oscillation stop detection
Event link function (input)	—	Switching of clock source to low-speed on-chip oscillator

Note: 1. Can be used for products with at least 1.5 MB of code flash memory.

Table 2.12 Comparative Listing of Clock Generation Circuit Registers

Register	Bit	RX63N	RX65N
SCKCR	PCKD[3:0]	—	Peripheral module clock D (PCLKD) select bits
	PCKC[3:0]	—	Peripheral module clock C (PCLKC) select bits
ROMWT	—	—	ROM wait cycle setting register
SCKCR2	IEBCK[3:0]	IEBUS clock (IECLK) select bits	—
	UCK[3:0]	USB clock (UCLK) select bits b7 b4 0 0 1 0: ×1/3 0 0 1 1: ×1/4 Settings other than the above are prohibited when USB is in use. When USB is not in use, these bits are read as 0001b. The write value should be 0001b.	USB clock (UCLK) select bits b7 b4 0 0 0 1: ×1/2 0 0 1 0: ×1/3 0 0 1 1: ×1/4 0 1 0 0: ×1/5 Settings other than the above are prohibited when USB is in use. When USB is not in use, these bits are read as 0001b. The write value should be 0001b.
PLLCR	PLIDIV[1:0]	PLL input frequency division ratio select bits b1 b0 0 0: ×1 0 1: ×1/2 1 0: ×1/4 1 1: Setting prohibited.	PLL input frequency division ratio select bits b1 b0 0 0: ×1 0 1: ×1/2 1 0: ×1/3 1 1: Setting prohibited.
	PLLSRCSEL	—	PLL clock source select bit

Register	Bit	RX63N	RX65N
PLLCR	STC[5:0]	Frequency multiplication factor select bits b13 b8 0 0 0 1 1 1: ×8 0 0 1 0 0 1: ×10 0 0 1 0 1 1: ×12 0 0 1 1 1 1: ×16 0 1 0 0 1 1: ×20 0 1 0 1 1 1: ×24 0 1 1 0 0 0: ×25 1 1 0 0 0 1: ×50 Do not set to values other than the above.	Frequency multiplication factor select bits b13 b8 0 1 0 0 1 1: ×10.0 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11.0 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12.0 0 1 1 0 0 0: ×12.5 . . . 1 1 1 0 0 1: ×29.0 1 1 1 0 1 0: ×29.5 1 1 1 0 1 1: ×30.0 Do not set to values other than the above.

Register	Bit	RX63N	RX65N
		Initial values after a reset are different.	
HOCOCR2	—	—	High-speed on-chip oscillator control register 2
OSCOVFSR	—	—	Oscillation stabilization flag register
MOSCWTCR*1	MSTS	Bits 0 to 4: Main clock oscillator wait time select bits	Bits 0 to 7: Main clock oscillator wait time select bits
SOSCWTCR*1	SSTS	Bits 0 to 4: Sub-clock oscillator wait time select bits	Bits 0 to 7: Sub-clock oscillator wait time select bits
MOFCR	MODRV2 [1:0]	—	Main clock oscillator drive capability 2 switch bits
	MOSEL	—	Main clock oscillator switch bit

Note: 1. In the User's Manual: Hardware of the RX63N Group, MOSCWTCR and SOSCWTCR are described in section 11, Low Power Consumption.

2.7 Low Power Consumption Functions

Table 2.13 shows a comparative overview of the low power consumption, and Table 2.14 shows a comparative listing of the low power consumption function registers.

Table 2.13 Comparative Overview of Low Power Consumption Functions

Item	RX63N	RX65N
Reduction of power consumption by clock switching	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKA and PCLKB), external bus clock (BCLK), and Flash interface clock (FCLK).	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKA, PCLKB, PCLKC, and PCLKD), external bus clock (BCLK), and Flash interface clock (FCLK).
BCLK output control function	BCLK output or high-level output can be selected.	BCLK output or high-level output can be selected.
SDCLK output control function	SDCLK output or high-level output can be selected.	SDCLK output or high-level output can be selected.
Module stop function	Each peripheral module can be stopped independently.	Each peripheral module can be stopped independently.
Function for transition to low power consumption mode	It is possible to transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped.	It is possible to transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped.
Low power consumption modes	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode
Operating power reduction function	• Power consumption can be reduced in normal operation, sleep mode, and all-module clock stop mode by selecting an appropriate operating power consumption control mode according to the operating frequency and operating voltage. • Operating power control modes: 3 — High-speed operating mode — Low-speed operating mode 1 — Low-speed operating mode 2	• Power consumption can be reduced in normal operation, sleep mode, and all-module clock stop mode by selecting an appropriate operating power consumption control mode according to the operating frequency and operating voltage. • Operating power control modes: 3 — High-speed operating mode — Low-speed operating mode 1 — Low-speed operating mode 2 There is no difference in the power consumption when the same conditions (frequency and voltage) are specified in low-speed operating mode 1 and low-speed operating mode 2.

Table 2.14 Comparative Listing of Low Power Consumption Function Registers

Register	Bit	RX63N	RX65N
MSTPCRA	MSTPA0	—	Compare match timer W (unit 1) module stop bit
	MSTPA1	—	Compare match timer W (unit 0) module stop bit
	MSTPA9	Multi-function timer pulse unit 2 module stop bit	Multi-function timer pulse unit 3 module stop bit
	MSTPA12	16-bit timer pulse unit 1 (unit 1) module stop bit	—
	MSTPA16	—	12-bit A/D converter (unit 1) module stop bit
	MSTPA23	10-bit A/D converter module stop bit	—
MSTPCRB	MSTPB2	CAN module 2 module stop bit	—
	MSTPB4	Serial communication interface SCId module stop bit	Serial communication interface SCIh module stop bit
	MSTPB6	—	Data operation circuit module stop bit
	MSTPB9	—	Event link controller module stop bit
	MSTPB15	Ethernet controller DMAC(channel0) module stop bit	Ethernet controller and Ethernet controller DMAC(channel0) module stop bit
	MSTPB18	Universal serial bus interface (port 1) module stop bit	—
	MSTPB20	I^2C bus interface module stop bit	I^2C bus interface module stop bit*2
MSTPCRC	MSTPC1	RAM1 module stop bit	—
	MSTPC2	—	Expansion RAM Module Stop*2
	MSTPC7	—	Standby RAM module stop bit
	MSTPC16	I^2C bus interface 3 module stop bit	—
	MSTPC18	IEBUS module stop bit	—
	MSTPC19	Frequency measurement circuit module stop bit	CAC module stop bit
	MSTPC23	—	Quad serial/parallel interface module stop bit
	MSTPC28	—	2D drawing engine Module Stop*2
	MSTPC29	—	Graphic-LCD controller Module Stop*2
MSTPCRD	MSTPD0	—	Module stop D0 setting bit
	MSTPD1	—	Module stop D1 setting bit
	MSTPD2	—	Module stop D2 setting bit
	MSTPD3	—	Module stop D3 setting bit
	MSTPD4	—	Module stop D4 setting bit
	MSTPD5	—	Module stop D5 setting bit
	MSTPD6	—	Module stop D6 setting bit
	MSTPD7	—	Module stop D7 setting bit
	MSTPD13	—	SD slave interface module stop bit
	MSTPD19	—	SD host interface module stop bit
	MSTPD21	—	MMC host interface module stop bit
	MSTPD27	—	Trusted Secure IP Module Stop*2
	MSTPD31	Data encryption unit (DEU) module stop bit	—

Register	Bit	RX63N	RX65N
MOSCWTCR *1	MSTS	Bits 0 to 4: Main clock oscillator wait time select bits	Bits 0 to 7: Main clock oscillator wait time select bits
SOSCWTCR *1	SSTS	Bits 0 to 4: Main clock oscillator wait time select bits	Bits 0 to 7: Main clock oscillator wait time select bits
PLLWTCR	—	PLL wait control register	—

Notes: 1. In the User's Manual: Hardware of the RX65N Group, MOSCWTCR and SOSCWTCR are described in the Clock Generation Circuit section.
2. Can be used for products with at least 1.5 MB of code flash memory.

2.8 Register Write Protection Function

Table 2.15 shows a comparative overview of the register write protection function.

Table 2.15 Comparative Overview of Register Write Protection Function

Item	RX63N	RX65N
PRC0 bit	Registers related to the clock generation circuit SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR	Registers related to the clock generation circuit SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, OSTDCR, OSTDSR
PRC1 bit	• Registers related to the operating modes SYSCR0, SYSCR1 • Registers related to the low power consumption functions SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, MOSCWTCR*1, SOSCWTCR*1, PLLWTCR, DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, DPSIEGR0 to DPSIEGR3 • Registers related to the clock generation circuit MOFCR, HOCOPCR • Software reset register SWRR	• Registers related to the operating modes SYSCR0, SYSCR1 • Registers related to the low power consumption functions SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, DPSIEGR0 to DPSIEGR3 • Registers related to the clock generation circuit MOSCWTCR*1, SOSCWTCR*1, MOFCR, HOCOPCR • Software reset register SWRR
PRC3 bit	Registers related to the LVD LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	Registers related to the LVD LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

Note: 1. In the User's Manual: Hardware of the RX65N Group, MOSCWTCR and SOSCWTCR are described in the Clock Generation Circuit section.

2.9 Interrupt Controller

Table 2.16 shows a comparative overview of the interrupt controller specifications, and Table 2.17 shows a comparative listing of the interrupt controller registers.

Table 2.16 Comparative Overview of Interrupt Controller Specifications

Item		RX63N (ICUb)	RX65N (ICUB)
Interrupt	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection (detection method is fixed for each interrupt source) • Interrupt grouping: Multiple interrupt sources can be grouped together and treated as a single interrupt source. — Number of groups for edge detection interrupts: 7 (groups 0 to 6) — Number of groups for edge detection interrupts: 1 (group 12) • Interrupt unit selection: One of two interrupt requests can be selected as the interrupt request source. Number of units: 6	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection (detection method is fixed for each interrupt source) • Interrupt grouping: Multiple interrupt sources can be grouped together and treated as a single interrupt source. — Group BE0 interrupt: Peripheral module interrupt source using PCLKB as operation clock (edge detection) — Group BL0, BL1, and BL2 interrupts: Peripheral module interrupt sources using PCLKB as operation clock (level detection) — Group AL0 and AL1 interrupts: Peripheral module interrupt sources using PCLKA as operation clock (level detection) • Selectable interrupt B: For each interrupt vector number from 128 to 207, one peripheral module interrupt source using PCLKB as operation clock may be assigned. • Selectable interrupt A: For each interrupt vector number from 208 to 255, one peripheral module interrupt source using PCLKA as operation clock may be assigned.

Item		RX63N (ICUb)	RX65N (ICUB)
Interrupt	External pin interrupts	• Interrupts from signals input to IRQi pins (i = 0 to 15) • Interrupt detection: Low level, falling edge, rising edge, and rising and falling edges. One of these detection methods can be set for each source. • Digital filter may be used to suppress noise.	• Interrupts from signals input to IRQi pins (i = 0 to 15) • Interrupt detection: Low level, falling edge, rising edge, and rising and falling edges. One of these detection methods can be set for each source. • Digital filter may be used to suppress noise.
	Software interrupt	• Interrupts can be generated by writing to a register. • Interrupt sources: 1	• Interrupts can be generated by writing to a register. • Interrupt sources: 2
	Interrupt priority level	Priority level can be set with interrupt source priority register r (IPRr) (r = 000 to 255).	Priority level can be set with interrupt source priority register r (IPRr) (r = 000 to 255).
	Fast interrupt function	CPU interrupt response time can be reduced. This function can be used for only one interrupt source.	CPU interrupt response time can be reduced. This function can be used for only one interrupt source.
	DTC and DMAC control	Interrupt sources can be used to start the DTC and DMAC.	Interrupt sources can be used to start the DTC and DMAC.
	EXDMAC control	—	• Interrupt selected by software configurable interrupt B source select register 144 or software configurable interrupt A source select register 208 can be used to start EXDMAC0. • Interrupt selected by software configurable interrupt B source select register 145 or software configurable interrupt A source select register 209 can be used to start EXDMAC1.
Non-maskable interrupts	NMI pin interrupt	Interrupts from signals input to NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter may be used to suppress noise.	Interrupts from signals input to NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter may be used to suppress noise.
	Oscillation stop detection interrupt	Interrupt on detection of oscillation stop by main clock oscillator	Interrupt on detection of oscillation stop by main clock oscillator
	WDT underflow/ refresh error interrupt	This interrupt occurs when the watchdog timer (WDT) underflows or a refresh error occurs.	This interrupt occurs when the watchdog timer (WDT) underflows or a refresh error occurs.
	IWDT underflow/ refresh error interrupt	This interrupt occurs when the independent watchdog timer (IWDT) underflows or a refresh error occurs.	This interrupt occurs when the independent watchdog timer (IWDT) underflows or a refresh error occurs.

Item		RX63N (ICUb)	RX65N (ICUB)
Non-maskable interrupts	Voltage monitoring 1 interrupt	Interrupt triggered by voltage detection circuit 1 (LVD1)	Interrupt triggered by voltage detection circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Interrupt triggered by voltage detection circuit 2 (LVD2)	Interrupt triggered by voltage detection circuit 2 (LVD2)
	RAM error interrupt	—	Interrupt triggered when RAM parity error detected
Return from low power consumption modes	Sleep mode	Return is initiated by any interrupt source.	Return is initiated by any interrupt source.
	All-module clock stop mode	Return is initiated by NMI pin interrupts, external pin interrupts, and peripheral function interrupts (voltage monitor 1, voltage monitor 2, oscillation stop detection, USB resume, RTC alarm, RTC period, IWDT, TMR interrupts).	Return is initiated by NMI pin interrupts, external pin interrupts, and peripheral function interrupts (voltage monitor 1, voltage monitor 2, oscillation stop detection, USB resume, RTC alarm, RTC period, IWDT, selectable interrupts 146 to 157).
	Software standby mode	Return is initiated by NMI pin interrupts, external pin interrupts, and peripheral function interrupts (voltage monitor 1, voltage monitor 2, USB resume, RTC alarm, RTC period, IWDT).	Return is initiated by NMI pin interrupts, external pin interrupts, and peripheral function interrupts (voltage monitor 1, voltage monitor 2, USB resume, RTC alarm, RTC period, IWDT).
	Deep software standby mode	Return is initiated by NMI pin interrupts, some external pin interrupts, and peripheral function interrupts (voltage monitor 1, voltage monitor 2, USB resume, RTC alarm, RTC period).	Return is initiated by NMI pin interrupts, some external pin interrupts, and peripheral function interrupts (voltage monitor 1, voltage monitor 2, USB resume, RTC alarm, RTC period).

Table 2.17 Comparative Listing Interrupt Controller Registers

Register	Bit	RX63N (ICUb)	RX65N (ICUB)
SWINT2R	—	—	Software interrupt 2 generation register
DTCERn	—	DTC activation enable register n (n = 027 to 251)	DTC transfer request enable register n (n = 026 to 255)
DMRSRm	—	DMAC activation request select register (m = 0 to 3)	DMAC trigger request select register (m = 0 to 7)
GRPm	—	Group m interrupt source register (m = 0 to 6, 12)	—
NMISR	RAMST	—	RAM error interrupt status flag
NMIER	RAMEN	—	RAM error interrupt enable bit
GRPBE0	—	—	Group BE0 interrupt request register
GRPBL0	—	—	Group BL0 interrupt request register
GRPBL1	—	—	Group BL1 interrupt request register
GRPBL2			Group BL2 interrupt request register
GRPAL0	—	—	Group AL0 interrupt request register

Register	Bit	RX63N (ICUb)	RX65N (ICUB)
GRPAL1	—	—	Group AL1 interrupt request register
GENm	—	Group m interrupt enable register (m = 0 to 6, 12)	—
GENBE0	—	—	Group BE0 interrupt request enable register
GENBL0	—	—	Group BL0 interrupt request enable register
GENBL1	—	—	Group BL1 interrupt request enable register
GENBL2			Group BL2 interrupt request enable register
GENAL0	—	—	Group AL0 interrupt request enable register
GENAL1	—	—	Group AL1 interrupt request enable register
GCRm	—	Group m interrupt clear register (m = 0 to 6)	—
GCRBE0	—	—	Group BE0 interrupt clear register
SEL	—	Unit selecting register	—
PIBRk	—	—	Software configurable interrupt B request register k (k = 0h to Bh)
PIARk	—	—	Software configurable interrupt A request register k (k = 0h to 5h, Bh)
SLIBXRn	—	—	Software configurable interrupt B source select register Xn (n = 128 to 143)
SLIBRn	—	—	Software configurable interrupt B source select register n (n = 144 to 207)
SLIARn	—	—	Software configurable interrupt A source select register n (n = 208 to 255)
SELEXDR	—	—	EXDMAC trigger select register
SLIPRCR	—	—	Software configurable interrupt source select register write protect register

2.10 Buses

Table 2.18 shows a comparative overview of the bus specifications, Table 2.19 shows a comparative overview of the external bus specifications, and Table 2.20 shows a comparative listing of the bus registers.

Table 2.18 Comparative Overview of Bus Specifications

Bus Type		RX63N	RX65N
CPU bus	Instruction bus	• Connected to the CPU (for instructions). • Connected to the on-chip memory (RAM and ROM). • Operates in synchronization with the system clock (ICLK).	• Connected to the CPU (for instructions). • Connected to the on-chip memory (RAM, expansion RAM*1, code flash memory). • Operates in synchronization with the system clock (ICLK).
	Operand bus	• Connected to the CPU (for operand). • Connected to the on-chip memory (RAM and ROM). • Operates in synchronization with the system clock (ICLK).	• Connected to the CPU (for operand). • Connected to the on-chip memory (RAM, code flash memory). • Operates in synchronization with the system clock (ICLK).
Memory buses	Memory bus 1	Connected to the RAM.	Connected to the RAM.
	Memory bus 2	Connected to the ROM.	Connected to the code flash memory
	Memory bus 3	None	Connected to expansion RAM*1
Internal main buses	Internal main bus 1	• Connected to the CPU. • Operates in synchronization with the system clock (ICLK).	• Connected to the CPU. • Operates in synchronization with the system clock (ICLK).
	Internal main bus 2	• Connected to the DTC, DMAC, and EDMAC. • Connected to the on-chip memory (RAM and ROM). • Operates in synchronization with the system clock (ICLK).	Connected to the DTC, DMAC, EDMAC, SDSI, GLCDC*1, and DRW2D*1. • Connected to the on-chip memory (RAM, expansion RAM*1, code flash memory). • Operates in synchronization with the system clock (ICLK).
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, DMAC, EXDMAC, DEU, interrupt controller, and bus error monitoring section). • Operates in synchronization with the system clock (ICLK). (EXDMAC operates in synchronization with BCLK.)	• Connected to peripheral modules (DTC, DMAC, EXDMAC, interrupt controller, and bus error monitoring section). • Operates in synchronization with the system clock (ICLK). (EXDMAC operates in synchronization with BCLK.)
	Internal peripheral bus 2	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, 4, and 5). • Operates in synchronization with the peripheral module clock (PCLKB).	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, 4, and 5). • Operates in synchronization with the peripheral module clock (PCLKB).
	Internal peripheral bus 3	• Connected to peripheral modules (USB0 and PDC). • Operates in synchronization with the peripheral module clock (PCLKB).	• Connected to peripheral modules (USBb, PDC, and standby RAM). • Operates in synchronization with the peripheral module clock (PCLKB).

Bus Type		RX63N	RX65N
Internal peripheral buses	Internal peripheral bus 4	• Connected to peripheral modules (EDMAC and ETHERC). • Operates in synchronization with the peripheral module clock (PCLKA).	• Connected to peripheral modules (EDMAC, ETHERC, MTU3, SCIi, RSPI, and AES). • Operates in synchronization with the peripheral module clock (PCLKA).
	Internal peripheral bus 5	Reserved area	• Connected to peripheral modules (GLCDC, DRW2D)*1 • Operates in synchronization with the peripheral-module clock (PCLKA)*1
	Internal peripheral bus 6	• Connected to the ROM (in P/E) and E2 data flash. • Operates in synchronization with the FlashIF clock (FCLK).	• Connected to code flash (in P/E) and data flash memory*1. • Operates in synchronization with the FlashIF clock (FCLK).
External bus	CS area	• Connected to external devices. • Operates in synchronization with the external bus clock (BCLK).	• Connected to external devices. • Operates in synchronization with the external bus clock (BCLK).
	SDRAM area	• Connected to SDRAM. • Operates in synchronization with the SDRAM clock (SDCLK).	• Connected to SDRAM. • Operates in synchronization with the SDRAM clock (SDCLK).

Note: 1. Can be used for products with at least 1.5 MB of code flash memory.

Table 2.19 Comparative Overview of External Bus Specifications

Item	RX63N	RX65N
External address space	• The external address space is divided into eight CS areas (CS0 to CS7) and the SDRAM area (SDCS) for management. • Chip select signals can be output for each area. • The bus width can be specified for each area. — Separate bus: An 8, 16, or 32-bit bus space is selectable. — Address/data multiplexed bus: An 8 or 16-bit bus space is selectable. • The endian mode can be specified for each area.	• The external address space is divided into eight CS areas (CS0 to CS7) and the SDRAM area (SDCS) for management. • Chip select signals can be output for each area. • The bus width can be specified for each area. — Separate bus: An 8, 16, or 32-bit bus space*2 is selectable. — Address/data multiplexed bus: An 8 or 16-bit bus space is selectable. • The endian mode can be specified for each area.

Item	RX63N	RX65N
CS area controller	• Recovery cycles can be inserted. Read recovery: Up to 15 cycles Write recovery: Up to 15 cycles • Cycle wait function: Wait for up to 31 cycles (page access: up to 7 cycles) • Wait control — Timing of assertion and negation of chip-select signals (CS0# to CS7#) — Timing of assertion of the read signal (RD#) and write signals (WR#, WR0# to WR3#) — Timing of start and end of data output. • Write access mode: Single write strobe mode/byte strobe mode • Separate bus or address/data multiplexed bus can be set for each area.	• Recovery cycles can be inserted. Read recovery: Up to 15 cycles Write recovery: Up to 15 cycles • Cycle wait function: Wait for up to 31 cycles (page access: up to 7 cycles) • Wait control — Timing of assertion and negation of chip-select signals (CS0# to CS7#) — Timing of assertion of the read signal (RD#) and write signals (WR#, WR0#, and WR1# to WR3#*2) — Timing of start and end of data output. • Write access mode: Single write strobe mode/byte strobe mode • Separate bus or address/data multiplexed bus can be set for each area.
SDRAM area controller	• Multiplexed output of row address/column address (8, 9, 10, or 11 bits) • Selectable between self-refresh and auto-refresh. • CAS latency can be specified from one to three cycles.	• Multiplexed output of row address/column address (8, 9, 10, or 11 bits) • Selectable between self-refresh and auto-refresh. • CAS latency can be specified from one to three cycles.
Write buffer function	When write data from the bus master has been written to the write buffer, write access by the bus master is completed.	When write data from the bus master has been written to the write buffer, write access by the bus master is completed.
Frequency	• The CS area controller (CSC) operates in synchronization with the external-bus clock (BCLK).*1 • The SDRAM area controller (SDRAMC) operates in synchronization with the SDRAM clock (SDCLK).	• The CS area controller (CSC) operates in synchronization with the external-bus clock (BCLK).*1 • The SDRAM area controller (SDRAMC) operates in synchronization with the SDRAM clock (SDCLK).

Notes: 1. BCLK and the SDCLK operate at the same frequency when the SDRAM is in use.
2. Can be used for products with at least 1.5 MB of code flash memory.

Table 2.20 Comparative Listing of Bus Registers

Register	Bit	RX63N	RX65N
CSnCR (n = 0 to 7)	BSIZE[1:0]	External bus width select bits b5 b4 0 0: A 16-bit bus width is selected. 0 1: A 32-bit bus width is selected. 1 0: An 8-bit bus width is selected. 1 1: Setting prohibited.	External bus width select bits b5 b4 0 0: A 16-bit bus width is selected. 0 1: Setting prohibited./A 32-bit bus width is selected*1. 1 0: An 8-bit bus width is selected. 1 1: Setting prohibited.
SDCCR	BSIZE[1:0]	SDRAM bus width select bits b5 b4 0 0: A 16-bit bus width is selected. 0 1: A 32-bit bus width is selected. 1 0: An 8-bit bus width is selected. 1 1: Setting prohibited.	SDRAM bus width select bits b5 b4 0 0: A 16-bit bus width is selected. 0 1: Setting prohibited. /A 32-bit bus width is selected*1. 1 0: An 8-bit bus width is selected. 1 1: Setting prohibited.
BERSR1	MST[2:0]	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: EDMAC 1 1 1: EXDMAC	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Extended bus master 1 1 1: EXDMAC
BUSPRI	BPRA[1:0]	Memory bus 1 (RAM) priority control bits	Memory bus 1 and 3 (RAM/expansion RAM) priority control bits*2
EBMAPCR	—	—	Extended bus master priority control register*1

Note: 1. Can be used for products with at least 1.5 MB of code flash memory.

2.11 Memory Protection Unit

Table 2.21 shows a comparative listing of the memory protection unit registers.

Table 2.21 Comparative Listing of Memory Protection Unit Registers

Register	Bit	RX63N	RX65N
MPESTS	IA	Instruction memory protection error generated bit	—
	DA	Data memory protection error generated bit	—
	IMPER	—	Instruction memory protection error generation bit
	DMPER	—	Data memory protection error generation bit

2.12 DMA Controller

Table 2.22 shows a comparative overview of the DMA controller specifications, and Table 2.23 shows a comparative listing of the DMA controller registers.

Table 2.22 Comparative Overview of DMA Controller

Item		RX63N (DMACA)	RX65N (DMACAa)
Number of channels		4 (DMACm (m = 0 to 3))	8 (DMACm (m = 0 to 7))
Transfer space		512 MB (00000000h to 0FFFFFFFh and F0000000h to FFFFFFFFh, excluding reserved areas)	512 MB (00000000h to 0FFFFFFFh and F0000000h to FFFFFFFFh, excluding reserved areas)
Maximum transfer volume		1 MB (maximum number of transfers in block transfer mode: 1,024 data × 1,024 blocks)	64 MB (maximum number of transfers in block transfer mode: 1,024 data × 65,536 blocks)
DMA request sources		Activation source selectable for each channel • Software trigger • Interrupt requests from peripheral modules or trigger input to external interrupt input pins	Activation source selectable for each channel • Software trigger • Interrupt requests from peripheral modules or trigger input to external interrupt input pins
Channel priority		Channel 0 > channel 1 > channel 2 > channel 3 (channel 0: highest)	Channel 0 > channel 1 > channel 2 > channel 3 ... > channel 7 (channel 0: highest)
Transfer data	Single data	Bit length: 8, 16, 32 bits	Bit length: 8, 16, 32 bits
	Block size	Number of data: 1 to 1,024	Number of data: 1 to 1,024
Transfer modes	Normal transfer mode	• One data transfer per DMA transfer request • Setting in which total number of data transfers is not specified (free running mode) is available.	• One data transfer per DMA transfer request • Setting in which total number of data transfers is not specified (free running mode) is available.
	Repeat transfer mode	• One data transfer per DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. • Maximum settable repeat size: 1,024 data	• One data transfer per DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. • Maximum settable repeat size: 1,024 data
	Block transfer mode	• One block data transfer per DMA transfer request • Maximum settable block size: 1,024 data	• One block data transfer per DMA transfer request • Maximum settable block size: 1,024 data
Selective functions	Extended repeat area function	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed • Area of 2 bytes to 128 MB separately settable as extended repeat area for transfer source or destination	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed • Area of 2 bytes to 128 MB separately settable as extended repeat area for transfer source or destination

Item		RX63N (DMACA)	RX65N (DMACAa)
Interrupt request	Transfer end interrupt	Generated on completion of transferring data volume specified by the transfer counter.	Generated on completion of transferring data volume specified by the transfer counter.
	Transfer escape end interrupt	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.
Event link activation		—	Event link request generated after one data transfer (or after one block transfer in case of block transfer operation).
Low power consumption function		Module stop state can be set.	Module stop state can be set.

Table 2.23 Comparative Listing of DMA Controller Registers

Register	Bit	RX63N (DMACA)	RX65N (DMACAa)
DMCRB	—	DMA block transfer count register (b9 to b0)	DMA block transfer count register (b15 to b0)
DMIST	—	—	DMAC74 interrupt status monitor register

2.13 EXDMA Controller

Table 2.24 shows a comparative overview of the EXDMA controller specifications, and Table 2.25 shows a comparative listing of the EXDMA controller registers.

Table 2.24 Comparative Overview of EXDMA Controller

Item		RX63N (EXDMACa)	RX65N (EXDMACa)
Number of channels		2 (EXDMAC0 and EXDMAC1)	2 (EXDMAC0 and EXDMAC1)
Transfer space		512 MB (external areas from 0000 0000h to 0FFF FFFFh and F000 0000h to FFFF FFFFh, excluding reserved areas)	512 MB (external areas from 0000 0000h to 0FFF FFFFh and F000 0000h to FFFF FFFFh, excluding reserved areas)
Maximum transfer volume		1 MB (maximum number of transfers in block transfer mode: 1,024 data × 1,024 blocks)	1 MB (maximum number of transfers in block transfer mode: 1,024 data × 1,024 blocks)
DMA request sources		Activation source selectable from the following three sources for each channel: • Software trigger • External DMA transfer request input • DMA transfer request from peripheral module (compare match A of MTU1 or TPU7)	Activation source selectable from the following three sources for each channel: • Software trigger • External DMA transfer request input • DMA transfer request from peripheral module (TPU1.TRGA or MTU1.TRGA) (Channel 0: a software configurable interrupt B request from TPU1.TRGA selected in ICU.SLIBR144 or a software configurable interrupt A request from MTU1.TRGA selected in ICU.SLIAR208; Channel 1: a software configurable interrupt B request from TPU1.TRGA selected in ICU.SLIBR145 or a software configurable interrupt A request from MTU1.TRGA selected in ICU.SLIAR209)
Channel priority		Channel 0 > channel 1 (channel 0: highest)	Channel 0 > channel 1 (channel 0: highest)
Transfer data	Single data	Bit length: 8, 16, 32 bits	Bit length: 8, 16, 32 bits
	Block size	Number of data: 1 to 1,024 data	Number of data: 1 to 1,024 data
	Cluster size	Number of data: 1 to 8 data	Number of data: 1 to 8 data
Transfer modes	Normal transfer mode	• One data transfer per DMA transfer request • Setting in which total number of data transfers is not specified (free running mode) is available.	• One data transfer per DMA transfer request • Setting in which total number of data transfers is not specified (free running mode) is available.

Item		RX63N (EXDMACa)	RX65N (EXDMACa)
Transfer modes	Repeat transfer mode	• One data transfer per DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. • Maximum settable repeat size: 1,024 data	• One data transfer per DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. • Maximum settable repeat size: 1,024 data
	Block transfer mode	• One block data transfer per DMA transfer request • Maximum settable block size: 1,024 data	• One block data transfer per DMA transfer request • Maximum settable block size: 1,024 data
	Cluster transfer	• One cluster data transfer per DMA transfer request • Maximum settable cluster size: 8 data (32 bytes)	• One cluster data transfer per DMA transfer request • Maximum settable cluster size: 8 data (32 bytes)
Address modes	Single address mode	• Transfers data by accessing the transfer source or destination peripheral device with the EDACKn (n = 0 or 1) signal and specifying the address of the other peripheral device. • Available in normal transfer mode, repeat transfer mode, and block transfer mode.	• Transfers data by accessing the transfer source or destination peripheral device with the EDACKn (n = 0 or 1) signal and specifying the address of the other peripheral device. • Available in normal transfer mode, repeat transfer mode, and block transfer mode.
	Dual address mode	• Transfers data by specifying the addresses of the transfer source and destination. • Available in normal transfer mode, repeat transfer mode, block transfer mode, and cluster transfer mode.	• Transfers data by specifying the addresses of the transfer source and destination. • Available in normal transfer mode, repeat transfer mode, block transfer mode, and cluster transfer mode.
Selective functions	Extended repeat area function	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed • Area of 2 bytes to 128 MB separately settable as extended repeat area for transfer source or destination	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed • Area of 2 bytes to 128 MB separately settable as extended repeat area for transfer source or destination
Interrupt request	Transfer end interrupt	Generated on completion of transferring data volume specified by the transfer counter.	Generated on completion of transferring data volume specified by the transfer counter.
	Transfer escape end interrupt	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.
Low power consumption function		Module stop state can be set.	Module stop state can be set.

Table 2.25 Comparative Listing of EXDMA Controller Registers

Register	Bit	RX63N (EXDMAa)	RX65N (EXDMAa)
EDMTMD	DCTG[1:0]	Transfer request source select bits b1 b0 0 0: Software 0 1: Setting prohibited. 1 0: External DMA transfer request pin (EDREQn) 1 1: DMA transfer requests from peripheral modules (compare match A of MTU1 or TPU7)	Transfer request source select bits b1 b0 0 0: Software 0 1: Setting prohibited. 1 0: External DMA transfer request pin (EDREQn) 1 1: DMA transfer requests from peripheral modules (TPU1.TRGA or MTU1.TRGA)

2.14 Data Transfer Controller

Table 2.26 shows a comparative overview of the data transfer controller specifications, and Table 2.27 shows a comparative listing of the data transfer controller registers.

Table 2.26 Comparative Overview of Data Transfer Controller

Item	RX63N (DTCa)	RX65N (DTCb)
Transfer modes	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address is returned to the transfer start address after a number of data transfers corresponding to the repeat size. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, 1,024 bytes. • Block transfer mode — A single activation leads to the transfer of a single block. — Maximum block size setting: 256 × 32 bits = 1,024 bytes	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address is returned to the transfer start address after a number of data transfers corresponding to the repeat size. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, 1,024 bytes. • Block transfer mode — A single activation leads to the transfer of a single block. — Maximum block size setting: 256 × 32 bits = 1,024 bytes
Transfer channels	• Channel transfer corresponding to the interrupt source is possible (transferred by DTC activation request from the ICU). • Data of multiple channels can be transferred on a single activation source (chain transfer). • Either “executed when the counter is 0” or “always executed” can be selected for chain transfer.	• Channel transfer corresponding to the interrupt source is possible (transferred by DTC activation request from the ICU). • Data of multiple channels can be transferred on a single activation source (chain transfer). • Either “executed when the counter is 0” or “always executed” can be selected for chain transfer.
Transfer space	• 16 MB in short-address mode (areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh, excepting reserved areas) • 4 GB in full-address mode (area from 0000 0000h to FFFF FFFFh, excepting reserved areas)	• 16 MB in short-address mode (areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh, excepting reserved areas) • 4 GB in full-address mode (area from 0000 0000h to FFFF FFFFh, excepting reserved areas)
Data transfer units	• Single data: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data	• Single data: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data
CPU interrupt requests	• An interrupt request can be generated to the CPU on a DTC activation interrupt. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of a specified volume.	• An interrupt request can be generated to the CPU on a DTC activation interrupt. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of a specified volume.

Item	RX63N (DTCa)	RX65N (DTCb)
Event link activation	—	Event link request generated after one data transfer (or after one block transfer in case of block transfer operation).
Read skip	Reading of the transfer information can be skipped when the same transfer is repeated.	Reading of the transfer information can be skipped when the same transfer is repeated.
Write-back skip	When “fixed” is selected for the transfer source address or transfer destination address, write-back of non-updated transfer data can be omitted.	When “fixed” is selected for the transfer source address or transfer destination address, write-back of non-updated transfer data can be omitted.
Write-back disable	—	It is possible to disable write-back of transfer information.
Sequence transfer	—	A series of complicated transfers can be registered as a sequence. Any sequence can be selected by the transfer data and executed. • Only one trigger source can be set at a time. • Up to 256 sequences for a single trigger source • The data that is initially transferred in response to a transfer request determines a sequence • The whole sequence can be executed on a single request, or be suspended in the middle of the sequence and resumed on the next transfer request (division of sequence).
Displacement addition	—	Displacement can be added to the transfer source address (selectable in each set of transfer information).
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Table 2.27 Comparative Listing of Data Transfer Controller Registers

Register	Bit	RX63N (DTCa)	RX65N (DTCb)
MRA	WBDIS	—	Write-back disable bit
MRB	SQEND	—	Sequence transfer end bit
	INDX	—	Index table reference bit
MRC	—	—	DTC mode register C
DTCVBR	—	DTC vector base register (b31 to b0) Values written to the upper 4 bits are ignored, and the value of b27 is extended to these bits. The lower 12 bits are reserved, and their value is fixed at 0. Always write 0 to these bits. Valid settings are in the ranges 0000 0000h to 07FF F000h and F800 0000h to FFFF F000h, in 4 KB units.	DTC vector base register (b31 to b0) Values written to the upper 4 bits are ignored, and the value of b27 is extended to these bits. The lower 10 bits are reserved, and their value is fixed at 0. Always write 0 to these bits. Valid settings are in the ranges 0000 0000h to 07FF FC00h and F800 0000h to FFFF FC00h, in 1 KB units.
DTCIBR	—	—	DTC index table base register
DTCOR	—	—	DTC operation register
DTCSQE	—	—	DTC sequence transfer enable register
DTCDISP	—	—	DTC address displacement register

2.15 I/O Ports

Table 2.28 to Table 2.31 show a comparative overview of I/O ports specifications for each package, and Table 2.32 shows a comparative listing of the I/O port registers.

Table 2.28 Comparative Overview of I/O Ports on 177- and 176-Pin Packages

Port Symbol	RX63N (177-, 176-Pin)	RX65N (177-, 176-Pin)
PORT0	P00 to P03, P05, P07	P00 to P03, P05, P07
PORT1	P10 to P17	P10 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P57	P50 to P57
PORT6	P60 to P67	P60 to P67
PORT7	P70 to P77	P70 to P77
PORT8	P80 to P87	P80 to P87
PORT9	P90 to P97	P90 to P97
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7
PORTF	PF0 to PF5	PF0 to PF5
PORTG	PG0 to PG7	PG0 to PG7
PORTJ	PJ3, PJ5	PJ0 to PJ3, PJ5

Table 2.29 Comparative Overview of I/O Ports on 145- and 144-Pin Packages

Port Symbol	RX63N (145-, 144-Pin)	RX65N (145-, 144-Pin)
PORT0	P00 to P03, P05, P07	P00 to P03, P05, P07
PORT1	P12 to P17	P12 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P56	P50 to P56
PORT6	P60 to P67	P60 to P67
PORT7	P70 to P77	P70 to P77
PORT8	P80 to P83, P86, P87	P80 to P83, P86, P87
PORT9	P90 to P93	P90 to P93
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7
PORTF	PF5	PF5
PORTG	—	—
PORTJ	PJ3, PJ5	PJ3, PJ5

Table 2.30 Comparative Overview of I/O Ports on 100-Pin Packages

Port Symbol	RX63N (100-Pin)	RX65N (100-Pin)
PORT0	P05, P07	P05, P07
PORT1	P12 to P17	P12 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P55	P50 to P55
PORT6	—	—
PORT7	—	—
PORT8	—	—
PORT9	—	—
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7
PORTF	—	—
PORTG	—	—
PORTJ	PJ3	PJ3

Table 2.31 Comparative Overview of I/O Ports on 64-Pin Packages

Port Symbol	RX631 (64-Pin)*1		RX651 (64-Pin)*1
	LQFP	TFLGA	
PORT0	P05	P05	P05
PORT1	P14 to P17	P14 to P17	P12, P13, P16, P17
PORT2	P26, P27	P26, P27	P26, P27
PORT3	P30, P31, P35 to P37	P30, P31, P35 to P37	P30, P31, P34 to P37
PORT4	P40 to P44, P46	P40 to P44, P46	P40 to P43
PORT5	P54, P55	—	P53
PORT6	—	—	—
PORT7	—	—	—
PORT8	—	—	—
PORT9	—	—	—
PORTA	PA0, PA1, PA3, PA4, PA6	PA0, PA1, PA3, PA4, PA6	PA1, PA2, PA4, PA6, PA7
PORTB	PB0, PB1, PB3, PB5 to PB7	PB0, PB1, PB3, PB5 to PB7	PB5 to PB7
PORTC	PC2 to PC7	PC2 to PC6	PC0, PC1, PC4 to PC7
PORTD	—	—	PD2 to PD7
PORTE	PE0 to PE5	PE0 to PE5	PE0 to PE2, PE6, PE7
PORTF	—	—	—
PORTG	—	—	—
PORTJ	—	—	—

Note: 1. The RX63N and RX65N are not available in 64-pin package versions.

Table 2.32 Comparative Listing of I/O Port Registers

Register	Bit	RX63N	RX65N
ODR0	B3	—	PE1 output type select bit
PSRA*1	—	Port switching register A	—
PSRB*2	—	Port switching register B	—
DSCR2	—	—	Drive capacity control register 2

Notes: 1. This register exists only on the 64-pin package version of the RX631.
2. This register exists only on the 48-pin package version of the RX631.

2.16 Multi-Function Pin Controller

Table 2.33 shows a comparative listing of the multi-function pin controller registers.

Table 2.33 Comparative Listing of Multi-Function Pin Controller Registers

Register	Bit	RX63N	RX65N
PmnPFS	—	Refer to the user's manual for descriptions of the pin function control registers.	
PFBCR0	ADRHMS2	—	A18 to A20 output enable 2 bit
	BCLKO	—	BCLK forced output bit
	DH32E	D16 to D31 output enable bit	D16 to D31 output enable*1
	WR32BC32E	WR3#/BC3# output enable bit WR2#/BC2# output enable bit	WR3#/BC3# and WR2#/BC2# output enable bit*1
PFBCR1	WAITS[1:0]	WAIT select bits b1 b0 0 0: Configures P57 as the WAIT# input pin. 0 1: Configures P55 as the WAIT# input pin. 1 0: Configures PC5 as the WAIT# input pin. 1 1: Configures P51 as the WAIT# input pin.	WAIT select bits b1 b0 0 0: Setting invalid 0 1: Configures P55 as the WAIT# input pin. 1 0: Configures PC5 as the WAIT# input pin. 1 1: Configures P51 as the WAIT# input pin.
	ALES	—	ALE select bit
PFBCR2	—	—	External bus control register 2*1
PFBCR3	—	—	External bus control register 3*1
PFENET	PHYMODE (RX63N) PHYMODE0 (RX65N)	Ethernet mode setting bit	Ethernet channel 0 mode setting bit
PFUSB0	—	USB0 control register	—
PFUSB1	—	USB1 control register	—

Note: 1. Can be used for products with at least 1.5 MB of code flash memory.

2.17 16-Bit Timer Pulse Unit

Table 2.34 shows a comparative overview of 16-bit timer pulse unit specifications.

Table 2.34 Comparative Overview of 16-Bit Timer Pulse Unit

Item	RX63N (TPUa)	RX65N (TPUa)
Pulse input/output	Maximum 32	Maximum 16
Count clocks	7 and 8 clocks for each channel	7 and 8 clocks for each channel
Available operations	• Waveform output on compare match • Input capture function (noise filter setting available) • Counter-clearing operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Synchronous input/output for registers by counter synchronous operation • Maximum of 15-phase PWM output by combination with synchronous operation • Cascade connection operation available	• Waveform output on compare match • Input capture function (noise filter setting available) • Counter-clearing operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Synchronous input/output for registers by counter synchronous operation • Maximum of 15-phase PWM output by combination with synchronous operation • Cascade connection operation available
Buffer operation	• Channels 0, 3, 6, and 9 • Automatic transfer of register data	• Channels 0 and 3 • Automatic transfer of register data
Phase coefficient mode	Channels 1, 2, 4, 5, 7, 8, 10, and 11	Channels 1, 2, 4, and 5
Interrupt sources	52	26
Trigger generation	Programmable pulse generator (PPG) output trigger generation is available.	Programmable pulse generator (PPG) output trigger generation is available.
	A/D converter start triggers can be generated.	A/D converter start triggers can be generated.
Event link function (output)	—	Ability to output six event types to the ELC • Compare match A (TPU0 to TPU3) • Compare match B (TPU0 to TPU3) • Compare match C (TPU0, TPU3) • Compare match D (TPU0, TPU3) • Overflow (TPU0 to TPU3) • Underflow (TPU1, TPU2)
Event link function (input)	—	Any of the three operations in response to event input is possible. • Counter start (TPU0 to TPU3) • Counter restart (TPU0 to TPU3) • Input capture (TPU0 to TPU3)
Low power consumption function	Module stop state can be set.	Module stop state can be set.

2.18 Programmable Pulse Generator

Table 2.35 shows a comparative listing of the programmable pulse generator registers.

Table 2.35 Comparative Listing of the Programmable Pulse Generator Registers

Register	Bit	RX63N (PPG)	RX65N (PPG)
NDRH2	—	—	Next data register H2
NDRL2	—	—	Next data register L2

2.19 8-Bit Timer

Table 2.36 shows a comparative overview of 8-bit timer specifications, and Table 2.37 shows a comparative listing of the 8-bit timer registers.

Table 2.36 Comparative Overview of 8-Bit Timer

Item	RX63N (TMR)	RX65N (TMR)
Count clocks	• Frequency-divided clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock	• Frequency-divided clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock
Number of channels	(8 bits × 2 channels) × 2 units	(8 bits × 2 channels) × 2 units
Compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selectable among compare match A, compare match B, and external reset signal.	Selectable among compare match A, compare match B, and external reset signal.
Timer output	Output pulses with a user-defined duty cycle or PWM output	Output pulses with a user-defined duty cycle or PWM output
Cascading of two channels	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode • TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
Event link function (output)	—	Compare match A, compare match B, and overflow (TMR0 to TMR3)
Event link function (input)	—	Ability to perform one of three actions according to accepted event (1) Counter start (TMR0 to TMR3) (2) Event counter (TMR0 to TMR3) (3) Counter restart (TMR0 to TMR3)
DTC activation	The DTC can be activated by compare match A interrupts or compare match B interrupts.	The DTC can be activated by compare match A interrupts or compare match B interrupts.
Generation of trigger to start A/D converter	Compare match A of TMR0 or TMR2	Compare match A of TMR0 or TMR2
Generation of baud rate clock for SCI	Generation of baud rate clock for SCI	Generation of baud rate clock for SCI
Low power consumption function	Each unit can be placed in a module stop state.	Each unit can be placed in a module stop state.

Table 2.37 Comparative Listing of 8-Bit Timer Registers

Register	Bit	RX63N (TMR)	RX65N (TMR)
TCSTR	—	—	Time counter start register

2.20 Compare Match Timer

Table 2.38 shows a comparative overview of the compare match timer specifications.

Table 2.38 Comparative Overview of Compare Match Timer

Item	RX63N (CMT)	RX65N (CMT)
Count clocks	Four frequency-divided clocks One clock from among PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected individually for each channel.	Four frequency-divided clocks One clock from among PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected individually for each channel.
Interrupt	A compare match interrupt can be requested individually for each channel.	A compare match interrupt can be requested individually for each channel.
Event link function (output)	—	Event signal output at CMT1 compare match
Event link function (input)	—	• Support for linked operation of specified module • Support for CMT1 counter start, event counter, and count restart
Low power consumption function	Each unit can be placed in a module stop state.	Each unit can be placed in a module stop state.

2.21 Realtime Clock

Table 2.39 shows a comparative overview of the realtime clock specifications, and Table 2.40 shows a comparative listing of the realtime clock registers.

Table 2.39 Comparative Overview of Realtime Clock

Item	RX63N (RTCa)	RX65N (RTCd)
Count modes	Calendar count mode	Calendar count mode, binary count mode
Count source	Sub-clock (XCIN) or main clock (EXTAL)	Sub-clock (XCIN) or main clock (EXTAL)
Clock and calendar functions	• Calendar count mode — Year, month, date, day of the week, hours, minutes, and seconds are counted and represented in BCD format — Selection of 12- or 24-hour mode — 30-second adjustment (30 seconds or less are rounded down to 00 seconds, and 30 seconds or more are rounded up to one minute.) — Automatic leap year adjustment — Start/stop function — Binary display of digits below seconds (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, 64 Hz) — Time error adjustment function — Clock (1 Hz) output	• Calendar count mode — Year, month, date, day of the week, hours, minutes, and seconds are counted and represented in BCD format — Selection of 12- or 24-hour mode — 30-second adjustment (30 seconds or less are rounded down to 00 seconds, and 30 seconds or more are rounded up to one minute.) — Automatic leap year adjustment • Binary count mode — Count seconds in 32 bits, binary display • Common to both modes — Start/stop function — Binary display of digits below seconds (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, 64 Hz) — Time error adjustment function — Clock (1 Hz/64 Hz) output
Interrupt	• Alarm interrupt (ALM) Year, month, date, day of the week, hours, minutes, and seconds can be selected as conditions for the alarm interrupt. • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second can be selected as the interrupt period. • Carry interrupt (CUP) An interrupt is generated at either of the following timings — When a carry from the 64 Hz counter to the second counter is generated. — When the 64 Hz counter is changed and the R64CNT register is read at the same time.	• Alarm interrupt (ALM) Any of the following can be selected as conditions for the alarm interrupt: — Calendar count mode: Year, month, date, day of the week, hours, minutes, and seconds — Binary count mode: Each bit of 32-bit binary counter • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second can be selected as the interrupt period. • Carry interrupt (CUP) An interrupt is generated at either of the following timings — When a carry from the 64 Hz counter to the second counter is generated. — When the 64 Hz counter is changed and the R64CNT register is read at the same time.

Item	RX63N (RTCa)	RX65N (RTCd)
Interrupt	• Recovery from software standby mode or deep software standby mode can be performed by an alarm interrupt or periodic interrupt	• Recovery from software standby mode or deep software standby mode can be performed by an alarm interrupt or periodic interrupt
Time-capture function	Time capture using edge detection on the time capture event input pin is available. At each input event the month, date, hour, minute, and second is captured.	Time capture using edge detection on the time capture event input pin is available. At each input event the month, date, hour, minute, and second is captured, or the 32-bit counter value is captured.
Event link function	—	Periodic event output

Table 2.40 Comparative Listing of Realtime Clock Registers

Register	Bit	RX63N (RTCa)	RX65N (RTCd)
BCNT0*1	—	—	Binary counter 0
BCNT1*1	—	—	Binary counter 1
BCNT2*1	—	—	Binary counter 2
BCNT3*1	—	—	Binary counter 3
BCNT0AR*1	—	—	Binary counter 0 alarm register
BCNT1AR*1	—	—	Binary counter 1 alarm register
BCNT2AR*1	—	—	Binary counter 2 alarm register
BCNT3AR*1	—	—	Binary counter 3 alarm register
BCNT0AER*1	—	—	Binary counter 0 alarm enable register
BCNT1AER*1	—	—	Binary counter 1 alarm enable register
BCNT2AER*1	—	—	Binary counter 2 alarm enable register
BCNT3AER*1	—	—	Binary counter 3 alarm enable register
RCR1	RTCOS	—	RTCOUT output select bit
RCR2	CNTMD	—	Count mode select bit
BCNT0CPy*1	—	—	BCNT0 capture register y (y = 0 to 2)
BCNT1CPy*1	—	—	BCNT1 capture register y (y = 0 to 2)
BCNT2CPy*1	—	—	BCNT2 capture register y (y = 0 to 2)
BCNT3CPy*1	—	—	BCNT3 capture register y (y = 0 to 2)

Note: 1. In binary count mode

2.22 Watchdog Timer

Table 2.41 shows a comparative overview of the watchdog timer specifications, and Table 2.42 shows a comparative listing of the watchdog timer registers.

Table 2.41 Comparative Overview of Watchdog Timer

Item	RX63N (WDTA)	RX65N (WDTA)
Count source	Peripheral clock (PCLK)	Peripheral module clock (PCLK)
Clock division ratio	Divide by 4, 64, 128, 512, 2,048, or 8,192	Divide by 4, 64, 128, 512, 2,048, or 8,192
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Counting starts automatically after a reset (auto-start mode). • Counting is started (register start mode) by refreshing the counter (writing 00h and then FFh to the WDTRR register).	• Auto-start mode: Counting starts automatically after a reset. • Register start mode: Counting is started by refreshing the counter (writing 00h and then FFh to the WDTRR register).
Conditions for stopping the counter	• Reset (The down-counter and other registers return to their initial values.) • A counter underflows or a refresh error is generated. (auto-start mode: automatic, register start mode: refresh)	• Reset (The down-counter and other registers return to their initial values.) • Low power consumption state • Underflow or refresh error (register start mode only)
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods).	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods).
Reset output sources	• Down-counter underflow • Refresh outside the refresh-permitted period (refresh error)	• Down-counter underflow • Refresh outside the refresh-permitted period (refresh error)
Interrupt sources	Interrupt request output sources • Generation of a non-maskable interrupt (WUNI) by an underflow of the down-counter • Refresh outside the refresh-permitted period (refresh error)	Non-maskable interrupt/interrupt sources • Down-counter underflow • Refresh outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read by reading the WDTSR register.	The down-counter value can be read by reading the WDTSR register.

Table 2.42 Comparative Listing of Watchdog Timer Registers

Register	Bit	RX63N (WDTA)	RX65N (WDTA)
WDTRCR	RSTIRQS	Reset interrupt request selection bit 0: Non-maskable interrupt request output is enabled. 1: Reset output is enabled.	Reset interrupt request selection bit 0: Non-maskable interrupt request or interrupt request output is enabled.*1 1: Reset output is enabled.

Note: 1. A non-maskable interrupt is generated when the value of the NMIER.WDTEN bit is 1, and a maskable interrupt is generated when it is 0.

2.23 Independent Watchdog Timer

Table 2.43 shows a comparative overview of the independent watchdog timer specifications, and table 2.44 shows a comparative listing of the independent watchdog timer registers.

Table 2.43 Comparative Overview of Independent Watchdog Timer

Item	RX63N (IWDTa)	RX65N (IWDTa)
Count source	IWDT-dedicated clock (IWDTCLK)	IWDT-dedicated clock (IWDTCLK)
Clock division ratio	Division by 1, 16, 32, 64, 128, or 256	Division by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Counting starts automatically after a reset (auto-start mode). • Counting is started (register start mode) by refreshing the counter (writing 00h and then FFh to the IWDTRR register).	• Auto-start mode: Counting starts automatically after a reset. • Register start mode: Counting is started by refreshing the counter (writing 00h and then FFh to the IWDTRR register).
Conditions for stopping the counter	• Reset (The down-counter and other registers return to their initial values.) • A counter underflows or a refresh error is generated. Count restart (auto-start mode: count restarts automatically after a reset or a non-maskable interrupt request; register start mode: count restarts after the counter is refreshed)	• Reset (The down-counter and other registers return to their initial values.) • Low power consumption state (by means of register setting) • Underflow or refresh error (register start mode only)
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods).	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods).
Reset output sources	• Down-counter underflow • Refresh outside the refresh-permitted period (refresh error)	• Down-counter underflow • Refresh outside the refresh-permitted period (refresh error)
Interrupt sources	Interrupt request output sources • Generation of a non-maskable interrupt (WUNI) by an underflow of the down-counter • Refresh outside the refresh-permitted period (refresh error)	Non-maskable interrupt/interrupt sources • Down-counter underflow • Refresh outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read by reading the IWDTSR register.	The down-counter value can be read by reading the IWDTSR register.
Event link function (output)	—	• Down-counter underflow event output • Refresh error event output
Output signals (internal signals)	• Reset output • Interrupt request output • Sleep mode count stop control output	• Reset output • Interrupt request output • Sleep mode count stop control output

Item	RX63N (IWDTa)	RX65N (IWDTa)
Auto-start mode (controlled by option function select register 0 (OFS0))	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)
Register start mode (controlled by the IWDT registers)	• Selecting the clock frequency division ratio after a refresh (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)	• Selecting the clock frequency division ratio after a refresh (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)

Table 2.44 Comparative Listing of Independent Watchdog Timer Registers

Register	Bit	RX63N (IWDTa)	RX65N (IWDTa)
IWDTRCR	RSTIRQS	Reset interrupt request selection bit 0: Non-maskable interrupt request output is enabled. 1: Reset output is enabled.	Reset interrupt request selection bit 0: Non-maskable interrupt request or interrupt request output is enabled.*1 1: Reset output is enabled.

Note: 1. A non-maskable interrupt is generated when the value of the NMIER.IWDTEN bit is 1, and a maskable interrupt is generated when it is 0.

2.24 DMA Controller for The Ethernet Controller

Table 2.45 shows a comparative listing of the DMA controller for the ethernet controller registers.

Table 2.45 Comparative Listing of DMA Controller for The Ethernet Controller Registers

Register	Bit	RX63N (EDMAC)	RX65N (EDMACa)
EESR	ADE	Address error flag	—
EESIPR	ADEIP	Address error interrupt enable bit	—
TRSCER	CERFCE	CERF bit copy directive bit	—
	PRECE	PRE bit copy directive bit	—
	RTSFCE	RTSF bit copy directive bit	—
	RTLFCE	RTLF bit copy directive bit	—
	TROCE	TRO bit copy directive bit	—
	CDCE	CD bit copy directive bit	—
	DLCCE	DLC bit copy directive bit	—
	CNDCE	CND bit copy directive bit	—
FDR	RFD[4:0]	Receive FIFO size bits b4 b0 0 0 0 0 0: 256 bytes 0 0 0 0 1: 512 bytes 0 0 0 1 0: 768 bytes 0 0 0 1 1: 1,024 bytes 0 0 1 0 0: 1,280 bytes 0 0 1 0 1: 1,536 bytes 0 0 1 1 0: 1,792 bytes 0 0 1 1 1: 2,048 bytes Do not set to values other than the above.	Receive FIFO size bits b4 b0 0 0 1 1 1: 1,968 bytes Do not set to values other than the above.
	TFD[4:0]	Transmit FIFO size bits b12 b8 0 0 0 0 0: 256 bytes 0 0 0 0 1: 512 bytes 0 0 0 1 0: 768 bytes 0 0 0 1 1: 1,024 bytes 0 0 1 0 0: 1,280 bytes 0 0 1 0 1: 1,536 bytes 0 0 1 1 0: 1,792 bytes 0 0 1 1 1: 2,048 bytes Do not set to values other than the above.	Transmit FIFO size bits b12 b8 0 0 1 1 1: 2,048 bytes Do not set to values other than the above.
RMCR	RNC	Receive request bit non-reset mode bit	—

Register	Bit	RX63N (EDMAC)	RX65N (EDMACa)
FCFTR	RFDO[2:0]	Receive FIFO overflow BSY output threshold bits b2 b0 0 0 0: When 256 to 32 bytes of data is stored in the receive FIFO 0 0 1: When 512 to 32 bytes of data is stored in the receive FIFO . . 1 1 0: When 1,792 to 32 bytes of data is stored in the receive FIFO 1 1 1: When 2,048 to 64 bytes of data is stored in the receive FIFO	Receive FIFO data PAUSE output threshold bits b2 b0 0 0 0: When 256 to 32 bytes of data is stored in the receive FIFO 0 0 1: When 512 to 32 bytes of data is stored in the receive FIFO . . 1 1 0: When 1,792 to 32 bytes of data is stored in the receive FIFO 1 1 1: When 2,048 to 96 bytes of data is stored in the receive FIFO

2.25 USB 2.0 Host/Function Module

Table 2.46 shows a comparative overview of the USB 2.0 Host/Function module specifications, and Table 2.47 shows a comparative listing of the USB 2.0 Host/Function module registers.

Table 2.46 Comparative Overview of USB 2.0 Host/Function Module

Item	RX63N (USBa)	RX65N (USBb)
Ports	2	1
Features	• Integrated USB Device Controller (UDC) and transceiver for USB 2.0 — USB0: Support for Host controller, Function controller, and on-the-go (OTG) functionality — USB1: Support for Function controller • Software can switch between the Host controller and Function controller modes. • Self-power mode or bus-power mode can be selected.	• Integrated USB Device Controller (UDC) and transceiver for USB 2.0 — Support for Host controller, Function controller, and on-the-go (OTG) functionality • Software can switch between the Host controller and Function controller modes. • Self-power mode or bus-power mode can be selected.
	When Host controller operation is selected: • Full-speed transfer (12 Mbps) is supported. • Automatic scheduling of SOF and packet transmissions • Transfer interval setting function for isochronous and interrupt transfers • Communication with multiple peripheral devices connected via a single hub	When Host controller operation is selected: • Full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) are supported. • Automatic scheduling of SOF and packet transmissions • Transfer interval setting function for isochronous and interrupt transfers • Communication with multiple peripheral devices connected via a single hub
	When Function controller operation is selected: • Support for full-speed transfer (12 Mbps) • Control transfer stage control function • Device state control function • Auto response function for SET_ADDRESS requests • SOF interpolation function	When Function controller operation is selected: • Support for full-speed transfer (12 Mbps)*1 • Control transfer stage control function • Device state control function • Auto response function for SET_ADDRESS requests • SOF interpolation function
Communication data transfer types	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer
Pipe configuration	• Buffer memory for USB communication is provided. • Up to ten pipes can be selected (including the default control pipe). • Endpoint numbers can be assigned flexibly to PIPE1 to PIPE9.	• Buffer memory for USB communication is provided. • Up to ten pipes can be selected (including the default control pipe). • Endpoint numbers can be assigned flexibly to PIPE1 to PIPE9.

Item	RX63N (USBa)	RX65N (USBb)
Pipe configuration	Transfer conditions that can be set for each pipe: • PIPE0: Control transfer only (default control pipe: DPC), buffer size: 8, 16, 32, and 64 bytes (single buffer) • PIPE1 and PIPE2: Bulk transfer or isochronous transfer, bulk transfer buffer size: 8, 16, 32, and 64 bytes (support for double buffer setting), isochronous transfer buffer size: 1 to 256 bytes (support for double buffer setting) • PIPE3 to PIPE5: Bulk transfer only, buffer size: 8, 16, 32, and 64 bytes (support for double buffer setting) • PIPE6 to PIPE9: Interrupt transfer only: buffer size: 1 to 64 bytes (single buffer)	Transfer conditions that can be set for each pipe: • PIPE0: Control transfer only (default control pipe: DPC), buffer size: 64 bytes (single buffer) • PIPE1 and PIPE2: Bulk transfer or isochronous transfer, bulk transfer buffer size: 64 bytes (support for double buffer setting), isochronous transfer buffer size: 256 bytes (support for double buffer setting) • PIPE3 to PIPE5: Bulk transfer only, buffer size: 64 bytes (support for double buffer setting) • PIPE6 to PIPE9: Interrupt transfer only: buffer size: 64 bytes (single buffer)
Other functions	• Reception end function using transaction count • Function that changes the BRDY interrupt event notification timing (BFRE) • Function that automatically clears the buffer memory after the data for the pipe specified at the DnFIFO (n = 0 or 1) port has been read (DCLRM) • NAK setting function for response PID generated by end of transfer (SHTNAK)	• Reception end function using transaction count • Function that changes the BRDY interrupt event notification timing (BFRE) • Function that automatically clears the buffer memory after the data for the pipe specified at the DnFIFO (n = 0 or 1) port has been read (DCLRM) • NAK setting function for response PID generated by end of transfer (SHTNAK) • On-chip DP/DM pull-up and pull-down resistors
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Note: 1. Low-speed transfer (1.5 Mbps) is not supported when Function controller operation is selected.

Table 2.47 Comparative Listing of USB 2.0 Host/Function Module Registers

Register	Bit	RX63N (USBa)	RX65N (USBb)
SYSSTS0	SOFEA	—	SOF active monitor flag when the host controller is selected
SOFCFG	TRNENSEL	—	Transaction-enabled time select bit
DEVADDn (n = 0 to 5)	USBSPD [1:0]	Transfer speed of communication target device bits b7 b6 0 0: DEVADDn register is not used. 0 1: Setting prohibited. 1 0: Full speed 1 1: Setting prohibited.	Transfer speed of communication target device bits b7 b6 0 0: DEVADDn register is not used. 0 1: Low speed 1 0: Full speed 1 1: Setting prohibited.
PHYSLEW	—	—	PHY cross point adjustment register
DPUSR0R	RPUE0	—	D+ pull-up resistor control bit
	DRPD0	—	D+/D− pull-down resistor control bit
	SRPC1	USB1 single end receiver control bit	—
	FIXPHY1	USB1 transceiver output fix bit	—
	DP1	USB1 DP input	—
	DM1	USB1 DM input	—
	DVBSTS1	USB1 VBUS input	—
DPUSR1R	DPINTE1	USB1 DP interrupt enable/clear bit	—
	DMINTE1	USB1 DM interrupt enable/clear bit	—
	DVBSE1	USB1 VBUS interrupt enable/clear bit	—
	DPINT1	USB1 DP interrupt source recovery bit	—
	DMINT1	USB1 DM interrupt source recovery bit	—
	DVBINT1	USB1 VBUS interrupt source recovery bit	—

2.26 Serial Communication Interface

The RX63N Group has 13 independent serial communications interface (SCI) channels (SCIc: 12 channels, SCId: 1 channel).

The RX65N Group has 13 independent serial communications interface (SCI) channels (SCIg: 10 channels, SCIi: 2 channels, SCIh: 1 channel).

Table 2.48 shows a comparative overview of the SCIc and SCIg specifications, Table 2.49 shows a comparative overview of the SCIi specifications, Table 2.50 shows a comparative overview of the SCId and SCIh specifications, Table 2.51 shows a comparative overview of the SCI channel specifications, and Table 2.52 shows a comparative listing of the serial communications interface registers.

Table 2.48 Comparative Overview of SCIc and SCIg Specifications

Item		RX63N (SCIc)	RX65N (SCIg)
Number of channels		12 channels	10 channels
Serial communication modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator. (The settable bit rates will differ due to differences in the electrical characteristics. See the user's manual for details.)
Full-duplex communication		• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable between LSB-first or MSB-first transfer.*1	Selectable between LSB-first or MSB-first transfer.*1
Interrupt sources		Transmit end, transmit data empty, receive data full, receive error, completion of generation of start condition, restart condition, or stop condition (simple I²C mode)	Transmit end, transmit data empty, receive data full, receive error, completion of generation of start condition, restart condition, or stop condition (simple I²C mode)
Low power consumption function		The module stop state can be specified for each channel.	The module stop state can be specified for each channel.
Asynchronous mode	Data length	7 or 8 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	The CTSn# and RTSn# pins can be used to control transmission and reception.	The CTSn# and RTSn# pins can be used to control transmission and reception.
	Start bit detection	Low level detection	Selectable between low level and falling edge.

Item		RX63N (SCIc)	RX65N (SCIg)
Synchronous mode	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.
	Clock source	An internal or external clock can be selected. Transfer rate clock input from the TMR can be used (SCI5 and SCI6).	An internal or external clock can be selected. Transfer rate clock input from the TMR can be used (SCI5 and SCI6).
	Double-speed mode	—	Baud rate generator double-speed mode is selectable.
	Multi-processor communication function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate on-chip digital noise filters.	The signal paths from input on the RXDn pins incorporate on-chip digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	The CTSn# and RTSn# pins can be used to control transmission and reception.	The CTSn# and RTSn# pins can be used to control transmission and reception.
Smart card interface mode	Error processing	An error signal can be transmitted automatically when a parity error is detected during reception.	An error signal can be transmitted automatically when a parity error is detected during reception.
		Data can be retransmitted automatically when an error signal is received during transmission.	Data can be retransmitted automatically when an error signal is received during transmission.
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	I^2C bus format	I^2C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer rate	Fast mode is supported.	Fast mode is supported.
	Noise canceler	The signal paths from input on the SSCLn and SSDAn pins incorporate on-chip digital noise filters, and the noise cancellation bandwidth is adjustable.	The signal paths from input on the SSCLn and SSDAn pins incorporate on-chip digital noise filters, and the noise cancellation bandwidth is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Error detection	Overrun error	Overrun error
	SS input pin function	Applying a high-level signal to the SSn# pin causes the output pins to enter the high-impedance state.	Applying a high-level signal to the SSn# pin causes the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.
Bit rate modulation function		—	On-chip baud rate generator output correction can reduce errors.
Event link function		—	Error (receive error, error signal detection) event output
		—	Receive data full event output
		—	Transmit data empty event output
		—	Transmit end event output

Note: 1. Only MSB-first is available in simple I^2C mode.

Table 2.49 Comparative Overview of SCIi Specifications

Item		RX63N (—)	RX65N (SCIi)
Number of channels		—	2 channels
Serial communication modes		—	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		—	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		—	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		—	Selectable between LSB-first or MSB-first transfer.*1
Interrupt sources		—	Transmit end, transmit data empty, receive data full, receive error, receive data ready, and data match, completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)
Low power consumption function		—	The module stop state can be specified for each channel.
Asynchronous mode	Data length	—	7, 8, or 9 bits
	Transmission stop bits	—	1 or 2 bits
	Parity	—	Even parity, odd parity, or no parity
	Receive error detection	—	Parity, overrun, and framing errors
	Hardware flow control	—	The CTSn# and RTSn# pins can be used to control transmission and reception.
	Transmit/ receive FIFO	—	Usable as a FIFO with 16 transmit stages and 16 receive stages.
	Data match detection	—	Compares receive data and comparison data, and generates interrupt when they are matched
	Start bit detection	—	Selectable between low level and falling edge.
	Break detection	—	When a framing error occurs, a break can be detected by reading the level of the RXDn pin directly or reading the SPTR.RXDMON flag.
	Clock source	—	An internal or external clock can be selected.
	Double-speed mode	—	Baud rate generator double-speed mode is selectable.
	Multi-processor communication function	—	Serial communication among multiple processors

Item		RX63N (—)	RX65N (SCIi)
Asynchronous mode	Noise cancellation	—	The signal paths from input on the RXDn pins incorporate on-chip digital noise filters.
Clock synchronous mode	Data length	—	8 bits
	Receive error detection	—	Overrun error
	Hardware flow control	—	The CTSn# and RTSn# pins can be used to control transmission and reception.
	Transmit/receive FIFO	—	Usable as a FIFO with 16 transmit stages and 16 receive stages.
Smart card interface mode	Error processing	—	An error signal can be transmitted automatically when a parity error is detected during reception.
		—	Data can be retransmitted automatically when an error signal is received during transmission.
	Data type	—	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	—	I^2C bus format
	Operating mode	—	Master (single-master operation only)
	Transfer rate	—	Fast mode is supported.
	Noise canceler	—	The signal paths from input on the SSCLn and SSDAn pins incorporate on-chip digital noise filters, and the noise cancellation bandwidth is adjustable.
Simple SPI mode	Data length	—	8 bits
	Error detection	—	Overrun error
	SS input pin function	—	Applying a high-level signal to the SSn# pin causes the output pins to enter the high-impedance state.
	Clock settings	—	Four kinds of settings for clock phase and clock polarity are selectable.
Bit rate modulation function		—	On-chip baud rate generator output correction can reduce errors.

Table 2.50 Comparative Overview of SCId and SCIh Specifications

Item		RX63N (SCId)	RX65N (SCIh)
Number of channels		1 channel	1 channel
Serial communication modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable between LSB-first or MSB-first transfer.*1	Selectable between LSB-first or MSB-first transfer.*1
Interrupt sources		Transmit end, transmit data empty, receive data full, receive error, completion of generation of start condition, restart condition, or stop condition (simple I²C mode)	Transmit end, transmit data empty, receive data full, receive error, completion of generation of start condition, restart condition, or stop condition (simple I²C mode)
Low power consumption function		Module stop state can be set.	Module stop state can be set.
Asynchronous mode	Data length	7 or 8 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	The CTSn# and RTSn# pins can be used to control transmission and reception.	The CTSn# and RTSn# pins can be used to control transmission and reception.
	Start bit detection	Low level detection	Selectable between low level and falling edge.
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.
	Clock source	An internal or external clock can be selected. Transfer rate clock input from the TMR can be used.	An internal or external clock can be selected. Transfer rate clock input from the TMR can be used.
	Double-speed mode	—	Baud rate generator double-speed mode is selectable.
	Multi-processor communication function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate on-chip digital noise filters.	The signal paths from input on the RXDn pins incorporate on-chip digital noise filters.

Item		RX63N (SCId)	RX65N (SCIh)
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	The CTSn# and RTSn# pins can be used to control transmission and reception.	The CTSn# and RTSn# pins can be used to control transmission and reception.
Smart card interface mode	Error processing	An error signal can be transmitted automatically when a parity error is detected during reception.	An error signal can be transmitted automatically when a parity error is detected during reception.
		Data can be retransmitted automatically when an error signal is received during transmission.	Data can be retransmitted automatically when an error signal is received during transmission.
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	I^2C bus format	I^2C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer speed	Fast mode is supported.	Fast mode is supported.
	Noise canceler	The signal paths from input on the SSCLn and SSDAn pins incorporate on-chip digital noise filters, and the noise cancellation bandwidth is adjustable.	The signal paths from input on the SSCLn and SSDAn pins incorporate on-chip digital noise filters, and the noise cancellation bandwidth is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Error detection	Overrun error	Overrun error
	SS input pin function	Applying a high-level signal to the SSn# pin causes the output pins to enter the high-impedance state.	Applying a high-level signal to the SSn# pin causes the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.
Extended serial mode	Start frame transmission	• Output of the break field low width and generation of an interrupt on detection • Detection of bus collisions and the generation of interrupts on detection	• Output of the break field low width and generation of an interrupt on detection • Detection of bus collisions and the generation of interrupts on detection

Item		RX63N (SCId)	RX65N (SCIh)
Extended serial mode	Start frame reception	• Detection of the break field low width and generation of an interrupt on detection • Comparison of data in control fields 0 and 1 and generation of an interrupt when the two match • Two kinds of data for comparison (primary and secondary) can be set in control field 1. • A priority interrupt bit can be set in control field 1. • Support for handling of start frames that do not include a break field • Support for handling of start frames that do not include control field 0 • Function for measuring bit rates	• Detection of the break field low width and generation of an interrupt on detection • Comparison of data in control fields 0 and 1 and generation of an interrupt when the two match • Two kinds of data for comparison (primary and secondary) can be set in control field 1. • A priority interrupt bit can be set in control field 1. • Support for handling of start frames that do not include a break field • Support for handling of start frames that do not include control field 0 • Function for measuring bit rates
	I/O control functions	• Selectable polarity for TXDX12 and RXDX12 signals • Ability to enable digital filter function for RXDX12 • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Selectable timing for the sampling of data received through RXDX12 • Signals received on RXDX12 can be passed through to SCIc when the extended serial mode control section is off.	• Selectable polarity for TXDX12 and RXDX12 signals • Ability to enable digital filter function for RXDX12 • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Selectable timing for the sampling of data received through RXDX12 • Signals received on RXDX12 can be passed through to SCIg when the extended serial mode control section is off.
	Timer function	Usable as a reloading timer	Usable as a reloading timer
Bit rate modulation function		—	On-chip baud rate generator output correction can reduce errors.

Note: 1. Only MSB-first is available in simple I^2C mode.

Table 2.51 Comparative Overview of SCI Channel Specifications

Item	RX63N (SCIc, SCId)	RX65N (SCIg, SCIi, SCIh)
Synchronous mode	SCI0 to SCI12	SCI0 to SCI12
Clock synchronous mode	SCI0 to SCI12	SCI0 to SCI12
Smart card interface mode	SCI0 to SCI12	SCI0 to SCI12
Simple I^2C mode	SCI0 to SCI12	SCI0 to SCI12
Simple SPI mode	SCI0 to SCI12	SCI0 to SCI12
Extended serial mode	SCI12	SCI12
TMR clock input	SCI5, SCI6, SCI12	SCI5, SCI6, SCI12
Event link function	—	SCI5
FIFO mode	—	SCI10, SCI11
Data match detection	—	SCI10, SCI11

Table 2.52 Comparative Listing of Serial Communication Interface Registers

Register	Bit	RX63N (SCIc, SCId)	RX65N (SCIg, SCIi, SCIh)
RDRH	—	—	Receive data register H
RDRL	—	—	Receive data register L
RDRHL	—	—	Receive data register HL
FRDR	—	—	Receive FIFO data register
TDRH	—	—	Transmit data register H
TDRL	—	—	Transmit data register L
TDRHL	—	—	Transmit data register HL
FTDR	—	—	Transmit FIFO data register
SMR	CHR	Character length bit (Valid only in asynchronous mode) 0: Selects 8 bits as the data length for transmission and reception 1: Selects 7 bits as the data length for transmission and reception	Character length bit (Valid only in asynchronous mode) Selection is made in combination with the SCMR.CHR1 bit. CHR1CHR 0 0: Selects 9 bits as the data length for transmission and reception 0 1: Selects 9 bits as the data length for transmission and reception 1 0: Selects 8 bits as the data length for transmission and reception 1 1: Selects 7 bits as the data length for transmission and reception
SSRFIFO	—	—	Serial status register*1
SCMR	CHR1	—	Character length bit 1
MDDR	—	—	Modulation duty register

Register	Bit	RX63N (SCIc, SCId)	RX65N (SCIg, SCIi, SCIh)
SEMR	BRME	—	Bit rate modulation enable bit
	BGDM	—	Baud rate generator double-speed mode select bit
	RXDESEL	—	Asynchronous start bit edge detection select bit
FCR	—	—	FIFO control register
FDR	—	—	FIFO data count register
LSR	—	—	Line status register
CDR	—	—	Comparison data register
DCCR	—	—	Data comparison control register
SPTR	—	—	Serial port register
CR2	BCCS[1:0]	Bus collision detection clock select bits b5 b4 0 0: SCI base clock 0 1: SCI base clock frequency divided by 2 1 0: SCI base clock frequency divided by 4 1 1: Setting prohibited.	Bus collision detection clock select bits • When SEMR.BGDM bit = 0, or SEMR.BGDM bit = 1 and SMR.CKS[1.0] bits = other than 00b b5 b4 0 0: SCI base clock 0 1: SCI base clock frequency divided by 2 1 0: SCI base clock frequency divided by 4 1 1: Setting prohibited. • When SEMR.BGDM bit = 1 and SMR.CKS[1.0] bits = 00b b5 b4 0 0: SCI base clock frequency divided by 2 0 1: SCI base clock frequency divided by 4 1 0: Setting prohibited. 1 1: Setting prohibited.

Note: 1. Non-smart card interface mode and FIFO mode (SCMR.SMIF = 0 and FCR.FM = 1)

2.27 I²C bus Interface

Table 2.53 shows a comparative overview of the I²C bus interface specifications, and Table 2.54 shows a comparative listing of the I²C bus interface registers.

Table 2.53 Comparative Overview of I²C Bus Interface

Item	RX63N (RIIC)	RX65N (RIICa)
Number of channels	4 channels	2 channels / 3 channels*1
Communication format	• I²C bus format or SMBus format • Selectable between master mode or slave mode. • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate	• I²C bus format or SMBus format • Selectable between master mode or slave mode. • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate
Transfer speed	Fast mode is supported.	Fast mode is supported.
SCL clock	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%.	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%.
Issuing and detection conditions	Start, restart, and stop conditions are generated automatically. Start conditions (including restart conditions) and stop conditions are detectable.	Start, restart, and stop conditions are generated automatically. Start conditions (including restart conditions) and stop conditions are detectable.
Slave addresses	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.
Acknowledgement	• For transmission, the acknowledge bit is loaded automatically. — Transfer of the next data for transmission can be suspended automatically on reception of a not-acknowledge bit. • For reception, the acknowledge bit is transmitted automatically. — If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.	• For transmission, the acknowledge bit is loaded automatically. — Transfer of the next data for transmission can be suspended automatically on reception of a not-acknowledge bit. • For reception, the acknowledge bit is transmitted automatically. — If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.
Wait function	For reception, the following wait periods can be obtained by holding the SCL clock at the low level: • Wait between the eighth and ninth clock cycles • Wait between the ninth and first clock cycles (wait function)	For reception, the following wait periods can be obtained by holding the SCL clock at the low level: • Wait between the eighth and ninth clock cycles • Wait between the ninth and first clock cycles
SDA output delay function	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.

Item	RX63N (RIIC)	RX65N (RIICa)
Arbitration	• Multi-master support — Operation to synchronize the SCL clock in cases of conflict with the SCL clock from another master is possible. — When issuing a start condition, loss of arbitration is detected by testing for non-matching of the signals for the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching of transmit data. • Loss of arbitration due to detection of a start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the signals for the SDA line not matching is detectable. • Loss of arbitration due to non-matching of data is detectable in slave transmission.	• Multi-master support — Operation to synchronize the SCL clock in cases of conflict with the SCL clock from another master is possible. — When issuing a start condition, loss of arbitration is detected by testing for non-matching of the signals for the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching of transmit data. • Loss of arbitration due to detection of a start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the signals for the SDA line not matching is detectable. • Loss of arbitration due to non-matching of data is detectable in slave transmission.
Timeout detection function	The internal timeout function is capable of detecting long-interval stop of the SCL clock.	The internal timeout function is capable of detecting long-interval stop of the SCL clock.
Noise canceler	The interface incorporates digital noise filters for both the SCL and SDA inputs, and the bandwidth for noise cancellation by the filters is adjustable by software.	The interface incorporates digital noise filters for both the SCL and SDA inputs, and the bandwidth for noise cancellation by the filters is adjustable by software.
Interrupt sources	Four sources • Communication error or event occurrence Arbitration detection, NACK detection, timeout detection, start condition detection (including restart condition), stop condition detection • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end	Four sources • Communication error or event occurrence Arbitration detection, NACK detection, timeout detection, start condition detection (including restart condition), stop condition detection • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end
Low power consumption function	Module stop state can be set.	Module stop state can be set.
Event link function	—	• Communication error/communication event generation • Receive data full • Transmit data empty • Transmit end

Note: 1. Can be used for products with at least 1.5 MB of code flash memory. However, two channels on 64-pin versions.

Table 2.54 Comparative Listing of I²C Bus Interface Registers

Register	Bit	RX63N (RIIC)	RX65N (RIICa)
ICMR2	TMWE	Timeout internal counter write enable bit	—
TMOCNTL	—	Timeout internal counter L	—
TMOCNTU	—	Timeout internal counter U	—

2.28 CAN Module

Table 2.55 shows a comparative overview of the CAN module specifications.

Table 2.55 Comparative Overview of CAN Module

Item	RX63N (CAN)	RX65N (CAN)
Number of channels	3 channels	2 channels
Protocol	ISO 11898-1 compliant (standard and extended frames)	ISO 11898-1 compliant (standard and extended frames)
Bit rate	Programmable bit rate below 1 Mbps (fCAN ≥ 8 MHz) fCAN: CAN clock source	Programmable bit rate below 1 Mbps (fCAN ≥ 8 MHz) fCAN: CAN clock source
Message box	32 mailboxes: Two selectable mailbox modes • Normal mailbox mode: 32 mailboxes can be configured for either transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for either transmission or reception. Of the other mailboxes, four FIFO stages can be configured for transmission and four FIFO stages for reception.	32 mailboxes: Two selectable mailbox modes • Normal mailbox mode: 32 mailboxes can be configured for either transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for either transmission or reception. Of the other mailboxes, four FIFO stages can be configured for transmission and four FIFO stages for reception.
Reception	• Data frames and remote frames can be received. • Selectable receiving ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot reception function • Selectable between overwrite mode (messages overwritten) and overrun mode (messages discarded) • Reception-complete interrupt can be individually enabled or disabled for each mailbox.	• Data frames and remote frames can be received. • Selectable receiving ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot reception function • Selectable between overwrite mode (messages overwritten) and overrun mode (messages discarded) • Reception-complete interrupt can be individually enabled or disabled for each mailbox.
Acceptance filter	• Eight acceptance masks (one mask for every four mailboxes) • The mask can be individually enabled or disabled for each mailbox.	• Eight acceptance masks (one mask for every four mailboxes) • The mask can be individually enabled or disabled for each mailbox.

Item	RX63N (CAN)	RX65N (CAN)
Transmission	• Data frames and remote frames can be transmitted. • Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot transmission function • Selectable between ID priority mode and mailbox number priority mode • Transmission requests can be aborted. (Completion of abort can be confirmed with a flag.) • Transmission-complete interrupt can be individually enabled or disabled for each mailbox.	• Data frames and remote frames can be transmitted. • Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot transmission function • Selectable between ID priority mode and mailbox number priority mode • Transmission requests can be aborted. (Completion of abort can be confirmed with a flag.) • Transmission-complete interrupt can be individually enabled or disabled for each mailbox.
Mode transition for bus-off recovery	The mode transition for recovery from the bus-off state can be selected. • ISO 11898-1 compliant • Automatic transition to CAN halt mode at bus-off start • Automatic transition to CAN halt mode at bus-off end • Transition to CAN halt mode by a program • Transition to error-active state by a program	The mode transition for recovery from the bus-off state can be selected. • ISO 11898-1 compliant • Automatic transition to CAN halt mode at bus-off start • Automatic transition to CAN halt mode at bus-off end • Transition to CAN halt mode by a program • Transition to error-active state by a program
Error status monitoring	• CAN bus errors (stack error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored. • Transition to error states can be detected (error-warning, error-passive, bus-off start, and bus-off recovery). • The error counters can be read.	• CAN bus errors (stack error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored. • Transition to error states can be detected (error-warning, error-passive, bus-off start, and bus-off recovery). • The error counters can be read.
Time stamp function	• Time stamp function using a 16-bit counter • The reference clock can be selected from 1-, 2-, 4- and 8-bit time periods.	• Time stamp function using a 16-bit counter • The reference clock can be selected from 1-, 2-, 4- and 8-bit time periods.
Interrupt function	Five interrupt sources (reception complete, transmission complete, receive FIFO, transmit FIFO, and error interrupt)	Five interrupt sources (reception complete, transmission complete, receive FIFO, transmit FIFO, and error interrupt)
CAN sleep mode	Current consumption can be reduced by stopping the CAN clock.	Current consumption can be reduced by stopping the CAN clock.
Software support units	Three software support units: • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support	Three software support units: • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support
CAN clock source	Peripheral module clock (PCLKB), CANMCLK	Peripheral module clock (PCLKB), CANMCLK

Item	RX63N (CAN)	RX65N (CAN)
Test mode	Three test modes for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback)	Three test modes for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback)
Low power consumption function	Module stop state can be set.	Module stop state can be set.

2.29 Serial Peripheral Interface

Table 2.56 shows a comparative overview of the serial peripheral interface specifications, and Table 2.57 shows a comparative listing of the serial peripheral interface registers.

Table 2.56 Comparative Overview of Serial Peripheral Interface

Item	RX63N (RSPI)	RX65N (RSPIc)
Number of channels	3 channels	3 channels
RSPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communication through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK is supported. • Switching of the phase of RSPCK is supported.	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communication through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK is supported. • Switching of the phase of RSPCK is supported.
Data format	• Selectable between MSB-first and LSB-first. • Transfer bit length is selectable among 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (with each frame consisting of up to 32 bits).	• Selectable between MSB-first and LSB-first. • Transfer bit length is selectable among 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (with each frame consisting of up to 32 bits). • Ability to swap transmit data and receive data in byte units
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from 2 to 4,096). • In slave mode, the minimum PCLK clock divided by 8 can be input as RSPCK (the maximum frequency of RSPCK is PCLK divided by 8). Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from 2 to 4,096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is PCLK divided by 4). Width at high level: 2 cycles of PCLK; width at low level: 2 cycles of PCLK
Buffer configuration	• The transmit and receive buffers have a double buffer configuration. • The transmit and receive buffers are each 128 bits in size.	• The transmit and receive buffers have a double buffer configuration. • The transmit and receive buffers are each 128 bits in size.

Item	RX63N (RSPI)	RX65N (RSPIc)
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection When master receive and the RSPCK auto-stop function are enabled, the transfer clock stops at the point in time when overrun error detection occurs, so no overrun error is generated. • Parity error detection • Underrun error detection
SSL control function	• Four SSL signals (SSLn0 to SSLn3) for each channel • In single-master mode, SSLn0 to SSLn3 signals are output. • In multi-master mode: SSLn0 signal is input, and SSLn1 to SSLn3 signals are either output or unused. • In slave mode: SSLn0 signal is input, and SSLn1 to SSLn3 signals are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • SSL polarity-change function	• Four SSL pins (SSLn0 to SSLn3) for each channel • In single-master mode, SSLn0 to SSLn3 pins are output. • In multi-master mode: SSLn0 pin is input, and SSLn1 to SSLn3 pins are either output or unused. • In slave mode: SSLn0 pin is input, and SSLn1 to SSLn3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • SSL polarity-change function

Item	RX63N (RSPI)	RX65N (RSPIc)
Control in master transfer	• Transfers of up to eight commands can be performed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, LSB/MSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value when SSL is negated can be specified.	• Transfers of up to eight commands can be performed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, LSB/MSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value when SSL is negated can be specified. • RSPCK auto-stop function
Interrupt sources	• Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, parity error) • RSPI idle interrupt (RSPI idle)	• Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, underrun, parity error) • RSPI idle interrupt (RSPI idle)
Event link function (output)	—	The following events can be output to the event link controller (RSPI0): • Receive buffer run event signal • Transmit buffer empty event signal • Mode fault, overrun, underrun, or parity error event signal • RSPI idle event signal • Transmit end event signal
Other functions	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode function	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode function
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Table 2.57 Comparative Listing of Serial Peripheral Interface Registers

Register	Bit	RX63N (RSPI)	RX65N (RSPIc)
SPSR	MODF	Mode fault error flag 0: No mode fault error occurred 1: A mode fault error occurred	Mode fault error flag 0: No mode fault error occurred, no underrun error occurred. 1: A mode fault error occurred, an underrun error occurred.
	UDRF	—	Underrun error flag
	SPTEF	—	Transmit buffer empty flag
	SPRF	—	Receive buffer full flag
SPDR	—	RSPI data register Possible access sizes: • Longword access (SPDCR.SPLW = 1) • Word access (SPDCR.SPLW = 0)	RSPI data register Possible access sizes: • Longword access (SPDCR.SPLW = 1, SPBYTE = 0) • Word access (SPDCR.SPLW = 0, SPBYTE = 0) • Byte access (SPDCR.SPBYT = 1)

SPDCR	SPBYT	—	RSPI byte access specification bit
SPCR2	SCKASE	—	RSPCK auto-stop function enable bit
SPDCR2	—	—	RSPI data control register 2

2.30 CRC Calculator

Table 2.58 shows a comparative overview of the CRC calculator specifications, and Table 2.59 shows a comparative listing of the CRC calculator registers.

Table 2.58 Comparative Overview of CRC Calculator

Item	RX63N (CRC)	RX65N (CRCA)
Data size	8 or 16 bits	8 or 32 bits
Data for CRC calculation	• 8- or 16-bit data size: CRC code generated for 8n bits of data (n = natural number)	• 8-bit data size: CRC code generated for 8n bits of data (n = natural number) • 32-bit data size: CRC code generated for 32n bits of data (n = natural number)
CRC processor unit	• Operation executed on eight bits in parallel	• Operation executed on eight bits in parallel • Operation executed on 32 bits in parallel
CRC generating polynomial	One of three generating polynomials selectable: • 8-bit CRC $X^8 + X^2 + X + 1$ • 16-bit CRC $X^{16} + X^{15} + X^2 + 1$ $X^{16} + X^{12} + X^5 + 1$	One of five generating polynomials selectable: • 8-bit CRC $X^8 + X^2 + X + 1$ • 16-bit CRC $X^{16} + X^{15} + X^2 + 1$ $X^{16} + X^{12} + X^5 + 1$ • 32-bit CRC $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$
CRC calculation switching	The order of the bits produced by CRC calculation can be switched for LSB first or MSB first communication	The order of the bits produced by CRC calculation can be switched for LSB first or MSB first communication
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Table 2.59 Comparative Listing of CRC Calculator Registers

Register	Bit	RX63N (CRC)	RX65N (CRCA)
CRCCR	GPS	CRC generating polynomial switching bits (b1 and b0)	CRC generating polynomial switching bits (b2 to b0)
	LMS	CRC calculation switching bit (b2)	CRC calculation switching bit (b6)
CRCDIR	—	• When generating 16-bit or 8-bit CRCs CRC data input register (b7 to b0)	• When generating 32-bit CRCs CRC data input register (b31 to b0) • When generating 16-bit or 8-bit CRCs CRC data input register (b7 to b0)
CRCDOR	—	• When generating 16-bit CRCs CRC data output register (b15 to b0) The bottom byte (b7 to b0) is used when generating 8-bit CRCs.	• When generating 32-bit CRCs CRC data output register (b31 to b0) • When generating 16-bit CRCs CRC data output register (b15 to b0) • When generating 8-bit CRCs CRC data output register (b7 to b0) All access the same address.

2.31 Parallel Data Capture Unit

Table 2.60 shows a comparative overview of the parallel data capture unit specifications. The parallel data capture unit (PDC) is implemented on the RX631 only.

Table 2.60 Comparative Overview of Parallel Data Capture Unit

Item	RX631 (PDC)	RX65N (PDC)
Capture range	User-specified amounts of parallel data within the following ranges in the vertical and horizontal directions: Vertical direction: 1 to 4,095 lines Horizontal direction: 4 to 4,095 bytes	User-specified amounts of parallel data within the following ranges in the vertical and horizontal directions: Vertical direction: 1 to 4,095 lines Horizontal direction: 4 to 4,095 bytes
Parallel transfer clock (PIXCLK)	Operating frequency: 1 to 27 MHz	Operating frequency: 1 to 27 MHz
Interrupt sources	• Receive data ready • Frame end • Overrun • Underrun • Error in the setting for the number of vertical lines • Error in setting for the number of horizontal bytes per line	• Receive data ready • Frame end • Overrun • Underrun • Error in the setting for the number of vertical lines • Error in setting for the number of horizontal bytes per line
DTC/DMAC activation	Support for activation by receive data ready interrupt	Support for activation by receive data ready interrupt
Parallel transfer clock output (PCKO)	• Operating frequency: 1 to 25 MHz • Clock source: Peripheral module clock B (PCLKB) • Frequency division ratio: Selectable among 2, 4, 6, 8, 10, 12, 14, and 16	• Operating frequency: 1 to 30 MHz • Clock source: Peripheral module clock B (PCLKB) • Frequency division ratio: Selectable among 2, 4, 6, 8, 10, 12, 14, and 16
Other functions	• PDC reset function • Selectable polarity for VSYNC and HSYNC signals • Monitoring of VSYNC and HSYNC signals • Endianness selection function	• PDC reset function • Selectable polarity for VSYNC and HSYNC signals • Monitoring of VSYNC and HSYNC signals • Endianness selection function
Low power consumption function	Module stop state can be set.	Module stop state can be set.
Internal bus interface	Connected to internal peripheral bus 3	Connected to internal peripheral bus 3

2.32 12-Bit A/D Converter

Table 2.61 shows a comparative overview of the 12-bit A/D converter specifications, and Table 2.62 shows a comparative listing of the 12-bit A/D converter registers.

Table 2.61 Comparative Overview of 12-Bit A/D Converter

Item	RX63N (S12ADa)	RX65N (S12ADFa)
Number of units	1 unit	2 units
Input channels	21 channels	Unit 0: 8 channels Unit 1: 21 channels + one extended channel
Extended analog function	Temperature sensor output, internal reference voltage	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	1.0 µs per channel (when operating with A/D conversion clock ADCLK = 50 MHz)	(0.48 µs) per channel (12-bit conversion mode) (0.45 µs) per channel (10-bit conversion mode) (0.42 µs) per channel (8-bit conversion mode) (Operating with A/D conversion clock ADCLK = 60 MHz)
A/D conversion clock (ADCLK)	4 clocks: PCLK, PCLK/2, PCLK/4, PCLK/8	Peripheral module clock PCLKB and A/D conversion clock ADCLK can be set so that the division ratio is one of the following: PCLKB: ADCLK frequency ratio = 1:1, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit (CPG).
Data register	• For analog input: 21 data registers • For temperature sensor: One data register • For internal reference voltage: One data register • The results of A/D conversion are stored in 12-bit A/D data registers.	• For analog input: 29 data registers (unit 0: 8 data registers, unit 1: 21 data registers), one data register for each unit for A/D conversion data multiplexing in double trigger mode, two data registers for each unit for A/D conversion data multiplexing in double trigger mode extended operation • For temperature sensor: One data register (unit 1 only) • For internal reference voltage: One data register (unit 1 only) • 1 register per unit for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • 8-, 10-, and 12-bit accuracy output for the results of A/D conversion

Item	RX63N (S12ADa)	RX65N (S12ADFa)
Data register	• In A/D-converted value addition mode, A/D conversion results are stored in a 14-bit A/D data register.	• In value addition mode, the value obtained by adding up A/D-converted results is stored as a value (number of conversion accuracy bits + 2 bits/4 bits) in the A/D data registers. • Double trigger mode (selectable in single scan and group scan modes) • The value obtained by adding up A/D-converted results is stored as a value (number of conversion accuracy bits + 2 bits/4 bits) in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.
Operating mode	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 21 user-selected channels. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs of up to 21 user-selected channels. (Continuous scan mode should not be used when temperature sensor output or the internal reference voltage is selected.)	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 8 (unit 0) or up to 12 (unit 1) user-selected channels. — A/D conversion is performed only once on the temperature sensor output (unit 1 only). — A/D conversion is performed only once on the internal reference voltage (unit 1 only). — A/D conversion is performed only once on the extended analog input (unit 1 only). • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs of up to 8 (unit 0) or up to 21 (unit 1) user-selected channels, the temperature sensor output (unit 1 only), or the internal reference voltage (unit 1 only). — A/D conversion is performed repeatedly on the extended analog input (unit 1 only).

Item	RX63N (S12ADa)	RX65N (S12ADFa)
Operating mode		• Group scan mode: — Either two (A and B) or three (A, B, and C) groups can be selected. (When the number of groups selected is two, only the combination of group A and group B is selectable.) — The analog inputs of user-selected channels, the temperature sensor output (unit 1 only), or the internal reference voltage (unit 1 only) are divided up among group A and group B, or among groups A, B, and C, and A/D conversion is performed only once on the analog inputs selected as a group unit. — The conditions for scanning start of groups A, B, and C (synchronous trigger) can be independently selected, thus allowing A/D conversion of each group to be started independently. • Group scan mode (with group priority control selected): — If a priority-group trigger is input during scanning of the low-priority group, scan of the low-priority group is stopped and scan of the priority group is started. The priority order is group A (highest) > group B > group C (lowest). Whether or not to restart scanning of the low-priority group after processing for the high-priority group completes, is selectable. Rescan can also be set to start either from the beginning of the selected channel or the channel on which A/D conversion is not completed.
A/D conversion start conditions	• Software trigger • Synchronous trigger Conversion start is triggered by the MTU, TPU, and TMR. • Asynchronous trigger A/D conversion can be triggered by the ADTRG0# pin.	• Software trigger • Synchronous trigger Conversion start is triggered by the MTU, TPU, TMR, and ELC. • Asynchronous trigger A/D conversion can be started by the external trigger ADTRG0# pin (unit 0) or ADTRG1# pin (unit 1).

Item	RX63N (S12ADa)	RX65N (S12ADFa)
Functions	• Sample-and-hold function • Variable sampling state count • Selectable A/D-converted value adding mode	• Sample-and-hold function • Channel-dedicated sample-and-hold function (3 channels: unit 1) • Variable sampling state count • Self-diagnostic function for 12-bit A/D converter • Selectable A/D-converted value adding mode or averaging mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Function for switching among 12-, 10-, and 8-bit conversion • A/D data register auto-clear function • Extended analog input function • Compare function (window A, window B)
Interrupt sources	• An scan end interrupt request (S12ADI0) can be generated on completion of A/D conversion.	• In modes other than double trigger mode and group scan mode, an A/D scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of a single scan. • In double trigger mode, an A/D scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of a double scan. • In group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of a group A scan. On completion of a group B scan a dedicated group B scan end interrupt request (S12GBADI or S12GBADI1) can be generated, and on completion of a group C scan a dedicated group C scan end interrupt request (S12GCADI or S12GCADI1) can be generated. • When double trigger mode is selected in group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of two scans of group A. On completion of two scans of group B or C a dedicated group B or group C scan end interrupt request (S12GBADI/S12GCADI or S12GBADI1/S12GCADI1) can be generated.

Item	RX63N (S12ADa)	RX65N (S12ADFa)
Interrupt sources	• A S12ADI0 interrupt can activate the DMAC and DTC.	• A compare interrupt (S12CMPAI, S12CMPAI1, S12CMPBI, or S12CMPBI1) can be generated when the digital compare function comparison conditions are met. • The DMAC or DTC can be activated by the S12ADI/S12ADI1, S12GBADI/S12GBADI1, or S12GCADI/S12GCADI1 interrupt.
Event link function	—	• An ELC event can be generated at end of all scans. • Scanning can be started by a trigger from the ELC.
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Table 2.62 Comparative Listing of 12-Bit A/D Converter Registers

Register	Bit	RX63N (S12ADa)	RX65N (S12ADFa)
ADDBLDR	—	—	A/D data duplication register
ADDBLDRA	—	—	A/D data duplication register A
ADDBLDRB	—	—	A/D data duplication register B
ADRD	—	—	A/D self-diagnosis data register
ADCSR	DBLANS[4:0]	—	Double trigger channel select bits (b4 to b0)
	GBADIE	—	Group B scan end interrupt enable bit (b6)
	DBLE	—	Double trigger mode select bit (b7)
	EXTRG	Trigger select bit (b0)	Trigger select bit (b8)
	TRGE	Trigger start enable bit (b1)	Trigger start enable bit (b9)
	CKS[1:0]	A/D conversion clock select bits (b3, b2)	—
	ADIE	Scan end interrupt enable bit (b4)	Scan end interrupt enable bit (b12)
	ADCS	Scan mode select bit (b6) 0: Single scan mode 1: Continuous scan mode	Scan mode select bit (b14, b13) b14 b13 0 0: Single scan mode 0 1: Group scan mode 1 0: Continuous scan mode 1 1: Setting prohibited
	ADST	A/D conversion start bit (b7)	A/D conversion start bit (b15)
ADANS0	—	A/D channel select register 0	—
ADANS1	—	A/D channel select register 1	—
ADANSA0	—	—	A/D channel select register A0
ADANSA1	—	—	A/D channel select register A1
ADANSB0	—	—	A/D channel select register B0
ADANSB1	—	—	A/D channel select register B1
ADANSC0	—	—	A/D channel select register C0
ADANSC1	—	—	A/D channel select register C1
ADADS0	—	A/D-converted value addition mode select register 0	A/D-converted value addition/average function select register 0

Register	Bit	RX63N (S12ADa)	RX65N (S12ADFa)
ADADS1	—	A/D-converted value addition mode select register 1	A/D-converted value addition/average function select register 1
ADADC	ADC	Addition count select bits (b1, b0) b1 b0 0 0: 1-time conversion (no addition, same as normal conversion) 0 1: 2-time conversion (addition once) 1 0: 3-time conversion (addition twice) 1 1: 4-time conversion (addition three times)	Addition count select bits (b2 to b0) b2 b0 0 0 0: 1-time conversion (no addition, same as normal conversion) 0 0 1: 2-time conversion (addition once) 0 1 0: 3-time conversion (addition twice) 0 1 1: 4-time conversion (addition three times) 1 0 1: 16-time conversion (addition 15 times) Do not set to values other than the above.
ADADC	AVEE	—	Average mode enable bit
ADCER	ADPRC[1:0]	—	A/D conversion resolution setting bit
	DIAGVAL[1:0]	—	Self-diagnostic conversion voltage select bits
	DIAGLD	—	Self-diagnostic mode select bit
	DIAGM	—	Self-diagnostic enable bit
ADSTRGR	ADSTRS[3:0]	A/D conversion start trigger select bits	—
	TRSB[5:0]	—	A/D conversion start trigger select for group B bits
	TRSA[5:0]	—	A/D conversion start trigger select bits
ADEXICR	TSSAD	Temperature sensor output A/D-converted value addition mode select bit	Temperature sensor output A/D-converted value addition/average mode select bit
	OCSAD	A/D internal reference voltage A/D converted value addition mode select bit	Internal reference voltage A/D-converted value addition/average mode select bit
	TSS	Temperature sensor output A/D conversion select bit	—
	TSSA	—	Temperature sensor output A/D conversion select bit
	OCS	A/D internal reference voltage A/D conversion select bit	—
	OCSA	—	Internal reference voltage A/D conversion select bit
	TSSB	—	Temperature sensor output A/D conversion select bit
	OCSB	—	Internal reference voltage A/D conversion select bit
	EXSEL[1:0]	—	Extended analog input select bits
	EXOEN	—	Extended analog output control bit

Register	Bit	RX63N (S12ADa)	RX65N (S12ADFa)
ADGCEXCR	—	—	A/D group C extended input control register
ADGCTRGR	—	—	A/D group C trigger select register
ADSSTR01	—	A/D sampling state register 01	—
ADSSTR23	—	A/D sampling state register 23	—
ADSSTRn	—	—	A/D sampling state register n (n = 0 to 15, L, T, and O)
ADSHCR	—	—	A/D sample-and-hold circuit control register
ADSHMSR	—	—	A/D sample-and-hold operating mode select register
ADDISCR	—	—	A/D disconnection detection control register
ADGSPCR	—	—	A/D group scan priority control register
ADCMPCR	—	—	A/D comparison function control register
ADCMPANSR0	—	—	A/D comparison function window A channel select register 0
ADCMPANSR1	—	—	A/D comparison function window A channel select register 1
ADCMPANSER	—	—	A/D comparison function window A extended input select register
ADCMPLR0	—	—	A/D comparison function window A compare condition setting register 0
ADCMPLR1	—	—	A/D comparison function window A compare condition setting register 1
ADCMPLER	—	—	A/D comparison function window A extended input compare condition setting register
ADCMPDR0	—	—	A/D comparison function window A lower level setting register
ADCMPDR1	—	—	A/D comparison function window A upper level setting register
ADCMPSR0	—	—	A/D comparison function window A channel status register 0
ADCMPSR1	—	—	A/D comparison function window A channel status register 1
ADCMPSER	—	—	A/D comparison function window A extended input channel status register
ADWINMON	—	—	A/D comparison function window A/B status monitor register
ADCMPBNSR	—	—	A/D comparison function window B channel select register
ADWINLLB	—	—	A/D comparison function window B lower level setting register
ADWINULB	—	—	A/D comparison function window B upper level setting register

Register	Bit	RX63N (S12ADa)	RX65N (S12ADFa)
ADCMPBSR	—	—	A/D comparison function window B channel status register

Register	Bit	RX63N (S12ADa)	RX65N (S12ADFa)
ADSAM	—	—	A/D conversion time setting register
ADSAMPR	—	—	A/D conversion time setting protection release register

2.33 D/A Converter

Table 2.63 shows a comparative overview of the D/A converter specifications, and Table 2.64 shows a comparative listing of the D/A converter registers.

Table 2.63 Comparative Overview of D/A Converter

Item	RX63N (DAa)	RX65N (R12DAa)
Resolution	10 bits	12 bits
Output channel	2 channels	2 channels
Measure against mutual interference between analog modules	Measure against interference between D/A and A/D conversion: D/A converted data update timing is controlled by the 10-bit A/D converter synchronous D/A conversion enable input signal output by the the 10-bit A/D converter. (Degradation of A/D conversion accuracy caused by interference is reduced by controlling the D/A converter inrush current generation timing with the enable signal.)	Measure against interference between D/A and A/D conversion: D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable input signal output by the the 12-bit A/D converter (unit 1). Degradation of 12-bit A/D conversion accuracy caused by interference is reduced by controlling the D/A converter inrush current generation timing with the enable signal.
Low power consumption function	Module stop state can be set.	Module stop state can be set.
Event link function (input)	—	Ability to activate D/A conversion on channel 0 by event signal input
Output buffer amplifier control function	—	Buffered output (gain = 1) or unbuffered output can be selected.

Table 2.64 Comparative Listing of D/A Converter Registers

Register	Bit	RX63N (DAa)	RX65N (R12DAa)
DAADUSR	—	—	D/A A/D synchronous unit select register
DAAMPCR	—	—	D/A output amplifier control register
DAASWCR	—	—	D/A output amplifier stabilization wait control register

2.34 Temperature Sensor

Table 2.65 shows a comparative listing of the temperature sensor registers.

Table 2.65 Comparative Listing of Temperature Sensor Registers

Register	Bit	RX63N	RX65N (TEMPS)
TSCDRH, TSCDRL (RX63N) TSCDR (RX65N)	—	Temperature sensor calibration data register (b7 to b0) Bits 3 to 0 in TSCDRH and bits 7 to 0 in TSCDRL hold the temperature sensor calibration data measured for each chip at the time of shipment.	Temperature sensor calibration data register (b31 to b0) Bits 11 to 0 hold the temperature sensor calibration data measured for each chip at the time of shipment.

2.35 RAM

Table 2.66 shows a comparative overview of the RAM specifications, and Table 2.67 shows a comparative listing of the RAM registers.

Table 2.66 Comparative Overview of RAM

Item	RX63N	RX65N (No ECC Error Correction)
RAM capacity	• 64 KB RAM0: 64 KB • 128 KB RAM0: 64 KB, RAM1: 64 KB • 192 KB RAM0: 64 KB, RAM1: 128 KB • 256 KB RAM0: 64 KB, RAM1: 192 KB	• 256 KB / 384 KB*1 RAM: 256 KB Expansion RAM: 384 KB*1
RAM address	• When the RAM capacity is 64 KB RAM0: 0000 0000h to 0000 FFFFh (64 KB) RAM1: None • When the RAM capacity is 128 KB RAM0: 0000 0000h to 0000 FFFFh (64 KB) RAM1: 0001 0000h to 0001 FFFFh (64 KB) • When the RAM capacity is 192 KB RAM0: 0000 0000h to 0000 FFFFh (64 KB) RAM1: 0001 0000h to 0002 FFFFh (128 KB) • When the RAM capacity is 256 KB RAM0: 0000 0000h to 0000 FFFFh (64 KB) RAM1: 0001 0000h to 0003 FFFFh (192 KB)	RAM: 0000 0000h to 0003 FFFFh Expansion RAM: 0080 0000h to 0085 FFFFh*1
Access	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.
Data retention function	Data in RAM0 can be retained in deep software standby mode.	Data is not retained in deep software standby mode. (Data can be retained in standby RAM.)
Low power consumption function	The module-stop state is independently selectable for RAM0 and RAM1.	Transition to the module stop state is separately possible for the RAM and expansion RAM*1.
Error checking function	None	• Single-bit error detection • Generation of non-maskable interrupt or interrupt when an error occurs

Note: 1. Can be used for products with at least 1.5 MB of code flash memory.

Table 2.67 Comparative Listing of RAM Registers

Register	Bit	RX63N	RX65N
RAMMODE	—	—	RAM operating mode control register
RAMSTS	—	—	RAM error status register
RAMECAD	—	—	RAM error address capture register
RAMPRCR	—	—	RAM protection register
EXRAMMODE	—	—	Expansion RAM Operating Mode Control Register*1
EXRAMSTS	—	—	Expansion RAM Error Status Register*1
EXRAMECAD	—	—	Expansion RAM Error Address Capture Register*1
EXRAMPRCR	—	—	Expansion RAM Protection Register*1

Note: 1. Can be used for products with at least 1.5 MB of code flash memory.

2.36 Flash Memory (Code Flash)

Table 2.68 shows a comparative overview of the flash memory (code flash) specifications, and Table 2.69 shows a comparative listing of the flash memory registers.

Table 2.68 Comparative Overview of Flash Memory (Code Flash) Specifications

Item	RX63N	RX65N
Memory space	• User area: Maximum 2 MB • User boot area: 16 KB	• User area: Maximum 1 MB/2 MB*1
Cache	Not provided	• Capacity: Max. 256 bytes • Mapping method: 8-way set associative • Replacement method: LRU algorithm • Line size: 16 bytes
Read cycle	High-speed read operation using 1 cycle of ICLK is supported.	• When cache hit occurs: 1 cycle • When cache miss occurs: 1 cycle if ICLK ≤ 50 MHz, 2 cycles if 50 MHz < ICLK ≤ 100 MHz, 3 cycles if ICLK > 100 MHz
Value after erase	FFh	FFh
Programming/ erasing method	• On-chip dedicated sequencer (FCU) for programming the ROM • Programming/erasing the ROM are handled by issuing commands to the FCU.	• Programming and erasing the code flash memory is handled by the FACI commands specified in the FACI command issuing area (007E 0000h) • Programming/erasure through transfer by a dedicated flash-memory programmer via a serial interface (serial programming) • Programming/erasure of flash memory by a user program (self-programming)
Security function	Prevents unauthorized modification or reading of data.	Prevents unauthorized modification or reading of data.
Protection function	Prevents unintentional programming of the flash memory.	Prevents unintentional programming of the flash memory.
Dual bank function*1	—	The dual-bank structure makes a safe update possible in cases where programming is suspended. • Linear mode: the code flash memory is used as one area • Dual mode: the code flash memory is divided into two areas
Trusted Memory (TM) function	—	Prevents unauthorized reading of blocks 8 and 9 in the code flash memory. Dual mode: blocks 8, 9 ,46, and 47*1
Background operation (BGO) function	The CPU is able to execute program code from the ROM while the E2 Data Flash memory is being programmed or erased.	• The code flash memory can be read while the code flash memory is being programmed or erased. • The data flash memory can be read while the code flash memory is being programmed or erased. • The code flash memory can be read while the data flash memory is being programmed or erased.

Item	RX63N	RX65N
Suspend/resume function	• Halts (suspends) programming/ erasure of the ROM, allowing the CPU to execute program code from the ROM area. • Halts (suspends) programming/ erasure of the E2 data flash, allowing the CPU to read from the E2 data flash area (suspend). • Programming/erasure of the ROM or E2 data flash can be restarted (resumed) after suspension.	• Halts (suspends) programming/ erasure of the code flash, allowing the CPU to execute program code (suspend) from the code flash area. • Programming/erasure of the code flash can be restarted (resumed) after suspension.
Units of programming and erasure	• Programming the user area and user boot area: 128 bytes • Erasing the user area: One block	• Programming the user area: 128 bytes • Erasing the user area: One block
Other functions	Ability to accept interrupts during self-programming	Ability to accept interrupts during self-programming
	Ability to specify initial settings for the microcontroller in option-setting memory	Ability to specify initial settings for the microcontroller in option-setting memory
	—	Ability to select block 0 or 1 as the startup area of the code flash memory
On-board programming	• Programming in boot mode (SCI interface) — The asynchronous serial interface (SCI1) is used. — The communication speed is adjusted automatically. — The user boot area can also be programmed. • Programming in USB boot mode — USB0 is used. — Dedicated hardware is not required, so direct connection to a PC is possible. • Programming in user boot mode — Users can create their own boot programs. • Programming by a routine for ROM programming within the user program — This allows ROM programming without resetting the system.	• Programming/erasing in boot mode (SCI interface) — The asynchronous serial interface (SCI1) is used. — The communication speed is adjusted automatically. • Programming/erasing in USB boot mode — USBb is used. — Dedicated hardware is not required, so direct connection to a PC is possible. • Programming/erasing in boot mode (FINE interface) — Uses FINE. • Programming/erasing by a routine for code flash memory programming within the user program — This allows code flash memory programming/erasing without resetting the system.
Off-board programming (products with 100 pins or more)	A flash programmer can be used to program the user area and user boot area.	A flash programmer can be used to program/erase the user area.
Unique ID	A unique 16-byte ID code is provided for each MCU. (The unique ID is only available for the G-version products.)	A unique 16-byte ID code is provided for each MCU.

Note: 1. Can be used for products with at least 1.5 MB of code flash memory.

Table 2.69 Comparative Listing of Flash Memory Registers

Register	Bit	RX63N	RX65N
FWEPROR	FLWE[1:0]	Flash programming/erasure bits b1 b0 0 0: Programming/erasure, programming/erasure of lock bits, reading of lock bits, and blank checking disabled. 0 1: Programming/erasure, programming/erasure of lock bits, reading of lock bits, and blank checking enabled. 1 0: Programming/erasure, programming/erasure of lock bits, reading of lock bits, and blank checking disabled. 1 1: Programming/erasure, programming/erasure of lock bits, reading of lock bits, and blank checking disabled.	Flash programming and erasure enable bits Products with at least 1.5 MB of code flash memory: b1 b0 0 0: Programming/erasure and blank checking disabled. 0 1: Programming/erasure and blank checking enabled. 1 0: Programming/erasure and blank checking disabled. 1 1: Programming/erasure and blank checking disabled. Products with 1 MB of code flash memory or less: b1 b0 0 0: Programming/erasure disabled. 0 1: Programming/erasure enabled. 1 0: Programming/erasure disabled. 1 1: Programming/erasure disabled.
FMODR	—	Flash mode register	—
FASTAT	DFLWPE	E2 data flash programming/erasure protection violation flag	—
	DFLRPE	E2 data flash read protection violation flag	—
	DFLAE	E2 data flash access violation flag	—
	ROMAE	ROM access violation flag	—
	CFAE	—	Code flash memory access violation flag
FAEINT	DFLWPEIE	E2 data flash programming/erasure protection violation interrupt enable bit	—
	DFLRPEIE	E2 data flash read protection violation interrupt enable bit	—
	DFAEIE	—	E2 data flash access violation interrupt enable bit
	DFLAEIE	E2 data flash access violation interrupt enable bit	—
	ROMAEIE	ROM access violation interrupt enable bit	—
	CFAEIE	—	Code flash memory access violation interrupt enable bit
DFLRE0	—	E2 data flash read enable register 0	—

Register	Bit	RX63N	RX65N
DFLRE1	—	E2 data flash read enable register 1	—
DFLWE0	—	E2 data flash P/E enable register 0	—
DFLWE1	—	E2 data flash P/E enable register 1	—
FSADDR	—	—	FACI command start address register
FCURAME	—	FCURAM enable register	—
FSTATR0	—	Flash status register 0	—
FSTATR1	—	Flash status register 1	—
FSTATR	—	—	Flash status register
FENTRYR	FENTRY0	ROM P/E mode entry 0 bit	—
	FENTRYC	—	Code flash P/E mode entry bit
	FENTRY1	ROM P/E mode entry 1 bit	—
	FENTRY2	ROM P/E mode entry 2 bit	—
	FENTRY3	ROM P/E mode entry 3 bit	—
	FENTRYD	E2 data flash P/E mode entry bit	—
	FEKEY[7:0]	Key code bits	—
	KEY[7:0]	—	Key code bits
FPROTR	—	Flash protection register	—
FRESETR	—	Flash reset register	—
FSUINITR	—	—	Flash sequencer set-up initialization register
DFLBCCNT	—	E2 data flash blank check control register	—
FPESTAT	—	Flash P/E status register	—
DFLBCSTAT	—	E2 data flash blank check status register	—
FAWMON	—	—	Flash access window monitor register
FPCKAR	—	—	Flash sequencer processing clock notification register
FSUACR	—	—	Start-up area control register
PCKAR	—	Peripheral clock notification register	—
ROMCE	—	—	ROM cache enable register
ROMCIV	—	—	ROM cache invalidate register

2.37 Package

As indicated in Table 2.70, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage. For details, refer to Design Guide for Migration between RX Family: Differences in Package External form (R01AN4591EJ).

Table 2.70 Package

Package Type	Renesas Code	
	RX63N	**RX65N**
144-pin LFQFP	PLQP0144KA-A	PLQP0144KA-B
100-pin LFQFP	PLQP0100KB-A	PLQP0100KB-B
64-pin TFLGA	○	×
64-pin LFQFP	PLQP0064KB-A	PLQP0064KB-C
48-pin LQFP	○	×

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

A comparison of pin functions, power supplies, clocks, and system control pins is shown below. Items that apply to one group only are colored blue, while items that are implemented on both groups but with points of difference are colored red. Items are shown in **black** when there are no points of difference in their specifications.

3.1 177-/176-Pin Package

Table 3.1 shows a comparative listing of the pin functions on the 177-/176-pin package.

Table 3.1 Comparative Listing of Pin Functions on 177-/176-Pin Package

177-/176-Pin	RX63N	RX65N
A1	AVSS0	AVSS0
A2	AVCC0	AVCC0
A3	VREFL0	VREFL0
A4	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
A5	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
A6	VCC	VCC
A7	VSS	VSS
A8	P94/A20/D20	P94/D20/A20
A9	VCC	VCC
A10	P97/A23/D23	TRSYNC1/P97/D23/A23
A11	PD6/D6[A6/D6]/MTIC5V/POE1#/SSLC2/IRQ6/AN6	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/MMC_D0-B/LCD_DATA18-B/IRQ6/AN106
A12	P60/CS0#	P60/CS0#
A13	P63/CS3#/CAS#	P63/CAS#/D2[A2/D2]/CS3#
A14	PE1/D9[A9/D9]/MTIOC4C/TIOCD9/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2/RSPCKB/ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B/MMC_D5-B/LCD_DATA15-B/ANEX1
A15	PE2/D10[A10/D10]/MTIOC4A/TIOCA9/PO23/RXD12/SMISO12/SSCL12/RXDX12/SSLB3/MOSIB/IRQ7-DS/AN0	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/PO23/TIC3/RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B/MMC_D6-B/LCD_DATA14-B/IRQ7-DS/AN100
B1	P05/IRQ13/DA1	P05/IRQ13/DA1
B2	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
B3	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
B4	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
B5	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
B6	P91/A17/D17/SCK7/AN015	P91/D17/A17/SCK7/AN115
B7	P92/A18/D18/RXD7/SMISO7/SSCL7/AN016	P92/D18/A18/POE4#/RXD7/SMISO7/SSCL7/AN116
B8	PD1/D1[A1/D1]/MTIOC4B/TIOCB7/TCLKG/MOSIC/CTX0/IRQ1/AN009	PD1/D1[A1/D1]/MTIOC4B/POE0#/MOSIC-A/CTX0/LCD_DATA23-B/IRQ1/AN109
B9	P96/A22/D22	TRDATA5/P96/D22/A22
B10	PD4/D4[A4/D4]/POE3#/SSLC0/IRQ4/AN012	PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0-A/QSSL-B/SDHI_CMD-B/MMC_CMD-B/LCD_DATA20-B/IRQ4/AN112
B11	PG1/D25	TRDATA7/PG1/D25

177-/ 176-Pin	RX63N	RX65N
B12	VSS	VSS
B13	P64/CS4#/WE#	P64/WE#/D3[A3/D3]/CS4#
B14	PE0/D8[A8/D8]/TIOCC9/SCK12/SSLB1/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/SCK12/SSLB1-B/MMC_D4-B/LCD_DATA16-B/ANEX0
B15	PE3/D11[A11/D11]/MTIOC4B/TIOCB9/PO26/POE8#/ET_ERXD3/CTS12#/RTS12#/SS12#/MISOB/AN1	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/PO26/TOC3/POE8#/ET0_ERXD3/CTS12#/RTS12#/SS12#/MMC_D7-B/LCD_DATA13-B/AN101
C1	VREFL	AVSS1
C2	VREFH	AVCC1
C3	VREFH0	VREFH0
C4	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
C5	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
C6	P90/A16/D16/TXD7/SMOSI7/SSDA7/AN014	P90/D16/A16/TXD7/SMOSI7/SSDA7/AN114
C7	PD0/D0[A0/D0]/TIOCA7/IRQ0/AN008	PD0/D0[A0/D0]/POE4#/LCD_EXTCLK-B/IRQ0/AN108
C8	PD2/D2[A2/D2]/MTIOC4D/TIOCA8/MISOC/CRX0/IRQ2/AN010	PD2/D2[A2/D2]/MTIOC4D/TIC2/MISOC-A/CRX0/QIO2-B/SDHI_D2-B/MMC_D2-B/LCD_DATA22-B/IRQ2/AN110
C9	PD3/D3[A3/D3]/TIOCB8/TCLKH/POE8#/RSPCKC/IRQ3/AN011	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/RSPCKC-A/QIO3-B/SDHI_D3-B/MMC_D3-B/LCD_DATA21-B/IRQ3/AN111
C10	PG0/D24	TRDATA6/PG0/D24
C11	VCC	VCC
C12	P62/CS2#/RAS#	P62/RAS#/D1[A1/D1]/CS2#
C13	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/TIOCA10/PO28/ET_ERXD2/SSLB0/AN2	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/MTIOC1A/PO28/ET0_ERXD2/SSLB0-B/LCD_DATA12-B/AN102
C14	VSS	VSS
C15	P70/SDCLK	P70/SDCLK
D1	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/AN019	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/AN119
D2	P02/TMCI1/SCK6/IRQ10/AN020	P02/TMCI1/SCK6/IRQ10/AN120
D3	P03/IRQ11/DA0	P03/IRQ11/DA0
D4	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/AN018	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/AN118
D5	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
D6	P93/A19/D19/CTS7#/RTS7#/SS7#/AN017	P93/D19/A19/POE0#/CTS7#/RTS7#/SS7#/AN117
D7	P95/A21/D21	TRDATA4/P95/D21/A21
D8	VSS	VSS
D9	PD5/D5[A5/D5]/MTIC5W/POE2#/SSLC1/IRQ5/AN013	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/SSLC1-A/QSPCLK-B/SDHI_CLK-B/MMC_CLK-B/LCD_DATA19-B/IRQ5/AN113
D10	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3/IRQ7/AN7	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B/LCD_DATA17-B/IRQ7/AN107
D11	P61/CS1#/SDCS#	P61/SDCS#/D0[A0/D0]/CS1#
D12	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/TIOCB10/ET_RX_CLK/REF50CK/RSPCKB/IRQ5/AN3	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/MTIOC2B/ET0_RX_CLK/REF50CK0/RSPCKB-B/LCD_DATA11-B/IRQ5/AN103

177-/ 176-Pin	RX63N	RX65N
D13	VCC	VCC
D14	PE7/D15[A15/D15]/TIOCB11/MISOB/IRQ7/AN5	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/TOC1/MISOB-B/SDHI_WP/MMC_RES#-B/LCD_DATA9-B/IRQ7/AN105
D15	P65/CS5#/CKE	P65/CKE/CS5#
E1	PJ5	PJ5/POE8#/CTS2#/RTS2#/SS2#
E2	EMLE	EMLE
E3	PF5/IRQ4	PF5/IRQ4
E4	VSS	VSS
E5*1	NC	NC
E12	PE6/D14[A14/D14]/TIOCA11/MOSIB/IRQ6/AN4	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/TIC1/MOSIB-B/SDHI_CD/MMC_CD-B/LCD_DATA10-B/IRQ6/AN104
E13	TRDATA0/PG2/D26	TRDATA0/PG2/D26
E14	TRDATA1/PG3/D27	TRDATA1/PG3/D27
E15	P67/CS7#/DQM1/CRX2*3/IRQ15	P67/DQM1/CS7#/MTIOC7C/IRQ15
F1	VBATT	VBATT
F2	VCL	VCL
F3	PJ3/MTIOC3C/CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0#	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/CTS6#/RTS6#/SS6#/CTS0#/RTS0#/SS0#
F4	BSCANP	BSCANP
F12	P66/CS6#/DQM0/CTX2*3	P66/DQM0/CS6#/MTIOC7D
F13	TRSYNC/PG4/D28	TRSYNC/PG4/D28
F14	PA0/A0/BC0#/DQM2/MTIOC4A/TIOCA0/PO16/ET_TX_EN/RMII_TXD_EN/SSLA1	PA0/DQM2/BC0#/A0/MTIOC4A/MTIOC6D/TIOCA0/PO16/CACREF/ET0_TX_EN/RMII0_TXD_EN/SSLA1-B/LCD_DATA8-B
F15	VSS	VSS
G1	XCIN	XCIN
G2	XCOUT	XCOUT
G3	MD/FINED	MD/FINED
G4	TRST#/PF4	TRST#/PF4
G12	TRCLK/PG5/D29	TRCLK/PG5/D29
G13	TRDATA2/PG6/D30	TRDATA2/PG6/D30
G14	PA1/A1/DQM3/MTIOC0B/MTCLKC/TIOCB0/PO17/ET_WOL/SCK5/SSLA2/IRQ11	PA1/DQM3/A1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/PO17/ET0_WOL/SCK5/SSLA2-B/LCD_DATA7-B/IRQ11
G15	VCC	VCC
H1	XTAL/P37	XTAL/P37
H2	VSS	VSS
H3	RES#	RES#
H4	P35/NMI	UPSEL/P35/NMI
H12	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/ET_MDC/TXD5/SMOSI5/SSDA5/SSLA0/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/ET0_MDC/TXD5/SMOSI5/SSDA5/SSLA0-B/LCD_DATA4-B/IRQ5-DS
H13	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/ET_MDIO/RXD5/SMISO5/SSCL5/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/ET0_MDIO/RXD5/SMISO5/SSCL5/LCD_DATA5-B/IRQ6-DS
H14	PA2/A2/PO18/RXD5/SMISO5/SSCL5/SSLA3	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/SSCL5/SSLA3-B/LCD_DATA6-B
H15	TRDATA3/PG7/D31	TRDATA3/PG7/D31

177-/ 176-Pin	RX63N	RX65N
J1	EXTAL/P36	EXTAL/P36
J2	VCC	VCC
J3	P34/MTIOC0A/TMCI3/PO12/POE2#/SCK6/SCK0/USB0_DPRPD/IRQ4	P34/MTIOC0A/TMCI3/PO12/POE10#/ET0_LINKSTA/SCK6/SCK0/IRQ4
J4	TMS/PF3	TMS/PF3
J12	PA5/A5/TIOCB1/PO21/ET_LINKSTA/RSPCKA	PA5/A5/MTIOC6B/TIOCB1/PO21/ET0_LINKSTA/RSPCKA-B/LCD_DATA3-B
J13	VSS	VSS
J14	PA7/A7/TIOCB2/PO23/ET_WOL/MISOA	PA7/A7/TIOCB2/PO23/ET0_WOL/MISOA-B/LCD_DATA1-B
J15	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE2#/ET_EXOUT/CTS5#/RTS5#/SS5#/MOSIA	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE10#/ET0_EXOUT/CTS5#/RTS5#/SS5#/MOSIA-B/LCD_DATA2-B
K1	P33/MTIOC0D/TIOCD0/TMRI3/PO11/POE3#/RXD6/RXD0/SMISO6/SMISO0/SSCL6/SSCL0/CRX0/PCKO/IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/POE4#/POE11#/RXD6/SMISO6/SSCL6/RXD0/SMISO0/SSCL0/CRX0/PCKO/IRQ3-DS
K2	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCOUT/RTCIC2/TXD6/TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCIC2/RTCOUT/POE0#/POE10#/TXD6/SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS
K3	TDI/PF2/RXD1/SMISO1/SSCL1	TDI/PF2/RXD1/SMISO1/SSCL1
K4	TCK/FINEC/PF1/SCK1	TCK/PF1/SCK1
K12	PB2/A10/TIOCC3/TCLKC/PO26/ET_RX_CLK/REF50CK/CTS4#/RTS4#/CTS6#/RTS6#/SS4#/SS6#	PB2/A10/TIOCC3/TCLKC/PO26/ET0_RX_CLK/REF50CK0/CTS4#/RTS4#/SS4#/CTS6#/RTS6#/SS6#/SDSI_D2-B/LCD_TCON2-B
K13	P71/CS1#/ET_MDIO	P71/A18/CS1#/ET0_MDIO
K14	VCC	VCC
K15	PB0/A8/MTIC5W/TIOCA3/PO24/ET_ERXD1/RMII_RXD1/RXD4/RXD6/SMISO4/SMISO6/SSCL4/SSCL6/RSPCKA/IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/ET0_ERXD1/RMII0_RXD1/RXD4/SMISO4/SSCL4/RXD6/SMISO6/SSCL6/LCD_DATA0-B/IRQ12
L1	P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0/USB0_DPUPE/IRQ1-DS	P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS
L2	P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB/USB0_DRPD/IRQ0-DS	P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS
L3	TDO/PF0/TXD1/SMOSI1/SSDA1	TDO/PF0/TXD1/SMOSI1/SSDA1
L4	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/USB0_DPRPD/HSYNC/ADTRG0#	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/SDHI_CD/HSYNC/ADTRG0#
L12	PB6/A14/MTIOC3D/TIOCA5/PO30/ET_ETXD1/RMII_TXD1/RXD9/SMISO9/SSCL9	PB6/A14/MTIOC3D/TIOCA5/PO30/ET0_ETXD1/RMII0_TXD1/RXD9/SMISO9/SSCL9/SMISO11/SSCL11/RXD11/SDSI_D0-B
L13	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE3#/ET_RX_ER/RMII_RX_ER/SCK4/SCK6	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE11#/ET0_RX_ER/RMII0_RX_ER/SCK4/SCK6/SDSI_D3-B/LCD_TCON1-B
L14	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/ET_ERXD0/RMII_RXD0/TXD4/TXD6/SMOSI4/SMOSI6/SSDA4/SSDA6/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/ET0_ERXD0/RMII0_RXD0/TXD4/SMOSI4/SSDA4/TXD6/SMOSI6/SSDA6/LCD_TCON3-B/IRQ4-DS
L15	P72/CS2#/ET_MDC	P72/A19/CS2#/ET0_MDC/LCD_DATA23-A

177-/ 176-Pin	RX63N	RX65N
M1	P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB	P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB-A
M2	P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/MOSIB	P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/MOSIB-A
M3	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/PIXCLK	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/SDHI_WP/PIXCLK
M4	P86/TIOCA0/PIXD1	P86/MTIOC4D/TIOCA0/SMISO10/SSCL10/RXD10/PIXD1
M5	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG#	PJ2/TXD8/SMOSI8/SSDA8/SSLC3-B/LCD_TCON2-A
M6	P56/WR2#/BC2#/EDACK1/MTIOC3C/TIOCA1	PJ1/MTIOC6A/RXD8/SMISO8/SSCL8/SSLC2-B/LCD_TCON3-A
M7	P54/ALE/EDACK0/MTIOC4B/TMCI1/ET_LINKSTA/CTS2#/RTS2#/SS2#/CTX1	P85/MTIOC6C/TIOCC0/LCD_DATA1-A
M8	BCLK/P53*2	P55/D0[A0/D0]/EDREQ0/WAIT#/MTIOC4D/TMO3/ET0_EXOUT/TXD7/SMOSI7/SSDA7/MISOC-B/CRX1/LCD_DATA5-A/IRQ10
M9	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A
M10	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TIOCD6/TCLKF/TMRI2/PO29/ET_ETXD2/SCK8/RSPCKA	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/PO29/ET0_ETXD2/SCK8/SCK10/RSPCKA-A/MMC_D5-A/LCD_DATA11-A
M11	P81/EDACK0/MTIOC3D/PO27/ET_ETXD0/RMII_TXD0/RXD10/SMISO10/SSCL10	P81/EDACK0/MTIOC3D/PO27/ET0_ETXD0/RMII0_TXD0/SMISO10/SSCL10/RXD10/QIO3-A/SDHI_CD/MMC_D3-A/LCD_DATA13-A
M12	P77/CS7#/PO23/ET_RX_ER/RMII_RX_ER/TXD11/SMOSI11/SSDA11	P77/CS7#/PO23/ET0_RX_ER/RMII0_RX_ER/SMOSI11/SSDA11/TXD11/QSPCLK-A/SDHI_CLK-A/SDSI_CLK-A/MMC_CLK-A/LCD_DATA17-A
M13	PB7/A15/MTIOC3B/TIOCB5/PO31/ET_CRS/RMII_CRS_DV/TXD9/SMOSI9/SSDA9	PB7/A15/MTIOC3B/TIOCB5/PO31/ET0_CRS/RMII0_CRS_DV/TXD9/SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/SDSI_D1-B
M14	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE1#/ET_ETXD0/RMII_TXD0/SCK9	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE4#/ET0_ETXD0/RMII0_TXD0/SCK9/SCK11/SDSI_CLK-B/LCD_CLK-B
M15	PB4/A12/TIOCA4/PO28/ET_TX_EN/RMII_TXD_EN/CTS9#/RTS9#/SS9#	PB4/A12/TIOCA4/PO28/ET0_TX_EN/RMII0_TXD_EN/CTS9#/RTS9#/SS9#/SS11#/CTS11#/RTS11#/SDSI_CMD-B/LCD_TCON0-B
N1	VCC	VCC
N2	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/SSDA3/USB0_DPUPE/PIXD7	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/SS0#/SDHI_D1-C/PIXD7
N3	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_DRPD/PIXD6	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB/SDHI_D0-C/PIXD6
N4	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/CRX1-DS/USB1_DPUPE/PIXD0/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SMISO1/SSCL1/SCK3/CRX1-DS/PIXD0/IRQ5
N5	P12/MTIC5U/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/IRQ2	P12/WR3#/BC3#/MTIC5U/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/LCD_TCON1-A/IRQ2

177-/ 176-Pin	RX63N	RX65N
N6	P57/WAIT#/WR3#/BC3#/EDREQ1	PJ0/MTIOC6B/SCK8/SSLC1-B/LCD_DATA0-A
N7	P55/WAIT#/EDREQ0/MTIOC4D/TMO3/ET_EXOUT/CRX1/IRQ10	P84/MTIOC6D/LCD_DATA2-A
N8	VCC_USB	P54/D1[A1/D1]/EDACK0/ALE/MTIOC4B/TMCI1/ET0_LINKSTA/CTS2#/RTS2#/SS2#/MOSIC-B/CTX1/LCD_DATA6-A
N9	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A
N10	PC7/A23/CS0#/MTIOC3A/MTCLKB/TIOCB6/TMO2/PO31/ET_COL/TXD8/SMOSI8/SSDA8/MISOA/IRQ14	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/PO31/TOC0/CACREF/ET0_COL/TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/MMC_D7-A/LCD_DATA9-A/IRQ14
N11	P82/EDREQ1/MTIOC4A/PO28/ET_ETXD1/RMII_TXD1/TXD10/SMOSI10/SSDA10	P82/EDREQ1/MTIOC4A/PO28/ET0_ETXD1/RMII0_TXD1/SMOSI10/SSDA10/TXD10/MMC_D4-A/LCD_DATA12-A
N12	PC3/A19/MTIOC4D/TCLKB/PO24/ET_TX_ER/TXD5/SMOSI5/SSDA5/IETXD	PC3/A19/MTIOC4D/TCLKB/PO24/ET0_TX_ER/TXD5/SMOSI5/SSDA5/QMO-A/QIO0-A/SDHI_D0-A/SDSI_D0-A/MMC_D0-A/LCD_DATA16-A
N13	PC0/A16/MTIOC3C/TCLKC/PO17/ET_ERXD3/CTS5#/RTS5#/SS5#/SSLA1/SCL3/IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/ET0_ERXD3/CTS5#/RTS5#/SS5#/SSLA1-A/IRQ14
N14	P73/CS3#/PO16/ET_WOL	P73/CS3#/PO16/ET0_WOL/LCD_EXTCLK-A
N15	VSS	VSS
P1	VSS	VSS
P2	P17/MTIOC3A/MTIOC3B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/MISOA/SDA2-DS/IETXD/USB1_VBUS/PIXD3/IRQ7/ADTRG#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/SDHI_D3-C/PIXD3/IRQ7/ADTRG1#
P3	P87/TIOCA2/PIXD2	P87/MTIOC4C/TIOCA2/SMOSI10/SSDA10/TXD10/SDHI_D2-C/PIXD2
P4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_DPUPE/USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/LCD_CLK-A/IRQ4
P5	P10/MTIC5W/TMRI3/IRQ0	VCC_USB
P6	VCC_USB	VSS_USB
P7	VSS_USB	P57/RXD7/SMISO7/SSCL7/SSLC0-B/LCD_DATA3-A
P8	USB1_DP	P10/ALE/MTIC5W/TMRI3/IRQ0
P9	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A
P10	P83/EDACK1/MTIOC4C/ET_CRS/RMII_CRS_DV/CTS10#/RTS10#/SS10#	P83/EDACK1/MTIOC4C/ET0_CRS/RMII0_CRS_DV/SCK10/SS10#/CTS10#/LCD_DATA8-A
P11	PC6/A22/CS1#/MTIOC3C/MTCLKA/TIOCA6/TMCI2/PO30/ET_ETXD3/RXD8/SMISO8/SSCL8/MOSIA/IRQ13	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/PO30/TIC0/ET0_ETXD3/RXD8/SMISO8/SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/MMC_D6-A/LCD_DATA10-A/IRQ13
P12	PC4/A20/CS3#/MTIOC3D/MTCLKC/TIOCC6/TCLKE/TMCI1/PO25/POE0#/ET_TX_CLK/SCK5/CTS8#/RTS8#/SS8#/SSLA0	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/POE0#/ET0_TX_CLK/SCK5/CTS8#/RTS8#/SS8#/SS10#/CTS10#/RTS10#/SSLA0-A/QMI-A/QIO1-A/SDHI_D1-A/SDSI_D1-A/MMC_D1-A/LCD_DATA15-A

177-/ 176-Pin	RX63N	RX65N
P13	PC2/A18/MTIOC4B/TCLKA/PO21/ET_RX_DV/RXD5/SMISO5/SSCL5/SSLA3/IERXD	PC2/A18/MTIOC4B/TCLKA/PO21/ET0_RX_DV/RXD5/SMISO5/SSCL5/SSLA3-A/SDHI_D3-A/SDSI_D3-A/MMC_CD-A/LCD_DATA19-A
P14	P75/CS5#/PO20/ET_ERXD0/RMII_RXD0/SCK11	P75/CS5#/PO20/ET0_ERXD0/RMII0_RXD0/SCK11/RTS11#/SDHI_D2-A/SDSI_D2-A/MMC_RES#-A/LCD_DATA20-A
P15	VCC	VCC
R1	P21/MTIOC1B/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/SCL1/USB0_EXICEN/PIXD5/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/SCL1/USB0_EXICEN/SDHI_CLK-C/PIXD5/IRQ9
R2	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/SDA1/USB0_ID/PIXD4/IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/SDA1/USB0_ID/SDHI_CMD-C/PIXD4/IRQ8
R3	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/SMISO3/SSDA1/SSCL3/MOSIA/SCL2-DS/IERXD/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/SMOSI1/SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/USB0_VBUSEN/USB0_VBUS/USB0_OVRCURB/IRQ6/ADTRG0#
R4	P85	P13/WR2#/BC2#/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/LCD_TCON0-A/IRQ3/ADTRG1#
R5	P11/MTIC5V/TMCI3/SCK2/IRQ1	USB0_DM
R6	USB0_DM	USB0_DP
R7	USB0_DP	P56/EDACK1/MTIOC3C/TIOCA1/SCK7/RSPCKC-B/LCD_DATA4-A
R8	USB1_DM	P11/MTIC5V/TMCI3/SCK2/LCD_DATA7-A/IRQ1
R9	P84	P53*2/BCLK
R10	VSS	VSS
R11	VCC	VCC
R12	P80/EDREQ0/MTIOC3B/PO26/ET_TX_EN/RMII_TXD_EN/SCK10	P80/EDREQ0/MTIOC3B/PO26/ET0_TX_EN/RMII0_TXD_EN/SCK10/RTS10#/QIO2-A/SDHI_WP/MMC_D2-A/LCD_DATA14-A
R13	P76/CS6#/PO22/ET_RX_CLK/REF50CK/RXD11/SMISO11/SSCL11	P76/CS6#/PO22/ET0_RX_CLK/REF50CK0/SMISO11/SSCL11/RXD11/QSSL-A/SDHI_CMD-A/SDSI_CMD-A/MMC_CMD-A/LCD_DATA18-A
R14	P74/CS4#/PO19/ET_ERXD1/RMII_RXD1/CTS11#/RTS11#/SS11#	P74/A20/CS4#/PO19/ET0_ERXD1/RMII0_RXD1/SS11#/CTS11#/LCD_DATA21-A
R15	PC1/A17/MTIOC3A/TCLKD/PO18/ET_ERXD2/SCK5/SSLA2/SDA3/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/ET0_ERXD2/SCK5/SSLA2-A/LCD_DATA22-A/IRQ12

Notes: 1. The 176-pin LFBGA has no E5 pin.
2. When the external bus is enabled, P53, which is multiplexed with the BCLK pin, cannot be used as an I/O port.
3. Valid only on products with a ROM capacity of 2 MB or 1.5 MB.

3.2 176-Pin Package

Table 3.2 shows a comparative listing of the pin functions on the 176-pin package.

Table 3.2 Comparative Listing of Pin Functions on 176-Pin Package

176-Pin	RX63N	RX65N
1	AVSS0	AVSS0
2	P05/IRQ13/DA1	P05/IRQ13/DA1
3	VREFH	AVCC1
4	P03/IRQ11/DA0	P03/IRQ11/DA0
5	VREFL	AVSS1
6	P02/TMCI1/SCK6/IRQ10/AN020	P02/TMCI1/SCK6/IRQ10/AN120
7	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/AN019	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/AN119
8	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/AN018	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/AN118
9	PF5/IRQ4	PF5/IRQ4
10	EMLE	EMLE
11	PJ5	PJ5/POE8#/CTS2#/RTS2#/SS2#
12	VSS	VSS
13	PJ3/MTIOC3C/CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0#	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/CTS6#/RTS6#/SS6#/CTS0#/RTS0#/SS0#
14	VCL	VCL
15	VBATT	VBATT
16	NC	NC
17	TRST#/PF4	TRST#/PF4
18	MD/FINED	MD/FINED
19	XCIN	XCIN
20	XCOUT	XCOUT
21	RES#	RES#
22	XTAL/P37	XTAL/P37
23	VSS	VSS
24	EXTAL/P36	EXTAL/P36
25	VCC	VCC
26	P35/NMI	UPSEL/P35/NMI
27	P34/MTIOC0A/TMCI3/PO12/POE2#/SCK6/SCK0/USB0_DPRPD/IRQ4	P34/MTIOC0A/TMCI3/PO12/POE10#/ET0_LINKSTA/SCK6/SCK0/IRQ4
28	P33/MTIOC0D/TIOCD0/TMRI3/PO11/POE3#/RXD6/RXD0/SMISO6/SMISO0/SSCL6/SSCL0/CRX0/PCKO/IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/POE4#/POE11#/RXD6/SMISO6/SSCL6/RXD0/SMISO0/SSCL0/CRX0/PCKO/IRQ3-DS
29	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCOUT/RTCIC2/TXD6/TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCIC2/RTCOUT/POE0#/POE10#/TXD6/SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS
30	TMS/PF3	TMS/PF3
31	TDI/PF2/RXD1/SMISO1/SSCL1	TDI/PF2/RXD1/SMISO1/SSCL1
32	P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0/USB0_DPUPE/IRQ1-DS	P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS
33	P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB/USB0_DRPD/IRQ0-DS	P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS
34	TCK/FINEC/PF1/SCK1	TCK/PF1/SCK1

176-Pin	RX63N	RX65N
35	TDO/PF0/TXD1/SMOSI1/SSDA1	TDO/PF0/TXD1/SMOSI1/SSDA1
36	P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB	P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB-A
37	P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/MOSIB	P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/MOSIB-A
38	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/USB0_DPRPD/HSYNC/ADTRG0#	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/SDHI_CD/HSYNC/ADTRG0#
39	VCC	VCC
40	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/PIXCLK	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/SDHI_WP/PIXCLK
41	VSS	VSS
42	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/SSDA3/USB0_DPUPE/PIXD7	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/SS0#/SDHI_D1-C/PIXD7
43	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_DRPD/PIXD6	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB/SDHI_D0-C/PIXD6
44	P21/MTIOC1B/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/SCL1/USB0_EXICEN/PIXD5/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/SCL1/USB0_EXICEN/SDHI_CLK-C/PIXD5/IRQ9
45	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/SDA1/USB0_ID/PIXD4/IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/SDA1/USB0_ID/SDHI_CMD-C/PIXD4/IRQ8
46	P17/MTIOC3A/MTIOC3B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/MISOA/SDA2-DS/IETXD/USB1_VBUS/PIXD3/IRQ7/ADTRG#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/SDHI_D3-C/PIXD3/IRQ7/ADTRG1#
47	P87/TIOCA2/PIXD2	P87/MTIOC4C/TIOCA2/SMOSI10/SSDA10/TXD10/SDHI_D2-C/PIXD2
48	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/SMISO3/SSDA1/SSCL3/MOSIA/SCL2-DS/IERXD/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/SMOSI1/SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/USB0_VBUSEN/USB0_VBUS/USB0_OVRCURB/IRQ6/ADTRG0#
49	P86/TIOCA0/PIXD1	P86/MTIOC4D/TIOCA0/SMISO10/SSCL10/RXD10/PIXD1
50	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/CRX1-DS/USB1_DPUPE/PIXD0/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SMISO1/SSCL1/SCK3/CRX1-DS/PIXD0/IRQ5
51	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_DPUPE/USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/LCD_CLK-A/IRQ4
52	P85	P13/WR2#/BC2#/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/LCD_TCON0-A/IRQ3/ADTRG1#
53	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG#	P12/WR3#/BC3#/MTIC5U/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/LCD_TCON1-A/IRQ2
54	P12/MTIC5U/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/IRQ2	VCC_USB
55	P11/MTIC5V/TMCI3/SCK2/IRQ1	USB0_DM
56	P10/MTIC5W/TMRI3/IRQ0	USB0_DP

176-Pin	RX63N	RX65N
57	VCC_USB	VSS_USB
58	USB0_DM	PJ2/TXD8/SMOSI8/SSDA8/SSLC3-B/LCD_TCON2-A
59	USB0_DP	PJ1/MTIOC6A/RXD8/SMISO8/SSCL8/SSLC2-B/LCD_TCON3-A
60	VSS_USB	PJ0/MTIOC6B/SCK8/SSLC1-B/LCD_DATA0-A
61	P57/WAIT#/WR3#/BC3#/EDREQ1	P85/MTIOC6C/TIOCC0/LCD_DATA1-A
62	P56/WR2#/BC2#/EDACK1/MTIOC3C/TIOCA1	P84/MTIOC6D/LCD_DATA2-A
63	USB1_DM	P57/RXD7/SMISO7/SSCL7/SSLC0-B/LCD_DATA3-A
64	USB1_DP	P56/EDACK1/MTIOC3C/TIOCA1/SCK7/RSPCKC-B/LCD_DATA4-A
65	VCC_USB	P55/D0[A0/D0]/EDREQ0/WAIT#/MTIOC4D/TMO3/ET0_EXOUT/TXD7/SMOSI7/SSDA7/MISOC-B/CRX1/LCD_DATA5-A/IRQ10
66	P55/WAIT#/EDREQ0/MTIOC4D/TMO3/ET_EXOUT/CRX1/IRQ10	P54/D1[A1/D1]/EDACK0/ALE/MTIOC4B/TMCI1/ET0_LINKSTA/CTS2#/RTS2#/SS2#/MOSIC-B/CTX1/LCD_DATA6-A
67	P54/ALE/EDACK0/MTIOC4B/TMCI1/ET_LINKSTA/CTS2#/RTS2#/SS2#/CTX1	P11/MTIC5V/TMCI3/SCK2/LCD_DATA7-A/IRQ1
68	BCLK/P53*1	P10/ALE/MTIC5W/TMRI3/IRQ0
69	P84	P53*1/BCLK
70	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A
71	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A
72	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A
73	VSS	VSS
74	P83/EDACK1/MTIOC4C/ET_CRS/RMII_CRS_DV/CTS10#/RTS10#/SS10#	P83/EDACK1/MTIOC4C/ET0_CRS/RMII0_CRS_DV/SCK10/SS10#/CTS10#/LCD_DATA8-A
75	VCC	VCC
76	PC7/A23/CS0#/MTIOC3A/MTCLKB/TIOCB6/TMO2/PO31/ET_COL/TXD8/SMOSI8/SSDA8/MISOA/IRQ14	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/PO31/TOC0/CACREF/ET0_COL/TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/MMC_D7-A/LCD_DATA9-A/IRQ14
77	PC6/A22/CS1#/MTIOC3C/MTCLKA/TIOCA6/TMCI2/PO30/ET_ETXD3/RXD8/SMISO8/SSCL8/MOSIA/IRQ13	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/PO30/TIC0/ET0_ETXD3/RXD8/SMISO8/SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/MMC_D6-A/LCD_DATA10-A/IRQ13
78	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TIOCD6/TCLKF/TMRI2/PO29/ET_ETXD2/SCK8/RSPCKA	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/PO29/ET0_ETXD2/SCK8/SCK10/RSPCKA-A/MMC_D5-A/LCD_DATA11-A
79	P82/EDREQ1/MTIOC4A/PO28/ET_ETXD1/RMII_TXD1/TXD10/SMOSI10/SSDA10	P82/EDREQ1/MTIOC4A/PO28/ET0_ETXD1/RMII0_TXD1/SMOSI10/SSDA10/TXD10/MMC_D4-A/LCD_DATA12-A
80	P81/EDACK0/MTIOC3D/PO27/ET_ETXD0/RMII_TXD0/RXD10/SMISO10/SSCL10	P81/EDACK0/MTIOC3D/PO27/ET0_ETXD0/RMII0_TXD0/SMISO10/SSCL10/RXD10/QIO3-A/SDHI_CD/MMC_D3-A/LCD_DATA13-A
81	P80/EDREQ0/MTIOC3B/PO26/ET_TX_EN/RMII_TXD_EN/SCK10	P80/EDREQ0/MTIOC3B/PO26/ET0_TX_EN/RMII0_TXD_EN/SCK10/RTS10#/QIO2-A/SDHI_WP/MMC_D2-A/LCD_DATA14-A

176-Pin	RX63N	RX65N
82	PC4/A20/CS3#/MTIOC3D/MTCLKC/TIOCC6/TCLKE/TMCI1/PO25/POE0#/ET_TX_CLK/SCK5/CTS8#/RTS8#/SS8#/SSLA0	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/POE0#/ET0_TX_CLK/SCK5/CTS8#/RTS8#/SS8#/SS10#/CTS10#/RTS10#/SSLA0-A/QMI-A/QIO1-A/SDHI_D1-A/SDSI_D1-A/MMC_D1-A/LCD_DATA15-A
83	PC3/A19/MTIOC4D/TCLKB/PO24/ET_TX_ER/TXD5/SMOSI5/SSDA5/IETXD	PC3/A19/MTIOC4D/TCLKB/PO24/ET0_TX_ER/TXD5/SMOSI5/SSDA5/QMO-A/QIO0-A/SDHI_D0-A/SDSI_D0-A/MMC_D0-A/LCD_DATA16-A
84	P77/CS7#/PO23/ET_RX_ER/RMII_RX_ER/TXD11/SMOSI11/SSDA11	P77/CS7#/PO23/ET0_RX_ER/RMII0_RX_ER/SMOSI11/SSDA11/TXD11/QSPCLK-A/SDHI_CLK-A/SDSI_CLK-A/MMC_CLK-A/LCD_DATA17-A
85	P76/CS6#/PO22/ET_RX_CLK/REF50CK/RXD11/SMISO11/SSCL11	P76/CS6#/PO22/ET0_RX_CLK/REF50CK0/SMISO11/SSCL11/RXD11/QSSL-A/SDHI_CMD-A/SDSI_CMD-A/MMC_CMD-A/LCD_DATA18-A
86	PC2/A18/MTIOC4B/TCLKA/PO21/ET_RX_DV/RXD5/SMISO5/SSCL5/SSLA3/IERXD	PC2/A18/MTIOC4B/TCLKA/PO21/ET0_RX_DV/RXD5/SMISO5/SSCL5/SSLA3-A/SDHI_D3-A/SDSI_D3-A/MMC_CD-A/LCD_DATA19-A
87	P75/CS5#/PO20/ET_ERXD0/RMII_RXD0/SCK11	P75/CS5#/PO20/ET0_ERXD0/RMII0_RXD0/SCK11/RTS11#/SDHI_D2-A/SDSI_D2-A/MMC_RES#-A/LCD_DATA20-A
88	P74/CS4#/PO19/ET_ERXD1/RMII_RXD1/CTS11#/RTS11#/SS11#	P74/A20/CS4#/PO19/ET0_ERXD1/RMII0_RXD1/SS11#/CTS11#/LCD_DATA21-A
89	PC1/A17/MTIOC3A/TCLKD/PO18/ET_ERXD2/SCK5/SSLA2/SDA3/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/ET0_ERXD2/SCK5/SSLA2-A/LCD_DATA22-A/IRQ12
90	VCC	VCC
91	PC0/A16/MTIOC3C/TCLKC/PO17/ET_ERXD3/CTS5#/RTS5#/SS5#/SSLA1/SCL3/IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/ET0_ERXD3/CTS5#/RTS5#/SS5#/SSLA1-A/IRQ14
92	VSS	VSS
93	P73/CS3#/PO16/ET_WOL	P73/CS3#/PO16/ET0_WOL/LCD_EXTCLK-A
94	PB7/A15/MTIOC3B/TIOCB5/PO31/ET_CRS/RMII_CRS_DV/TXD9/SMOSI9/SSDA9	PB7/A15/MTIOC3B/TIOCB5/PO31/ET0_CRS/RMII0_CRS_DV/TXD9/SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/SDSI_D1-B
95	PB6/A14/MTIOC3D/TIOCA5/PO30/ET_ETXD1/RMII_TXD1/RXD9/SMISO9/SSCL9	PB6/A14/MTIOC3D/TIOCA5/PO30/ET0_ETXD1/RMII0_TXD1/RXD9/SMISO9/SSCL9/SMISO11/SSCL11/RXD11/SDSI_D0-B
96	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE1#/ET_ETXD0/RMII_TXD0/SCK9	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE4#/ET0_ETXD0/RMII0_TXD0/SCK9/SCK11/SDSI_CLK-B/LCD_CLK-B
97	PB4/A12/TIOCA4/PO28/ET_TX_EN/RMII_TXD_EN/CTS9#/RTS9#/SS9#	PB4/A12/TIOCA4/PO28/ET0_TX_EN/RMII0_TXD_EN/CTS9#/RTS9#/SS9#/SS11#/CTS11#/RTS11#/SDSI_CMD-B/LCD_TCON0-B
98	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE3#/ET_RX_ER/RMII_RX_ER/SCK4/SCK6	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE11#/ET0_RX_ER/RMII0_RX_ER/SCK4/SCK6/SDSI_D3-B/LCD_TCON1-B
99	PB2/A10/TIOCC3/TCLKC/PO26/ET_RX_CLK/REF50CK/CTS4#/RTS4#/CTS6#/RTS6#/SS4#/SS6#	PB2/A10/TIOCC3/TCLKC/PO26/ET0_RX_CLK/REF50CK0/CTS4#/RTS4#/SS4#/CTS6#/RTS6#/SS6#/SDSI_D2-B/LCD_TCON2-B

176-Pin	RX63N	RX65N
100	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/ET_ERXD0/RMII_RXD0/TXD4/TXD6/SMOSI4/SMOSI6/SSDA4/SSDA6/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/ET0_ERXD0/RMII0_RXD0/TXD4/SMOSI4/SSDA4/TXD6/SMOSI6/SSDA6/LCD_TCON3-B/IRQ4-DS
101	P72/CS2#/ET_MDC	P72/A19/CS2#/ET0_MDC/LCD_DATA23-A
102	P71/CS1#/ET_MDIO	P71/A18/CS1#/ET0_MDIO
103	VCC	VCC
104	PB0/A8/MTIC5W/TIOCA3/PO24/ET_ERXD1/RMII_RXD1/RXD4/RXD6/SMISO4/SMISO6/SSCL4/SSCL6/RSPCKA/IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/ET0_ERXD1/RMII0_RXD1/RXD4/SMISO4/SSCL4/RXD6/SMISO6/SSCL6/LCD_DATA0-B/IRQ12
105	VSS	VSS
106	PA7/A7/TIOCB2/PO23/ET_WOL/MISOA	PA7/A7/TIOCB2/PO23/ET0_WOL/MISOA-B/LCD_DATA1-B
107	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE2#/ET_EXOUT/CTS5#/RTS5#/SS5#/MOSIA	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE10#/ET0_EXOUT/CTS5#/RTS5#/SS5#/MOSIA-B/LCD_DATA2-B
108	PA5/A5/TIOCB1/PO21/ET_LINKSTA/RSPCKA	PA5/A5/MTIOC6B/TIOCB1/PO21/ET0_LINKSTA/RSPCKA-B/LCD_DATA3-B
109	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/ET_MDC/TXD5/SMOSI5/SSDA5/SSLA0/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/ET0_MDC/TXD5/SMOSI5/SSDA5/SSLA0-B/LCD_DATA4-B/IRQ5-DS
110	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/ET_MDIO/RXD5/SMISO5/SSCL5/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/ET0_MDIO/RXD5/SMISO5/SSCL5/LCD_DATA5-B/IRQ6-DS
111	TRDATA3/PG7/D31	TRDATA3/PG7/D31
112	PA2/A2/PO18/RXD5/SMISO5/SSCL5/SSLA3	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/SSCL5/SSLA3-B/LCD_DATA6-B
113	TRDATA2/PG6/D30	TRDATA2/PG6/D30
114	PA1/A1/DQM3/MTIOC0B/MTCLKC/TIOCB0/PO17/ET_WOL/SCK5/SSLA2/IRQ11	PA1/DQM3/A1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/PO17/ET0_WOL/SCK5/SSLA2-B/LCD_DATA7-B/IRQ11
115	VCC	VCC
116	TRCLK/PG5/D29	TRCLK/PG5/D29
117	VSS	VSS
118	PA0/A0/BC0#/DQM2/MTIOC4A/TIOCA0/PO16/ET_TX_EN/RMII_TXD_EN/SSLA1	PA0/DQM2/BC0#/A0/MTIOC4A/MTIOC6D/TIOCA0/PO16/CACREF/ET0_TX_EN/RMII0_TXD_EN/SSLA1-B/LCD_DATA8-B
119	TRSYNC/PG4/D28	TRSYNC/PG4/D28
120	P67/CS7#/DQM1/CRX2*2/IRQ15	P67/DQM1/CS7#/MTIOC7C/IRQ15
121	TRDATA1/PG3/D27	TRDATA1/PG3/D27
122	P66/CS6#/DQM0/CTX2*2	P66/DQM0/CS6#/MTIOC7D
123	TRDATA0/PG2/D26	TRDATA0/PG2/D26
124	P65/CS5#/CKE	P65/CKE/CS5#
125	PE7/D15[A15/D15]/TIOCB11/MISOB/IRQ7/AN5	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/TOC1/MISOB-B/SDHI_WP/MMC_RES#-B/LCD_DATA9-B/IRQ7/AN105
126	PE6/D14[A14/D14]/TIOCA11/MOSIB/IRQ6/AN4	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/TIC1/MOSIB-B/SDHI_CD/MMC_CD-B/LCD_DATA10-B/IRQ6/AN104
127	VCC	VCC
128	P70/SDCLK	P70/SDCLK
129	VSS	VSS

176-Pin	RX63N	RX65N
130	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/TIOCB10/ET_RX_CLK/REF50CK/RSPCKB/IRQ5/AN3	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/MTIOC2B/ET0_RX_CLK/REF50CK0/RSPCKB-B/LCD_DATA11-B/IRQ5/AN103
131	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/TIOCA10/PO28/ET_ERXD2/SSLB0/AN2	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/MTIOC1A/PO28/ET0_ERXD2/SSLB0-B/LCD_DATA12-B/AN102
132	PE3/D11[A11/D11]/MTIOC4B/TIOCB9/PO26/POE8#/ET_ERXD3/CTS12#/RTS12#/SS12#/MISOB/AN1	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/PO26/TOC3/POE8#/ET0_ERXD3/CTS12#/RTS12#/SS12#/MMC_D7-B/LCD_DATA13-B/AN101
133	PE2/D10[A10/D10]/MTIOC4A/TIOCA9/PO23/RXD12/SMISO12/SSCL12/RXDX12/SSLB3/MOSIB/IRQ7-DS/AN0	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/PO23/TIC3/RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B/MMC_D6-B/LCD_DATA14-B/IRQ7-DS/AN100
134	PE1/D9[A9/D9]/MTIOC4C/TIOCD9/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2/RSPCKB/ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B/MMC_D5-B/LCD_DATA15-B/ANEX1
135	PE0/D8[A8/D8]/TIOCC9/SCK12/SSLB1/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/SCK12/SSLB1-B/MMC_D4-B/LCD_DATA16-B/ANEX0
136	P64/CS4#/WE#	P64/WE#/D3[A3/D3]/CS4#
137	P63/CS3#/CAS#	P63/CAS#/D2[A2/D2]/CS3#
138	P62/CS2#/RAS#	P62/RAS#/D1[A1/D1]/CS2#
139	P61/CS1#/SDCS#	P61/SDCS#/D0[A0/D0]/CS1#
140	VSS	VSS
141	P60/CS0#	P60/CS0#
142	VCC	VCC
143	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3/IRQ7/AN7	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B/LCD_DATA17-B/IRQ7/AN107
144	PG1/D25	TRDATA7/PG1/D25
145	PD6/D6[A6/D6]/MTIC5V/POE1#/SSLC2/IRQ6/AN6	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/MMC_D0-B/LCD_DATA18-B/IRQ6/AN106
146	PG0/D24	TRDATA6/PG0/D24
147	PD5/D5[A5/D5]/MTIC5W/POE2#/SSLC1/IRQ5/AN013	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/SSLC1-A/QSPCLK-B/SDHI_CLK-B/MMC_CLK-B/LCD_DATA19-B/IRQ5/AN113
148	PD4/D4[A4/D4]/POE3#/SSLC0/IRQ4/AN012	PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0-A/QSSL-B/SDHI_CMD-B/MMC_CMD-B/LCD_DATA20-B/IRQ4/AN112
149	P97/A23/D23	TRSYNC1/P97/D23/A23
150	PD3/D3[A3/D3]/TIOCB8/TCLKH/POE8#/RSPCKC/IRQ3/AN011	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/RSPCKC-A/QIO3-B/SDHI_D3-B/MMC_D3-B/LCD_DATA21-B/IRQ3/AN111
151	VSS	VSS
152	P96/A22/D22	TRDATA5/P96/D22/A22
153	VCC	VCC
154	PD2/D2[A2/D2]/MTIOC4D/TIOCA8/MISOC/CRX0/IRQ2/AN010	PD2/D2[A2/D2]/MTIOC4D/TIC2/MISOC-A/CRX0/QIO2-B/SDHI_D2-B/MMC_D2-B/LCD_DATA22-B/IRQ2/AN110
155	P95/A21/D21	TRDATA4/P95/D21/A21

176-Pin	RX63N	RX65N
156	PD1/D1[A1/D1]/MTIOC4B/TIOCB7/TCLKG/MOSIC/CTX0/IRQ1/AN009	PD1/D1[A1/D1]/MTIOC4B/POE0#/MOSIC-A/CTX0/LCD_DATA23-B/IRQ1/AN109
157	P94/A20/D20	P94/D20/A20
158	PD0/D0[A0/D0]/TIOCA7/IRQ0/AN008	PD0/D0[A0/D0]/POE4#/LCD_EXTCLK-B/IRQ0/AN108
159	P93/A19/D19/CTS7#/RTS7#/SS7#/AN017	P93/D19/A19/POE0#/CTS7#/RTS7#/SS7#/AN117
160	P92/A18/D18/RXD7/SMISO7/SSCL7/AN016	P92/D18/A18/POE4#/RXD7/SMISO7/SSCL7/AN116
161	P91/A17/D17/SCK7/AN015	P91/D17/A17/SCK7/AN115
162	VSS	VSS
163	P90/A16/D16/TXD7/SMOSI7/SSDA7/AN014	P90/D16/A16/TXD7/SMOSI7/SSDA7/AN114
164	VCC	VCC
165	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
166	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
167	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
168	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
169	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
170	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
171	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
172	VREFL0	VREFL0
173	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
174	VREFH0	VREFH0
175	AVCC0	AVCC0
176	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#

Notes: 1. When the external bus is enabled, P53, which is multiplexed with the BCLK pin, cannot be used as an I/O port.
2. Valid only on products with a ROM capacity of 2 MB or 1.5 MB.

3.3 144-/145-Pin Package

Table 3.3 shows a comparative listing of the pin functions on the 144-/145-pin package.

Table 3.3 Comparative Listing of Pin Functions on 144-/145-Pin Package

144-Pin LFQFP	145-Pin TFLGA	RX63N	RX65N
1	A1	AVSS0	AVSS0
2	B3	P05/IRQ13/DA1	P05/IRQ13/DA1
3	B1	VREFH	AVCC1
4	D3	P03/IRQ11/DA0	P03/IRQ11/DA0
5	C1	VREFL	AVSS1
6	C2	P02/TMCI1/SCK6/IRQ10/AN020	P02/TMCI1/SCK6/IRQ10/AN120
7	D4	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/AN019	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/AN119
8	D1	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/AN018	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/AN118
9	D2	PF5/IRQ4	PF5/IRQ4
10	E4	EMLE	EMLE
11	E3	PJ5	PJ5/POE8#/CTS2#/RTS2#/SS2#
12	A10	VSS	VSS
13	F3	PJ3/MTIOC3C/CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0#	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0#
14	E2	VCL	VCL
15	F4	VBATT	VBATT
16	G3	MD/FINED	MD/FINED
17	F1	XCIN	XCIN
18	F2	XCOUT	XCOUT
19	G2	RES#	RES#
20	G1	P37/XTAL	P37/XTAL
21	C6	VSS	VSS
22	H1	P36/EXTAL	P36/EXTAL
23	B10	VCC	VCC
24	H4	P35/NMI	P35/UPSEL/NMI
25	J1	P34/TRST#/MTIOC0A/TMCI3/PO12/POE2#/SCK6/SCK0/USB0_DPRPD/IRQ4	P34/TRST#/MTIOC0A/TMCI3/PO12/POE10#/SCK6/SCK0/ET0_LINKSTA/IRQ4
26	J2	P33/MTIOC0D/TIOCD0/TMRI3/PO11/POE3#/RXD6/RXD0/SMISO6/SMISO0/SSCL6/SSCL0/CRX0/PCKO/IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/POE4#/POE11#/RXD6/RXD0/SMISO6/SMISO0/SSCL6/SSCL0/CRX0/PCKO/IRQ3-DS
27	J3	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCOUT/RTCIC2/TXD6/TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCOUT/RTCIC2/POE0#/POE10#/TXD6/TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS
28	K3	P31/TMS/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0/USB0_DPUPE/IRQ1-DS	P31/TMS/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS
29	J4	P30/TDI/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB/USB0_DRPD/IRQ0-DS	P30/TDI/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS

144-Pin LFQFP	145-Pin TFLGA	RX63N	RX65N
30	K1	P27/TCK/FINEC/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB	P27/TCK/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB-A
31	K2	P26/TDO/CS6#/MTIOC2A/TMO1/PO6/TXD1/CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/MOSIB	P26/TDO/CS6#/MTIOC2A/TMO1/PO6/TXD1/CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/MOSIB-A
32	L1	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/USB0_DPRPD/HSYNC/ADTRG0#	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/HSYNC/ADTRG0#/(SDHI_CD)*1
33	L4	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/PIXCLK	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/PIXCLK/(SDHI_WP)*1
34	L2	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/SSDA3/USB0_DPUPE/PIXD7	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/SSDA3/PIXD7/(SDHI_D1-C)*1
35	M1	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_DRPD/PIXD6	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB/PIXD6/(SDHI_D0-C)*1
36	N1	P21/MTIOC1B/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/SCL1/USB0_EXICEN/PIXD5/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/USB0_EXICEN/PIXD5/IRQ9/(SCL1/SDHI_CLK-C)*1
37	N2	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/SDA1/USB0_ID/PIXD4/IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/USB0_ID/PIXD4/IRQ8/(SDA1/SDHI_CMD-C)*1
38	M2	P17/MTIOC3A/MTIOC3B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/MISOA/SDA2-DS/IETXD/PIXD3/IRQ7/ADTRG#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/PIXD3/IRQ7/ADTRG1#/(SDHI_D3-C)*1
39	N3	P87/TIOCA2/PIXD2	P87/MTIOC4C/TIOCA2/TXD10/SMOSI10/SSDA10/PIXD2/(SDHI_D2-C)*1
40	L3	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/SMISO3/SSDA1/SSCL3/MOSIA/SCL2-DS/IERXD/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/SMISO3/SSDA1/SSCL3/SCL2-DS/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0#
41	M3	P86/TIOCA0/PIXD1	P86/MTIOC4D/TIOCA0/RXD10/SMISO10/SSCL10/PIXD1
42	K4	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/CRX1-DS/PIXD0/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/CRX1-DS/PIXD0/IRQ5
43	N4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_DPUPE/USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/IRQ4
44	L5	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG#	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG1#
45	M4	P12/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/IRQ2	P12/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/IRQ2
46	M5	VCC_USB	VCC_USB
47	N5	USB0_DM	USB0_DM

144-Pin LFQFP	145-Pin TFLGA	RX63N	RX65N
48	N6	USB0_DP	USB0_DP
49	M6	VSS_USB	VSS_USB
50	L6	P56/EDACK1/MTIOC3C/TIOCA1	P56/EDACK1/MTIOC3C/TIOCA1/(SCK7)*1
51	N7	P55/TRDATA3/WAIT#/EDREQ0/MTIOC4D/TMO3/CRX1/ET_EXOUT/IRQ10	P55/TRDATA3/WAIT#/EDREQ0/MTIOC4D/TMO3/CRX1/ET0_EXOUT/IRQ10/(D0[A0/D0]/ TXD7/SMOSI7/SSDA7)*1
52	K5	P54/TRDATA2/ALE/EDACK0/MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/CTX1/ET_LINKSTA	P54/TRDATA2/ALE/EDACK0/MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/CTX1/ET0_LINKSTA/(D1[A1/D1])*1
53	K6	P53/BCLK	P53/BCLK
54	L7	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A
55	K7	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A
56	M7	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A
57	C13	VSS	VSS
58	L8	P83/TRCLK/EDACK1/MTIOC4C/CTS10#/RTS10#/SS10#/ET_CRS/RMII_CRS_DV	P83/TRCLK/EDACK1/MTIOC4C/CTS10#/SS10#/ET0_CRS/RMII0_CRS_DV/SCK10
59	D5	VCC	VCC
60	N9	PC7/A23/CS0#/MTIOC3A/MTCLKB/TIOCB6/TMO2/PO31/TXD8/SMOSI8/SSDA8/MISOA/ET_COL/IRQ14	PC7/UB/A23/CS0#/MTIOC3A/MTCLKB/TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/SSDA8/MISOA-A/ET0_COL/TXD10/SMOSI10/SSDA10/MMC_D7-A/IRQ14
61	M8	PC6/A22/CS1#/MTIOC3C/MTCLKA/TIOCA6/TMCI2/PO30/RXD8/SMISO8/SSCL8/MOSIA/ET_ETXD3/IRQ13	PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/TIC0/PO30/RXD8/SMISO8/SSCL8/MOSIA-A/ET0_ETXD3/RXD10/SMISO10/SSCL10/MMC_D6-A/IRQ13/(D2[A2/D2])*1
62	L9	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TIOCD6/TCLKF/TMRI2/PO29/SCK8/RSPCKA/ET_ETXD2	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/PO29/SCK8/RSPCKA-A/ET0_ETXD2/SCK10/MMC_D5-A/(D3[A3/D3])*1
63	N10	P82/TRSYNC/EDREQ1/MTIOC4A/PO28/TXD10/SMOSI10/SSDA10/ET_ETXD1/RMII_TXD1	P82/TRSYNC/EDREQ1/MTIOC4A/PO28/TXD10/SMOSI10/SSDA10/ET0_ETXD1/RMII0_TXD1/MMC_D4-A
64	M9	P81/TRDATA1/EDACK0/MTIOC3D/PO27/RXD10/SMISO10/SSCL10/ET_ETXD0/RMII_TXD0	P81/TRDATA1/EDACK0/MTIOC3D/PO27/RXD10/SMISO10/SSCL10/ET0_ETXD0/RMII0_TXD0/MMC_D3-A/SDHI_CD-A/QIO3-A/(SDHI_CD)*1
65	K9	P80/TRDATA0/EDREQ0/MTIOC3B/PO26/SCK10/ET_TX_EN/RMII_TXD_EN	P80/TRDATA0/EDREQ0/MTIOC3B/PO26/SCK10/RTS10#/ET0_TX_EN/RMII0_TXD_EN/MMC_D2-A/SDHI_WP-A/QIO2-A/(SDHI_WP)*1
66	L10	PC4/A20/CS3#/MTIOC3D/MTCLKC/TIOCC6/TCLKE/TMCI1/PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0/ET_TX_CLK	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0-A/ET0_TX_CLK/CTS10#/RTS10#/SS10#/MMC_D1-A/SDHI_D1-A/SDSI_D1-A/QIO1-A/QMI-A

144-Pin LFQFP	145-Pin TFLGA	RX63N	RX65N
67	N11	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/SMOSI5/SSDA5/IETXD/ET_TX_ER	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/SMOSI5/SSDA5/ET0_TX_ER/MMC_D0-A/SDHI_D0-A/SDSI_D0-A/QIO0-A/QMO-A
68	M10	P77/CS7#/PO23/TXD11/SMOSI11/SSDA11/ET_RX_ER/RMII_RX_ER	P77/TRDATA7/CS7#/PO23/TXD11/SMOSI10/SSDA10/ET0_RX_ER/RMII0_RX_ER/MMC_CLK-A/SDHI_CLK-A/SDSI_CLK-A/QSPCLK-A
69	K10	P76/CS6#/PO22/RXD11/SMISO11/SSCL11/ET_RX_CLK/REF50CK	P76/TRDATA6/CS6#/PO22/RXD11/SMISO11/SSCL11/ET0_RX_CLK/REF50CK0/MMC_CMD-A/SDHI_CMD-A/SDSI_CMD-A/QSSL-A
70	L11	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/SMISO5/SSCL5/SSLA3/IERXD/ET_RX_DV	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/SMISO5/SSCL5/SSLA3-A/ET0_RX_DV/MMC_CD-A/SDHI_D3-A/SDSI_D3-A
71	N12	P75/CS5#/PO20/SCK11/ET_ERXD0/RMII_RXD0	P75/TRSYNC1/CS5#/PO20/SCK11/RTS11#/ET0_ERXD0/RMII0_RXD0/MMC_RES#-A/SDHI_D2-A/SDSI_D2-A
72	N13	P74/CS4#/PO19/CTS11#/RTS11#/SS11#/ET_ERXD1/RMII_RXD1	P74/TRDATA5/A20/CS4#/PO19/CTS11#/SS11#/ET0_ERXD1/RMII0_RXD1
73	M12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/SSLA2/SDA3/ET_ERXD2/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/SSLA2-A/ET0_ERXD2/IRQ12
74	D11	VCC	VCC
75	M11	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1/SCL3/ET_ERXD3/IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14
76	E1	VSS	VSS
77	L12	P73/CS3#/PO16/ET_WOL	P73/TRDATA4/CS3#/PO16/ET0_WOL
78	K11	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/SMOSI9/SSDA9/ET_CRS/RMII_CRS_DV	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/SMOSI9/SSDA9/ET0_CRS/RMII0_CRS_DV/TXD11/SMOSI11/SSDA11/SDSI_D1-B
79	K12	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/SMISO9/SSCL9/ET_ETXD1/RMII_TXD1	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/SMISO9/SSCL9/ET0_ETXD1/RMII0_TXD1/RXD11/SMISO11/SSCL11/SDSI_D0-B
80	K13	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE1#/SCK9/ET_ETXD0/RMII_TXD0	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE4#/SCK9/ET0_ETXD0/RMII0_TXD0/SCK11/SDSI_CLK-B/(LCD_CLK-B)*1
81	J11	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/SS9#/ET_TX_EN/RMII_TXD_EN	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/SS9#/ET0_TX_EN/RMII0_TXD_EN/CTS11#/RTS11#/SS11#/SDSI_CMD-B/(LCD_TCON0-B)*1
82	J10	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE3#/SCK4/SCK6/ET_RX_ER/RMII_RX_ER	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ET0_RX_ER/RMII0_RX_ER/SDSI_D3-B/(LCD_TCON1-B)*1
83	J12	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/RTS4#/CTS6#/RTS6#/SS4#/SS6#/ET_RX_CLK/REF50CK	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/RTS4#/CTS6#/RTS6#/SS4#/SS6#/ET0_RX_CLK/REF50CK0/SDSI_D2-B/(LCD_TCON2-B)*1

144-Pin LFQFP	145-Pin TFLGA	RX63N	RX65N
84	J13	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/TXD4/TXD6/SMOSI4/SMOSI6/SSDA4/SSDA6/ET_ERXD0/RMII_RXD0/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/TXD4/TXD6/SMOSI4/SMOSI6/SSDA4/SSDA6/ET0_ERXD0/RMII0_RXD0/IRQ4-DS/(LCD_TCON3-B)*1
85	H10	P72/CS2#/ET_MDC	P72/A19/CS2#/ET0_MDC
86	H11	P71/CS1#/ET_MDIO	P71/A18/CS1#/ET0_MDIO
87	H12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/RXD6/SMISO4/SMISO6/SSCL4/SSCL6/RSPCKA/ET_ERXD1/RMII_RXD1/IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/RXD6/SMISO4/SMISO6/SSCL4/SSCL6/ET0_ERXD1/RMII0_RXD1/IRQ12/(LCD_DATA0-B)*1
88	H13	PA7/A7/TIOCB2/PO23/MISOA/ET_WOL	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/(LCD_DATA1-B)*1
89	G11	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE2#/CTS5#/RTS5#/SS5#/MOSIA/ET_EXOUT	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE10#/CTS5#/RTS5#/SS5#/MOSIA-B/ET0_EXOUT/(LCD_DATA2-B)*1
90	G10	PA5/A5/TIOCB1/PO21/RSPCKA/ET_LINKSTA	PA5/A5/MTIOC6B/TIOCB1/PO21/RSPCKA-B/ET0_LINKSTA/(LCD_DATA3-B)*1
91	G12	VCC	VCC
92	G13	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/TXD5/SMOSI5/SSDA5/SSLA0/ET_MDC/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ET0_MDC/IRQ5-DS/(LCD_DATA4-B)*1
93	F11	VSS	VSS
94	F10	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/RXD5/SMISO5/SSCL5/ET_MDIO/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/RXD5/SMISO5/SSCL5/ET0_MDIO/IRQ6-DS/(LCD_DATA5-B)*1
95	F13	PA2/A2/PO18/RXD5/SMISO5/SSCL5/SSLA3	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/SSCL5/SSLA3-B/(LCD_DATA6-B)*1
96	F12	PA1/A1/MTIOC0B/MTCLKC/TIOCB0/PO17/SCK5/SSLA2/ET_WOL/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/PO17/SCK5/SSLA2-B/ET0_WOL/IRQ11/(LCD_DATA7-B)*1
97	E10	PA0/A0/BC0#/MTIOC4A/TIOCA0/PO16/SSLA1/ET_TX_EN/RMII_TXD_EN	PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/CACREF/PO16/SSLA1-B/ET0_TX_EN/RMII0_TXD_EN/(LCD_DATA8-B)*1
98	E13	P67/CS7#/DQM1/CRX2/IRQ15	P67/CS7#/DQM1/MTIOC7C/IRQ15
99	E11	P66/CS6#/DQM0/CTX2	P66/CS6#/DQM0/MTIOC7D
100	E12	P65/CS5#/CKE	P65/CS5#/CKE
101	D10	PE7/D15[A15/D15]/TIOCB11/MISOB/IRQ7/AN5	PE7/D15[A15/D15]/MTIOC6A/TOC1/MISOB-B/MMC_RES#-B/SDHI_WP-B/IRQ7/AN105/(D7[A7/D7]/ LCD_DATA9-B)*1
102	D13	PE6/D14[A14/D14]/TIOCA11/MOSIB/IRQ6/AN4	PE6/D14[A14/D14]/MTIOC6C/TIC1/MOSIB-B/MMC_CD-B/SDHI_CD-B/IRQ6/AN104/(D6[A6/D6]/ SDHI_CD/LCD_DATA10-B)*1
103	H2	VCC	VCC
104	C12	P70/SDCLK	P70/SDCLK
105	H3	VSS	VSS
106	D12	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/TIOCB10/RSPCKB/ET_RX_CLK/REF50CK/IRQ5/AN3	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/ET0_RX_CLK/REF50CK0/RSPCKB-B/IRQ5/AN103/(D5[A5/D5]/ LCD_DATA11-B)*1

144-Pin LFQFP	145-Pin TFLGA	RX63N	RX65N
107	B13	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/TIOCA10/PO28/SSLB0/ET_ERXD2/AN2	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/PO28/ET0_ERXD2/SSLB0-B/AN102/(D4[A4/D4]/ LCD_DATA12-B)*1
108	A13	PE3/D11[A11/D11]/MTIOC4B/TIOCB9/PO26/POE8#/CTS12#/RTS12#/SS12#/MISOB/ET_ERXD3/AN1	PE3/D11[A11/D11]/MTIOC4B/PO26/POE8#/TOC3/CTS12#/RTS12#/SS12#/ET0_ERXD3/MMC_D7-B/AN101/(D3[A3/D3]/ LCD_DATA13-B)*1
109	B12	PE2/D10[A10/D10]/MTIOC4A/TIOCA9/PO23/RXD12/SMISO12/SSCL12/RXDX12/SSLB3/MOSIB/IRQ7-DS/AN0	PE2/D10[A10/D10]/MTIOC4A/PO23/TIC3/RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B/MMC_D6-B/IRQ7-DS/AN100/(D2[A2/D2]/ LCD_DATA14-B)*1
110	A12	PE1/D9[A9/D9]/MTIOC4C/TIOCD9/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2/RSPCKB/ANEX1	PE1/D9[A9/D9]/MTIOC4C/MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B/MMC_D5-B/ANEX1/(D1[A1/D1]/ LCD_DATA15-B)*1
111	C11	PE0/D8[A8/D8]/TIOCC9/SCK12/SSLB1/ANEX0	PE0/D8[A8/D8]/MTIOC3D/SCK12/SSLB1-B/MMC_D4-B/ANEX0/(D0[A0/D0]/ LCD_DATA16-B)*1
112	D9	P64/CS4#/WE#	P64/CS4#/WE#/(D3[A3/D3])*1
113	C10	P63/CS3#/CAS#	P63/CS3#/CAS#/(D2[A2/D2])*1
114	A11	P62/CS2#/RAS#	P62/CS2#/RAS#/(D1[A1/D1])*1
115	B11	P61/CS1#/SDCS#	P61/CS1#/SDCS#/(D0[A0/D0])*1
116	L13	VSS	VSS
117	D8	P60/CS0#	P60/CS0#
118	K8	VCC	VCC
119	C9	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3/IRQ7/AN7	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3/MMC_D1-B/SDHI_D1-B/QIO1-B/QMI-B/IRQ7/AN107/(SSLC3-A/LCD_DATA17-B)*1
120	A9	PD6/D6[A6/D6]/MTIC5V/POE1#/SSLC2/IRQ6/AN6	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/SSLC2/MMC_D0-B/SDHI_D0-B/QIO0-B/QMO-B/IRQ6/AN106/(SSLC2-A/LCD_DATA18-B)*1
121	D7	PD5/D5[A5/D5]/MTIC5W/POE2#/SSLC1/IRQ5/AN013	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/SSLC1/MMC_CLK-B/SDHI_CLK-B/QSPCLK-B/IRQ5/AN113/(SSLC1-A/LCD_DATA19-B)*1
122	B9	PD4/D4[A4/D4]/POE3#/SSLC0/IRQ4/AN012	PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0/MMC_CMD-B/SDHI_CMD-B/QSSL-B/IRQ4/AN112/(SSLC0-A/LCD_DATA20-B)*1
123	C8	PD3/D3[A3/D3]/TIOCB8/TCLKH/POE8#/RSPCKC/IRQ3/AN011	PD3/D3[A3/D3]/MTIOC8D/POE8#/TOC2/RSPCKC/MMC_D3-B/SDHI_D3-B/QIO3-B/IRQ3/AN111/(RSPCKC-A/LCD_DATA21-B)*1
124	A8	PD2/D2[A2/D2]/MTIOC4D/TIOCA8/MISOC/CRX0/IRQ2/AN010	PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0/MISOC/MMC_D2-B/SDHI_D2-B/QIO2-B/IRQ2/AN110/(MISOC-A/LCD_DATA22-B)*1
125	C7	PD1/D1[A1/D1]/MTIOC4B/TIOCB7/TCLKG/MOSIC/CTX0/IRQ1/AN009	PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0/MOSIC/IRQ1/AN109/(MOSIC-A/LCD_DATA23-B)*1

144-Pin LFQFP	145-Pin TFLGA	RX63N	RX65N
126	B8	PD0/D0[A0/D0]/TIOCA7/IRQ0/AN008	PD0/D0[A0/D0]/POE4#/IRQ0/AN108/(LCD_EXTCLK-B)*1
127	D6	P93/A19/CTS7#/RTS7#/SS7#/AN017	P93/A19/POE0#/CTS7#/RTS7#/SS7#/AN117
128	A7	P92/A18/RXD7/SMISO7/SSCL7/AN016	P92/A18/POE4#/RXD7/SMISO7/SSCL7/AN116
129	B7	P91/A17/SCK7/AN015	P91/A17/SCK7/AN115
130	N8	VSS	VSS
131	A6	P90/A16/TXD7/SMOSI7/SSDA7/AN014	P90/A16/TXD7/SMOSI7/SSDA7/AN114
132	M13	VCC	VCC
133	B6	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
134	C5	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
135	A5	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
136	E5	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
137	B5	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
138	A4	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
139	C4	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
140	B4	VREFL0	VREFL0
141	A3	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
142	C3	VREFH0	VREFH0
143	B2	AVCC0	AVCC0
144	A2	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
—	G4	—	BSCANP

Note: 1. Can be used for products with at least 1.5 MB of code flash memory.

3.4 100-Pin Package

Table 3.4 shows a comparative listing of the pin functions on the 100-pin package.

Table 3.4 Comparative Listing of Pin Functions on 100-Pin Package

100-Pin LFQFP	100-Pin TFLGA	RX63N	RX65N
1	A2	VREFH	AVCC1
2	B1	EMLE	EMLE
3	C2	VREFL	AVSS1
4	C3	PJ3/MTIOC3C/CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0#	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0#
5	C1	VCL	VCL
6	D4	VBATT	VBATT
7	D3	MD/FINED	MD/FINED
8	D1	XCIN	XCIN
9	D2	XCOUT	XCOUT
10	E3	RES#	RES#
11	E1	P37/XTAL	P37/XTAL
12	E2	VSS	VSS
13	F1	P36/EXTAL	P36/EXTAL
14	F2	VCC	VCC
15	F3	P35/NMI	P35/UPSEL/NMI
16	E4	P34/TRST#/MTIOC0A/TMCI3/PO12/POE2#/SCK6/SCK0/USB0_DPRPD/IRQ4	P34/TRST#/MTIOC0A/TMCI3/PO12/POE10#/SCK6/SCK0/ET0_LINKSTA/IRQ4
17	G1	P33/MTIOC0D/TIOCD0/TMRI3/PO11/POE3#/RXD6/RXD0/SMISO6/SMISO0/SSCL6/SSCL0/CRX0/IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/POE4#/POE11#/RXD6/RXD0/SMISO6/SMISO0/SSCL6/SSCL0/CRX0/IRQ3-DS
18	F4	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCOUT/RTCIC2/TXD6/TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/CTX0/USB0_VBUSEN/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCOUT/RTCIC2/POE0#/POE10#/TXD6/TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/CTX0/USB0_VBUSEN/IRQ2-DS
19	G2	P31/TMS/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0/USB0_DPUPE/IRQ1-DS	P31/TMS/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS
20	G3	P30/TDI/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB/USB0_DRPD/IRQ0-DS	P30/TDI/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS
21	G4	P27/TCK/FINEC/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB	P27/TCK/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB-A
22	H1	P26/TDO/CS6#/MTIOC2A/TMO1/PO6/TXD1/CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/MOSIB	P26/TDO/CS6#/MTIOC2A/TMO1/PO6/TXD1/CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/MOSIB-A
23	H2	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/USB0_DPRPD/ADTRG0#	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/ADTRG0#
24	J1	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN
25	K1	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/SSDA3/USB0_DPUPE	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/SSDA3

100-Pin LFQFP	100-Pin TFLGA	RX63N	RX65N
26	K2	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_DRPD	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB
27	J2	P21/MTIOC1B/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/USB0_EXICEN/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/USB0_EXICEN/IRQ9/(SCL1)*1
28	K3	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/USB0_ID/IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/USB0_ID/IRQ8/(SDA1)*1
29	J3	P17/MTIOC3A/MTIOC3B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/MISOA/SDA2-DS/IETXD/IRQ7/ADTRG#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/IRQ7/ADTRG1#
30	H3	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/SMISO3/SSDA1/SSCL3/MOSIA/SCL2-DS/IERXD/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/SMISO3/SSDA1/SSCL3/SCL2-DS/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0#
31	H4	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/CRX1-DS/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/CRX1-DS/IRQ5
32	K4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_DPUPE/USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/IRQ4
33	J4	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG#	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG1#
34	F5	P12/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/IRQ2	P12/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/IRQ2
35	J6	VCC_USB	VCC_USB
36	K5	USB0_DM	USB0_DM
37	K6	USB0_DP	USB0_DP
38	J5	VSS_USB	VSS_USB
39	H5	P55/WAIT#/EDREQ0/MTIOC4D/TMO3/CRX1/ET_EXOUT/IRQ10	P55/WAIT#/EDREQ0/MTIOC4D/TMO3/CRX1/ET0_EXOUT/IRQ10/(D0[A0/D0])*1
40	H6	P54/ALE/EDACK0/MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/CTX1/ET_LINKSTA	P54/ALE/EDACK0/MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/CTX1/ET0_LINKSTA/(D1[A1/D1])*1
41	G5	P53/BCLK	P53/BCLK
42	G6	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A
43	K7	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A
44	J7	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A
45	H7	PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/PO31/TXD8/SMOSI8/SSDA8/MISOA/ET_COL/IRQ14	PC7/UB/A23/CS0#/MTIOC3A/MTCLKB/TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/SSDA8/MISOA-A/ET0_COL/TXD10/SMOSI10/SSDA10/IRQ14

100-Pin LFQFP	100-Pin TFLGA	RX63N	RX65N
46	H8	PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/PO30/RXD8/SMISO8/SSCL8/MOSIA/ET_ETXD3/IRQ13	PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/TIC0/PO30/RXD8/SMISO8/SSCL8/MOSIA-A/ET0_ETXD3/RXD10/SMISO10/SSCL10/IRQ13/(D2[A2/D2])*1
47	K8	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/PO29/SCK8/RSPCKA/ET_ETXD2	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/PO29/SCK8/RSPCKA-A/ET0_ETXD2/SCK10/(D3[A3/D3])*1
48	J8	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0/ET_TX_CLK	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0-A/ET0_TX_CLK/CTS10#/RTS10#/SS10#
49	K9	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/SMOSI5/SSDA5/IETXD/ET_TX_ER	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/SMOSI5/SSDA5/ET0_TX_ER
50	K10	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/SMISO5/SSCL5/SSLA3/IERXD/ET_RX_DV	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/SMISO5/SSCL5/SSLA3-A/ET0_RX_DV
51	J10	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/SSLA2/ET_ERXD2/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/SSLA2-A/ET0_ERXD2/IRQ12
52	J9	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1/ET_ERXD3/IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14
53	H10	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/SMOSI9/SSDA9/ET_CRS/RMII_CRS_DV	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/SMOSI9/SSDA9/ET0_CRS/RMII0_CRS_DV/TXD11/SMOSI11/SSDA11/SDSI_D1-B
54	H9	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/SMISO9/SSCL9/ET_ETXD1/RMII_TXD1	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/SMISO9/SSCL9/ET0_ETXD1/RMII0_TXD1/RXD11/SMISO11/SSCL11/SDSI_D0-B
55	G7	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE1#/SCK9/ET_ETXD0/RMII_TXD0	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE4#/SCK9/ET0_ETXD0/RMII0_TXD0/SCK11/SDSI_CLK-B/(LCD_CLK-B)*1
56	G8	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/SS9#/ET_TX_EN/RMII_TXD_EN	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/SS9#/ET0_TX_EN/RMII0_TXD_EN/CTS11#/RTS11#/SS11#/SDSI_CMD-B/(LCD_TCON0-B)*1
57	F6	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE3#/SCK6/ET_RX_ER/RMII_RX_ER	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE11#/SCK6/ET0_RX_ER/RMII0_RX_ER/SDSI_D3-B/(LCD_TCON1-B)*1
58	F7	PB2/A10/TIOCC3/TCLKC/PO26/CTS6#/RTS6#/SS6#/ET_RX_CLK/REF50CK	PB2/A10/TIOCC3/TCLKC/PO26/CTS6#/RTS6/#SS6#/ET0_RX_CLK/REF50CK0/SDSI_D2-B/(LCD_TCON2-B)*/
59	G9	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/TXD6/SMOSI6/SSDA6/ET_ERXD0/RMII_RXD0/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/TXD6/SMOSI6/SSDA6/ET0_ERXD0/RMII0_RXD0/IRQ4-DS/(LCD_TCON3-B)*1
60	G10	VCC	VCC
61	F8	PB0/A8/MTIC5W/TIOCA3/PO24/RXD6/SMISO6/SSCL6/RSPCKA/ET_ERXD1/RMII_RXD1/IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD6/SMISO6/SSCL6/ET0_ERXD1/RMII0_RXD1/IRQ12/(LCD_DATA0-B)*1
62	F10	VSS	VSS

100-Pin LFQFP	100-Pin TFLGA	RX63N	RX65N
63	F9	PA7/A7/TIOCB2/PO23/MISOA/ET_WOL	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/(LCD_DATA1-B)*1
64	E7	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE2#/CTS5#/RTS5#/SS5#/MOSIA/ET_EXOUT	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE10#/CTS5#/RTS5#/SS5#/MOSIA-B/ET0_EXOUT/(LCD_DATA2-B)*1
65	E9	PA5/A5/TIOCB1/PO21/RSPCKA/ET_LINKSTA	PA5/A5/MTIOC6B/TIOCB1/PO21/RSPCKA-B/ET0_LINKSTA/(LCD_DATA3-B)*1
66	E8	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/TXD5/SMOSI5/SSDA5/SSLA0/ET_MDC/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ET0_MDC/IRQ5-DS/(LCD_DATA4-B)*1
67	E10	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/RXD5/SMISO5/SSCL5/ET_MDIO/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/RXD5/SMISO5/SSCL5/ET0_MDIO/IRQ6-DS/(LCD_DATA5-B)*1
68	E6	PA2/A2/PO18/RXD5/SMISO5/SSCL5/SSLA3	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/SSCL5/SSLA3-B/(LCD_DATA6-B)*1
69	D9	PA1/A1/MTIOC0B/MTCLKC/TIOCB0/PO17/SCK5/SSLA2/ET_WOL/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/PO17/SCK5/SSLA2-B/ET0_WOL/IRQ11/(LCD_DATA7-B)*1
70	D10	PA0/A0/BC0#/MTIOC4A/TIOCA0/PO16/SSLA1/ET_TX_EN/RMII_TXD_EN	PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/CACREF/PO16/SSLA1-B/ET0_TX_EN/RMII0_TXD_EN/(LCD_DATA8-B)*1
71	D8	PE7/D15[A15/D15]/MISOB/IRQ7/AN5	PE7/D15[A15/D15]/MTIOC6A/TOC1/MISOB-B/MMC_RES#-B/SDHI_WP-B/IRQ7/AN105/(D7[A7/D7]/ LCD_DATA9-B)*1
72	D7	PE6/D14[A14/D14]/MOSIB/IRQ6/AN4	PE6/D14[A14/D14]/MTIOC6C/TIC1/MOSIB-B/MMC_CD-B/SDHI_CD-B/IRQ6/AN104/(D6[A6/D6]/ SDHI_CD/LCD_DATA10-B)*1
73	C9	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/RSPCKB/ET_RX_CLK/REF50CK/IRQ5/AN3	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/ET0_RX_CLK/REF50CK0/RSPCKB-B/IRQ5/AN103/(D5[A5/D5]/ LCD_DATA11-B)*1
74	C10	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/PO28/SSLB0/ET_ERXD2/AN2	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/PO28/ET0_ERXD2/SSLB0-B/AN102/(D4[A4/D4]/ LCD_DATA12-B)*1
75	B10	PE3/D11[A11/D11]/MTIOC4B/PO26/POE8#/CTS12#/RTS12#/SS12#/MISOB/ET_ERXD3/AN1	PE3/D11[A11/D11]/MTIOC4B/PO26/POE8#/TOC3/CTS12#/RTS12#/SS12#/ET0_ERXD3/MMC_D7-B/AN101/(D3[A3/D3]/ LCD_DATA13-B)*1
76	A10	PE2/D10[A10/D10]/MTIOC4A/PO23/RXD12/SMISO12/SSCL12/RXDX12/SSLB3/MOSIB/IRQ7-DS/AN0	PE2/D10[A10/D10]/MTIOC4A/PO23/TIC3/RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B/MMC_D6-B/IRQ7-DS/AN100/(D2[A2/D2]/ LCD_DATA14-B)*1
77	A9	PE1/D9[A9/D9]/MTIOC4C/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2/RSPCKB/ANEX1	PE1/D9[A9/D9]/MTIOC4C/MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B/MMC_D5-B/ANEX1/(D1[A1/D1]/ LCD_DATA15-B)*1
78	A8	PE0/D8[A8/D8]/SCK12/SSLB1/ANEX0	PE0/D8[A8/D8]/MTIOC3D/SCK12/SSLB1-B/MMC_D4-B/ANEX0/(D0[A0/D0]/ LCD_DATA16-B)*1

100-Pin LFQFP	100-Pin TFLGA	RX63N	RX65N
79	B9	PD7/D7[A7/D7]/MTIC5U/POE0#/IRQ7/AN7	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3/MMC_D1-B/SDHI_D1-B/QIO1-B/QMI-B/IRQ7/AN107/(SSLC3-A/LCD_DATA17-B)*1
80	B8	PD6/D6[A6/D6]/MTIC5V/POE1#/IRQ6/AN6	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/SSLC2/MMC_D0-B/SDHI_D0-B/QIO0-B/QMO-B/IRQ6/AN106/(SSLC2-A/LCD_DATA18-B)*1
81	C8	PD5/D5[A5/D5]/MTIC5W/POE2#/IRQ5/AN013	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/SSLC1/MMC_CLK-B/SDHI_CLK-B/QSPCLK-B/IRQ5/AN113/(SSLC1-A/LCD_DATA19-B)*1
82	A7	PD4/D4[A4/D4]/POE3#/IRQ4/AN012	PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0/MMC_CMD-B/SDHI_CMD-B/QSSL-B/IRQ4/AN112/(SSLC0-A/LCD_DATA20-B)*1
83	B7	PD3/D3[A3/D3]/POE8#/IRQ3/AN011	PD3/D3[A3/D3]/MTIOC8D/POE8#/TOC2/RSPCKC/MMC_D3-B/SDHI_D3-B/QIO3-B/IRQ3/AN111/(RSPCKC-A/LCD_DATA21-B)*1
84	C7	PD2/D2[A2/D2]/MTIOC4D/CRX0/IRQ2/AN010	PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0/MISOC/MMC_D2-B/SDHI_D2-B/QIO2-B/IRQ2/AN110/(MISOC-A/LCD_DATA22-B)*1
85	B6	PD1/D1[A1/D1]/MTIOC4B/CTX0/IRQ1/AN009	PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0/MOSIC/IRQ1/AN109/(MOSIC-A/LCD_DATA23-B)*1
86	A6	PD0/D0[A0/D0]/IRQ0/AN008	PD0/D0[A0/D0]/POE4#/IRQ0/AN108/(LCD_EXTCLK-B)*1
87	C6	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
88	D6	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
89	D5	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
90	B5	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
91	A5	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
92	C5	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
93	E5	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
94	A4	VREFL0	VREFL0
95	B4	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
96	C4	VREFH0	VREFH0
97	B3	AVCC0	AVCC0
98	A3	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
99	B2	AVSS0	AVSS0
100	A1	P05/IRQ13/DA1	P05/IRQ13/DA1

Note: 1. Can be used for products with at least 1.5 MB of code flash memory.

3.5 64-Pin Package (RX631: TFLGA, RX651: TFBGA)

Table 3.5 shows a comparative listing of the pin functions on the 64-pin package (RX631: TFLGA, RX651: TFBGA). Note that the RX63N Group and RX65N Group are not available in 64-pin package versions.

Table 3.5 Comparative Listing of Pin Functions on 64-Pin Package (RX631: TFLGA, RX651: TFBGA)

64-Pin	RX631 (64-Pin TFLGA)	RX651 (64-Pin TFBGA)
A1	P05/IRQ13/DA1	AVCC1
A2	AVCC0	AVSS0
A3	VREFH0	VREFH0
A4	VREFL0	VREFL0
A5	VREFH	PD2/MTIOC4D/TIC2/QIO2-B/SDHI_D2-B/IRQ2/AN110
A6	VREFL	PD7/MTIC5U/POE0#/QMI-B/QIO1-B/SDHI_D1-B/IRQ7/AN107
A7	PE2/MTIOC4A/PO23/RXD12/SMISO12/SSCL12/RXDX12/SSLB3/MOSIB/IRQ7-DS/AN010	PE0/MTIOC3D/SCK12/ANEX0
A8	PE3/MTIOC4B/PO26/POE8#/CTS12#/RTS12#/SS12#/MISOB/AN011	PE2/MTIOC4A/TIC3/RXD12/SSCL12/RXDX12/IRQ7-DS
B1	VCL	EMLE
B2	AVSS0	AVSS1
B3	P40/IRQ8-DS/AN000	AVCC0
B4	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
B5	P44/IRQ12-DS/AN004	PD3/MTIOC8D/TOC2/POE8#/QIO3-B/SDHI_D3-B/IRQ3/AN111
B6	P46/IRQ14-DS/AN006	PD6/MTIC5V/MTIOC8A/POE4#/QMO-B/QIO0-B/SDHI_D0-B/IRQ6/AN106
B7	PE1/MTIOC4C/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2/RSPCKB/AN009	PE1/MTIOC4C/MTIOC3B/TXD12/SSDA12/TXDX12/SIOX12/ANEX1
B8	PE4/MTIOC4D/MTIOC1A/PO28/SSLB0/AN012	PE6/MTIOC6C/TIC1/SDHI_CD/IRQ6
C1	XCIN	VCL
C2	MD/FINED	VBATT
C3	EMLE	MD/FINED
C4	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
C5	P43/IRQ11-DS/AN003	PD4/MTIOC8B/POE11#/QSSL-B/SDHI_CMD-B/IRQ4/AN112
C6	PE0/SCK12/SSLB1/AN008	PD5/MTIC5W/MTIOC8C/POE10#/QSPCLK-B/SDHI_CLK-B/IRQ5/AN113
C7	PE5/MTIOC4C/MTIOC2B/RSPCKB/IRQ5/AN013	PA1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/SCK5/IRQ11
C8	PA0/MTIOC4A/TIOCA0/PO16/SSLA1	PE7/MTIOC6A/TOC1/SDHI_WP/IRQ7
D1	XCOUT	XCIN
D2	RES#	XCOUT
D3	TCK/FINEC/P27/MTIOC2B/TMCI3/SCK1/RSPCKB	RES#
D4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/CTS1#/RTS1#/SS1#/CTX1/USB0_DPUPE/USB0_OVRCURA/IRQ4	P40/IRQ8-DS/AN000

64-Pin	RX631 (64-Pin TFLGA)	RX651 (64-Pin TFBGA)
D5	PA6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE2#/CTS5#/RTS5#/SS5#/MOSIA	P43/IRQ11-DS/AN003
D6	PA4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/TXD5/SMOSI5/SSDA5/SSLA0/IRQ5-DS	PA6/MTIC5V/MTCLKB/TIOCA2/TMCI3/POE10#/CTS5#/RTS5#/SS5#
D7	PA1/MTIOC0B/MTCLKC/TIOCB0/PO17/SCK5/SSLA2/SCL2/IRQ11	PA2/MTIOC7A/RXD5/SMISO5/SSCL5
D8	PA3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/RXD5/SMISO5/SSCL5/SDA2/IRQ6-DS	PA4/MTIC5U/MTCLKA/TIOCA1/TMRI0/TXD5/SMOSI5/SSDA5/IRQ5-DS
E1	VSS	XTAL/P37
E2	VBATT	VSS
E3	TDI/P30/MTIOC4B/TMRI3/POE8#/RTCIC0/RXD1/SMISO1/SSCL1/MISOB/USB0_DRPD/IRQ0-DS	TRST#/P34/MTIOC0A/TMCI3/POE10#/IRQ4
E4	TMS/P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/RTCOUT/TXD1/SMOSI1/SSDA1/MOSIA/SCL2-DS/IERXD/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0#	P13/MTIOC0B/TIOCA5/TMO3/TXD2/SSDA2/SDA0[FM+]/IRQ3/ADTRG1#
E5	PC4/MTIOC3D/MTCLKC/TMCI1/PO25/POE0#/SCK5/SSLA0/USB0_DPRPD	BSCANP
E6	VCC	PA7/TIOCB2
E7	VSS	VCC
E8	PB0/MTIC5W/TIOCA3/PO24/RXD6/SMISO6/SSCL6/RSPCKA/IRQ12	VSS
F1	VCC	EXTAL/P36
F2	P35/NMI	VCC
F3	P31/MTIOC4D/TMCI2/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0/USB0_DPUPE/IRQ1-DS	UPSEL/P35/NMI
F4	PC5/MTIOC3B/MTCLKD/TMRI2/PO29/RSPCKA/USB0_ID	P12/TMCI1/RXD2/SSCL2/SCL0[FM+]/IRQ2
F5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/RXD1/SMISO1/SSCL1/CRX1-DS/USB1_DPUPE/IRQ5	P53
F6	PB1/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/TXD6/SMOSI6/SSDA6/IRQ4-DS	PB7/MTIOC3B/TIOCB5/TXD9/SSDA9/SSDA11/TXD11
F7	PB5/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE1#/SCK9	PB6/MTIOC3D/TIOCA5/RXD9/SSCL9/SSCL11/RXD11
F8	PB3/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE3#/SCK6	PB5/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/POE4#/SCK9/SCK11
G1	EXTAL/P36	TCK/P27/MTIOC2B/TMCI3/SCK1/RSPCKB-A
G2	TDO/P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/MOSIB/USB0_VBUSEN	TMS/P31/MTIOC4D/TMCI2/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS
G3	VCC_USB	TDI/P30/MTIOC4B/TMRI3/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS
G4	VSS_USB	VCC_USB
G5	VCC_USB	VSS_USB
G6	PC6/MTIOC3C/MTCLKA/TMCI2/PO30/MOSIA/USB0_EXICEN/IRQ13	UB/PC7/MTIOC3A/MTCLKB/TMO2/TOC0/CACREF/TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/IRQ14
G7	PC3/MTIOC4D/TCLKB/PO24/TXD5/SMOSI5/SSDA5/SDA2/IETXD	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/SCK10/RSPCKA-A

64-Pin	RX631 (64-Pin TFLGA)	RX651 (64-Pin TFBGA)
G8	PB6/MTIOC3D/TIOCA5/PO30/RXD9/SMISO9/SSCL9	PC0/MTIOC3C/TCLKC/SSLA1-A/IRQ14
H1	XTAL/P37	TDO/P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/MOSIB-A
H2	TRST#/P17/MTIOC3A/MTIOC3B/TIOCB0/TCLKD/TMO1/POE8#/SCK1/MISOA/SDA2-DS/IETXD/USB1_VBUS/IRQ7	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/POE8#/SCK1/TXD3/SSDA3/SDA2-DS/IRQ7/ADTRG1#
H3	USB0_DM	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/RTCOUT/TXD1/SMOSI1/SSDA1/RXD3/SSCL3/SCL2-DS/USB0_VBUS/IRQ6/ADTRG0#
H4	USB0_DP	USB0_DM
H5	USB1_DM	USB0_DP
H6	USB1_DP	PC6/MTIOC3C/MTCLKA/TMCI2/TIC0/RXD8/SMISO8/SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/IRQ13
H7	PC2/MTIOC4B/TCLKA/PO21/RXD5/SMISO5/SSCL5/SSLA3/SCL2/IERXD	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/CTS8#/RTS8#/SS8#/SS10#/CTS10#/RTS10#/SSLA0-A
H8	PB7/MTIOC3B/TIOCB5/PO31/TXD9/SMOSI9/SSDA9	PC1/MTIOC3A/TCLKD/SSLA2-A/IRQ12

3.6 64-Pin Package (RX631: LQFP, RX651: LFQFP)

Table 3.6 shows a comparative listing of the pin functions on the 64-pin package (RX631: LQFP, RX651: LFQFP). Note that the RX63N Group and RX65N Group are not available in 64-pin package versions.

Table 3.6 Comparative Listing of Pin Functions on 64-Pin Package (RX631: LQFP, RX651: LFQFP)

64-Pin	RX631 (64-Pin LQFP)	RX651 (64-Pin LFQFP)
1	EMLE	AVCC1
2	VCL	EMLE
3	MD/FINED	AVSS1
4	XCIN	VCL
5	XCOUT	VBATT
6	RES#	MD/FINED
7	XTAL/P37	XCIN
8	VSS	XCOUT
9	EXTAL/P36	RES#
10	VCC	XTAL/P37
11	P35/NMI	VSS
12	VBATT	EXTAL/P36
13	P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0/USB0_DPUPE/IRQ1-DS	VCC
14	TDI/P30/MTIOC4B/TMRI3/PO8/POE8#/RTCIC0/RXD1/SMISO1/SSCL1/MISOB/USB0_DRPD/IRQ0-DS	UPSEL/P35/NMI
15	TCK/FINEC/P27/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB	TRST#/P34/MTIOC0A/TMCI3/POE10#/IRQ4
16	TDO/P26/MTIOC2A/TMO1/PO6/TXD1/SMOSI1/SSDA1/MOSIB/USB0_VBUSEN	TDI/P30/MTIOC4B/TMRI3/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS
17	TRST#/P17/MTIOC3A/MTIOC3B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/MISOA/SDA2-DS/IETXD/IRQ7	TMS/P31/MTIOC4D/TMCI2/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS
18	TMS/P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/SMOSI1/SSDA1/MOSIA/SCL2-DS/IERXD/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0#	TDO/P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/MOSIB-A
19	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SMISO1/SSCL1/CRX1-DS/IRQ5	TCK/P27/MTIOC2B/TMCI3/SCK1/RSPCKB-A
20	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_DPUPE/USB0_OVRCURA/IRQ4	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/POE8#/SCK1/TXD3/SSDA3/SDA2-DS/IRQ7/ADTRG1#
21	VCC_USB	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/RTCOUT/TXD1/SMOSI1/SSDA1/RXD3/SSCL3/SCL2-DS/USB0_VBUS/IRQ6/ADTRG0#
22	USB0_DM	P13/MTIOC0B/TIOCA5/TMO3/TXD2/SSDA2/SDA0[FM+]/IRQ3/ADTRG1#
23	USB0_DP	P12/TMCI1/RXD2/SSCL2/SCL0[FM+]/IRQ2
24	VSS_USB	VCC_USB
25	P55/MTIOC4D/TMO3/CRX1/IRQ10	USB0_DM
26	P54/MTIOC4B/TMCI1/CTX1	USB0_DP

64-Pin	RX631 (64-Pin LQFP)	RX651 (64-Pin LFQFP)
27	PC7/MTIOC3A/MTCLKB/TMO2/PO31/TXD8/SMOSI8/SSDA8/MISOA/IRQ14	VSS_USB
28	PC6/MTIOC3C/MTCLKA/TMCI2/PO30/RXD8/SMISO8/SSCL8/MOSIA/USB0_EXICEN/IRQ13	P53
29	PC5/MTIOC3B/MTCLKD/TMRI2/PO29/SCK8/RSPCKA/USB0_ID	UB/PC7/MTIOC3A/MTCLKB/TMO2/TOC0/CACREF/TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/IRQ14
30	PC4/MTIOC3D/MTCLKC/TMCI1/PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0/USB0_DPRPD	PC6/MTIOC3C/MTCLKA/TMCI2/TIC0/RXD8/SMISO8/SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/IRQ13
31	PC3/MTIOC4D/TCLKB/PO24/TXD5/SMOSI5/SSDA5/IETXD	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/SCK10/RSPCKA-A
32	PC2/MTIOC4B/TCLKA/PO21/RXD5/SMISO5/SSCL5/SSLA3/IERXD	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/CTS8#/RTS8#/SS8#/SS10#/CTS10#/RTS10#/SSLA0-A
33	PB7/PC1/MTIOC3B/TIOCB5/PO31/TXD9/SMOSI9/SSDA9	PC1/MTIOC3A/TCLKD/SSLA2-A/IRQ12
34	PB6/PC0/MTIOC3D/TIOCA5/PO30/RXD9/SMISO9/SSCL9	PC0/MTIOC3C/TCLKC/SSLA1-A/IRQ14
35	PB5/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE1#/SCK9	PB7/MTIOC3B/TIOCB5/TXD9/SSDA9/SSDA11/TXD11
36	PB3/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE3#/SCK6	PB6/MTIOC3D/TIOCA5/RXD9/SSCL9/SSCL11/RXD11
37	PB1/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/TXD6/SMOSI6/SSDA6/IRQ4-DS	PB5/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/POE4#/SCK9/SCK11
38	VCC	VCC
39	PB0/MTIC5W/TIOCA3/PO24/RXD6/SMISO6/SSCL6/RSPCKA/IRQ12	VSS
40	VSS	PA7/TIOCB2
41	PA6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE2#/CTS5#/RTS5#/SS5#/MOSIA	PA6/MTIC5V/MTCLKB/TIOCA2/TMCI3/POE10#/CTS5#/RTS5#/SS5#
42	PA4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/TXD5/SMOSI5/SSDA5/SSLA0/IRQ5-DS	PA4/MTIC5U/MTCLKA/TIOCA1/TMRI0/TXD5/SMOSI5/SSDA5/IRQ5-DS
43	PA3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/RXD5/SMISO5/SSCL5/IRQ6-DS	PA2/MTIOC7A/RXD5/SMISO5/SSCL5
44	PA1/MTIOC0B/MTCLKC/TIOCB0/PO17/SCK5/SSLA2/IRQ11	PA1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/SCK5/IRQ11
45	PA0/MTIOC4A/TIOCA0/PO16/SSLA1	PE7/MTIOC6A/TOC1/SDHI_WP/IRQ7
46	PE5/MTIOC4C/MTIOC2B/RSPCKB/IRQ5/AN013	PE6/MTIOC6C/TIC1/SDHI_CD/IRQ6
47	PE4/MTIOC4D/MTIOC1A/PO28/SSLB0/AN012	PE2/MTIOC4A/TIC3/RXD12/SSCL12/RXDX12/IRQ7-DS
48	PE3/MTIOC4B/PO26/POE8#/CTS12#/RTS12#/SS12#/MISOB/AN011	PE1/MTIOC4C/MTIOC3B/TXD12/SSDA12/TXDX12/SIOX12/ANEX1
49	PE2/MTIOC4A/PO23/RXD12/SMISO12/SSCL12/RXDX12/SSLB3/MOSIB/IRQ7-DS/AN010	PE0/MTIOC3D/SCK12/ANEX0
50	PE1/MTIOC4C/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2/RSPCKB/AN009	PD7/MTIC5U/POE0#/QMI-B/QIO1-B/SDHI_D1-B/IRQ7/AN107
51	PE0/SCK12/SSLB1/AN008	PD6/MTIC5V/MTIOC8A/POE4#/QMO-B/QIO0-B/SDHI_D0-B/IRQ6/AN106

64-Pin	RX631 (64-Pin LQFP)	RX651 (64-Pin LFQFP)
52	VREFL	PD5/MTIC5W/MTIOC8C/POE10#/QSPCLK-B/SDHI_CLK-B/IRQ5/AN113
53	P46/IRQ14-DS/AN006	PD4/MTIOC8B/POE11#/QSSL-B/SDHI_CMD-B/IRQ4/AN112
54	VREFH	PD3/MTIOC8D/TOC2/POE8#/QIO3-B/SDHI_D3-B/IRQ3/AN111
55	P44/IRQ12-DS/AN004	PD2/MTIOC4D/TIC2/QIO2-B/SDHI_D2-B/IRQ2/AN110
56	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
57	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
58	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
59	VREFL0	VREFL0
60	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
61	VREFH0	VREFH0
62	AVCC0	AVCC0
63	P05/IRQ13/DA1	AVSS0
64	AVSS0	P05/IRQ13/DA1

4. Notes on Migration

4.1 Notes on Pin Design

4.1.1 VCL Pin (External Capacitor)

Connect a decoupling capacitor rated at 0.22 µF to the VCL pin of the RX65N Group for stabilization of the internal power supply.

4.1.2 Inputting an External Clock

On the RX63N Group it was permissible, when inputting an external clock, to input on the XTAL pin the reverse phase of the clock input on the EXTAL pin. However, this is not permitted on the RX65N Group. Keep this in mind when designing systems.

4.1.3 On-Chip USB DP/DM Pull-Up/Pull-Down Resistors

The RX65N Group has on-chip DP/DM pull-up and pull-down resistors. This means that the external connection circuits are different from those for the RX63N Group.

For details on external connection circuits, see RX65N Group, RX651 Group User's Manual: Hardware, listed in section 5, Reference Documents.

4.2 Notes on Function Settings

4.2.1 Changing Option-Setting Memory by Self-Programming

Making changes to the option-setting memory by self-programming on the RX65N Group is accomplished by programming the configuration setting area in the option-setting memory using the configuration setting command.

For details on the configuration setting command, see RX65N Group, RX651 Group Flash Memory User's Manual: Hardware Interface, listed in section 5, Reference Documents.

4.2.2 Setting Number of Flash Memory Access Wait States

On the RX65N Group it is necessary to specify the number of access wait states to be used when accessing the flash memory, based on the system clock (ICLK) frequency of the microcontroller. This setting is made to the ROMWT register.

Table 4.1 lists the number of flash memory access wait states, according to ICLK frequency.

Table 4.1 Flash Memory Access Wait States by ICLK Frequency

	ICLK ≤ 50 MHz	50 MHz < ICLK ≤ 100 MHz	100 MHz < ICLK ≤ 200 MHz
Wait states	0 to 2	1 or 2	2

For details on external connection circuits, see RX65N Group, RX651 Group User's Manual: Hardware, listed in section 5, Reference Documents.

4.2.3 Software Configurable Interrupts

A software configurable interrupt function has been added to the RX65N Group. An interrupt source assigned to each interrupt vector number from 128 to 255 can be selected from multiple sources.

For details on external connection circuits, see RX65N Group, RX651 Group User's Manual: Hardware, listed in section 5, Reference Documents.

4.2.4 User Boot Mode

UB code A, UB code B, and user boot mode are implemented on the RX63N Group but not on the RX65N Group.

When using the startup program protection function on the RX65N Group, it is possible to use any interface to program and erase the user area in flash memory as an alternative to user boot mode. For details, see 7.3, Startup Program Protection Function, in RX65N Group, RX651 Group Flash Memory User's Manual: Hardware Interface, cited in 5, Reference Documents.

4.2.5 Transferring Firmware to FCU RAM

In order to use FCU commands with the RX63N Group, it is necessary first to store the FCU firmware in the FCU RAM. This step is not necessary for the RX65N Group.

4.2.6 Command Usage with Flash Memory

On the RX63N Group it is possible to program and erase the flash memory by issuing FCU commands to the FCU. On the RX65N Group the FCU can be controlled in order to program and erase the flash memory by setting FACI commands in the FACI command issuance area.

Table 4.2 shows a comparison of the specifications of the FCU and FACI commands.

Table 4.2 Specification Comparison of FCU and FACI Commands

Item	FCU Command (RX63N)	FACI Command (RX65N)
Command issuance area	Programming/erasure address (00E0 0000h to 00FF FFFFh)	FACI command issuance area (007E 0000h)
Usable commands	• P/E normal mode transition • Status read mode transition • Lock bit read mode transition • Peripheral clock notification • Programming • Block erase • P/E suspend • P/E resume • Status register clear • Lock bit read 2 • Lock bit programming • Blank checking	• Programming • Block erase • Multi-block erase • P/E suspend • P/E resume • Status clear • Forced end • Blank checking • Configuration settings

4.2.7 Flash Access Window Setting Register (FAW)

On the RX65N Group, once the access window protect bit (FSPR) in the flash access window setting register (FAW) is written to 0, it cannot be reset to 1.

For details, see RX65N Group, RX651 Group User's Manual: Hardware, cited in 5, Reference Documents.

5. Reference Documents

User's Manual: Hardware

RX63N Group, RX631 Group User's Manual: Hardware Rev.1.80 (R01UH0041EJ0180)
(The latest version can be downloaded from the Renesas Electronics website.)

RX65N Group, RX651 Group User's Manual: Hardware Rev.2.30 (R01UH0590EJ0230)
(The latest version can be downloaded from the Renesas Electronics website.)

RX65N Group, RX651 Group Flash Memory User's Manual: Hardware Interface Rev.2.10 (R01UH0602EJ0210)
(The latest version can be downloaded from the Renesas Electronics website.)

Application Note

Design Guide for Migration between RX Family: Differences in Package External form (R01AN4591EJ)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

Consistency with Technical Updates

This application note reflects the contents of the following technical updates:

- TN-RX*-A104A/E
- TN-RX*-A108A/E
- TN-RX*-A116A/E
- TN-RX*-A120A/E
- TN-RX*-A138A/E

Revision History

Rev.	Date	Description	
		Page	Summary
0.40	Sep. 17, 2015	—	First edition issued
0.50	Feb. 25, 2016		Revisions accompanying update of User's Manual: Hardware from revision 0.4 to 0.5
		4	(1) Boot mode (FINE interface) added
		11	(2) Bit names changed (MSTPA0 and MSTPA1)
		21	(3) IR2C bit in DTC mode register A deleted
		61	(4) Specifications for 16-bit data size deleted
		66	(5) Ring buffer deleted from compare function
		68	(6) Number of channels in A/D sampling state register changed
		69	(7) A/D data storage buffer register (ADBUF), A/D data storage buffer enable register (ADBUFEN), and A/D data storage buffer pointer register (ADBUFPTR) deleted
		71	(8) Temperature sensor calibration data registers added
			(9) Table 2.50, Comparison of Data Sensor Specifications, deleted to accompany addition of temperature sensor calibration data registers
		74	(10) Content of cache and read cycle items changed to accompany deletion of AFU
		75	(11) Boot mode (FINE interface) added to onboard programming item
		77	(12) Register name changed (FSUACR)
			(13) Unique ID register n added
		55	Revisions to correct errors
		61	(14) CAN module added
			(15) 32-bit polynomial expression amended
		68	(16) Register added (CRCDIR)
			(17) Register name amended (ADGCEXCR)
		74	(18) Register added (ADGCTRGR)
			(19) Term (data flash memory) deleted from programming/erasure item
0.51	Apr. 30, 2016	1	(1) Titles in groups and contents amended
		5	(2) IWDT reset interrupt request select bit (OFS0.IWDTRSTIRQS) added to option function select register 0
			(3) WDT reset interrupt request select bit (OFS0.WDTRSTIRQS) added to option function select register 0
		7	(4) Voltage detection 1 level select bits (LVDLVLR.LVD1LVL[3:0]) and voltage detection 2 level select bits (LVDLVLR.LVD2LVL[3:0]) added to voltage detection level select register
			(5) Sampling clock select bits (LVD1CR0.LVD1FSAMP[1:0]) added to voltage monitoring 1 circuit control register 0
			(6) Sampling clock select bits (LVD2CR0.LVD2FSAMP[1:0]) added to voltage monitoring 2 circuit control register 0

Rev.	Date	Description	
		Page	Summary
0.51	Apr. 30, 2016	10	(7) USB clock (UCLK) select bits (SCKCR2.UCK[3:0]) added to system clock control register 2
		10	(8) PLL input frequency division ratio select bits (PLIDIV[1:0]) added to PLL control register
		20	(9) Bus section added
		25	(10) DMA block transfer count register (DMCRB) added
		26	(11) EXDMA controller section added
		30	(12) DTC vector base register (DTCVBR) added
		33	(13) TPU notation in event link function item amended
			(14) TPU register comparison deleted
		35	(15) Interrupt item added
		39	(16) Independent watchdog timer section added
		42	(18) FIFO depth register (FDR) added
		43	(19) Receive FIFO overflow BSY output threshold bits (FCFTR.RFDO[2:0]) added to flow control start FIFO threshold setting register
		46	(20) Transaction-enabled time select bit (SOFCFG.TRNENSEL) added to SOF output configuration register
			(21) Device address n configuration register (DEVADDn) added
		53	(22) Errors in extended serial mode I/O control function item corrected
		54	(23) Receive registers (RDRH and RDRL) and transmit registers (TDRH and TDRL) added
			(24) Character length bit (CMR.CHR) and communications mode bit (CMR.CM) added to serial mode register
		55	(25) Bus collision detection clock select bits (CR2.BCCS[1:0]) added to control register 2
		65	(26) Notation of CRC data input register (CRCDIR) and CRC data output register (CRCDOR) changed
		72	(27) Notation of double trigger target channel select bits (ADCSR.DBLANS[4:0]), group B scan end interrupt enable bit (ADCSR.GBADIE), and double trigger mode select bit (ADCSR.DBLE) in A/D control register added
		73	(28) Details of scan mode select bit (ADCSR.ADCS) in in A/D control register added
			(29) Addition count select bits (ADADC.ACD) added to A/D-converted value addition count select register
		80	(30) Suspend/resume function added
		82	(31) Details of flash programming/erasure bits (FWEPROR.FLWE[1:0]) in flash write erase protection register added
			(32) Command lock flag (FASTAT.CMDLK) deleted from flash access status register
			(33) FCU command lock interrupt enable bit (FAEINT.CMDLKIE) deleted from flash access error interrupt enable register
		84	(34) Comparison of pin functions added
		54	(35) SCI receive data-full flag (SSR.RDRF) and transmit data-empty flag (SSR.TDRE) deleted (TU support (TN-RX*-A138A/J))

Rev.	Date	Description	
		Page	Summary
0.51	Apr. 30, 2016	64	(36) RSPI receive buffer-full flag (SPSR.SPRF) and transmit buffer-empty flag (SPSR.SPTEF) deleted (TU support (TN-RX*-A138A/J))
		77	(37) Temperature sensor register comparison amended (TU support (TN-RX*-A116A/J))
		83	(38) Unique ID register deleted (TU support (TN-RX*-A116A/J))
0.80	Jul. 8, 2016	1	(1) Summary amended
		3, 17, 19	(2) Interrupt control abbreviation changed
		6	(3) ROM code protection register (ROMCODE) added
		18	(4) RAM error interrupt added
		19	(5) RAM error interrupt status flag (RAMST) added
			(6) RAM error interrupt enable bit (RAMEN) added
			(7) Range of k for electable interrupt A request register k (PIARk) changed
		21	(8) SDSI added to peripheral modules connected to internal main bus 2 of RX65N
		23	(9) SDSI added to details of bus master code bits
		31	(10) Read skip, write-back skip, and sequence transfer sections changed
			(11) Displacement addition item added
			(12) Name of write-back disable bit changed
		33	(13) Drive capacity control register 2 (DSCR2) added
			(14) ADRHMS bit deleted from external bus control register 0 (PFBCR0)
		42	(15) Address error flag (ADE) and address error interrupt enable bit (ADEIP) added
			(16) Receive request reset bit (RNC) deleted from RX65N
		53	(17) Item names related to FIFO changed
		64	(18) Mode fault error flag (MODF) added to RSPI status register (SPSR)
			(19) RSPI data register (SPDR) added
			(20) RSPI byte access setting bit (SPBYT) added
		68	(21) PCLKB:ADCLK frequency ratio changed
		68, 69, 71	(22) Japanese notation in sections changed
		72	(23) Register names changed (ADDBLDR, ADDBLDRA, and ADDBLDRB)
		75	(24) A/D successive approximation time setting register (ADSAM) and A/D successive approximation time setting protection cancel register (ADSAMPR) added
		76	(25) Description of D/A output method switching changed
			(26) D/A output disable register (DAODISR) added
		81	(27) Unique ID item added
		82	(28) RX65N register bit (FLWE) name changed
		85 to 98	(29) Comparison tables amended
		99	(30) Table number added (table 4.1)
		100	(31) Sections 4.2.4 to 4.2.7 added

Rev.	Date	Description	
		Page	**Summary**
1.00	Oct. 1, 2016	5	(1) MDSR register name amended
		7	(2) RX65N bit name amended (LVDnLVL)
		33	(3) Details of settable operations amended
			(4) Event link function (input) section amended
			(5) Low power consumption function section amended
		37	(6) Note added to table 2.30
		46	(7) Data match detection item added to asynchronous mode
		58	(8) Errors in description of SSL control function amended
		60	(9) RX65N mode fault error flag (MODF) amended
		64	(10) RX65N conversion time amended
		68	(11) Notation added for A/D conversion clock select bit
		71	(12) D/A output mode switching item deleted
			(13) D/A output amplifier control register (DAAMPCR) and D/A output disable register (DAODISR) deleted
		74	(14) RX65N portion of program/erasure method section amended
			(15) Trusted memory function section amended
			(16) BGO function section amended
		75	(17) Other functions amended
			(18) Onboard programming section amended
			(19) Item names amended (off programming → dedicated parallel programmer ...)
			(20) RX65N portion of programming/erasing with dedicated parallel programmer section amended
			(21) RX63N portion of unique ID section added
		76	(22) Register name of E2 data flash P/E enable register 1 amended (DFLWE0 → DFLWE1)
		80	(23) RX65N portion on page 83 amended
		91	(24) 4.2.4, User Boot Mode, added
2.00	Nov. 6, 2017	All pages	Supports RX65N with at least 1.5 MB of code flash memory
2.10	May 21, 2019	1	Summary revised
		3	1, Comparison of Functions of RX65N Group and RX63N Group, revised
			1, Table 1.1, Comparison of Functions of RX65N and RX63N, revised
		5	2.1, CPU, added
			2.1, Table 2.1, Comparative Overview of CPU Features, added
			2.2, Table 2.2, Comparison of CPU Registers, added
		7	2.3, Address Space, added
			2.3, Table 2.5, Comparative Memory Map of Single-Chip Mode, added
		8	2.3, Table 2.6, Comparative Memory Map of On-Chip ROM Enabled Extended Mode, added
		9	2.3, Table 2.7, Comparative Memory Map of On-Chip ROM Disabled Extended Mode, added
		10	2.4, Table 2.8, Comparative Overview of Option-Setting Memory Registers, revised
		12	2.5, Table 2.10, Comparative Listing of Voltage Detection Circuit Registers, revised

Rev.	Date	Description	
		Page	Summary
2.10	May 21, 2019	13	2.6, Table 2.11, Comparative Overview of Clock Generation Circuit Specifications, revised
		15	2.6, Table 2.12, Comparative Listing of Clock Generation Circuit Registers, revised
		21	2.9, Table 2.16, Comparative Overview of Interrupt Controller Specifications, revised
		23	2.9, Table 2.17, Comparative Listing Interrupt Controller Registers, revised
		25	2.10, Table 2.18, Comparative Overview of Bus Specifications, revised
		28	2.10, Table 2.20, Comparative Listing of Bus Registers, revised
		38	2.15, Table 2.28, Comparative Overview of I/O Ports on 177- and 176-Pin Packages, added
			2.15, Table 2.29, Comparative Overview of I/O Ports on 145- and 144-Pin Packages, added
		39	2.15, Table 2.30, Comparative Overview of I/O Ports on 100-Pin Packages, added
			2.15, Table 2.31, Comparative Overview of I/O Ports on 64-Pin Packages, added
		40	2.15, Table 2.32, Comparative Listing of I/O Port Registers, revised
		41	2.16, Table 2.33, Comparative Listing of Multi-Function Pin Controller Registers, revised
		43	2.18, Programmable Pulse Generator, added
			2.18, Table 2.35, Comparative Listing of the Programmable Pulse Generator Registers, added
		49	2.22, Watchdog Timer, added
			2.22, Table 2.41, Comparative Overview of Watchdog Timer, added
			2.22, Table 2.42, Comparative Listing of Watchdog Timer Registers, added
		50	2.23, Table 2.43, Comparative Overview of Independent Watchdog Timer, changed
		51	2.23, Table 2.44, Comparative Listing of Independent Watchdog Timer Registers, added
		52	2.24, Table 2.45, Comparative Listing of DMA Controller for The Ethernet Controller Registers, revised
		57	2.26, Table 2.48, Comparative Overview of SCIc and SCIg Specifications, revised
		59	2.26, Table 2.49, Comparative Overview of SCIi Specifications, revised
		61	2.26, Table 2.50, Comparative Overview of SCId and SCIh Specifications, revised
		64	2.26, Table 2.51, Comparative Overview of SCI Channel Specifications, revised
		74	2.29, Table 2.57, Comparative Listing of Serial Peripheral Interface Registers, revised
		77	2.31, Table 2.60, Comparative Overview of Parallel Data Capture Unit, revised
		78	2.32, Table 2.61, Comparative Overview of 12-Bit A/D Converter, revised

Rev.	Date	Description	
		Page	Summary
2.10	May 21, 2019	86	2.33, Table 2.63, Comparative Overview of D/A Converter, revised
			2.33, Table 2.64, Comparative Listing of D/A Converter Registers, revised
		87	2.34, Table 2.65, Comparative Listing of Temperature Sensor Registers, revised
		90	2.36, Table 2.68, Comparative Overview of Flash Memory (Code Flash) Specifications, revised
		92	2.36, Table 2.69, Comparative Listing of Flash Memory Registers, revised
		94	2.37, Package, added
			2.37, Table 2.70, Package, added
		95	3.1, 177-/176-Pin Package, added
			3.1, Table 3.1, Comparative Listing of Pin Functions on 177-/176-Pin Package, added
		102	3.2, 176-Pin Package, added
			3.2, Table 3.2, Comparative Listing of Pin Functions on 176-Pin Package, added
		121	3.5, 64-Pin Package (RX631: TFLGA, RX651: TFBGA), added
			3.5, Table 3.5, Comparative Listing of Pin Functions on 64-Pin Package (RX631: TFLGA, RX651: TFBGA), added
		124	3.6, 64-Pin Package (RX631: LQFP, RX651: LFQFP), added
			3.6, Table 3.6, Comparative Listing of Pin Functions on 64-Pin Package (RX631: LQFP, RX651: LFQFP), added
		128	4.2.4, User Boot Mode, revised
			4.2.6, Table 4.2, Specification Comparison of FCU and FACI Commands, revised
			4.2.8, Erasing the Code Flash Area with the ID Code Protection Function, deleted
		129	5, Reference Documents, revised
		130	Consistency with Technical Updates revised

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/.