RX26T Group, RX66T Group

Differences Between the RX26T Group and the RX66T Group

Introduction

This application note is intended as a reference to points of difference between the peripheral functions, I/O registers, and pin functions of the RX26T Group and RX66T Group, as well as a guide to key points to consider when migrating between the two groups.

Unless specifically otherwise noted, the information in this application note applies to the 100-pin package version of the RX26T Group and the 144-pin package version (with programmable gain amplifier (PGA) pseudo-differential input and USB pins) of the RX66T Group as the maximum specifications. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the User's Manual: Hardware of the products in question.

Target Device

RX26T Group and RX66T Group

Contents

1. Comparison of Built-In Functions of RX26T Group and RX66T Group

A comparison of the built-in functions of the RX26T Group and RX66T Group is provided below. For details of the functions, refer to 2. Comparative Overview of Specifications and 5. Reference Documents.

Table 1.1 is Comparison of Built-In Functions of RX66T Group and RX26T Group.

Table 1.1 Comparison of Built-In Functions of RX66T Group and RX26T Group

Function	RX66T	RX26T
CPU	●/■	
Operating modes	■	
Address space	▲	
Resets	●/■	
Option-setting memory (OSFM)	●/▲/■	
Voltage detection circuit (LVDA)	○	
Clock generation circuit	●/▲/■	
Clock frequency accuracy measurement circuit (CAC)	○	
Low power consumption	●/▲/■	
Register write protection function	■	
Exception handling	○	
Interrupt controller (ICUC: RX66T, ICUG: RX26T)	●/■	
Buses	●/■	
Memory-protection unit (MPU)	○	
DMA controller (DMACAa)	○	
Data transfer controller (DTCa: RX66T, DTCb: RX26T)	●	
Event link controller (ELC)	●/■	
I/O ports	●/■	
Multi-function pin controller (MPC)	●/■	
Multi-function timer pulse unit 3 (MTU3d)	○	
Port output enable 3 (POE3B: RX66T, POE3D: RX26T)	●/▲/■	
General-purpose PWM timer (GPTW: RX66T, GPTWa: RX26T)	●/▲/■	
High resolution PWM waveform generation circuit (HRPWM)	▲	
Port output enable for GPTW (POEG)	●/▲	
8-bit timer (TMRb)	○	
Compare match timer (CMT)	○	
Compare match timer W (CMTW)	×	○
Watchdog timer (WDTA)	○	
Independent watchdog timer (IWDTa)	■	
USB2.0FS host or function module (USBb)	○	×
Serial communications interface (SCIj, SCIi, SCIh: RX66T, SCIk, SCIh: RX26T)	●/▲/■	
Serial communications interface (RSCI)	×	○
I^2C bus interface (RIICa)	○	
I^3C bus interface (RI3C)	×	○
CAN module (CAN): RX66T, CAN FD module (CANFD): RX26T	●/▲/■	
Serial peripheral interface (RSPIc: RX66T, RSPId: RX26T)	●/▲	
Serial peripheral interface (RSPIA)	×	○
CRC calculator (CRCA)	○	
Trigonometric function calculator (TFUv2)	×	○
Trusted Secure IP (TSIP-Lite)	○	
12-bit A/D converter (S12ADH: RX66T, S12ADHa: RX26T)	●/▲/■	
12-bit D/A converter (R12DAb)	○	
Temperature sensor (TEMPS)	○	

Function	RX66T	RX26T
Comparator C (CMPC: RX66T, CMPCa: RX26T)	●	
Data operation circuit (DOC: RX66T, DOCA: RX26T)	●/▲	
RAM	■	
Flash memory	●/▲/■	
Packages	●/■	

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Differences in register specifications are not listed.

2.1 CPU

Table 2.1 is Comparative Overview of CPU.

Table 2.1 Comparative Overview of CPU

Item	RX66T	RX26T
CPU	• Maximum operating frequency: 160 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • 111 instructions — Standard provided instructions: 111 Basic instructions: 77 Single-precision floating point instructions: 11 DSP instructions: 23 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits	• Maximum operating frequency: 120 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • 113 instructions — Standard provided instructions: 111 Basic instructions: 77 Single-precision floating point instructions: 11 DSP instructions: 23 — Instructions for register bank save function: 2 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits
FPU	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard
Register bank save function	—	• Fast collective saving and restoration of the values of CPU registers • 16 save register banks

2.2 Operating Modes

Table 2.2 is Comparative Overview of Operating Modes, and Table 2.3 is Comparison of Operating Mode Registers.

Table 2.2 Comparative Overview of Operating Modes

Item	RX66T	RX26T
Operating modes specified by mode setting pins	Single-chip mode	Single-chip mode
	Boot mode (SCI interface)	Boot mode (SCI interface)
	Boot mode (USB interface)	—
	User boot mode	—
	Boot mode (FINE interface)	Boot mode (FINE interface)
Operating modes selected by register settings	Single-chip mode	Single-chip mode
	User boot mode	—
	On-chip ROM disabled extended mode	—
	On-chip ROM enabled extended mode	—
Selection of endian	MDE register	MDE register

Table 2.3 Comparison of Operating Mode Registers

Register	Bit	RX66T	RX26T
MDSR	—	Mode status register	—
SYSCR0	EXBE	External bus enable bit	—
SYSCR1	ECCRAME	ECCRAM enable bit	—
VOLSR	USBVON	USB power supply control bit	—
	PGAVLS	PGA operating condition setting bit	—

2.3 Address Space

Figure 2.1 is Comparison of Memory Maps in Single-Chip Mode.

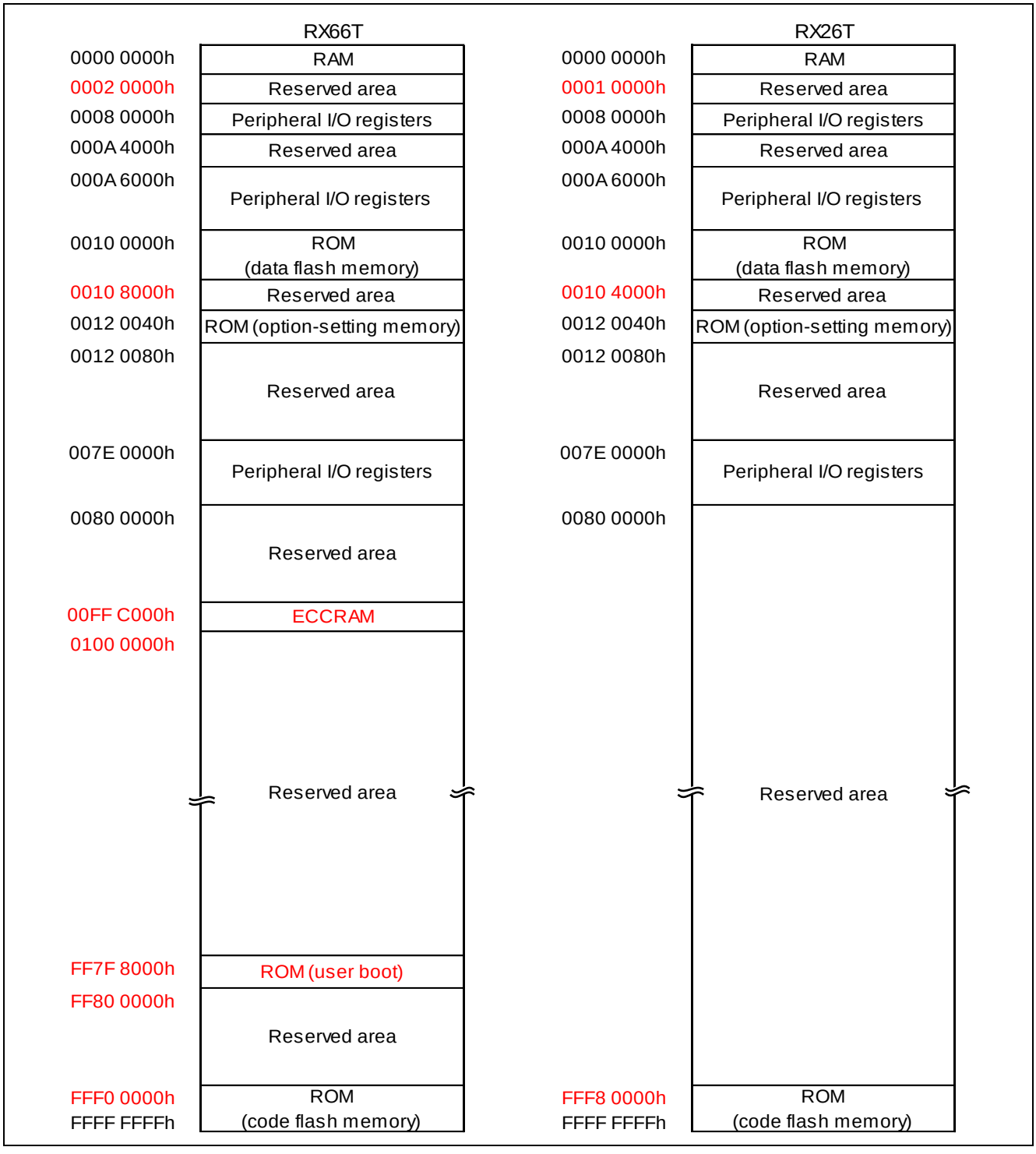

Figure 2.1 Comparison of Memory Maps in Single-Chip Mode

2.4 Resets

Table 2.4 is Comparative Overview of Resets, and Table 2.5 is Comparison of Reset-Related Registers.

Table 2.4 Comparative Overview of Resets

Item	RX66T	RX26T
RES# pin reset	Voltage input to the RES# pin is driven low.	Voltage input to the RES# pin is driven low.
Power-on reset	VCC rises (voltage detection: VPOR).	VCC rises (voltage detection: VPOR).
Voltage monitoring 0 reset	VCC falls (voltage detection: Vdet0).	VCC falls (voltage detection: Vdet0).
Voltage Monitoring 1 reset	VCC falls (voltage detection: Vdet1).	VCC falls (voltage detection: Vdet1).
Voltage monitoring 2 reset	VCC falls (voltage detection: Vdet2).	VCC falls (voltage detection: Vdet2).
Deep software standby reset	Deep software standby mode is canceled by an interrupt.	—
Independent watchdog timer reset	The independent watchdog timer underflows, or a refresh error occurs.	The independent watchdog timer underflows, or a refresh error occurs.
Watchdog timer reset	The watchdog timer underflows, or a refresh error occurs.	The watchdog timer underflows, or a refresh error occurs.
Software reset	Register setting	Register setting

Table 2.5 Comparison of Reset-Related Registers

Register	Bit	RX66T	RX26T
RSTSR0	DPSRSTF	Deep software standby reset flag	—

2.5 Option-Setting Memory

Figure 2.2 is Comparison of Option-Setting Memory Areas, and Table 2.6 is Comparison of Option-Setting Memory Registers.

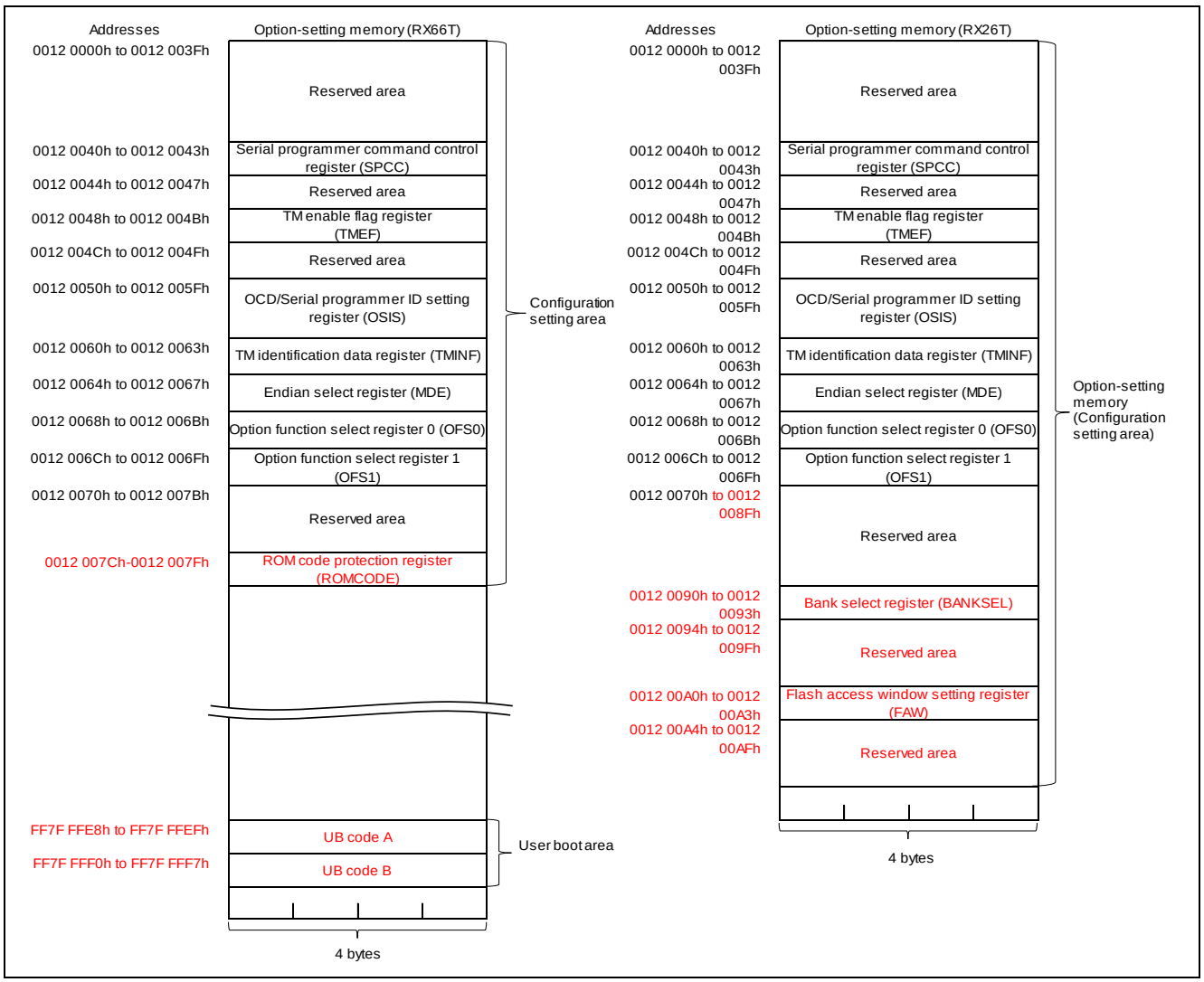

Figure 2.2 Comparison of Option-Setting Memory Areas

Table 2.6 Comparison of Option-Setting Memory Registers

Register	Bit	RX66T (OFSM)	RX26T (OFSM)
SPCC	OCDE	—	On-chip debugger connection enable bit
	IDE	ID code protection enable bit 0: The ID code protection function is enabled after a reset.*1 1: The ID code protection function is disabled after a reset.	Serial programmer ID code protection enable bit 0: The serial programmer ID code protection is enabled after a reset.*1 1: The serial programmer ID code protection is disabled after a reset.*2
MDE	BANKMD [2:0]	—	Bank mode select bits
TMEF	TMEF[2:0]	TM enable bits b26 b24 0 0 0: The TM function is enabled. 1 1 1: The TM function is disabled. Settings other than the above are prohibited.	TM enable bits b26 b24 0 0 0: The TM function is enabled for blocks 8 and 9 in the code flash memory. 1 1 1: The TM function is disabled for blocks 8 and 9 in the code flash memory. Settings other than the above are prohibited.
	TMEFDB [2:0]	—	Dual bank TM enable bits
BANKSEL	—	—	Bank select register
FAW	—	—	Flash access window setting register
ROMCODE	—	ROM code protection register	—

Notes: 1. To enable the serial programmer ID code protection, set the RDPR, SEPR, and WRPR bits to 0.
2. To disable the serial programmer ID code protection, set the RDPR, SEPR, and WRPR bits to 1.

2.6 Clock Generation Circuit

Table 2.7 is Comparative Overview of Clock Generation Circuits, and Table 2.8 is Comparison of Clock Generation Circuit Registers.

Table 2.7 Comparative Overview of Clock Generation Circuits

Item	RX66T	RX26T
Use	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the RSPI, SCIi, MTU3 (internal peripheral bus), GPTW (internal peripheral bus), and HRPWM (internal peripheral bus). • Generates the peripheral module clock (PCLKB) to be supplied to the peripheral modules. • Generates the counter reference clock for peripheral modules and the HRPWM reference clock (PCLKC) to be supplied to the MTU3 and GPTW. • Generates the peripheral module clock (for analog conversion) (PCLKD) to be supplied to the S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the USB clock (UCLK) to be supplied to the USBb. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.	• Generates the system clock (ICLK) to be supplied to the CPU, TFU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the RSPI, RSPIA, RSCI, RI3C, CANFD, MTU (internal peripheral bus), GPTW (internal peripheral bus), and HRPWM (internal peripheral bus). • Generates the peripheral module clock (PCLKB) to be supplied to the peripheral modules. • Generates the counter reference clock for peripheral modules and the HRPWM reference clock (PCLKC) to be supplied to the MTU and GPTW. • Generates the peripheral module clock (for analog conversion) (PCLKD) to be supplied to the S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CANFD clock (CANFDCLK) to be supplied to the CANFD. • Generates the CANFD main clock (CANFDMCLK) to be supplied to the CANFD. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.

Item	RX66T	RX26T
Operating frequency	• ICLK: 160 MHz (max.) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKC: 160 MHz (max.) • PCLKD: 8 MHz to 60 MHz (for conversion with 12-bit A/D converter) • FCLK: — 4 MHz to 60 MHz (for programming and erasing the code flash memory or data flash memory) — 60 MHz (max.) (for reading from the data flash memory) • BCLK: 60 MHz (max.) • BCLK pin output: 40 MHz (max.) • UCLK: 48 MHz (max.) • CACCLK: Same as clock from respective oscillators • CANMCLK: 24 MHz (max.) • IWDTCLK: 120 kHz	• ICLK: 120 MHz (max.) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKC: 120 MHz (max.) • PCLKD: 8 MHz to 60 MHz (for conversion with 12-bit A/D converter) • FCLK: — 4 MHz to 60 MHz (for programming and erasing the code flash memory or data flash memory) — 60 MHz (max.) (for reading from the data flash memory) • CACCLK: Same as clock from respective oscillators • CANFDCLK: 60 MHz (max.) • CANFDMCLK: 24 MHz (max.) • IWDTCLK: 120 kHz
Main clock oscillator	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal • Connection pins: EXTAL and XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, this function switches the system clock source to LOCO and drives the MTU3 and GPTW pins to high-impedance.	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal • Connection pins: EXTAL and XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, this function switches the system clock source to LOCO and drives the MTU and GPTW pins to high-impedance.
PLL frequency synthesizer	• Input clock source: Main clock, HOCO • Input pulse frequency division ratio: Selectable from 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable from 10 to 30 • Output clock frequency of the PLL frequency synthesizer: 120 MHz to 240 MHz	• Input clock source: Main clock and HOCO • Input pulse frequency division ratio: Selectable from 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable from 10 to 30 • Output clock frequency of the PLL frequency synthesizer: 120 MHz to 240 MHz
High-speed on-chip oscillator (HOCO)	• Oscillation frequency: Selectable from 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control	• Oscillation frequency: Selectable from 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control

Item	RX66T	RX26T
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 240 kHz	Oscillation frequency: 240 kHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 120 kHz	Oscillation frequency: 120 kHz
BCLK pin output control function	• BCLK clock output or high-level output can be selected. • BCLK or BCLK/2 can be selected for the output clock.	—
Event link function (output)	Detection of stopping of the main clock oscillator	Detection of stopping of the main clock oscillator
Event link function (input)	Switching of the clock source to the low-speed on-chip oscillator	Switching of the clock source to the low-speed on-chip oscillator

Table 2.8 Comparison of Clock Generation Circuit Registers

Register	Bit	RX66T	RX26T
SCKCR	BCK[3:0]	External bus clock (BCLK) select bits	—
	PSTOP1	BCLK pin output control bit	—
MEMWAIT	—	Memory wait cycle setting register	—
SCKCR2	UCK[3:0]	USB clock (UCLK) select bits	—
	CFDCK[3:0]	—	CANFD clock (CANFDCLK) select bits
BCKCR	—	External bus clock control register	—

2.7 Low Power Consumption

Table 2.9 is Comparative Overview of Low Power Consumption Functions, Table 2.10 is Comparison of Transition and Cancellation Methods and Operating States in Each Mode, and Table 2.11 is Comparison of Low Power Consumption Registers.

Table 2.9 Comparative Overview of Low Power Consumption Functions

Item	RX66T	RX26T
Reducing power consumption by switching clock signals	• The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, and PCLKD), external bus clock (BCLK), and flash interface clock (FCLK).	• The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, and PCLKD), and flash interface clock (FCLK).
BCLK output control function	BCLK output or high-level output can be selected.	—
Module stop function	Each peripheral module can be stopped independently.	Each peripheral module can be stopped independently.
Function for transition to low power consumption mode	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.
Low power consumption modes	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode	• Sleep mode • All-module clock stop mode • Software standby mode

Table 2.10 Comparison of Transition and Cancellation Methods and Operating States in Each Mode

Mode	Transition and Cancellation Methods and Operating States	RX66T	RX26T
Sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupts	Interrupts
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM and ECCRAM: RX66T RAM: RX26T	Operation possible (retained)	Operation possible (retained)
	Flash memory	Operation	Operation
	USBFS host or function module (USBb)	Operation possible	—
	Watchdog timer (WDTA: RX66T, WDT: RX26T)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Port output enable (POE)	Operation possible	Operation possible
	8-bit timer (unit 0 and unit 1) (TMR)	Operation possible	Operation possible

Mode	Transition and Cancellation Methods and Operating States	RX66T	RX26T
Sleep mode	Voltage detection circuit (LVDA: RX66T, LVD: RX26T)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Operation possible	Operation possible
	I/O ports	Operation	Operation
All-module clock stop mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupts	Interrupts
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM and ECCRAM: RX66T RAM: RX26T	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	USBFS host or function module (USBb)	Stopped	—
	Watchdog timer (WDTA: RX66T, WDT: RX26T)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Port output enable (POE)	Operation possible	Operation possible
	8-bit timer (unit 0 and unit 1) (TMR)	Operation possible	Operation possible
	Voltage detection circuit (LVDA: RX66T, LVD: RX26T)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained
Software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupts	Interrupts
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Stopped	Stopped
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Stopped
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Stopped	Stopped
	CPU	Stopped (retained)	Stopped (retained)
	RAM and ECCRAM: RX66T RAM: RX26T	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	USBFS host or function module (USBb)	Stopped	—
	Watchdog timer (WDTA: RX66T, WDT: RX26T)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Port output enable (POE)	Stopped (retained)	Stopped (retained)

Mode	Transition and Cancellation Methods and Operating States	RX66T	RX26T
Software standby mode	8-bit timer (unit 0 and unit 1) (TMR)	Stopped (retained)	Stopped (retained)
	Voltage detection circuit (LVDA: RX66T, LVD: RX26T)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained

“Operation possible” means that whether the state is operating or stopped is controlled by the control register setting.
“Stopped (retained)” means that internal register values are retained and internal operations are suspended.

Table 2.11 Comparison of Low Power Consumption Registers

Register	Bit	RX66T	RX26T
SBYCR	OPE	Output port enable bit	—
MSTPCRA	MSTPA0	—	Module stop bit for compare match timer W (unit 1)
	MSTPA1	—	Module stop bit for compare match timer W (unit 0)
	MSTPA9	Module stop bit for multi-function timer pulse unit 3 Target module: MTU3 0: Release from module-stop state 1: Transition to module-stop state	Module stop bit for multi-function timer pulse unit 3 Target module: MTU 0: Release from module-stop state 1: Transition to module-stop state
MSTPCRB	MSTPB0	Module stop bit for CAN module 0	—
	MSTPB19	Universal serial bus 2.0 FS interface module stop bit	—
MSTPCRC	MSTPC6	ECCRAM module stop bit	—
	MSTPC24	Serial communications interface 11 module stop bit Target module: SCI11 0: Release from module-stop state 1: Transition to module-stop state	Serial communications interface 11 module stop bit Target module: RSCI11 0: Release from module-stop state 1: Transition to module-stop state
	MSTPC26	Serial communications interface 9 module stop bit Target module: SCI9 0: Release from module-stop state 1: Transition to module-stop state	Serial communications interface 9 module stop bit Target module: RSCI9 0: Release from module-stop state 1: Transition to module-stop state
	MSTPC27	Serial communications interface 8 module stop bit Target module: SCI8 0: Release from module-stop state 1: Transition to module-stop state	Serial communications interface 8 module stop bit Target module: RSCI8 0: Release from module-stop state 1: Transition to module-stop state

Register	Bit	RX66T	RX26T
MSTPCRD	—	Module stop control register D	Module stop control register D
		Initial value after a reset differs.	
	MSTPD0	Module stop D0 setting bit	—
	MSTPD1	Module stop D1 setting bit	—
	MSTPD2	Module stop D2 setting bit	—
	MSTPD3	Module stop D3 setting bit	—
	MSTPD4	Module stop D4 setting bit	—
	MSTPD5	Module stop D5 setting bit Reading and writing are enabled. To transfer to all-module clock stop mode, this bit must be set to 1.	Module stop bit for I3C bus interface 0 Target module: RI3C0 0: Release from module-stop state 1: Transition to module-stop state
	MSTPD6	Module stop D6 setting bit	—
	MSTPD7	Module stop D7 setting bit	—
	MSTPD10	—	CANFD module stop bit
	MSTPD26	—	Module stop bit for serial peripheral interface 0
DPSBYCR	—	Deep standby control register	—
DPSIER0	—	Deep standby interrupt enable register 0	—
DPSIER1	—	Deep standby interrupt enable register 1	—
DPSIER2	—	Deep standby interrupt enable register 2	—
DPSIFR0	—	Deep standby interrupt flag register 0	—
DPSIFR1	—	Deep standby interrupt flag register 1	—
DPSIFR2	—	Deep standby interrupt flag register 2	—
DPSIEGR0	—	Deep standby interrupt edge register 0	—
DPSIEGR1	—	Deep standby interrupt edge register 1	—
DPSIEGR2	—	Deep standby interrupt edge register 2	—
DPSBKRy	—	Deep standby backup register (y = 0 to 31)	—

2.8 Register Write Protection Function

Table 2.12 is Comparative Overview of Register Write Protection Functions.

Table 2.12 Comparative Overview of Register Write Protection Functions

Item	RX66T	RX26T
PRC0 bit	• Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, OSTDCR, OSTDSR	• Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, MOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, OSTDCR, OSTDSR
PRC1 bit	• Registers related to the operating modes: SYSCR0, SYSCR1, VOLSR • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, RSTCKCR, DPSBYCR, DPSIER0 to DPSIER2, DPSIFR0 to DPSIFR2, DPSIEGR0 to DPSIEGR2 • Registers related to the clock generation circuit: MOSCWTCR, MOFCR, HOCOPCR • Software reset register: SWRR	• Registers related to the operating modes: SYSCR1, VOLSR • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, RSTCKCR • Registers related to the clock generation circuit: MOSCWTCR, MOFCR, HOCOPCR • Software reset register: SWRR
PRC3 bit	• Registers related to the LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	• Registers related to the LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

2.9 Interrupt Controller

Table 2.13 is Comparative Overview of Interrupt Controllers, and Table 2.14 is Comparison of Interrupt Controller Registers.

Table 2.13 Comparative Overview of Interrupt Controllers

Item		RX66T (ICUC)	RX26T (ICUG)
Interrupts	Peripheral interrupts	• Interrupts from peripheral modules • Interrupt detection method: Edge detection or level detection (fixed for each interrupt source) • Group interrupt: Multiple interrupt sources are grouped together and treated as an interrupt source. — Group IE0 interrupt: Interrupt sources of coprocessors that use ICLK as the operating clock (edge detection) — Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) — Group BL0/BL1/BL2 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) — Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.	• Interrupts from peripheral modules • Interrupt detection method: Edge detection or level detection (fixed for each interrupt source) • Group interrupt: Multiple interrupt sources are grouped together and treated as an interrupt source. — Group IE0 interrupt: Interrupt sources of coprocessors that use ICLK as the operating clock (edge detection) — Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) — Group BL0/BL1/BL2 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) — Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.
	External pin interrupts	Interrupts by input signals on IRQi pins (i = 0 to 15) • Interrupt detection: Detection of low level, falling edge, rising edge, or rising and falling edges can be set for each source. • A digital filter can be used to remove noise.	Interrupts by input signals on IRQi pins (i = 0 to 15) • Interrupt detection: Detection of low level, falling edge, rising edge, or rising and falling edges can be set for each source. • A digital filter can be used to remove noise.
	Software interrupts	• An interrupt request can be generated by writing to a register. • Number of interrupt sources: 2	• An interrupt request can be generated by writing to a register. • Number of interrupt sources: 2

Item		RX66T (ICUC)	RX26T (ICUG)
Interrupts	Interrupt priority level	The priority level is set with the interrupt source priority register r (IPRr) (r = 000 to 255).	The priority level is set with the interrupt source priority register r (IPRr) (r = 000 to 255).
	Fast interrupt function	The CPU interrupt response time can be reduced. This setting can be used for one interrupt source only.	The CPU interrupt response time can be reduced. This setting can be used for one interrupt source only.
	DTC and DMAC control	The DTC and DMAC can be activated by an interrupt source.	The DTC and DMAC can be activated by an interrupt source.
Non-maskable interrupts	NMI pin interrupt	Interrupt by the input signal on the NMI pin • Interrupt detection: Falling edge or rising edge • A digital filter can be used to remove noise.	Interrupt by the input signal on the NMI pin • Interrupt detection: Falling edge or rising edge • A digital filter can be used to remove noise.
	Oscillation stop detection interrupt	Interrupt generated when stopped oscillation on main clock oscillation is detected	Interrupt generated when stopped oscillation on main clock oscillation is detected
	WDT underflow/ refresh error interrupt	Interrupt generated when the watchdog timer underflows or a refresh error occurs	Interrupt generated when the watchdog timer underflows or a refresh error occurs
	IWDT underflow/ refresh error interrupt	Interrupt generated when the independent watchdog timer underflows or a refresh error occurs	Interrupt generated when the independent watchdog timer underflows or a refresh error occurs
	Voltage monitoring 1 interrupt	Interrupt from voltage detection circuit 1 (LVD1)	Interrupt from voltage detection circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Interrupt from voltage detection circuit 2 (LVD2)	Interrupt from voltage detection circuit 2 (LVD2)
	RAM error interrupt	Interrupt generated when a parity check error is detected in the RAM or an ECC error is detected in the ECCRAM	Interrupt generated when a parity check error is detected in the RAM
Return from low power consumption state	Sleep mode	Exit sleep mode by any interrupt source.	Exit sleep mode by any interrupt source.
	All-module clock stop mode	Exit all-module clock stop mode by the NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection, USB0 resume, IWDT, or TMR0 to TMR3).	Exit all-module clock stop mode by the NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection, IWDT, or TMR0 to TMR3).
	Software standby mode	Exit software standby mode by the NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB0 resume, or IWDT).	Exit software standby mode by the NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, or IWDT).

Item		RX66T (ICUC)	RX26T (ICUG)
Return from low power consumption state	Deep software standby mode	Exit deep software standby mode by the NMI pin interrupt, specific external pin interrupt, or peripheral interrupt (voltage monitoring 1 or voltage monitoring 2).	Exit deep software standby mode by the NMI pin interrupt, specific external pin interrupt, or peripheral interrupt (voltage monitoring 1 or voltage monitoring 2).

Table 2.14 Comparison of Interrupt Controller Registers

Register	Bit	RX66T (ICUC)	RX26T (ICUG)
GRPBE0	—	Group BE0 interrupt request register	—
GRPBL2	—	—	Group BL2 interrupt request register
GRPAL1	—	—	Group AL1 interrupt request register
GENBE0	—	Group BE0 interrupt request enable register	—
GENBL2	—	—	Group BL2 interrupt request enable register
GENAL1	—	—	Group AL1 interrupt request enable register
GCRBE0	—	Group BE0 interrupt clear register	—
PIARk	—	Software configurable interrupt A request register k (k = 0h to 12h)	Software configurable interrupt A request register k (k = 0h to Fh, 12h to 14)
SLIARn	b7-b0	Software configurable interrupt A source select register 00h: Interrupt sources are not selected. 01h: Interrupt source number 1 : : 80h: Interrupt source number 128 : : 91h: Interrupt source number 145 : : : : : : : : FEh: Interrupt source number 254 FFh: Interrupt sources are not selected.	Software configurable interrupt A source select register 00h: No interrupt sources are selected. 01h: Interrupt source number 1 : : : : : : : : 92h: Interrupt source number 146 : : A7h: Interrupt source number 167 : : FEh: Interrupt source number 254 FFh: No interrupt sources are selected.

2.10 Buses

Table 2.15 is Comparative Overview of Buses, Table 2.16 is Comparative Overview of External Buses, and Table 2.17 is Comparison of Bus Registers.

Table 2.15 Comparative Overview of Buses

Item		RX66T	RX26T
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ECCRAM, or code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM or code flash memory) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ECCRAM, or code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM or code flash memory) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	Connected to RAM	Connected to RAM
	Memory bus 2	Connected to code flash memory	Connected to code flash memory
	Memory bus 3	Connected to ECCRAM	—
Internal main buses	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DTC and DMAC • Connected to on-chip memory (RAM, ECCRAM, or code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the DTC and DMAC • Connected to on-chip memory (RAM or code flash memory) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (TFU, DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral module clock (PCLKB)	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral module clock (PCLKB)
	Internal peripheral bus 3	• Connected to peripheral modules (USBb and CMPC) • Operates in synchronization with the peripheral module clock (PCLKB)	• Connected to peripheral modules (DOC, RSCI, CANFD, and CMPC) • Operates in synchronization with the peripheral module clock (PCLKB)

Item		RX66T	RX26T
Internal peripheral buses	Internal peripheral bus 4	• Connected to peripheral modules (MTU3, GPTW, HRPWM, RSPI, and SCIi) • Operates in synchronization with the peripheral module clock (PCLKA)	• Connected to peripheral modules (MTU, GPTW, HRPWM, and RSPI) • Operates in synchronization with the peripheral module clock (PCLKA)
	Internal peripheral bus 5	Reserved area	• Connected to peripheral modules (RSCI, RSCI, RI3C, and CANFD) • Operates in synchronization with the peripheral-module clock (PCLKA)
	Internal peripheral bus 6	• Connected to code flash memory (for programming and erasure) or data flash memory • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to code flash memory (for programming and erasure) or data flash memory • Operates in synchronization with the FlashIF clock (FCLK)
External bus	CS area	• Connected to an external device • Operates in synchronization with the external bus clock (BCLK)	—

Table 2.16 Comparative Overview of External Buses

Item	RX66T	RX26T
External address space	• An external address space is divided into four CS areas (CS0 to CS3) for management. • Chip select signals can be output for each area. • The bus width can be selected for each area. — Separate bus: 8-bit or 16-bit bus space can be selected. — Address/data multiplexed bus: 8-bit or 16-bit bus space can be selected. • Endian can be specified for each area.	—
CS area controller	• Recovery cycles can be inserted. — Read recovery: Up to 15 cycles — Write recovery: Up to 15 cycles • Cycle wait function: Up to 31 wait cycles (page access: Up to 7 wait cycles) • Wait control — Timing of assertion and negation for chip select signals (CS0# to CS3#) can be specified. — Assertion timing for read signals (RD#) and write signals (WR0# and WR# to WR1#) can be specified. — The timing at which data output starts and ends can be specified. • Write access mode: — Single write strobe mode — Byte strobe mode • Separate bus or address/data multiplexed bus can be specified for each area.	—
Write buffer function	When write data from the bus master is written to the write buffer, write access by the bus master is completed.	—
Frequency	The CS area controller (CSC) operates in synchronization with the external-bus clock (BCLK).	—

Table 2.17 Comparison of Bus Registers

Register	Bit	RX66T	RX26T
CSnCR	—	CSn control register (n = 0 to 3)	—
CSnREC	—	CSn recovery cycle setting register (n = 0~3)	—
CSRECEN	—	CS recovery cycle insertion enable register	—
CSnMOD	—	CSn mode register (n = 0 to 3)	—
CSnWCR1	—	CSn wait control register 1 (n = 0 to 3)	—
CSnWCR2	—	CSn wait control register 2 (n = 0 to 3)	—
BUSPRI	BPRA[1:0]	Memory bus 1 or 3 (RAM/ECCRAM) priority control bits b1 b0 0 0: Priority fixed 0 1: Priority toggled 1 0: Setting prohibited. 1 1: Setting prohibited.	Memory bus 1 (RAM) priority control bits b1 b0 0 0: Priority fixed 0 1: Priority toggled 1 0: Setting prohibited 1 1: Setting prohibited
	BPHB[1:0]	Internal peripheral bus 4 priority control bits b9 b8 0 0: Priority fixed 0 1: Priority toggled 1 0: Setting prohibited 1 1: Setting prohibited	Priority control bits for internal peripheral buses 4 and 5 b9 b8 0 0: Priority fixed 0 1: Priority toggled 1 0: Setting prohibited 1 1: Setting prohibited
	BPEB[1:0]	External bus priority control bits	—

2.11 Data Transfer Controller

Table 2.18 is Comparative Overview of Data Transfer Controllers, and Table 2.19 is Comparison of Data Transfer Controller Registers.

Table 2.18 Comparative Overview of Data Transfer Controllers

Item	RX66T (DTCa)	RX26T (DTCb)
Number of transfer channels	Equal to the number of all interrupt sources that can start a DTC transfer	Equal to the number of all interrupt sources that can start a DTC transfer
Transfer modes	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode A single activation leads to a single data transfer. The transfer address returns to the transfer start address after the number of data transfers corresponding to “repeat size”. The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, or 1,024 bytes. • Block transfer mode A single activation leads to the transfer of a single block of data. The maximum block size is 256 × 32 bits = 1,024 bytes.	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode A single activation leads to a single data transfer. The transfer address returns to the transfer start address after the number of data transfers corresponding to “repeat size”. The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, or 1,024 bytes. • Block transfer mode A single activation leads to the transfer of a single block of data. The maximum block size is 256 × 32 bits = 1,024 bytes.
Chain transfer function	• Multiple types of data transfer can be performed sequentially in response to a single transfer request. • Either “performed only when the transfer counter reaches 0” or “every time” can be selected.	• Multiple types of data transfer can be performed sequentially in response to a single transfer request. • Either “performed only when the transfer counter reaches 0” or “every time” can be selected.
Sequence transfer	—	A complex series of transfers can be registered as a sequence. Any sequence can be selected by the transfer data and executed. • Only one sequence transfer trigger source can be selected at a time. • Up to 256 sequences can correspond to a single trigger source. • The data that is initially transferred in response to a transfer request determines the sequence. • The entire sequence can be executed on a single request, or the sequence can be suspended in the middle and resumed on the next transfer request (sequence division).

Item	RX66T (DTCa)	RX26T (DTCb)
Transfer space	• Short-address mode: 16 MB (from 0000 0000h to 007F FFFFh or from FF80 0000h to FFFF FFFFh, excluding reserved areas) • Full-address mode: 4 GB (within 0000 0000h to FFFF FFFFh, excluding reserved areas)	• Short-address mode: 16 MB (from 0000 0000h to 007F FFFFh or from FF80 0000h to FFFF FFFFh, excluding reserved areas) • Full-address mode: 4 GB (within 0000 0000h to FFFF FFFFh, excluding reserved areas)
Data transfer units	• Single data: 1 byte (8 bits), 1 word (16 bits), 1 longword (32 bits) • Single block size: 1 to 256 data units	• Single data: 1 byte (8 bits), 1 word (16 bits), 1 longword (32 bits) • Single block size: 1 to 256 data units
CPU interrupt requests	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.
Event link function	An event link request is generated after one data transfer (for block transfers, after one block).	An event link request is generated after one data transfer (for block transfers, after one block).
Read skip	Reading of the transfer information can be skipped when the same transfer is repeated.	Reading of the transfer information can be skipped when the same transfer is repeated.
Write-back skip	Write-back of transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.	Write-back of transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.
Write-back disable	—	Ability to disable write-back of transfer information
Displacement addition	—	Ability to add displacement to the transfer source address (selectable by each transfer information)
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Table 2.19 Comparison of Data Transfer Controller Registers

Register	Bit	RX66T (DTCa)	RX26T (DTCb)
MRA	WBDIS	—	Write-back disable bit
MRB	SQEND	—	Sequence transfer end bit
	INDX	—	Index table reference bit
MRC	—	—	DTC mode register C
DTCIBR	—	—	DTC index table base register
DTCOR	—	—	DTC operation register
DTCSQE	—	—	DTC sequence transfer enable register
DTCDISP	—	—	DTC address displacement register

2.12 Event Link Controller

Table 2.20 is Comparative Overview of Event Link Controllers, Table 2.21 is Comparison of Event Link Controller Registers, Table 2.22 is Correspondence between ELSRn Registers and Peripheral Modules, and Table 2.23 is Correspondence between Values Set in ELSRn.ELS[7:0] Bits and Event Signal Names.

Table 2.20 Comparative Overview of Event Link Controllers

Item	RX66T (ELC)	RX26T (ELC)
Event link function	• 188 types of event signals can be directly connected to peripheral modules. • The operation of peripheral timer modules at event input is selectable. • Event link operation is possible for port B and port E. — Single port*1: Event link operation can be enabled for a specified single port. — Port group*1: Event link operation can be enabled for multiple specified ports within a group of up to eight ports.	• 182 types of event signals can be directly connected to peripheral modules. • The operation of peripheral timer modules at event input is selectable. • Event link operation is possible for port B and port E. — Single port*1: Event link operation can be enabled for a specified single port. — Port group*1: Event link operation can be enabled for multiple specified ports within a group of up to eight ports.
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Note: 1. For the single port or port group specified for input, an event occurs when the input signal on the corresponding pin changes.

Table 2.21 Comparison of Event Link Controller Registers

Register	Bit	RX66T (ELC)	RX26T (ELC)
ELSRn	—	Event link setting register n (ELSRn) (n = 0, 3, 4, 7, 10 to 13, 15, 16, 18 to 28, 30, 31, 45 to 58)	Event link setting register n (ELSRn) (n = 0, 3, 4, 7, 10 to 13, 15, 16, 18 to 28, 30, 31, 33, 45 to 58)
	ELS[7:0]	Event link select bits 00h: Event signal output to the corresponding peripheral module is disabled. 01h to F1h: Specifies the number of the event signal to be linked. Settings other than the above are prohibited.	Event link select bits 00h: Event signal output to the corresponding peripheral module is disabled. 01h to FBh: Specifies the number of the event signal to be linked. Settings other than the above are prohibited.
ELOPH	—	—	Event link option setting register H

Table 2.22 Correspondence between ELSRn Registers and Peripheral Modules

Register	RX66T (ELC)	RX26T (ELC)
ELSR0	MTU0	MTU0
ELSR3	MTU3	MTU3
ELSR4	MTU4	MTU4
ELSR7	CMT1	CMT1
ELSR10	TMR0	TMR0
ELSR11	TMR1	TMR1
ELSR12	TMR2	TMR2
ELSR13	TMR3	TMR3
ELSR15	S12AD (ELCTRG00N)	S12AD (ELCTRG00N)
ELSR16	DA0	DA0
ELSR18	ICU (interrupt 1)*1	ICU (interrupt 1)*1
ELSR19	ICU (interrupt 2)*1	ICU (interrupt 2)*1
ELSR20	Output port group 1	Output port group 1
ELSR21	Output port group 2	Output port group 2
ELSR22	Input port group 1	Input port group 1
ELSR23	Input port group 2	Input port group 2
ELSR24	Single port 0*2	Single port 0*2
ELSR25	Single port 1*2	Single port 1*2
ELSR26	Single port 2*2	Single port 2*2
ELSR27	Single port 3*2	Single port 3*2
ELSR28	Clock source switching to LOCO	Clock source switching to LOCO
ELSR30	MTU6	MTU6
ELSR31	MTU7	MTU7
ELSR33	—	CMTW0
ELSR45	S12AD1 (ELCTRG10N)	S12AD1 (ELCTRG10N)
ELSR46	S12AD2 (ELCTRG20N)	S12AD2 (ELCTRG20N)
ELSR47	MTU9	MTU9
ELSR48	GPTW event cause A (common to all channels)	GPTW event cause A (common to all channels)
ELSR49	GPTW event cause B (common to all channels)	GPTW event cause B (common to all channels)
ELSR50	GPTW event cause C (common to all channels)	GPTW event cause C (common to all channels)
ELSR51	GPTW event cause D (common to all channels)	GPTW event cause D (common to all channels)
ELSR52	GPTW event cause E (common to all channels)	GPTW event cause E (common to all channels)
ELSR53	GPTW event cause F (common to all channels)	GPTW event cause F (common to all channels)
ELSR54	GPTW event cause G (common to all channels)	GPTW event cause G (common to all channels)
ELSR55	GPTW event cause H (common to all channels)	GPTW event cause H (common to all channels)
ELSR56	S12AD (ELCTRG01N)	S12AD (ELCTRG01N)
ELSR57	S12AD1 (ELCTRG11N)	S12AD1 (ELCTRG11N)
ELSR58	S12AD2 (ELCTRG21N)	S12AD2 (ELCTRG21N)

Notes: 1. Select the event signal from EAh to F1h. Setting any other value is prohibited.
2. The DOC data operation condition set signal (F1h) cannot be set in the ELSR24, ELSR25, ELSR26, or ELSR27 register.

Table 2.23 Correspondence between Values Set in ELSRn.ELS[7:0] Bits and Event Signal Names

Value of [7:0] Bits	Peripheral Modules	RX66T (ELC)	RX26T (ELC)
01h	Multi-function timer pulse unit 3	MTU0 compare match 0A	MTU0 compare match 0A
02h		MTU0 compare match 0B	MTU0 compare match 0B
03h		MTU0 compare match 0C	MTU0 compare match 0C
04h		MTU0 compare match 0D	MTU0 compare match 0D
05h		MTU0 compare match 0E	MTU0 compare match 0E
06h		MTU0 compare match 0F	MTU0 compare match 0F
07h		MTU0 overflow	MTU0 overflow
10h		MTU3 compare match 3A	MTU3 compare match 3A
11h		MTU3 compare match 3B	MTU3 compare match 3B
12h		MTU3 compare match 3C	MTU3 compare match 3C
13h		MTU3 compare match 3D	MTU3 compare match 3D
14h		MTU3 overflow	MTU3 overflow
15h		MTU4 compare match 4A	MTU4 compare match 4A
16h		MTU4 compare match 4B	MTU4 compare match 4B
17h		MTU4 compare match 4C	MTU4 compare match 4C
18h		MTU4 compare match 4D	MTU4 compare match 4D
19h		MTU4 overflow	MTU4 overflow
1Ah		MTU4 underflow	MTU4 underflow
1Eh		MTU6 compare match 6A	MTU6 compare match 6A
1Fh		MTU6 compare match 6B	MTU6 compare match 6B
20h		MTU6 compare match 6C	MTU6 compare match 6C
21h		MTU6 compare match 6D	MTU6 compare match 6D
22h		MTU6 overflow	MTU6 overflow
23h		MTU7 compare match 7A	MTU7 compare match 7A
24h		MTU7 compare match 7B	MTU7 compare match 7B
25h		MTU7 compare match 7C	MTU7 compare match 7C
26h		MTU7 compare match 7D	MTU7 compare match 7D
27h		MTU7 overflow	MTU7 overflow
28h		MTU7 underflow	MTU7 underflow
2Fh		MTU9 compare match 9A	MTU9 compare match 9A
30h		MTU9 compare match 9B	MTU9 compare match 9B
31h		MTU9 compare match 9C	MTU9 compare match 9C
32h		MTU9 compare match 9D	MTU9 compare match 9D
33h		MTU9 compare match 9E	MTU9 compare match 9E
34h		MTU9 compare match 9F	MTU9 compare match 9F
35h		MTU9 overflow	MTU9 overflow
37h	Compare match timer	CMT1 compare match 1	CMT1 compare match 1
3Ah	Compare match timer W	—	CMTW0 compare match
3Ch	8-bit timer	TMR0 compare match A0	TMR0 compare match A0
3Dh		TMR0 compare match B0	TMR0 compare match B0
3Eh		TMR0 overflow	TMR0 overflow
3Fh		TMR1 compare match A1	TMR1 compare match A1
40h		TMR1 compare match B1	TMR1 compare match B1
41h		TMR1 overflow	TMR1 overflow
42h		TMR2 compare match A2	TMR2 compare match A2
43h		TMR2 compare match B2	TMR2 compare match B2
44h		TMR2 overflow	TMR2 overflow

Value of [7:0] Bits	Peripheral Modules	RX66T (ELC)	RX26T (ELC)
45h	8-bit timer	TMR3 compare match A3	TMR3 compare match A3
46h		TMR3 compare match B3	TMR3 compare match B3
47h		TMR3 overflow	TMR3 overflow
48h	General purpose PWM timer	GPTW0 compare match A	GPTW0 compare match A
49h		GPTW0 compare match B	GPTW0 compare match B
4Ah		GPTW0 compare match C	GPTW0 compare match C
4Bh		GPTW0 compare match D	GPTW0 compare match D
4Ch		GPTW0 compare match E	GPTW0 compare match E
4Dh		GPTW0 compare match F	GPTW0 compare match F
4Eh		GPTW0 overflow	GPTW0 overflow
4Fh		GPTW0 underflow	GPTW0 underflow
50h		GPTW0 A/D conversion start request A	GPTW0 A/D conversion start request A
51h		GPTW0 A/D conversion start request B	GPTW0 A/D conversion start request B
52h		GPTW1 compare match A	GPTW1 compare match A
53h		GPTW1 compare match B	GPTW1 compare match B
54h		GPTW1 compare match C	GPTW1 compare match C
55h		GPTW1 compare match D	GPTW1 compare match D
56h		GPTW1 compare match E	GPTW1 compare match E
57h		GPTW1 compare match F	GPTW1 compare match F
58h		GPTW1 overflow	GPTW1 overflow
59h		GPTW1 underflow	GPTW1 underflow
5Ah		GPTW1 A/D conversion start request A	GPTW1 A/D conversion start request A
5Bh		GPTW1 A/D conversion start request B	GPTW1 A/D conversion start request B
5Ch		GPTW2 compare match A	GPTW2 compare match A
5Dh		GPTW2 compare match B	GPTW2 compare match B
5Eh		GPTW2 compare match C	GPTW2 compare match C
5Fh		GPTW2 compare match D	GPTW2 compare match D
60h		GPTW2 compare match E	GPTW2 compare match E
61h		GPTW2 compare match F	GPTW2 compare match F
62h		GPTW2 overflow	GPTW2 overflow
63h		GPTW2 underflow	GPTW2 underflow
64h		GPTW2 A/D conversion start request A	GPTW2 A/D conversion start request A
65h		GPTW2 A/D conversion start request B	GPTW2 A/D conversion start request B
66h		GPTW3 compare match A	GPTW3 compare match A
67h		GPTW3 compare match B	GPTW3 compare match B
68h		GPTW3 compare match C	GPTW3 compare match C
69h		GPTW3 compare match D	GPTW3 compare match D
6Ah		GPTW3 compare match E	GPTW3 compare match E
6Bh		GPTW3 compare match F	GPTW3 compare match F
6Ch		GPTW3 overflow	GPTW3 overflow
6Dh		GPTW3 underflow	GPTW3 underflow
6Eh		GPTW3 A/D conversion start request A	GPTW3 A/D conversion start request A
6Fh		GPTW3 A/D conversion start request B	GPTW3 A/D conversion start request B
70h		GPTW4 compare match A	GPTW4 compare match A
71h		GPTW4 compare match B	GPTW4 compare match B
72h		GPTW4 compare match C	GPTW4 compare match C
73h		GPTW4 compare match D	GPTW4 compare match D
74h		GPTW4 compare match E	GPTW4 compare match E
75h		GPTW4 compare match F	GPTW4 compare match F
76h		GPTW4 overflow	GPTW4 overflow

Value of [7:0] Bits	Peripheral Modules	RX66T (ELC)	RX26T (ELC)
77h	General purpose PWM timer	GPTW4 underflow	GPTW4 underflow
78h		GPTW4 A/D conversion start request A	GPTW4 A/D conversion start request A
79h		GPTW4 A/D conversion start request B	GPTW4 A/D conversion start request B
7Ah		GPTW5 compare match A	GPTW5 compare match A
7Bh		GPTW5 compare match B	GPTW5 compare match B
7Ch		GPTW5 compare match C	GPTW5 compare match C
7Dh		GPTW5 compare match D	GPTW5 compare match D
7Eh		GPTW5 compare match E	GPTW5 compare match E
7Fh		GPTW5 compare match F	GPTW5 compare match F
80h		GPTW5 overflow	GPTW5 overflow
81h		GPTW5 underflow	GPTW5 underflow
82h		GPTW5 A/D conversion start request A	GPTW5 A/D conversion start request A
83h		GPTW5 A/D conversion start request B	GPTW5 A/D conversion start request B
84h		GPTW6 compare match A	GPTW6 compare match A
85h		GPTW6 compare match B	GPTW6 compare match B
86h		GPTW6 compare match C	GPTW6 compare match C
87h		GPTW6 compare match D	GPTW6 compare match D
88h		GPTW6 compare match E	GPTW6 compare match E
89h		GPTW6 compare match F	GPTW6 compare match F
8Ah		GPTW6 overflow	GPTW6 overflow
8Bh		GPTW6 underflow	GPTW6 underflow
8Ch		GPTW6 A/D conversion start request A	GPTW6 A/D conversion start request A
8Dh		GPTW6 A/D conversion start request B	GPTW6 A/D conversion start request B
8Eh		GPTW7 compare match A	GPTW7 compare match A
8Fh		GPTW7 compare match B	GPTW7 compare match B
90h		GPTW7 compare match C	GPTW7 compare match C
91h		GPTW7 compare match D	GPTW7 compare match D
92h		GPTW7 compare match E	GPTW7 compare match E
93h		GPTW7 compare match F	GPTW7 compare match F
94h		GPTW7 overflow	GPTW7 overflow
95h		GPTW7 underflow	GPTW7 underflow
96h		GPTW7 A/D conversion start request A	GPTW7 A/D conversion start request A
97h		GPTW7 A/D conversion start request B	GPTW7 A/D conversion start request B
98h		GPTW8 compare match A	—
99h		GPTW8 compare match B	—
9Ah		GPTW8 compare match C	—
9Bh		GPTW8 compare match D	—
9Ch		GPTW8 compare match E	—
9Dh		GPTW8 compare match F	—
9Eh		GPTW8 overflow	—
9Fh		GPTW8 underflow	—
A0h		GPTW8 A/D conversion start request A	—
A1h		GPTW8 A/D conversion start request B	—
A2h		GPTW9 compare match A	—
A3h		GPTW9 compare match B	—
A4h		GPTW9 compare match C	—
A5h		GPTW9 compare match D	—
A6h		GPTW9 compare match E	—
A7h		GPTW9 compare match F	—
A8h		GPTW9 overflow	—

Value of [7:0] Bits	Peripheral Modules	RX66T (ELC)	RX26T (ELC)
A9h	General purpose PWM timer	GPTW9 underflow	—
AAh		GPTW9 A/D conversion start request A	—
ABh		GPTW9 A/D conversion start request B	—
AFh	Independent watchdog timer	IWDT underflow or refresh error	IWDT underflow or refresh error
B8h	Serial communications interface	SCI5 error (receive error or error signal detection)	SCI5 error (receive error or error signal detection)
B9h		SCI5 receive data full	SCI5 receive data full
BAh		SCI5 transmit data empty	SCI5 transmit data empty
BBh		SCI5 transmit end	SCI5 transmit end
C8h		—	RSCI11 error
C9h		—	RSCI11 receive data full
CAh		—	RSCI11 transmit data empty
CBh		—	RSCI11 transmit end
CCh	I^2C bus interface	RIIC0 communication error or event generation	RIIC0 communication error or event generation
CDh		RIIC0 receive data full	RIIC0 receive data full
CEh		RIIC0 transmit data empty	RIIC0 transmit data empty
CFh		RIIC0 transmit end	RIIC0 transmit end
D0h	Serial peripheral interface	RSPI0 error (mode fault, overrun, underrun, or parity error)	RSPI0 error (mode fault, overrun, underrun, or parity error)
D1h		RSPI0 idle	RSPI0 idle
D2h		RSPI0 receive buffer full	RSPI0 receive buffer full
D3h		RSPI0 transmit buffer empty	RSPI0 transmit buffer empty
D4h		RSPI0 transmit end	RSPI0 transmit end
D6h	12-bit A/D converter	S12AD A/D conversion end	S12AD A/D conversion end
D8h		S12AD1 A/D conversion end	S12AD1 A/D conversion end
DAh		S12AD2 A/D conversion end	S12AD2 A/D conversion end
DCh	Comparator C	Comparator C0 comparison result change	Comparator C0 comparison result change
DDh		Comparator C1 comparison result change	Comparator C1 comparison result change
DEh		Comparator C2 comparison result change	Comparator C2 comparison result change
DFh		Comparator C3 comparison result change	Comparator C3 comparison result change
E0h		Comparator C4 comparison result change	Comparator C4 comparison result change
E1h		Comparator C5 comparison result change	Comparator C5 comparison result change
E2h	Voltage detection circuit	LVD1 voltage detection	LVD1 voltage detection
E3h		LVD2 voltage detection	LVD2 voltage detection
E4h	DMA controller	DMAC0 transfer end	DMAC0 transfer end
E5h		DMAC1 transfer end	DMAC1 transfer end
E6h		DMAC2 transfer end	DMAC2 transfer end
E7h		DMAC3 transfer end	DMAC3 transfer end
E8h	Data Transfer Controller	DTC transfer end	DTC transfer end
E9h	Clock generation circuit	Oscillation stop detection of the clock generation circuit	Oscillation stop detection of the clock generation circuit

Value of [7:0] Bits	Peripheral Modules	RX66T (ELC)	RX26T (ELC)
EAh	I/O ports	Input edge detection of input port group 1	Input edge detection of input port group 1
EBh		Input edge detection of input port group 2	Input edge detection of input port group 2
ECh		Input edge detection of single input port 0	Input edge detection of single input port 0
EDh		Input edge detection of single input port 1	Input edge detection of single input port 1
EEh		Input edge detection of single input port 2	Input edge detection of single input port 2
EFh		Input edge detection of single input port 3	Input edge detection of single input port 3
F0h	Event link controller	Software event	Software event
F1h	Data operation circuit	DOC data operation condition met	DOC data operation condition met
F2h	I^3C bus interface	—	RI3C0 communication error or event generation
F3h		—	RI3C0 receive data full
F4h		—	RI3C0 transmit data empty
F6h	Serial peripheral interface	—	RSPIA0 error
F7h		—	RSPIA0 idle
F8h		—	RSPIA0 receive buffer full
F9h		—	RSPIA0 transmit buffer empty
FAh		—	RSPIA0 communication complete
FBh	General purpose PWM timer	—	Input edge detection for UVW phase of GPTW (OPS)

2.13 I/O Ports

Table 2.24 to Table 2.27 provide comparative overviews of I/O ports for each package (including Comparative Overview of I/O Ports on 100-Pin Products), Table 2.28 is Comparison of I/O Port Functions, and Table 2.30 is Comparison of I/O Port Registers.

Table 2.24 Comparative Overview of I/O Ports on 100-Pin Products

Item	RX66T (100-Pin)	RX26T (100-Pin)
PORT0	P00, P01	P00, P01
PORT1	P10, P11	P10, P11
PORT2	P20 to P24	P20 to P24, P27
PORT3	P30 to P33, P36, P37	P30 to P33, P36, P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P55	P50 to P55
PORT6	P60 to P65	P60 to P65
PORT7	P70 to P76	P70 to P76
PORT8	P80 to P82	P80 to P82
PORT9	P90 to P96	P90 to P96
PORTA	PA0 to PA5	PA0 to PA5
PORTB	PB0 to PB7	PB0 to PB7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE5	PE0 to PE5
PORTN	—	PN6, PN7

Table 2.25 Comparative Overview of I/O Ports on 80-Pin Products

Item	RX66T (80-Pin)	RX26T (80-Pin)
PORT0	P00, P01	P00, P01
PORT1	P10, P11	P10, P11
PORT2	P20 to P22, P27	P20 to P22, P27
PORT3	P30, P31, P36, P37	P30, P31, P36, P37
PORT4	P40 to P47	P40 to P47
PORT5	P52 to P55	P50 to P55
PORT6	P62, P64, P65	P60, P64, P65
PORT7	P70 to P76	P70 to P76
PORT9	P90 to P96	P90 to P96
PORTA	PA3, PA5	PA3, PA5
PORTB	PB0 to PB6	PB0 to PB6
PORTD	PD2 to PD7	PD2 to PD7
PORTE	PE2 to PE4	PE2 to PE4
PORTH	PH0, PH4	—
PORTN	—	PN6, PN7

Table 2.26 Comparative Overview of I/O Ports on 64-Pin Products

Item	RX66T (64-Pin)	RX26T (64-Pin)
PORT0	P00, P01	P00, P01
PORT1	P11	P11
PORT2	P20 to P22	P20 to P22
PORT3	P36, P37	P36, P37
PORT4	P40 to P42, P44 to P46	P40 to P47
PORT5	P52 to P54	P52 to P54
PORT6	P64, P65	P64, P65
PORT7	P70 to P76	P70 to P76
PORT9	P90 to P96	P90 to P96
PORTB	PB0 to PB6	PB0 to PB6
PORTD	PD3 to PD7	PD3 to PD7
PORTE	PE2	PE2
PORTH	PH0, PH4	—
PORTN	—	PN6, PN7

Table 2.27 Comparative Overview of I/O Ports on 48-Pin Products

Item	RX66T (48-Pin)	RX26T (48-Pin)
PORT0	P00	P00
PORT1	P10, P11	P10, P11
PORT2	—	P20, P21
PORT3	P36, P37	P36, P37
PORT4	P40 to P44	P40 to P44
PORT5	—	P52, P53
PORT6	P62, P64, P65	P62
PORT7	P71 to P76	P71 to P76
PORT9	P94	P91 to P95
PORTA	PA3, PA5	—
PORTB	PB0 to PB6	PB0 to PB6
PORTD	PD3, PD5, PD7	PD3, PD5, PD7
PORTE	PE2	PE2
PORTN	—	PN6

Table 2.28 Comparison of I/O Port Functions

Item	Port Symbol	RX66T	RX26T
Input pull-up function	PORT0	P00, P01	P00, P01
	PORT1	P10 to P17	P10, P11
	PORT2	P20 to P27	P20 to P24, P27
	PORT3	P30 to P37	P30 to P33, P36, P37
	PORT4	P43, P47	P40 to P47
	PORT5	P50 to P55	P50 to P55
	PORT6	P60 to P65	P60 to P65
	PORT7	P70 to P76	P70 to P76
	PORT8	P80 to P82	P80 to P82
	PORT9	P90 to P96	P90 to P96
	PORTA	PA0 to PA7	PA0 to PA5
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC6	—
	PORTD	PD0 to PD7	PD0 to PD7
	PORTE	PE0, PE1, PE3 to PE6	PE0, PE1, PE3 to PE5
	PORTF	PF0 to PF3	—
	PORTG	PG0 to PG2	—
	PORTH	PH1 to PH3, PH5 to PH7	—
	PORTK	PK0 to PK2	—
	PORTN	—	PN6, PN7
Open-drain output function	PORT0	P00, P01	P00, P01
	PORT1	P10 to P17	P10, P11
	PORT2	P20 to P27	P20 to P24, P27
	PORT3	P30 to P37	P30 to P33, P36, P37
	PORT4	P43, P47	P40 to P47
	PORT5	P50 to P55	P50 to P55
	PORT6	P60 to P65	P60 to P65
	PORT7	P70 to P76	P70 to P76
	PORT8	P80 to P82	P80 to P82
	PORT9	P90 to P96	P90 to P96
	PORTA	PA0 to PA7	PA0 to PA5
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC6	—
	PORTD	PD0 to PD7	PD0 to PD7
	PORTE	PE0, PE1, PE3 to PE6	PE0, PE1, PE3 to PE5
	PORTF	PF0 to PF3	—
	PORTG	PG0 to PG2	—
	PORTH	PH1 to PH3, PH5 to PH7	—
	PORTK	PK0 to PK2	—
	PORTN	—	PN6
5 V tolerant	PORTB	PB1, PB2	PB1, PB2
	PORTC	PC0*1	—
	PORTD	PD2*1	—

Note: 1. Valid only for products with a RAM capacity of 128 KB

Table 2.29 Comparison of Driving Capability Switching Function

Port Symbol	Driving Ability Switching	RX66T	RX26T
PORT0	Fixed to normal drive output	—	—
	Normal drive/high drive	P00, P01	P00, P01
PORT1	Fixed to normal drive output	—	—
	Normal drive/high drive	P10 to P17	P10, P11
PORT2	Fixed to normal drive output	—	—
	Normal drive/high drive	P20 to P27	P20 to P24, P27
PORT3	Fixed to normal drive output	P36, P37	P36, P37
	Normal drive/high drive	P30 to P35	P30 to P33
PORT4	Fixed to normal drive output	P43, P47	P40 to P47
	Normal drive/high drive	—	—
PORT5	Fixed to normal drive output	P50 to P55	P50 to P55
	Normal drive/high drive	—	—
PORT6	Fixed to normal drive output	P60 to P65	P60 to P65
	Normal drive/high drive	—	—
PORT7	Fixed to normal drive output	—	—
	Fixed to high drive output	—	—
	Normal drive/high drive	P70	P70
	Normal drive/high drive/large current output	P71 to P76	P71 to P76
PORT8	Fixed to normal drive output	—	—
	Fixed to high drive output	—	—
	Normal drive/high drive	P80, P82	P80, P82
	Normal drive/high drive/large current output	P81	P81
PORT9	Fixed to normal drive output	—	—
	Fixed to high drive output		—
	Normal drive/high drive	P96	P96
	Normal drive/high drive/large current output	P90 to P95	P90 to P95
PORTA	Fixed to normal drive output	—	—
	Normal drive/high drive	PA0 to PA7	PA0 to PA5
PORTB	Fixed to normal drive output	—	PB1, PB2
	Fixed to high drive output	—	—
	Normal drive/high drive	PB0 to PB4, PB6, PB7	PB0, PB3, PB4, PB6, PB7
	Normal drive/high drive/large current output	PB5	PB5
PORTC	Fixed to normal drive output	—	—
	Normal drive/high drive	PC0 to PC6	—

PORTD	Fixed to normal drive output	—	—
	Normal drive/high drive	PD0 to PD1, PD4 to PD7	PD0 to PD2, PD4 to PD7
	Normal drive/high drive/large current output	PD3	PD3
PORTE	Fixed to normal drive output	—	—
	Normal drive/high drive	PE0, PE1, PE3 to PE6	PE0, PE1, PE3 to PE5
PORTF	Normal drive/high drive	PF0 to PF3	—
PORTG	Normal drive/high drive	PG0 to PG2	—
PORTH	Fixed to normal drive output	PH1 to PH3, PH5 to PH7	—
PORTK	Normal drive/high drive	PK0 to PK2	—
PORTN	Fixed to normal drive output	—	—
	Normal drive/high drive	—	PN6, PN7

Table 2.30 Comparison of I/O Port Registers

Register	Bit	RX66T	RX26T
PDR	B0 to B7	Pm0 to Pm7 I/O select bits (m = 0 to 9, A to H, K)	Pm0 to Pm7 I/O select bits (m = 0 to 9, A, B, D, E, N)
PODR	B0 to B7	Pm0 to Pm7 output data store bits (m = 0 to 9, A to H, K)	Pm0 to Pm7 output data store bits (m = 0 to 9, A, B, D, E, N)
PIDR	B0 to B7	Pm0 to Pm7 bits (m = 0 to 9, A to H, K)	Pm0 to Pm7 bits (m = 0 to 9, A, B, D, E, N)
PMR	B0 to B7	Pm0 to Pm7 pin mode control bits (m = 0 to 9, A to H, K)	Pm0 to Pm7 pin mode control bits (m = 0 to 9, A, B, D, E, N)
ODR0	B0, B2, B4, B6	Pm0, Pm1, Pm2, and Pm3 output type select bits (m = 0 to 9, A to H, K)	Pm0, Pm1, Pm2, and Pm3 output type select bits (m = 0 to 9, A, B, D, E)
ODR1	B0, B2, B4, B6	Pm4, Pm5, Pm6, and Pm7 output type select bits (m = 1 to 7, 9, A to E, H)	Pm4, Pm5, Pm6, and Pm7 output type select bits (m = 2 to 7, 9, A, B, D, E, N)
PCR	B0 to B7	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A to H, K)	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A, B, D, E, N)
DSCR	B0 to B7	Pm0 to Pm7 drive capability control bits (m = 0 to 3, 7 to 9, A to G, K)	Pm0 to Pm7 drive capability control bits (m = 0 to 3, 7 to 9, A, B, D, E, N)
POHSR1	—	—	Port output retention setting register 1
POHSR2	—	—	Port output retention setting register 2
POHCR	—	—	Port output retention control register
GPSEXT	—	—	Extended register for general-purpose I/O pin selection

2.14 Multi-Function Pin Controller

Table 2.31 is Comparison of Multiplexed Pin Assignments, and Table 2.32 to Table 2.48 are comparisons of multi-function pin controller registers.

In the following comparison of the assignments of multiplexed pins, **blue text** designates pins that exist on the RX26T Group only, and **orange text** designates pins that exist on the RX66T Group only. A circle (○) indicates that a function is assigned, a cross (×) that the pin does not exist or that no function is assigned, and grayed out items mean that the function is not implemented.

Table 2.31 Comparison of Multiplexed Pin Assignments

Module/ Function	Pin Function	Port Allocation	RX66T (MPC)				RX26T (MPC)			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Interrupts	NMI (input)	PE2	○	○	○	○	○	○	○	○
	IRQ0-DS (input)	P10	○	○	×	○				
	IRQ0 (input)	P52	○	○	○	×	○	○	○	○
		PE5	○	×	×	×	○	×	×	×
		P10	×	×	×	×	○	○	×	○
		PE2	×	×	×	×	○	○	○	○
	IRQ1-DS (input)	P11	○	○	○	○				
	IRQ1 (input)	P53	○	○	○	×	○	○	○	○
		PA5	○	○	×	○	○	○	×	×
		PE4	○	○	×	×	○	○	×	×
		P11	×	×	×	×	○	○	○	○
		P95	×	×	×	×	○	○	○	○
	IRQ2-DS (input)	PE3	○	○	×	×				
	IRQ2 (input)	P00	○	○	○	○	○	○	○	○
		P54	○	○	○	×	○	○	○	×
		PB6	○	○	○	○	○	○	○	○
		PD4	○	○	○	×	○	○	○	×
		PE3	×	×	×	×	○	○	×	×
	IRQ3-DS (input)	PB4	○	○	○	○				
	IRQ3 (input)	P55	○	○	×	×	○	○	×	×
		P82	○	×	×	×	○	×	×	×
		PB4	×	×	×	×	○	○	○	○
	IRQ4-DS (input)	P96	○	○	○	×				
	IRQ4 (input)	P01	○	○	○	×	○	○	○	×
		P24	○	×	×	×	○	×	×	×
		P60	○	×	×	×	○	○	×	×
		PB1	○	○	○	○	○	○	○	○
		P96	×	×	×	×	○	○	○	×
	IRQ5-DS (input)	P70	○	○	○	×				
	IRQ5 (input)	P61	○	×	×	×	○	×	×	×
		P80	○	×	×	×	○	×	×	×
		PD6	○	○	○	×	○	○	○	×
		P70	×	×	×	×	○	○	○	×
		PN7	×	×	×	×	○	○	○	×
	IRQ6-DS (input)	P21	○	○	○	×				
	IRQ6 (input)	P31	○	○	×	×	○	○	×	×
		P62	○	○	×	○	○	×	×	○
		PD5	○	○	○	○	○	○	○	○
		P21	×	×	×	×	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX66T (MPC)				RX26T (MPC)			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Interrupts	IRQ7-DS (input)	P20	○	○	○	×				
	IRQ7 (input)	P30	○	○	×	×	○	○	×	×
		P63	○	×	×	×	○	×	×	×
		PE0	○	×	×	×	○	×	×	×
		P20	×	×	×	×	○	○	○	○
	IRQ8 (input)	P64	○	○	○	○	○	○	○	×
		PB0	○	○	○	○	○	○	○	○
		PD7	○	○	○	○	○	○	○	○
	IRQ9 (input)	P65	○	○	○	○	○	○	○	×
		PB3	○	○	○	○	○	○	○	○
	IRQ10 (input)	P22	○	○	○	×	○	○	○	×
	IRQ11 (input)	P23	○	×	×	×	○	×	×	×
	IRQ12-DS (input)	P32	○	×	×	×				
	IRQ12 (input)	P32	×	×	×	×	○	×	×	×
	IRQ13-DS (input)	P33	○	×	×	×				
	IRQ13 (input)	P33	×	×	×	×	○	×	×	×
	IRQ14-DS (input)	PA1	○	×	×	×				
	IRQ14 (input)	P93	×	×	×	×	○	○	○	○
		PA1	×	×	×	×	○	×	×	×
	IRQ15 (input)	P27	×	○	×	×	○	○	×	×
		PE1	○	×	×	×	○	×	×	×
Multi-function timer unit 3	MTIOC0A (input/output)/ MTIOC0A# (input/output)	P31	○	○	×	×	○	○	×	×
		PB3	○	○	○	○	○	○	○	○
		P70	×	×	×	×	○	○	○	×
	MTIOC0B (input/output)/ MTIOC0B# (input/output)	P30	○	○	×	×	○	○	×	×
		PB2	○	○	○	○	○	○	○	○
	MTIOC0C (input/output)/ MTIOC0C# (input/output)	P27	×	○	×	×	○	○	×	×
		PB1	○	○	○	○	○	○	○	○
	MTIOC0D (input/output)/ MTIOC0D# (input/output)	PB0	○	○	○	○	○	○	○	○
	MTIOC1A (input/output)/ MTIOC1A# (input/output)	P27	×	○	×	×	○	○	×	×
		PA5	○	○	×	○	○	○	×	×
		P95	×	×	×	×	○	○	○	○
	MTIOC1B (input/output)/ MTIOC1B# (input/output)	PA4	○	×	×	×	○	×	×	×
	MTIOC2A (input/output)/ MTIOC2A# (input/output)	PA3	○	○	×	○	○	○	×	×
		P94	×	×	×	×	○	○	○	○
	MTIOC2B (input/output)/ MTIOC2B# (input/output)	PA2	○	×	×	×	○	×	×	×
	MTIOC3A (input/output)/ MTIOC3A# (input/output)	P11	○	○	○	○	○	○	○	○
		P33	○	×	×	×	○	×	×	×
	MTIOC3B (input/output)/ MTIOC3B# (input/output)	P71	○	○	○	○	○	○	○	○
	MTIOC3C (input/output)/ MTIOC3C# (input/output)	P32	○	×	×	×	○	×	×	×
	MTIOC3D (input/output)/ MTIOC3D# (input/output)	P74	○	○	○	○	○	○	○	○
	MTIOC4A (input/output)/ MTIOC4A# (input/output)	P72	○	○	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX66T (MPC)				RX26T (MPC)			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Multi-function timer unit 3	MTIOC4B (input/output)/ MTIOC4B# (input/output)	P73	○	○	○	○	○	○	○	○
	MTIOC4C (input/output)/ MTIOC4C# (input/output)	P75	○	○	○	○	○	○	○	○
	MTIOC4D (input/output)/ MTIOC4D# (input/output)	P76	○	○	○	○	○	○	○	○
	MTIC5U (input/output)/ MTIC5U# (input/output)	P24	○	×	×	×	○	×	×	×
		P82	○	×	×	×	○	×	×	×
	MTIC5V (input/output)/ MTIC5V# (input/output)	P23	○	×	×	×	○	×	×	×
		P81	○	×	×	×	○	×	×	×
	MTIC5W (input/output)/ MTIC5W# (input/output)	P22	○	○	○	×	○	○	○	×
		P80	○	×	×	×	○	×	×	×
	MTIOC6A (input/output)/ MTIOC6A# (input/output)	PA1	○	×	×	×	○	×	×	×
		P93	×	×	×	×	○	○	○	○
	MTIOC6B (input/output)/ MTIOC6B# (input/output)	P95	○	○	○	×	○	○	○	○
	MTIOC6C (input/output)/ MTIOC6C# (input/output)	PA0	○	×	×	×	○	×	×	×
		P92	×	×	×	×	○	○	○	○
	MTIOC6D (input/output)/ MTIOC6D# (input/output)	P92	○	○	○	×	○	○	○	○
	MTIOC7A (input/output)/ MTIOC7A# (input/output)	P94	○	○	○	○	○	○	○	○
	MTIOC7B (input/output)/ MTIOC7B# (input/output)	P93	○	○	○	×	○	○	○	○
	MTIOC7C (input/output)/ MTIOC7C# (input/output)	P91	○	○	○	×	○	○	○	○
	MTIOC7D (input/output)/ MTIOC7D# (input/output)	P90	○	○	○	×	○	○	○	×
	MTIOC9A (input/output)/ MTIOC9A# (input/output)	P00	○	○	○	○	○	○	○	○
		P21	○	○	○	×	○	○	○	○
		PD7	○	○	○	○	○	○	○	○
	MTIOC9B (input/output)	P22	○	○	○	×	○	○	○	×
	MTIOC9B (input/output)/ MTIOC9B# (input/output)	P10	○	○	×	○	○	○	×	○
		PE0	○	×	×	×	○	×	×	×
	MTIOC9C (input/output)/ MTIOC9C# (input/output)	P01	○	○	○	×	○	○	○	×
		P20	○	○	○	×	○	○	○	○
		PD6	○	○	○	×	○	○	○	×
	MTIOC9D (input/output)	P11	○	○	○	○	○	○	○	○
	MTIOC9D (input/output)/ MTIOC9D# (input/output)	PE1	○	×	×	×	○	×	×	×
		PE5	○	×	×	×	○	×	×	×
		PN7	×	×	×	×	○	○	○	×
	MTCLKA (input)/ MTCLKA# (input)	P21	○	○	○	×	○	○	○	○
		P33	○	×	×	×	○	×	×	×
	MTCLKB (input)/ MTCLKB# (input)	P20	○	○	○	×	○	○	○	○
		P32	○	×	×	×	○	×	×	×
	MTCLKC (input)/ MTCLKC# (input)	P11	○	○	○	○	○	○	○	○
		P31	○	○	×	×	○	○	×	×
		PE4	○	○	×	×	○	○	×	×
		P70	×	×	×	×	○	○	○	×

Module/ Function	Pin Function	Port Allocation	RX66T (MPC)				RX26T (MPC)			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Multi-function timer unit 3	MTCLKC (input)/ MTCLKC# (input)	P10	○	○	×	○	○	○	×	○
		P22	○	○	○	×	○	○	○	×
		P30	○	○	×	×	○	○	×	×
		PE3	○	○	×	×	○	○	×	×
	ADSM0 (output)	PB2	○	○	○	○	○	○	○	○
	ADSM1 (output)	PB1	○	○	○	○	○	○	○	○
General purpose PWM timer	GTIOC0A (input/output)/ GTIOC0A# (input/output)	P71	○	○	○	○	○	○	○	○
		PD2	○	○	×	×	○	○	×	×
		PD7	○	○	○	○	○	○	○	○
	GTIOC0B (input/output)/ GTIOC0B# (input/output)	P74	○	○	○	○	○	○	○	○
		PD1	○	×	×	×	○	×	×	×
		PD6	○	○	○	×	○	○	○	×
	GTIOC1A (input/output)/ GTIOC1A# (input/output)	P72	○	○	○	○	○	○	○	○
		PD0	○	×	×	×	○	×	×	×
		PD5	○	○	○	○	○	○	○	○
	GTIOC1B (input/output)/ GTIOC1B# (input/output)	P75	○	○	○	○	○	○	○	○
		PB7	○	×	×	×	○	×	×	×
		PD4	○	○	○	×	○	○	○	×
	GTIOC2A (input/output)/ GTIOC2A# (input/output)	P73	○	○	○	○	○	○	○	○
		PB6	○	○	○	○	○	○	○	○
		PD3	○	○	○	○	○	○	○	○
	GTIOC2B (input/output)/ GTIOC2B# (input/output)	P76	○	○	○	○	○	○	○	○
		PB5	○	○	○	○	○	○	○	○
		PD2	○	○	×	×	○	○	×	×
	GTIOC3A (input/output)/ GTIOC3A# (input/output)	P32	○	×	×	×	○	×	×	×
		PD1	○	×	×	×	○	×	×	×
		PD7	○	○	○	○	○	○	○	○
		PE5	○	×	×	×	○	×	×	×
		P10	×	×	×	×	○	○	×	○
		PB6	×	×	×	×	○	○	○	○
	GTIOC3B (input/output)/ GTIOC3B# (input/output)	P11	○	○	○	○	○	○	○	○
		P33	○	×	×	×	○	×	×	×
		PD0	○	×	×	×	○	×	×	×
		PD6	○	○	○	×	○	○	○	×
		PB5	×	×	×	×	○	○	○	○
	GTIOC4A (input/output)/ GTIOC4A# (input/output)	P71	○	○	○	○	○	○	○	○
		P95	○	○	○	×	○	○	○	○
	GTIOC4B (input/output)/ GTIOC4B# (input/output)	P74	○	○	○	○	○	○	○	○
		P92	○	○	○	×	○	○	○	○
	GTIOC5A (input/output)/ GTIOC5A# (input/output)	P72	○	○	○	○	○	○	○	○
		P94	○	○	○	○	○	○	○	○
	GTIOC5B (input/output)/ GTIOC5B# (input/output)	P75	○	○	○	○	○	○	○	○
		P91	○	○	○	×	○	○	○	○
	GTIOC6A (input/output)/ GTIOC6A# (input/output)	P73	○	○	○	○	○	○	○	○
		P93	○	○	○	×	○	○	○	○
	GTIOC6B (input/output)/ GTIOC6B# (input/output)	P76	○	○	○	○	○	○	○	○
		P90	○	○	○	×	○	○	○	×

Module/ Function	Pin Function	Port Allocation	RX66T (MPC)				RX26T (MPC)			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
General purpose PWM timer	GTIOC7A (input/output)/ GTIOC7A# (input/output)	P95	○	○	○	×	○	○	○	○
		P32	×	×	×	×	○	×	×	×
		PB2	×	×	×	×	○	○	○	○
	GTIOC7B (input/output)/ GTIOC7B# (input/output)	P92	○	○	○	×	○	○	○	○
		P33	×	×	×	×	○	×	×	×
		PB1	×	×	×	×	○	○	○	○
	GTIOC8A (input/output)/ GTIOC8A# (input/output)	P94	○	○	○	○				
	GTIOC8B (input/output)/ GTIOC8B# (input/output)	P91	○	○	○	×				
	GTIOC9A (input/output)/ GTIOC9A# (input/output)	P93	○	○	○	×				
	GTIOC9B (input/output)/ GTIOC9B# (input/output)	P90	○	○	○	×				
	GTETRGA (input)	P01	○	○	○	×	○	○	○	×
		P11	○	○	○	○	○	○	○	○
		P70	○	○	○	×	○	○	○	×
		P96	○	○	○	×	○	○	○	×
		PB4	○	○	○	○	○	○	○	○
		PD5	○	○	○	○	○	○	○	○
		PE3	○	○	×	×	○	○	×	×
		PE4	○	○	×	×	○	○	×	×
	GTETRGB (input)	P01	○	○	○	×	○	○	○	×
		P10	○	○	×	○	○	○	×	○
		P70	○	○	○	×	○	○	○	×
		P96	○	○	○	×	○	○	○	×
		PB4	○	○	○	○	○	○	○	○
		PD4	○	○	○	×	○	○	○	×
		PE3	○	○	×	×	○	○	×	×
		PE4	○	○	×	×	○	○	×	×
		PE5	○	×	×	×	○	×	×	×
	GTETRGC (input)	P01	○	○	○	×	○	○	○	×
		P11	○	○	○	○	○	○	○	○
		P70	○	○	○	×	○	○	○	×
		P96	○	○	○	×	○	○	○	×
		PB4	○	○	○	○	○	○	○	○
		PD3	○	○	○	○	○	○	○	○
		PE3	○	○	×	×	○	○	×	×
		PE4	○	○	×	×	○	○	×	×
	GTETRGD (input)	P01	○	○	○	×	○	○	○	×
		P10	○	○	×	○	○	○	×	○
		P70	○	○	○	×	○	○	○	×
		P96	○	○	○	×	○	○	○	×
		PB4	○	○	○	○	○	○	○	○
		PE3	○	○	×	×	○	○	×	×
		PE4	○	○	×	×	○	○	×	×
		PE5	○	×	×	×	○	×	×	×

Module/ Function	Pin Function	Port Allocation	RX66T (MPC)				RX26T (MPC)			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
General purpose PWM timer	GTADSM0 (output)	PA3	○	○	×	○	○	○	×	×
		PB2	○	○	○	○	○	○	○	○
		P94	×	×	×	×	○	○	○	○
	GTADSM1 (output)	PA2	○	×	×	×	○	×	×	×
		PB1	○	○	○	○	○	○	○	○
Port output enable 3	POE0# (input)	P70	○	○	○	×	○	○	○	×
	POE4# (input)	P96	○	○	○	×	○	○	○	×
	POE8# (input)	PB4	○	○	○	○	○	○	○	○
	POE9# (input)	P11	○	○	○	○	○	○	○	○
		P27	×	○	×	×	○	○	×	×
	POE10# (input)	PE2	○	○	○	○	○	○	○	○
		PE4	○	○	×	×	○	○	×	×
	POE11# (input)	PE3	○	○	×	×	○	○	×	×
	POE12# (input)	P01	○	○	○	×	○	○	○	×
		P10	○	○	×	○	○	○	×	○
8-bit timer	TMO0 (output)	P33	○	×	×	×	○	×	×	×
		PB0	○	○	○	○	○	○	○	○
		PD3	○	○	○	○	○	○	○	○
	TMCI0 (input)	PB1	○	○	○	○	○	○	○	○
		PD4	○	○	○	×	○	○	○	×
	TMRI0 (input)	PB2	○	○	○	○	○	○	○	○
		PD5	○	○	○	○	○	○	○	○
	TMO1 (output)	PD6	○	○	○	×	○	○	○	×
	TMCI1 (input)	PD2	○	○	×	×	○	○	×	×
		PE0	○	×	×	×	○	×	×	×
	TMRI1 (input)	PD7	○	○	○	○	○	○	○	○
	TMO2 (output)	P23	○	×	×	×	○	×	×	×
		PA0	○	×	×	×	○	×	×	×
		PD1	○	×	×	×	○	×	×	×
		P20	×	×	×	×	○	○	○	○
		P27	×	×	×	×	○	○	×	×
		P92	×	×	×	×	○	○	○	○
	TMCI2 (input)	P24	○	×	×	×	○	×	×	×
	TMRI2 (input)	P22	○	○	○	×	○	○	○	×
	TMO3 (output)	P11	○	○	○	○	○	○	○	○
	TMCI3 (input)	PA5	○	○	×	○	○	○	×	×
		P95	×	×	×	×	○	○	○	○
	TMRI3 (input)	P10	○	○	×	○	○	○	×	○
	TMO4 (output)	P22	○	○	○	×	○	○	○	×
		P82	○	×	×	×	○	×	×	×
		PA1	○	×	×	×	○	×	×	×
		PD2	○	○	×	×	○	○	×	×
		P93	×	×	×	×	○	○	○	○
	TMCI4 (input)	P21	○	○	○	×	○	○	○	○
		P81	○	×	×	×	○	×	×	×
	TMRI4 (input)	P20	○	○	○	×	○	○	○	○
		P80	○	×	×	×	○	×	×	×
	TMO5 (output)	PE1	○	×	×	×	○	×	×	×
	TMCI5 (input)	PE0	○	×	×	×	○	×	×	×

Module/ Function	Pin Function	Port Allocation	RX66T (MPC)				RX26T (MPC)			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
8-bit timer	TMRI5 (input)	PD7	○	○	○	○	○	○	○	○
	TMO6 (output)	P24	○	×	×	×	○	×	×	×
		P32	○	×	×	×	○	×	×	×
		PD0	○	×	×	×	○	×	×	×
		P21	×	×	×	×	○	○	○	○
		P27	×	×	×	×	○	○	×	×
	TMCI6 (input)	P30	○	○	×	×	○	○	×	×
		PD4	○	○	○	×	○	○	○	×
	TMRI6 (input)	P31	○	○	×	×	○	○	×	×
		PD5	○	○	○	○	○	○	○	○
		P70	×	×	×	×	○	○	○	×
	TMO7 (output)	PA2	○	×	×	×	○	×	×	×
	TMCI7 (input)	PA4	○	×	×	×	○	×	×	×
	TMRI7 (input)	PA3	○	○	×	○	○	○	×	×
		P94	×	×	×	×	○	○	○	○
Serial communications interface	RXD1 (input)/ SMISO1 (input/output)/ SSCL1 (input/output)	PD5	○	○	○	○	○	○	○	○
	TXD1 (output)/ SMOSI1 (input/output)/ SSDA1 (input/output)	PD3	○	○	○	○	○	○	○	○
	SCK1 (input/output)	PD4	○	○	○	×	○	○	○	×
	CTS1# (input)/ RTS1# (output)/ SS1# (input)	PD6	○	○	○	×	○	○	○	×
	RXD5 (input)/ SMISO5 (input/output)/ SSCL5 (input/output)	PB6	○	○	○	○	○	○	○	○
		PE0	○	×	×	×	○	×	×	×
		P37	×	×	×	×	○	○	○	○
		P91	×	×	×	×	○	○	○	○
	TXD5 (output)/ SMOSI5 (input/output)/ SSDA5 (input/output)	PB5	○	○	○	○	○	○	○	○
		PD7	○	○	○	○	○	○	○	○
		P36	×	×	×	×	○	○	○	○
		P90	×	×	×	×	○	○	○	×
	SCK5 (input/output)	PB7	○	×	×	×	○	×	×	×
		PD2	○	○	×	×	○	○	×	×
		P70	×	×	×	×	○	○	○	×
	CTS5# (input)/ RTS5# (output)/ SS5# (input)	PB4	○	○	○	○	○	○	○	○
		PE1	○	×	×	×	○	×	×	×
	RXD6 (input)/ SMISO6 (input/output)/ SSCL6 (input/output)	P80	○	×	×	×	○	×	×	×
		PA5	○	○	×	○	○	○	×	×
		PB1	○	○	○	○	○	○	○	○
		P95	×	×	×	×	○	○	○	○
	TXD6 (output)/ SMOSI6 (input/output)/ SSDA6 (input/output)	P81	○	×	×	×	○	×	×	×
		PB0	○	○	○	○	○	○	○	○
		PB2	○	○	○	○	○	○	○	○
	SCK6 (input/output)	P82	○	×	×	×	○	×	×	×
		PA4	○	×	×	×	○	×	×	×
		PB3	○	○	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX66T (MPC)				RX26T (MPC)			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial communications interface	CTS6# (input)/ RTS6# (output)/ SS6# (input)	P10	○	○	×	○	○	○	×	○
		PA2	○	×	×	×	○	×	×	×
	RXD8 (input)/ SMISO8 (input/output)/ SSCL8 (input/output)	P22	○	○	○	×				
		PA5	○	○	×	×				
		PD1	○	×	×	×				
	TXD8 (output)/ SMOSI8 (input/output)/ SSDA8 (input/output)	P21	○	○	○	×				
		P23	○	×	×	×				
		PA4	○	×	×	×				
		PD0	○	×	×	×				
	SCK8 (input/output)	P20	○	○	○	×				
		P24	○	×	×	×				
		P30	○	○	×	×				
		PA3	○	○	×	×				
		PD2	○	○	×	×				
	CTS8# (input)/ RTS8# (output)/ SS8# (input)	P20	○	○	○	×				
		P24	○	×	×	×				
		P30	○	○	×	×				
		P96	○	○	○	×				
	RXD9 (input)/ SMISO9 (input/output)/ SSCL9 (input/output)	P00	○	○	○	○				
		PA2	○	×	×	×				
	TXD9 (output)/ SMOSI9 (input/output)/ SSDA9 (input/output)	P01	○	○	○	×				
		PA1	○	×	×	×				
		PA3	○	○	×	○				
	SCK9 (input/output)	PA0	○	×	×	×				
		PE4	○	○	×	×				
		PE5	○	×	×	×				
	CTS9# (input)/ RTS9# (output)/ SS9# (input)	P70	○	○	○	×				
		PE3	○	○	×	×				
		PE5	○	×	×	×				
	RXD11 (input)/ SMISO11 (input/output)/ SSCL11 (input/output)	PA1	○	×	×	×				
		PB6	○	○	○	○				
		PD5	○	○	○	○				
	TXD11 (output)/ SMOSI11 (input/output)/ SSDA11 (input/output)	PA0	○	×	×	×				
		PB5	○	○	○	○				
		PD3	○	○	○	○				
	SCK11 (input/output)	PA2	○ *1	×	×	×				
		PB4	○	○	○	○				
		PB7	○	×	×	×				
		PD4	○	○	○	×				
	CTS11# (input)/ RTS11# (output)/ SS11# (input)	PB0	○	○	○	○				
		PB4	○	○	○	○				
		PD6	○	○	○	×				

Module/ Function	Pin Function	Port Allocation	RX66T (MPC)				RX26T (MPC)			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial communications interface	RXD12 (input)/ SMISO12 (input/output)/ SSCL12 (input/output)/ RXDX12 (input)	P00	○	○	○	○	○	○	○	○
		P22	○	○	○	×	○	○	○	×
		P80	○	×	×	×	○	×	×	×
		PB6	○	○	○	○	○	○	○	○
		PB4	×	×	×	×	○	○	○	○
		PD6	×	×	×	×	○	○	○	×
	TXD12 (output)/ SMOSI12 (input/output)/ SSDA12 (input/output)/ TXDX12 (output)/ SIOX12 (input/output)	P01	○	○	○	×	○	○	○	×
		P21	○	○	○	×	○	○	○	○
		P23	○	×	×	×	○	×	×	×
		P81	○	×	×	×	○	×	×	×
		PB5	○	○	○	○	○	○	○	○
		PB3	×	×	×	×	○	○	○	○
		PD4	×	×	×	×	○	○	○	×
	SCK12 (input/output)	P82	○	×	×	×	○	×	×	×
		PB7	○	×	×	×	○	×	×	×
	CTS12# (input)/ RTS12# (output)/ SS12# (input)	PE1	○	×	×	×	○	×	×	×
I^2C bus interface	SCL0 (input/output)	PB1	○	○	○	○	○	○	○	○
	SDA0 (input/output)	PB2	○	○	○	○	○	○	○	○
CAN module	CTX0 (output)	P23	○	×	×	×				
		PA0	○	×	×	×				
		PB5	○	○	○	○				
		PD7	○	○	○	○				
	CRX0 (input)	P22	○	○	○	×				
		PA1	○	×	×	×				
		PB6	○	○	○	○				
		PE0	○	×	×	×				
Serial peripheral interface	RSPCKA (input/output)	P20	○	○	○	×	○	○	○	○
		P24	○	×	×	×	○	×	×	×
		PA4	○	×	×	×	○	×	×	×
		PB3	○	○	○	○	○	○	○	○
		PD0	○	×	×	×	○	×	×	×
		P27	×	×	×	×	○	○	×	×
	MOSIA (input/output)	P21	○	○	○	×	○	○	○	○
		P23	○	×	×	×	○	×	×	×
		PB0	○	○	○	○	○	○	○	○
		PD2	○	○	×	×	○	○	×	×
	MISOA (input/output)	P22	○	○	○	×	○	○	○	×
		PA5	○	○	×	○	○	○	×	×
		PD1	○	×	×	×	○	×	×	×
		P95	×	×	×	×	○	○	○	○
		PB4	×	×	×	×	○	○	○	○
	SSLA0 (input/output)	P30	○	○	×	×	○	○	×	×
		PA3	○	○	×	○	○	○	×	×
		PD6	○	○	○	×	○	○	○	×
		P70	×	×	×	×	○	○	○	×
		P94	×	×	×	×	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX66T (MPC)				RX26T (MPC)			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial peripheral interface	SSLA1 (output)	P31	○	○	×	×	○	○	×	×
		PA2	○	×	×	×	○	×	×	×
		PD7	○	○	○	○	○	○	○	○
	SSLA2 (output)	P32	○	×	×	×	○	×	×	×
		PA1	○	×	×	×	○	×	×	×
		PE0	○	×	×	×	○	×	×	×
		P93	×	×	×	×	○	○	○	○
	SSLA3 (output)	P33	○	×	×	×	○	×	×	×
		PA0	○	×	×	×	○	×	×	×
		PE1	○	×	×	×	○	×	×	×
		P92	×	×	×	×	○	○	○	○
12-bit A/D converter	AN000 (input)	P40	○	○	○	○	○	○	○	○
	AN001 (input)	P41	○	○	○	○	○	○	○	○
	AN002 (input)	P42	○	○	○	○	○	○	○	○
	AN003 (input)	P43	○	○	×	○	○	○	○	○
	AN007 (input)	PH0	×	○	○	×				
	ADTRG0# (input)	P20	○	○	○	×	○	○	○	○
		PA1	○	×	×	×	○	×	×	×
		PA4	○	×	×	×	○	×	×	×
		P93	×	×	×	×	○	○	○	○
	ADST0 (output)	PD6	○	○	○	×	○	○	○	×
		PE5	○	×	×	×	○	×	×	×
		PN7	×	×	×	×	○	○	○	×
	PGAVSS0 (input)	PH0	×	○	○	×				
	AN100 (input)	P44	○	○	○	○	○	○	○	○
	AN101 (input)	P45	○	○	○	×	○	○	○	×
	AN102 (input)	P46	○	○	○	×	○	○	○	×
	AN103 (input)	P47	○	○	×	×	○	○	○	×
	AN107 (input)	PH4	×	○	○	×				
	ADTRG1# (input)	P21	○	○	○	×	○	○	○	○
		PA5	○	○	×	○	○	○	×	×
		P95	×	×	×	×	○	○	○	○
	ADST1 (output)	P00	○	○	○	○	○	○	○	○
	PGAVSS1 (input)	PH4	×	○	○	×				
	AN200 (input)	P52	○	○	○	×	○	○	○	○
	AN201 (input)	P53	○	○	○	×	○	○	○	○
	AN202 (input)	P54	○	○	○	×	○	○	○	×
	AN203 (input)	P55	○	○	×	×	○	○	×	×
	AN204 (input)	P50	○	×	×	×	○	○	×	×
	AN205 (input)	P51	○	×	×	×	○	○	×	×
	AN206 (input)	P60	○	×	×	×	○	○	×	×
	AN207 (input)	P61	○	×	×	×	○	×	×	×
	AN208 (input)	P62	○	○	×	○	○	×	×	○
	AN209 (input)	P63	○	×	×	×	○	×	×	×
	AN210 (input)	P64	○	○	○	○	○	○	○	×
	AN211 (input)	P65	○	○	○	○	○	○	○	×
	AN216 (input)	P20	○	○	○	×	○	○	○	○
	AN217 (input)	P21	○	○	○	×	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX66T (MPC)				RX26T (MPC)			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
12-bit A/D converter	ADTRG2# (input)	P22	○	○	○	×	○	○	○	×
		PB0	○	○	○	○	○	○	○	○
	ADST2 (output)	P01	○	○	○	×	○	○	○	×
12-bit D/A converter	DA0 (output)	P64	○	○	○	○	○	○	○	×
	DA1 (output)	P65	○	○	○	○	○	○	○	×
Clock frequency accuracy measurement circuit	CACREF (input)	P00	○	○	○	○	○	○	○	○
		P23	○	×	×	×	○	×	×	×
		PB3	○	○	○	○	○	○	○	○
Comparator	COMP0 (output)	P00	○	○	○	○	○	○	○	○
		P24	○	×	×	×	○	×	×	×
	COMP1 (output)	P01	○	○	○	×	○	○	○	×
		P23	○	×	×	×	○	×	×	×
	COMP2 (output)	P22	○	○	○	×	○	○	○	×
	COMP3 (output)	P30	○	○	×	×	○	○	×	×
		P80	○	×	×	×	○	×	×	×
	COMP4 (output)	P20	○	○	○	×	○	○	○	○
		P81	○	×	×	×	○	×	×	×
	COMP5 (output)	P21	○	○	○	×	○	○	○	○
		P82	○	×	×	×	○	×	×	×
	CVREFC0 (input)	P53	×	×	×	×	○	○	○	○
	CVREFC1 (input)	P54	×	×	×	×	○	○	○	×
	CMPC00 (input)	P40	○	○	○	○	○	○	○	○
	CMPC01 (input)	P40	○	○	○	○	○	○	○	○
	CMPC02 (input)	P52	○	○	○	×	○	○	○	○
	CMPC03 (input)	P60	○	×	×	×	○	○	×	×
	CMPC10 (input)	P41	○	○	○	○	○	○	○	○
	CMPC11 (input)	P41	○	○	○	○	○	○	○	○
	CMPC12 (input)	P53	○	○	○	×	○	○	○	○
	CMPC13 (input)	P61	○	×	×	×	○	×	×	×
	CMPC20 (input)	P42	○	○	○	○	○	○	○	○
	CMPC21 (input)	P42	○	○	○	○	○	○	○	○
	CMPC22 (input)	P54	○	○	○	×	○	○	○	×
	CMPC23 (input)	P63	○	×	×	×	○	×	×	×
	CMPC30 (input)	P44	○	○	○	○	○	○	○	○
	CMPC31 (input)	P44	○	○	○	○	○	○	○	○
	CMPC32 (input)	P55	○	○	×	×	○	○	×	×
	CMPC33 (input)	P64	○	○	○	○	○	○	○	×
	CMPC40 (input)	P45	○	○	○	×	○	○	○	×
	CMPC41 (input)	P45	○	○	○	×	○	○	○	×
	CMPC42 (input)	P50	○	×	×	×	○	○	×	×
	CMPC43 (input)	P62	○	○	×	○	○	×	×	○
	CMPC50 (input)	P46	○	○	○	×	○	○	○	×
	CMPC51 (input)	P46	○	○	○	×	○	○	○	×
	CMPC52 (input)	P51	○	×	×	×	○	○	×	×
	CMPC53 (input)	P65	○	○	○	○	○	○	○	×

Module/ Function	Pin Function	Port Allocation	RX66T (MPC)				RX26T (MPC)			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
General purpose PWM timer	GTIOC7A (input/output)	PD5					○	○	○	○
	GTIOC7B (input/output)	PD3					○	○	○	○
	GTCPPO0 (output)	P11					○	○	○	○
		P33					○	×	×	×
		P70					○	○	○	×
		PB4					○	○	○	○
	GTCPPO4 (output)	P96					○	○	○	×
		PA1					○	×	×	×
	GTIU (input)	P00					○	○	○	○
		P21					○	○	○	○
		P31					○	○	×	×
		PB3					○	○	○	○
		PD7					○	○	○	○
	GTIV (input)	P10					○	○	×	○
		P22					○	○	○	×
		P30					○	○	×	×
		PB2					○	○	○	○
		PE0					○	×	×	×
	GTIW (input)	P01					○	○	○	×
		P20					○	○	○	○
		PB1					○	○	○	○
		PD6					○	○	○	×
	GTOULO (output)	P74					○	○	○	○
		P92					○	○	○	○
	GTOUUP (output)	P71					○	○	○	○
		P95					○	○	○	○
	GTOVLO (output)	P75					○	○	○	○
		P91					○	○	○	○
	GTOVUP (output)	P72					○	○	○	○
		P94					○	○	○	○
	GTOWLO (output)	P76					○	○	○	○
		P90					○	○	○	×
	GTOWUP (output)	P73					○	○	○	○
		P93					○	○	○	○
Compare match timer W	TOC0 (output)	PB6					○	○	○	○
	TIC0 (input)	PB5					○	○	○	○
	TOC1 (output)	PB3					○	○	○	○
	TIC1 (input)	PB2					○	○	○	○
	TOC2 (output)	PB1					○	○	○	○
	TIC2 (input)	PB0					○	○	○	○
	TOC3 (output)	P11					○	○	○	○
	TIC3 (input)	P00					○	○	○	○
		P10					○	○	×	○
Serial communications interface	RXD008 (input)/ SMISO008 (input/output)/ SSCL008 (input/output)	P20					○	○	○	○
		P22					○	○	○	×
		P95					○	○	○	○
		PA5					○	○	×	×
		PD1					○	×	×	×

Module/ Function	Pin Function	Port Allocation	RX66T (MPC)				RX26T (MPC)			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial communications interface	TXD008 (output)/ TXDA008 (output)/ SMOSI008 (input/output)/ SSDA008 (input/output)	P21					○	○	○	○
		P23					○	×	×	×
		PA4					○	×	×	×
		PB0					○	○	○	○
		PD0					○	×	×	×
		PD7					○	○	○	○
	SCK008 (input/output)	P11					○	○	○	○
		P22					○	○	○	×
		P24					○	×	×	×
		P30					○	○	×	×
		P94					○	○	○	○
		PA3					○	○	×	×
		PD2					○	○	×	×
	TXDB008 (output)	P22					○	○	○	×
		P94					○	○	○	○
		PA3					○	○	×	×
		PD2					○	○	×	×
	CTS008# (input)/ RTS008# (output)/ SS008# (input)	P20					○	○	○	○
		P24					○	×	×	×
		P30					○	○	×	×
		P96					○	○	○	×
	DE008 (output)	P20					○	○	○	○
		P24					○	×	×	×
		P30					○	○	×	×
		P96					○	○	○	×
	RXD009 (input)/ SMISO009 (input/output)/ SSCL009 (input/output)	P00					○	○	○	○
		PA2					○	×	×	×
	TXD009 (output)/ TXDA009 (output)/ SMOSI009 (input/output)/ SSDA009 (input/output)	P01					○	○	○	×
		P10					○	○	×	○
		P93					○	○	○	○
		P94					○	○	○	○
		PA1					○	×	×	×
		PA3					○	○	×	×
	SCK009 (input/output)	P11					○	○	○	○
		P92					○	○	○	○
		PA0					○	×	×	×
		PD7					○	○	○	○
		PE4					○	○	×	×
		PE5					○	×	×	×
	TXDB009 (output)	P11					○	○	○	○
		P92					○	○	○	○
		PA0					○	×	×	×
		PD7					○	○	○	○
		PE4					○	○	×	×
		PE5					○	×	×	×

Module/ Function	Pin Function	Port Allocation	RX66T (MPC)				RX26T (MPC)			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial communications interface	CTS009# (input)/ RTS009# (output)/ SS009# (input)	P70					○	○	○	×
		PB3					○	○	○	○
		PE3					○	○	×	×
		PE5					○	×	×	×
	DE009 (output)	P70					○	○	○	×
		PB3					○	○	○	○
		PE3					○	○	×	×
	RXD011 (input)/ SMISO011 (input/output)/ SSCL011 (input/output)	P93					○	○	○	○
		PA1					○	×	×	×
		PB6					○	○	○	○
		PD5					○	○	○	○
	TXD011 (output)/ TXDA011 (output)/ SMOSI011 (input/output)/ SSDA011 (input/output)	P92					○	○	○	○
		PA0					○	×	×	×
		PB5					○	○	○	○
		PD3					○	○	○	○
	SCK011 (input/output)	PB4					○	○	○	○
		PB7					○	×	×	×
		PD4					○	○	○	×
	TXDB011 (output)	PB4					○	○	○	○
		PB7					○	×	×	×
		PD4					○	○	○	×
	CTS011# (input)/ RTS011# (output)/ SS011# (input)	PB0					○	○	○	○
		PB4					○	○	○	○
		PD6					○	○	○	×
	DE011 (output)	PB0					○	○	○	○
		PD6					○	○	○	×
I^3C bus interface	SCL00 (input/output)	PB1					○	○	○	○
	SDA00 (input/output)	PB2					○	○	○	○
CAN FD module	CTX0 (output)	P23					○	×	×	×
		PA0					○	×	×	×
		PB5					○	○	○	○
		PD7					○	○	○	○
		P92					○	○	○	○
		PB3					○	○	○	○
	CRX0 (input)	P22					○	○	○	×
		PA1					○	×	×	×
		PB6					○	○	○	○
		PE0					○	×	×	×
		P93					○	○	○	○
		PB4					○	○	○	○
Serial peripheral interface	RSPCK0 (input/output)	P20					○	○	○	○
		P24					○	×	×	×
		P27					○	○	×	×
		P70					○	○	○	×
		P91					○	○	○	○
		P96					○	○	○	×
		PA4					○	×	×	×
		PB5					○	○	○	○
		PD0					○	×	×	×

Module/ Function	Pin Function	Port Allocation	RX66T (MPC)				RX26T (MPC)			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial peripheral interface	MOSI0 (input/output)	P21					○	○	○	○
		P23					○	×	×	×
		P72					○	○	○	○
		P93					○	○	○	○
		PB0					○	○	○	○
		PD2					○	○	×	×
		PD3					○	○	○	○
	MISO0 (input/output)	P22					○	○	○	×
		P71					○	○	○	○
		P92					○	○	○	○
		P95					○	○	○	○
		PA5					○	○	×	×
		PB6					○	○	○	○
		PD1					○	×	×	×
	SSL00 (input/output)	P30					○	○	×	×
		P73					○	○	○	○
		P94					○	○	○	○
		PA3					○	○	×	×
		PD5					○	○	○	○
		PD6					○	○	○	×
	SSL01 (output)	P31					○	○	×	×
		P74					○	○	○	○
		P90					○	○	○	×
		PA2					○	×	×	×
		PB4					○	○	○	○
		PD7					○	○	○	○
	SSL02 (output)	P32					○	×	×	×
		P75					○	○	○	○
		P93					○	○	○	○
		P95					○	○	○	○
		PA1					○	×	×	×
		PD4					○	○	○	×
		PE0					○	×	×	×
	SSL03 (output)	P33					○	×	×	×
		P76					○	○	○	○
		P92					○	○	○	○
		P96					○	○	○	×
		PA0					○	×	×	×
		PB7					○	×	×	×
		PE1					○	×	×	×

Note: 1. This pin is provided only on products with a RAM capacity of 128 KB.

Table 2.32 Comparison of P0n Pin Function Control Registers (P0nPFS)

Register	Bit	RX66T (n = 0, 1)	RX26T (n = 0, 1)
P00PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9A 000011b: MTIOC9A# 000111b: CACREF 001001b: ADST1 001010b: RXD9/SMISO9/SSCL9 001100b: RXD12/SMISO12/SSCL12/ RXDX12 011110b: COMP0	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9A 000011b: MTIOC9A# 000111b: CACREF 001001b: ADST1 001100b: RXD12/SMISO12/SSCL12/ RXDX12 011000b: GTIU 011101b: TIC3 011110b: COMP0 101100b: RXD009/SMISO009/ SSCL009
P01PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9C 000011b: MTIOC9C# 000111b: POE12# 001001b: ADST2 001010b: TXD9/SMOSI9/SSDA9 001100b: TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD 011110b: COMP1	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9C 000011b: MTIOC9C# 000111b: POE12# 001001b: ADST2 001100b: TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD 011000b: GTIW 011110b: COMP1 101100b: TXD009/TXDA009/ SMOSI009/SSDA009
P0nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P00: IRQ2 (48/64/80/100/112/144-pin) P01: IRQ4 (64/80/100/112/144-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P00: IRQ2 (48/64/80/100-pin) P01: IRQ4 (64/80/100-pin)

Table 2.33 Comparison of P1n Pin Function Control Registers (P1nPFS)

Register	Bit	RX66T (n = 0 to 7)	RX26T (n = 0, 1)
P10PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9B 000010b: MTCLKD 000011b: MTIOC9B# 000100b: MTCLKD# 000101b: TMRI3 000111b: POE12# 001010b: CTS6#/RTS6#/SS6# 010101b: GTETRGB 010111b: GTETRGD	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9B 000010b: MTCLKD 000011b: MTIOC9B# 000100b: MTCLKD# 000101b: TMRI3 000111b: POE12# 001010b: CTS6#/RTS6#/SS6# 010100b: GTIOC3A 010101b: GTETRGB 010110b: GTIOC3A# 010111b: GTETRGD 011000b: GTIV 011101b: TIC3 101100b: TXD009/TXDA009/ SMOSI009/SSDA009
P11PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKC 000011b: MTIOC3A# 000100b: MTCLKC# 000101b: TMO3 000111b: POE9# 001000b: MTIOC9D 010100b: GTIOC3B 010101b: GTETRGA 010110b: GTIOC3B# 010111b: GTETRGC	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKC 000011b: MTIOC3A# 000100b: MTCLKC# 000101b: TMO3 000111b: POE9# 001000b: MTIOC9D 010100b: GTIOC3B 010101b: GTETRGA 010110b: GTIOC3B# 010111b: GTETRGC 011000b: GTCPPO0 011101b: TOC3 101100b: SCK009 101101b: SCK008 101110b: TXDB009
P12PFS	—	P12 pin function select register	—
P13PFS	—	P13 pin function select register	—
P14PFS	—	P14 pin function select register	—
P15PFS	—	P15 pin function select register	—
P16PFS	—	P16 pin function select register	—
P17PFS	—	P17 pin function select register	—

Register	Bit	RX66T (n = 0 to 7)	RX26T (n = 0, 1)
P1nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P10: IRQ0-DS (48/80/100/112/144-pin) P11: IRQ1-DS (48/64/80/100/112/144-pin) P12: IRQ9 (112/144-pin) P13: IRQ10 (112/144-pin) P14: IRQ11 (112/144-pin) P15: IRQ12 (112/144-pin) P16: IRQ13 (112/144-pin) P17: IRQ14 (112/144-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P10: IRQ0 (48/80/100-pin) P11: IRQ1 (48/64/80/100-pin)

Table 2.34 Comparison of P2n Pin Function Control Registers (P2nPFS)

Register	Bit	RX66T (n = 0 to 7)	RX26T (n = 0 to 4, 7)
P20PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9C 000010b: MTCLKB 000011b: MTIOC9C# 000100b: MTCLKB# 000101b: TMRI4 001001b: ADTRG0# 001010b: CTS8#/RTS8#/SS8# 001011b: SCK8 001101b: RSPCKA 011110b: COMP4	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9C 000010b: MTCLKB 000011b: MTIOC9C# 000100b: MTCLKB# 000101b: TMRI4 000110b: TMO2 001001b: ADTRG0# 001101b: RSPCKA 001110b: RSPCK0 011000b: GTIW 011110b: COMP4 101100b: CTS008#/RTS008#/ SS008# 101101b: RXD008/SMISO008/ SSCL008 101110b: DE008
P21PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9A 000010b: MTCLKA 000011b: MTIOC9A# 000100b: MTCLKA# 000101b: TMCI4 001001b: ADTRG1# 001010b: TXD8/SMOSI8/SSDA8 001100b: TXD12/SMISO12/SSDA12/ TXDX12/SIOX12 001101b: MOSIA 011110b: COMP5	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9A 000010b: MTCLKA 000011b: MTIOC9A# 000100b: MTCLKA# 000101b: TMCI4 000110b: TMO6 001001b: ADTRG1# 001100b: TXD12/SMISO12/SSDA12/ TXDX12/SIOX12 001101b: MOSIA 001110b: MOSI0 011000b: GTIU 011110b: COMP5 101100b: TXD008/TXDA008/ SMOSI008/SSDA008

Register	Bit	RX66T (n = 0 to 7)	RX26T (n = 0 to 4, 7)
P22PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIC5W 000010b: MTCLKD 000011b: MTIC5W# 000100b: MTCLKD# 000101b: TMRI2 000110b: TMO4 001000b: MTIOC9B 001001b: ADTRG2# 001010b: RXD8/SMISO8/SSCL8 001100b: RXD12/SMISO12/SSCL12/ RXDX12 001101b: MISOA 010000b: CRX0 011110b: COMP2	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIC5W 000010b: MTCLKD 000011b: MTIC5W# 000100b: MTCLKD# 000101b: TMRI2 000110b: TMO4 001000b: MTIOC9B 001001b: ADTRG2# 001100b: RXD12/SMISO12/SSCL12/ RXDX12 001101b: MISOA 001110b: MISO0 010000b: CRX0 011000b: GTIV 011110b: COMP2 101100b: RXD008/SMISO008/ SSCL008 101101b: SCK008 101110b: TXDB008
P23PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIC5V 000011b: MTIC5V# 000101b: TMO2 000111b: CACREF 001010b: TXD8/SMOSI8/SSDA8 001100b: TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12 001101b: MOSIA 010000b: CTX0 011110b: COMP1	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIC5V 000011b: MTIC5V# 000101b: TMO2 000111b: CACREF 001100b: TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12 001101b: MOSIA 001110b: MOSI0 010000b: CTX0 011110b: COMP1 101100b: TXD008/TXDA008/ SMOSI008/SSDA008

Register	Bit	RX66T (n = 0 to 7)	RX26T (n = 0 to 4, 7)
P24PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIC5U 000011b: MTIC5U# 000101b: TMCI2 000110b: TMO6 001010b: CTS8#/RTS8#/SS8# 001011b: SCK8 001101b: RSPCKA 011110b: COMP0	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIC5U 000011b: MTIC5U# 000101b: TMCI2 000110b: TMO6 001101b: RSPCKA 001110b: RSPCK0 011110b: COMP0 101100b: CTS008#/RTS008#/ SS008# 101101b: SCK008 101110b: DE008
P25PFS	—	P25 pin function control register	—
P26PFS	—	P26 pin function control register	—
P27PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC1A 000010b: MTIOC0C 000011b: MTIOC1A# 000100b: MTIOC0C# 000111b: POE9#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC1A 000010b: MTIOC0C 000011b: MTIOC1A# 000100b: MTIOC0C# 000101b: TMO2 000110b: TMO6 000111b: POE9# 001101b: RSPCKA 001110b: RSPCK0
P2nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P20: IRQ7-DS (64/80/100/112/144-pin) P21: IRQ6-DS (64/80/100/112/144-pin) P22: IRQ10 (64/80/100/112/144-pin) P23: IRQ11 (100/112/144-pin) P24: IRQ4 (100/112/144-pin) P25: IRQ10 (144-pin) P26: IRQ11 (144-pin) P27: IRQ15 (80/100*1/112/144 pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P20: IRQ7 (48/64/80/100-pin) P21: IRQ6 (48/64/80/100-pin) P22: IRQ10 (64/80/100-pin) P23: IRQ11 (100-pin) P24: IRQ4 (100-pin) P27: IRQ15 (80/100-pin)
	ASEL	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin P20: AN216 (64/80/100/112/144-pin) P21: AN217 (64/80/100/112/144-pin)	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin P20: AN216 (48/64/80/100-pin) P21: AN217 (48/64/80/100-pin)

Note: 1. Supported only on products provided with PGA pseudo-differential input

Table 2.35 Comparison of P3n Pin Function Control Registers (P3nPFS)

Register	Bit	RX66T (n = 0 to 5)	RX26T (n = 0 to 3, 6, 7)
P30PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKD 000011b: MTIOC0B# 000100b: MTCLKD# 000101b: TMCI6 001010b: SCK8 001011b: CTS8#/RTS8#/SS8# 001101b: SSLA0 011110b: COMP3	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKD 000011b: MTIOC0B# 000100b: MTCLKD# 000101b: TMCI6 001101b: SSLA0 001110b: SSL00 011000b: GTIV 011110b: COMP3 101100b: SCK008 101101b: CTS008#/RTS008#/ SS008# 101110b: DE008
P31PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0A 000010b: MTCLKC 000011b: MTIOC0A# 000100b: MTCLKC# 000101b: TMRI6 001101b: SSLA1	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0A 000010b: MTCLKC 000011b: MTIOC0A# 000100b: MTCLKC# 000101b: TMRI6 001101b: SSLA1 001110b: SSL01 011000b: GTIU
P32PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTCLKB 000011b: MTIOC3C# 000100b: MTCLKB# 000101b: TMO6 001101b: SSLA2 010100b: GTIOC3A 010110b: GTIOC3A#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTCLKB 000011b: MTIOC3C# 000100b: MTCLKB# 000101b: TMO6 001101b: SSLA2 001110b: SSL02 010100b: GTIOC3A 010101b: GTIOC7A 010110b: GTIOC3A# 010111b: GTIOC7A#

Register	Bit	RX66T (n = 0 to 5)	RX26T (n = 0 to 3, 6, 7)
P33PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKA 000011b: MTIOC3A# 000100b: MTCLKA# 000101b: TMO0 001101b: SSLA3 010100b: GTIOC3B 010110b: GTIOC3B#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKA 000011b: MTIOC3A# 000100b: MTCLKA# 000101b: TMO0 001101b: SSLA3 001110b: SSL03 010100b: GTIOC3B 010101b: GTIOC7B 010110b: GTIOC3B# 010111b: GTIOC7B# 011000b: GTCPPO0
P34PFS	—	P34 pin function control register	—
P35PFS	—	P35 pin function control register	—
P36PFS	—	—	P36 pin function control register
P37PFS	—	—	P37 pin function control register
P3nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ7 (80/100/112/144-pin) P31: IRQ6 (80/100/112/144-pin) P32: IRQ12-DS (100/112/144-pin) P33: IRQ13-DS (100/112/144-pin) P34: IRQ3 (144-pin) P35: IRQ6 (144-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ7 (80/100-pin) P31: IRQ6 (80/100-pin) P32: IRQ12 (100-pin) P33: IRQ13 (100-pin)

Table 2.36 Comparison of P7n Pin Function Control Registers (P7nPFS)

Register	Bit	RX66T (n = 0 to 6)	RX26T (n = 0 to 6)
P70PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000111b: POE0# 001010b: CTS9#/RTS9#/SS9# 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0A 000010b: MTCLKC 000011b: MTIOC0A# 000100b: MTCLKC# 000101b: TMRI6 000111b: POE0# 001010b: SCK5 001101b: SSLA0 001110b: RSPCK0 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD 011000b: GTCPPO0 101100b: CTS009#/RTS009#/ SS009# 101110b: DE009
P71PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3B 000011b: MTIOC3B# 010100b: GTIOC0A 010101b: GTIOC4A 010110b: GTIOC0A# 010111b: GTIOC4A#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3B 000011b: MTIOC3B# 001110b: MISO0 010100b: GTIOC0A 010101b: GTIOC4A 010110b: GTIOC0A# 010111b: GTIOC4A# 011000b: GTOUUP
P72PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4A 000011b: MTIOC4A# 010100b: GTIOC1A 010101b: GTIOC5A 010110b: GTIOC1A# 010111b: GTIOC5A#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4A 000011b: MTIOC4A# 001110b: MOSI0 010100b: GTIOC1A 010101b: GTIOC5A 010110b: GTIOC1A# 010111b: GTIOC5A# 011000b: GTOVUP

Register	Bit	RX66T (n = 0 to 6)	RX26T (n = 0 to 6)
P73PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4B 000011b: MTIOC4B# 010100b: GTIOC2A 010101b: GTIOC6A 010110b: GTIOC2A# 010111b: GTIOC6A#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4B 000011b: MTIOC4B# 001110b: SSL00 010100b: GTIOC2A 010101b: GTIOC6A 010110b: GTIOC2A# 010111b: GTIOC6A# 011000b: GTOWUP
P74PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3D 000011b: MTIOC3D# 010100b: GTIOC0B 010101b: GTIOC4B 010110b: GTIOC0B# 010111b: GTIOC4B#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3D 000011b: MTIOC3D# 001110b: SSL01 010100b: GTIOC0B 010101b: GTIOC4B 010110b: GTIOC0B# 010111b: GTIOC4B# 011000b: GTOULO
P75PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4C 000011b: MTIOC4C# 010100b: GTIOC1B 010101b: GTIOC5B 010110b: GTIOC1B# 010111b: GTIOC5B#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4C 000011b: MTIOC4C# 001110b: SSL02 010100b: GTIOC1B 010101b: GTIOC5B 010110b: GTIOC1B# 010111b: GTIOC5B# 011000b: GTOVLO
P76PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4D 000011b: MTIOC4D# 010100b: GTIOC2B 010101b: GTIOC6B 010110b: GTIOC2B# 010111b: GTIOC6B#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4D 000011b: MTIOC4D# 001110b: SSL03 010100b: GTIOC2B 010101b: GTIOC6B 010110b: GTIOC2B# 010111b: GTIOC6B# 011000b: GTOWLO

Register	Bit	RX66T (n = 0 to 6)	RX26T (n = 0 to 6)
P7nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P70: IRQ5-DS (64/80/100/112/144-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P70: IRQ5 (64/80/100-pin)

Table 2.37 Comparison of P9n Pin Function Control Registers (P9nPFS)

Register	Bit	RX66T (n = 0 to 6)	RX26T (n = 0 to 6)
P90PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC7D 000011b: MTIOC7D# 010100b: GTIOC6B 010101b: GTIOC9B 010110b: GTIOC6B# 010111b: GTIOC9B#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC7D 000011b: MTIOC7D# 001010b: TXD5/SMOSI5/SSDA5 001110b: SSL01 010100b: GTIOC6B 010110b: GTIOC6B# 011000b: GTOWLO
P91PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC7C 000011b: MTIOC7C# 010100b: GTIOC5B 010101b: GTIOC8B 010110b: GTIOC5B# 010111b: GTIOC8B#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC7C 000011b: MTIOC7C# 001010b: RXD5/SMISO5/SSCL5 001110b: RSPCK0 010100b: GTIOC5B 010110b: GTIOC5B# 011000b: GTOVLO

Register	Bit	RX66T (n = 0 to 6)	RX26T (n = 0 to 6)
P92PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC6D 000011b: MTIOC6D# 010100b: GTIOC4B 010101b: GTIOC7B 010110b: GTIOC4B# 010111b: GTIOC7B#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC6D 000010b: MTIOC6C 000011b: MTIOC6D# 000100b: MTIOC6C# 000101b: TMO2 001101b: SSLA3 001110b: MISO0 010000b: CTX0 010100b: GTIOC4B 010101b: GTIOC7B 010110b: GTIOC4B# 010111b: GTIOC7B# 011000b: GTOULO 101100b: SCK009 101101b: TXD011/TXDA011/ SMOSI011/SSDA011 101110b: TXDB009 110011b: SSL03
P93PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC7B 000011b: MTIOC7B# 010100b: GTIOC6A 010101b: GTIOC9A 010110b: GTIOC6A# 010111b: GTIOC9A#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC7B 000010b: MTIOC6A 000011b: MTIOC7B# 000100b: MTIOC6A# 000101b: TMO4 001001b: ADTRG0# 001101b: SSLA2 001110b: MOSI0 010000b: CRX0 010100b: GTIOC6A 010110b: GTIOC6A# 011000b: GTOWUP 101100b: TXD009/TXDA009/ SMOSI009/SSDA009 101101b: RXD011/SMISO011/ SSCL011 110011b: SSL02

Register	Bit	RX66T (n = 0 to 6)	RX26T (n = 0 to 6)
P94PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC7A 000011b: MTIOC7A# 010100b: GTIOC5A 010101b: GTIOC8A 010110b: GTIOC5A# 010111b: GTIOC8A#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC7A 000010b: MTIOC2A 000011b: MTIOC7A# 000100b: MTIOC2A# 000101b: TMRI7 001101b: SSLA0 001110b: SSL00 010100b: GTIOC5A 010101b: GTADSM0 010110b: GTIOC5A# 011000b: GTOVUP 101100b: TXD009/TXDA009/ SMOSI009/SSDA009 101101b: SCK008 101110b: TXDB008 110011b: SSL00
P95PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC6B 000011b: MTIOC6B# 010100b: GTIOC4A 010101b: GTIOC7A 010110b: GTIOC4A# 010111b: GTIOC7A#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC6B 000010b: MTIOC1A 000011b: MTIOC6B# 000100b: MTIOC1A# 000101b: TMCI3 001001b: ADTRG1# 001010b: RXD6/SMISO6/SSCL6 001101b: MISOA 001110b: SSL02 010100b: GTIOC4A 010101b: GTIOC7A 010110b: GTIOC4A# 010111b: GTIOC7A# 011000b: GTOUUP 101101b: RXD008/SMISO008/ SSCL008 110011b: MISO0

Register	Bit	RX66T (n = 0 to 6)	RX26T (n = 0 to 6)
P96PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000111b: POE4# 001010b: CTS8#/RTS8#/SS8# 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD	Pin function select bits b5 b0 000000b: Hi-Z 000111b: POE4# 001110b: SSL03 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD 011000b: GTCPPO4 101100b: CTS008#/RTS008#/ SS008# 101110b: DE008 110011b: RSPCK0
P9nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P96: IRQ4-DS (64/80/100/112/144-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P93: IRQ14 (48/64/80/100-pin) P95: IRQ1 (48/64/80/100-pin) P96: IRQ4 (64/80/100-pin)

Table 2.38 Comparison of PAn Pin Function Control Registers (PAnPFS)

Register	Bit	RX66T (n = 0 to 7)	RX26T (n = 0 to 5)
PA0PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC6C 000011b: MTIOC6C# 000101b: TMO2 001010b: SCK9 001011b: TXD11/SMOSI11 001101b: SSLA3 010000b: CTX0 010001b: USB0_EXICEN 010010b: USB0_VBUSEN	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC6C 000011b: MTIOC6C# 000101b: TMO2 001101b: SSLA3 001110b: SSL03 010000b: CTX0 101100b: SCK009 101101b: TXD011/TXDA011/ SMOSI011/SSDA011 101110b: TXDB009
PA1PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC6A 000011b: MTIOC6A# 000101b: TMO4 001001b: ADTRG0# 001010b: TXD9/SMOSI9/SSDA9 001011b: RXD11/SMISO11/SSCL11 001101b: SSLA2 010000b: CRX0 010001b: USB0_ID 010010b: USB0_OVRCURA	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC6A 000011b: MTIOC6A# 000101b: TMO4 001001b: ADTRG0# 001101b: SSLA2 001110b: SSL02 010000b: CRX0 011000b: GTCPPO4 101100b: TXD009/TXDA009/ SMOSI009/SSDA009 101101b: RXD011/SMISO011/ SSCL011

Register	Bit	RX66T (n = 0 to 7)	RX26T (n = 0 to 5)
PA2PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC2B 000011b: MTIOC2B# 000101b: TMO7 001010b: CTS6#/RTS6#/SS6# 001011b: RXD9/SMISO9/SSCL9 001100b: SCK11 001101b: SSLA1 010100b: GTADSM1	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC2B 000011b: MTIOC2B# 000101b: TMO7 001010b: CTS6#/RTS6#/SS6# 001101b: SSLA1 001110b: SSL01 010100b: GTADSM1 101101b: RXD009/SMISO009/ SSCL009
PA3PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC2A 000011b: MTIOC2A# 000101b: TMRI7 001010b: TXD9/SMOSI9/SSDA9 001011b: SCK8 001101b: SSLA0 010100b: GTADSM0	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC2A 000011b: MTIOC2A# 000101b: TMRI7 001101b: SSLA0 001110b: SSL00 010100b: GTADSM0 101100b: TXD009/TXDA009/ SMOSI009/SSDA009 101101b: SCK008 101110b: TXDB008
PA4PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC1B 000011b: MTIOC1B# 000101b: TMCI7 001001b: ADTRG0# 001010b: SCK6 001011b: TXD8/SMOSI8/SSDA8 001101b: RSPCKA	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC1B 000011b: MTIOC1B# 000101b: TMCI7 001001b: ADTRG0# 001010b: SCK6 001101b: RSPCKA 001110b: RSPCK0 101101b: TXD008/TXDA008/ SMOSI008/SSDA008

Register	Bit	RX66T (n = 0 to 7)	RX26T (n = 0 to 5)
PA5PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC1A 000011b: MTIOC1A# 000101b: TMCI3 001001b: ADTRG1# 001010b: RXD6/SMISO6/SSCL6 001011b: RXD8/SMISO8/SSCL8 001101b: MISOA	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC1A 000011b: MTIOC1A# 000101b: TMCI3 001001b: ADTRG1# 001010b: RXD6/SMISO6/SSCL6 001101b: MISOA 001110b: MISO0 101101b: RXD008/SMISO008/ SSCL008
PA6PFS	—	PA6 pin function control register	—
PA7PFS	—	PA7 pin function control register	—
PAnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA1: IRQ14-DS (100/112/144-pin) PA5: IRQ1 (48/80/100/112/144-pin) PA6: IRQ7 (144-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA1: IRQ14 (100-pin) PA5: IRQ1 (80/100-pin)

Table 2.39 Comparison of PBn Pin Function Control Registers (PBnPFS)

Register	Bit	RX66T (n = 0 to 7)	RX26T (n = 0 to 7)
PB0PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0D 000011b: MTIOC0D# 000101b: TMO0 001001b: ADTRG2# 001010b: TXD6/SMOSI6/SSDA6 001011b: CTS11#/RTS11#/SS11# 001101b: MOSIA	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0D 000011b: MTIOC0D# 000101b: TMO0 001001b: ADTRG2# 001010b: TXD6/SMOSI6/SSDA6 001101b: MOSIA 001110b: MOSI0 011101b: TIC2 101100b: TXD008/TXDA008/ SMOSI008/SSDA008 101101b: CTS011#/RTS011#/ SS011# 101110b: DE011
PB1PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0C 000011b: MTIOC0C# 000101b: TMCI0 001001b: ADSM1 001010b: RXD6/SMISO6/SSCL6 001111b: SCL0 010100b: GTADSM1	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0C 000011b: MTIOC0C# 000101b: TMCI0 001001b: ADSM1 001010b: RXD6/SMISO6/SSCL6 001111b: SCL0 010100b: GTADSM1 010101b: GTIOC7B 010111b: GTIOC7B# 011000b: GTIW 011101b: TOC2 110010b: SCL00
PB2PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0B 000011b: MTIOC0B# 000101b: TMRI0 001001b: ADSM0 001010b: TXD6/SMOSI6/SSDA6 001111b: SDA0 010100b: GTADSM0	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0B 000011b: MTIOC0B# 000101b: TMRI0 001001b: ADSM0 001010b: TXD6/SMOSI6/SSDA6 001111b: SDA0 010100b: GTADSM0 010101b: GTIOC7A 010111b: GTIOC7A# 011000b: GTIV 011101b: TIC1 110010b: SDA00

Register	Bit	RX66T (n = 0 to 7)	RX26T (n = 0 to 7)
PB3PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0A 000011b: MTIOC0A# 000111b: CACREF 001010b: SCK6 001101b: RSPCKA	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0A 000011b: MTIOC0A# 000111b: CACREF 001010b: SCK6 001100b: TXD12/SMOSI12/SSDA12 TXDX12/SIOX12 001101b: RSPCKA 010000b: CTX0 011000b: GTIU 011101b: TOC1 101100b: CTS009#/RTS009#/ SS009# 101110b: DE009
PB4PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000111b: POE8# 001010b: CTS5#/RTS5#/SS5# 001011b: SCK11 001100b: CTS11#/RTS11#/SS11# 010001b: USB0_OVRCURB 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD	Pin function select bits b5 b0 000000b: Hi-Z 000111b: POE8# 001010b: CTS5#/RTS5#/SS5# 001100b: RXD12/SMISO12/SSCL12/ RXDX12 001101b: MISOA 001110b: SSL01 010000b: CRX0 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD 011000b: GTCPPO0 101100b: CTS011#/RTS011#/ SS011# 101101b: SCK011 101110b: TXDB011

Register	Bit	RX66T (n = 0 to 7)	RX26T (n = 0 to 7)
PB5PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 001010b: TXD5/SMOSI5/SSDA5 001011b: TXD11/SMOSI11/SSDA11 001100b: TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12 010000b: CTX0 010001b: USB0_VBUSEN 010100b: GTIOC2B 010110b: GTIOC2B#	Pin function select bits b5 b0 000000b: Hi-Z 001010b: TXD5/SMOSI5/SSDA5 001100b: TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12 001110b: RSPCK0 010000b: CTX0 010100b: GTIOC2B 010101b: GTIOC3B 010110b: GTIOC2B# 010111b: GTIOC3B# 011101b: TIC0 101101b: TXD011/TXDA011/ SMOSI011/SSDA011
PB6PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 001010b: RXD5/SMISO5/SSCL5 001011b: RXD11/SMISO11/SSCL11 001100b: RXD12/SMISO12/SSCL12/ RXDX12 010000b: CRX0 010001b: USB0_OVRCURA 010100b: GTIOC2A 010110b: GTIOC2A#	Pin function select bits b5 b0 000000b: Hi-Z 001010b: RXD5/SMISO5/SSCL5 001100b: RXD12/SMISO12/SSCL12/ RXDX12 001110b: MISO0 010000b: CRX0 010100b: GTIOC2A 010101b: GTIOC3A 010110b: GTIOC2A# 010111b: GTIOC3A# 011101b: TOC0 101101b: RXD011/SMISO011/ SSCL011
PB7PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 001010b: SCK5 001011b: SCK11 001100b: SCK12 010001b: USB0_OVRCURB 010100b: GTIOC1B 010110b: GTIOC1B#	Pin function select bits b5 b0 000000b: Hi-Z 001010b: SCK5 001100b: SCK12 001110b: SSL03 010100b: GTIOC1B 010110b: GTIOC1B# 101101b: SCK011 101110b: TXDB011

Register	Bit	RX66T (n = 0 to 7)	RX26T (n = 0 to 7)
PBnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB0: IRQ8 (48/64/80/100/112/144-pin) PB1: IRQ4 (48/64/80/100/112/144-pin) PB3: IRQ9 (48/64/80/100/112/144-pin) PB4: IRQ3-DS (48/64/80/100/112/144-pin) PB6: IRQ2 (48/64/80/100/112/144-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB0: IRQ8 (48/64/80/100-pin) PB1: IRQ4 (48/64/80/100-pin) PB3: IRQ9 (48/64/80/100-pin) PB4: IRQ3 (48/64/80/100-pin) PB6: IRQ2 (48/64/80/100-pin)

Table 2.40 Comparison of PCn Pin Function Control Register (PCnPFS)

Register	Bit	RX66T	RX26T
PCnPFS	—	PCn pin function control register (n = 0 to 6)	—

Table 2.41 Comparison of PDn Pin Function Control Registers (PDnPFS)

Register	Bit	RX66T (n = 0 to 7)	RX26T (n = 0 to 7)
PD0PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000101b: TMO6 001011b: TXD8/SMOSI8/SSDA8 001101b: RSPCKA 010100b: GTIOC3B 010101b: GTIOC1A 010110b: GTIOC3B# 010111b: GTIOC1A#	Pin function select bits b5 b0 000000b: Hi-Z 000101b: TMO6 001101b: RSPCKA 001110b: RSPCK0 010100b: GTIOC3B 010101b: GTIOC1A 010110b: GTIOC3B# 010111b: GTIOC1A# 101101b: TXD008/TXDA008/ SMOSI008/SSDA008
PD1PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000101b: TMO2 001011b: RXD8/MISO8/SSCL8 001101b: MISOA 010100b: GTIOC3A 010101b: GTIOC0B 010110b: GTIOC3A# 010111b: GTIOC0B#	Pin function select bits b5 b0 000000b: Hi-Z 000101b: TMO2 001101b: MISOA 001110b: MISO0 010100b: GTIOC3A 010101b: GTIOC0B 010110b: GTIOC3A# 010111b: GTIOC0B# 101101b: RXD008/SMISO008/ SSCL008

Register	Bit	RX66T (n = 0 to 7)	RX26T (n = 0 to 7)
PD2PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000101b: TMCI1 000110b: TMO4 001010b: SCK5 001011b: SCK8 001101b: MOSIA 010001b: USB0_VBUS 010100b: GTIOC2B 010101b: GTIOC0A 010110b: GTIOC2B# 010111b: GTIOC0A#	Pin function select bits b5 b0 000000b: Hi-Z 000101b: TMCI1 000110b: TMO4 001010b: SCK5 001101b: MOSIA 001110b: MOSI0 010100b: GTIOC2B 010101b: GTIOC0A 010110b: GTIOC2B# 010111b: GTIOC0A# 101101b: SCK008 101110b: TXDB008
PD3PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000101b: TMO0 001010b: TXD1/SMOSI1/SSDA1 001011b: TXD11/SMOSI11/SSDA11 010100b: GTIOC2A 010101b: GTETRGC 010110b: GTIOC2A#	Pin function select bits b5 b0 000000b: Hi-Z 000101b: TMO0 001010b: TXD1/SMOSI1/SSDA1 001110b: MOSI0 010100b: GTIOC2A 010101b: GTETRGC 010110b: GTIOC2A# 010111b: GTIOC7B 101101b: TXD011/TXDA011/ SMOSI011/SSDA011
PD4PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000101b: TMCI0 000110b: TMCI6 001010b: SCK1 001011b: SCK11 010100b: GTIOC1B 010101b: GTETRGB 010110b: GTIOC1B#	Pin function select bits b5 b0 000000b: Hi-Z 000101b: TMCI0 000110b: TMCI6 001010b: SCK1 001100b: TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12 001110b: SSL02 010100b: GTIOC1B 010101b: GTETRGB 010110b: GTIOC1B# 101101b: SCK011 101110b: TXDB011

Register	Bit	RX66T (n = 0 to 7)	RX26T (n = 0 to 7)
PD5PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000101b: TMRI0 000110b: TMRI6 001010b: RXD1/SMISO1/SSCL1 001011b: RXD11/SMISO11/SSCL11 010100b: GTIOC1A 010101b: GTETRGA 010110b: GTIOC1A#	Pin function select bits b5 b0 000000b: Hi-Z 000101b: TMRI0 000110b: TMRI6 001010b: RXD1/SMISO1/SSCL1 001110b: SSL00 010100b: GTIOC1A 010101b: GTETRGA 010110b: GTIOC1A# 010111b: GTIOC7A 101101b: RXD011/SMISO011/ SSCL011
PD6PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9C 000011b: MTIOC9C# 000101b: TMO1 001001b: ADST0 001010b: CTS1#/RTS1#/SS1# 001011b: CTS11#/RTS11#/SS11# 001101b: SSLA0 010100b: GTIOC0B 010101b: GTIOC3B 010110b: GTIOC0B# 010111b: GTIOC3B#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9C 000011b: MTIOC9C# 000101b: TMO1 001001b: ADST0 001010b: CTS1#/RTS1#/SS1# 001100b: RXD12/SMISO12/ SSCL12/RXDX12 001101b: SSLA0 001110b: SSL00 010100b: GTIOC0B 010101b: GTIOC3B 010110b: GTIOC0B# 010111b: GTIOC3B# 011000b: GTIW 101101b: CTS011#/RTS011#/ SS011# 101110b: DE011

Register	Bit	RX66T (n = 0 to 7)	RX26T (n = 0 to 7)
PD7PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9A 000011b: MTIOC9A# 000101b: TMRI1 000110b: TMRI5 001010b: TXD5/SMOSI5/SSDA5 001101b: SSLA1 010000b: CTX0 010100b: GTIOC0A 010101b: GTIOC3A 010110b: GTIOC0A# 010111b: GTIOC3A#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9A 000011b: MTIOC9A# 000101b: TMRI1 000110b: TMRI5 001010b: TXD5/SMOSI5/SSDA5 001101b: SSLA1 001110b: SSL01 010000b: CTX0 010100b: GTIOC0A 010101b: GTIOC3A 010110b: GTIOC0A# 010111b: GTIOC3A# 011000b: GTIU 101100b: SCK009 101101b: TXD008/TXDA008/ SMOSI008/SSDA008 101110b: TXDB009

Table 2.42 Comparison of PEn Pin Function Control Registers (PEnPFS)

Register	Bit	RX66T (n = 0 to 6)	RX26T (n = 0 to 5)
PE0PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9B 000011b: MTIOC9B# 000101b: TMCI1 000110b: TMCI5 001010b: RXD5/SMISO5/SSCL5 001101b: SSLA2 010000b: CRX0 010001b: USB0_OVRCURB	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9B 000011b: MTIOC9B# 000101b: TMCI1 000110b: TMCI5 001010b: RXD5/SMISO5/SSCL5 001101b: SSLA2 001110b: SSL02 010000b: CRX0 011000b: GTIV
PE1PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9D 000011b: MTIOC9D# 000101b: TMO5 001010b: CTS5#/RTS5#SS5# 001100b: CTS12#/RTS12#/SS12# 001101b: SSLA3	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9D 000011b: MTIOC9D# 000101b: TMO5 001010b: CTS5#/RTS5#SS5# 001100b: CTS12#/RTS12#/SS12# 001101b: SSLA3 001110b: SSL03
PE3PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000010b: MTCLKD 000100b: MTCLKD# 000111b: POE11# 001010b: CTS9#/RTS9#/SS9# 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD	Pin function select bits b5 b0 000000b: Hi-Z 000010b: MTCLKD 000100b: MTCLKD# 000111b: POE11# 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD 101100b: CTS009#/RTS009#/ SS009# 101110b: DE009

Register	Bit	RX66T (n = 0 to 6)	RX26T (n = 0 to 5)
PE4PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000010b: MTCLKC 000100b: MTCLKC# 000111b: POE10# 001010b: SCK9 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD	Pin function select bits b5 b0 000000b: Hi-Z 000010b: MTCLKC 000100b: MTCLKC# 000111b: POE10# 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD 101100b: SCK009 101110b: TXDB009
PE5PFS	PSEL[5:0]	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9D 000011b: MTIOC9D# 001001b: ADST0 001010b: SCK9 001011b: CTS9#/RTS9#/SS9# 010100b: GTIOC3A 010101b: GTETRGB 010110b: GTIOC3A# 010111b: GTETRGD	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9D 000011b: MTIOC9D# 001001b: ADST0 010100b: GTIOC3A 010101b: GTETRGB 010110b: GTIOC3A# 010111b: GTETRGD 101100b: SCK009 101101b: CTS009#/RTS009#/ SS009# 101110b: TXDB009
PE6PFS	—	PE6 pin function control register	—
PEnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE0: IRQ7 (100/112/144-pin) PE1: IRQ15 (100/112/144-pin) PE3: IRQ2-DS (80/100/112/144-pin) PE4: IRQ1 (80/100/112/144-pin) PE5: IRQ0 (100/112/144-pin) PE6: IRQ3 (144-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE0: IRQ7 (100-pin) PE1: IRQ15 (100-pin) PE2: IRQ0 (48/64/80/100) PE3: IRQ2 (80/100-pin) PE4: IRQ1 (80/100-pin) PE5: IRQ0 (100-pin)

Table 2.43 Comparison of PFn Pin Function Control Register (PFnPFS)

Register	Bit	RX66T	RX26T
PFnPFS	—	PFn pin function control register (n = 0 to 3)	—

Table 2.44 Comparison of PGn Pin Function Control Register (PGnPFS)

Register	Bit	RX66T	RX26T
PGnPFS	—	PGn pin function control register (n = 0 to 2)	—

Table 2.45 Comparison of PHn Pin Function Control Register (PHnPFS)

Register	Bit	RX66T	RX26T
PHnPFS	—	PHn pin function control register (n = 0 to 7)	—

Table 2.46 Comparison of PKn Pin Function Control Register (PKnPFS)

Register	Bit	RX66T	RX26T
PKnPFS	—	PKn pin function control register (n = 0 to 2)	—

Table 2.47 Comparison of PN7 Pin Function Control Register (PN7PFS)

Register	Bit	RX66T	RX26T
PN7PFS	—	—	PN7 pin function control register

Table 2.48 Comparison of Multi-Function Pin Controller Registers

Register	Bit	RX66T (MPC)	RX26T (MPC)
PFCSE	—	CS output enable register	—
PFCSS0	—	CS output pin select register 0	—
PFAOE0	—	Address output enable register 0	—
PFAOE1	—	Address output enable register 1	—
PFBCR0	—	External bus control register 0	—
PFBCR1	—	External bus control register 1	—
PFBCR2	—	External bus control register 2	—
PFBCR3	—	External bus control register 3	—
PFBCR4	—	External bus control register 4	—

2.15 Port Output Enable 3

Table 2.49 is Comparative Overview of Port Output Enable 3, and Table 2.50 is Comparison of Port Output Enable 3 Registers.

Table 2.49 Comparative Overview of Port Output Enable 3

Item	RX66T (POE3B)	RX26T (POE3D)
Pin status while output is disabled	• High-impedance • General I/O port	• High-impedance • General I/O port
Target pins for output stop control	• MTU output pins — MTU0 pins (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) — MTU3 pins (MTIOC3B, MTIOC3D) — MTU4 pins (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) — MTU6 pins (MTIOC6B, MTIOC6D) — MTU7 pins (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D) — MTU9 pins (MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D) • GPTW output pins — GPTW0 pins (GTIOC0A, GTIOC0B) — GPTW1 pins (GTIOC1A, GTIOC1B) — GPTW2 pins (GTIOC2A, GTIOC2B) — GPTW3 pins (GTIOC3A, GTIOC3B) — GPTW4 pins (GTIOC4A, GTIOC4B) — GPTW5 pins (GTIOC5A, GTIOC5B) — GPTW6 pins (GTIOC6A, GTIOC6B) — GPTW7 pins (GTIOC7A, GTIOC7B) — GPTW8 pins (GTIOC8A, GTIOC8B) — GPTW9 pins (GTIOC9A, GTIOC9B)	• MTU output pins — MTU0 pins (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) — MTU3 pins (MTIOC3B, MTIOC3D) — MTU4 pins (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) — MTU6 pins (MTIOC6B, MTIOC6D) — MTU7 pins (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D) — MTU9 pins (MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D) • GPTW output pins — GPTW0 pins (GTIOC0A, GTIOC0B) — GPTW1 pins (GTIOC1A, GTIOC1B) — GPTW2 pins (GTIOC2A, GTIOC2B) — GPTW3 pins (GTIOC3A, GTIOC3B) — GPTW4 pins (GTIOC4A, GTIOC4B) — GPTW5 pins (GTIOC5A, GTIOC5B) — GPTW6 pins (GTIOC6A, GTIOC6B) — GPTW7 pins (GTIOC7A, GTIOC7B)

Item	RX66T (POE3B)	RX26T (POE3D)
Conditions for generating output stop requests	• Input pin changes: Signal input occurs on the POE0#, POE4#, POE8#, POE9, POE10#, POE11#, POE12#, POE13#, or POE14# pin. • Short circuit of output pins: A match (short circuit condition) between the output signal levels at the active level lasts at least one cycle on one of the following combinations of pins. [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D — MTIOC6B and MTIOC6D — MTIOC7A and MTIOC7C — MTIOC7B and MTIOC7D [GPTW output pins] — GTIOC0A and GTIOC0B — GTIOC1A and GTIOC1B — GTIOC2A and GTIOC2B — GTIOC4A and GTIOC4B — GTIOC5A and GTIOC5B — GTIOC6A and GTIOC6B — GTIOC7A and GTIOC7B — GTIOC8A and GTIOC8B — GTIOC9A and GTIOC9B • Setting of the SPOER register • Detection of stopped oscillation on main clock oscillator • Detection of comparator C (CMPC) output	• Input pin changes: Signal input occurs on the POE0#, POE4#, POE8#, POE10#, POE11#, POE12#, or POE9# pin. • Short circuit of output pins: A match (short circuit condition) between the output signal levels at the active level lasts at least one cycle on one of the following combinations of pins. [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D — MTIOC6B and MTIOC6D — MTIOC7A and MTIOC7C — MTIOC7B and MTIOC7D [GPTW output pins] — GTIOC0A and GTIOC0B — GTIOC1A and GTIOC1B — GTIOC2A and GTIOC2B — GTIOC4A and GTIOC4B — GTIOC5A and GTIOC5B — GTIOC6A and GTIOC6B — GTIOC7A and GTIOC7B • Setting of the SPOER register • Detection of stopped oscillation on main clock oscillator • Detection of comparator C (CMPC) output
Functions	• Falling-edge detection or low level detection can be set for each of the POE0#, POE4#, POE8#, POE9#, POE11#, POE12#, POE13#, and POE14# pins. For low level detection, the sampling clock can be selected from PCLK/1, PCLK/2, PCLK/4, PCLK/8, PCLK/16, and PCLK/128, and the sampling count can be selected from 4, 8, and 16. • Output on all control target pins can be stopped on detection of the falling edge or low level of input to the POE0#, POE4#, POE8#, POE9#, POE10#, POE11#, POE12#, POE13#, or POE14# pin. • Output on all control target pins can be stopped when oscillation stop is detected in the clock generation circuit.	• Falling-edge detection or low level detection can be set for each of the POE0#, POE4#, POE8#, POE10#, POE11#, POE12#, and POE9# pins. For low level detection, the sampling clock can be selected from PCLK/1, PCLK/2, PCLK/4, PCLK/8, PCLK/16, and PCLK/128, and the sampling count can be selected from 4, 8, and 16. • Output on all control target pins can be stopped on detection of the falling edge or low level of input to the POE0#, POE4#, POE8#, POE10#, POE11#, POE12#, or POE9# pin. • Output on all control target pins can be stopped when oscillation stop is detected in the clock generation circuit.

Item	RX66T (POE3B)	RX26T (POE3D)
Functions	• Output on the MTU complementary PWM output pins can be stopped when output levels of those pins are compared and simultaneous active-level output continues for one or more cycles. • Output on the GPTW output pins (GPTW0 to GPTW2, GPTW4 to GPTW6, and GPTW7 to GPTW9 pins) can be stopped when output levels of those pins are compared and simultaneous active-level output continues for at least one cycle. • Output on all control target pins can be stopped on detection of output of Comparator C (CMPC). • Output on all control target pins can be stopped by modifying the settings of POE registers. • Interrupts can be generated in response to the results of input level sampling or output-level comparison.	• Output on the MTU complementary PWM output pins can be stopped when output levels of those pins are compared and simultaneous active-level output continues for one or more cycles. • Output on the GPTW output pins (GPTW0 to GPTW2, GPTW4 to GPTW7) can be stopped when output levels of those pins are compared and simultaneous active-level output continues for at least one cycle. • Output on all control target pins can be stopped on detection of output of Comparator C (CMPC). • Output on all control target pins can be stopped by modifying the settings of POE registers. • Interrupts can be generated in response to the results of input level sampling or output-level comparison. • Output stop requests in response to level detection signals on the POE0#, POE4#, POE8#, POE10#, POE11#, POE12#, and POE9# pins and COMP0 to COMP5 can be masked by using signals output from the MTU output pins (MTU0 to MTU4, MTU6, MTU7, and MTU9) and GPTW output pins (GPTW0 to GPTW7).

Table 2.50 Comparison of Port Output Enable 3 Registers

Register	Bit	RX66T (POE3B)	RX26T (POE3D)
ICSR1	POE0M[3:0]	POE0 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge of POE0# pin input. 0 0 0 1: Samples the level of the POE0# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 0 1 0: Samples the level of the POE0# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 0 1 1: Samples the level of the POE0# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 0 0: Samples the level of the POE0# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 0 1: Samples the level of the POE0# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 1 0: Samples the level of the POE0# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified number of times. Settings other than the above are prohibited.	POE0 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge or rising edge of POE0# pin input. 0 0 0 1: Samples input on the POE0# pin by PCLK/8, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 0 1 0: Samples input on the POE0# pin by PCLK/16, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 0 1 1: Samples input on the POE0# pin by PCLK/128, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 1 0 0: Samples input on the POE0# pin by PCLK, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 1 0 1: Samples input on the POE0# pin by PCLK/2, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 1 1 0: Samples input on the POE0# pin by PCLK/4, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. Settings other than the above are prohibited.

Register	Bit	RX66T (POE3B)	RX26T (POE3D)
ICSR1	POE0M2[3:0]	POE0 sampling count select bits b7 b4 0 0 0 0: 16 times 0 0 0 1: 4 times 0 0 1 0: 8 times Settings other than the above are prohibited.	POE0 sampling count select bits b7 b4 0 0 0 0: 16 times 0 0 0 1: 4 times 0 0 1 0: 8 times 0 0 1 1: 9 times 0 1 0 0: 10 times 0 1 0 1: 11 times 0 1 1 0: 12 times 0 1 1 1: 13 times 1 0 0 0: 14 times 1 0 0 1: 15 times Settings other than the above are prohibited.
	INV	—	POE0# pin input invert bit

Register	Bit	RX66T (POE3B)	RX26T (POE3D)
ICSR2	POE4M[3:0]	POE4 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge of POE4# pin input. 0 0 0 1: Samples the level of the POE4# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 0 1 0: Samples the level of the POE4# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 0 1 1: Samples the level of the POE4# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 0 0: Samples the level of the POE4# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 0 1: Samples the level of the POE4# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 1 0: Samples the level of the POE4# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified number of times. Settings other than the above are prohibited.	POE4 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge or rising edge of POE4# pin input. 0 0 0 1: Samples input on the POE4# pin by PCLK/8, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 0 1 0: Samples input on the POE4# pin by PCLK/16, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 0 1 1: Samples input on the POE4# pin by PCLK/128, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 1 0 0: Samples input on the POE4# pin by PCLK, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 1 0 1: Samples input on the POE4# pin by PCLK/2, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 1 1 0: Samples input on the POE4# pin by PCLK/4, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. Settings other than the above are prohibited.

Register	Bit	RX66T (POE3B)	RX26T (POE3D)
ICSR2	POE4M2[3:0]	POE4 sampling count select bits b7 b4 0 0 0 0: 16 times 0 0 0 1: 4 times 0 0 1 0: 8 times Settings other than the above are prohibited.	POE4 sampling count select bits b7 b4 0 0 0 0: 16 times 0 0 0 1: 4 times 0 0 1 0: 8 times 0 0 1 1: 9 times 0 1 0 0: 10 times 0 1 0 1: 11 times 0 1 1 0: 12 times 0 1 1 1: 13 times 1 0 0 0: 14 times 1 0 0 1: 15 times Settings other than the above are prohibited.
	INV	—	POE4# pin input invert bit

Register	Bit	RX66T (POE3B)	RX26T (POE3D)
ICSR3	POE8M[3:0]	POE8 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge of POE8# pin input. 0 0 0 1: Samples the level of the POE8# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 0 1 0: Samples the level of the POE8# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 0 1 1: Samples the level of the POE8# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 0 0: Samples the level of the POE8# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 0 1: Samples the level of the POE8# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 1 0: Samples the level of the POE8# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified number of times. Settings other than the above are prohibited.	POE8 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge or rising edge of POE8# pin input. 0 0 0 1: Samples input on the POE8# pin by PCLK/8, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 0 1 0: Samples input on the POE8# pin by PCLK/16, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 0 1 1: Samples input on the POE8# pin by PCLK/128, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 1 0 0: Samples input on the POE8# pin by PCLK, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 1 0 1: Samples input on the POE8# pin by PCLK/2, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 1 1 0: Samples input on the POE8# pin by PCLK/4, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. Settings other than the above are prohibited.

Register	Bit	RX66T (POE3B)	RX26T (POE3D)
ICSR3	POE8M2[3:0]	POE8 sampling count select bits b7 b4 0 0 0 0: 16 times 0 0 0 1: 4 times 0 0 1 0: 8 times Settings other than the above are prohibited.	POE8 sampling count select bits b7 b4 0 0 0 0: 16 times 0 0 0 1: 4 times 0 0 1 0: 8 times 0 0 1 1: 9 times 0 1 0 0: 10 times 0 1 0 1: 11 times 0 1 1 0: 12 times 0 1 1 1: 13 times 1 0 0 0: 14 times 1 0 0 1: 15 times Settings other than the above are prohibited.
	INV	—	POE8# pin input invert bit

Register	Bit	RX66T (POE3B)	RX26T (POE3D)
ICSR4	POE10M[3:0]	POE10 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge of POE10# pin input. 0 0 0 1: Samples the level of the POE10# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 0 1 0: Samples the level of the POE10# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 0 1 1: Samples the level of the POE10# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 0 0: Samples the level of the POE10# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 0 1: Samples the level of the POE10# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 1 0: Samples the level of the POE10# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified number of times. Settings other than the above are prohibited.	POE10 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge or rising edge of the POE10# pin input. 0 0 0 1: Samples input on the POE10# pin by PCLK/8, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 0 1 0: Samples input on the POE10# pin by PCLK/16, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 0 1 1: Samples input on the POE10# pin by PCLK/128, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 1 0 0: Samples input on the POE10# pin by PCLK, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 1 0 1: Samples input on the POE10# pin by PCLK/2, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 1 1 0: Samples input on the POE10# pin by PCLK/4, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. Settings other than the above are prohibited.

Register	Bit	RX66T (POE3B)	RX26T (POE3D)
ICSR4	POE10M2[3:0]	POE10 sampling count select bits b7 b4 0 0 0 0: 16 times 0 0 0 1: 4 times 0 0 1 0: 8 times Settings other than the above are prohibited.	POE10 sampling count select bits b7 b4 0 0 0 0: 16 times 0 0 0 1: 4 times 0 0 1 0: 8 times 0 0 1 1: 9 times 0 1 0 0: 10 times 0 1 0 1: 11 times 0 1 1 0: 12 times 0 1 1 1: 13 times 1 0 0 0: 14 times 1 0 0 1: 15 times Settings other than the above are prohibited.
	INV	—	POE10# pin input invert bit

Register	Bit	RX66T (POE3B)	RX26T (POE3D)
ICSR5	POE11M[3:0]	POE11 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge of POE11# pin input. 0 0 0 1: Samples the level of the POE11# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 0 1 0: Samples the level of the POE11# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 0 1 1: Samples the level of the POE11# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 0 0: Samples the level of the POE11# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 0 1: Samples the level of the POE11# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 1 0: Samples the level of the POE11# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified number of times. Settings other than the above are prohibited.	POE11 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge or rising edge of the POE11# pin input. 0 0 0 1: Samples input on the POE11# pin by PCLK/8, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 0 1 0: Samples input on the POE11# pin by PCLK/16, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 0 1 1: Samples input on the POE11# pin by PCLK/128, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 1 0 0: Samples input on the POE11# pin by PCLK, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 1 0 1: Samples input on the POE11# pin by PCLK/2, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 1 1 0: Samples input on the POE11# pin by PCLK/4, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. Settings other than the above are prohibited.

Register	Bit	RX66T (POE3B)	RX26T (POE3D)
ICSR5	POE11M2[3:0]	POE11 sampling count select bits b7 b4 0 0 0 0: 16 times 0 0 0 1: 4 times 0 0 1 0: 8 times Settings other than the above are prohibited.	POE11 sampling count select bits b7 b4 0 0 0 0: 16 times 0 0 0 1: 4 times 0 0 1 0: 8 times 0 0 1 1: 9 times 0 1 0 0: 10 times 0 1 0 1: 11 times 0 1 1 0: 12 times 0 1 1 1: 13 times 1 0 0 0: 14 times 1 0 0 1: 15 times Settings other than the above are prohibited.
	INV	—	POE11# pin input invert bit

Register	Bit	RX66T (POE3B)	RX26T (POE3D)
ICSR7	POE12M[3:0]	POE12 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge of POE12# pin input. 0 0 0 1: Samples the level of the POE12# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 0 1 0: Samples the level of the POE12# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 0 1 1: Samples the level of the POE12# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 0 0: Samples the level of the POE12# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 0 1: Samples the level of the POE12# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 1 0: Samples the level of the POE12# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified number of times. Settings other than the above are prohibited.	POE12 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge or rising edge of the POE12# pin input. 0 0 0 1: Samples input on the POE12# pin by PCLK/8, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 0 1 0: Samples input on the POE12# pin by PCLK/16, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 0 1 1: Samples input on the POE12# pin by PCLK/128, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 1 0 0: Samples input on the POE12# pin by PCLK, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 1 0 1: Samples input on the POE12# pin by PCLK/2, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 1 1 0: Samples input on the POE12# pin by PCLK/4, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. Settings other than the above are prohibited.

Register	Bit	RX66T (POE3B)	RX26T (POE3D)
ICSR7	POE12M2[3:0]	POE12 sampling count select bits b7 b4 0 0 0 0: 16 times 0 0 0 1: 4 times 0 0 1 0: 8 times Settings other than the above are prohibited.	POE12 sampling count select bits b7 b4 0 0 0 0: 16 times 0 0 0 1: 4 times 0 0 1 0: 8 times 0 0 1 1: 9 times 0 1 0 0: 10 times 0 1 0 1: 11 times 0 1 1 0: 12 times 0 1 1 1: 13 times 1 0 0 0: 14 times 1 0 0 1: 15 times Settings other than the above are prohibited.
	INV	—	POE12# pin input invert bit

Register	Bit	RX66T (POE3B)	RX26T (POE3D)
ICSR8	POE9M[3:0]	POE9 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge of POE9# pin input. 0 0 0 1: Samples the level of the POE9# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 0 1 0: Samples the level of the POE9# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 0 1 1: Samples the level of the POE9# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 0 0: Samples the level of the POE9# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 0 1: Samples the level of the POE9# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified number of times. 0 1 1 0: Samples the level of the POE9# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified number of times. Settings other than the above are prohibited.	POE9 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge or rising edge of POE9# pin input. 0 0 0 1: Samples input on the POE9# pin by PCLK/8, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 0 1 0: Samples input on the POE9# pin by PCLK/16, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 0 1 1: Samples input on the POE9# pin by PCLK/128, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 1 0 0: Samples input on the POE9# pin by PCLK, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 1 0 1: Samples input on the POE9# pin by PCLK/2, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. 0 1 1 0: Samples input on the POE9# pin by PCLK/4, and accepts a request when consecutive low-level or high-level results are detected for the specified number of times. Settings other than the above are prohibited.

Register	Bit	RX66T (POE3B)	RX26T (POE3D)
ICSR8	POE9M2[3:0]	POE9 sampling count select bits b7 b4 0 0 0 0: 16 times 0 0 0 1: 4 times 0 0 1 0: 8 times Settings other than the above are prohibited.	POE9 sampling count select bits b7 b4 0 0 0 0: 16 times 0 0 0 1: 4 times 0 0 1 0: 8 times 0 0 1 1: 9 times 0 1 0 0: 10 times 0 1 0 1: 11 times 0 1 1 0: 12 times 0 1 1 1: 13 times 1 0 0 0: 14 times 1 0 0 1: 15 times Settings other than the above are prohibited.
	INV	—	POE9# pin input invert bit
ICSR9	—	Output level control/status register 9	—
ICSR10	—	Output level control/status register 10	—
ALR5	OLSG1A	GTIOC8A pin active level setting bit	—
	OLSG1B	GTIOC8B pin active level setting bit	—
	OLSG2A	GTIOC9A pin active level setting bit	—
	OLSG2B	GTIOC9B pin active level setting bit	—
SPOER	GPT79HIZ	GPTW7 to GPTW9 pin output stop enable bit 0: Does not stop output on pins. 1: Stops output on pins.	GPTW7 pin output stop enable bit 0: Does not stop output on pins. 1: Stops output on pins.
POECR3	GPT8ABZE	GTIOC8A/GTIOC8B pin high impedance enable bit	—
	GPT9ABZE	GTIOC9A/GTIOC9B pin high impedance enable bit	—
POECR4	IC9ADDMT34ZE	Bit for adding POE13F to the MTU3 and MTU4 output stop conditions	—
	IC10ADDMT34ZE	Bit for adding POE14F to the MTU3 and MTU4 output stop conditions	—
POECR4B	IC9ADDMT67ZE	Bit for adding POE13F to the MTU6 and MTU7 output stop conditions	—
	IC10ADDMT67ZE	Bit for adding POE14F to the MTU6 and MTU7 output stop conditions	—
POECR5	IC9ADDMT0ZE	Bit for adding POE13F to the MTU0 output stop conditions	—
	IC10ADDMT0ZE	Bit for adding POE14F to the MTU0 output stop conditions	—
POECR6	IC9ADDGPT01ZE	Bit for adding POE13F to the GPTW0 and GPTW1 output stop conditions	—
	IC10ADDGPT01ZE	Bit for adding POE14F to the GPTW0 and GPTW1 output stop conditions	—
POECR6B	IC9ADDGPT23ZE	Bit for adding POE13F to the GPTW2 and GPTW3 output stop conditions	—
	IC10ADDGPT23ZE	Bit for adding POE14F to the GPTW2 and GPTW3 output stop conditions	—

Register	Bit	RX66T (POE3B)	RX26T (POE3D)
POECR8	IC9ADDMT9ZE	Bit for adding POE13F to the MTU9 output stop conditions	—
	IC10ADDMT9ZE	Bit for adding POE14F to the MTU9 output stop conditions	—
POECR9	IC9ADDGPT02ZE	Bit for adding POE13F to the GPTW0 to GPTW2 output stop conditions	—
	IC10ADDGPT02ZE	Bit for adding POE14F to the GPTW0 to GPTW2 output stop conditions	—
POECR10	IC9ADDGPT46ZE	Bit for adding POE13F to the GPTW4 to GPTW6 output stop conditions	—
	IC10ADDGPT46ZE	Bit for adding POE14F to the GPTW4 to GPTW6 output stop conditions	—
POECR11	CMADDGPT79ZE	Bit for adding CFLAG to the GPTW7 to GPTW9 output stop conditions 0: The flag is not added to the output stop control conditions. 1: The flag is added to the output stop control conditions.	Bit for adding CFLAG to the GPTW7 output stop conditions 0: The flag is not added to the output stop control conditions. 1: The flag is added to the output stop control conditions.
	IC1ADDGPT79ZE	Bit for adding POE0F to the GPTW7 to GPTW9 output stop conditions 0: The flag is not added to the output stop control conditions. 1: The flag is added to the output stop control conditions.	Bit for adding POE0F to the GPTW7 output stop conditions 0: The flag is not added to the output stop control conditions. 1: The flag is added to the output stop control conditions.
	IC2ADDGPT79ZE	Bit for adding POE4F to the GPTW7 to GPTW9 output stop conditions 0: The flag is not added to the output stop control conditions. 1: The flag is added to the output stop control conditions.	Bit for adding POE4F to the GPTW7 output stop conditions 0: The flag is not added to the output stop control conditions. 1: The flag is added to the output stop control conditions.
	IC3ADDGPT79ZE	Bit for adding POE8F to the GPTW7 to GPTW9 output stop conditions 0: The flag is not added to the output stop control conditions. 1: The flag is added to the output stop control conditions.	Bit for adding POE8F to the GPTW7 output stop conditions 0: The flag is not added to the output stop control conditions. 1: The flag is added to the output stop control conditions.
	IC4ADDGPT79ZE	Bit for adding POE10F to the GPTW7 to GPTW9 output stop conditions 0: The flag is not added to the output stop control conditions. 1: The flag is added to the output stop control conditions.	Bit for adding POE10F to the GPTW7 output stop conditions 0: The flag is not added to the output stop control conditions. 1: The flag is added to the output stop control conditions.
	IC5ADDGPT79ZE	Bit for adding POE11F to the GPTW7 to GPTW9 output stop conditions 0: The flag is not added to the output stop control conditions. 1: The flag is added to the output stop control conditions.	Bit for adding POE11F to the GPTW7 output stop conditions 0: The flag is not added to the output stop control conditions. 1: The flag is added to the output stop control conditions.

Register	Bit	RX66T (POE3B)	RX26T (POE3D)
POECR11	IC6ADDGPT79ZE	Bit for adding POE12F to the GPTW7 to GPTW9 output stop conditions 0: The flag is not added to the output stop control conditions. 1: The flag is added to the output stop control conditions.	Bit for adding POE12F to the GPTW7 output stop conditions 0: The flag is not added to the output stop control conditions. 1: The flag is added to the output stop control conditions.
	IC8ADDGPT79ZE	Bit for adding POE9F to the GPTW7 to GPTW9 output stop conditions 0: The flag is not added to the output stop control conditions. 1: The flag is added to the output stop control conditions.	Bit for adding POE9F to the GPTW7 output stop conditions 0: The flag is not added to the output stop control conditions. 1: The flag is added to the output stop control conditions.
	IC9ADDGPT79ZE	Bit for adding POE13F to the GPTW7 to GPTW9 output stop conditions	—
	IC10ADDGPT79ZE	Bit for adding POE14F to the GPTW7 to GPTW9 output stop conditions	—
PMMCR3	—	Port mode mask control register 3	—
M0SELR1	M0ASEL[3:0]	MTU0-A (MTIOC0A) pin select bits b3 b0 0 0 0 0: Does not control the output stop state for any MTIOC0A pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC0A pin is assigned to PB3. 0 0 1 0: Controls the output stop state on the assumption that the MTIOC0A pin is assigned to P31. Settings other than the above are prohibited.	MTU0-A (MTIOC0A) pin select bits b3 b0 0 0 0 0: Does not control the output stop state for any MTIOC0A pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC0A pin is assigned to PB3. 0 0 1 0: Controls the output stop state on the assumption that the MTIOC0A pin is assigned to P31. 0 0 1 1: Controls the output stop state on the assumption that the MTIOC0A pin is assigned to P70. Settings other than the above are prohibited.

Register	Bit	RX66T (POE3B)	RX26T (POE3D)
M0SELR1	M0BSEL[3:0]	MTU0-B (MTIOC0B) pin select bits b7 b4 0 0 0 0: Does not control the output stop state for any MTIOC0B pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC0B pin is assigned to PB2. 0 0 1 0: Controls the output stop state on the assumption that the MTIOC0B pin is assigned to P30. 0 0 1 1: Controls the output stop state on the assumption that the MTIOC0B pin is assigned to PC0. Settings other than the above are prohibited.	MTU0-B (MTIOC0B) pin select bits b7 b4 0 0 0 0: Does not control the output stop state for any MTIOC0B pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC0B pin is assigned to PB2. 0 0 1 0: Controls the output stop state on the assumption that the MTIOC0B pin is assigned to P30. Settings other than the above are prohibited.
M0SELR2	M0CSEL[3:0]	MTU0-C (MTIOC0C) pin select bits b3 b0 0 0 0 0: Does not control the output stop state for any MTIOC0C pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC0C pin is assigned to PB1. 0 0 1 0: Controls the output stop state on the assumption that the MTIOC0C pin is assigned to P27. 0 0 1 1: Controls the output stop state on the assumption that the MTIOC0C pin is assigned to PC1. Settings other than the above are prohibited.	MTU0-C (MTIOC0C) pin select bits b3 b0 0 0 0 0: Does not control the output stop state for any MTIOC0C pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC0C pin is assigned to PB1. 0 0 1 0: Controls the output stop state on the assumption that the MTIOC0C pin is assigned to P27. Settings other than the above are prohibited.
	M0DSEL[3:0]	MTU0-D (MTIOC0D) pin select bits b7 b4 0 0 0 0: Does not control the output stop state for any MTIOC0D pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC0D pin is assigned to PB0. 0 0 1 1: Controls the output stop state on the assumption that the MTIOC0D pin is assigned to PC2. Settings other than the above are prohibited.	MTU0-D (MTIOC0D) pin select bits b7 b4 0 0 0 0: Does not control the output stop state for any MTIOC0D pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC0D pin is assigned to PB0. Settings other than the above are prohibited.

Register	Bit	RX66T (POE3B)	RX26T (POE3D)
M3SELR	M3BSEL[3:0]	MTU3-B (MTIOC3B) pin select bits b3 b0 0 0 0 0: Does not control the output stop state for any MTIOC3B pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC3B pin is assigned to P71. 0 0 1 0: Controls the output stop state on the assumption that the MTIOC3B pin is assigned to P12. Settings other than the above are prohibited.	MTU3-B (MTIOC3B) pin select bits b3 b0 0 0 0 0: Does not control the output stop state for any MTIOC3B pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC3B pin is assigned to P71. Settings other than the above are prohibited.
	M3DSEL[3:0]	MTU3-D (MTIOC3D) pin select bits b7 b4 0 0 0 0: Does not control the output stop state for any MTIOC3D pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC3D pin is assigned to P74. 0 0 1 0: Controls the output stop state on the assumption that the MTIOC3D pin is assigned to P15. Settings other than the above are prohibited.	MTU3-D (MTIOC3D) pin select bits b7 b4 0 0 0 0: Does not control the output stop state for any MTIOC3D pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC3D pin is assigned to P74. Settings other than the above are prohibited.
M4SELR1	M4ASEL[3:0]	MTU4-A (MTIOC4A) pin select bits b3 b0 0 0 0 0: Does not control the output stop state for any MTIOC4A pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC4A pin is assigned to P72. 0 0 1 0: Controls the output stop state on the assumption that the MTIOC4A pin is assigned to P13. Settings other than the above are prohibited.	MTU4-A (MTIOC4A) pin select bits b3 b0 0 0 0 0: Does not control the output stop state for any MTIOC4A pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC4A pin is assigned to P72. Settings other than the above are prohibited.

Register	Bit	RX66T (POE3B)	RX26T (POE3D)
M4SELR1	M4CSEL[3:0]	MTU4-C (MTIOC4C) pin select bits b7 b4 0 0 0 0: Does not control the output stop state for any MTIOC4C pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC4C pin is assigned to P75. 0 0 1 0: Controls the output stop state on the assumption that the MTIOC4C pin is assigned to P16. Settings other than the above are prohibited.	MTU4-C (MTIOC4C) pin select bits b7 b4 0 0 0 0: Does not control the output stop state for any MTIOC4C pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC4C pin is assigned to P75. Settings other than the above are prohibited.
M4SELR2	M4BSEL[3:0]	MTU4-B (MTIOC4B) pin select bits b3 b0 0 0 0 0: Does not control the output stop state for any MTIOC4B pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC4B pin is assigned to P73. 0 0 1 0: Controls the output stop state on the assumption that the MTIOC4B pin is assigned to P14. Settings other than the above are prohibited.	MTU4-B (MTIOC4B) pin select bits b3 b0 0 0 0 0: Does not control the output stop state for any MTIOC4B pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC4B pin is assigned to P73. Settings other than the above are prohibited.
	M4DSEL[3:0]	MTU4-D (MTIOC4D) pin select bits b7 b4 0 0 0 0: Does not control the output stop state for any MTIOC4D pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC4D pin is assigned to P76. 0 0 1 0: Controls the output stop state on the assumption that the MTIOC4D pin is assigned to P17. Settings other than the above are prohibited.	MTU4-D (MTIOC4D) pin select bits b7 b4 0 0 0 0: Does not control the output stop state for any MTIOC4D pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC4D pin is assigned to P76. Settings other than the above are prohibited.

Register	Bit	RX66T (POE3B)	RX26T (POE3D)
M9SELR1	M9ASEL[3:0]	MTU9-A (MTIOC9A) pin select bits b3 b0 0 0 0 0: Does not control the output stop state for any MTIOC9A pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC9A pin is assigned to PD7. 0 0 1 0: Controls the output stop state on the assumption that the MTIOC9A pin is assigned to P21. 0 0 1 1: Controls the output stop state on the assumption that the MTIOC9A pin is assigned to P00. 0 1 0 0: Controls the output stop state on the assumption that the MTIOC9A pin is assigned to P26. 0 1 0 1: Controls the output stop state on the assumption that the MTIOC9A pin is assigned to P35. Settings other than the above are prohibited.	MTU9-A (MTIOC9A) pin select bits b3 b0 0 0 0 0: Does not control the output stop state for any MTIOC9A pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC9A pin is assigned to PD7. 0 0 1 0: Controls the output stop state on the assumption that the MTIOC9A pin is assigned to P21. 0 0 1 1: Controls the output stop state on the assumption that the MTIOC9A pin is assigned to P00. Settings other than the above are prohibited.
	M9BSEL[3:0]	MTU9-B (MTIOC9B) pin select bits b7 b4 0 0 0 0: Does not control the output stop state for any MTIOC9B pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC9B pin is assigned to PE0. 0 0 1 0: Controls the output stop state on the assumption that the MTIOC9B pin is assigned to PC4. 0 0 1 1: Controls the output stop state on the assumption that the MTIOC9B pin is assigned to P10. 0 1 0 0: Controls the output stop state on the assumption that the MTIOC9B pin is assigned to P22. 0 1 0 1: Controls the output stop state on the assumption that the MTIOC9B pin is assigned to P34. Settings other than the above are prohibited.	MTU9-B (MTIOC9B) pin select bits b7 b4 0 0 0 0: Does not control the output stop state for any MTIOC9B pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC9B pin is assigned to PE0. 0 0 1 1: Controls the output stop state on the assumption that the MTIOC9B pin is assigned to P10. 0 1 0 0: Controls the output stop state on the assumption that the MTIOC9B pin is assigned to P22. Settings other than the above are prohibited.

Register	Bit	RX66T (POE3B)	RX26T (POE3D)
M9SELR2	M9CSEL[3:0]	MTU9-C (MTIOC9C) pin select bits b3 b0 0 0 0 0: Does not control the output stop state for any MTIOC9C pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC9C pin is assigned to PD6. 0 0 1 0: Controls the output stop state on the assumption that the MTIOC9C pin is assigned to P20. 0 0 1 1: Controls the output stop state on the assumption that the MTIOC9C pin is assigned to P01. 0 1 0 0: Controls the output stop state on the assumption that the MTIOC9C pin is assigned to P25. 0 1 0 1: Controls the output stop state on the assumption that the MTIOC9C pin is assigned to PC6. Settings other than the above are prohibited.	MTU9-C (MTIOC9C) pin select bits b3 b0 0 0 0 0: Does not control the output stop state for any MTIOC9C pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC9C pin is assigned to PD6. 0 0 1 0: Controls the output stop state on the assumption that the MTIOC9C pin is assigned to P20. 0 0 1 1: Controls the output stop state on the assumption that the MTIOC9C pin is assigned to P01. Settings other than the above are prohibited.
	M9DSEL[3:0]	MTU9-D (MTIOC9D) pin select bits b7 b4 0 0 0 0: Does not control the output stop state for any MTIOC9D pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC9D pin is assigned to PE1. 0 0 1 0: Controls the output stop state on the assumption that the MTIOC9D pin is assigned to PC3. 0 0 1 1: Controls the output stop state on the assumption that the MTIOC9D pin is assigned to PE5. 0 1 0 0: Controls the output stop state on the assumption that the MTIOC9D pin is assigned to P11. 0 1 0 1: Controls the output stop state on the assumption that the MTIOC9D pin is assigned to PC5. Settings other than the above are prohibited.	MTU9-D (MTIOC9D) pin select bits b7 b4 0 0 0 0: Does not control the output stop state for any MTIOC9D pin. 0 0 0 1: Controls the output stop state on the assumption that the MTIOC9D pin is assigned to PE1. 0 0 1 0: Controls the output stop state on the assumption that the MTIOC9D pin is assigned to PN7. 0 0 1 1: Controls the output stop state on the assumption that the MTIOC9D pin is assigned to PE5. 0 1 0 0: Controls the output stop state on the assumption that the MTIOC9D pin is assigned to P11. Settings other than the above are prohibited.

Register	Bit	RX66T (POE3B)	RX26T (POE3D)
G0SELR	G0ASEL[3:0]	GPTW0-A (GTIOC0A) pin select bits b3 b0 0 0 0 0: Does not control the output stop state for any GTIOC0A pin. 0 0 0 1: Controls the output stop state on the assumption that the GTIOC0A pin is assigned to P71. 0 0 1 0: Controls the output stop state on the assumption that the GTIOC0A pin is assigned to PD7. 0 0 1 1: Controls the output stop state on the assumption that the GTIOC0A pin is assigned to P12. 0 1 0 0: Controls the output stop state on the assumption that the GTIOC0A pin is assigned to PD2. 0 1 0 1: Controls the output stop state on the assumption that the GTIOC0A pin is assigned to PG1. Settings other than the above are prohibited.	GPTW0-A (GTIOC0A) pin select bits b3 b0 0 0 0 0: Does not control the output stop state for any GTIOC0A pin. 0 0 0 1: Controls the output stop state on the assumption that the GTIOC0A pin is assigned to P71. 0 0 1 0: Controls the output stop state on the assumption that the GTIOC0A pin is assigned to PD7. 0 1 0 0: Controls the output stop state on the assumption that the GTIOC0A pin is assigned to PD2. Settings other than the above are prohibited.
	G0BSEL[3:0]	GPTW0-B (GTIOC0B) pin select bits b7 b4 0 0 0 0: Does not control the output stop state for any GTIOC0B pin. 0 0 0 1: Controls the output stop state on the assumption that the GTIOC0B pin is assigned to P74. 0 0 1 0: Controls the output stop state on the assumption that the GTIOC0B pin is assigned to PD6. 0 0 1 1: Controls the output stop state on the assumption that the GTIOC0B pin is assigned to P15. 0 1 0 0: Controls the output stop state on the assumption that the GTIOC0B pin is assigned to PD1. 0 1 0 1: Controls the output stop state on the assumption that the GTIOC0B pin is assigned to PG2. Settings other than the above are prohibited.	GPTW0-B (GTIOC0B) pin select bits b7 b4 0 0 0 0: Does not control the output stop state for any GTIOC0B pin. 0 0 0 1: Controls the output stop state on the assumption that the GTIOC0B pin is assigned to P74. 0 0 1 0: Controls the output stop state on the assumption that the GTIOC0B pin is assigned to PD6. 0 1 0 0: Controls the output stop state on the assumption that the GTIOC0B pin is assigned to PD1. Settings other than the above are prohibited.

Register	Bit	RX66T (POE3B)	RX26T (POE3D)
G1SELR	G1ASEL[3:0]	GPTW1-A (GTIOC1A) pin select bits b3 b0 0 0 0 0: Does not control the output stop state for any GTIOC1A pin. 0 0 0 1: Controls the output stop state on the assumption that the GTIOC1A pin is assigned to P72. 0 0 1 0: Controls the output stop state on the assumption that the GTIOC1A pin is assigned to PD5. 0 0 1 1: Controls the output stop state on the assumption that the GTIOC1A pin is assigned to P13. 0 1 0 0: Controls the output stop state on the assumption that the GTIOC1A pin is assigned to PD0. 0 1 0 1: Controls the output stop state on the assumption that the GTIOC1A pin is assigned to PK2. Settings other than the above are prohibited.	GPTW1-A (GTIOC1A) pin select bits b3 b0 0 0 0 0: Does not control the output stop state for any GTIOC1A pin. 0 0 0 1: Controls the output stop state on the assumption that the GTIOC1A pin is assigned to P72. 0 0 1 0: Controls the output stop state on the assumption that the GTIOC1A pin is assigned to PD5. 0 1 0 0: Controls the output stop state on the assumption that the GTIOC1A pin is assigned to PD0. Settings other than the above are prohibited.
	G1BSEL[3:0]	GPTW1-B (GTIOC1B) pin select bits b7 b4 0 0 0 0: Does not control the output stop state for any GTIOC1B pin. 0 0 0 1: Controls the output stop state on the assumption that the GTIOC1B pin is assigned to P75. 0 0 1 0: Controls the output stop state on the assumption that the GTIOC1B pin is assigned to PD4. 0 0 1 1: Controls the output stop state on the assumption that the GTIOC1B pin is assigned to P16. 0 1 0 0: Controls the output stop state on the assumption that the GTIOC1B pin is assigned to PB7. 0 1 0 1: Controls the output stop state on the assumption that the GTIOC1B pin is assigned to PG0. Settings other than the above are prohibited.	GPTW1-B (GTIOC1B) pin select bits b7 b4 0 0 0 0: Does not control the output stop state for any GTIOC1B pin. 0 0 0 1: Controls the output stop state on the assumption that the GTIOC1B pin is assigned to P75. 0 0 1 0: Controls the output stop state on the assumption that the GTIOC1B pin is assigned to PD4. 0 1 0 0: Controls the output stop state on the assumption that the GTIOC1B pin is assigned to PB7. Settings other than the above are prohibited.

Register	Bit	RX66T (POE3B)	RX26T (POE3D)
G2SELR	G2ASEL[3:0]	GPTW2-A (GTIOC2A) pin select bits b3 b0 0 0 0 0: Does not control the output stop state for any GTIOC2A pin. 0 0 0 1: Controls the output stop state on the assumption that the GTIOC2A pin is assigned to P73. 0 0 1 0: Controls the output stop state on the assumption that the GTIOC2A pin is assigned to PD3. 0 0 1 1: Controls the output stop state on the assumption that the GTIOC2A pin is assigned to P14. 0 1 0 0: Controls the output stop state on the assumption that the GTIOC2A pin is assigned to PB6. 0 1 0 1: Controls the output stop state on the assumption that the GTIOC2A pin is assigned to PK0. Settings other than the above are prohibited.	GPTW2-A (GTIOC2A) pin select bits b3 b0 0 0 0 0: Does not control the output stop state for any GTIOC2A pin. 0 0 0 1: Controls the output stop state on the assumption that the GTIOC2A pin is assigned to P73. 0 0 1 0: Controls the output stop state on the assumption that the GTIOC2A pin is assigned to PD3. 0 1 0 0: Controls the output stop state on the assumption that the GTIOC2A pin is assigned to PB6. Settings other than the above are prohibited.
	G2BSEL[3:0]	GPTW2-B (GTIOC2B) pin select bits b7 b4 0 0 0 0: Does not control the output stop state for any GTIOC2B pin. 0 0 0 1: Controls the output stop state on the assumption that the GTIOC2B pin is assigned to P76. 0 0 1 0: Controls the output stop state on the assumption that the GTIOC2B pin is assigned to PD2. 0 0 1 1: Controls the output stop state on the assumption that the GTIOC2B pin is assigned to P17. 0 1 0 0: Controls the output stop state on the assumption that the GTIOC2B pin is assigned to PB5. 0 1 0 1: Controls the output stop state on the assumption that the GTIOC2B pin is assigned to PK1. Settings other than the above are prohibited.	GPTW2-B (GTIOC2B) pin select bits b7 b4 0 0 0 0: Does not control the output stop state for any GTIOC2B pin. 0 0 0 1: Controls the output stop state on the assumption that the GTIOC2B pin is assigned to P76. 0 0 1 0: Controls the output stop state on the assumption that the GTIOC2B pin is assigned to PD2. 0 1 0 0: Controls the output stop state on the assumption that the GTIOC2B pin is assigned to PB5. Settings other than the above are prohibited.

Register	Bit	RX66T (POE3B)	RX26T (POE3D)
G3SELR	G3ASEL[3:0]	GPTW3-A (GTIOC3A) pin select bits b3 b0 0 0 0 0: Does not control the output stop state for any GTIOC3A pin. 0 0 0 1: Controls the output stop state on the assumption that the GTIOC3A pin is assigned to P32. 0 0 1 0: Controls the output stop state on the assumption that the GTIOC3A pin is assigned to PD1. 0 0 1 1: Controls the output stop state on the assumption that the GTIOC3A pin is assigned to PE5. 0 1 0 0: Controls the output stop state on the assumption that the GTIOC3A pin is assigned to PD7. Settings other than the above are prohibited.	PTW3-A (GTIOC3A) pin select bits b3 b0 0 0 0 0: Does not control the output stop state for any GTIOC3A pin. 0 0 0 1: Controls the output stop state on the assumption that the GTIOC3A pin is assigned to P32. 0 0 1 0: Controls the output stop state on the assumption that the GTIOC3A pin is assigned to PD1. 0 0 1 1: Controls the output stop state on the assumption that the GTIOC3A pin is assigned to PE5. 0 1 0 0: Controls the output stop state on the assumption that the GTIOC3A pin is assigned to PD7. 0 1 0 1: Controls the output stop state on the assumption that the GTIOC3A pin is assigned to PB6. 0 1 1 0: Controls the output stop state on the assumption that the GTIOC3A pin is assigned to P10. Settings other than the above are prohibited.

Register	Bit	RX66T (POE3B)	RX26T (POE3D)
G3SELR	G3BSEL[3:0]	GPTW3-B (GTIOC3B) pin select bits b7 b4 0 0 0 0: Does not control the output stop state for any GTIOC3B pin. 0 0 0 1: Controls the output stop state on the assumption that the GTIOC3B pin is assigned to P33. 0 0 1 0: Controls the output stop state on the assumption that the GTIOC3B pin is assigned to PD0. 0 0 1 1: Controls the output stop state on the assumption that the GTIOC3B pin is assigned to P11. 0 1 0 0: Controls the output stop state on the assumption that the GTIOC3B pin is assigned to PD6. Settings other than the above are prohibited.	GPTW3-B (GTIOC3B) pin select bits b7 b4 0 0 0 0: Does not control the output stop state for any GTIOC3B pin. 0 0 0 1: Controls the output stop state on the assumption that the GTIOC3B pin is assigned to P33. 0 0 1 0: Controls the output stop state on the assumption that the GTIOC3B pin is assigned to PD0. 0 0 1 1: Controls the output stop state on the assumption that the GTIOC3B pin is assigned to P11. 0 1 0 0: Controls the output stop state on the assumption that the GTIOC3B pin is assigned to PD6. 0 1 0 1: Controls the output stop state on the assumption that the GTIOC3B pin is assigned to PB5. Settings other than the above are prohibited.
G7SELR	G7BSEL[3:0]	GPTW7-A (GTIOC7A) pin select bits b3 b0 0 0 0 0: Does not control the output stop state for any GTIOC7A pin. 0 0 0 1: Controls the output stop state on the assumption that the GTIOC7A pin is assigned to P95. 0 0 1 0: Controls the output stop state on the assumption that the GTIOC7A pin is assigned to P12. Settings other than the above are prohibited.	GPTW7-A (GTIOC7A) pin select bits b3 b0 0 0 0 0: Does not control the output stop state for any GTIOC7A pin. 0 0 0 1: Controls the output stop state on the assumption that the GTIOC7A pin is assigned to P95. 0 0 1 0: Controls the output stop state on the assumption that the GTIOC7A pin is assigned to PB2. 0 0 1 1: Controls the output stop state on the assumption that the GTIOC7A pin is assigned to P32. 0 1 0 0: Controls the output stop state on the assumption that the GTIOC7A pin is assigned to PD5. Settings other than the above are prohibited.

Register	Bit	RX66T (POE3B)	RX26T (POE3D)
G7SELR	G7ASEL[3:0]	GPTW7-B (GTIOC7B) pin select bits b7 b4 0 0 0 0: Does not control the output stop state for any GTIOC7B pin. 0 0 0 1: Controls the output stop state on the assumption that the GTIOC7B pin is assigned to P92. 0 0 1 0: Controls the output stop state on the assumption that the GTIOC7B pin is assigned to P15. Settings other than the above are prohibited.	GPTW7-B (GTIOC7B) pin select bits b7 b4 0 0 0 0: Does not control the output stop state for any GTIOC7B pin. 0 0 0 1: Controls the output stop state on the assumption that the GTIOC7B pin is assigned to P92. 0 0 1 0: Controls the output stop state on the assumption that the GTIOC7B pin is assigned to PB1. 0 0 1 1: Controls the output stop state on the assumption that the GTIOC7B pin is assigned to P33. 0 1 0 0: Controls the output stop state on the assumption that the GTIOC7B pin is assigned to PD3. Settings other than the above are prohibited.
G8SELR	—	GPTW8 pin select register	—
G9SELR	—	GPTW9 pin select register	—
IMCR0	—	—	Input signal mask control register 0
IMCR1	—	—	Input signal mask control register 1
IMCR2	—	—	Input signal mask control register 2
IMCR3	—	—	Input signal mask control register 3
IMCR4	—	—	Input signal mask control register 4
IMCR5	—	—	Input signal mask control register 5
IMCR6	—	—	Input signal mask control register 6
IMCR9	—	—	Input signal mask control register 9
IMCR10	—	—	Input signal mask control register 10
IMCR11	—	—	Input signal mask control register 11
IMCR12	—	—	Input signal mask control register 12
IMCR13	—	—	Input signal mask control register 13
IMCR14	—	—	Input signal mask control register 14

2.16 General Purpose PWM Timer

Table 2.51 is Comparative Overview of General PWM Timers, and Table 2.52 is Comparison of General Purpose PWM Timer Registers.

Table 2.51 Comparative Overview of General PWM Timers

Item	RX66T (GPTW)	RX26T (GPTWa)
Functions	• 32 bits × 10 channels • Up-counting or down-counting (saw waves) and up/down-counting (triangle waves) selectable for each counter • Independent lock sources selectable for each channel • Two input/output pins provided for each channel • Two output compare/input capture registers provided for each channel • For the two output compare/input capture registers for each channel, four buffer registers are provided and they can operate as comparison registers when buffering is not in use. • In output compare operation, buffer operation is possible at crests and troughs, and laterally asymmetric PWM waveforms are generated. • A register for setting up frame cycles is provided for each channel (interrupts can be generated at overflow or underflow). • Dead time can be generated during PWM operation. • Simultaneous start, stop, and clearing of any channel counters • Count start, count stop, counter clearing, up-counting, down-counting, and input capture operations can be triggered by a maximum of eight ELC events specified in the ELS settings. • Count start, count stop, counter clearing, up-counting, down-counting, and input capture operations can be performed by detection of the condition of two input signals. • Count start, count stop, counter clearing, up-counting, down-counting, and input capture operations can be triggered by a maximum of four external triggers.	• 32 bits × 8 channels • Up-counting or down-counting (saw waves) and up/down-counting (triangle waves) selectable for each counter • Independent lock sources selectable for each channel • Two input/output pins provided for each channel • Two output compare/input capture registers provided for each channel • For the two output compare/input capture registers for each channel, four buffer registers are provided and they can operate as comparison registers when buffering is not in use. • In output compare operation, buffer operation is possible at crests and troughs, and laterally asymmetric PWM waveforms are generated. • A register for setting up frame cycles is provided for each channel (interrupts can be generated at overflow or underflow). • Dead time can be generated during PWM operation. • A high precision duty cycle of near 100% and 0% of the PWM output can be generated. • In output compare operation, PWM waveforms can be generated by immediately applying the compare register settings to provide dead times. • Simultaneous start, stop, and clearing of any channel counters • Count start, count stop, counter clearing, up-counting, down-counting, and input capture operations can be triggered by a maximum of eight ELC events specified in the ELS settings. • Count start, count stop, counter clearing, up-counting, down-counting, and input capture operations can be performed by detection of the condition of two input signals. • Count start, count stop, counter clearing, up-counting, down-counting, and input capture operations can be triggered by a maximum of four external triggers.

Item	RX66T (GPTW)	RX26T (GPTWa)
Functions	• Function to control output negation due to output stop requests from the POEG • Function to generate A/D converter start trigger • Event signals for compare match A to F and for underflow or overflow can be output to the ELC. • The noise filter function can be selected for input capture input. • Bus clock: PCLKA, GPTW count reference clock: PCLKC PCLKA to PCLKC frequency ratio = 1:N (N = 1/2)	• Function to control output negation due to dead time errors or output stop requests from the POEG • Function to generate A/D converter start trigger • Event signals for compare match A to F and for underflow or overflow can be output to the ELC. • The noise filter function can be selected for input capture input. • Cycle count function • Function for measuring the external input pulse width • Logical operations of compare match output are possible between channels. • Synchronized setting, clearing, and input capture can be performed between channels. • Bus clock: PCLKA, GPTWa count reference clock: PCLKC PCLKA to PCLKC frequency ratio = 1:N (N = 1/2)

Table 2.52 Comparison of General Purpose PWM Timer Registers

Register	Bit	RX66T (GPTW)	RX26T (GPTWa)
GTSTR	CSTRT8	Channel 8 count start bit	—
	CSTRT9	Channel 9 count start bit	—
GTSTP	CSTOP8	Channel 8 count stop bit	—
	CSTOP9	Channel 9 count stop bit	—
GTCLR	CCLR8	Channel 8 counter clear bit	—
	CCLR9	Channel 9 counter clear bit	—
GTSSR	—	General purpose PWM timer start source select register (n = 0 to 9)	General purpose PWM timer start source select register (n = 0 to 7)
GTPSR	—	General purpose PWM timer stop source select register (n = 0 to 9)	General purpose PWM timer stop source select register (n = 0 to 7)
GTCSR	—	General purpose PWM timer clear source select register (n = 0 to 9)	General purpose PWM timer clear source select register (n = 0 to 7)
	CSCMSC [2:0]	—	Compare Match/Input Capture/Synchronous Counter Clearing Source Counter Clear Enable bit
	CP1CCE	—	Counter clear enable bit at crest in complementary PWM mode 1
GTUPSR	—	General purpose PWM timer count-up source select register (n = 0 to 9)	General purpose PWM timer count-up source select register (n = 0 to 7)
	USILVL[3:0]	—	External input level source count-up enable bits
GTDNSR	—	General purpose PWM timer count-down source select register (n = 0 to 9)	General purpose PWM timer count-down source select register (n = 0 to 7)
	DSILVL[3:0]	—	External input level source count-down enable bits
GTICASR	—	General purpose PWM timer input capture source select register A (n = 0 to 9)	General purpose PWM timer input capture source select register A (n = 0 to 7)
	ASOC	—	GTCCRA input capture enable bit for other channel sources
GTICBSR	—	General purpose PWM timer input capture source select register B (n = 0 to 9)	General purpose PWM timer input capture source select register B (n = 0 to 7)
	BSOC	—	GTCCRB input capture enable bit for other channel sources
GTCR	ICDS	—	Bit for selecting input capture operation at count stop
	SCGTIOC	—	GTIOC input source simultaneous clearing enable bit
	SSOGRP [1:0]	—	Simultaneous setting or clearing group select bits
	CPSCD	—	Bit for disabling simultaneous clearing in complementary PWM mode
	SSCEN	—	Simultaneous setting or resetting enable bit

Register	Bit	RX66T (GPTW)	RX26T (GPTWa)
GTCR	MD[2:0] (RX66T) MD[3:0] (RX26T)	Mode select bits b18 b16 0 0 0: Saw-wave PWM mode (single buffer or double buffer possible) 0 0 1: Saw-wave one-shot pulse mode (fixed buffer operation) 0 1 0: Setting prohibited 0 1 1: Setting prohibited 1 0 0: Triangle-wave PWM mode 1 (32-bit transfer at trough) (single buffer or double buffer possible) 1 0 1: Triangle-wave PWM mode 2 (32-bit transfer at crest and trough) (single buffer or double buffer possible) 1 1 0: Triangle-wave PWM mode 3 (64-bit transfer at trough) (fixed buffer operation) 1 1 1: Setting prohibited	Mode select bits b19 b16 0 0 0 0: Saw-wave PWM mode 1 (single buffer or double buffer possible) 0 0 0 1: Saw-wave one-shot pulse mode (fixed buffer operation) 0 0 1 0: Saw-wave PWM mode 2 (single buffer or double buffer possible) 0 0 1 1: Setting prohibited. 0 1 0 0: Saw-wave PWM mode 1 (32-bit transfer at trough) (single buffer or double buffer possible) 0 1 0 1: Triangle-wave PWM mode 2 (32-bit transfer at crest and trough) (single buffer or double buffer possible) 0 1 1 0: Triangle-wave PWM mode 3 (64-bit transfer at trough) (fixed buffer operation) 0 1 1 1: Setting prohibited 1 0 0 0: Setting prohibited 1 0 0 1: Setting prohibited 1 0 1 0: Setting prohibited 1 0 1 1: Setting prohibited 1 1 0 0: Complementary PWM mode 1 (transfer at crest) 1 1 0 1: Complementary PWM mode 2 (transfer at trough) 1 1 1 0: Complementary PWM mode 3 (transfer at crest and trough) 1 1 1 1: Complementary PWM mode 4 (immediate transfer)

Register	Bit	RX66T (GPTW)	RX26T (GPTWa)
GTCR	TPCS[3:0]	Timer prescaler select bits b26 b23 0 0 0 0: PCLKC 0 0 0 1: PCLKC/2 0 0 1 0: PCLKC/4 0 0 1 1: PCLKC/8 0 1 0 0: PCLKC/16 0 1 0 1: PCLKC/32 0 1 1 0: PCLKC/64 0 1 1 1: Setting prohibited 1 0 0 0: PCLKC/256 1 0 0 1: Setting prohibited 1 0 1 0: PCLKC/1024 1 0 1 1: Setting prohibited 1 1 0 0: GTETRGA (via the POEG) 1 1 0 1: GTETRGB (via the POEG) 1 1 1 0: GTETRGC (via the POEG) 1 1 1 1: GTETRGD (via the POEG)	Timer prescaler select bits b26 b23 0 0 0 0: PCLKC 0 0 0 1: PCLKC/2 0 0 1 0: PCLKC/4 0 0 1 1: PCLKC/8 0 1 0 0: PCLKC/16 0 1 0 1: PCLKC/32 0 1 1 0: PCLKC/64 0 1 1 1: PCLKC/128 1 0 0 0: PCLKC/256 1 0 0 1: PCLKC/512 1 0 1 0: PCLKC/1024 1 0 1 1: Setting prohibited 1 1 0 0: GTETRGA (via the POEG) 1 1 0 1: GTETRGB (via the POEG) 1 1 1 0: GTETRGC (via the POEG) 1 1 1 1: GTETRGD (via the POEG)
	CKEG[1:0]	—	Clock edge select bits
GTUDDTYC	—	General purpose PWM timer count direction and duty setting register (n = 0 to 9)	General purpose PWM timer count direction and duty setting register (n = 0 to 7)
GTIOR	—	General purpose PWM timer I/O control register (n = 0 to 9)	General purpose PWM timer I/O control register (n = 0 to 7)
	CPSCIR	—	Bit for suppressing initial output for simultaneous clearing in complementary PWM mode
	OAEOCD	—	Bit for disabling output of the end of the cycle on a compare match in the GTCCRA register
	PSYE	—	PWM cycle simultaneous output enable bit
sGTINTAD	GTINTA	Interrupt enable bit on compare match or input capture in the GTCCRA register	—
	GTINTB	Interrupt enable bit on compare match or input capture in the GTCCRB register	—
	GTINTC	GTCCRC register compare match interrupt enable bit	—
	GTINTD	GTCCRD register compare match interrupt enable bit	—
	GTINTE	GTCCRE register compare match interrupt enable bit	—
	GTINTF	GTCCRF register compare match interrupt enable bit	—
	GTINTPR [1:0]	GTPR register compare match interrupt enable bits	—
	SCFA	—	GTCCRA Register Compare Match/Input Capture Source Synchronous Clear Enable bit

Register	Bit	RX66T (GPTW)	RX26T (GPTWa)
sGTINTAD	SCFB	—	GTCCRB Register Compare Match/Input Capture Source Synchronous Clear Enable bit
GTINTAD	SCFC	—	GTCCRC Register Compare Match/Source Synchronous Clear Enable bit
	SCFD	—	GTCCRD Register Compare Match/Source Synchronous Clear Enable bit
	SCFE	—	GTCCRE Register Compare Match/Source Synchronous Clear Enable bit
	SCFF	—	GTCCRF Register Compare Match/Source Synchronous Clear Enable bit
	SCFPO	—	Bit for enabling simultaneous clearing due to overflow
	SCFPU	—	Bit for enabling simultaneous clearing due to underflow
	GTINTPC	—	Cycle count function end interrupt enable bit
GTST	TCFA	—	Compare match/input capture flag A
	TCFB	—	Compare match/input capture flag B
	TCFC	—	Compare match flag C
	TCFD	—	Compare match flag D
	TCFE	—	Compare match flag E
	TCFF	—	Compare match flag F
	TCFPO	—	Overflow flag
	TCFPU	—	Underflow flag
	PCF	—	Cycle count function end flag
GTBER	DBRTSCA	—	Bit for selecting the repeat operation period for the GTCCRA register double buffer
	DBRTSCB	—	Bit for selecting the repeat operation period for the GTCCRB register double buffer
	DBRTEADA	—	Bit for enabling repeat operation of the GTADTRA register double buffer
	DBRTSADA	—	Bit for selecting the repeat period for the GTADTRA register double buffer
	DBRTEADB	—	Bit for enabling repeat operation of the GTADTRB register double buffer
	DBRTSADB	—	Bit for selecting the repeat period for the GTADTRB register double buffer

Register	Bit	RX66T (GPTW)	RX26T (GPTWa)
GTBER	ADTTA[1:0]	GTADTRA register buffer transfer timing select bits • For triangle waves b25 b24 0 0: No transfer 0 1: Transfer at trough 1 0: Transfer at crest 1 1: Transfer at crest and trough • For sawtooth waves b25 b24 0 0: No transfer Other than 0 0: Transfer at underflow (for counting-down) or overflow (for counting-up), or when the counter is cleared	GTADTRA register buffer transfer timing select bits • For triangle waves and complementary PWM mode b25 b24 0 0: No transfer 0 1: Transfer at trough 1 0: Transfer at crest 1 1: Transfer at crest and trough • For sawtooth waves b25 b24 0 0: No transfer Other than 0 0: Transfer at underflow (for counting-down) or overflow (for counting-up), or when the counter is cleared
	ADTTB[1:0]	GTADTRB register buffer transfer timing select bits • For triangle waves b29 b28 0 0: No transfer 0 1: Transfer at trough 1 0: Transfer at crest 1 1: Transfer at crest and trough • For sawtooth waves b29 b28 0 0: No transfer Other than 0 0: Transfer at underflow (for counting-down) or overflow (for counting-up), or when the counter is cleared	GTADTRB register buffer transfer timing select bits • For triangle waves and complementary PWM mode b29 b28 0 0: No transfer 0 1: Transfer at trough 1 0: Transfer at crest 1 1: Transfer at crest and trough • For sawtooth waves b29 b28 0 0: No transfer Other than 0 0: Transfer at underflow (for counting-down) or overflow (for counting-up), or when the counter is cleared
GTICLF	—	—	Register for logical operations between general purpose PWM timer channels
GTPC	—	—	General purpose PWM timer cycle count register
GTADCMSC	—	—	General purpose PWM timer A/D conversion start request compare match skipping setting register
GTADCMSS	—	—	General purpose PWM timer A/D conversion start request compare match skipping setting register
GTSECSR	SECSEL8	Simultaneous control channel select bit for channel 8 operation enable bit	—
	SECSEL9	Simultaneous control channel select bit for channel 9 operation enable bit	—

Register	Bit	RX66T (GPTW)	RX26T (GPTWa)
GTSECR	SPCE	—	Cycle count function simultaneous enable bit
	SSCE	—	Simultaneous setting and clearing enable bit
	SPCD	—	Cycle count function simultaneous disable bit
	SSCD	—	Simultaneous setting and clearing disable bit
GTBER2	—	—	General purpose PWM timer buffer enable register 2
GTOLBR	—	—	General purpose PWM timer output level buffer register
GTICCR	—	—	Input capture control register for linkage between general purpose PWM timer channels
OPSCR	—	—	Output phase switch control register

2.17 High Resolution PWM Waveform Generation Circuit

Table 2.53 is Comparative Overview of High Resolution PWM Waveform Generation Circuits.

Table 2.53 Comparative Overview of High Resolution PWM Waveform Generation Circuits

Item	RX66T (HRPWM)	RX26T (HRPWM)
Functions	• High-resolution waveforms generated from complementary PWM waveforms of a maximum of four channels • The DLL (Delay Locked Loop) circuit implements high resolution with 1/32 (minimum of approximately 195 ps) of PCLKC cycle. • The rising and falling timing of PWM waveforms can be adjusted independently. • Waveforms generated by the GPTW by bypassing HRPWM can be output as they are.	• High-resolution waveforms generated from complementary PWM waveforms of a maximum of four channels • The DLL (Delay Locked Loop) circuit implements high resolution with 1/32 (minimum of approximately 260 ps) of PCLKC cycle. • The rising and falling timing of PWM waveforms can be adjusted independently. • Waveforms generated by the GPTW by bypassing HRPWM can be output as they are.
Operating frequency (f(PCLKC))	8 MHz to 160 MHz	8 MHz to 120 MHz

2.18 Port Output Enable for GPTWa

Table 2.54 is Comparative Overview of Port Output Enable for GPTWa, and Table 2.55 is Comparison of Port Output Enable Registers for GPTWa.

Table 2.54 Comparative Overview of Port Output Enable for GPTWa

Item	RX66T (POEG)	RX26T (POEG)
Stop request due to input level or edge detection	• When the POEGGn.PIDF flag is set due to input level detection of the GTETRGn pins (n = A to D), an output stop request is issued to the GPTW. • An output stop request is directly issued to the GPTW after input level detection of the GTETRGn pins.	• When the POEGGn.PIDF flag is set due to input level or edge detection of the GTETRGn pins (n = A to D), an output stop request is issued to the GPTWa. • An output stop request is directly issued to the GPTWa after input level detection of the GTETRGn pins.
Stop request by an output stop signal from GPTW (RX66T) or GPTWa (RX26T)	• When the GPTW detects simultaneous active level (high or low level) on the GTIOCA and GTIOCB pins and the POEGGn.IOCF flag is set, an output stop request is issued to the GPTW. • When the GPTW detects a dead time error and the POEGGn.IOCF flag is set, an output stop request is issued to the GPTW.	• When the GPTWa detects simultaneous active level (high or low level) on the GTIOCA and GTIOCB pins and the POEGGn.IOCF flag is set, an output stop request is issued to the GPTWa. • When the GPTWa detects a dead time error and the POEGGn.IOCF flag is set, an output stop request is issued to the GPTWa.
Stop request due to comparator detection	• When the POEGGn.IOCF flag is set due to comparator edge detection, an output stop request is issued to the GPTW. • An output stop request is directly issued to the GPTW based on the comparator level detection.	• When the POEGGn.IOCF flag is set due to comparator edge detection, an output stop request is issued to the GPTWa. • An output stop request is directly issued to the GPTWa based on the comparator level detection. • Whether to enable or disable the output stop request is controlled based on the PWM output level from the GPTW selected with the POEGICRn.MSEL[4:0] bits.
Stop request due to oscillation stop detection	When the oscillation stop detection circuit for the main clock detects a stop state and the POEGGn.OSTPF flag is set, an output stop request is issued to the GPTW.	When the oscillation stop detection circuit for the main clock detects a stop state and the POEGGn.OSTPF flag is set, an output stop request is issued to the GPTWa.
Stop request by software	An output stop request is issued to the GPTW by setting the POEGGn.SSF flag with software.	An output stop request is issued to the GPTWa by setting the POEGGn.SSF flag with software.
Interrupts	• An interrupt is generated in response to a stop request by setting the POEGGn.PIDF flag. • An interrupt is generated in response to a stop request by setting the POEGGn.IOCF flag.	• An interrupt is generated in response to a stop request by setting the POEGGn.PIDF flag. • An interrupt is generated in response to a stop request by setting the POEGGn.IOCF flag.

Item	RX66T (POEG)	RX26T (POEG)
External trigger output to the GPTW (RX66T) and GPTWa (RX26T)	GTETRGn pins output external triggers to the GPTW.	GTETRGn pins output external triggers to the GPTWa.
Noise cancellation	• The GTETRGn pins incorporate digital noise filters. • One of four sampling clocks can be selected.	• The GTETRGn pins incorporate digital noise filters. • One of eight sampling clocks can be selected. • The sampling count can be specified in the range from 3 to 6.

Table 2.55 Comparison of Port Output Enable Registers for GPTWa

Register	Bit	RX66T (POEG)	RX26T (POEG)
POEGGn	NFPSC	—	Noise filter clock select bit
	ELSEL	—	GTETRGn input edge level detection select bit
	NFSN[1:0]	—	Noise filter sampling count select bits
	NFCS[1:0]	Noise filter clock select bits b31 b30 0 0: Samples the input level of the GTETRGn pin 3 times at PCLKB/1 clock pulses. 0 1: Samples the input level of the GTETRGn pin 3 times at PCLKB/8 clock pulses. 1 0: Samples the input level of the GTETRGn pin 3 times at PCLKB/32 clock pulses. 1 1: Samples the input level of the GTETRGn pin 3 times at PCLKB/128 clock pulses.	Noise filter clock select bits <When the NFPSC bit is set to 0> b31 b30 0 0: Samples the input level of the GTETRGn pin at PCLK_GPTn/1 clock pulses. 0 1: Samples the input level of the GTETRGn pin at PCLK_GPTn/8 clock pulses. 1 0: Samples the input level of the GTETRGn pin at PCLK_GPTn/32 clock pulses. 1 1: Samples the input level of the GTETRGn pin at PCLK_GPTn/128 clock pulses. <When the NFPSC bit is set to 1> b31 b30 0 0: Samples the input level of the GTETRGn pin at PCLK_GPTn/2 clock pulses. 0 1: Samples the input level of the GTETRGn pin at PCLK_GPTn/4 clock pulses. 1 0: Samples the input level of the GTETRGn pin at PCLK_GPTn/16 clock pulses. 1 1: Samples the input level of the GTETRGn pin at PCLK_GPTn/64 clock pulses.
POEGICRn	—	—	POEG group n input control register (n = A to D)
GTONCCRn	MSEL[4:0]	—	Negation control disable signal select bits

2.19 Independent Watchdog Timer

Table 2.56 is Comparative Overview of Independent Watchdog Timers, and Table 2.57 is Comparison of Independent Watchdog Timer Registers.

Table 2.56 Comparative Overview of Independent Watchdog Timers

Item	RX66T (IWDTa)	RX26T (IWDTa)
Count source	IWDT-dedicated clock (IWDTCLK)	IWDT-dedicated clock (IWDTCLK)
Clock division ratio	Divided by 1, 16, 32, 64, 128, or 256	Divided by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Auto-start mode: Counting starts automatically after a reset. • Register start mode: Counting is started by refreshing the counter (writing 00h and then FFh to the IWDTRR register).	• Auto-start mode: Counting starts automatically after a reset. • Register start mode: Counting is started by refreshing the counter (writing 00h and then FFh to the IWDTRR register).
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • Low power consumption state (by means of register setting) • Underflow or refresh error (register start mode only)	• Reset (the down-counter and other registers return to their initial values) • Low power consumption state (by means of register setting) • Underflow or refresh error (register start mode only)
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods).	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods).
Reset output sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt and interrupt sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read by reading the IWDTSR register.	The down-counter value can be read by reading the IWDTSR register.
Event link function (output)	• Down-counter underflow event output • Refresh error event output	• Down-counter underflow event output • Refresh error event output
Output signals (internal signals)	• Reset output • Interrupt request output • Sleep mode count stop control output	• Reset output • Interrupt request output • Sleep mode count stop control output

Item	RX66T (IWDTa)	RX26T (IWDTa)
Auto-start mode (controlled by option function select register 0 (OFS0))	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0]bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at a transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0]bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at a transition to sleep mode, software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)
Register start mode (controlled by the IWDT registers)	• Selecting the clock frequency division ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at a transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)	• Selecting the clock frequency division ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at a transition to sleep mode, software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)

Table 2.57 Comparison of Independent Watchdog Timer Registers

Register	Bit	RX66T (IWDTa)	RX26T (IWDTa)
IWDTCSTPR	SLCSTP	Sleep mode count stop control bit 0: Counting stop is disabled. 1: Counting stop is enabled at a transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode.	Sleep mode count stop control bit 0: Counting stop is disabled. 1: Counting stop is enabled at a transition to sleep mode, software standby mode, or all-module clock stop mode.

2.20 Serial Communications Interface

Table 2.58 is Comparative Overview of Serial Communications Interfaces, Table 2.59 is Comparison of Serial Communications Interface Channels, and Table 2.60 is Comparison of Serial Communications Interface Registers.

Table 2.58 Comparative Overview of Serial Communications Interfaces

Item		RX66T (SCIj, SCIi, SCIh)	RX26T (SCIk, SCIh)
Serial communications modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator	Bit rate specifiable by on-chip baud rate generator
Full-duplex communication		• Transmitter: Continuous transmission is possible by using the double-buffer structure. • Receiver: Continuous reception is possible by using the double-buffer structure.	• Transmitter: Continuous transmission is possible by using the double-buffer structure. • Receiver: Continuous reception is possible by using the double-buffer structure.
Data transfer		Selectable as LSB first or MSB first transfer	Selectable as LSB first or MSB first transfer
I/O signal level inversion		—	The levels of input and output signals can be inverted independently (SCI1, SCI5, and SCI6).
Interrupt sources		• Transmit end, transmit data empty, receive data full, receive error, receive data ready (SCI11), and data match (SCI1, SCI5, SCI6, SCI8, SCI9, SCI11) • Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)	• Transmit end, transmit data empty, receive data full, receive error, and data match (SCI1, SCI5, SCI6) • Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)
Low power consumption function		Transition to the module stop state is possible for each channel.	Transition to the module stop state is possible for each channel.
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection function	Parity error, overrun error, and framing error	Parity error, overrun error, and framing error
	Hardware overflow control	CTSn# and RTSn# pins can be used in controlling transmission and reception.	CTSn# and RTSn# pins can be used in controlling transmission and reception.
	Transmit/receive FIFO	Ability to use 16-stage FIFOs for transmission and reception (SCI11)	—
	Data match detection	Compares the received data and the comparison data register, and generates an interrupt request when they match (SCI1, SCI5, SCI6, SCI8, SCI9, and SCI11).	Compares the received data and the comparison data register, and generates an interrupt request when they match (SCI1, SCI5, and SCI6).
	Start-bit detection	Low level or falling edge is selectable.	Low level or falling edge is selectable.

Item		RX66T (SCIj, SCIi, SCIh)	RX26T (SCIk, SCIh)
Asynchronous mode	Receive data sampling timing adjustment	—	The receive data sampling point can be shifted from the center of the data forward or backward to a base point (SCI1, SCI5, SCI6).
	Transmit signal change timing adjustment	—	Either the falling or rising edge of the transmit data can be delayed (SCI1, SCI5, and SCI6).
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly or by reading the SPTR.RXDMON flag.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly or by reading the SPTR.RXDMON flag.
	Clock source	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5, SCI6, and SCI12).	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5, SCI6, and SCI12).
	Double-speed mode	Baud rate generator double-speed mode can be selected.	Baud rate generator double-speed mode can be selected.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise elimination function	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware overflow control	CTSn# and RTSn# pins can be used in controlling transmission and reception.	CTSn# and RTSn# pins can be used in controlling transmission and reception.
	Transmit/ receive FIFO	Ability to use 16-stage FIFOs for transmission and reception (SCI11)	—
Smart card interface mode	Error processing	• An error signal can be automatically transmitted when a parity error is detected during reception. • Data is automatically retransmitted when an error signal is received during transmission.	• An error signal can be automatically transmitted when a parity error is detected during reception. • Data can be automatically retransmitted when an error signal is received during transmission.
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	I^2C bus format	I^2C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer speed	Fast mode is supported.	Fast mode is supported.
	Noise cancellation	• The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters. • The interval for noise cancellation is adjustable.	• The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters. • The interval for noise cancellation is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.

Item		RX66T (SCIj, SCIi, SCIh)	RX26T (SCIk, SCIh)
Simple SPI mode	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.
Extended serial mode (supported by SCI12 only)	Start frame transmission	• Output of break field low width and generation of interrupt on completion of output • Detection of bus collision and generation of interrupt on detection	• Output of break field low width and generation of interrupt on completion of output • Detection of bus collision and generation of interrupt on detection
	Start frame reception	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Two kinds of data for comparison (primary and secondary) can be set in Control Field 1. • A priority interrupt bit can be set in Control Field 1. • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Two kinds of data for comparison (primary and secondary) can be set in Control Field 1. • A priority interrupt bit can be set in Control Field 1. • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates
	I/O control function	• Polarity can be selected for TXDX12 and RXDX12 signals. • Digital filtering can be specified for the RXDX12 signal. • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Receive data sampling timing of RXDX12 pin can be selected.	• Polarity can be selected for TXDX12 and RXDX12 signals. • Digital filtering can be specified for the RXDX12 signal. • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Receive data sampling timing of RXDX12 pin can be selected.
	Timer function	Usable as reloading timer	Usable as reloading timer
Bit rate modulation function		Correction of outputs from the on-chip baud rate generator can reduce errors.	Correction of outputs from the on-chip baud rate generator can reduce errors.
Event link function (supported by SCI5 only)		• Error (receive error or error signal detection) event output • Receive buffer full event output • Transmit data empty event output • Transmit end event output	• Error (receive error or error signal detection) event output • Receive buffer full event output • Transmit data empty event output • Transmit end event output

Table 2.59 Comparison of Serial Communications Interface Channels

Item	RX66T (SCIj, SCIi, SCIh)	RX26T (SCIk, SCIh)
Asynchronous mode	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12	SCI1, SCI5, SCI6, SCI12
Clock synchronous mode	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12	SCI1, SCI5, SCI6, SCI12
Smart card interface mode	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12	SCI1, SCI5, SCI6, SCI12
Simple I^2C mode	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12	SCI1, SCI5, SCI6, SCI12
Simple SPI mode	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12	SCI1, SCI5, SCI6, SCI12
FIFO mode	SCI11	—
Data match detection	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11	SCI1, SCI5, SCI6
Extended serial mode	SCI12	SCI12
TMR clock input	SCI5, SCI6, SCI12	SCI5, SCI6, SCI12
Event link function	SCI5	SCI5
Peripheral module clock	PCLKB: SCI1, SCI5, SCI6, SCI8,SCI9, SCI12 PCLKA: SCI11	PCLKB

Table 2.60 Comparison of Serial Communications Interface Registers

Register	Bit	RX66T (SCIj, SCIi, SCIh)	RX26T (SCIk, SCIh)
FRDR	—	Receive FIFO data register	—
FTDR	—	Transmit FIFO data register	—
SEMR	ITE	—	Immediate transmission enable bit*1
FCR	—	FIFO control register	—
FDR	—	FIFO data count register	—
LSR	—	Line status register	—
SPTR	RXDMON	RXD line monitoring flag 0: RXDn pin is at the low level. 1: RXDn pin is at the high level.	RXD line monitoring flag When the RINV bit is set to 0: 0: RXDn pin is at the low level. 1: RXDn pin is at the high level. When the RINV bit is set to 1: 0: RXDn pin is at the high level. 1: RXDn pin is at the low level.
	SPB2DT SPB2IO	Serial port break data bit Serial port break input/output bit The TXDn pins are controlled by combining the SCR.TE bit, SPB2DT bit, and SPB2IO bit.	Serial port break data bit Serial port break input/output bit The TXDn pins are controlled by combining the SCR.TE bit, SPB2DT bit, SPB2IO bit, and TINV bit.
	RINV	—	Receiver input invert bit
	TINV	—	Transmission output inversion bit
	RTADJ	—	Receive data sampling timing adjustment bit
	TTADJ	—	Transmit signal change timing adjustment bit
TMGR	—	—	Transmit/receive timing select register
PRDFR0	—	—	Product function select register 0

Note: 1. This bit is reserved in SCI12. This bit is read as 0. The write value should be 0.

2.21 CAN Module and CAN FD Module

Table 2.61 is Comparative Overview of CAN Module and CAN FD Module, and Table 2.62 is Comparison of CAN Module Registers and CAN FD Module Registers.

Table 2.61 Comparative Overview of CAN Module and CAN FD Module

Item	RX66T (CAN)	RX26T (CANFD)
Protocol	Conforming to the SO 11898-1 standard (standard frame or extension frame)	Conforming to the ISO 11898-1:2015 specifications
Bit rate (RX66T) Data transfer rate (RX26T)	Programming is possible with a maximum bit rate of 1 Mbps (fCAN ≥ 8 MHz). fCAN: CAN clock source	Arbitration phase: Maximum of 1 Mbps Data phase: Maximum of 8 Mbps*1
Operating frequency	PCLKB: 60 MHz (max.) CANMCLK: 24 MHz (max.)	Register block: Maximum of 60 MHz (PCLKB) Message buffer RAM: Maximum of 120 MHz (PCLKA)
Operating clock (DLL clock) for data link layer	—	Maximum of 60 MHz (either CANFDMCLK or CANFDCLK can be selected)
Message box (RX66T) Message buffer (RX26T)	32 mailboxes: Two mailbox modes can be selected. • Normal mailbox mode: 32 mailboxes can be configured for transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for transmission or reception. Of the other mailboxes, four FIFO stages can be configured for transmission and four FIFO stages for reception.	• 32 receive message buffers • Four transmit message buffers • One transmit queue Automatic transfer of messages to the transmit queue is supported.
Frame type	• Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID) • Remote frame in base format (11-bit ID) • Remote frame in extended format (29-bit ID)	Classic CAN (CAN 2.0) • Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID) • Remote frame in base format (11-bit ID) • Remote frame in extended format (29-bit ID) CAN FD*1 • Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID)

Item	RX66T (CAN)	RX26T (CANFD)
Reception	• Data frames and remote frames can be received. • The ID format to be received (base ID only, extended ID only, or both base ID and extended ID) can be selected. • The one-shot receive function can be selected. • Overwrite mode (message is overwritten) or overrun mode (message is discarded) can be selected. • Reception end interrupt can be enabled or disabled individually for each mailbox.	• Data frames and remote frames can be received. • The ID format to be received (base ID only, extended ID only, or both base ID and extended ID) can be selected. • Receive message buffer interrupt can be enabled or disabled individually for each message buffer.
Data length	0 to 8 bytes	Classic CAN: 0 to 8 bytes CAN FD: 0 to 8, 12, 16, 20, 24, 32, 48, and 64 bytes*1
Acceptance filter	• Eight acceptance masks (an individual mask for every four mailboxes) • Mailbox masks can be enabled or disabled individually.	Filtering is possible in the following fields: • IDE bit (base format, extended format, or both) • ID field • RTR bit (data frame or remote frame) (only for Classic CAN) • DLC field Data (data length) The protection function when the payload size is exceeded is provided. Acceptance filter list (AFL) entries can be updated during communication.
Transmission	• Data frames and remote frames can be sent. • The ID format to be sent (base ID only, extended ID only, or both base ID and extended ID) can be selected. • The one-shot transmission function can be selected. • Either ID priority transmission mode or mailbox number priority transmission mode can be selected. • Transmission requests can be aborted (completion of abort can be confirmed with a flag). • Transmission end interrupt can be enabled or disabled individually for each mailbox.	• Data frames and remote frames can be sent. • The ID format to be sent (base ID only or extended ID only) can be selected. • The one-shot transmission function can be selected. • Either ID priority transmission mode or message buffer number priority transmission mode can be selected. • Transmission requests can be aborted (completion of abort can be confirmed with a flag). • Channel transmission interrupt can be enabled and disabled.
FIFO	• 24 mailboxes can be configured for transmission or reception. • Of the other mailboxes, four FIFO stages can be configured for transmission and four FIFO stages for reception.	The FIFO size is programmable. • Two receive FIFOs • One common FIFO (Whether to use the FIFO as a receive FIFO or transmit FIFO can be selected.)

Item	RX66T (CAN)	RX26T (CANFD)
Automatic transmission interval adjustment	—	Available when the common FIFO is configured as a transmit FIFO The interval between messages sent from the FIFO can be adjusted.
Bus-off recovery method	How to recover from the bus-off state can be selected. • Conforming to the ISO 11898-1 standard • The mode automatically changes to CAN Halt mode when bus off starts. • The mode automatically changes to CAN Halt mode when bus off ends. • A program causes a transition to CAN Halt mode. • A program causes a transition to error active state.	How to recover from the bus-off state can be selected. • Normal mode (ISO 11898-1 compliant) • Automatically enters CH_HALT mode when bus off starts. • Automatically enters CH_HALT mode when bus off ends. • Software causes a transition CH_HALT mode (during bus-off recovery period). • A program causes a transition to error active state.
Timestamp function	• Timestamp function with a 16-bit counter • The reference clock can be selected from 1, 2, 4, and 8 bit time.	Transmission and reception timestamp function
Interrupt function	• Five types of interrupt sources (reception end interrupt, transmission end interrupt, receive FIFO interrupt, transmit FIFO interrupt, and error interrupt)	Receive FIFO interrupt Global error interrupt Channel transmission interrupt Channel error interrupt Common FIFO reception interrupt Receive message buffer interrupt
CAN sleep mode	Current consumption can be reduced by stopping the CAN clock.	Module start/stop function for each CAN node (CH_SLEEP mode and GL_SLEEP mode)
Error status monitoring	• CAN bus errors (stack error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored. • Change of the error status can be detected (error warning, error passive, bus-off start, and bus-off recovery). • The error counter can be read.	—
Software support	—	Label information is automatically added to received messages.
Software support units	Three software support unis • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support	

Item	RX66T (CAN)	RX26T (CANFD)
Test modes	Three test modes are provided for user evaluation: • Listen-only mode • Self test mode 0 (external loopback) • Self test mode 1 (internal loopback)	• Basic test mode • Listen-only mode • Self test mode 0 (external loopback mode) • Self test mode 1 (internal loopback mode)
Low power consumption function (RX66T) Power down function (RX26T)	Ability to specify module stop state	Module start/stop function for each CAN node (CH_SLEEP mode and GL_SLEEP mode) Ability to transition to module stop state
RAM	—	RAM with ECC protection

Note: 1. This is only available for products that support the CAN FD protocol.

Table 2.62 Comparison of CAN Module Registers and CAN FD Module Registers

Register	Bit	RX66T (CAN)	RX26T (CANFD)
CTLR	—	Control register	—
BCR	—	Bit configuration register	—
MKRk	—	Mask register k (k = 0 to 7)	—
FIDCR0 FIDCR1	—	FIFO receive ID comparison registers 0 and 1	—
MKIVLR	—	Mask disable register	—
MBj	—	Mailbox register j (j = 0 to 31)	—
MIER	—	Mailbox interrupt enable register	—
MCTLj	—	Message control register j (j = 0 to 3)	—
RFCR	—	Receive FIFO control register	—
RFPCR	—	Receive FIFO pointer control register	—
TFCR	—	Transmit FIFO control register	—
TFPCR	—	Transmit FIFO pointer control register	—
STR	—	Status register	—
MSMR	—	Mailbox search mode register	—
MSSR	—	Mailbox search status register	—
CSSR	—	Channel search support register	—
AFSR	—	Acceptance filter support register	—
EIER	—	Error interrupt enable register	—
EIFR	—	Error interrupt source decision register	—
RECR	—	Receive error count register	—
TECR	—	Transmit error count register	—
ECSR	—	Error code storage register	—
TSR	—	Timestamp register	—
TCR	—	Test control register	—
NBCR	—	—	Nominal bit rate configuration register
CHCR	—	—	Channel control register
CHSR	—	—	Channel status register
CHESR	—	—	Channel error status register
DBCR	—	—	Data bit rate configuration register
FDCFG	—	—	CAN FD configuration register
FDCTR	—	—	CAN FD control register
FDSTS	—	—	CAN FD status register
FDCRC	—	—	CAN FD CRC register
GCFG	—	—	Global configuration register
GCR	—	—	Global control register
GSR	—	—	Global status register
GESR	—	—	Global error status register
TISR	—	—	Transmit interrupt status register
TSCR	—	—	Timestamp counter register
AFCR	—	—	Acceptance filter list control register
AFCFG	—	—	Acceptance filter list configuration register
AFLn.IDR	—	—	Acceptance filter list n ID register (n = 0 to 15)
AFLn.MASK	—	—	Acceptance filter list n mask register (n = 0 to 15)

Register	Bit	RX66T (CAN)	RX26T (CANFD)
AFLn.PTR0	—	—	Acceptance filter list n pointer register 0 (n = 0 to 15)
AFLn.PTR1	—	—	Acceptance filter list n pointer register 1 (n = 0 to 15)
RMCR	—	—	Receive message buffer configuration register
RMNDR	—	—	Receive message buffer new data register
RFCRn	—	—	Receive FIFO n configuration register (n = 0 or 1)
RFSRn	—	—	Receive FIFO n status register (n = 0 or 1)
RFPCRn	—	—	Receive FIFO n pointer control register (n = 0, 1)
CFCR0	—	—	Common FIFO 0 configuration register
CFSR0	—	—	Common FIFO 0 status register
CFPCR0	—	—	Common FIFO 0 pointer control register
FESR	—	—	FIFO empty status register
FFSR	—	—	FIFO full status register
FMLSR	—	—	FIFO message lost status register
RFISR	—	—	Receive FIFO interrupt status register
DTCR	—	—	DMA transfer control register
DTSR	—	—	DMA transfer status register
TMCRn	—	—	Transmit message buffer n control register (n = 0 to 3)
TMSRn	—	—	Transmit message buffer n status register (n = 0 to 3)
TMTRSR0	—	—	Transmit message buffer transmission request status register 0
TMARSR0	—	—	Transmit message buffer transmission abort request status register 0
TMTCSR0	—	—	Transmit message buffer transmission completion status register 0
TMTASR0	—	—	Transmit message buffer transmission abort status register 0
TMIER0	—	—	transmission message buffer interrupt enable register 0
TQCR0	—	—	Transmit queue 0 configuration register
TQSR0	—	—	Transmit queue 0 status register
TQPCR0	—	—	Transmit queue 0 pointer control register
THCR	—	—	Transmission history configuration register
THSR	—	—	Transmission history status register
THACR0	—	—	Transmission history access register 0

Register	Bit	RX66T (CAN)	RX26T (CANFD)
THACR1	—	—	Transmission history access register 1
THPCR	—	—	Transmission history pointer control register
GRCR	—	—	Global reset control register
GTMCR	—	—	Global test mode configuration register
GTMER	—	—	Global test mode enable register
GFDCFG	—	—	Global CAN FD configuration register
GTMLKR	—	—	Global test mode lock key register
RTPARk	—	—	RAM test page access register k (k= 0 to 63)
AFIGSR	—	—	Acceptance filter list ignore entry setting register
AFIGER	—	—	Acceptance filter list ignore entry enable register
RMIER	—	—	Receive message buffer interrupt enable register
ECCSR	—	—	ECC control/status register
ECTMR	—	—	ECC test mode register
ECTDR	—	—	ECC decoder test data register
ECEAR	—	—	ECC error address register

2.22 Serial Peripheral Interface

Table 2.63 is Comparative Overview of Serial Peripheral Interfaces, and Table 2.64 is Comparison of Serial Peripheral Interface Registers.

Table 2.63 Comparative Overview of Serial Peripheral Interfaces

Item	RX66T (RSPIc)	RX26T (RSPId)
Number of channels	1 channel	1 channel
RSPI transfer functions	• Use of MOSI (Master out/slave in), MISO (Master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Communication modes: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK	• Use of MOSI (Master out/slave in), MISO (Master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Communication modes: Full-duplex or simplex (transmit-only or reception-only (in slave mode)) can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK
Data format	• Switching between MSB first and LSB first is possible. • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits). • Byte swapping of transmit and receive data is possible.	• Switching between MSB first and LSB first is possible. • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits). • Byte swapping of transmit and receive data is possible. • Ability to invert the logic level of transmit/receive data
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4). — Width at high level: 2 cycles of PCLK — Width at low level: 2 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4). — Width at high level: 2 cycles of PCLK — Width at low level: 2 cycles of PCLK
Buffer configuration	• Double buffer configuration for the transmit and receive buffers • 128 bits for the transmit and receive buffers	• Double buffer configuration for the transmit and receive buffers • 128 bits for the transmit and receive buffers

Item	RX66T (RSPIc)	RX26T (RSPId)
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection
SSL control function	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity
Control in master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • The following items can be specified for each command: — SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value can be specified in SSL negation. • RSPCK auto-stop function	• A transfer of up to eight commands can be executed sequentially in looped execution. • The following items can be specified for each command: — SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value can be specified in SSL negation. • RSPCK auto-stop function • The delay between data bytes can be shortened during burst transfers.
Interrupt sources	• Interrupt sources — Receive buffer full interrupt — Transmit buffer empty interrupt — Error interrupt (mode fault, overrun, underrun, or parity error) — Idle interrupt	• Interrupt sources — Receive buffer full interrupt — Transmit buffer empty interrupt — Error interrupt (mode fault, overrun, underrun, or parity error) — Idle interrupt — Communication end interrupt

Item	RX66T (RSPIc)	RX26T (RSPId)
Event link function (output)	• The following events can be output to the event link controller (RSPI0): — Receive buffer full events — Transmit buffer empty events — Error events (mode fault, overrun, underrun, and parity error) — Idle event — Transmit completion event	• The following events can be output to the event link controller (RSPI0): — Receive buffer full events — Transmit buffer empty events — Error events (mode fault, overrun, underrun, and parity error) — Idle event — Communication completion events
Other functions	• Function for initializing the RSPI • Loopback mode function	• Function for initializing the RSPI • Loopback mode function
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.64 Comparison of Serial Peripheral Interface Registers

Register	Bit	RX66T (RSPIc)	RX26T (RSPId)
SPSR	SPCF	—	Communication completion flag
SPDCR2	DINV	—	Transfer data invert bit
SPCR3	—	—	RSPI control register 3

2.23 12-Bit A/D Converter

Table 2.65 is Comparative Overview of 12-Bit A/D Converters, Table 2.66 is Comparison of 12-Bit A/D Converter Registers, Table 2.67 is Comparison of A/D Start Sources to be Set in ADSTRGR Register, and Table 2.68 is Comparison of A/D Start Sources to be Set in ADGCTRGR Register and ADGCTRGR2 Register.

Table 2.65 Comparative Overview of 12-Bit A/D Converters

Item	RX66T (S12ADH)	RX26T (S12ADHa)
Number of units	Three units (S12AD, S12AD1, and S12AD2)	Three units (S12AD, S12AD1, and S12AD2) (For products with a RAM capacity of 64 KB) Two units (S12AD and S12AD2) (For products with a RAM capacity of 48 KB)
Input channels	S12AD: 8 channels S12AD1: 8 channels S12AD2: 14 channels	S12AD: 4 channels S12AD1: 4 channels S12AD2: 14 channels
Extended analog function	Temperature sensor output, internal reference voltage (S12AD2 only)	Temperature sensor output, internal reference voltage (S12AD2 only)
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	0.9 µs per channel (when A/D conversion clock (ADCLK) = 60 MHz)	0.9 µs per channel (when A/D conversion clock (ADCLK) = 60 MHz)
A/D conversion clock	• Peripheral module clock PCLKB and A/D conversion clock ADCLK can be set so that the frequency division ratio should be one of the following. — PCLKB to ADCLK frequency ratio = 1:1, 2:1, 4:1, or 1:2 • ADCLK is set by using the clock generation circuit. • The A/D conversion clock (ADCLK) can operate at frequencies from a maximum of 60 MHz to a minimum of 8 MHz.	• Peripheral module clock PCLKB and A/D conversion clock ADCLK can be set so that the frequency division ratio should be one of the following. — PCLKB to ADCLK frequency ratio = 1:1, 2:1, 4:1, or 1:2 • ADCLK is set by using the clock generation circuit. • The A/D conversion clock (ADCLK) can operate at frequencies from a maximum of 60 MHz to a minimum of 8 MHz.

Item	RX66T (S12ADH)	RX26T (S12ADHa)
Data register	• 30 registers for analog input (S12AD: 8 registers, S12AD1: 8 registers, S12AD2: 14 registers), one register for A/D-converted data duplication in double trigger mode for each unit, and two registers for A/D-converted data duplication during extended operation in double trigger mode for each unit • One register for temperature sensor output (S12AD2) • One register for internal reference (S12AD2) • One register for self-diagnosis for each unit • The results of A/D conversion are stored in 12-bit A/D data registers. • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): — The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): — A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.	• 22 registers for analog input (S12AD: 4 registers, S12AD1: 4 registers, S12AD2: 14 registers), one register for A/D-converted data duplication in double trigger mode for each unit, and two registers for A/D-converted data duplication during extended operation in double trigger mode for each unit • One register for temperature sensor output (S12AD2) • One register for internal reference (S12AD2) • One register for self-diagnosis for each unit • The results of A/D conversion are stored in 12-bit A/D data registers. • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): — The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): — A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.
Operating mode	The operating mode can be set individually for each of three units. • Single scan mode: — A/D conversion is performed only once on arbitrarily selected analog input channels. — A/D conversion is performed only once on the temperature sensor output (S12AD2). — A/D conversion is performed only once on the internal reference voltage. (S12AD2) • Continuous scan mode: — A/D conversion is performed repeatedly on arbitrarily selected analog input channels.	The operating mode can be set individually for each of three units. • Single scan mode: — A/D conversion is performed only once on arbitrarily selected analog input channels. — A/D conversion is performed only once on the temperature sensor output (S12AD2). — A/D conversion is performed only once on the internal reference voltage. (S12AD2) • Continuous scan mode: — A/D conversion is performed repeatedly on arbitrarily selected analog input channels.

Item	RX66T (S12ADH)	RX26T (S12ADHa)
Operating mode	• Group scan mode: — Two (groups A and B) or three (groups A, B, and C) can be selected as the number of groups to be used. (Only the combination of groups A and B can be selected when the number of groups is two.) — Arbitrarily selected analog input channels, the temperature sensor output (S12AD2), and the internal reference voltage (S12AD2) are divided into two groups (group A and B) or three groups (group A, B, and C), and A/D conversion of the analog input selected on a group basis is performed only once. — The scanning start condition for groups A, B, and C (synchronous trigger) can be independently selected, allowing A/D conversion of each group to be started independently. • Group scan mode (with group priority control selected): — If a higher-priority group trigger is input during scanning of a lower-priority group, scanning of the lower-priority group stops and scanning of the higher-priority group starts. The priority order is group A (highest) > group B > group C (lowest). — Whether or not to restart scanning (rescan) of the lower-priority group after processing for the higher-priority group completes, is selectable. Rescan can also be set to start either from the first selected channel or from the channel on which A/D conversion did not complete.	• Group scan mode: — Two (groups A and B) or three (groups A, B, and C) can be selected as the number of groups to be used. (Only the combination of groups A and B can be selected when the number of groups is two.) — Arbitrarily selected analog input channels, the temperature sensor output (S12AD2), and the internal reference voltage (S12AD2) are divided into two groups (group A and B) or three groups (group A, B, and C), and A/D conversion of the analog input selected on a group basis is performed only once. — The scanning start condition for groups A, B, and C (synchronous trigger) can be independently selected, allowing A/D conversion of each group to be started independently. • Group scan mode (with group priority control selected): — If a higher-priority group trigger is input during scanning of a lower-priority group, scanning of the lower-priority group stops and scanning of the higher-priority group starts. The priority order is group A (highest) > group B > group C (lowest). — Whether or not to restart scanning (rescan) of the lower-priority group after processing for the higher-priority group completes, is selectable. Rescan can also be set to start either from the first selected channel or from the channel on which A/D conversion did not complete.
Conditions for A/D conversion start	• Software trigger • Synchronous trigger — Trigger by the multi-function timer pulse unit (MTU), 8-bit timer (TMR), or event link controller (ELC) • Asynchronous trigger — A/D conversion can be triggered by the external trigger ADTRG0# (S12AD), ADTRG1# (S12AD1), and ADTRG2# (S12AD2) pins (individually for each of three units).	• Software trigger • Synchronous trigger — Trigger by the multi-function timer pulse unit (MTU), general purpose PWM timer (GPTW), 8-bit timer (TMR), or event link controller (ELC) • Asynchronous trigger — A/D conversion can be triggered by the external trigger ADTRG0# (S12AD), ADTRG1# (S12AD1), and ADTRG2# (S12AD2) pins (individually for each of three units).

Item	RX66T (S12ADH)	RX26T (S12ADHa)
Functions	• Sample & hold function dedicated to channels (three channels for S12AD and three channels for S12AD1) (Constant sampling can be set.) • Variable sampling time (settable on a per-channel basis) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection assist function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers • Compare function (window A and window B) • Order of channel conversion can be specified for each unit. • Input signal amplification function using the programmable gain amplifier (3-channel single-ended input or pseudo-differential input can be selected for each unit.)	• Sample & hold function dedicated to channels (three channels for S12AD and three channels for S12AD1) (Constant sampling can be set.) • Variable sampling time (settable on a per-channel basis) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection assist function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers • Compare function (window A and window B) • Order of channel conversion can be specified for each unit. • Input signal amplification function using the programmable gain amplifier (3 channels for each unit)
Interrupt sources	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI, S12ADI, S12ADI1, or S12ADI2) can be generated on completion of single scan (individually for each of 3 units). • In double trigger mode, A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of double scan (individually for each of 3 units). • In group scan mode, an A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of group A scan, an A/D scan end interrupt request (S12GBADI, S12GBADI1, or S12GBADI2) for group B can be generated on completion of group B scan, and an A/D scan end interrupt request (S12GCADI, S12GCADI1, or S12GCADI2) for group C can be generated on completion of group C scan.	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI, S12ADI, S12ADI1, or S12ADI2) can be generated on completion of single scan (individually for each of 3 units). • In double trigger mode, A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of double scan (individually for each of 3 units). • In group scan mode, an A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of group A scan, an A/D scan end interrupt request (S12GBADI, S12GBADI1, or S12GBADI2) for group B can be generated on completion of group B scan, and an A/D scan end interrupt request (S12GCADI, S12GCADI1, or S12GCADI2) for group C can be generated on completion of group C scan.

Item	RX66T (S12ADH)	RX26T (S12ADHa)
Interrupt sources	• When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of a double scan of group A. A corresponding scan end interrupt request (S12GBADI/S12GCADI, S12GBADI1/S12GCADI1, or S12GBADI2/S12GCADI2) can be generated on completion of a group B or group C scan. • A compare interrupt request (S12CMPAI, S12CMPAI1, S12CMPAI2, S12CMPBI, S12CMPBI1, or S12CMPBI2) can be generated upon a match with the comparison condition for the digital compare function. • The S12ADI/S12ADI1/S12ADI2, S12GBADI/S12GBADI1/S12GBADI2, and S12GCADI/S12GCADI1/S12GCADI2 interrupts can activate the DMA controller (DMAC) or data transfer controller (DTC).	• When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of a double scan of group A. A corresponding scan end interrupt request (S12GBADI/S12GCADI, S12GBADI1/S12GCADI1, or S12GBADI2/S12GCADI2) can be generated on completion of a group B or group C scan. • A compare interrupt request (S12CMPAI, S12CMPAI1, S12CMPAI2, S12CMPBI, S12CMPBI1, or S12CMPBI2) can be generated upon a match with the comparison condition for the digital compare function. • The S12ADI/S12ADI1/S12ADI2, S12GBADI/S12GBADI1/S12GBADI2, and S12GCADI/S12GCADI1/S12GCADI2 interrupts can activate the DMA controller (DMAC) or data transfer controller (DTC).
Event link function	• An event can be output upon completion of all scans. • In single scan mode, an event can be output when the compare function window condition is met. • Scan can be started by a trigger output by the ELC.	• An event can be output upon completion of all scans. • In single scan mode, an event can be output when the compare function window condition is met. • Scan can be started by a trigger output by the ELC.
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Table 2.66 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX66T (S12ADH)	RX26T (S12ADHa)
ADDRy	—	A/D data register y (y = 0 to 7 in S12AD, y = 0 to 7 in S12AD1, y = 0 to 11, 16, 17 in S12AD2)	A/D data register y (y = 0 to 6 in S12AD, y = 0 to 3 in S12AD1, y = 0 to 11, 16, 17 in S12AD2)
ADCSR	DBLANS[4:0]	Double trigger target channel select bits These bits select an analog input channel subject to double trigger mode. This setting is valid only when double trigger mode is selected. • S12AD (unit 0) b4 b0 0 0 0 0 0: AN000 0 0 0 0 1: AN001 0 0 0 1 0: AN002 0 0 0 1 1: AN003 0 0 1 0 0: AN004 0 0 1 0 1: AN005 0 0 1 1 0: AN006 0 0 1 1 1: AN007 • S12AD 1 (unit 1) b4 b0 0 0 0 0 0: AN100 0 0 0 0 1: AN101 0 0 0 1 0: AN102 0 0 0 1 1: AN103 0 0 1 0 0: AN104 0 0 1 0 1: AN105 0 0 1 1 0: AN106 0 0 1 1 1: AN107 • S12AD2 (unit 2) b4 b0 0 0 0 0 0: AN200 0 0 0 0 1: AN201 0 0 0 1 0: AN202 0 0 0 1 1: AN203 0 0 1 0 0: AN204 0 0 1 0 1: AN205 0 0 1 1 0: AN206 0 0 1 1 1: AN207 0 1 0 0 0: AN208 0 1 0 0 1: AN209 0 1 0 1 0: AN210 0 1 0 1 1: AN211 1 0 0 0 0: AN216 1 0 0 0 1: AN217	Double trigger target channel select bits These bits select an analog input channel subject to double trigger mode. This setting is valid only when double trigger mode is selected. • S12AD (unit 0) b4 b0 0 0 0 0 0: AN000 0 0 0 0 1: AN001 0 0 0 1 0: AN002 0 0 0 1 1: AN003 0 0 1 0 0: AN004 0 0 1 0 1: AN005 0 0 1 1 0: AN006 • S12AD 1 (unit 1) b4 b0 0 0 0 0 0: AN100 0 0 0 0 1: AN101 0 0 0 1 0: AN102 0 0 0 1 1: AN103 • S12AD2 (unit 2) b4 b0 0 0 0 0 0: AN200 0 0 0 0 1: AN201 0 0 0 1 0: AN202 0 0 0 1 1: AN203 0 0 1 0 0: AN204 0 0 1 0 1: AN205 0 0 1 1 0: AN206 0 0 1 1 1: AN207 0 1 0 0 0: AN208 0 1 0 0 1: AN209 0 1 0 1 0: AN210 0 1 0 1 1: AN211 1 0 0 0 0: AN216 1 0 0 0 1: AN217

Register	Bit	RX66T (S12ADH)	RX26T (S12ADHa)
S12AD. ADANSA0	ANSA007	A/D conversion channel select bit	—
S12AD1. ADANSA0	ANSA004	A/D conversion channel select bits	—
	ANSA005		
	ANSA006		
	ANSA007		
S12AD. ADANSB0	ANSB007	A/D conversion channel select bit	—
S12AD1. ADANSB0	ANSB004	A/D conversion channel select bits	—
	ANSB005		
	ANSB006		
	ANSB007		
S12AD. ADANSC0	ANSC007	A/D conversion channel select bit	—
S12AD1. ADANSC0	ANSC004	A/D conversion channel select bits	—
	ANSC005		
	ANSC006		
	ANSC007		
S12AD. ADSCSn	—	A/D channel conversion order setting register n (n = 0 to 7)	A/D channel conversion order setting register n (n = 0 to 6)
S12AD1. ADSCSn	—	A/D channel conversion order setting register n (n = 0 to 7)	A/D channel conversion order setting register n (n = 0 to 3)
S12AD. ADADS0	ADS007	A/D-converted value addition/ average function select bit	—
S12AD1. ADADS0	ADS004	A/D-converted value addition/ average function select bits	—
	ADS005		
	ADS006		
	ADS007		
ADCER	ASE	—	A/D data register automatic setting enable bit
ADSTRGR	TRSB[5:0] (RX66T) TRSB[6:0] (RX26T)	Group B A/D conversion start trigger select bit	Group B A/D conversion start trigger select bit
	TRSA[5:0] (RX66T) TRSA[6:0] (RX26T)	A/D conversion start trigger select bit	A/D conversion start trigger select bit
ADGCTRGR	TRSC[5:0]	This bit selects the A/D conversion start trigger for group C in group scan mode.	This bit is used with the ADGCTRGR2.TRSC6 bit to select the A/D conversion start trigger for group C in group scan mode.
ADGCTRGR2	—	—	A/D group C trigger select register 2
ADSSTRn	—	A/D sampling state register n (n = 0 to 7 in S12AD, n = 0 to 7 in S12AD1, n = n = 0 to 11, L, T, or O in S12AD2)	A/D sampling state register n (n = 0 to 6 in S12AD, n = 0 to 3 in S12AD1, n = n = 0 to 11, L, T, or O in S12AD2)
S12AD. ADCMPANSR0	CMPCHA007	Compare window A channel select bit	—

Register	Bit	RX66T (S12ADH)	RX26T (S12ADHa)
S12AD1. ADCMPANSR0	CMPCHA004 CMPCHA005 CMPCHA006 CMPCHA007	Compare window A channel select bits	—
S12AD. ADCMPLR0	CMPLCHA007	Compare window A comparison condition select bit	—
S12AD1. ADCMPLR0	CMPLCHA004 CMPLCHA005 CMPLCHA006 CMPLCHA007	Compare window A comparison condition select bits	—
S12AD. ADCMPSR0	CMPSTCHA007	Compare window A flag	—
S12AD1. ADCMPSR0	CMPSTCHA004 CMPSTCHA005 CMPSTCHA006 CMPSTCHA007	Compare window A flag	—
S12AD. ADCMPBNSR	CMPCHB[5:0]	Compare window B channel select bits These bits select channels to be compared with the conditions for compare window B. b5 b0 0 0 0 0 0 0: AN000 0 0 0 0 0 1: AN001 0 0 0 0 1 0: AN002 : : 0 0 0 1 1 0: AN006 0 0 0 1 1 1: AN007 Settings other than the above are prohibited.	Compare window B channel select bits These bits select channels to be compared with the conditions for compare window B. b5 b0 0 0 0 0 0 0: AN000 0 0 0 0 0 1: AN001 0 0 0 0 1 0: AN002 : : 0 0 0 1 1 0: AN006 Settings other than the above are prohibited.
S12AD1. ADCMPBNSR	CMPCHB[5:0]	Compare window B channel select bits These bits select channels to be compared with the conditions for compare window B. b5 b0 0 0 0 0 0 0: AN100 0 0 0 0 0 1: AN101 0 0 0 0 1 0: AN102 : : 0 0 0 1 1 0: AN106 0 0 0 1 1 1: AN107 Settings other than the above are prohibited.	Compare window B channel select bits These bits select channels to be compared with the conditions for compare window B. b5 b0 0 0 0 0 0 0: AN100 0 0 0 0 0 1: AN101 0 0 0 0 1 0: AN102 0 0 0 0 1 1: AN103 Settings other than the above are prohibited.

Register	Bit	RX66T (S12ADH)	RX26T (S12ADHa)
S12AD. ADPGAGS0	P000GAIN[3:0] P001GAIN[3:0] P002GAIN[3:0]	P000 amplifier gain setting bits P001 amplifier gain setting bits P002 amplifier gain setting bits • When pseudo-differential input is disabled (ADPGADCR0.PxDEN bit = 0): 0 0 0 0: × 2.000 0 0 0 1: × 2.500 0 0 1 1: × 3.077 0 1 0 1: × 3.636 0 1 1 0: × 4.000 0 1 1 1: × 4.444 1 0 0 0: × 5.000 1 0 1 0: × 6.667 1 0 1 1: × 8.000 1 1 0 0: × 10.000 1 1 0 1: × 13.333 1 1 1 0: × 20.000 Settings other than the above are prohibited. • When pseudo-differential input is enabled (ADPGADCR0.PxDEN bit = 1 and ADPGACR.PxCR[2] bit = 1): 0 0 0 1: × 1.500 1 0 0 0: × 4.000 1 0 1 1: × 7.000 1 1 0 1: × 12.333 Settings other than the above are prohibited.	P000 amplifier gain setting bits P001 amplifier gain setting bits P002 amplifier gain setting bits 0 0 0 0: × 2.000 0 0 0 1: × 2.500 0 0 1 1: × 3.077 0 1 0 1: × 3.636 0 1 1 0: × 4.000 0 1 1 1: × 4.444 1 0 0 0: × 5.000 1 0 1 0: × 6.667 1 0 1 1: × 8.000 1 1 0 0: × 10.000 1 1 0 1: × 13.333 1 1 1 0: × 20.000 Settings other than the above are prohibited.

Register	Bit	RX66T (S12ADH)	RX26T (S12ADHa)
S12AD1. ADPGAGS0	P100GAIN[3:0] P101GAIN[3:0] P102GAIN[3:0]	P100 amplifier gain setting bits P101 amplifier gain setting bits P102 amplifier gain setting bits • When pseudo-differential input is disabled (ADPGADCR0.PxDEN bit = 0): 0 0 0 0: × 2.000 0 0 0 1: × 2.500 0 0 1 1: × 3.077 0 1 0 1: × 3.636 0 1 1 0: × 4.000 0 1 1 1: × 4.444 1 0 0 0: × 5.000 1 0 1 0: × 6.667 1 0 1 1: × 8.000 1 1 0 0: × 10.000 1 1 0 1: × 13.333 1 1 1 0: × 20.000 Settings other than the above are prohibited. • When pseudo-differential input is enabled (ADPGADCR0.PxDEN bit = 1 and ADPGACR.PxCR[2] bit = 1): 0 0 0 1: × 1.500 1 0 0 0: × 4.000 1 0 1 1: × 7.000 1 1 0 1: × 12.333 Settings other than the above are prohibited.	P100 amplifier gain setting bits P101 amplifier gain setting bits P102 amplifier gain setting bits 0 0 0 0: × 2.000 0 0 0 1: × 2.500 0 0 1 1: × 3.077 0 1 0 1: × 3.636 0 1 1 0: × 4.000 0 1 1 1: × 4.444 1 0 0 0: × 5.000 1 0 1 0: × 6.667 1 0 1 1: × 8.000 1 1 0 0: × 10.000 1 1 0 1: × 13.333 1 1 1 0: × 20.000 Settings other than the above are prohibited.
ADPGADCR0	—	A/D programmable gain differential input control register	—

Table 2.67 Comparison of A/D Start Sources to be Set in ADSTRGR Register

Bit	RX66T (S12ADH)	RX26T (S12ADHa)
TRSB[5:0] (RX66T) TRSB[6:0] (RX26T)	Group B A/D conversion start trigger select bit b5 b0 111111: No trigger sources are selected. 000001: TRGA0N 000010: TRGA1N 000011: TRGA2N 000100: TRGA3N 000101: TRGA4N 000110: TRGA6N 000111: TRGA7N 001000: TRG0N 001001: TRG4AN 001010: TRG4BN 001011: TRG4AN or TRG4BN 001100: TRG4ABN 001101: TRG7AN 001110: TRG7BN 001111: TRG7AN or TRG7BN 010000: TRG7ABN 010011: TRGA9N 010100: TRG9N 011001: TRGA0N or TRG0N 011010: TRGA9N or TRG9N 011011: TRGA0N or TRGA9N 011100: TRG0N or TRG9N 100001: TRG9AEN 100010: TRG0AEN 100011: TRGA09N 100100: TRG09N	Group B A/D conversion start trigger select bit b6 b0 0111111: No trigger sources are selected. 1111111: No trigger sources are selected. 0000001: TRGA0N 0000010: TRGA1N 0000011: TRGA2N 0000100: TRGA3N 0000101: TRGA4N 0000110: TRGA6N 0000111: TRGA7N 0001000: TRG0N 0001001: TRG4AN 0001010: TRG4BN 0001011: TRG4AN or TRG4BN 0001100: TRG4ABN 0001101: TRG7AN 0001110: TRG7BN 0001111: TRG7AN or TRG7BN 0010000: TRG7ABN 0010011: TRGA9N 0010100: TRG9N 0011001: TRGA0N or TRG0N 0011010: TRGA9N or TRG9N 0011011: TRGA0N or TRGA9N 0011100: TRG0N or TRG9N 0100001: TRG9AEN 0100010: TRG0AEN 0100011: TRGA09N 0100100: TRG09N 1000000: GTADTRA0N 1000001: GTADTRB0N 1000010: GTADTRA1N 1000011: GTADTRB1N 1000100: GTADTRA2N 1000101: GTADTRB2N 1000110: GTADTRA3N 1000111: GTADTRB3N 1001000: GTADTRA0N or GTADTRB0N 1001001: GTADTRA1N or GTADTRB1N 1001010: GTADTRA2N or GTADTRB2N 1001011: GTADTRA3N or GTADTRB3N 1001100: GTADTRA4N 1001101: GTADTRB4N 1001110: GTADTRA5N 1001111: GTADTRB5N 1010000: GTADTRA6N 1010001: GTADTRB6N 1010010: GTADTRA7N

Bit	RX66T (S12ADH)	RX26T (S12ADHa)
TRSB[5:0] (RX66T) TRSB[6:0] (RX26T)		1010011: GTADTRB7N 1010100: GTADTRA4N or GTADTRB4N 1010101: GTADTRA5N or GTADTRB5N 1010110: GTADTRA6N or GTADTRB6N 1010111: GTADTRA7N or GTADTRB7N
	011101: TMTRG0AN_0	0011101: TMTRG0AN_0
	011110: TMTRG0AN_1	0011110: TMTRG0AN_1
	011111: TMTRG0AN_2	0011111: TMTRG0AN_2
	100000: TMTRG0AN_3	0100000: TMTRG0AN_3
	110010: ELCTRG00N*1 ELCTRG10N*2 ELCTRG20N*3	0110010: ELCTRG00N*1 ELCTRG10N*2 ELCTRG20N*3
	110011: ELCTRG01N*1 ELCTRG11N*2 ELCTRG21N*3	0110011: ELCTRG01N*1 ELCTRG11N*2 ELCTRG21N*3
	111010: ELCTRG00N or ELCTRG01N*1 ELCTRG10N or ELCTRG11N*2 ELCTRG20N or ELCTRG21N*3	0111010: ELCTRG00N or ELCTRG01N*1 ELCTRG10N or ELCTRG11N*2 ELCTRG20N or ELCTRG21N*3

Bit	RX66T (S12ADH)	RX26T (S12ADHa)
TRSA[5:0] (RX66T) TRSA[6:0] (RX26T)	A/D conversion start trigger select bit b13 b8 111111: No trigger sources are selected. 000000: ADTRGn# 000001: TRGA0N 000010: TRGA1N 000011: TRGA2N 000100: TRGA3N 000101: TRGA4N 000110: TRGA6N 000111: TRGA7N 001000: TRG0N 001001: TRG4AN 001010: TRG4BN 001011: TRG4AN or TRG4BN 001100: TRG4ABN 001101: TRG7AN 001110: TRG7BN 001111: TRG7AN or TRG7BN 010000: TRG7ABN 010011: TRGA9N 010100: TRG9N 011001: TRGA0N or TRG0N 011010: TRGA9N or TRG9N 011011: TRGA0N or TRGA9N 011100: TRG0N or TRG9N 100001: TRG9AEN 100010: TRG0AEN 100011: TRGA09N 100100: TRG09N	A/D conversion start trigger select bit b14 b8 0111111: No trigger sources are selected. 1111111: No trigger sources are selected. 0000000: ADTRGn# 0000001: TRGA0N 0000010: TRGA1N 0000011: TRGA2N 0000100: TRGA3N 0000101: TRGA4N 0000110: TRGA6N 0000111: TRGA7N 0001000: TRG0N 0001001: TRG4AN 0001010: TRG4BN 0001011: TRG4AN or TRG4BN 0001100: TRG4ABN 0001101: TRG7AN 0001110: TRG7BN 0001111: TRG7AN or TRG7BN 0010000: TRG7ABN 0010011: TRGA9N 0010100: TRG9N 0011001: TRGA0N or TRG0N 0011010: TRGA9N or TRG9N 0011011: TRGA0N or TRGA9N 0011100: TRG0N or TRG9N 0100001: TRG9AEN 0100010: TRG0AEN 0100011: TRGA09N 0100100: TRG09N 1000000: GTADTRA0N 1000001: GTADTRB0N 1000010: GTADTRA1N 1000011: GTADTRB1N 1000100: GTADTRA2N 1000101: GTADTRB2N 1000110: GTADTRA3N 1000111: GTADTRB3N 1001000: GTADTRA0N or GTADTRB0N 1001001: GTADTRA1N or GTADTRB1N 1001010: GTADTRA2N or GTADTRB2N 1001011: GTADTRA3N or GTADTRB3N 1001100: GTADTRA4N 1001101: GTADTRB4N 1001110: GTADTRA5N 1001111: GTADTRB5N 1010000: GTADTRA6N 1010001: GTADTRB6N 1010010: GTADTRA7N 1010011: GTADTRB7N

Bit	RX66T (S12ADH)	RX26T (S12ADHa)
TRSA[5:0] (RX66T) TRSA[6:0] (RX26T)		1010100: GTADTRA4N or GTADTRB4N 1010101: GTADTRA5N or GTADTRB5N 1010110: GTADTRA6N or GTADTRB6N 1010111: GTADTRA7N or GTADTRB7N
	011101: TMTRG0AN_0/	0011101: TMTRG0AN_0
	011110: TMTRG0AN_1	0011110: TMTRG0AN_1
	011111: TMTRG0AN_2	0011111: TMTRG0AN_2
	100000: TMTRG0AN_3	0100000: TMTRG0AN_3
	110010: ELCTRG00N*1 ELCTRG10N*2 ELCTRG20N*3	0110010: ELCTRG00N*1 ELCTRG10N*2 ELCTRG20N*3
	110011: ELCTRG01N*1 ELCTRG11N*2 ELCTRG21N*3	0110011: ELCTRG01N*1 ELCTRG11N*2 ELCTRG21N*3
	111010: ELCTRG00N or ELCTRG01N*1 ELCTRG10N or ELCTRG11N*2 ELCTRG20N or ELCTRG21N*3	0111010: ELCTRG00N or ELCTRG01N*1 ELCTRG10N or ELCTRG11N*2 ELCTRG20N or ELCTRG21N*3

Notes: 1. Unit 0
2. Unit 1
3. Unit 2

Table 2.68 Comparison of A/D Start Sources to be Set in ADGCTRGR Register and ADGCTRGR2 Register

Bit	RX66T (S12ADH)	RX26T (S12ADHa)
TRSC[5:0] (RX66T) TRSC[5:0], TRSC6 (RX26T)	Group B A/D conversion start trigger select bit b5 b0 111111: No trigger sources are selected. 000001: TRGA0N 000010: TRGA1N 000011: TRGA2N 000100: TRGA3N 000101: TRGA4N 000110: TRGA6N 000111: TRGA7N 001000: TRG0N 001001: TRG4AN 001010: TRG4BN 001011: TRG4AN or TRG4BN 001100: TRG4ABN 001101: TRG7AN 001110: TRG7BN 001111: TRG7AN or TRG7BN 010000: TRG7ABN 010011: TRGA9N 010100: TRG9N 011001: TRGA0N or TRG0N 011010: TRGA9N or TRG9N 011011: TRGA0N or TRGA9N 011100: TRG0N or TRG9N 100001: TRG9AEN 100010: TRG0AEN 100011: TRGA09N 100100: TRG09N	Group C A/D conversion start trigger select bit Group C A/D conversion start trigger select bit 6 b6 b0 0111111: No trigger sources are selected. 1111111: No trigger sources are selected. 0000001: TRGA0N 0000010: TRGA1N 0000011: TRGA2N 0000100: TRGA3N 0000101: TRGA4N 0000110: TRGA6N 0000111: TRGA7N 0001000: TRG0N 0001001: TRG4AN 0001010: TRG4BN 0001011: TRG4AN or TRG4BN 0001100: TRG4ABN 0001101: TRG7AN 0001110: TRG7BN 0001111: TRG7AN or TRG7BN 0010000: TRG7ABN 0010011: TRGA9N 0010100: TRG9N 0011001: TRGA0N or TRG0N 0011010: TRGA9N or TRG9N 0011011: TRGA0N or TRGA9N 0011100: TRG0N or TRG9N 0100001: TRG9AEN 0100010: TRG0AEN 0100011: TRGA09N 0100100: TRG09N 1000000: GTADTRA0N 1000001: GTADTRB0N 1000010: GTADTRA1N 1000011: GTADTRB1N 1000100: GTADTRA2N 1000101: GTADTRB2N 1000110: GTADTRA3N 1000111: GTADTRB3N 1001000: GTADTRA0N or GTADTRB0N 1001001: GTADTRA1N or GTADTRB1N 1001010: GTADTRA2N or GTADTRB2N 1001011: GTADTRA3N or GTADTRB3N 1001100: GTADTRA4N 1001101: GTADTRB4N 1001110: GTADTRA5N 1001111: GTADTRB5N

Bit	RX66T (S12ADH)	RX26T (S12ADHa)
TRSC[5:0] (RX66T) TRSC[5:0], TRSC6 (RX26T)		1010000: GTADTRA6N 1010001: GTADTRB6N 1010010: GTADTRA7N 1010011: GTADTRB7N 1010100: GTADTRA4N or GTADTRB4N 1010101: GTADTRA5N or GTADTRB5N 1010110: GTADTRA6N or GTADTRB6N 1010111: GTADTRA7N or GTADTRB7N
	011101: TMTRG0AN_0 011110: TMTRG0AN_1 011111: TMTRG0AN_2 100000: TMTRG0AN_3 110010: ELCTRG00N*1 ELCTRG10N*2 ELCTRG20N*3 110011: ELCTRG01N*1 ELCTRG11N*2 ELCTRG21N*3 111010: ELCTRG00N or ELCTRG01N*1 ELCTRG10N or ELCTRG11N*2 ELCTRG20N or ELCTRG21N*3	0011101: TMTRG0AN_0 0011110: TMTRG0AN_1 0011111: TMTRG0AN_2 0100000: TMTRG0AN_3 0110010: ELCTRG00N*1 ELCTRG10N*2 ELCTRG20N*3 0110011: ELCTRG01N*1 ELCTRG11N*2 ELCTRG21N*3 0111010: ELCTRG00N or ELCTRG01N*1 ELCTRG10N or ELCTRG11N*2 ELCTRG20N or ELCTRG21N*3

Notes: 1. Unit 0
2. Unit 1
3. Unit 2

2.24 Comparator C

Table 2.69 is Comparison of Comparator C Registers.

Table 2.69 Comparison of Comparator C Registers

Register	Bit	RX66T (CMPC)	RX26T (CMPCa)
CMPCTL2	—	—	Comparator control register 2

2.25 Data Operation Circuit

Table 2.70 is Comparative Overview of Data Operation Circuits, and Table 2.71 is Comparison of Data Operation Circuit Registers.

Table 2.70 Comparative Overview of Data Operation Circuits

Item	RX66T (DOC)	RX26T (DOCA)
Data operation functions	16-bit data comparison, addition, and subtraction	• Comparison of 16- or 32-bit data (match/mismatch, greater/less, in/out of range) • Addition or subtraction of 16- or 32-bit data
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state
Interrupts	• The result of data comparison matches the detection condition. • The result of data addition is greater than FFFFh (overflow). • The result of data subtraction is less than 0000h (underflow).	• The result of data comparison matches the detection condition. • The result of data addition is greater than FFFFh (when DOCR.DOPSZ = 0) or FFFF FFFFh (when DOCR.DOPSZ = 1) (overflow). • The result of data subtraction is less than 0000h (when DOCR.DOPSZ = 0) or 0000 0000h (when DOCR.DOPSZ = 1) (underflow).
Event link function (output)	• The result of data comparison matches the detection condition. • The result of data addition is greater than FFFFh (overflow). • The result of data subtraction is less than 0000h (underflow).	• The result of data comparison matches the detection condition. • The result of data addition is greater than FFFFh (when DOCR.DOPSZ = 0) or FFFF FFFFh (when DOCR.DOPSZ = 1) (overflow). • The result of data subtraction is less than 0000h (when DOCR.DOPSZ = 0) or 0000 0000h (when DOCR.DOPSZ = 1) (underflow).

Table 2.71 Comparison of Data Operation Circuit Registers

Register	Bit	RX66T (DOC)	RX26T (DOCA)
DOCR	DCSEL (RX66T) DCSEL[2:0] (RX26T)	Detection condition select bit b2 0: Data mismatches are detected. 1: Data matches are detected.	Detection condition select bits b6 b4 0 0 0: Mismatch (DODIR ≠ DODSR0) 0 0 1: Match (DODIR = DODSR0) 0 1 0: Less (DODIR < DODSR0) 0 1 1: Greater (DODIR > DODSR0) 1 0 0: In range (DODSR0 < DODIR < DODSR1) 1 0 1: Out of range (DODIR < DODSR0, DODSR1 < DODIR) Other than above: Setting prohibited.
	DOPSZ	—	Data operation size select bit
	DOPCIE	Data operation circuit interrupt enable bit b4 0: Interrupt disabled 1: Interrupt enabled	Data operation circuit interrupt enable bit b7 0: Interrupt disabled 1: Interrupt enabled
	DOPCF	Data operation result flag	—
	DOPCFCL	Data operation result clear bit	—
DOSR	—	—	DOC status register
DOSCR	—	—	DOC status clear register
DODIR	—	DOC data input register	DOC data input register
		16-bit readable/writable register	32-bit readable/writable register
DODSR0	—	DOC data setting register 0	DOC data setting register 0
		16-bit readable/writable register	32-bit readable/writable register
DODSR1	—	—	DOC data setting register 1

2.26 RAM

Table 2.72 is Comparative Overview of RAM, and Table 2.73 is Comparison of RAM Registers.

Table 2.72 Comparative Overview of RAM

Item	RX66T		RX26T (RAM)
	Without ECC (Error Checking and Correcting feature) (RAM)	**With ECC (Error Checking and Correcting feature) (ECCRAM)**	
Capacity	64 KB 128 KB	16 KB	48 KB 64 KB
Addresses	• For RAM capacity 64 KB — 0000 0000h to 0000 FFFFh • For RAM capacity 128 KB — 0000 0000h to 0001 FFFFh	• 00FF C000h to 00FF FFFFh	• For RAM capacity 48 KB — 0000 0000h to 0000 BFFFh • For RAM capacity 64 KB — 0000 0000h to 0000 FFFFh
Memory buses	Memory bus 1	Memory bus 3	Memory bus 1
Access	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.	• The ECC feature can be enabled or disabled. [When MEMWAIT is set to 0] • If the ECC feature is disabled: — Two-cycle access is possible for both reading and writing. • If the ECC feature is enabled (no error): — Two-cycle access is possible for both reading and writing. • If the ECC feature is enabled (an error occurred): — Three-cycle access is possible for both reading and writing.	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.

Item	RX66T		RX26T (RAM)
	Without ECC (Error Checking and Correcting feature) (RAM)	With ECC (Error Checking and Correcting feature) (ECCRAM)	
Access		[When MEMWAIT is set to 1] • If the ECC feature is disabled: — Three-cycle access is possible for both reading and writing. • If the ECC feature is enabled (no error): — Three-cycle access is possible for reading and four-cycle access is possible for writing. • If the ECC feature is enabled (an error occurred): — Five-cycle access is possible for both reading and writing.	
Data retention function	Not available in deep software standby mode		—
Low power consumption function	RAM and ECCRAM can individually transfer to the module stop state.		Ability to transition to module stop state
Error checking	• Detection of 1-bit errors • A non-maskable interrupt or an interrupt is generated when an error occurs.	• ECC (Error Checking and Correcting feature) — Correction of 1-bit errors and detection of 2-bit errors • A non-maskable interrupt or an interrupt is generated when an error occurs.	• Parity check: Detection of 1-bit errors • A non-maskable interrupt or an interrupt is generated when an error occurs.

Table 2.73 Comparison of RAM Registers

Register	Bit	RX66T (RAM, ECCRAM)	RX26T (RAM)
ECCRAMMODE	—	ECCRAM operating mode control register	—
ECCRAM2STS	—	ECCRAM 2-bit error status register	—
ECCRAM1STSEN	—	ECCRAM 1-bit error information update enable register	—
ECCRAM1STS	—	ECCRAM 1-bit error status register	—
ECCRAMPRCR	—	ECCRAM protection register	—
ECCRAM2ECAD	—	ECCRAM 2-bit error address capture register	—
ECCRAM1ECAD	—	ECCRAM 1-bit error address capture register	—
ECCRAMPRCR2	—	ECCRAM protection register 2	—
ECCRAMETST	—	ECCRAM test control register	—

2.27 Flash Memory

Table 2.74 is Comparative Overview of Flash Memory, and Table 2.75 is Comparison of Flash Memory Registers.

Table 2.74 Comparative Overview of Flash Memory

Item	RX66T		RX26T	
	Code Flash Memory	**Data Flash Memory**	**Code Flash Memory**	**Data Flash Memory**
Memory capacity	• User area: Max. 1 MB • User boot area: 32 KB	• Data area: 32 KB	• Max. 512 KB	• 16 KB
ROM cache	• Capacity: 8 KB • Mapping method: Direct map • Line size: 16 bytes	—	—	—
Read cycles	• When ROM cache operation is enabled: One cycle in response to a cache hit When the cache is missed: — One or two cycles if ICLK is equal to or smaller than 120 MHz — two or three cycles if ICLK is larger than 120 MHz • When ROM cache operation is prohibited: — One cycle if ICLK is equal to or smaller than 120 MHz — Two cycles if ICLK is larger than 120 MHz	16-bit or 8-bit read access requires 8 FCLK clock cycles.	One cycle	16-bit or 8-bit read access requires 8 FCLK clock cycles.
Value after erasure	FFh	Undefined	FFh	Undefined
Programming/ erasing method	• FACI commands specified in the FACI command issuing area (007E 0000h) can be used to program and erase the code flash memory and data flash memory. • Programming and erasure through serial interface transfer by a flash memory programmer (serial programming) • Programming and erasure of flash memory by using a user program (self-programming)		• FACI commands specified in the FACI command issuing area (007E 0000h) can be used to program and erase the code flash memory and data flash memory. • Programming and erasure through serial interface transfer by a flash memory programmer (serial programming) • Programming and erasure of flash memory by using a user program (self-programming)	
Security function	Protects against illicit tampering with or reading of data in flash memory.		Protects against illicit tampering with or reading of data in flash memory.	
Protection function	Protects against erroneous programming of the flash memory.		Protects against erroneous programming of the flash memory.	

Item	RX66T		RX26T	
	Code Flash Memory	**Data Flash Memory**	**Code Flash Memory**	**Data Flash Memory**
Dual bank function	—	—	A dual bank configuration allows secure update to be performed when write operation is suspended. • Linear mode: Code flash memory is used as one area. • Dual mode: Code flash memory is divided into two areas.	—
Trusted Memory (TM) function	Protects against illicit reading of blocks 8 and 9 in the code flash memory.		Protects against illicit reading of code flash memory. • Linear mode: Blocks 8 and 9 • Dual mode: Blocks 8, 9, 30, and 31	—
BGO (Background operation) function	The user area can be read while the data area is being programmed or erased.		• The code flash memory can be read while the code flash memory is being programmed or erased. • The data flash memory can be read while the code flash memory is being programmed or erased. • The code flash memory can be read while the data flash memory is being programmed or erased.	
Units of programming and erasure	• Programming the user area and user boot area: 256 bytes • Erasing the user area: Block units	• Programming the data area: 4 bytes • Erasing the data area: Block units	• Programming: 128 bytes • Erasing: Block unit	• Programming: 4 bytes • Erasing: Block unit
Other functions	Interrupts can be accepted during self-programming.		Interrupts can be accepted during self-programming.	

Item	RX66T		RX26T	
	Code Flash Memory	**Data Flash Memory**	**Code Flash Memory**	**Data Flash Memory**
On-board programming (serial programming and self-programming)	• Programming/erasure in boot mode (SCI interface) — The asynchronous serial interface (SCI1) is used. — The communication speed is adjusted automatically. — Programming and erasure of the user boot area is also possible. • Programming/erasure in boot mode (USB interface) — USB0 is used. — Direct connection to a PC is possible because special hardware is not needed. • Programming/erasure in boot mode (FINE interface) — FINE is used. • Programming/erasure in user boot mode — A user-specific boot program can be created. • Programming/erasure in single-chip mode and on-chip ROM enabled extended mode — Programming and erasure are possible by using the code flash memory/data flash memory rewrite routine in the user program.		• Programming/erasure in boot mode (SCI interface) — The asynchronous serial interface (SCI1) is used. — The communication speed is adjusted automatically. • Programming/erasure in boot mode (FINE interface) — FINE is used. • Programming/erasure in single-chip mode — Programming and erasure are possible by using the code flash memory/data flash memory rewrite routine in the user program.	
Off-board programming (programming/ erasure using a parallel programmer)	The user area and user boot area can be programmed and erased by using a parallel programmer.	The data area cannot be programmed or erased by using a parallel programmer.	—	—
Unique ID	A unique 12-byte ID code is provided for each MCU.		A unique 12-byte ID code is provided for each MCU.	

Table 2.75 Comparison of Flash Memory Registers

Register	Bit	RX66T	RX26T
ROMCE	—	ROM cache enable register	—
ROMCIV	—	ROM cache disable register	—
NCRGn	—	Non-cacheable area n address register (n = 0 or 1)	—
NCRCn	—	Non-cacheable area n configuration register (n = 0 or 1)	—
FWEPROR	FLWE[1:0]	Flash write/erase enable bits b1 b0 0 0: Programming and erasure, programming and reading of the lock bit, and blank check are disabled. 0 1: Programming and erasure, programming and reading of the lock bit, and blank check are enabled. 1 0: Programming and erasure, programming and reading of the lock bit, and blank check are disabled. 1 1: Programming and erasure, programming and reading of the lock bit, and blank check are disabled.	Flash write/erase enable bits b1 b0 0 0: Programming, block erase, and blank check are disabled. 0 1: Programming block erase, and blank check are enabled. 1 0: Programming, block erase, and blank check are disabled. 1 1: Programming, block erase, and blank check are disabled.
FSTATR	FRDY	Flash ready flag 0: Processing of the programming, block erase, P/E suspend, P/E resume, forced stop, blank check, configuration setting, lock-bit programming, or lock-bit read command is being performed. 1: The above processing is not performed.	Flash ready flag 0: Processing of the programming, block erase, P/E suspend, P/E resume, forced stop, blank check, or configuration setting command is being performed. 1: None of the above processing is being performed.
FPROTR	—	Flash protection register	—
FLKSTAT	—	Lock bit status register	—
FPESTAT	PEERRST [7:0]	P/E error status flag 00h: No error 01h: Program error for an area protected by the lock bit 02h: Program error due to a cause other than the lock bit 11h: Erase error for an area protected by the lock bit 12h: Erase error due to a cause other than the lock bit	P/E error status flag 00h: No error 02h: Program error 12h: Erase error
FAWMON	—	—	Flash access window monitor register
FSUACR	—	—	Start-up area control register

2.28 Packages

As indicated in Table 2.76, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage.

Table 2.76 Packages

Package Type	RX66T	RX26T
144-pin LFQFP	○	×
112-pin LQFP	○	×
80-pin LQFP	○	×
64-pin LFQFP	×	○
48-pin LFQFP	×	○

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by **blue text**. Items that exist on both groups with different specifications are indicated by **red text**. Black text indicates there is no differences in the item's specifications between groups.

3.1 100-Pin Package

Table 3.1 is Comparative Listing of 100-Pin Package Pin Functions.

Table 3.1 Comparative Listing of 100-Pin Package Pin Functions

100-Pin	RX66T	RX26T
1	PE5/BCLK/MTIOC9D/MTIOC9D#/GTIOC3A/ GTETRGB/GTIOC3A#/GTETRGD/SCK9/ CTS9#/RTS9#/SS9#/IRQ0/ADST0	PE5/MTIOC9D/MTIOC9D#/GTIOC3A/ GTETRGB/GTIOC3A#/GTETRGD/SCK009/ CTS009#/RTS009#/SS009#/TXDB009/IRQ0/ ADST0
2	EMLE	EMLE/PN7/MTIOC9D/MTIOC9D#/IRQ5/ ADST0
3	VSS	VSS
4	UB/P00/A11/MTIOC9A/MTIOC9A#/CACREF/ RXD9/SMISO9/SSCL9/RXD12/SMISO12/ SSCL12/RXDX12/IRQ2/ADST1/COMP0	P00/MTIOC9A/MTIOC9A#/CACREF/GTIU/ TIC3/RXD12/SMISO12/SSCL12/RXDX12/ RXD009/SMISO009/SSCL009/IRQ2/ADST1/ COMP0
5	VCL	VCL
6	MD/FINED	MD/FINED/PN6
7	P01/A10/MTIOC9C/MTIOC9C#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE12#/ TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/IRQ4/ADST2/ COMP1	P01/MTIOC9C/MTIOC9C#/POE12#/ GTETRGA/GTETRGB/GTETRGC/ GTETRGD/GTIW/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/TXD009/TXDA009/ SMOSI009/SSDA009/IRQ4/ADST2/COMP1
8	PE4/A9/MTCLKC/MTCLKC#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE10#/ SCK9/IRQ1	PE4/MTCLKC/MTCLKC#/POE10#/ GTETRGA/GTETRGB/GTETRGC/ GTETRGD/SCK009/TXDB009/IRQ1
9	PE3/A8/MTCLKD/MTCLKD#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE11#/ CTS9#/RTS9#/SS9#/IRQ2-DS	PE3/MTCLKD/MTCLKD#/POE11#/ GTETRGA/GTETRGB/GTETRGC/ GTETRGD/CTS009#/RTS009#/SS009#/ DE009/IRQ2
10	RES#	RES#
11	XTAL/P37	XTAL/P37/RXD5/SMISO5/SSCL5
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36/TXD5/SMOSI5/SSDA5
14	VCC	VCC
15	PE2/POE10#/NMI	PE2/POE10#/NMI/IRQ0
16	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/ TMO5/CTS5#/RTS5#/SS5#/CTS12#/ RTS12#/SS12#/SSLA3/IRQ15	PE1/MTIOC9D/MTIOC9D#/TMO5/CTS5#/ RTS5#/SS5#/CTS12#/RTS12#/SS12#/ SSLA3/SSL03/IRQ15
17	PE0/WR1#/BC1#/WAIT#/MTIOC9B/ MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/ SSCL5/SSLA2/CRX0/IRQ7	PE0/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/ GTIV/RXD5/SMISO5/SSCL5/SSLA2/SSL02/ CRX0/IRQ7

100-Pin	RX66T	RX26T
18	TRST#/PD7/MTIOC9A/MTIOC9A#/ GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/ TMRI1/TMRI5/TXD5/SMOSI5/SSDA5/ SSLA1/CTX0/IRQ8	TRST#/PD7/MTIOC9A/MTIOC9A#/TMRI1/ TMRI5/GTIOC0A/GTIOC3A/GTIOC0A#/ GTIOC3A#/GTIU/TXD5/SMOSI5/SSDA5/ SCK009/TXD008/TXDA008/SMOSI008/ SSDA008/TXDB009/SSLA1/SSL01/CTX0/ IRQ8
19	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/ GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/ CTS1#/RTS1#/SS1#/CTS11#/RTS11#/ SS11#/SSLA0/IRQ5/ADST0	TMS/PD6/MTIOC9C/MTIOC9C#/TMO1/ GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/ GTIW/CTS1#/RTS1#/SS1#/RXD12/ SMISO12/SSCL12/RXDX12/CTS011#/ RTS011#/SS011#/DE011/SSLA0/SSL00/ IRQ5/ADST0
20	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6	TDI/PD5/TMRI0/TMRI6/GTIOC1A/ GTETRGA/GTIOC1A#/GTIOC7A/RXD1/ SMISO1/SSCL1/RXD011/SMISO011/ SSCL011/SSL00/IRQ6
21	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/ TMCI0/TMCI6/SCK1/SCK11/IRQ2	TCK/PD4/TMCI0/TMCI6/GTIOC1B/ GTETRGB/GTIOC1B#/SCK1/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SCK011/TXDB011/SSL02/IRQ2
22	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11	TDO/PD3/TMO0/GTIOC2A/GTETRGC/ GTIOC2A#/GTIOC7B/TXD1/SMOSI1/ SSDA1/TXD011/TXDA011/SMOSI011/ SSDA011/MOSI0
23	TRCLK/PD2/A7/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/TMCI1/TMO4/SCK5/ SCK8/MOSIA	PD2/TMCI1/TMO4/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/SCK5/SCK008/ TXDB008/MOSIA/MOSI0
24	TRDATA3/PD1/A6/GTIOC3A/GTIOC0B/ GTIOC3A#/GTIOC0B#/TMO2/RXD8/ SMISO8/SSCL8/MISOA	PD1/TMO2/GTIOC3A/GTIOC0B/GTIOC3A#/ GTIOC0B#/RXD008/SMISO008/SSCL008/ MISOA/MISO0
25	TRDATA2/PD0/A5/GTIOC3B/GTIOC1A/ GTIOC3B#/GTIOC1A#/TMO6/TXD8/ SMOSI8/SSDA8/RSPCKA	PD0/TMO6/GTIOC3B/GTIOC1A/GTIOC3B#/ GTIOC1A#/TXD008/TXDA008/SMOSI008/ SSDA008/RSPCKA/RSPCK0
26	TRDATA1/PB7/A4/GTIOC1B/GTIOC1B#/ SCK5/SCK11/SCK12	PB7/GTIOC1B/GTIOC1B#/SCK5/SCK12/ SCK011/TXDB011/SSL03
27	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/ RXD5/SMISO5/SSCL5/RXD11/SMISO11/ SSCL11/RXD12/SMISO12/SSCL12/RXDX12/ CRX0/IRQ2	PB6/GTIOC2A/GTIOC3A/GTIOC2A#/ GTIOC3A#/TOC0/RXD5/SMISO5/SSCL5/ RXD12/SMISO12/SSCL12/RXDX12/ RXD011/SMISO011/SSCL011/MISO0/CRX0/ IRQ2
28	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/ TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/ SSDA11/TXD12/SMOSI12/SSDA12/TXDX12/ SIOX12/CTX0	PB5/GTIOC2B/GTIOC3B/GTIOC2B#/ GTIOC3B#/TIC0/TXD5/SMOSI5/SSDA5/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ TXD011/TXDA011/SMOSI011/SSDA011/ RSPCK0/CTX0
29	VCC	VCC
30	PB4/A1/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/IRQ3-DS	PB4/POE8#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/GTCPPO0/CTS5#/ RTS5#/SS5#/RXD12/SMISO12/SSCL12/ RXDX12/CTS011#/RTS011#/SS011#/ SCK011/TXDB011/MISOA/SSL01/CRX0/ IRQ3
31	VSS	VSS

100-Pin	RX66T	RX26T
32	PB3/A7*1/MTIOC0A/MTIOC0A#/CACREF/ SCK6/RSPCKA/IRQ9	PB3/MTIOC0A/MTIOC0A#/CACREF/GTIU/ TOC1/SCK6/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTS009#/RTS009#/ SS009#/DE009/RSPCKA/CTX0/IRQ9
33	PB2/A6*1/MTIOC0B/MTIOC0B#/GTADSM0/ TMRI0/TXD6/SMOSI6/SSDA6/SDA0/ADSM0	PB2/MTIOC0B/MTIOC0B#/TMRI0/ GTADSM0/GTIOC7A/GTIOC7A#/GTIV/ TIC1/TXD6/SMOSI6/SSDA6/SDA0/SDA00/ ADSM0
34	PB1/A5*1/MTIOC0C/MTIOC0C#/GTADSM1/ TMCI0/RXD6/SMISO6/SSCL6/SCL0/IRQ4/ ADSM1	PB1/MTIOC0C/MTIOC0C#/TMCI0/ GTADSM1/GTIOC7B/GTIOC7B#/GTIW/ TOC2/RXD6/SMISO6/SSCL6/SCL0/SCL00/ IRQ4/ADSM1
35	PB0/A0/A4*1/BC0#/MTIOC0D/MTIOC0D#/ TMO0/TXD6/SMOSI6/SSDA6/CTS11#/ RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#	PB0/MTIOC0D/MTIOC0D#/TMO0/TIC2/ TXD6/SMOSI6/SSDA6/TXD008/TXDA008/ SMOSI008/SSDA008/CTS011#/RTS011#/ SS011#/DE011/MOSIA/MOSI0/IRQ8/ ADTRG2#
36	PA5/A3*1/MTIOC1A/MTIOC1A#/TMCI3/ RXD6/SMISO6/SSCL6/RXD8/SMISO8/ SSCL8/MISOA/IRQ1/ADTRG1#	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/ SMISO6/SSCL6/RXD008/SMISO008/ SSCL008/MISOA/MISO0/IRQ1/ADTRG1#
37	PA4/A2*1/MTIOC1B/MTIOC1B#/TMCI7/ SCK6/TXD8/SMOSI8/SSDA8/RSPCKA/ ADTRG0#	PA4/MTIOC1B/MTIOC1B#/TMCI7/SCK6/ TXD008/TXDA008/SMOSI008/SSDA008/ RSPCKA/RSPCK0/ADTRG0#
38	PA3/A1*1/MTIOC2A/MTIOC2A#/GTADSM0/ TMRI7/TXD9/SMOSI9/SSDA9/SCK8/SSLA0	PA3/MTIOC2A/MTIOC2A#/TMRI7/ GTADSM0/TXD009/TXDA009/SMOSI009/ SSDA009/SCK008/TXDB008/SSLA0/SSL00
39	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/ GTADSM1/TMO7/CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/SCK11*1/SSLA1	PA2/MTIOC2B/MTIOC2B#/TMO7/ GTADSM1/CTS6#/RTS6#/SS6#/RXD009/ SMISO009/SSCL009/SSLA1/SSL01
40	PA1/MTIOC6A/MTIOC6A#/TMO4/TXD9/ SMOSI9/SSDA9/RXD11/SMISO11/SSCL11/ SSLA2/CRX0/IRQ14-DS/ADTRG0#	PA1/MTIOC6A/MTIOC6A#/TMO4/GTCPPO4/ TXD009/TXDA009/SMOSI009/SSDA009/ RXD011/SMISO011/SSCL011/SSLA2/ SSL02/CRX0/IRQ14/ADTRG0#
41	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK9/ TXD11/SMOSI11/SSDA11/SSLA3/CTX0	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK009/ TXD011/TXDA011/SMOSI011/SSDA011/ TXDB009/SSLA3/SSL03/CTX0
42	VCC	VCC
43	P96/CS0#/WAIT#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE4#/CTS8#/ RTS8#/SS8#/IRQ4-DS	P96/POE4#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/GTCPPO4/CTS008#/ RTS008#/SS008#/DE008/SSL03/IRQ4/ RSPCK0
44	VSS	VSS
45	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#	P95/MTIOC6B/MTIOC1A/MTIOC6B#/ MTIOC1A#/TMCI3/GTIOC4A/GTIOC7A/ GTIOC4A#/GTIOC7A#/GTOUUP/RXD6/ SMISO6/SSCL6/RXD008/SMISO008/ SSCL008/MISOA/SSL02/IRQ1/ADTRG1#/ MISO0
46	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#	P94/MTIOC7A/MTIOC2A/MTIOC7A#/ MTIOC2A#/TMRI7/GTIOC5A/GTADSM0/ GTIOC5A#/GTOVUP/TXD009/TXDA009/ SMOSI009/SSDA009/SCK008/TXDB008/ SSLA0/SSL00

100-Pin	RX66T	RX26T
47	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#	P93/MTIOC7B/MTIOC6A/MTIOC7B#/ MTIOC6A#/TMO4/GTIOC6A/GTIOC6A#/ GTOWUP/TXD009/TXDA009/SMOSI009/ SSDA009/RXD011/SMISO011/SSCL011/ SSLA2/SSL02/MOSI0/CRX0/IRQ14/ ADTRG0#
48	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#	P92/MTIOC6D/MTIOC6C/MTIOC6D#/ MTIOC6C#/TMO2/GTIOC4B/GTIOC7B/ GTIOC4B#/GTIOC7B#/GTOULO/SCK009/ TXD011/TXDA011/SMOSI011/SSDA011/ TXDB009/SSLA3/SSL03/MISO0/CTX0
49	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC5B#/GTOVLO/RXD5/SMISO5/SSCL5/ RSPCK0
50	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC6B#/GTOWLO/TXD5/SMOSI5/ SSDA5/SSL01
51	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC6B/GTIOC2B#/GTIOC6B#/GTOWLO/ SSL03
52	P75/D1[A1/D1]/MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC5B/GTIOC1B#/GTIOC5B#/GTOVLO/ SSL02
53	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC4B/GTIOC0B#/GTIOC4B#/GTOULO/ SSL01
54	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC6A/GTIOC2A#/GTIOC6A#/GTOWUP/ SSL00
55	P72/D4[A4/D4]/MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC5A/GTIOC1A#/GTIOC5A#/GTOVUP/ MOSI0
56	P71/D5[A5/D5]/MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC4A/GTIOC0A#/GTIOC4A#/GTOUUP/ MISO0
57	P70/D6[A6/D6]/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE0#/CTS9#/ RTS9#/SS9#/IRQ5-DS	P70/MTIOC0A/MTCLKC/MTIOC0A#/ MTCLKC#/TMRI6/POE0#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/ GTCPPO0/SCK5/CTS009#/RTS009#/ SS009#/DE009/SSLA0/RSPCK0/IRQ5
58	P33/D7[A7/D7]/MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/GTIOC3B/GTIOC3B#/ TMO0/SSLA3/IRQ13-DS	P33/MTIOC3A/MTCLKA/MTIOC3A#/ MTCLKA#/TMO0/GTIOC3B/GTIOC7B/ GTIOC3B#/GTIOC7B#/GTCPPO0/SSLA3/ SSL03/IRQ13
59	P32/D8[A8/D8]/MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/GTIOC3A/GTIOC3A#/ TMO6/SSLA2/IRQ12-DS	P32/MTIOC3C/MTCLKB/MTIOC3C#/ MTCLKB#/TMO6/GTIOC3A/GTIOC7A/ GTIOC3A#/GTIOC7A#/SSLA2/SSL02/IRQ12
60	VCC	VCC
61	P31/D9[A9/D9]/MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6	P31/MTIOC0A/MTCLKC/MTIOC0A#/ MTCLKC#/TMRI6/GTIU/SSLA1/SSL01/IRQ6
62	VSS	VSS
63	P30/D10[A10/D10]/MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/TMCI6/SCK8/CTS8#/ RTS8#/SS8#/SSLA0/IRQ7/COMP3	P30/MTIOC0B/MTCLKD/MTIOC0B#/ MTCLKD#/TMCI6/GTIV/SCK008/CTS008#/ RTS008#/SS008#/DE008/SSLA0/SSL00/ IRQ7/COMP3

100-Pin	RX66T	RX26T
64	P24/D11[A11/D11]/MTIC5U/MTIC5U#/TMCI2/TMO6/CTS8#/RTS8#/SS8#/SCK8/RSPCKA/IRQ4/COMP0	P27/MTIOC1A/MTIOC0C/MTIOC1A#/MTIOC0C#/TMO2/TMO6/POE9#/RSPCKA/RSPCK0/IRQ15
65	P23/D12[A12/D12]/MTIC5V/MTIC5V#/TMO2/CACREF/TXD8/SMOSI8/SSDA8/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/MOSIA/CTX0/IRQ11/COMP1	P24/MTIC5U/MTIC5U#/TMCI2/TMO6/CTS008#/RTS008#/SS008#/SCK008/DE008/RSPCKA/RSPCK0/IRQ4/COMP0
66	P22/D13[A13/D13]/MTIC5W/MTCLKD/MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/TMO4/RXD8/SMISO8/SSCL8/RXD12/SMISO12/SSCL12/RXDX12/MISOA/CRX0/IRQ10/ADTRG2#/COMP2	P23/MTIC5V/MTIC5V#/TMO2/CACREF/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/TXD008/TXDA008/SMOSI008/SSDA008/MOSIA/MOSI0/CTX0/IRQ11/COMP1
67	P21/D14[A14/D14]/MTIOC9A/MTCLKA/MTIOC9A#/MTCLKA#/TMCI4/TXD8/SMOSI8/SSDA8/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/MOSIA/IRQ6-DS/AN217/ADTRG1#/COMP5	P22/MTIC5W/MTCLKD/MTIC5W#/MTCLKD#/TMRI2/TMO4/MTIOC9B/GTIV/RXD12/SMISO12/SSCL12/RXDX12/RXD008/SMISO008/SSCL008/SCK008/TXDB008/MISOA/MISO0/CRX0/IRQ10/ADTRG2#/COMP2
68	P20/D15[A15/D15]/MTIOC9C/MTCLKB/MTIOC9C#/MTCLKB#/TMRI4/CTS8#/RTS8#/SS8#/SCK8/RSPCKA/IRQ7-DS/AN216/ADTRG0#/COMP4	P21/MTIOC9A/MTCLKA/MTIOC9A#/MTCLKA#/TMCI4/TMO6/GTIU/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/TXD008/TXDA008/SMOSI008/SSDA008/MOSIA/MOSI0/IRQ6/AN217/ADTRG1#/COMP5
69	P65/A12/IRQ9/AN211/CMPC53/DA1	P20/MTIOC9C/MTCLKB/MTIOC9C#/MTCLKB#/TMRI4/TMO2/GTIW/CTS008#/RTS008#/SS008#/RXD008/SMISO008/SSCL008/DE008/RSPCKA/RSPCK0/IRQ7/AN216/ADTRG0#/COMP4
70	P64/A13/IRQ8/AN210/CMPC33/DA0	P65/IRQ9/AN211/CMPC53/DA1
71	AVCC2	P64/IRQ8/AN210/CMPC33/DA0
72	AVCC2	AVCC2
73	AVSS2	AVSS2
74	P63/A12*1/A14/IRQ7/AN209/CMPC23	P63/IRQ7/AN209/CMPC23
75	P62/A13*1/A15/IRQ6/AN208/CMPC43	P62/IRQ6/AN208/CMPC43
76	P61/A14*1/A16/IRQ5/AN207/CMPC13	P61/IRQ5/AN207/CMPC13
77	P60/A15*1/A17/IRQ4/AN206/CMPC03	P60/IRQ4/AN206/CMPC03
78	P55/A16*1/A18/IRQ3/AN203/CMPC32	P55/IRQ3/AN203/CMPC32
79	P54/A17*1/A19/IRQ2/AN202/CMPC22	P54/IRQ2/AN202/CMPC22/CVREFC1
80	P53/A18*1/A20/IRQ1/AN201/CMPC12	P53/IRQ1/AN201/CMPC12/CVREFC0
81	P52/IRQ0/AN200/CMPC02	P52/IRQ0/AN200/CMPC02
82	P51/AN205/CMPC52	P51/AN205/CMPC52
83	P50/AN204/CMPC42	P50/AN204/CMPC42
84	P47/AN103	P47/AN103
85	P46/AN102/CMPC50/CMPC51	P46/AN102/CMPC50/CMPC51
86	P45/AN101/CMPC40/CMPC41	P45/AN101/CMPC40/CMPC41
87	P44/AN100/CMPC30/CMPC31	P44/AN100/CMPC30/CMPC31
88	P43/AN003	P43/AN003
89	P42/AN002/CMPC20/CMPC21	P42/AN002/CMPC20/CMPC21
90	P41/AN001/CMPC10/CMPC11	P41/AN001/CMPC10/CMPC11
91	P40/AN000/CMPC00/CMPC01	P40/AN000/CMPC00/CMPC01
92	AVCC1	AVCC1
93	AVCC0	AVCC0

100-Pin	RX66T	RX26T
94	AVSS0	AVSS0
95	AVSS1	AVSS1
96	P82/ALE/WAIT#/MTIC5U/MTIC5U#/TMO4/ SCK6/SCK12/IRQ3/COMP5	P82/MTIC5U/MTIC5U#/TMO4/SCK6/SCK12/ IRQ3/COMP5
97	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/TXD6/ SMOSI6/SSDA6/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/COMP4	P81/MTIC5V/MTIC5V#/TMCI4/TXD6/ SMOSI6/SSDA6/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/COMP4
98	P80/CS1#/MTIC5W/MTIC5W#/TMRI4/RXD6/ SMISO6/SSCL6/RXD12/SMISO12/SSCL12/ RXDX12/IRQ5/COMP3	P80/MTIC5W/MTIC5W#/TMRI4/RXD6/ SMISO6/SSCL6/RXD12/SMISO12/SSCL12/ RXDX12/IRQ5/COMP3
99	P11/RD#/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/MTIOC9D/GTIOC3B/GTETRGA/ GTIOC3B#/GTETRGC/TMO3/POE9#/ IRQ1-DS	P11/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/TMO3/POE9#/MTIOC9D/ GTIOC3B/GTETRGA/GTIOC3B#/GTETRGC/ GTCPPO0/TOC3/SCK009/SCK008/ TXDB009/IRQ1
100	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0-DS	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/TMRI3/POE12#/GTIOC3A/ GTETRGB/GTIOC3A#/GTETRGD/GTIV/ TIC3/CTS6#/RTS6#/SS6#/TXD009/ TXDA009/SMOSI009/SSDA009/IRQ0

Note: 1. Only for products with RAM capacity 128 KB

3.2 80-Pin Package

Table 3.2 is Comparative Listing of 80-Pin Package Pin Functions.

Table 3.2 Comparative Listing of 80-Pin Package Pin Functions

80-Pin	RX66T (80-Pin LQFP and 80-Pin LFQFP)	RX26T (80-Pin LFQFP)
1	EMLE	EMLE/PN7/MTIOC9D/MTIOC9D#/IRQ5/ ADST0
2	VSS	VSS
3	UB/P00/MTIOC9A/MTIOC9A#/CACREF/ RXD9/SMISO9/SSCL9/RXD12/SMISO12/ SSCL12/RXDX12/IRQ2/ADST1/COMP0	P00/MTIOC9A/MTIOC9A#/CACREF/GTIU/ TIC3/RXD12/SMISO12/SSCL12/RXDX12/ RXD009/SMISO009/SSCL009/IRQ2/ADST1/ COMP0
4	VCL	VCL
5	MD/FINED	MD/FINED/PN6
6	P01/MTIOC9C/MTIOC9C#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE12#/ TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/IRQ4/ADST2/ COMP1	P01/MTIOC9C/MTIOC9C#/POE12#/ GTETRGA/GTETRGB/GTETRGC/ GTETRGD/GTIW/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/TXD009/TXDA009/ SMOSI009/SSDA009/IRQ4/ADST2/COMP1
7	PE4/MTCLKC/MTCLKC#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE10#/ SCK9/IRQ1	PE4/MTCLKC/MTCLKC#/POE10#/ GTETRGA/GTETRGB/GTETRGC/ GTETRGD/SCK009/TXDB009/IRQ1
8	PE3/MTCLKD/MTCLKD#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE11#/ CTS9#/RTS9#/SS9#/IRQ2-DS	PE3/MTCLKD/MTCLKD#/POE11#/ GTETRGA/GTETRGB/GTETRGC/ GTETRGD/CTS009#/RTS009#/SS009#/ DE009/IRQ2
9	RES#	RES#
10	XTAL/P37	XTAL/P37/RXD5/SMISO5/SSCL5
11	VSS	VSS
12	EXTAL/P36	EXTAL/P36/TXD5/SMOSI5/SSDA5
13	VCC	VCC
14	PE2/POE10#/NMI	PE2/POE10#/NMI/IRQ0
15	TRST#/PD7/MTIOC9A/MTIOC9A#/ GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/ TMRI1/TMRI5/TXD5/SMOSI5/SSDA5/ SSLA1/CTX0/IRQ8	TRST#/PD7/MTIOC9A/MTIOC9A#/TMRI1/ TMRI5/GTIOC0A/GTIOC3A/GTIOC0A#/ GTIOC3A#/GTIU/TXD5/SMOSI5/SSDA5/ SCK009/TXD008/TXDA008/SMOSI008/ SSDA008/TXDB009/SSLA1/SSL01/CTX0/ IRQ8
16	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/ GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/ CTS1#/RTS1#/SS1#/CTS11#/RTS11#/ SS11#/SSLA0/IRQ5/ADST0	TMS/PD6/MTIOC9C/MTIOC9C#/TMO1/ GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/ GTIW/CTS1#/RTS1#/SS1#/RXD12/ SMISO12/SSCL12/RXDX12/CTS011#/ RTS011#/SS011#/DE011/SSLA0/SSL00/ IRQ5/ADST0
17	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6	TDI/PD5/TMRI0/TMRI6/GTIOC1A/ GTETRGA/GTIOC1A#/GTIOC7A/RXD1/ SMISO1/SSCL1/RXD011/SMISO011/ SSCL011/SSL00/IRQ6
18	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/ TMCI0/TMCI6/SCK1/SCK11/IRQ2	TCK/PD4/TMCI0/TMCI6/GTIOC1B/ GTETRGB/GTIOC1B#/SCK1/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SCK011/TXDB011/SSL02/IRQ2

80-Pin	RX66T (80-Pin LQFP and 80-Pin LFQFP)	RX26T (80-Pin LFQFP)
19	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11	TDO/PD3/TMO0/GTIOC2A/GTETRGC/ GTIOC2A#/GTIOC7B/TXD1/SMOSI1/ SSDA1/TXD011/TXDA011/SMOSI011/ SSDA011/MOSI0
20	PD2/GTIOC2B/GTIOC0A/GTIOC2B#/ GTIOC0A#/TMCI1/TMO4/SCK5/SCK8/ MOSIA	PD2/TMCI1/TMO4/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/SCK5/SCK008/ TXDB008/MOSIA/MOSI0
21	PB6/GTIOC2A/GTIOC2A#/RXD5/SMISO5/ SSCL5/RXD11/SMISO11/SSCL11/RXD12/ SMISO12/SSCL12/RXDX12/CRX0/IRQ2	PB6/GTIOC2A/GTIOC3A/GTIOC2A#/ GTIOC3A#/TOC0/RXD5/SMISO5/SSCL5/ RXD12/SMISO12/SSCL12/RXDX12/ RXD011/SMISO011/SSCL011/MISO0/CRX0/ IRQ2
22	PB5/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/ SSDA5/TXD11/SMOSI11/SSDA11/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/CTX0	PB5/GTIOC2B/GTIOC3B/GTIOC2B#/ GTIOC3B#/TIC0/TXD5/SMOSI5/SSDA5/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ TXD011/TXDA011/SMOSI011/SSDA011/ RSPCK0/CTX0
23	VCC	VCC
24	PB4/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/IRQ3-DS	PB4/POE8#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/GTCPPO0/CTS5#/ RTS5#/SS5#/RXD12/SMISO12/SSCL12/ RXDX12/CTS011#/RTS011#/SS011#/ SCK011/TXDB011/MISOA/SSL01/CRX0/ IRQ3
25	VSS	VSS
26	PB3/MTIOC0A/MTIOC0A#/CACREF/SCK6/ RSPCKA/IRQ9	PB3/MTIOC0A/MTIOC0A#/CACREF/GTIU/ TOC1/SCK6/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTS009#/RTS009#/ SS009#/DE009/RSPCKA/CTX0/IRQ9
27	PB2/MTIOC0B/MTIOC0B#/GTADSM0/ TMRI0/TXD6/SMOSI6/SSDA6/SDA0/ADSM0	PB2/MTIOC0B/MTIOC0B#/TMRI0/ GTADSM0/GTIOC7A/GTIOC7A#/GTIV/TIC1/ TXD6/SMOSI6/SSDA6/SDA0/SDA00/ADSM0
28	PB1/MTIOC0C/MTIOC0C#/GTADSM1/ TMCI0/RXD6/SMISO6/SSCL6/SCL0/IRQ4/ ADSM1	PB1/MTIOC0C/MTIOC0C#/TMCI0/ GTADSM1/GTIOC7B/GTIOC7B#/GTIW/ TOC2/RXD6/SMISO6/SSCL6/SCL0/SCL00/ IRQ4/ADSM1
29	PB0/MTIOC0D/MTIOC0D#/TMO0/TXD6/ SMOSI6/SSDA6/CTS11#/RTS11#/SS11#/ MOSIA/IRQ8/ADTRG2#	PB0/MTIOC0D/MTIOC0D#/TMO0/TIC2/ TXD6/SMOSI6/SSDA6/TXD008/TXDA008/ SMOSI008/SSDA008/CTS011#/RTS011#/ SS011#/DE011/MOSIA/MOSI0/IRQ8/ ADTRG2#
30	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/ SMISO6/SSCL6/RXD8/SMISO8/SSCL8/ MISOA/IRQ1/ADTRG1#	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/ SMISO6/SSCL6/RXD008/SMISO008/ SSCL008/MISOA/MISO0/IRQ1/ADTRG1#
31	PA3/MTIOC2A/MTIOC2A#/GTADSM0/ TMRI7/TXD9/SMOSI9/SSDA9/SCK8/SSLA0	PA3/MTIOC2A/MTIOC2A#/TMRI7/ GTADSM0/TXD009/TXDA009/SMOSI009/ SSDA009/SCK008/TXDB008/SSLA0/SSL00
32	VCC	VCC
33	P96/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE4#/CTS8#/RTS8#/SS8#/ IRQ4-DS	P96/POE4#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/GTCPPO4/CTS008#/ RTS008#/SS008#/DE008/SSL03/IRQ4/ RSPCK0
34	VSS	VSS

80-Pin	RX66T (80-Pin LQFP and 80-Pin LFQFP)	RX26T (80-Pin LFQFP)
35	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#	P95/MTIOC6B/MTIOC1A/MTIOC6B#/ MTIOC1A#/TMCI3/GTIOC4A/GTIOC7A/ GTIOC4A#/GTIOC7A#/GTOUUP/RXD6/ SMISO6/SSCL6/RXD008/SMISO008/ SSCL008/MISOA/SSL02/MISO0/IRQ1/ ADTRG1#
36	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#	P94/MTIOC7A/MTIOC2A/MTIOC7A#/ MTIOC2A#/TMRI7/GTIOC5A/GTADSM0/ GTIOC5A#/GTOVUP/TXD009/TXDA009/ SMOSI009/SSDA009/SCK008/TXDB008/ SSLA0/SSL00
37	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#	P93/MTIOC7B/MTIOC6A/MTIOC7B#/ MTIOC6A#/TMO4/GTIOC6A/GTIOC6A#/ GTOWUP/TXD009/TXDA009/SMOSI009/ SSDA009/RXD011/SMISO011/SSCL011/ SSLA2/SSL02/MOSI0/CRX0/IRQ14/ ADTRG0#
38	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#	P92/MTIOC6D/MTIOC6C/MTIOC6D#/ MTIOC6C#/TMO2/GTIOC4B/GTIOC7B/ GTIOC4B#/GTIOC7B#/GTOULO/SCK009/ TXD011/TXDA011/SMOSI011/SSDA011/ TXDB009/SSLA3/SSL03/MISO0/CTX0
39	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC5B#/GTOVLO/RXD5/SMISO5/SSCL5/ RSPCK0
40	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC6B#/GTOWLO/TXD5/SMOSI5/ SSDA5/SSL01
41	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC6B/GTIOC2B#/GTIOC6B#	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC6B/GTIOC2B#/GTIOC6B#/GTOWLO/ SSL03
42	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC5B/GTIOC1B#/GTIOC5B#	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC5B/GTIOC1B#/GTIOC5B#/GTOVLO/ SSL02
43	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC4B/GTIOC0B#/GTIOC4B#	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC4B/GTIOC0B#/GTIOC4B#/GTOULO/ SSL01
44	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC6A/GTIOC2A#/GTIOC6A#	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC6A/GTIOC2A#/GTIOC6A#/GTOWUP/ SSL00
45	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC5A/GTIOC1A#/GTIOC5A#	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC5A/GTIOC1A#/GTIOC5A#/GTOVUP/ MOSI0
46	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC4A/GTIOC0A#/GTIOC4A#	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC4A/GTIOC0A#/GTIOC4A#/GTOUUP/ MISO0
47	P70/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE0#/CTS9#/RTS9#/SS9#/ IRQ5-DS	P70/MTIOC0A/MTCLKC/MTIOC0A#/ MTCLKC#/TMRI6/POE0#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/ GTCPPO0/SCK5/CTS009#/RTS009#/ SS009#/DE009/SSLA0/RSPCK0/IRQ5
48	VCC	VCC
49	P31/MTIOC0A/MTCLKC/MTIOC0A#/ MTCLKC#/TMRI6/SSLA1/IRQ6	P31/MTIOC0A/MTCLKC/MTIOC0A#/ MTCLKC#/TMRI6/GTIU/SSLA1/SSL01/IRQ6
50	VSS	VSS

80-Pin	RX66T (80-Pin LQFP and 80-Pin LFQFP)	RX26T (80-Pin LFQFP)
51	P30/MTIOC0B/MTCLKD/MTIOC0B#/ MTCLKD#/TMCI6/SCK8/CTS8#/RTS8#/ SS8#/SSLA0/IRQ7/COMP3	P30/MTIOC0B/MTCLKD/MTIOC0B#/ MTCLKD#/TMCI6/GTIV/SCK008/CTS008#/ RTS008#/SS008#/DE008/SSLA0/SSL00/ IRQ7/COMP3
52	P27/MTIOC1A/MTIOC0C/MTIOC1A#/ MTIOC0C#/POE9#/IRQ15	P27/MTIOC1A/MTIOC0C/MTIOC1A#/ MTIOC0C#/TMO2/TMO6/POE9#/RSPCKA/ RSPCK0/IRQ15
53	P22/MTIC5W/MTCLKD/MTIC5W#/ MTCLKD#/MTIOC9B/TMRI2/TMO4/RXD8/ SMISO8/SSCL8/RXD12/SMISO12/SSCL12/ RXDX12/MISOA/CRX0/IRQ10/ADTRG2#/ COMP2	P22/MTIC5W/MTCLKD/MTIC5W#/ MTCLKD#/TMRI2/TMO4/MTIOC9B/GTIV/ RXD12/SMISO12/SSCL12/RXDX12/ RXD008/SMISO008/SSCL008/SCK008/ TXDB008/MISOA/MISO0/CRX0/IRQ10/ ADTRG2#/COMP2
54	P21/MTIOC9A/MTCLKA/MTIOC9A#/ MTCLKA#/TMCI4/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ MOSIA/IRQ6-DS/AN217/ADTRG1#/COMP5	P21/MTIOC9A/MTCLKA/MTIOC9A#/ MTCLKA#/TMCI4/TMO6/GTIU/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ TXD008/TXDA008/SMOSI008/SSDA008/ MOSIA/MOSI0/IRQ6/AN217/ADTRG1#/ COMP5
55	P20/MTIOC9C/MTCLKB/MTIOC9C#/ MTCLKB#/TMRI4/CTS8#/RTS8#/SS8#/ SCK8/RSPCKA/IRQ7-DS/AN216/ADTRG0#/ COMP4	P20/MTIOC9C/MTCLKB/MTIOC9C#/ MTCLKB#/TMRI4/TMO2/GTIW/CTS008#/ RTS008#/SS008#/RXD008/SMISO008/ SSCL008/DE008/RSPCKA/RSPCK0/IRQ7/ AN216/ADTRG0#/COMP4
56	P65/IRQ9/AN211/CMPC53/DA1	P65/IRQ9/AN211/CMPC53/DA1
57	P64/IRQ8/AN210/CMPC33/DA0	P64/IRQ8/AN210/CMPC33/DA0
58	AVCC2	AVCC2
59	AVSS2	AVSS2
60	P62/IRQ6/AN208/CMPC43	P60/IRQ4/AN206/CMPC03
61	P55/IRQ3/AN203/CMPC32	P55/IRQ3/AN203/CMPC32
62	P54/IRQ2/AN202/CMPC22	P54/IRQ2/AN202/CMPC22/CVREFC1
63	P53/IRQ1/AN201/CMPC12	P53/IRQ1/AN201/CMPC12/CVREFC0
64	P52/IRQ0/AN200/CMPC02	P52/IRQ0/AN200/CMPC02
65	P47/AN103	P51/AN205/CMPC52
66	P46/AN102/CMPC50/CMPC51	P50/AN204/CMPC42
67	P45/AN101/CMPC40/CMPC41	P47/AN103
68	P44/AN100/CMPC30/CMPC31	P46/AN102/CMPC50/CMPC51
69	PH4/AN107/PGAVSS1	P45/AN101/CMPC40/CMPC41
70	P43/AN003	P44/AN100/CMPC30/CMPC31
71	P42/AN002/CMPC20/CMPC21	P43/AN003
72	P41/AN001/CMPC10/CMPC11	P42/AN002/CMPC20/CMPC21
73	P40/AN000/CMPC00/CMPC01	P41/AN001/CMPC10/CMPC11
74	PH0/AN007/PGAVSS0	P40/AN000/CMPC00/CMPC01
75	AVCC1	AVCC1
76	AVCC0	AVCC0
77	AVSS0	AVSS0
78	AVSS1	AVSS1
79	P11/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/MTIOC9D/GTIOC3B/GTETRGA/ GTIOC3B#/GTETRGC/TMO3/POE9#/ IRQ1-DS	P11/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/TMO3/POE9#/MTIOC9D/ GTIOC3B/GTETRGA/GTIOC3B#/GTETRGC/ GTCPPO0/TOC3/SCK009/SCK008/ TXDB009/IRQ1

80-Pin	RX66T (80-Pin LQFP and 80-Pin LFQFP)	RX26T (80-Pin LFQFP)
80	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0-DS	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/TMRI3/POE12#/GTIOC3A/ GTETRGB/GTIOC3A#/GTETRGD/GTIV/ TIC3/CTS6#/RTS6#/SS6#/TXD009/ TXDA009/SMOSI009/SSDA009/IRQ0

3.3 64-Pin Package

Table 3.3 is Comparative Listing of 64-Pin Package Pin Functions.

Table 3.3 Comparative Listing of 64-Pin Package Pin Functions

64-Pin	RX66T (64-Pin LFQFP)	RX26T (64-Pin LFQFP and 64-Pin HWQFN)
1	EMLE	EMLE/PN7/MTIOC9D/MTIOC9D#/IRQ5/ ADST0
2	UB/P00/MTIOC9A/MTIOC9A#/CACREF/ RXD9/SMISO9/SSCL9/RXD12/SMISO12/ SSCL12/RXDX12/IRQ2/ADST1/COMP0	P00/MTIOC9A/MTIOC9A#/CACREF/GTIU/ TIC3/RXD12/SMISO12/SSCL12/RXDX12/ RXD009*1/SMISO009*1/SSCL009*1/IRQ2/ ADST1*1/ COMP0
3	VCL	VCL
4	MD/FINED	MD/FINED/PN6
5	P01/MTIOC9C/MTIOC9C#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE12#/ TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/IRQ4/ADST2/ COMP1	P01/MTIOC9C/MTIOC9C#/POE12#/ GTETRGA/GTETRGB/GTETRGC/ GTETRGD/GTIW/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/TXD009*1/TXDA009*1/ SMOSI009*1/SSDA009*1/IRQ4/ADST2/ COMP1
6	RES#	RES#
7	XTAL/P37	XTAL/P37/RXD5/SMISO5/SSCL5
8	VSS	VSS
9	EXTAL/P36	EXTAL/P36/TXD5/SMOSI5/SSDA5
10	VCC	VCC
11	PE2/POE10#/NMI	PE2/POE10#/NMI/IRQ0
12	TRST#/PD7/MTIOC9A/MTIOC9A#/ GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/ TMRI1/TMRI5/TXD5/SMOSI5/SSDA5/ SSLA1/CTX0/IRQ8	TRST#/PD7/MTIOC9A/MTIOC9A#/TMRI1/ TMRI5/GTIOC0A/GTIOC3A/GTIOC0A#/ GTIOC3A#/GTIU/TXD5/SMOSI5/SSDA5/ SCK009*1/TXD008*1/TXDA008*1/SMOSI008*1/ SSDA008*1/TXDB009*1/SSLA1/SSL01*1/ CTX0/ IRQ8
13	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/ GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/ CTS1#/RTS1#/SS1#/CTS11#/RTS11#/ SS11#/SSLA0/IRQ5/ADST0	TMS/PD6/MTIOC9C/MTIOC9C#/TMO1/ GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/ GTIW/CTS1#/RTS1#/SS1#/RXD12/ SMISO12/SSCL12/RXDX12/CTS011#*1/ RTS011#*1/SS011#*1/DE011*1/SSLA0/ SSL00*1/ IRQ5/ADST0
14	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6	TDI/PD5/TMRI0/TMRI6/GTIOC1A/ GTETRGA/GTIOC1A#/GTIOC7A/RXD1/ SMISO1/SSCL1/RXD011*1/SMISO011*1/ SSCL011*1/SSL00*1/IRQ6
15	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/ TMCI0/TMCI6/SCK1/SCK11/IRQ2	TCK/PD4/TMCI0/TMCI6/GTIOC1B/ GTETRGB/GTIOC1B#/SCK1/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SCK011*1/TXDB011*1/SSL02*1/IRQ2
16	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11	TDO/PD3/TMO0/GTIOC2A/GTETRGC/ GTIOC2A#/GTIOC7B/TXD1/SMOSI1/ SSDA1/TXD011*1/TXDA011*1/SMOSI011*1/ SSDA011*1/MOSI0
17	PB6/GTIOC2A/GTIOC2A#/RXD5/SMISO5/ SSCL5/RXD11/SMISO11/SSCL11/RXD12/ SMISO12/SSCL12/RXDX12/CRX0/IRQ2	PB6/GTIOC2A/GTIOC3A/GTIOC2A#/ GTIOC3A#/TOC0/RXD5/SMISO5/SSCL5/ RXD12/SMISO12/SSCL12/RXDX12/ RXD011*1/SMISO011*1/SSCL011*1/MISO0*1/ CRX0/ IRQ2

64-Pin	RX66T (64-Pin LFQFP)	RX26T (64-Pin LFQFP and 64-Pin HWQFN)
18	PB5/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/ SSDA5/TXD11/SMOSI11/SSDA11/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/CTX0	PB5/GTIOC2B/GTIOC3B/GTIOC2B#/ GTIOC3B#/TIC0/TXD5/SMOSI5/SSDA5/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ TXD011*1/TXDA011*1/SMOSI011*1/ SSDA011*1/ RSPCK0*1/CTX0
19	PB4/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/IRQ3-DS	PB4/POE8#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/GTCPPO0/CTS5#/ RTS5#/SS5#/RXD12/SMISO12/SSCL12/ RXDX12/CTS011#/RTS011#*1/SS011#*1/ SCK011*1/TXDB011*1/MISOA/SSL01*1/CRX0/ IRQ3
20	PB3/MTIOC0A/MTIOC0A#/CACREF/SCK6/ RSPCKA/IRQ9	PB3/MTIOC0A/MTIOC0A#/CACREF/GTIU/ TOC1/SCK6/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTS009#*1/RTS009#*1/ SS009#*1/DE009*1/RSPCKA/CTX0/IRQ9
21	PB2/MTIOC0B/MTIOC0B#/GTADSM0/ TMRI0/TXD6/SMOSI6/SSDA6/SDA0/ADSM0	PB2/MTIOC0B/MTIOC0B#/TMRI0/ GTADSM0/GTIOC7A/GTIOC7A#/GTIV/TIC1/ TXD6/SMOSI6/SSDA6/SDA0/SDA00*1/ ADSM0
22	PB1/MTIOC0C/MTIOC0C#/GTADSM1/ TMCI0/RXD6/SMISO6/SSCL6/SCL0/IRQ4/ ADSM1	PB1/MTIOC0C/MTIOC0C#/TMCI0/ GTADSM1/GTIOC7B/GTIOC7B#/GTIW/ TOC2/RXD6/SMISO6/SSCL6/SCL0/SCL00*1/ IRQ4/ADSM1
23	PB0/MTIOC0D/MTIOC0D#/TMO0/TXD6/ SMOSI6/SSDA6/CTS11#/RTS11#/SS11#/ MOSIA/IRQ8/ADTRG2#	PB0/MTIOC0D/MTIOC0D#/TMO0/TIC2/ TXD6/SMOSI6/SSDA6/TXD008*1/TXDA008*1/ SMOSI008*1/SSDA008*1/CTS011#*1/ RTS011#*1/SS011#*1/DE011*1/MOSIA/ MOSI0*1/IRQ8/ ADTRG2#
24	VCC	VCC
25	P96/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE4#/CTS8#/RTS8#/SS8#/ IRQ4-DS	P96/POE4#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/GTCPPO4/ CTS008#*1/RTS008#*1/SS008#*1/DE008*1/ SSL03*1/RSPCK0*1/ IRQ4
26	VSS	VSS
27	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#	P95/MTIOC6B/MTIOC1A/MTIOC6B#/ MTIOC1A#/TMCI3/GTIOC4A/GTIOC7A/ GTIOC4A#/GTIOC7A#/GTOUUP/RXD6/ SMISO6/SSCL6/RXD008*1/SMISO008*1/ SSCL008*1/MISOA/SSL02*1/MISO0*1/IRQ1/ ADTRG1#*1
28	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#	P94/MTIOC7A/MTIOC2A/MTIOC7A#/ MTIOC2A#/TMRI7/GTIOC5A/GTADSM0/ GTIOC5A#/GTOVUP/TXD009*1/TXDA009*1/ SMOSI009*1/SSDA009*1/SCK008*1/ TXDB008*1/ SSLA0/SSL00
29	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#	P93/MTIOC7B/MTIOC6A/MTIOC7B#/ MTIOC6A#/TMO4/GTIOC6A/GTIOC6A#/ GTOWUP/TXD009*1/TXDA009*1/ SMOSI009*1/SSDA009*1/RXD011*1/ SMISO011*1/SSCL011*1/SSLA2/SSL02*1/ MOSI0*1/CRX0/IRQ14/ ADTRG0#

64-Pin	RX66T (64-Pin LFQFP)	RX26T (64-Pin LFQFP and 64-Pin HWQFN)
30	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#	P92/MTIOC6D/MTIOC6C/MTIOC6D#/ MTIOC6C#/TMO2/GTIOC4B/GTIOC7B/ GTIOC4B#/GTIOC7B#/GTOULO/SCK009*1/ TXD011*1/TXDA011*1/SMOSI011*1/ SSDA011*1/TXDB009*1/SSLA3/SSL03*1/ MISO0*1/CTX0
31	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC5B#/GTOVLO/RXD5/SMISO5/SSCL5/ RSPCK0*1
32	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC6B#/GTOWLO/TXD5/SMOSI5/ SSDA5/SSL01*1
33	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC6B/GTIOC2B#/GTIOC6B#	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC6B/GTIOC2B#/GTIOC6B#/GTOWLO/ SSL03*1
34	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC5B/GTIOC1B#/GTIOC5B#	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC5B/GTIOC1B#/GTIOC5B#/GTOVLO/ SSL02*1
35	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC4B/GTIOC0B#/GTIOC4B#	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC4B/GTIOC0B#/GTIOC4B#/GTOULO/ SSL01*1
36	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC6A/GTIOC2A#/GTIOC6A#	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC6A/GTIOC2A#/GTIOC6A#/GTOWUP/ SSL00*1
37	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC5A/GTIOC1A#/GTIOC5A#	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC5A/GTIOC1A#/GTIOC5A#/GTOVUP/ MOSI0*1
38	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC4A/GTIOC0A#/GTIOC4A#	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC4A/GTIOC0A#/GTIOC4A#/GTOUUP/ MISO0*1
39	P70/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE0#/CTS9#/RTS9#/SS9#/ IRQ5-DS	P70/MTIOC0A/MTCLKC/MTIOC0A#/ MTCLKC#/TMRI6/POE0#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/ GTCPPO0/SCK5/CTS009#*1/RTS009#*1/ SS009#*1/DE009*1/SSLA0/RSPCK0*1/IRQ5
40	VCC	VCC
41	VSS	VSS
42	P22/MTIC5W/MTCLKD/MTIC5W#/ MTCLKD#/MTIOC9B/TMRI2/TMO4/RXD8/ SMISO8/SSCL8/RXD12/SMISO12/SSCL12/ RXDX12/MISOA/CRX0/IRQ10/ADTRG2#/ COMP2	P22/MTIC5W/MTCLKD/MTIC5W#/ MTCLKD#/TMRI2/TMO4/MTIOC9B/GTIV/ RXD12/SMISO12/SSCL12/RXDX12/ RXD008*1/SMISO008*1/SSCL008*1/SCK008*1/ TXDB008*1/MISOA/MISO0*1/CRX0/IRQ10/ ADTRG2#/COMP2
43	P21/MTIOC9A/MTCLKA/MTIOC9A#/ MTCLKA#/TMCI4/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ MOSIA/IRQ6-DS/AN217/ADTRG1#/COMP5	P21/MTIOC9A/MTCLKA/MTIOC9A#/ MTCLKA#/TMCI4/TMO6/GTIU/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ TXD008*1/TXDA008*1/SMOSI008*1/ SSDA008*1/MOSIA/MOSI0*1/IRQ6/AN217/ ADTRG1#*1/ COMP5
44	P20/MTIOC9C/MTCLKB/MTIOC9C#/ MTCLKB#/TMRI4/CTS8#/RTS8#/SS8#/ SCK8/RSPCKA/IRQ7-DS/AN216/ADTRG0#/ COMP4	P20/MTIOC9C/MTCLKB/MTIOC9C#/ MTCLKB#/TMRI4/TMO2/GTIW/CTS008#*1/ RTS008#*1/SS008#*1/RXD008*1/SMISO008*1/ SSCL008*1/DE008*1/RSPCKA/RSPCK0/ IRQ7/ AN216/ADTRG0#/COMP4

64-Pin	RX66T (64-Pin LFQFP)	RX26T (64-Pin LFQFP and 64-Pin HWQFN)
45	P65/IRQ9/AN211/CMPC53/DA1	P65/IRQ9/AN211/CMPC53/DA1
46	P64/IRQ8/AN210/CMPC33/DA0	P64/IRQ8/AN210/CMPC33/CMPX52*2/DA0
47	AVCC2	AVCC2
48	AVSS2	AVSS2
49	P54/IRQ2/AN202/CMPC22	P54/IRQ2/AN202/CMPC22/CVREFC1
50	P53/IRQ1/AN201/CMPC12	P53/IRQ1/AN201/CMPC12/CVREFC0
51	P52/IRQ0/AN200/CMPC02	P52/IRQ0/AN200/CMPC02
52	P46/AN102/CMPC50/CMPC51	P47/AN103*1/AN206*2/CMPC03*2
53	P45/AN101/CMPC40/CMPC41	P46/AN102*1/AN006*2/CMPC50*1/CMPC51*1/ CMPC21*2
54	P44/AN100/CMPC30/CMPC31	P45/AN101*1AN005*2/CMPC40*1/CMPC41*1/ CMPC11*2
55	PH4/AN107/PGAVSS1	P44/AN100*1/AN004*2/CMPC30*1/CMPC31*1/ CMPC01*2
56	P42/AN002/CMPC20/CMPC21	P43/AN003/CMPC23*2/CMPC50*2
57	P41/AN001/CMPC10/CMPC11	P42/AN002/CMPC20/CMPC21*1
58	P40/AN000/CMPC00/CMPC01	P41/AN001/CMPC10/CMPC11*1
59	PH0/AN007/PGAVSS0	P40/AN000/CMPC00/CMPC01*1/CMPC13*2
60	AVCC1	AVCC1*1/NC*2
61	AVCC0	AVCC0
62	AVSS0	AVSS0
63	AVSS1	AVSS1*1/NC*2
64	P11/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/MTIOC9D/GTIOC3B/GTETRGA/ GTIOC3B#/GTETRGC/TMO3/POE9#/ IRQ1-DS	P11/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/TMO3/POE9#/MTIOC9D/ GTIOC3B/GTETRGA/GTIOC3B#/GTETRGC/ GTCPPO0/TOC3/SCK009*1/SCK008*1/ TXDB009*1/IRQ1

Notes: 1. Not present on products with a RAM capacity of 48 KB.
2. Not present on products with a RAM capacity of 64 KB.

3.4 48-Pin Package

Table 3.4 is Comparative Listing of 48-Pin Package Pin Functions.

Table 3.4 Comparative Listing of 48-Pin Package Pin Functions

48-Pin	RX66T (48-Pin LFQFP)	RX26T (48-Pin LFQFP and 48-Pin HWQFN)
1	UB/P00/MTIOC9A/MTIOC9A#/CACREF/ RXD9/SMISO9/SSCL9/RXD12/SMISO12/ SSCL12/RXDX12/IRQ2/ADST1/COMP0	P00/MTIOC9A/MTIOC9A#/CACREF/GTIU/ TIC3/RXD12/SMISO12/SSCL12/RXDX12/ RXD009*1/SMISO009*1/SSCL009*1/IRQ2/ ADST1*1/COMP0
2	VCL	VCL
3	MD/FINED	MD/FINED/PN6
4	RES#	RES#
5	XTAL/P37	XTAL/P37/RXD5/SMISO5/SSCL5
6	VSS	VSS
7	EXTAL/P36	EXTAL/P36/TXD5/SMOSI5/SSDA5
8	VCC	VCC
9	PE2/POE10#/NMI	PE2/POE10#/NMI/IRQ0
10	PD7/MTIOC9A/MTIOC9A#/GTIOC0A/ GTIOC3A/GTIOC0A#/GTIOC3A#/TMRI1/ TMRI5/TXD5/SMOSI5/SSDA5/SSLA1/CTX0/ IRQ8	TRST#/PD7/MTIOC9A/MTIOC9A#/TMRI1/ TMRI5/GTIOC0A/GTIOC3A/GTIOC0A#/ GTIOC3A#/GTIU/TXD5/SMOSI5/SSDA5/ SCK009*1/TXD008*1/TXDA008*1/SMOSI008*1/ SSDA008*1/TXDB009*1/SSLA1/SSL01*1/ CTX0/ IRQ8
11	PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6	TDI/PD5/TMRI0/TMRI6/GTIOC1A/ GTETRGA/GTIOC1A#/GTIOC7A/RXD1/ SMISO1/SSCL1/RXD011*1/SMISO011*1/ SSCL011*1/SSL00*1/IRQ6
12	PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11	TDO/PD3/TMO0/GTIOC2A/GTETRGC/ GTIOC2A#/GTIOC7B/TXD1/SMOSI1/ SSDA1/TXD011*1/TXDA011*1/SMOSI011*1/ SSDA011*1/MOSI0*1
13	PB6/GTIOC2A/GTIOC2A#/RXD5/SMISO5/ SSCL5/RXD11/SMISO11/SSCL11/RXD12/ SMISO12/SSCL12/RXDX12/CRX0/IRQ2	PB6/GTIOC2A/GTIOC3A/GTIOC2A#/ GTIOC3A#/TOC0/RXD5/SMISO5/SSCL5/ RXD12/SMISO12/SSCL12/RXDX12/ RXD011*1/SMISO011*1/SSCL011*1/MISO0*1/ CRX0/ IRQ2
14	PB5/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/ SSDA5/TXD11/SMOSI11/SSDA11/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/CTX0	PB5/GTIOC2B/GTIOC3B/GTIOC2B#/ GTIOC3B#/TIC0/TXD5/SMOSI5/SSDA5/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ TXD011*1/TXDA011*1/SMOSI011*1/ SSDA011*1/ RSPCK0*1/CTX0
15	PB4/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/IRQ3-DS	PB4/POE8#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/GTCPPO0/CTS5#/ RTS5#/SS5#/RXD12/SMISO12/SSCL12/ RXDX12/CTS011#*1/RTS011#*1/SS011#*1/ SCK011*1/TXDB011*1/MISOA/SSL01*1/CRX0/ IRQ3
16	PB3/MTIOC0A/MTIOC0A#/CACREF/SCK6/ RSPCKA/IRQ9	PB3/MTIOC0A/MTIOC0A#/CACREF/GTIU/ TOC1/SCK6/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTS009#*1/RTS009#*1/ SS009#*1/DE009*1/RSPCKA/CTX0/IRQ9

17	PB2/MTIOC0B/MTIOC0B#/GTADSM0/ TMRI0/TXD6/SMOSI6/SSDA6/SDA0/ADSM0	PB2/MTIOC0B/MTIOC0B#/TMRI0/ GTADSM0/GTIOC7A/GTIOC7A#/GTIV/TIC1/ TXD6/SMOSI6/SSDA6/SDA0/SDA00*1/ ADSM0
18	PB1/MTIOC0C/MTIOC0C#/GTADSM1/ TMCI0/RXD6/SMISO6/SSCL6/SCL0/IRQ4/ ADSM1	PB1/MTIOC0C/MTIOC0C#/TMCI0/ GTADSM1/GTIOC7B/GTIOC7B#/GTIW/ TOC2/RXD6/SMISO6/SSCL6/SCL0/SCL00*1/ IRQ4/ADSM1
19	PB0/MTIOC0D/MTIOC0D#/TMO0/TXD6/ SMOSI6/SSDA6/CTS11#/RTS11#/SS11#/ MOSIA/IRQ8/ADTRG2#	PB0/MTIOC0D/MTIOC0D#/TMO0/TIC2/ TXD6/SMOSI6/SSDA6/TXD008*1/TXDA008*1/ SMOSI008*1/SSDA008*1/CTS011#*1/ RTS011#*1/SS011#*1/DE011*1/MOSIA/ MOSI0*1/IRQ8/ ADTRG2#
20	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/ SMISO6/SSCL6/MISOA/IRQ1/ADTRG1#	P95/MTIOC6B/MTIOC1A/MTIOC6B#/ MTIOC1A#/TMCI3/GTIOC4A/GTIOC7A/ GTIOC4A#/GTIOC7A#/GTOUUP/RXD6/ SMISO6/SSCL6/RXD008*1/SMISO008*1/ SSCL008*1/MISOA/SSL02*1/MISO0*1/IRQ1/ ADTRG1#*1
21	PA3/MTIOC2A/MTIOC2A#/GTADSM0/ TMRI7/TXD9/SMOSI9/SSDA9/SSLA0	P94/MTIOC7A/MTIOC2A/MTIOC7A#/ MTIOC2A#/TMRI7/GTIOC5A/GTADSM0/ GTIOC5A#/GTOVUP/TXD009*1/TXDA009*1/ SMOSI009*1/SSDA009*1/SCK008*1/ TXDB008*1/SSLA0/SSL00*1
22	VCC	P93/MTIOC7B/MTIOC6A/MTIOC7B#/ MTIOC6A#/TMO4/GTIOC6A/GTIOC6A#/ GTOWUP/TXD009*1/TXDA009*1/ SMOSI009*1/SSDA009*1/RXD011*1/ SMISO011*1/SSCL011*1/SSLA2/SSL02*1/ MOSI0*1/CRX0/IRQ14/ ADTRG0#
23	VSS	P92/MTIOC6D/MTIOC6C/MTIOC6D#/ MTIOC6C#/TMO2/GTIOC4B/GTIOC7B/ GTIOC4B#/GTIOC7B#/GTOULO/SCK009*1/ TXD011*1/TXDA011*1/SMOSI011*1/ SSDA011*1/TXDB009*1/SSLA3/SSL03*1/ MISO0*1/CTX0
24	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC5B#/GTOVLO/RXD5/SMISO5/SSCL5/ RSPCK0*1
25	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC6B/GTIOC2B#/GTIOC6B#	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC6B/GTIOC2B#/GTIOC6B#/GTOWLO/ SSL03*1
26	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC5B/GTIOC1B#/GTIOC5B#	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC5B/GTIOC1B#/GTIOC5B#/GTOVLO/ SSL02*1
27	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC4B/GTIOC0B#/GTIOC4B#	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC4B/GTIOC0B#/GTIOC4B#/GTOULO/ SSL01*1
28	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC6A/GTIOC2A#/GTIOC6A#	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC6A/GTIOC2A#/GTIOC6A#/GTOWUP/ SSL00*1
29	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC5A/GTIOC1A#/GTIOC5A#	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC5A/GTIOC1A#/GTIOC5A#/GTOVUP/ MOSI0*1

30	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC4A/GTIOC0A#/GTIOC4A#	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC4A/GTIOC0A#/GTIOC4A#/GTOUUP/ MISO0*1
31	VCC	VCC
32	VSS	VSS
33	P65/IRQ9/AN211/CMPC53/DA1	P21/MTIOC9A/MTCLKA/MTIOC9A#/ MTCLKA#/TMCI4/TMO6/GTIU/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ TXD008*1/TXDA008*1/SMOSI008*1/ SSDA008*1/MOSIA/MOSI0*1/IRQ6/AN217/ ADTRG1#*1/ COMP5
34	P64/IRQ8/AN210/CMPC33/DA0	P20/MTIOC9C/MTCLKB/MTIOC9C#/ MTCLKB#/TMRI4/TMO2/GTIW/CTS008#*1/ RTS008#*1/SS008#*1/RXD008*1/SMISO008*1/ SSCL008*1/DE008*1/RSPCKA/RSPCK0*1/ IRQ7/ AN216/ADTRG0#/COMP4
35	AVCC2	AVCC2
36	AVSS2	AVSS2
37	P62/IRQ6/AN208/CMPC43	P62/IRQ6/AN208/CMPC43
38	P44/AN100/CMPC30/CMPC31	P53/IRQ1/AN201/CMPC12/CVREFC0
39	P43/AN003	P52/IRQ0/AN200/CMPC02
40	P42/AN002/CMPC20/CMPC21	P44/AN004*2/AN100*1/CMPC01*1/CMPC30*1/ CMPC31*1
41	P41/AN001/CMPC10/CMPC11	P43/AN003/CMPC23*2/CMPC50*2
42	P40/AN000/CMPC00/CMPC01	P42/AN002/CMPC20/CMPC21*1
43	AVCC1	P41/AN001/CMPC10/CMPC11*1
44	AVCC0	P40/AN000/CMPC00/CMPC01*1
45	AVSS0	AVCC0/AVCC1*1
46	AVSS1	AVSS0/AVSS1*1
47	P11/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/MTIOC9D/GTIOC3B/GTETRGA/ GTIOC3B#/GTETRGC/TMO3/POE9#/ IRQ1-DS	P11/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/TMO3/POE9#/MTIOC9D/ GTIOC3B/GTETRGA/GTIOC3B#/GTETRGC/ GTCPPO0/TOC3/SCK009*1/SCK008*1/ TXDB009*1/IRQ1
48	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0-DS	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/TMRI3/POE12#/GTIOC3A/ GTETRGB/GTIOC3A#/GTETRGD/GTIV/ TIC3/CTS6#/RTS6#/SS6#/TXD009*1/ TXDA009*1/SMOSI009*1/SSDA009*1/IRQ0

Notes: 1. Not present on products with a RAM capacity of 48 KB.
2. Not present on products with a RAM capacity of 64 KB.

4. Important Information when Migrating Between MCUs

This section presents important information on differences between the RX66T Group and the RX26T Group.

4.1, Notes on Pin Design presents notes regarding hardware. 4.2, Notes on Functional Design presents notes regarding software.

4.1 Notes on Pin Design

4.1.1 Mode Setting Pins

The mode setting pins when a reset is canceled are the MD and UB pins (multiplexed with P00) on the RX66T Group, and the MD pin on the RX26T Group.

4.1.2 Capacitors Connected to Analog Power Supply pins

When using an A/D conversion clock frequency higher than 40 MHz, add the capacitor described in Table 4.1 between the 0.1 µF capacitor and the power supply pin.

Table 4.1 Comparison of Capacitor Capacitance

RX66T		
RAM 64KB	**RAM 128KB**	**RX26T**
Add a 1000 pF capacitor to the 0.1 µF capacitor.	Add a 0.01 µF capacitor to the 0.1 µF capacitor.	Add a 0.01 µF capacitor to the 0.1 µF capacitor.

4.2 Notes on Functional Design

Some software that runs on the RX66T Group is compatible with the RX26T Group. Nevertheless, appropriate caution must be exercised due to differences in aspects such as operation timing and electrical characteristics.

Software-related considerations regarding function settings that differ between the RX66T Group and RX26T Group are as follows:

For differences between modules and functions, refer to 2. Comparative Overview of Specifications. For further information, refer to the User's Manual: Hardware of in 5. Reference Documents.

4.2.1 Flash Access Window Setting Register (FAW)

On the RX26T group, if the access window protection bit (FSPR) in the FAW register is set to 0, the bit cannot be changed to 1.

For further information, refer to the RX26T User's Manual: Hardware in 5. Reference Documents.

4.2.2 Clock Frequency Settings

The restrictions on clock frequency settings differ between the RX66T Group and RX26T Group. For details, refer to Table 4.2.

Table 4.2 Comparison of Restrictions on Clock Frequency Settings

Item	RX66T	RX26T
Restrictions on clock frequency settings	ICLK ≥ BCLK PCLKC ≥ PCLKA ≥ PCLKB	PCLKC ≥ PCLKA ≥ PCLKB
Clock frequency setting restrictions when using CANFD	—	PCLKA:PCLKB = 2:1 PCLKB ≥ CANFDCLK PCLKB ≥ CANFDMCLK
Restrictions on the clock frequency ratio	ICLK:FCLK = N:1 or 1:N ICLK:PCLKA = N:1 or 1:N ICLK:PCLKB = N:1 or 1:N ICLK:PCLKC = N:1 or 1:N ICLK:PCLKD = N:1 or 1:N PCLKA:PCLKC = 1:1 or 1:2 PCLKB:PCLKD = 1:1 or 2:1 or 4:1 or 1:2	ICLK:FCLK = N:1 or 1:N ICLK:PCLKA = N:1 or 1:N ICLK:PCLKB = N:1 or 1:N ICLK:PCLKC = N:1 or 1:N ICLK:PCLKD = N:1 or 1:N PCLKA:PCLKC = 1:1 or 1:2 PCLKB:PCLKD = 1:1 or 2:1 or 4:1 or 1:2

4.2.3 Performing RAM Self-Diagnostics on Save Register Banks

On the RX26T Group, save register banks are configured in the RAM. The save register banks are provided with a buffer. Therefore, if a SAVE instruction is used to write data to a register and then a RSTR instruction is used to read data from the same register, the data is actually read from the buffer and not from the RAM memory cells. When performing self-diagnostics on the RAM in a save register bank, use the following sequence of steps for checking the written data in order to prevent the data from being read from the buffer:

(1) Use the SAVE instruction to write data to the bank that is the target of the diagnostic test.

(2) Use the SAVE instruction to write data to a bank other than that written to in step 1.

(3) Use the RSTR instruction to read data from the bank written to in step 1.

4.2.4 Control when Output Stop Requests are Generated in Port Output Enable 3

When an output stop request is generated on the RX26T group, the pins for which the corresponding bit is set to 1 in the POECR1 to POECR3 and POECR7 registers are placed in the high-impedance state, and the pins for which the corresponding bit is set to 1 in the PMMCR0 to PMMCR2 registers are switched to the general I/O port.

If both bits are set to 1 for the same pin, the settings on the POECR1 to POECR3 and POECR7 registers have priority and the pin is placed in the high-impedance state.

After switching to the general I/O port, the pin status is determined by the settings on the PDR and PODR registers.

4.2.5 Initialization of Port Direction Register (PDR)

The method of initializing the PDR register differs between the RX66T Group and RX26T Group, even on products with the same pin count.

5. Reference Documents

User's manuals: Hardware

RX66T Group User's Manual: Hardware Rev1.21 (R01UH0749EJ0121)
(The latest version can be downloaded from the Renesas Electronics website.)

RX26T Group User's Manual: Hardware Rev.1.01 (R01UH0979EJ0101)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical updates and technical news

(The latest information can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This module reflects the content of the following technical updates:

TN-RX*-A0147B/E

TN-RX*-A200A/E

TN-RX*-A193A/E

TN-RX*-A194A/E

TN-RX*-A175A/E

TN-RX*-A173A/E

TN-RX*-A163A/E

TN-RX*-A151A/E

TN-RX*-A260A/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Apr.12.23	—	First edition issued
1.01	Sep. 28.23	180 to 186	Modified typos and added notes in Table 3.3 and Table 3.4.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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