RX26T Group, RX62T Group

Differences Between the RX26T Group and the RX62T Group

Introduction

This application note is intended as a reference to points of difference between the peripheral functions, I/O registers, and pin functions of the RX26T Group and RX62T Group, as well as a guide to key points to consider when migrating between the two groups.

Unless specifically otherwise noted, the information in this application note applies to the 100-pin package version of the RX26T Group and the 112-pin package version of the RX62T Group as the maximum specifications. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the User's Manual: Hardware of the products in question.

Target Devices

RX26T Group and RX62T Group

Contents

1. Comparison of Built-In Functions of RX26T Group and RX62T Group

A comparison of the built-in functions of the RX26T Group and RX62T Group is provided below. For details of the functions, refer to "2, Comparative Overview of Specifications" and "5, Reference Documents".

Table 1.1 is Comparison of Built-In Functions of RX62T Group and RX26T Group.

Table 1.1 Comparison of Built-In Functions of RX62T Group and RX26T Group

Function	RX62T	RX26T
CPU	●/▲	
Operating modes	▲	
Address space	▲	
Resets	▲	
Option-setting memory (OFSM)	×	○
Voltage detection circuit (LVD for RX62T, and LVDA for RX26T)	●/▲	
Clock generation circuit	●/▲	
Clock frequency accuracy measurement circuit (CAC)	×	○
Low power consumption function	●/▲/■	
Register write protection function	×	○
Exception handling	▲	
Interrupt controller (ICU for RX62T, and ICUG for RX26T)	●/▲	
Buses	▲	
Memory-protection unit (MPU)	▲	
DMA controller (DMACAa)	×	○
Data transfer controller (DTC for RX62T, and DTCb for RX26T)	●/▲	
Event link controller (ELC)	×	○
I/O ports	●/▲	
Multi-function pin controller (MPC)	×	○
Multi-function timer pulse unit 3 (MTU3 for RX62T, and MTU3d for RX26T)	●/▲	
Port output enable 3 (POE3 for RX62T, and POE3D for RX26T)	●/▲	
General-purpose PWM timer (GPT/GPTa for RX62T, and GPTWa for RX26T)	●/▲/■	
High resolution PWM waveform generation circuit (HRPWM)	×	○
Port output enable for GPTW (POEG)	×	○
8-bit timer (TMRb)	×	○
Compare match timer (CMT)	●	
Compare match timer W (CMTW)	×	○
Watchdog timer (WDT for RX62T, and WDTA for RX26T)	●/■	
Independent watchdog timer (IWDT for RX62T, and IWDTa for RX26T)	●/▲	
Serial communications interface (SCIb for RX62T, and SCIk and SCIh for RX26T)	●/▲	
Serial communications interface (RSCI)	×	○
I2C bus interface (RIIC for RX62, and RIICa for RX26T)	▲	
I^{3}C bus interface (RI3C)	×	○
CAN module (CAN) for RX62T CAN FD module (CANFD) for RX26T	●/■	
Serial peripheral interface (RSPI for RX62T, and RSPId for RX26T)	●/▲	
Serial peripheral interface (RSPIA)	×	○
CRC calculator (CRC for RX62T, and CRCA for RX26T)	▲	
Trigonometric function calculator (TFUv2)	×	○
Trusted Secure IP (TSIP-Lite)	×	○
LIN module (LIN)	○	×
12-bit A/D converter (S12ADA for RX62T, and S12ADHa for RX26T)	●/▲	

Function	RX62T	RX26T
10-bit A/D converter (ADA)	○	×
12-bit D/A converter (R12DAb)	×	○
Temperature sensor (TEMPS)	×	○
Comparator C (CMPCa)	×	○
Data operation circuit (DOCA)	×	○
RAM	●/▲	
ROM/data flash memory for RX62T, Flash memory (FLASH) for RX26T	●/▲	
Packages	▲	

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Register specification items that have no differences between the groups are not indicated.

2.1 CPU

Table 2.1 is Comparative Overview of CPUs.

Table 2.1 Comparative Overview of CPUs

Item	RX62T	RX26T
CPU	• Maximum operating frequency: 100 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per clock cycle • Address space: 4G byte, linear address • Register — General purpose: Sixteen 32-bit registers — Control: Nine 32-bit registers — Accumulator: One 64-bit register • Basic instructions: 73 • Floating point instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement — Instructions: Little endian — Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory-protection unit (MPU)	• Maximum operating frequency: 120 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4G byte, linear address • Register — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • 113 instructions (products with RAM capacity 64 KB) • 111 instructions (products with RAM capacity 48 KB) — Standard provided instructions: 111 — Basic instructions: 77 — Single-precision floating point instructions: 11 — DSP instructions: 23 — Instructions for register bank save function: 2 (Only for products with RAM capacity 64 KB) • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits
FPU	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard

Item	RX62T	RX26T
Register bank save function	—	• Fast collective saving and restoration of the values of CPU registers • 16 save register banks

2.2 Operating Modes

Table 2.2 is Comparative Overview of Operating Modes, and Table 2.3 is Comparison of Operating Mode Registers.

Table 2.2 Comparative Overview of Operating Modes

Item	RX62T	RX26T
Operating modes specified by mode setting pins	Single-chip mode	Single-chip mode
	Boot mode	Boot mode (SCI interface)
		Boot mode (FINE interface)
Operating modes selected by register settings	Single-chip mode enabled Single-chip mode disabled	—
Endians selected by mode pin	Little endian Big endian	—
Endians selected by register settings	—	Little endian Big endian

Table 2.3 Comparison of Operating Mode Registers

Register	Bit	RX62T	RX26T
MDMONR	MD0 MD1 (RX62T) MD (RX26T)	MD0 pin status flag	MD0 pin status flag
	MDE	MDE pin status flag	—
MDSR	—	Mode status register	—
SYSCR0	—	System control register 0	—
SYSCR1	—	System control register 1	System control register 1
		The initial value is different.	
VOLSR	—	—	Voltage level setting register

2.3 Address Space

Figure 2.1 to Figure 2.3 are Comparative Memory Map in Single-Chip Mode.

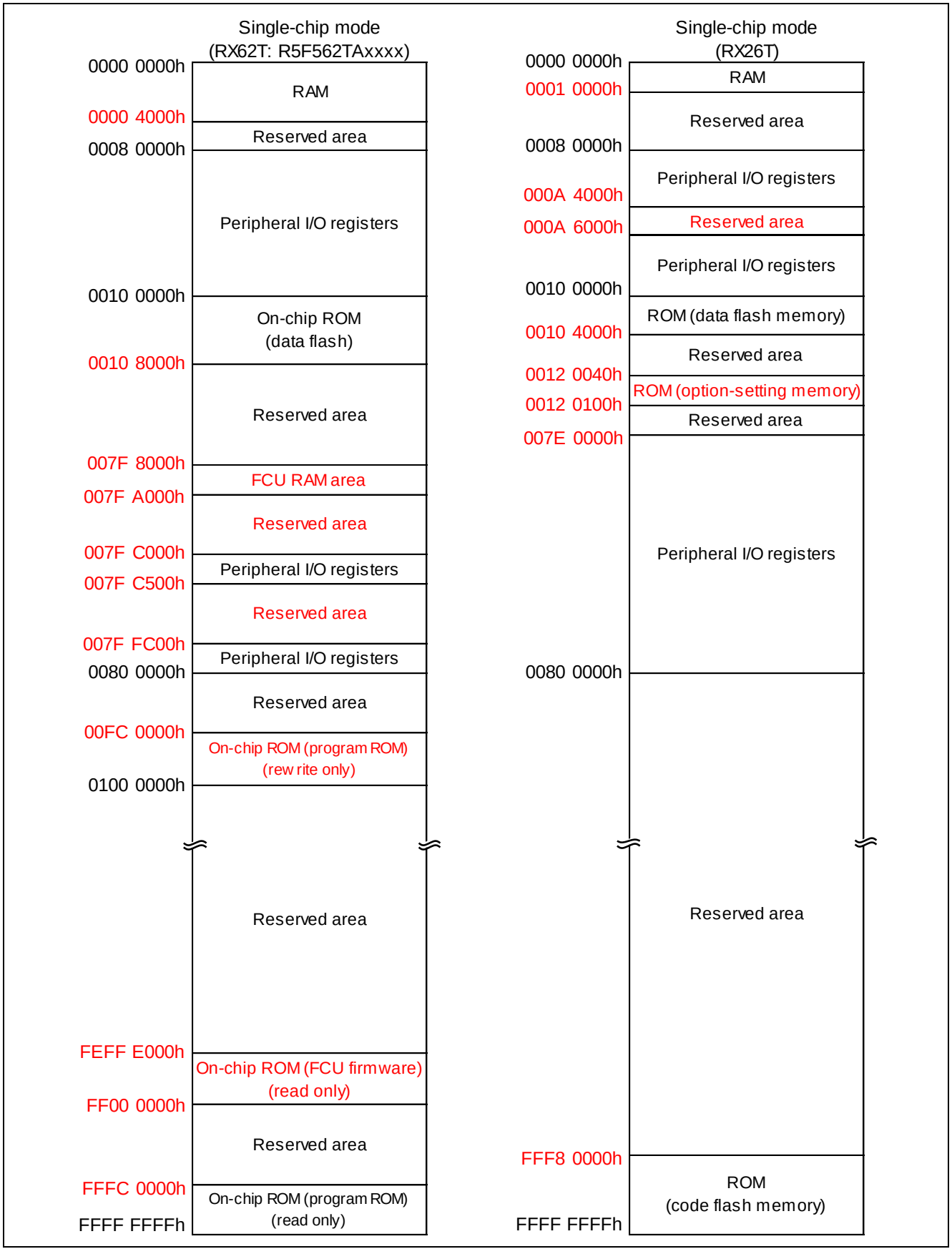

Figure 2.1 Comparative Memory Map in Single-Chip Mode (R5F562TAxxxx)

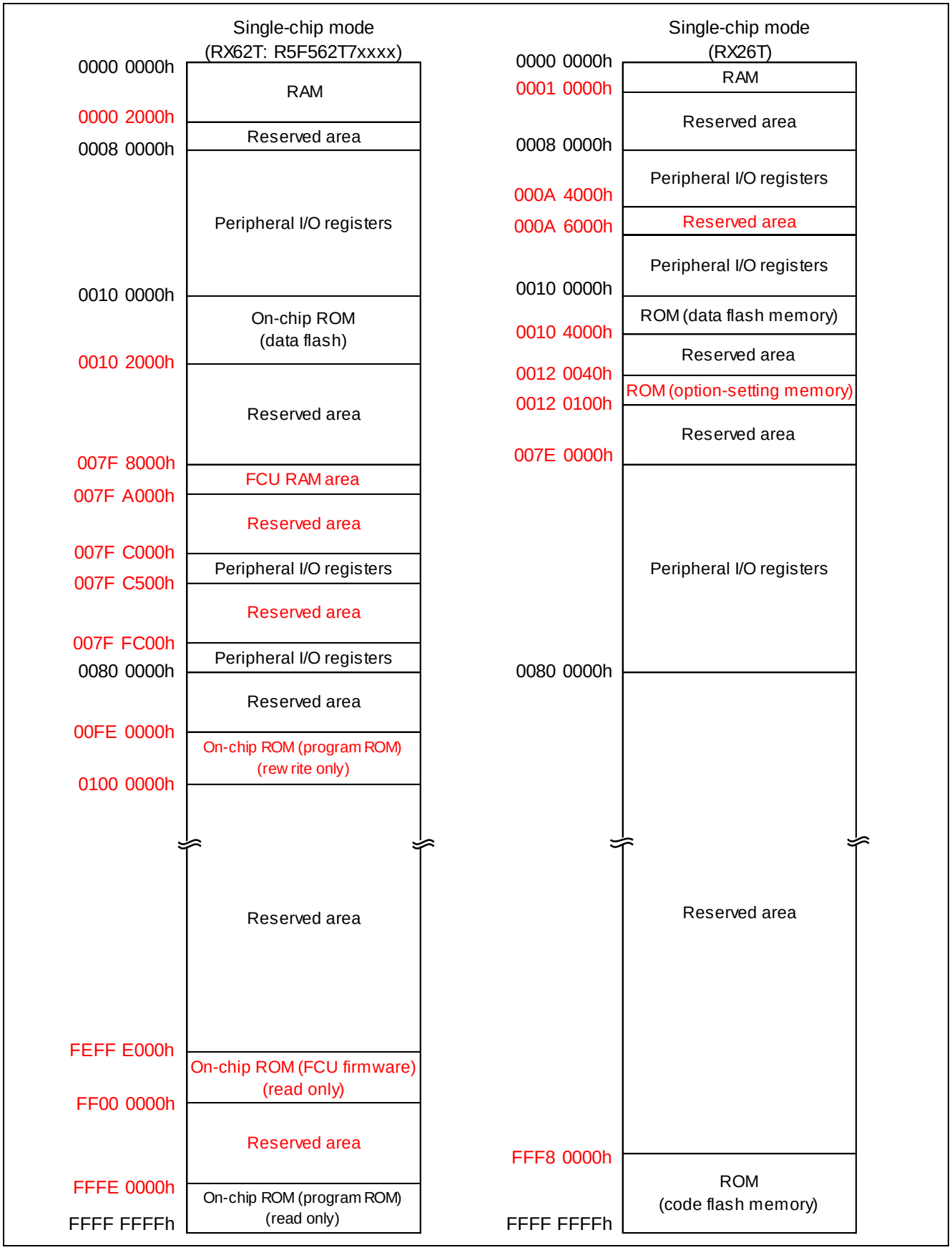

Figure 2.2 Comparison of Memory Maps in Single-Chip Mode (R5F562T7xxxx)

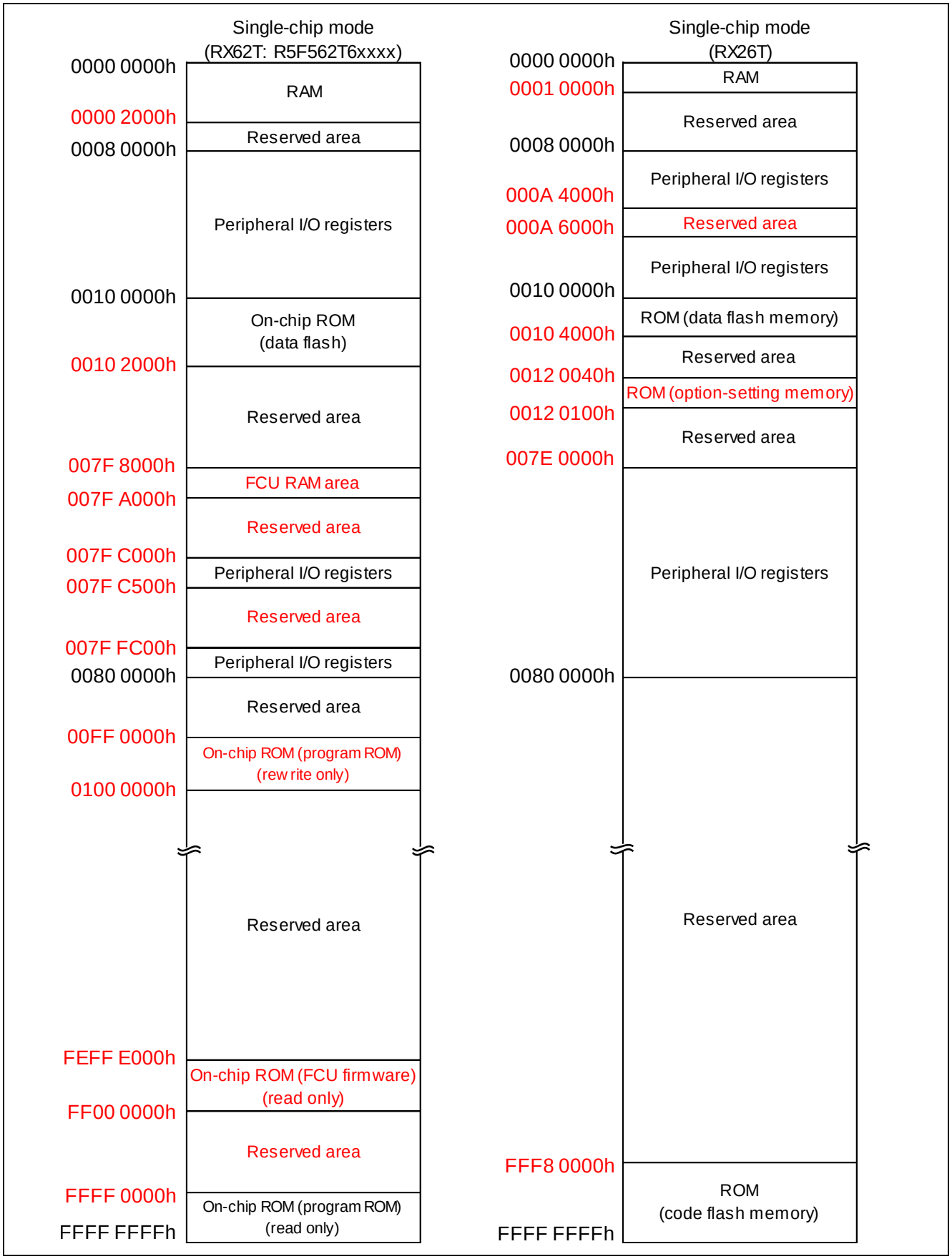

Figure 2.3 Comparative Memory Map in Single-Chip Mode (R5F562T6xxxx)

2.4 Resets

Table 2.4 is Comparative Overview of Resets, and Table 2.5 is Comparison of Reset-Related Registers.

Table 2.4 Comparative Overview of Resets

Item	RX62T	RX26T
RES# pin reset	Voltage input to the RES# pin is driven low.	Voltage input to the RES# pin is driven low.
Power-on reset	VCC rises (voltage detection: VPOR).	VCC rises (voltage detection: VPOR).
Voltage monitoring reset	VCC falls (voltage detection: Vdet1, Vdet2).	VCC falls (voltage detection: Vdet0 to Vdet2).
Deep software standby reset	Deep software standby mode is canceled by an interrupt.	—
Independent watchdog timer reset	Underflow of independent watchdog timer	The independent watchdog timer underflows, or a refresh error occurs.
Watchdog timer reset	Overflow of watchdog timer	The watchdog timer underflows, or a refresh error occurs.
Software reset	Register setting	Register setting

Table 2.5 Comparison of Reset-Related Registers

Register	Bit	RX62T	RX26T
RSTSR (RX62T) RSTSR0 (RX26T)	LVD0RF	—	Voltage monitoring 0 reset detect flag
	LVD1F (RX62T) LVD1RF (RX26T)	LVD1 detect flag 0: LVD1 not detected 1: LVD1 detected	Voltage monitoring 1 reset detect flag 0: Voltage monitoring 1 reset not detected 1: Voltage monitoring 1 reset detected
	LVD2F (RX62T) LVD2RF (RX26T)	LVD2 detect flag 0: LVD2 not detected 1: LVD2 detected	Voltage monitoring 2 reset detect flag 0: Voltage monitoring 2 reset not detected 1: Voltage monitoring 2 reset detected
	DPSRSTF	Deep software standby reset flag	—
RSTSR1	—	—	Reset status register 1
RSTSR2	—	—	Reset status register 2
RSTCSR	—	Reset control/status register	—
IWDTSR	—	IWDT status register	—
SWRR	—	—	Software reset register

2.5 Voltage Detection Circuit

Table 2.6 is Comparative Overview of Voltage Detection Circuits, and Table 2.7 is Comparison of Voltage Detection Circuit Registers.

Table 2.6 Comparative Overview of Voltage Detection Circuits

Item		RX62T (LVD)		RX26T (LVDA)		
		Voltage Monitoring 1	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	When voltage drops below Vdet1	When voltage drops below Vdet2	When voltage drops below Vdet0	When voltage rises above or drops below Vdet1	When voltage rises above or drops below Vdet2
	Detection voltage	Only 1 level	Only 1 level	Selectable from 2 levels using OFS1.VDSEL[1:0] bits	Selectable from 5 levels using LVDLVLR. LVD1LVL[3:0] bits	Selectable from 5 levels using LVDLVLR. LVD2LVL[3:0] bits
	Monitoring flag	Not available	Not available	Not available	LVD1SR. LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR. LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2
		RSTSR.LVD1F flag: Vdet1 detection	RSTSR.LVD2F flag: Vdet2 detection		LVD1SR. LVD1DET flag: Vdet1 passage detection	LVD2SR. LVD2DET flag: Vdet2 passage detection
Process upon voltage detection	Reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet1 ≥ VCC: CPU restart after specified time with VCC > Vdet1	Reset when Vdet2 > VCC: CPU restart after specified time with VCC > Vdet2	Reset when Vdet0 > VCC: CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet2 or Vdet2 > VCC
	Interrupt	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	Not available	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
		Non-maskable interrupt	Non-maskable interrupt	Not available	Selectable between non-maskable or maskable interrupt	Selectable between non-maskable or maskable interrupt
		Interrupt request when Vdet1> VCC	Interrupt request when Vdet2> VCC	Not available	Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either	Interrupt request issued when Vdet2 > VCC and VCC > Vdet2 or either
Digital filter	Enable/ disable switching	Digital filter function not available	Digital filter function not available	Digital filter function not available	Available	Available
	Sampling time	—	—	—	1/n LOCO frequency × 2 (n = 2, 4, 8, 16)	1/n LOCO frequency × 2 (n = 2, 4, 8, 16)
Event link function		—	—	Not available	Available Output of event signals on detection of Vdet crossings	Available Output of event signals on detection of Vdet crossings

Table 2.7 Comparison of Voltage Detection Circuit Registers

Register	Bit	RX62T (LVD)	RX26T (LVDA)
RSTSR	—	Reset status register	—
LVDKEYR	—	Key code register for lower voltage detection control register	—
LVDCR	—	Lower voltage detection control register	—
LVD1CR1	—	—	Voltage monitoring 1 circuit control register 1
LVD1SR	—	—	Voltage monitoring 1 circuit status register
LVD2CR1	—	—	Voltage monitoring 2 circuit control register 1
LVD2SR	—	—	Voltage monitoring 2 circuit status register
LVCMPCR	—	—	Voltage monitoring circuit control register
LVDLVLR	—	—	Voltage detection level select register
LVD1CR0	—	—	Voltage monitoring 1 circuit control register 0
LVD2CR0	—	—	Voltage monitoring 2 circuit control register 0

2.6 Clock Generation Circuit

Table 2.8 is Comparative Overview of Clock Generation Circuits, and Table 2.9 is Comparison of Clock Generation Circuit Registers.

Table 2.8 Comparative Overview of Clock Generation Circuits

Item	RX62T	RX26T
Use	• Generates the system clock (ICLK) to be supplied to CPU, DTC, MTU3, GPT, ROM, and RAM.	• Generates the system clock (ICLK) to be supplied to the CPU, TFU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the RSPI, RSPIA, RSCI, RI3C, CANFD, MTU (internal peripheral bus), GPTW (internal peripheral bus), and HRPWM (internal peripheral bus).
	• Generates the peripheral module clock (PCLK) to be supplied to the peripheral modules.	• Generates the peripheral module clock (PCLKB) to be supplied to the peripheral modules. • Generates the counter reference clock for peripheral modules and the HRPWM reference clock (PCLKC) to be supplied to the MTU and GPTW. • Generates the peripheral module clock (for analog conversion) (PCLKD) to be supplied to the S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CANFD clock (CANFDCLK) to be supplied to the CANFD. • Generates the CANFD main clock (CANFDMCLK) to be supplied to the CANFD.
	• Generates the on-chip oscillator clock (IWDTCLK) to be supplied to the IWDT.	• Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.

Item	RX62T	RX26T
Operating frequency	• ICLK: 8 MHz to 100 MHz • PCLK: 8 MHz to 50 MHz • IWDTCLK: 125 kHz (Typ.) • Restrictions on clock frequency settings: Maintain ICLK ≥ PCLK	• ICLK: 120 MHz (max.) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKC: 120 MHz (max.) • PCLKD: 8 MHz to 60 MHz (for conversion with 12-bit A/D converter) • FCLK: — 4 MHz to 60 MHz (for programming and erasing the code flash memory or data flash memory) — 60 MHz (max.) (for reading from the data flash memory) • CACCLK: Same as the clock from respective oscillators • CANFDCLK: 60 MHz (max.) • CANFDMCLK: 24 MHz (max.) • IWDTCLK: 120 kHz
Main clock oscillator	• Resonator frequency: 8 MHz to 12.5 MHz • External clock input frequency: 8 MHz to 12.5 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal • Connection pins: EXTAL and XTAL • Oscillation stop detection function: Function of switching to internal oscillation upon detection of stopping of the main clock oscillator Function of driving the MTU3 and GPT pins to high-impedance state	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal • Connection pins: EXTAL and XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO, and the MTU and GPTW pins are driven to high-impedance state.
PLL circuit (RX62T) PLL frequency synthesizer (RX26T)	• Input clock source: Main clock • Input pulse frequency division ratio: divided by 1 • Input frequency: 8 MHz to 12.5 MHz • Frequency multiplication ratio: 8 • Output clock frequency: 64 MHz to 100 MHz	• Input clock source: Main clock, HOCO • Input pulse frequency division ratio: Selectable from 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable from 10 to 30 • Output clock frequency of the PLL frequency synthesizer: 120 MHz to 240 MHz
High-speed on-chip oscillator (HOCO)	—	• Oscillation frequency: Selectable from 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control

Item	RX62T	RX26T
Low-speed on-chip oscillator (LOCO)	—	Oscillation frequency: 240 kHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 125 kHz (Typ.)	Oscillation frequency: 120 kHz
Selection of clock ICLK/PCLK	Selectable from EXTAL ×8, ×4, ×2, and ×1 for ICLK/PCLK individually	Selectable from the main clock, HOCO, and LOCO divided by 64, 32, 16, 8, 4, 2, or 1 for ICLK/PCLKA to PCLKD/FCLK individually
Event link function (output)	—	Detection of stopping of the main clock oscillator
Event link function (input)	—	Switching of the clock source to the low-speed on-chip oscillator

Table 2.9 Comparison of Clock Generation Circuit Registers

Register	Bit	RX62T	RX26T
SCKCR	—	System clock control register	System clock control register
		Initial value after a reset differs.	
	PCK[3:0]	Peripheral module clock select bits	—
	PCKD[3:0]	—	Peripheral module clock D (PCLKD) select bits
	PCKC[3:0]	—	Peripheral module clock C (PCLKC) select bits
	PCKB[3:0]	—	Peripheral module clock B (PCLKB) select bits
	PCKA[3:0]	—	Peripheral module clock A (PCLKA) select bits
	ICK[3:0]	System clock select bits b27 b24 0 0 0 0: ×8 0 0 0 1: ×4 0 0 1 0: ×2 0 0 1 1: ×1 Settings other than the above are prohibited.	System clock (ICLK) select bits b27 b24 0 0 0 0: divided by 1 0 0 0 1: divided by 2 0 0 1 0: divided by 4 0 0 1 1: divided by 8 0 1 0 0: divided by 16 0 1 0 1: divided by 32 0 1 1 0: divided by 64 Settings other than the above are prohibited.
	FCK[3:0]	—	FlashIF clock (FCLK) select bits
SCKCR2	—	—	System clock control register 2
SCKCR3	—	—	System clock control register 3
PLLCR	—	—	PLL control register
PLLCR2	—	—	PLL control register 2
MOSCCR	—	—	Main clock oscillator control register
LOCOCR	—	—	Low-speed on-chip oscillator control register
ILOCOCR	—	—	IWDT-dedicated on-chip oscillator control register

Register	Bit	RX62T	RX26T
HOCOCR	—	—	High-speed on-chip oscillator control register
HOCOCR2	—	—	High-speed on-chip oscillator Control register 2
OSCOVFSR	—	—	Oscillation stabilization flag register
OSTDCR	OSTDIE	—	Oscillation stop detection interrupt enable bit
	KEY[7:0]	OSTDCR key code	—
OSTDSR	—	—	Oscillation stop detection status register
MOSCWTCR	—	—	Main clock oscillator wait control register
MOFCR	—	—	Main clock oscillator function control register
HOCOPCR	—	—	High-speed on-chip oscillator power supply control register

2.7 Low Power Consumption Function

Table 2.10 is Comparative Overview of Low Power Consumption Functions, Table 2.11 is Comparison of Transition and Cancellation Methods and Operating States in Each Mode, and Table 2.12 is Comparison of Low Power Consumption Registers.

Table 2.10 Comparative Overview of Low Power Consumption Functions

Item	RX62T	RX26T
Reducing power consumption by switching clock signals	The frequency division ratio can be set independently for the system clock (ICLK) and peripheral module clock (PCLK).	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, and PCLKD), and FlashIF clock (FCLK).
Module stop function	Each peripheral module can be stopped independently.	Each peripheral module can be stopped independently.
Function for transition to low power consumption mode	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.
Low power consumption modes	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode	• Sleep mode • All-module clock stop mode • Software standby mode

Table 2.11 Comparison of Transition and Cancellation Methods and Operating States in Each Mode

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX62T	RX26T
Sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupts	Interrupts
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation	Operation possible
	High-speed on-chip oscillator	—	Operation possible
	Low-speed on-chip oscillator	—	Operation possible
	IWDT-dedicated on-chip oscillator	—	Operation possible
	PLL	—	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM	Operation (retained)	Operation possible (retained)
	Flash memory	Operation	Operation
	Watchdog timer	Operation	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation	Operation possible
	Port output enable (POE)	Operation possible	Operation possible
	8-bit timer (unit 0 and unit 1) (TMR)	—	Operation possible
	Voltage detection circuit (LVD)	Operation	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Operation	Operation possible
	I/O ports	Operation	Operation

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX62T	RX26T
All-module clock stop mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupts	Interrupts
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation	Operation possible
	High-speed on-chip oscillator	—	Operation possible
	Low-speed on-chip oscillator	—	Operation possible
	IWDT-dedicated on-chip oscillator	—	Operation possible
	PLL	—	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	Watchdog timer	Operation	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation	Operation possible
	Port output enable (POE)	Operation possible	Operation possible
	8-bit timer (unit 0 and unit 1) (TMR)	—	Operation possible
	Voltage detection circuit (LVD)	Operation	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained
Software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupts	Interrupts
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Stopped	Stopped
	High-speed on-chip oscillator	—	Stopped
	Low-speed on-chip oscillator	—	Stopped
	IWDT-dedicated on-chip oscillator	—	Operation possible
	PLL	—	Stopped
	CPU	Stopped (retained)	Stopped (retained)
	RAM	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	Watchdog timer	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Stopped (retained)	Operation possible
	Port output enable (POE)	Stopped (retained)	Stopped (retained)
	8-bit timer (unit 0 and unit 1) (TMR)	—	Stopped (retained)
	Voltage detection circuit (LVD)	Operation	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained
Deep software standby mode	Transition method	Control register + instruction	—
	Method of cancellation other than reset	Interrupts	—
	State after cancellation*1	Program execution state (Reset processing)	—

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX62T	RX26T
Deep software standby mode	Oscillator	Stopped	—
	CPU	Stopped (undefined)	—
	On-chip RAM	Stopped (undefined)	—
	Watchdog timer (WDT)	Stopped (undefined)	—
	Independent watchdog timer (IWDT)	Stopped (undefined)	—
	Voltage detection circuit	Operation	—
	Power-on reset circuit	Operation	—
	Port output enable	Stopped (undefined)	—
	Peripheral modules	Stopped (retained)	—
	I/O pin status	Retained	—

“Operation possible” means that whether the state is operating or stopped is controlled by the control register setting.
“Stopped (retained)” means that internal register values are retained and internal operations are suspended.
Note: 1. NMI, IRQ0-A, IRQ1-A, and some internal interrupts (voltage monitoring). Any of these sources is effective only if the relevant bit of the deep standby interrupt enable register (DPSIER) is "1".

Table 2.12 Comparison of Low Power Consumption Registers

Register	Bit	RX62T	RX26T
SBYCR	STS[4:0]	Standby time select bit	—
MSTPCRA	MSTPA0	—	Compare match timer W (unit 1) module stop bit
	MSTPA1	—	Compare match timer W (unit 0) module stop bit
	MSTPA2	—	8-bit timer 7/6 (unit 3) module stop bit
	MSTPA3	—	8-bit timer 5/4 (unit 2) module stop bit
	MSTPA4	—	8-bit timer 3/2 (unit 1) module stop bit
	MSTPA5	—	8-bit timer 1/0 (unit 0) module stop bit
	MSTPA7	General purpose PWM timer module stop bit Target module: GPT 0: Release from module-stop state 1: Transition to module-stop state	General purpose PWM timer/high resolution PWM/GPTW port output enable module stop bit Target modules: GPTW, HRPWM, and POEG 0: Release from module-stop state 1: Transition to module-stop state
	MSTPA19	—	12-bit D/A converter module stop bit
	MSTPA23	10-bit A/D converter module stop bit Target module: 10-bit ADC 0: Release from module-stop state 1: Transition to module-stop state	12-bit A/D converter (unit 2) module stop bit Target module: S12AD unit 2 (Temperature sensor) 0: Release from module-stop state 1: Transition to module-stop state
	MSTPA24	12-bit A/D converter control module stop bit Target module: S12ADA controller 0: Release from module-stop state 1: Transition to module-stop state	Module stop A24 setting bit Reading and writing are enabled. To transfer to all-module clock stop mode, this bit must be set to 1.
	MSTPA27	—	Module stop A27 setting bit

Register	Bit	RX62T	RX26T
MSTPCRA	MSTPA28	Data Transfer Controller module stop bit	DMA controller/data transfer controller module stop bit
	MSTPA29	—	Module stop A29 setting bit
MSTPCRB	MSTPB0	CAN module stop bit	—
	MSTPB4	—	Serial communications interface 12 module stop bit
	MSTPB6	—	Data operation circuit module stop bit
	MSTPB7	LIN module stop bit	—
	MSTPB9	—	Event link controller module stop bit
	MSTPB10	—	Comparator C module stop bit
	MSTPB25	—	Serial communications interface 6 module stop bit
	MSTPB26	—	Serial communications interface 5 module stop bit
	MSTPB29	Serial communications interface 2 module stop bit	—
	MSTPB31	Serial communications interface 0 module stop bit	—
MSTPCRC	MSTPC0	RAM module stop bit Target module: RAM (0000 0000h to 0000 3FFFh) 0: Release from module-stop state 1: Transition to module-stop state	RAM module stop bit Target module: RAM (0000 0000h to 0000 FFFFh) 0: RAM operating 1: RAM stopped
	MSTPC19	—	CAC module stop bit
	MSTPC24	—	Serial communications interface 11 module stop bit
	MSTPC26	—	Serial communications interface 9 module stop bit
	MSTPC27	—	Serial communications interface 8 module stop bit
MSTPCRD	—	—	Module stop control register D
DPSBYCR	—	Deep standby control register	—
DPSWCR	—	Deep standby wait control register	—
DPSIER	—	Deep standby interrupt enable register	—
DPSIFR	—	Deep standby interrupt flag register	—
DPSIEGR	—	Deep standby interrupt edge register	—
RSTSR	—	Reset status register	—
DPSBKRy	—	Deep standby backup register (y = 0 to 31)	—
RSTCKCR	—	—	Sleep mode return clock source switching register

2.8 Exception Handling

Table 2.13 is Comparative Overview of Exception Handling, Table 2.14 is Comparison of Vectors, and Table 2.15 is Comparison of Instructions for Returning from Exception Handling Routine.

Table 2.13 Comparative Overview of Exception Handling

Item	RX62T	RX26T
Exceptions	• Undefined instruction exception • Privileged instruction exception • Access exception • Floating-point exception • Resets • Non-maskable interrupts • Interrupts • Unconditional trap	• Undefined instruction exception • Privileged instruction exception • Access exception • Single-precision floating-point exception • Resets • Non-maskable interrupts • Interrupts • Unconditional trap

Table 2.14 Comparison of Vectors

Item		RX62T	RX26T
Undefined instruction exception		Fixed vector table	Exception vector table (EXTB)
Privileged instruction exception		Fixed vector table	Exception vector table (EXTB)
Access exception		—	Exception vector table (EXTB)
Floating-point exception (RX62T) Single-precision floating-point exception (RX26T)		—	Exception vector table (EXTB)
Resets		Fixed vector table	Exception vector table (EXTB)
Non-maskable interrupts		Fixed vector table	Exception vector table (EXTB)
Interrupts	Fast interrupt	FINTV	FINTV
	Other than fast interrupt	Variable vector table (INTB)	Interrupt vector table (INTB)
Unconditional trap		Variable vector table (INTB)	Interrupt vector table (INTB)

Table 2.15 Comparison of Instructions for Returning from Exception Handling Routine

Item		RX62T	RX26T
Undefined instruction exception		RTE	RTE
Privileged instruction exception		RTE	RTE
Access exception		RTE	RTE
Floating-point exception		RTE	RTE
Resets		Return not possible	Return not possible
Non-maskable interrupts		Return not possible	Prohibited
Interrupts	Fast interrupt	RTFI	RTFI
	Other than fast interrupt	RTE	RTE
Unconditional trap		RTE	RTE

2.9 Interrupt Controller

Table 2.16 is Comparative Overview of Interrupt Controllers, and Table 2.17 is Comparison of Interrupt Controller Registers.

Table 2.16 Comparative Overview of Interrupt Controllers

Item		RX62T (ICU)	RX26T (ICUG)
Interrupts	Peripheral interrupts	• Interrupts from peripheral modules • Number of interrupt sources: 101 • Interrupt detection: Edge detection/level detection — The detection method is determined for each interrupt source of connected peripheral modules.	• Interrupts from peripheral modules • Number of interrupt sources: 256 • Interrupt detection method: Edge detection or level detection (fixed for each interrupt source) • Group interrupt: Multiple interrupt sources are grouped together and treated as an interrupt source*1. — Group IE0 interrupt: Interrupt sources of coprocessors that use ICLK as the operating clock (edge detection) — Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) — Group BL0/BL1/BL2 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) — Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.

Item		RX62T (ICU)	RX26T (ICUG)
Interrupts	External pin interrupts	Interrupts from pins IRQ7 to IRQ0 • Number of interrupt sources: 8 • Interrupt detection: Detection of low, falling edge, rising edge, or rising and falling edges can be set for each source.	Interrupts by input signals on IRQi pins (i = 0 to 15) • Number of interrupt sources: 16 • Interrupt detection: Detection of low level, falling edge, rising edge, or rising and falling edges can be set for each source. • A digital filter can be used to remove noise.
	Software interrupts	• Interrupt generated by writing to a register • Number of interrupt sources: 1	• An interrupt request can be generated by writing to a register. • Number of sources: 2
	Interrupt priority level	Specified by registers.	The priority level is set with the interrupt source priority register r (IPRr) (r = 000 to 255).
	Fast interrupt function	Faster interrupt handling by the CPU can be specified for a single interrupt source only.	It is possible to reduce the CPU's interrupt response time. This setting can be used for one interrupt source only.
	DTC and DMAC control	The DTC can be activated by an interrupt source. DTC activation interrupt sources: 87 (Peripheral function interrupts: 78 + external pin interrupts: 8 + software interrupts: 1)	The DTC and DMAC can be activated by an interrupt source. DTC activation interrupt sources: 149 DMAC activation interrupt sources: 127
Non-maskable interrupts	NMI pin interrupt	Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge	Interrupt by the input signal on the NMI pin • Interrupt detection: Falling edge or rising edge • A digital filter can be used to remove noise.
	Oscillation stop detection interrupt	Interrupt on detection of oscillation having stopped	Interrupt occurs when the main clock oscillator stop is detected.
	WDT underflow/ refresh error interrupt	—	Interrupt occurs when the watchdog timer underflows or a refresh error occurs.
	IWDT underflow/ refresh error interrupt	—	Interrupt occurs when the independent watchdog timer underflows or a refresh error occurs
	Voltage monitoring 1 interrupt	Interrupt on detection of drop of power supply voltage	Interrupt from voltage detection circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	—	Interrupt from voltage detection circuit 2 (LVD2)
	RAM error interrupt	—	Interrupt occurs when a parity check error is detected in RAM.

Item		RX62T (ICU)	RX26T (ICUG)
Return from low power consumption state	Sleep mode	Exit sleep mode by a non-maskable interrupt or any other interrupt source.	Exit sleep mode by any interrupt source.
	All-module clock stop mode	Exit all-module clock stop mode by a non-maskable interrupt, IRQ7 to IRQ0 interrupt, or WDT interrupt.	Exit all-module clock stop mode by the NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection, IWDT, or TMR0 to TMR3).
	Software standby mode	Exit software standby mode by a non-maskable interrupt or IRQ0 to IRQ7 interrupt.	Exit software standby mode by the NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, or IWDT).

Note: 1. Groups to which no interrupt source is assigned are reserved. Also, there is no register corresponding to that group.

Table 2.17 Comparison of Interrupt Controller Registers

Register	Bit	RX62T (ICU)	RX26T (ICUG)
IPRm (RX62T) IPRr (RX26T)	—	Interrupt source priority register m (m = 00h to 90h)	Interrupt source priority register r (r = 000 to 255)
SWINT2R	—	—	Software interrupt 2 generation register
DTCERn	—	DTC activation enable register n (n = 027 to 256)	DTC transfer request enable register n (n = 026 to 255)
DMRSRm	—	—	DMAC activation source select register m
IRQCRn (RX62T) IRQCRi (RX26T)	—	IRQ control register n (n = 0 to 7)	IRQ control register I (i = 0 to 15)
IRQFLTE0	—	—	IRQ pin digital filter enable register 0
IRQFLTE1	—	—	IRQ pin digital filter enable register 1
IRQFLTC0	—	—	IRQ pin digital filter setting register 0
IRQFLTC1	—	—	IRQ pin digital filter setting register 1
NMISR	LVDST	Voltage monitoring interrupt status flag	—
	OSTST	Oscillation stop detection interrupt status flag (b2)	Oscillation stop detection interrupt status flag (b1)
	WDTST	—	WDT underflow/refresh error status flag
	IWDTST	—	IWDT underflow/refresh error status flag
	LVD1ST	—	Voltage monitoring 1 interrupt status flag
	LVD2ST	—	Voltage monitoring 2 interrupt status flag
	RAMST	—	RAM error interrupt status flag

Register	Bit	RX62T (ICU)	RX26T (ICUG)
NMIER	LVDEN	Voltage monitoring interrupt enable bit	—
	OSTEN	Oscillation stop detection interrupt enable bit (b2)	Oscillation stop detection interrupt enable bit (b1)
	WDTEN	—	WDT underflow/refresh error enable bit
	IWDTEN	—	IWDT underflow/refresh error enable bit
	LVD1EN	—	Voltage monitoring 1 interrupt enable bit
	LVD2EN	—	Voltage monitoring 2 interrupt enable bit
	RAMEN	—	RAM error interrupt enable bit
NMICLR	WDTCLR	—	WDT clear bit
	OSTCLR	OST clear bit (b2)	OST clear bit (b1)
	IWDTCLR	—	IWDT clear bit
	LVD1CLR	—	LVD1 clear bit
	LVD2CLR	—	LVD2 clear bit
NMIFLTE	—	—	NMI pin digital filter enable register
NMIFLTC	—	—	NMI pin digital filter setting register
GRPBL0/ GRPBL1/ GRPBL2	—	—	Group BL0/BL1/BL2 interrupt request register
GRPAL0/ GRPAL1	—	—	Group AL0/ AL1 interrupt request register
GENBL0/ GENBL1/ GENBL2	—	—	Group BL0/BL1/BL2 interrupt request enable register
GENAL0/ GENAL1	—	—	Group AL0/AL1 interrupt request enable register
PIARk	—	—	Software configurable interrupt A request register k (k = 0h to Fh, 12h to 14h)
SLIARn	—	—	Software configurable interrupt A source select register n (n = 208 to 255)
SLIPRCR	—	—	Software configurable interrupt source select register write protect register

2.10 Buses

Table 2.18 is Comparative Overview of Buses, and Table 2.19 is Comparison of Bus Registers.

Table 2.18 Comparative Overview of Buses

Item		RX62T	RX26T
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (on-chip RAM, on-chip ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (on-chip RAM, on-chip ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM or code flash memory) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	Connected to on-chip RAM	Connected to RAM
	Memory bus 2	Connected to on-chip ROM	Connected to code flash memory
Internal main buses	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DTC • Connected to on-chip memory (on-chip RAM, on-chip ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the DTC and DMAC • Connected to on-chip memory (RAM or code flash memory) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (bus error monitoring section, interrupts, etc.) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (TFU, DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules (WDT, CMT, CRC, SCI, etc.) • Operates in synchronization with the peripheral module clock (PCLK)	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral module clock (PCLKB)
	Internal peripheral bus 3	• Connected to peripheral modules (MTU3 and GPT) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (DOC, RSCI, CANFD, and CMPC) • Operates in synchronization with the peripheral module clock (PCLKB)
	Internal peripheral bus 4	• Connected to peripheral modules (MTU3) • Operates in synchronization with the peripheral module clock (PCLK)	• Connected to peripheral modules (MTU, GPTW, HRPWM, and RSPI) • Operates in synchronization with the peripheral module clock (PCLKA)

Item		RX62T	RX26T
Internal peripheral buses	Internal peripheral bus 5	—	• Connected to peripheral modules (RSCI, RSCI, RI3C, and CANFD) • Operates in synchronization with the peripheral module clock (PCLKA)
	Internal peripheral bus 6	• Connected to on-chip ROM (P/E) or data flash memory • Operates in synchronization with the peripheral module clock (PCLK)	• Connected to code flash memory (for programming and erasure) or data flash memory • Operates in synchronization with the FlashIF clock (FCLK)

Table 2.19 Comparison of Bus Registers

Register	Bit	RX62T	RX26T
BEREN	TOEN	—	Timeout detection enable bit*1, *2
BERSR1	TO	—	Timeout bits
	MST[2:0]	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Setting prohibited 0 1 0: Setting prohibited 0 1 1: DTC 1 0 0: Setting prohibited 1 0 1: Setting prohibited 1 1 0: Setting prohibited 1 1 1: Setting prohibited	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved
BUSPRI	—	—	Bus priority control register

Notes: 1. The bus may freeze if it is accessed when detection is prohibited (TOEN bit = 0).
2. Do not set the TOEN bit to “0” (detection prohibited) when a timeout error is detected.

2.11 Memory-Protection Unit

Table 2.20 is Comparison of Memory-Protection Unit Registers.

Table 2.20 Comparison of Memory-Protection Unit Registers

Register	Bit	RX62T	RX26T
MPECLR	CLR	[For reading] 0: Fixed to reading [For writing] 0: No operation 1: MPESTS.DRW, DA, and IA bits are set to “0”.	[For reading] 0: Fixed to reading [For writing] 0: No operation 1: MPESTS.DRW, DMPER, and IMPER bits are set to "0".

2.12 Data Transfer Controller

Table 2.21 is Comparative Overview of Data Transfer Controllers, and Table 2.22 is Comparison of Data Transfer Controller Registers.

Table 2.21 Comparative Overview of Data Transfer Controllers

Item	RX62T (DTC)	RX26T (DTCb)
Number of transfer channels	Equal to the number of all interrupt sources that can start a DTC transfer	Equal to the number of all interrupt sources that can start a DTC transfer
Transfer modes	• Normal transfer mode A single activation leads to a single data transfer • Repeat transfer mode A single activation leads to a single data transfer The transfer address returns to the transfer start address after the number of data transfers corresponding to "repeat size". The repeat size can be set to 256 at a maximum. • Block transfer mode A single activation leads to the transfer of a single block of data. The block size can be set to 255 data units at a maximum.	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode A single activation leads to a single data transfer. The transfer address returns to the transfer start address after the number of data transfers corresponding to "repeat size". The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, 1,024 bytes. • Block transfer mode A single activation leads to the transfer of a single block of data. The block size can be set to 256 × 32 bits = 1,024 bytes at a maximum.
Chain transfer function	Channel transfer is possible in accordance with the interrupt source (transferred by a DTC activation request from ICU). • Multiple data transfers can be made for one activation source (chain transfer). • For chain transfer, either “performed when counter = 0” or “every time” can be selected.	• Multiple types of data transfer can be performed sequentially in response to a single transfer request. • Either “performed only when the transfer counter reaches 0” or “every time” can be selected.
Sequence transfer	—	A complex series of transfers can be registered as a sequence. Any sequence can be selected by the transfer data and executed. • Only one sequence transfer trigger source can be selected at a time. • Up to 256 sequences can correspond to a single trigger source. • The data that is initially transferred in response to a transfer request determines the sequence. • The entire sequence can be executed on a single request, or the sequence can be suspended in the middle and resumed on the next transfer request (sequence division).

Item	RX62T (DTC)	RX26T (DTCb)
Transfer space	• 16 MB in short-address mode (from 0000 0000h to 007F FFFFh or from FF80 0000h to FFFF FFFFh, excluding reserved areas) • 4 GB in full-address mode (from 0000 0000h to FFFF FFFFh, excluding reserved areas)	• 16 MB in short-address mode (from 0000 0000h to 007F FFFFh or from FF80 0000h to FFFF FFFFh, excluding reserved areas) • 4 GB in full-address mode (within 0000 0000h to FFFF FFFFh, excluding reserved areas)
Data transfer units	• Single data unit: 8, 16, or 32 bits • Single block size: 1 to 255 data units	• Single data unit: 1 byte (8 bits), 1 word (16 bits), 1 long word (32 bits) • Single block size: 1 to 256 data units
CPU interrupt requests	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.
Event link function	—	An event link request is generated after one data transfer (for block transfers, after one block).
Read skip	Read skip of transferred information can be specified.	Reading of the transfer information can be skipped when the same transfer is repeated.
Write-back skip	Write-back skip can be executed when the address of the transfer source or destination is fixed.	Write-back of the transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.
Write-back disable	—	Ability to disable write-back of transfer information
Displacement addition	—	Ability to add displacement to the transfer source address (selectable by each transfer information)
Low power consumption function	—	Ability to transition to module stop state

Table 2.22 Comparison of Data Transfer Controller Registers

Register	Bit	RX62T (DTC)	RX26T (DTCb)
MRA	WBDIS	—	Write-back disable bit
MRB	SQEND	—	Sequence transfer end bit
	INDX	—	Index table reference bit
	CHNS	DTC chain transfer select bit 0: Chain transfer is performed continuously 1: Chain transfer is performed only when counter is 0	DTC chain transfer select bit 0: Chain transfer is performed every time a transfer finishes 1: Chain transfer is performed when the transfer counter changes from 1 to 0 or 1 to CRAH.
MRC	—	—	DTC mode register C
DTCIBR	—	—	DTC index table base register
DTCOR	—	—	DTC operation register
DTCSQE	—	—	DTC sequence transfer enable register
DTCDISP	—	—	DTC address displacement register

2.13 I/O Port

Table 2.23 to Table 2.27 provide comparative overviews of I/O ports, and Table 2.28 is Comparison of I/O Port Registers.

Table 2.23 Comparative Overview of I/O Ports on 100-Pin Products

Item	RX62T (100-Pin)	RX26T (100-Pin)
PORT0	—	P00, P01
PORT1	P10, P11	P10, P11
PORT2	P20 to P24	P20 to P24, P27
PORT3	P30 to P33	P30 to P33, P36, P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P55	P50 to P55
PORT6	P60 to P65	P60 to P65
PORT7	P70 to P76	P70 to P76
PORT8	P80 to P82	P80 to P82
PORT9	P90 to P96	P90 to P96
PORTA	PA0 to PA5	PA0 to PA5
PORTB	PB0 to PB7	PB0 to PB7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE5	PE0 to PE5
PORTN	—	PN6, PN7

Table 2.24 Comparative Overview of I/O Ports on 80-Pin Products

Item	RX62T (80-Pin)	RX26T (80-Pin)
PORT0	—	P00, P01
PORT1	P10, P11	P10, P11
PORT2	P20 to P24	P20 to P22, P27
PORT3	P30 to P33	P30, P31, P36, P37
PORT4	P40 to P47	P40 to P47
PORT5	—	P50 to P55
PORT6	P60 to P63	P60, P64, P65
PORT7	P70 to P76	P70 to P76
PORT9	P91 to P96	P90 to P96
PORTA	PA2 to PA5	PA3, PA5
PORTB	PB0 to PB7	PB0 to PB6
PORTD	PD3 to PD7	PD2 to PD7
PORTE	PE0, PE3, PE4	PE2 to PE4
PORTN	—	PN6, PN7

Table 2.25 Comparative Overview of I/O Ports on 80-Pin Products (R5F562TxGDFF)

Item	RX62T (80-pin (R5F562TxGDFF))	RX26T (80-Pin)
PORT0	—	P00, P01
PORT1	P10	P10, P11
PORT2	P20, P22 to P24	P20 to P22, P27
PORT3	P30 to P33	P30, P31, P36, P37
PORT4	P40 to P47	P40 to P47
PORT5	—	P50 to P55
PORT6	—	P60, P64, P65
PORT7	P70 to P76	P70 to P76
PORT8	P80 to P82	—
PORT9	P90 to P96	P90 to P96
PORTA	PA3, PA5	PA3, PA5
PORTB	PB0 to PB7	PB0 to PB6
PORTD	PD2 to PD7	PD2 to PD7
PORTE	PE0, PE1, PE3, PE4, PE5	PE2 to PE4
PORTN	—	PN6, PN7

Table 2.26 Comparative Overview of I/O Ports on 64-Pin Products

Item	RX62T (64-Pin)	RX26T (64-Pin)
PORT0	—	P00, P01
PORT1	P10, P11	P11
PORT2	P22 to P24	P20 to P22
PORT3	P30 to P33	P36, P37
PORT4	P40 to P47	P40 to P47
PORT5	—	P52 to P54
PORT6	—	P64, P65
PORT7	P70 to P76	P70 to P76
PORT9	P91 to P94	P90 to P96
PORTA	PA2 to PA5	—
PORTB	PB0 to PB7	PB0 to PB6
PORTD	PD3 to PD7	PD3 to PD7
PORTE	PE2	PE2
PORTN	—	PN6, PN7

Table 2.27 Comparison of I/O Port Functions

Item	Port Symbol	RX62T	RX26T
Input pull-up function	PORT0	—	P00, P01
	PORT1	—	P10, P11
	PORT2	—	P20 to P24, P27
	PORT3	—	P30 to P33, P36, P37
	PORT4	—	P40 to P47
	PORT5	—	P50 to P55
	PORT6	—	P60 to P65
	PORT7	—	P70 to P76
	PORT8	—	P80 to P82
	PORT9	—	P90 to P96
	PORTA	—	PA0 to PA5
	PORTB	—	PB0 to PB7
	PORTD	—	PD0 to PD7
	PORTE	—	PE0, PE1, PE3 to PE5
	PORTN	—	PN6, PN7
Open-drain output function	PORT0	—	P00, P01
	PORT1	—	P10, P11
	PORT2	—	P20 to P24, P27
	PORT3	—	P30 to P33, P36, P37
	PORT4	—	P40 to P47
	PORT5	—	P50 to P55
	PORT6	—	P60 to P65
	PORT7	—	P70 to P76
	PORT8	—	P80 to P82
	PORT9	—	P90 to P96
	PORTA	—	PA0 to PA5
	PORTB	PB1 (for SCL only), PB2 (for SDA only)	PB0 to PB7
	PORTD	—	PD0 to PD7
	PORTE	—	PE0, PE1, PE3 to PE5
	PORTN	—	PN6, PN7
5 V tolerant	PORTB	—	PB1, PB2

Table 2.28 Comparison of I/O Port Registers

Register	Bit	RX62T	RX26T
DDR	—	Data direction register	—
DR	—	Data register	—
PORT	—	Port register	—
ICR	—	Input buffer control register	—
PF8IRQ	—	Port function register 8	—
PF9IRQ	—	Port function register 9	—
PFAADC	—	Port function register A	—
PFCMTU	—	Port function register C	—
PFDGPT	—	Port function register D	—
PFFSCI	—	Port function register F	—
PFGSPI	—	Port function register G	—
PFHSPI	—	Port function register H	—
PFJCAN	—	Port function register F	—
PFKLIN	—	Port function register K	—
PFMPOE	—	Port function register H	—
PFNPOE	—	Port function register N	—
PDR	—	—	Port direction register
PODR	—	—	Port output data register
PIDR	—	—	Port input data register
PMR	—	—	Port mode register
ODR0	—	—	Open drain control register 0
ODR1	—	—	Open drain control register 1
PCR	—	—	Pull-up control register
DSCR	—	—	Drive capacity control register
DSCR2	—	—	Drive capacity control register 2
POHSR1	—	—	Port output retention setting register 1
POHSR2	—	—	Port output retention setting register 2
POHCR	—	—	Port output retention control register
GPSEXT	—	—	Extended register for general-purpose I/O pin selection

2.14 Multi-Function Timer Pulse Unit 3

Table 2.29 is Comparative Overview of Multi-Function Timer Pulse Unit 3, and Table 2.30 is Comparison of Multi-Function Timer Pulse Unit 3 Registers.

Table 2.29 Comparative Overview of Multi-Function Timer Pulse Unit 3

Item	RX62T (MTU3)	RX26T (MTU3d)
Pulse input/output	Max. 24 lines	Max. 28 lines
Pulse input	3 lines	3 lines
Count clocks	6 to 8 clocks for each channel (4 for channel 5)	11 clocks for each channel (14 for MTU0 and MTU9, 12 for MTU2, 10 for MTU5, and 4 for MTU1 and MTU2 (when LWA = 1))
Operating frequency	8 to 100 MHz	Up to 120 MHz
Available operations	[MTU0 to MTU4, MTU6, MTU7] • Waveform output at compare match • Input capture function • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Simultaneous register input/output by synchronous counter operation • Up to 12-phase PWM output in combination with synchronous operation	[MTU0 to MTU4, MTU6, MTU7, MTU9] • Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Simultaneous register input/output by synchronous counter operation • Up to 14-phase PWM output in combination with synchronous operation
	[MTU0, MTU3, MTU4, MTU6, MTU7] • Ability to specify buffer operation	[MTU0, MTU3, MTU4, MTU6, MTU7, MTU9] • Ability to specify buffer operation
	—	[MTU1, MTU2] • Independent specification of phase counting mode • Ability to specify 32-bit phase counting mode linked to MTU1 or MTU2 (when TMDR3.LWA = 1) • Cascade connection operation
	[MTU3, MTU4, MTU6, MTU7] • Ability to produce 12-phase waveform output, comprising six phases each of positive and negative output, in complementary PWM or reset PWM mode, through linked operation of MTU3 or MTU4 and MTU6 or MTU7 • In complementary PWM mode, ability to transfer data from the buffer register to a temporary register at peaks or troughs of the timer counter or when writes to the buffer register (MTU4.TGRD or MTU7.TGRD) occur • Ability to specify double buffer function in complementary PWM mode	[MTU3, MTU4, MTU6, MTU7] • Ability to produce 12-phase waveform output, comprising six phases each of positive and negative output, in complementary PWM or reset PWM mode, through linked operation of MTU3 or MTU4 and MTU6 or MTU7 • In complementary PWM mode, ability to transfer data from the buffer register to a temporary register at peaks or troughs of the timer counter or when writes to the buffer register (MTU4.TGRD or MTU7.TGRD) occur • Ability to specify double buffer function in complementary PWM mode

Item	RX62T (MTU3)	RX26T (MTU3d)
Available operations	[MTU3, MTU4] • Through linked operation with MTU0, ability to specify the AC synchronous motor (brushless DC motor) drive mode using complementary PWM or reset PWM and to select two types (chopping or level) of waveform output	[MTU3, MTU4] • Through linked operation with MTU0, ability to specify the AC synchronous motor (brushless DC motor) drive mode using complementary PWM or reset PWM and to select two types (chopping or level) of waveform output
	[MTU5] • Can be used as a dead time compensation counter.	[MTU5] • Can be used as a dead time compensation counter.
	—	[MTU6, MTU7] • Through linked operation with MTU9, ability to specify the AC synchronous motor (brushless DC motor) drive mode using complementary PWM or reset PWM and to select two types (chopping or level) of waveform output
Interrupt skipping function	Ability to skip interrupts at counter peak or trough and A/D conversion start triggers in complementary PWM mode	Ability to skip interrupts at counter peak or trough and A/D conversion start triggers in complementary PWM mode
Interrupt sources	38 sources	45 sources
Buffer operation	Automatic transfer of register data (transfer from buffer register to timer register)	Automatic transfer of register data (transfer from buffer register to timer register)
Trigger generation	• Ability to generate A/D conversion start trigger • Ability to start A/D conversion at user-specified timing using A/D conversion start request delaying function Ability to synchronize operation with PWM output	• Ability to generate A/D conversion start trigger • Ability to start A/D conversion at user-specified timing using A/D conversion start request delaying function Ability to synchronize operation with PWM output
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.30 Comparison of Multi-Function Timer Pulse Unit 3 Registers

Register	Bit	RX62T (MTU3)	RX26T (MTU3d)
TCR2	—	—	Timer control register 2
TMDR1	BFE	Buffer operation E bit 0: MTU0.TGRE and MTU0.TGRF are in normal operation 1: MTU0.TGRE and MTU0.TGRF are in buffer operation	Buffer operation E bit 0: MTU0.TGRE, MTU0.TGRF, MTU9.TGRE, and MTU9.TGRF are in normal operation 1: MTU0.TGRE, MTU0.TGRF, MTU9.TGRE, and MTU9.TGRF are in buffer operation
TMDR3	—	—	Timer mode register 3
MTU0, TIORH	IOA[3:0]	I/O control A bits b3 b0 0 0 0 0: Output prohibited 0 0 0 1: Initial output is low Low output upon compare match 0 0 1 0: Initial output is low High output upon compare match 0 0 1 1: Initial output is low Toggle output upon compare match 0 1 0 0: Output prohibited 0 1 0 1: Initial output is high Low output upon compare match 0 1 1 0: Initial output is high High output upon compare match 0 1 1 1: Initial output is high Toggle output upon compare match 1 0 0 0: Input capture at rising edge 1 0 0 1: Input capture at falling edge 1 0 1 x: Input capture at both edges 1 1 x x: Capture input source is MTU1/count clock. Input capture upon counting-up or counting-down of MTU1.TCNT	I/O control A bits b3 b0 0 0 0 0: Output prohibited 0 0 0 1: Initial output is low Low output upon compare match 0 0 1 0: Initial output is low High output upon compare match 0 0 1 1: Initial output is low Toggle output upon compare match 0 1 0 0: Output prohibited 0 1 0 1: Initial output is high Low output upon compare match 0 1 1 0: Initial output is high High output upon compare match 0 1 1 1: Initial output is high Toggle output upon compare match 1 0 0 0: Input capture at rising edge 1 0 0 1: Input capture at falling edge 1 0 1 x: Input capture at both edges 1 1 0 x: Capture input source is MTU1/count clock. Input capture upon counting-up or counting-down of MTU1.TCNT (LWA = 0) or MTU1.TCNTLW (LWA = 1)
MTU9, TIORH	IOA[3:0]	—	I/O control A bits

Register	Bit	RX62T (MTU3)	RX26T (MTU3d)
MTU1, TIOR	IOB[3:0]	I/O control B bits b3 b0 0 0 0 0: Output prohibited 0 0 0 1: Initial output is low Low output upon compare match 0 0 1 0: Initial output is low High output upon compare match 0 0 1 1: Initial output is low Toggle output upon compare match 0 1 0 0: Output prohibited 0 1 0 1: Initial output is high Low output upon compare match 0 1 1 0: Initial output is high High output upon compare match 0 1 1 1: Initial output is high Toggle output upon compare match 1 0 0 0: Input capture at rising edge 1 0 0 1: Input capture at falling edge 1 0 1 x: Input capture at both edges 1 1 x x: Input capture upon compare match or input capture of MTU0.TGRC	I/O control B bits b3 b0 0 0 0 0: Output prohibited 0 0 0 1: Initial output is low Low output upon compare match 0 0 1 0: Initial output is low High output upon compare match 0 0 1 1: Initial output is low Toggle output upon compare match 0 1 0 0: Output prohibited 0 1 0 1: Initial output is high Low output upon compare match 0 1 1 0: Initial output is high High output upon compare match 0 1 1 1: Initial output is high Toggle output upon compare match 1 0 0 0: Input capture at rising edge 1 0 0 1: Input capture at falling edge 1 0 1 x: Input capture at both edges 1 1 0 x: Input capture upon compare match or input capture of MTU0.TGRC
MTU9, TIORH	IOB[3:0]	—	I/O control B bits
MTU9, TIORL	IOC[3:0]	—	I/O control C bits
	IOD[3:0]	—	I/O control D bits

Register	Bit	RX62T (MTU3)	RX26T (MTU3d)
TIORU, TIORV, and TIORW (MTU5)	IOC[4:0]	I/O control C bits 0 0 0 0 0: Compare match 0 0 0 0 1: Setting prohibited 0 0 0 1 x: Setting prohibited 0 0 1 x x: Setting prohibited 0 1 x x x: Setting prohibited 1 0 0 0 0: Setting prohibited 1 0 0 0 1: Input capture at rising edge 1 0 0 1 0: Input capture at falling edge 1 0 0 1 1: Input capture at both edges 1 0 1 x x: Setting prohibited 1 1 0 0 0: Setting prohibited 1 1 0 0 1: Input capture at trough of complementary PWM mode for low pulse measurement of external input signal 1 1 0 1 0: Input capture at peak of complementary PWM mode for low pulse measurement of external input signal 1 1 0 1 1: Input capture at peak and trough of complementary PWM mode for Low pulse measurement of external input signal 1 1 1 0 0: Setting prohibited 1 1 1 0 1: Input capture at trough of complementary PWM mode for high pulse measurement of external input signal 1 1 1 1 0: Input capture at peak of complementary PWM mode for high pulse measurement of external input signal 1 1 1 1 1: Input capture at peak and trough of complementary PWM mode for high pulse measurement of external input signal	I/O control C bits 0 0 0 0 0: No function 0 0 0 0 1: Setting prohibited 0 0 0 1 x: Setting prohibited 0 0 1 x x: Setting prohibited 0 1 x x x: Setting prohibited 1 0 0 0 0: Setting prohibited 1 0 0 0 1: Input capture at rising edge 1 0 0 1 0: Input capture at falling edge 1 0 0 1 1: Input capture at both edges 1 0 1 x x: Setting prohibited 1 1 0 0 0: Setting prohibited 1 1 0 0 1: Input capture at trough of complementary PWM mode for low pulse measurement of external input signal 1 1 0 1 0: Input capture at peak of complementary PWM mode for low pulse measurement of external input signal 1 1 0 1 1: Input capture at peak and trough of complementary PWM mode for low pulse measurement of external input signal 1 1 1 0 0: Setting prohibited 1 1 1 0 1: Input capture at trough of complementary PWM mode for high pulse measurement of external input signal 1 1 1 1 0: Input capture at peak of complementary PWM mode for high pulse measurement of external input signal 1 1 1 1 1: Input capture at peak and trough of complementary PWM mode for high pulse measurement of external input signal
TSR	TGFA	Input capture/output compare flag A	—
	TGFB	Input capture/output compare flag B	—
	TGFC	Input capture/output compare flag C	—
	TGFD	Input capture/output compare flag D	—
TSR	TCFV	Overflow flag	—
	TCFU	Underflow flag	—

Register	Bit	RX62T (MTU3)	RX26T (MTU3d)
TBTM	TTSE	Timing select E bit 0: Transfer from MTU0.TGRF to MTU0.TGRE is made upon compare match E of MTU0 1: Transfer from MTU0.TGRF to MTU0.TGRE is made when MTU0.TCNT is cleared	Timing select E bit 0: Transfer from MTU0.TGRF to MTU0.TGRE or from MTU9.TGRF to MTU9.TGRE is made upon compare match E of MTU0 or MTU9. 1: Transfer from MTU0.TGRF to MTU0.TGRE or from MTU9.TGRF to MTU9.TGRE is made when MTU0.TCNT or MTU9.TCNT is cleared.
TCNTLW	—	—	Timer longword counter
TGRmLW	—	—	Timer longword general register m (m = A, B)
TSTR (RX62T) TSTRA/ TSTRB/ TSTR (RX26T)	CST9	—	Counter start 9 bit
TSYR (RX62T) TSYRA/ TSYRB (RX26T)	SYNC9	—	Timer synchronous 9 bit
TCSYSTR	SCH9	—	Synchronous start 9 bit
TOER (RX62T) TOERA/ TOERB (RX26T)	—	Timer output master enable register	Timer output master enable register
TGCRB	—	—	Timer gate control register B
NFCRn	—	—	Noise filter control register n (n = 0 to 4, 6, 7, 9, C)
NFCR5	—	—	Noise filter control register 5
TADSTRGR0	—	—	A/D conversion start request select register 0
TADSTRGR1	—	—	A/D conversion start request select register 1

2.15 Port Output Enable 3

Table 2.31 is Comparative Overview of Port Output Enable 3, and Table 2.32 is Comparison of Port Output Enable 3 Registers.

Table 2.31 Comparative Overview of Port Output Enable 3

Item	RX62T (POE3)	RX26T (POE3D)
Pin status while output is disabled	• High-impedance • General I/O port	• High-impedance • General I/O port
Target pins for output stop control	• MTU output pins — MTU3 pins (MTIOC3B, MTIOC3D) — MTU4 pins (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) — MTU6 pins (MTIOC6B, MTIOC6D) — MTU7 pins (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D) • GPT output pins — GPT0 pins (GTIOC0A-A, GTIOC0B-A) — GPT1 pins (GTIOC0A-B, GTIOC0B-B) — GPT2 pins (GTIOC0A-C, GTIOC0B-C)	• MTU output pins — MTU0 pins (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) — MTU3 pins (MTIOC3B, MTIOC3D) — MTU4 pins (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) — MTU6 pins (MTIOC6B, MTIOC6D) — MTU7 pins (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D) — MTU9 pins (MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D) • GPTW output pins — GPTW0 pins (GTIOC0A, GTIOC0B) — GPTW1 pins (GTIOC1A, GTIOC1B) — GPTW2 pins (GTIOC2A, GTIOC2B) — GPTW3 pins (GTIOC3A, GTIOC3B) — GPTW4 pins (GTIOC4A, GTIOC4B) — GPTW5 pins (GTIOC5A, GTIOC5B) — GPTW6 pins (GTIOC6A, GTIOC6B) — GPTW7 pins (GTIOC7A, GTIOC7B)

Item	RX62T (POE3)	RX26T (POE3D)
Conditions for generating output stop requests	• Input pin changes: When signal input occurs on pin POE0#, POE4#, POE8#, POE10#, or POE11# • When the SPOER register is set • Upon detection of stopped oscillation on clock oscillator • Short circuit of output pins: A match (short circuit condition) between the output signal levels at the active level lasts at least one cycle on one of the following combinations of pins. [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D — MTIOC6B and MTIOC6D — MTIOC7A and MTIOC7C — MTIOC7B and MTIOC7D [GPT output pins] — GTIOC0A-A and GTIOC0B-A — GTIOC1A-A and GTIOC1B-A — GTIOC2A-A and GTIOC2B-A	• Input pin changes: When signal input occurs on pin POE0#, POE4#, POE8#, POE10#, POE11#, POE12#, or POE9# • When the SPOER register is set • Detection of stopped oscillation on main clock oscillator • Detection of comparator C (CMPC) output • Short circuit of output pins: A match (short circuit condition) between the output signal levels at the active level lasts at least one cycle on one of the following combinations of pins. [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D — MTIOC6B and MTIOC6D — MTIOC7A and MTIOC7C — MTIOC7B and MTIOC7D [GPTW output pins] — GTIOC0A and GTIOC0B — GTIOC1A and GTIOC1B — GTIOC2A and GTIOC2B — GTIOC4A and GTIOC4B — GTIOC5A and GTIOC5B — GTIOC6A and GTIOC6B — GTIOC7A and GTIOC7B
Functions	• Falling-edge detection or sampling of the low level 16 times at PCLK/8, PCLK/16, or PCLK/128 can be set for each of the POE0#, POE4#, POE8#, POE10#, and POE11# input pins. • The MTU complementary PWM output pin, MTU0 pin, and GPT pin can be driven to the high-impedance state by a falling edge or low level sampling on the POE0#, POE4#, POE8#, POE10#, or POE11# pin.	• Falling-edge detection or low level detection can be set for each of the POE0#, POE4#, POE8#, POE10#, POE11#, POE12#, and POE9# pins. For low level detection, the sampling clock can be selected from PCLK/1, PCLK/2, PCLK/4, PCLK/8, PCLK/16, and PCLK/128, and the sampling count can be selected from 4, 8, and 16. • Output on all control target pins can be stopped on detection of the falling edge or low level of input to the POE0#, POE4#, POE8#, POE10#, POE11#, POE12#, or POE9# pin.

Item	RX62T (POE3)	RX26T (POE3D)
Functions	• The MTU complementary PWM output pin, MTU0 pin, and GPT pin can be driven to the high-impedance state upon detection of stopped oscillation on clock oscillator.	• Output on all control target pins can be stopped when oscillation stop is detected in the clock generation circuit.
	• The MTU complementary PWM output pins or GPT large current output pins can be driven to the high-impedance state when output levels of those pins are compared and simultaneous active-level output continues for one or more cycles.	• Output on the MTU complementary PWM output pins can be stopped when output levels of those pins are compared and simultaneous active-level output continues for one or more cycles.
		• Output on the GPTW output pins (GPTW0 to GPTW2, GPTW4 to GPTW7) can be stopped when output levels of those pins are compared and simultaneous active-level output continues for one or more cycles.
	• The MTU complementary PWM output pins, MTU0 pin, and GPT pin can be driven to the high-impedance state by comparator detection of 12-bit A/D converter (S12ADA).	
		• Output on all control target pins can be stopped on detection of output of comparator C (CMPC).
	• The MTU complementary PWM output pins, MTU0 pin, and GPT pin can be driven to the high-impedance state by POE3 register setting.	• Output on all control target pins can be stopped by modifying the settings of POE registers.
	• Interrupts can be generated in response to the results of input level sampling or output-level comparison.	• Interrupts can be generated in response to the results of input level sampling or output-level comparison.
		• Output stop requests in response to level detection signals on the POE0#, POE4#, POE8#, POE10#, POE11#, POE12#, and POE9# pins and COMP0 to COMP5 can be masked by using signals output from the MTU output pins (MTU0 to MTU4, MTU6, MTU7, and MTU9) and GPTW output pins (GPTW0 to GPTW7).

Table 2.32 Comparison of Port Output Enable 3 Registers

Register	Bit	RX62T (POE3)	RX26T (POE3D)
ICSR1	POE0M[1:0] (RX62T) POE0M[3:0] (RX26T)	POE0 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE0# pin input. 0 1: Samples the low level of the POE0# pin input 16 times at PCLK/8 clock pulses, and accepts a request when all are low level. 1 0: Samples the low level of the POE0# pin input 16 times at PCLK/16 clock pulses, and accepts a request when all are low level. 1 1: Samples the low level of the POE0# pin input 16 times at PCLK/128 clock pulses, and accepts a request when all are low level.	POE0 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge or rising edge of POE0# pin input. 0 0 0 1: Samples the input from the POE0# pin by PCLK/8, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 0 1 0: Samples the input from the POE0# pin by PCLK/16, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 0 1 1: Samples the input from the POE0# pin by PCLK/128, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 0 0: Samples the input from the POE0# pin by PCLK, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 0 1: Samples the input from the POE0# pin by PCLK/2, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 1 0: Samples the input from the POE0# pin by PCLK/4, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. Settings other than the above are prohibited.
	POE0M2[3:0]	—	POE0 sampling count select bits
	INV	—	POE0# pin input invert bit

Register	Bit	RX62T (POE3)	RX26T (POE3D)
ICSR2	POE4M[1:0] (RX62T) POE4M[3:0] (RX26T)	POE4 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE4# pin input. 0 1: Samples the low level of the POE4# pin input 16 times at PCLK/8 clock pulses, and accepts a request when all are low level. 1 0: Samples the low level of the POE4# pin input 16 times at PCLK/16 clock pulses, and accepts a request when all are low level. 1 1: Samples the low level of the POE4# pin input 16 times at PCLK/128 clock pulses, and accepts a request when all are low level.	POE4 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge or rising edge of the POE4# pin input. 0 0 0 1: Samples the input from the POE4# pin by PCLK/8, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 0 1 0: Samples the input from the POE4# pin by PCLK/16, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 0 1 1: Samples the input from the POE4# pin by PCLK/128, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 0 0: Samples the input from the POE4# pin by PCLK, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 0 1: Samples the input from the POE4# pin by PCLK/2, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 1 0: Samples the input from the POE4# pin by PCLK/4, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. Settings other than the above are prohibited.
	POE4M2[3:0]	—	POE4 sampling count select bits
	INV	—	POE4# pin input invert bit

Register	Bit	RX62T (POE3)	RX26T (POE3D)
ICSR3	POE8M[1:0] (RX62T) POE8M[3:0] (RX26T)	POE8 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE8# pin input. 0 1: Samples the low level of the POE8# pin input 16 times at PCLK/8 clock pulses, and accepts a request when all are low level. 1 0: Samples the low level of the POE8# pin input 16 times at PCLK/16 clock pulses, and accepts a request when all are low level. 1 1: Samples the low level of the POE8# pin input 16 times at PCLK/128 clock pulses, and accepts a request when all are low level.	POE8 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge or rising edge of the POE8# pin input. 0 0 0 1: Samples the input from the POE8# pin by PCLK/8, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 0 1 0: Samples the input from the POE8# pin by PCLK/16, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 0 1 1: Samples the input from the POE8# pin by PCLK/128, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 0 0: Samples the input from the POE8# pin by PCLK, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 0 1: Samples the input from the POE8# pin by PCLK/2, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 1 0: Samples the input from the POE8# pin by PCLK/4, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. Settings other than the above are prohibited.
	POE8M2[3:0]	—	POE8 sampling count select bits
	INV	—	POE8# pin input invert bit

Register	Bit	RX62T (POE3)	RX26T (POE3D)
ICSR4	POE10M[1:0] (RX62T) POE10M[3:0] (RX26T)	POE10 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE10# pin input. 0 1: Samples the low level of the POE10# pin input 16 times at PCLK/8 clock pulses, and accepts a request when all are low level. 1 0: Samples the low level of the POE10# pin input 16 times at PCLK/16 clock pulses, and accepts a request when all are low level. 1 1: Samples the low level of the POE10# pin input 16 times at PCLK/128 clock pulses, and accepts a request when all are low level.	POE10 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge or rising edge of the POE10# pin input. 0 0 0 1: Samples the input from the POE10# pin by PCLK/8, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 0 1 0: Samples the input from the POE10# pin by PCLK/16, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 0 1 1: Samples the input from the POE10# pin by PCLK/128, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 0 0: Samples the input from the POE10# pin by PCLK, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 0 1: Samples the input from the POE10# pin by PCLK/2, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 1 0: Samples the input from the POE10# pin by PCLK/4, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. Settings other than the above are prohibited.
	POE10M2[3:0]	—	POE10 sampling count select bits
	INV	—	POE10# pin input invert bit

Register	Bit	RX62T (POE3)	RX26T (POE3D)
ICSR5	POE11M[1:0] (RX62T) POE11M[3:0] (RX26T)	POE11 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE11# pin input. 0 1: Samples the low level of the POE11# pin input 16 times at PCLK/8 clock pulses, and accepts a request when all are low level. 1 0: Samples the low level of the POE11# pin input 16 times at PCLK/16 clock pulses, and accepts a request when all are low level. 1 1: Samples the low level of the POE11# pin input 16 times at PCLK/128 clock pulses, and accepts a request when all are low level.	POE11 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge or rising edge of the POE11# pin input. 0 0 0 1: Samples the input from the POE11# pin by PCLK/8, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 0 1 0: Samples the input from the POE11# pin by PCLK/16, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 0 1 1: Samples the input from the POE11# pin by PCLK/128, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 0 0: Samples the input from the POE11# pin by PCLK, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 0 1: Samples the input from the POE11# pin by PCLK/2, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 1 0: Samples the input from the POE11# pin by PCLK/4, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. Settings other than the above are prohibited.
	POE11M2[3:0]	—	POE11 sampling count select bits
	INV	—	POE11# pin input invert bit
ICSR6	—	—	Input level control/status register 6
ICSR7	—	—	Input level control/status register 7
ICSR8	—	—	Input level control/status register 8
OCSR3	—	—	Output level control/status register 3
OCSR4	—	—	Output level control/status register 4
OCSR5	—	—	Output level control/status register 5
ALR2	—	—	Active level register 2
ALR3	—	—	Active level register 3
ALR4	—	—	Active level register 4
ALR5	—	—	Active level register 5

Register	Bit	RX62T (POE3)	RX26T (POE3D)
SPOER	—	Software port output enable register SPOER is an 8-bit register.	Software port output enable register SPOER is a 16-bit register.
	GPT01HIZ	GPT0 and GPT1 pin output stop enable bit	GPTW0 and GPTW1 pin output stop enable bit
	GPT23HIZ	GPT2 and GPT3 pin output stop enable bit	GPTW2 and GPTW3 pin output stop enable bit
	MTUCH9HIZ	—	MTU9 pin output stop enable bit
	GPT02HIZ	—	GPTW0 to GPTW2 pin output stop enable bit
	GPT46HIZ	—	GPTW4 to GPTW6 pin output stop enable bit
	GPT79HIZ	—	GPTW7 pin output stop enable bit
POECR3	GPT2ABZE	GPT CH2AB high-impedance enable bit (b8)	GTIOC2A/GTIOC2B pin high impedance enable bit (b2)
	GPT3ABZE	GPT CH3AB high-impedance enable bit (b9)	GTIOC3A/GTIOC3B pin high impedance enable bit (b3)
	GPT4ABZE	—	GTIOC4A/GTIOC4B pin high impedance enable bit
	GPT5ABZE	—	GTIOC5A/GTIOC5B pin high impedance enable bit
	GPT6ABZE	—	GTIOC6A/GTIOC6B pin high impedance enable bit
	GPT7ABZE	—	GTIOC7A/GTIOC7B pin high impedance enable bit
POECR4	IC1ADDMT34ZE	—	Bit for adding POE0F to the MTU3 and MTU4 output stop conditions
	IC6ADDMT34ZE	—	Bit for adding POE12F to the MTU3 and MTU4 output stop conditions
	IC8ADDMT34ZE	—	Bit for adding POE9F to the MTU3 and MTU4 output stop conditions
	CMADDMT67ZE	Bit for adding CFLAG to MTU CH67 high-impedance	
	IC1ADDMT67ZE	Bit for adding POE0F to MTU CH67 high-impedance	
	IC3ADDMT67ZE	Bit for adding POE8F to MTU CH67 high-impedance	—
	IC4ADDMT67ZE	Bit for adding POE10F to MTU CH67 high-impedance	—
	IC5ADDMT67ZE	Bit for adding POE11F to MTU CH67 high-impedance	—
POECR4B	—	—	Port output enable control register 4B
POECR5	IC3ADDMT0ZE	—	Bit for adding POE8F to the MTU0 output stop conditions
	IC6ADDMT0ZE	—	Bit for adding POE12F to the MTU0 output stop conditions
	IC8ADDMT0ZE	—	Bit for adding POE9F to the MTU0 output stop conditions
POECR6	IC4ADDGPT01ZE	—	Bit for adding POE10F to the GPTW0 and GPTW1 output stop conditions
	IC6ADDGPT01ZE	—	Bit for adding POE12F to the GPTW0 and GPTW1 output stop conditions
	IC8ADDGPT01ZE	—	Bit for adding POE9F to the GPTW0 and GPTW1 output stop conditions
	CMADDGPT23ZE	Bit for adding CFLAG to GPT CH23 high-impedance	—
	IC1ADDGPT23ZE	Bit for adding POE0F to GPT CH23 high-impedance	—

Register	Bit	RX62T (POE3)	RX26T (POE3D)
POECR6	IC2ADDGPT23ZE	Bit for adding POE4F to GPT CH23 high-impedance	—
	IC3ADDGPT23ZE	Bit for adding POE8F to GPT CH23 high-impedance	—
	IC4ADDGPT23ZE	Bit for adding POE10F to GPT CH23 high-impedance	—
POECR6B	—	—	Port output enable control register 6B
POECR7	—	—	Port output enable control register 7
POECR8	—	—	Port output enable control register 8
POECR9	—	—	Port output enable control register 9
POECR10	—	—	Port output enable control register 10
POECR11	—	—	Port output enable control register 11
PMMCR0	—	—	Port mode mask control register 0
PMMCR1	—	—	Port mode mask control register 1
PMMCR2	—	—	Port mode mask control register 2
POECMPFR	—	—	Port output enable comparator detection flag register
POECMPSEL	—	—	Port output enable comparator request select register
POECMPEXm	—	—	Port output enable comparator request extended select register m (m = 0 to 8)
M0SELR1	—	—	MTU0 pin select register 1
M0SELR2	—	—	MTU0 pin select register 2
M3SELR	—	—	MTU3 pin select register
M4SELR1	—	—	MTU4 pin select register 1
M4SELR2	—	—	MTU4 pin select register 2
M6SELR	—	—	MTU6 pin select register
M7SELR1	—	—	MTU7 pin select register 1
M7SELR2	—	—	MTU7 pin select register 2
M9SELR1	—	—	MTU9 pin select register 1
M9SELR2	—	—	MTU9 pin select register 2
G0SELR	—	—	GPTW0 pin select register
G1SELR	—	—	GPTW1 pin select register
G2SELR	—	—	GPTW2 pin select register
G3SELR	—	—	GPTW3 pin select register
G4SELR	—	—	GPTW4 pin select register
G5SELR	—	—	GPTW5 pin select register
G6SELR	—	—	GPTW6 pin select register
G7SELR	—	—	GPTW7 pin select register
IMCR0	—	—	Input signal mask control register 0
IMCR1	—	—	Input signal mask control register 1
IMCR2	—	—	Input signal mask control register 2
IMCR3	—	—	Input signal mask control register 3
IMCR4	—	—	Input signal mask control register 4
IMCR5	—	—	Input signal mask control register 5
IMCR6	—	—	Input signal mask control register 6
IMCR9	—	—	Input signal mask control register 9
IMCR10	—	—	Input signal mask control register 10
IMCR11	—	—	Input signal mask control register 11
IMCR12	—	—	Input signal mask control register 12
IMCR13	—	—	Input signal mask control register 13
IMCR14	—	—	Input signal mask control register 14

2.16 General Purpose PWM Timer

Table 2.33 is Comparative Overview of General Purpose PWM Timers, and Table 2.34 is Comparison of General Purpose PWM Timer Registers.

Table 2.33 Comparative Overview of General Purpose PWM Timers

Item	RX62T (GPT/GPTa)	RX26T (GPTWa)
Functions	• 16 bits × 4 channels • Up-counting or down-counting (saw waves) and up/down-counting (triangle waves) selectable for each counter • Independent clock sources selectable for each channel • Two input/output pins provided for each channel • Two output compare/input capture registers provided for each channel • For the two output compare/input capture registers for each channel, four buffer registers are provided and they can operate as comparison registers when buffering is not in use. • In output compare operation, buffer operation is possible at crests and troughs, and laterally asymmetric PWM waveforms are generated. • A register for setting up frame cycles is provided for each channel (interrupts can be generated at overflow or underflow). • Synchronous operation of the several counters • Synchronous operation modes: simultaneous start or phase shifting start by desired times • Dead time can be generated during PWM operation. • Generation of three-phase PWM waveforms incorporating dead time by combining three counters • Starting, clearing, and stopping counters in response to external or internal triggers • Internal trigger sources: comparator detection, software, and compare match • The edge of the divided clock from the IWDT-dedicated low-speed on-chip oscillator can be measured by the count clock of the divided system clock (ICLK) (oscillation error detection).	• 32 bits × 8 channels (for products with RAM capacity 64 KB) • 16 bits × 8 channels (for products with RAM capacity 48 KB) • Up-counting or down-counting (saw waves) and up/down-counting (triangle waves) selectable for each counter • Independent clock sources selectable for each channel • Two input/output pins provided for each channel • Two output compare/input capture registers provided for each channel • For the two output compare/input capture registers for each channel, four buffer registers are provided and they can operate as comparison registers when buffering is not in use. • In output compare operation, buffer operation is possible at crests and troughs, and laterally asymmetric PWM waveforms are generated. • A register for setting up frame cycles is provided for each channel (interrupts can be generated at overflow or underflow). • Synchronized setting, clearing, and input capture can be performed between channels. • Dead time can be generated during PWM operation. • Count start, count stop, counter clearing, up-counting, down-counting, and input capture operations can be triggered by a maximum of four external triggers.

Item	RX62T (GPT/GPTa)	RX26T (GPTWa)
Functions	• For two PWM output pins of each channel, rising/falling timing can be controlled by the 1/32 resolution of the system clock (ICLK) (PWM delay generation function) (RX62G Group only).	• A high precision duty cycle of near 100% and 0% of the PWM output can be generated. • In output compare operation, PWM waveforms can be generated by immediately applying the compare register settings to provide dead times. • Simultaneous start, stop, and clearing of any channel counters • Operation of count start/count stop/counter clearing/up-counting/down-counting/input capture by maximum of eight ELC events based on ELC settings • Count start, count stop, counter clearing, up-counting, down-counting, and input capture operations can be performed by detection of the condition of two input signals. • Function to control output negation due to dead time errors or output stop requests from the POEG • A/D converter start trigger generation function • Event signals for compare match A to F and for underflow or overflow can be output to the ELC. • The noise filter function can be selected for input capture input. • Cycle count function • Function for measuring the external input pulse width • Logical operations of compare match output are possible between channels. • Bus clock: PCLKA, GPTWA count reference clock: PCLKC • PCLKA to PCLKC frequency ratio = 1:N (N = 1/2)

Table 2.34 Comparison of General Purpose PWM Timer Registers

Register	Bit	RX62T (GPT/GPTa)	RX26T (GPTWa)
GTSTR	CST0 (RX62T) CSTRT0 (RX26T)	GPT0.GTCNT count start bit	Channel 0 count start bit
	CST1 (RX62T) CSTRT1 (RX26T)	GPT1.GTCNT count start bit	Channel 1 count start bit
	CST2 (RX62T) CSTRT2 (RX26T)	GPT2.GTCNT count start bit	Channel 2 count start bit
	CST3 (RX62T) CSTRT3 (RX26T)	GPT3.GTCNT count start bit	Channel 3 count start bit
	CSTRT4	—	Channel 4 count start bit
	CSTRT5	—	Channel 5 count start bit
	CSTRT6	—	Channel 6 count start bit
	CSTRT7	—	Channel 7 count start bit
GTHSCR	—	General purpose PWM timer hardware source start control register	—
GTHCCR	—	General purpose PWM timer hardware source clear control register	—
GTHSSR	—	General purpose PWM timer hardware start source select register	—
GTHPSR	—	General purpose PWM timer hardware stop/clear source select register	—
GTWP	WP0	GPT0 register write enable bit	—
	WP1	GPT1 register write enable bit	—
	WP2	GPT2 register write enable bit	—
	WP3	GPT3 register write enable bit	—
	WP	—	Register write disable bit
	STRWP	—	GTSTR.CSTRT bit write disable bit
	STPWP	—	GTSTP.CSTOP bit write disable bit
	CLRWP	—	GTCLR.CCLR bit write disable bit
	CMNWP	—	Common register write disable bit
	PRKEY[7:0]	—	GTWP key code bit
GTSYNC	—	General purpose PWM timer sync register	—
GTETINT	—	General purpose PWM timer external trigger input interrupt register	—
GTBDR	—	General purpose PWM timer buffer operation disable register	—
GTSWP	—	General purpose PWM timer start write protection register	—
LCCR	—	LOCO count control register	—
LCST	—	LOCO count status register	—

Register	Bit	RX62T (GPT/GPTa)	RX26T (GPTWa)
LCNT	—	LOCO count value register	—
LCNTA	—	LOCO count result average register	—
LCNTn	—	LOCO count result register n (n = 00 to 15)	—
LCNTDU/ LCNTDL	—	LOCO count upper/lower permissible deviation register	—
GTIOR	GTIOA[5:0] (RX62T) GTIOA[4:0] (RX26T)	GTIOCnA pin function select bits GTIOR is a 16-bit register.	GTIOCnA pin function select bits GTIOR is a 32-bit register.
	CPSCIR	—	Bit for suppressing initial output for simultaneous clearing in complementary PWM mode
	OAE	—	GTIOCnA pin output enable bit
	OADF[1:0]	—	GTIOCnA pin negate value setting bits
	OAEOCD	—	Bit for disabling output of the end of the cycle on a compare match in the GTCCRA register
	PSYE	—	PWM cycle simultaneous output enable bit
	NFAEN	—	GTIOCnA pin input noise filter enable bit
	NFCSA[1:0]	—	GTIOCnA pin input noise filter sampling clock select bits
	GTIOB[5:0] (RX62T) GTIOB[4:0] (RX26T)	GTIOCnB pin function select bits (b13 to b8)	GTIOCnB pin function select bits (b20 to b16)
	OBDFLT	Output value at GTIOCnB pin count stop bit (b14)	Output value at GTIOCnB pin count stop bit (b22)
	OBHLD	Output retain at GTIOCnB pin count start/stop bit (b15)	Output retain at GTIOCnB pin count start/stop bit (b23)
	OBE	—	GTIOCnB pin output enable bit
	OBDF[1:0]	—	GTIOCnB pin negate value setting bits
	OBEOCD	—	Bit for disabling output of the end of the cycle on a compare match in the GTCCRB register
	NFBEN	—	GTIOCnB pin input noise filter enable bit
	NFCSB[1:0]	—	GTIOCnB pin input noise filter sampling clock select bits
GTINTAD	—	General purpose PWM timer interrupt output setting register GTINTAD is a 16-bit register.	General purpose PWM timer interrupt output setting register GTINTAD is a 32-bit register.
	SCFA	—	GTCCRA register compare match/input capture source synchronous clear enable bit
	SCFB	—	GTCCRB register compare match/input capture source synchronous clear enable bit

Register	Bit	RX62T (GPT/GPTa)	RX26T (GPTWa)
GTINTAD	SCFC	—	GTCCRC register compare match source synchronous clear enable bit
	SCFD	—	GTCCRD register compare match source synchronous clear enable bit
	SCFE	—	GTCCRE register compare match source synchronous clear enable bit
	SCFF	—	GTCCRF register compare match source synchronous clear enable bit
	SCFPO	—	Overflow source simultaneous clear enable bit
	SCFPU	—	Underflow source simultaneous clear enable bit
	EINT	Dead time error interrupt enable bit	—
	GRP[1:0]	—	Output stop group select bits
	GRPDTE	—	Dead time error output stop detection enable bit
	GRPABH	—	Simultaneous high output stop detection enable bit
	GRPABL	—	Simultaneous low output stop detection enable bit
	GTINTPC	—	Cycle count end interrupt enable bit
GTCR	—	General purpose PWM timer control register GTCR is a 16-bit register.	General purpose PWM timer control register GTCR is a 32-bit register.
	CST	—	Count start bit
	ICDS	—	Bit for selecting input capture operation at count stop
	SCGTIOC	—	GTIOC input source simultaneous clearing enable bit
	SSCGRP [1:0]	—	Simultaneous setting or clearing group select bits
	CPSCD	—	Bit for disabling simultaneous clearing in complementary PWM mode
	SSCEN	—	Simultaneous setting or resetting enable bit
	MD[2:0] (RX62T) MD[3:0] (RX26T)	Mode select bits b2 b0 0 0 0: Saw-wave PWM mode (single buffer or double buffer possible) 0 0 1: Sawtooth-wave one-shot pulse mode (fixed buffer operation) 0 1 0: Setting prohibited	Mode select bits b19 b16 0 0 0 0: Saw-wave PWM mode 1 (single buffer or double buffer possible) 0 0 0 1: Sawtooth-wave one-shot pulse mode (fixed buffer operation) 0 0 1 0: Saw-wave PWM mode 2 (single buffer or double buffer possible)

Register	Bit	RX62T (GPT/GPTa)	RX26T (GPTWa)
GTCR	MD[2:0] (RX62T) MD[3:0] (RX26T)	0 1 1: Setting prohibited 1 0 0: Triangle-wave PWM mode 1 (16-bit transfer at trough) (single buffer or double buffer possible) 1 0 1: Triangle-wave PWM mode 2 (16-bit transfer at crest and trough) (single buffer or double buffer possible) 1 1 0: Triangle-wave PWM mode 3 (32-bit transfer at trough) (fixed buffer operation) 1 1 1: Setting prohibited	0 0 1 1: Setting prohibited. 0 1 0 0: Saw-wave PWM mode 1 (32-bit transfer at trough) (single buffer or double buffer possible) 0 1 0 1: Triangle-wave PWM mode 2 (32-bit transfer at crest and trough) (single buffer or double buffer possible) 0 1 1 0: Triangle-wave PWM mode 3 (64-bit transfer at trough) (fixed buffer operation) 0 1 1 1: Setting prohibited 1 0 0 0: Setting prohibited 1 0 0 1: Setting prohibited 1 0 1 0: Setting prohibited 1 0 1 1: Setting prohibited 1 1 0 0: Complementary PWM mode 1 (transfer at crest)*1 1 1 0 1: Complementary PWM mode 2 (transfer at trough)*1 1 1 1 1: Complementary PWM mode 3 (transfer at crest/trough)*1 1 1 1 1: Complementary PWM mode 4 (immediate transfer)*1
	TPCS[1:0]	Timer prescaler select bits b9 b8 0 0: ICLK (system clock) 0 1: ICLK/2 (system clock/2) 1 0: ICLK/4 (system clock/4) 1 1: ICLK/8 (system clock/8)	Timer prescaler select bits b26 b23 0 0 0 0: PCLKC 0 0 0 1: PCLKC/2 0 0 1 0: PCLKC/4 0 0 1 1: PCLKC/8 0 1 0 0: PCLKC/16 0 1 0 1: PCLKC/32 0 1 1 0: PCLKC/64 0 1 1 1: PCLKC/128 1 0 0 0: PCLKC/256 1 0 0 1: PCLKC/512 1 0 1 0: PCLKC/1024 1 0 1 1: Setting prohibited 1 1 0 0: GTETRGA (via the POEG) 1 1 0 1: GTETRGB (via the POEG) 1 1 1 0: GTETRGC (via the POEG) 1 1 1 1: GTETRGD (via the POEG)
	CCLR[1:0]	Counter clear source select bits	—
	CKEG[1:0]	—	Clock edge select bits

Register	Bit	RX62T (GPT/GPTa)	RX26T (GPTWa)
GTBER	—	General purpose PWM timer buffer enable register GTBER is a 16-bit register.	General purpose PWM timer buffer enable register GTBER is a 32-bit register.
	BD[0]	—	GTCCRA/GTCCRB registers buffer operation disable bit
	BD[1]	—	GTPR register buffer operation disable bit
	BD[2]	—	GTADTRA/GTADTRB register buffer operation disable bit
	BD[3]	—	GTDVU/GTDVD registers buffer operation disable bit
	DBRTECA	—	GTCCRA register double buffer repeat operation enable bit
	DBRTSCA	—	Bit for selecting the repeat operation period for the GTCCRA register double buffer
	DBRTECB	—	GTCCRB register double buffer repeat operation enable bit
	DBRTSCB	—	Bit for selecting the repeat operation period for the GTCCRB register double buffer
	DBRTEADA	—	Bit for enabling repeat operation of the GTADTRA register double buffer
	DBRTSADA	—	Bit for selecting the repeat period for the GTADTRA register double buffer
	DBRTEADB	—	Bit for enabling repeat operation of the GTADTRB register double buffer
	DBRTSADB	—	Bit for selecting the repeat period for the GTADTRB register double buffer
	CCRA[1:0]	GTCCRA buffer operation bits (b1-b0)	GTCCRA buffer operation bits (b17-b16)
	CCRB[1:0]	GTCCRB buffer operation bits (b3-b2)	GTCCRB buffer operation bits (b19-b18)
	PR[1:0]	GTPR buffer operation bits (b5-b4)	GTPR buffer operation bits (b21-b20)
	CCRSWT	GTCCRA and GTCCRB forcible buffer operation bit (b6)	GTCCRA and GTCCRB forcible buffer operation bit (b22)
	ADTTA[1:0]	GTADTRA buffer transfer timing select bits (b7)	GTADTRA buffer transfer timing select bits (b23)
	ADTDA	GTADTRA double buffer operation bit (b10)	GTADTRA double buffer operation bit (b26)
	ADTTB[1:0]	GTADTRB buffer transfer timing select bits (b13-b12)	GTADTRB buffer transfer timing select bits (b29- b28)
	ADTDB	GTADTRB double buffer operation bit (b14)	GTADTRB double buffer operation bit (b30)
GTUDC	—	General purpose PWM timer count direction register	—
GTITC	—	General purpose PWM timer interrupt and A/D converter start request skipping setting register GTITC is a 16-bit register.	General purpose PWM timer interrupt and A/D converter start request skipping setting register GTITC is a 32-bit register.

Register	Bit	RX62T (GPT/GPTa)	RX26T (GPTWa)
GTST	—	General purpose PWM timer status register GTST is a 16-bit register.	General purpose PWM timer status register GTST is a 32-bit register.
	ADTRAUF	—	GTADTRA register compare match (up-counting) A/D conversion start request flag
	ADTRADF	—	GTADTRA register compare match (down-counting) A/D conversion start request flag
	ADTRBUF	—	GTADTRB register compare match (up-counting) A/D conversion start request flag
	ADTRBDF	—	GTADTRB register compare match (down-counting) A/D conversion start request flag
	ODF	—	Output stop request flag
	DTEF	Dead time error flag (b11)	Dead time error flag (b28)
	TUCF	Count direction flag	—
	OABHF	—	Simultaneous high output flag
	OABLF	—	Simultaneous low output flag
	PCF	—	Cycle count end flag
GTCNT	—	General purpose PWM timer counter GTCNT is a 16-bit register.	General purpose PWM timer counter GTCNT is a 32-bit register.
GTCCRm	—	General purpose PWM timer compare capture register m (m = A to F) GTCCRm is a 16-bit register.	General purpose PWM timer compare capture register m (m = A to F) GTCCRm is a 32-bit register.
GTPR	—	General purpose PWM timer cycle setting register GTPR is a 16-bit register.	General purpose PWM timer cycle setting register GTPR is a 32-bit register.
GTPBR	—	General purpose PWM timer cycle setting buffer register GTPBR is a 16-bit register.	General purpose PWM timer cycle setting buffer register GTPBR is a 32-bit register.
GTPDBR	—	General purpose PWM timer cycle setting double-buffer register GTPDBR is a 16-bit register.	General purpose PWM timer cycle setting double-buffer register GTPBR is a 32-bit register.
GTADTRm	—	A/D converter start request timing register m (m = A to B) GTADTRm is a 16-bit register.	A/D converter start request timing register m (m = A to B) GTADTRm is a 32-bit register.
GTADTBRm	—	A/D converter start request timing buffer register m (m = A to B) GTADTBRm is a 16-bit register.	A/D converter start request timing buffer register m (m = A to B) GTADTRm is a 32-bit register.
GTADTDBRm	—	A/D converter start request timing double buffer register m GTADTDBRm is a 16-bit register.	A/D converter start request timing double buffer register m GTADTDBRm is a 32-bit register.
GTONCR	—	General purpose PWM timer output negate control register	—
GTDTCR	—	Dead time control register GTDTCR is a 16-bit register.	Dead time control register GTDTCR is a 32-bit register.
GTDVm	—	General purpose PWM timer dead time value register m (m = U, D) GTDVm is a 16-bit register.	General purpose PWM timer dead time value register m (m = U, D) GTDVm is a 32-bit register.

Register	Bit	RX62T (GPT/GPTa)	RX26T (GPTWa)
GTDBm	—	General purpose PWM timer dead time buffer register m (m = U, D) GTDBm is a 16-bit register.	General purpose PWM timer dead time buffer register m (m = U, D) GTDBm is a 32-bit register.
GTSOS	—	General purpose PWM timer output protection function status register GTSOS is a 16-bit register.	General purpose PWM timer output protection function status register GTSOS is a 32-bit register.
GTSOTR	—	General purpose PWM timer output protection function temporary release register GTSOTR is a 16-bit register.	General purpose PWM timer output protection function temporary release register GTSOTR is a 32-bit register.
GTDLYCR	—	PWM output delay control register	—
GTDLYRA	—	GTIOCA rising output delay register	—
GTDLYFA	—	GTIOCA falling output delay register	—
GTDLYRB	—	GTIOCB rising output delay register	—
GTDLYFB	—	GTIOCB falling output delay register	—
GTCLR	—	—	General purpose PWM timer software clear register
GTSSR	—	—	General purpose PWM timer start source select register
GTPSR	—	—	General purpose PWM timer stop source select register
GTCSR	—	—	General purpose PWM timer clear source select register
GTUPSR	—	—	General purpose PWM timer count-up source select register
GTDNSR	—	—	General purpose PWM timer count-down source select register
GTICASR	—	—	General purpose PWM timer input capture source select register A
GTICBSR	—	—	General purpose PWM timer input capture source select register B
GTUDDTYC	—	—	General purpose PWM timer count direction and duty setting register
GTIOR	—	—	General purpose PWM timer I/O control register
GTADSMR	—	—	General purpose PWM timer A/D converter start request signal monitor register
GTEITC	—	—	General purpose PWM timer extended interrupt skipping counter control register
GTEITLI1	—	—	General purpose PWM timer extended interrupt skipping setting register 1
GTEITLI2	—	—	General purpose PWM timer extended interrupt skipping setting register 2
GTEITLB	—	—	General purpose PWM timer extended buffer transfer skipping setting register
GTICLF	—	—	Register for logical operations between general purpose PWM timer channels

Register	Bit	RX62T (GPT/GPTa)	RX26T (GPTWa)
GTPC	—	—	General purpose PWM timer cycle count register
GTADCMSC	—	—	General purpose PWM timer A/D conversion start request compare match skipping control register
GTADCMSS	—	—	General purpose PWM timer A/D conversion start request compare match skipping setting register
GTSECSR	—	—	General purpose PWM timer operation enable bit simultaneous control channel select register
GTSECR	—	—	General purpose PWM timer operation enable bit simultaneous control register
GTBER2	—	—	General purpose PWM timer buffer enable register 2
GTOLBR	—	—	General purpose PWM timer output level buffer register
GTICCR	—	—	Input capture control register for linkage between general purpose PWM timer channels
OPSCR	—	—	Output phase switch control register

Note: 1. Do not set it for GPTW3 or GPTW7.

2.17 Compare Match Timer

Table 2.35 is Comparative Overview of Compare Match Timers.

Table 2.35 Comparative Overview of Compare Match Timers

Item	RX62T (CMT)	RX26T (CMT)
Count clocks	• Four frequency dividing clocks: One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.	• Four frequency dividing clocks: One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.
Interrupts	A compare match interrupt can be requested for each channel.	A compare match interrupt can be requested for each channel.
Event link function (output)	—	An event signal is output upon a CMT1 compare match.
Event link function (input)	—	• Linking to the specified module is possible. • CMT1 count start, event counter, or count restart operation is possible.
Low power consumption function	Ability to transition each unit to the module stop state	Ability to transition each unit to the module stop state

2.18 Watchdog Timer

Table 2.36 is Comparative Overview of Watchdog Timers, and Table 2.37 is Comparison of Watchdog Timer Registers.

Table 2.36 Comparative Overview of Watchdog Timers

Item	RX62T (WDT)	RX26T (WDTA)
Count source	Peripheral module clock (PCLK)	Peripheral module clock (PCLK)
Clock frequency division ratio	PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192, PCLK/32768, PCLK/131072	Divided by 4, 64, 128, 512, 2048, or 8192
Counter operation	Counting up using a 8-bit timer	Counting down using a 14-bit down-counter
Operating mode	Switching between the watch dog timer mode and the interval timer mode	—
Conditions for starting the counter	• The TCSR.TME bit is set to 1. (The TCNT counter starts counting.)	• Auto-start mode: Counting starts automatically after a reset. • Register start mode: Counting is started by refreshing the counter (writing 00h and then FFh to the WDTRR register).
Conditions for stopping the counter	• The TCSR.TME bit is set to 1. (The TCNT counter stops counting and initialized to "00h".)	• Resets • Low power consumption state • Underflow or refresh error (register start mode only)
Window function	—	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods).
Watchdog timer reset issuance sources	• The WDTOVF# signal is output when the counter overflows. Whether or not to reset LSI at that time can be selected.	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt and interrupt sources	—	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	The counter value can be read by reading TCNT.	The down-counter value can be read by reading the WDTSR register.
Interval timer mode	An interval timer interrupt (WOVI) is generated when the counter overflows.	—

Table 2.37 Comparison of Watchdog Timer Registers

Register	Bit	RX62T (WDT)	RX26T (WDTA)
TCNT	—	Timer counter	—
TCSR	—	Timer control/status register	—
RSTCSR	—	Reset control/status register	—
WINA	—	Write window A register	—
WINB	—	Write window B register	—
WDTRR	—	—	WDT refresh register
WDTCR	—	—	WDT control register
WDTSR	—	—	WDT status register
WDTRCR	—	—	WDT reset control register
OFS0	—	—	Option function select register 0

2.19 Independent Watchdog Timer

Table 2.38 is Comparative Overview of Watchdog Timers, and Table 2.39 is Comparison of Independent Watchdog Timer Registers.

Table 2.38 Comparative Overview of Watchdog Timers

Item	RX62T (IWDT)	RX26T (IWDTa)
Count source	IWDT-dedicated clock (IWDTCLK)	IWDT-dedicated clock (IWDTCLK)
Clock division ratio	Divide by 1, 16, 32, 64, 128, or 256	Divide by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Counting starts when the down-counter is refreshed (writing 00h and then FFh to the IWDTRR register).	• Auto-start mode: Counting starts automatically after a reset. • Register start mode: Counting is started by refreshing the counter (writing 00h and then FFh to the IWDTRR register).
Conditions for stopping the counter	• Reset (The down-counter and other registers return to their initial values.) • At underflow	• Resets • Low power consumption state (by means of register setting) • Underflow or refresh error (register start mode only)
Window function	—	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods).
Reset output sources	• Down-counter underflows	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt and interrupt sources	—	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read by reading the IWDTSR register.	The down-counter value can be read by reading the IWDTSR register.
Event link function (output)	—	• Down-counter underflow event output • Refresh error event output
Output signals (internal signals)	—	• Reset output • Interrupt request output • Sleep mode count stop control output

Item	RX62T (IWDT)	RX26T (IWDTa)
Auto-start mode (controlled by option function select register 0 (OFS0))	—	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0]bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at a transition to sleep mode, software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)
Register start mode (controlled by the IWDT registers)	—	• Selecting the clock frequency division ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at a transition to sleep mode, software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)

Table 2.39 Comparison of Independent Watchdog Timer Registers

Register	Bit	RX62T (IWDT)	RX26T (IWDTa)
IWDTCR	CKS[3:0]	Clock select bits b7 b4 0 0 – –: IWDTCLK 0 1 0 0: IWDTCLK/16 0 1 0 1: IWDTCLK/32 0 1 1 0: IWDTCLK/64 0 1 1 1: IWDTCLK/128 1 – – –: IWDTCLK/256	Clock select bits b7 b4 0 0 0 0: no division 0 0 1 0: divided by 16 0 0 1 1: divided by 32 0 1 0 0: divided by 64 0 1 0 1: divided by 256 1 1 1 1: divided by 128 Settings other than the above are prohibited.
	RPES[1:0]	—	Window end position select bits
	RPSS[1:0]	—	Window start position select bits
IWDTSR	REFEF	—	Refresh error flag
IWDTRCR	—	—	IWDT reset control register
IWDTCSTPR	—	—	IWDT count stop control register
OFS0	—	—	Option function select register 0

2.20 Serial Communications Interface

Table 2.40 is Comparative Overview of Serial Communications Interfaces, Table 2.41 is Comparison of Serial Communications Interface Channel Specifications, and Table 2.42 is Comparison of Serial Communications Interface Registers.

Table 2.40 Comparative Overview of Serial Communications Interfaces

Item		RX62T (SCIb)	RX26T (SCIk, SCIh)
Number of channels		• SCIb: 3 channels	• SCIk: 3 channels • SCIh: 1 channel
Serial communications modes		• Asynchronous • Clock synchronous • Smart card interface	• Asynchronous • Clock synchronous • Smart card interface • Simple I^2C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator	Bit rate specifiable by on-chip baud rate generator
Full-duplex communication		• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable as LSB first or MSB first transfer	Selectable as LSB first or MSB first transfer
I/O signal level inversion		—	The levels of input and output signals can be inverted independently (SCI1, SCI5, SCI6).
RXD input signal select function (available only for SCI5)			When the RXD signal weakens by the impact of the transmission line, it can be improved by using the comparator as the receiver.
Interrupt sources		• Transmit end, transmit data empty, receive data full, and receive error	• Transmit end, transmit data empty, receive data full, and receive error, and data match (SCI1, SCI5, SCI6) • Completion of generation of a start condition, restart condition, or stop condition (for simple I^2C mode)
Low power consumption function		Transition to the module stop state is possible for each channel.	Transition to the module stop state is possible for each channel.
Asynchronous mode	Data length	7 or 8 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection function	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	—	CTSn# and RTSn# pins can be used in controlling transmission and reception.
	Data match detection	—	Compares the received data and the comparison data register, and generates an interrupt request when they match (SCI1, SCI5, SCI6).
	Start-bit detection	Low level or falling edge is selectable.	Low level or falling edge is selectable.

Item		RX62T (SCIb)	RX26T (SCIk, SCIh)
Asynchronous mode	Receive data sampling timing adjustment	—	The receive data sampling point can be shifted from the center of the data forward or backward to a base point (SCI1, SCI5, SCI6).
	Transmit signal change timing adjustment	—	Either the falling or rising edge of the transmit data can be delayed (SCI1, SCI5, SCI6).
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn (n = 0 to 2) pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly or by reading the SPTR.RXDMON flag (SCI5, SCI6).
	Clock source	• An internal or external clock can be selected.	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5, SCI6, SCI12).
	Double-speed mode	—	Baud rate generator double-speed mode can be selected.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	Noise can be eliminated from the input to the RXDn (n = 0 to 2) pin.	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	—	CTSn# and RTSn# pins can be used in controlling transmission and reception.
Smart card interface mode	Error processing	• An error signal can be automatically transmitted when a parity error is detected during reception. • Data can be automatically retransmitted when an error signal is received during transmission.	• An error signal can be automatically transmitted when a parity error is detected during reception. • Data can be automatically retransmitted when an error signal is received during transmission.
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	—	I^2C bus format
	Operating mode	—	Master (single-master operation only)
	Transfer speed	—	Fast mode is supported.
	Noise cancellation	—	• The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters. • The interval for noise cancellation is adjustable.
Simple SPI mode	Data length	—	8 bits
	Detection of errors	—	Overrun error
	SS input pin function	—	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	—	Four kinds of settings for clock phase and clock polarity are selectable.

Item		RX62T (SCIb)	RX26T (SCIk, SCIh)
Extended serial mode (supported by SCI12 only)	Start frame transmission	—	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection
	Start frame reception	—	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Two kinds of data for comparison (primary and secondary) can be set in control field 1. • A priority interrupt bit can be set in control field 1. • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates
	I/O control function	—	• Ability to select polarity or TXDX12 and RXDX12 signals • Digital filtering can be specified for the RXDX12 signal. • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Receive data sampling timing of RXDX12 pin can be selected.
	Timer function	—	Usable as reloading timer
Bit rate modulation function		—	Correction of outputs from the on-chip baud rate generator can reduce errors.
Event link function (supported by SCI5 only)		—	• Error (receive error or error signal detection) event output • Receive buffer full event output • Transmit data empty event output • Transmit end event output

Table 2.41 Comparison of Serial Communications Interface Channel Specifications

Item	RX62T (SCIg)	RX26T (SCIk, SCIh)
Asynchronous mode	SCI0, SCI1, SCI2	SCI1, SCI5, SCI6, SCI12
Clock synchronous mode	SCI0, SCI1, SCI2	SCI1, SCI5, SCI6, SCI12
Smart card interface mode	SCI0, SCI1, SCI2	SCI1, SCI5, SCI6, SCI12
Simple I²C mode	—	SCI1, SCI5, SCI6, SCI12
Simple SPI mode	—	SCI1, SCI5, SCI6, SCI12
Data match detection	—	SCI1, SCI5, SCI6
Extended serial mode	—	SCI12
TMR clock input	—	SCI5, SCI6, SCI12
Event link function	—	SCI5
Peripheral module clock	PCLK: SCI0, SCI1, SCI2	PCLKB: SCI1, SCI5, SCI6, SCI12

Table 2.42 Comparison of Serial Communications Interface Registers

Register	Bit	RX62T (SCIg)	RX26T (SCIk, SCIh)
RDRH, RDRL, RDRHL	—	—	Data register H, L, and HL
TDRH, TDRL, TDRHL	—	—	Transmit data register H, L, and HL
SMR	CHR	Character length bit (Valid only in asynchronous mode) 0: Sending/Receiving 8-bit data*1 1: Sending/Receiving 7-bit data*2	Character length bit (Valid only in asynchronous mode*1) Selection is made also using the SCMR.CHR1 bit. CHR1 CHR 0 0: Sending/Receiving 9-bit data 0 1: Sending/Receiving 9-bit data 1 0: Sending/Receiving 8-bit data (initial value) 1 1: Sending/Receiving 7-bit data*2
	CM	Communication mode bit 0: Operating in asynchronous mode 1: Operating in clock synchronous mode	Communication mode bit 0: Operating in asynchronous mode or simple I²C mode 1: Operating in clock synchronous mode or simple SPI mode

Register	Bit	RX62T (SCIg)	RX26T (SCIk, SCIh)
SCR	CKE[1:0]	Serial control register For asynchronous mode b1 b0 0 0: On-chip baud rate generator The SCKn pin can be used as input/output port. 0 1: On-chip baud rate generator Clock of the frequency of the bit rate is output from the SCKn pin. 1 0: External clock Input a clock of the frequency of 16 times the bit rate from the SCKn pin. Input a clock of the frequency of 8 times the bit rate when the SEMR.ABCS bit is "1". 1 1: External clock Input a clock of the frequency of 16 times the bit rate from the SCKn pin. Input a clock of the frequency of 8 times the bit rate when the SEMR.ABCS bit is "1". For clock synchronous mode b1 b0 0 0: Internal clock input The SCKn pin is a clock output pin. 0 1: Internal clock input The SCKn pin is a clock output pin. 1 0: External clock input The SCKn pin is a clock input pin. 1 1: External clock input The SCKn pin is a clock input pin.	Serial control register (For asynchronous mode) b1 b0 0 0: On-chip baud rate generator The SCKn pin is high-impedance. 0 1: On-chip baud rate generator Clock of the frequency of the bit rate is output from the SCKn pin. 1 x: External clock or TMR clock When an external clock is used, input a clock of the frequency of 16 times the bit rate from the SCKn pin. Input a clock of the frequency of 8 times the bit rate when the SEMR.ABCS bit is "1". The SCKn pin is high-impedance when the TMR clock is used. (For clock synchronous mode) b1 b0 0 x: Internal clock The SCKn pin is a clock output pin. 1 x: External clock The SCKn pin is a clock input pin.
MDDR	—	—	Modulation duty register
SEMR	ACS0	—	Asynchronous mode clock source select bit
	ITE	—	Immediate transmission enable bit
	BRME	—	Bit rate modulation enable bit
	ABCSE	—	Asynchronous mode base clock select extended bit*3
	BGDM	—	Baud rate generator double-speed mode select bit

Register	Bit	RX62T (SCIg)	RX26T (SCIk, SCIh)
SEMR	NFEN	Noise elimination function select bit (Valid only in asynchronous mode) 0: The noise elimination function for RXDn pin input is disabled. 1: The noise elimination function for RXDn pin input is enabled.	Digital noise filter function enable bit (Asynchronous mode) 0: The noise elimination function for RXDn input signal is disabled. 1: The noise elimination function for RXDn input signal is enabled. (Simple I2C mode) 0: The noise elimination function for the input signals of SSCLn and SSDAn is disabled. 1: The noise elimination function for the input signals of SSCLn and SSDAn is enabled. Set the NFEN bit to "0" for other modes.
CDR	—	—	Comparison data register
DCCR	—	—	Data comparison control register
SPTR	—	—	Serial port register
TMGR	—	—	Transmit/receive timing select register
ESMER	—	—	Extended serial mode enable register
CR0	—	—	Control register 0
CR1	—	—	Control register 1
CR2	—	—	Control register 2
CR3	—	—	Control register 3
PCR	—	—	Port control register
ICR	—	—	Interrupt control register
STR	—	—	Status register
STCR	—	—	Status clear register
CF0DR	—	—	Control Field 0 data register
CF0CR	—	—	Control Field 0 compare enable register
CF0RR	—	—	Control Field 0 receive data register
PCF1DR	—	—	Primary Control Field 1 data register
SCF1DR	—	—	Secondary Control Field 1 data register
CF1CR	—	—	Control Field 1 compare enable register
CF1RR	—	—	Control Field 1 receive data register
TCR	—	—	Timer control register
TMR	—	—	Timer mode register
TPRE	—	—	Timer prescaler register
TCNT	—	—	Timer count register

Notes: 1. In clock synchronous mode, the data length is always 8 bits regardless of the setting.
2. The bit order is always LSB first, and the MSB (b7) of the TDR register is not sent.
3. It is a reserved bit for SCI12. This bit is read as 0. The write value should be 0.

2.21 I²C Bus Interface

Table 2.43 is Comparative Overview of I²C Bus Interfaces, and Table 2.44 is Comparison of I²C Bus Interface Registers.

Table 2.43 Comparative Overview of I²C Bus Interfaces

Item	RX62T (RIIC)	RX26T (RIICa)
Communication format	• I²C-bus format or SMBus format • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate	• I²C-bus format or SMBus format • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate
Transfer rate	Up to 400 kbps	Fast-mode is supported (up to 400 kbps)
SCL clock	For master operation, the duty cycle of the SCL clock is selectable in the range from 4 to 96%.	For master operation, the duty cycle of the SCL clock is selectable in the range from 4 to 96%.
Issuing and detecting conditions	Start, restart, and stop conditions are automatically generated. Start conditions (including restart conditions) and stop conditions are detectable.	Start, restart, and stop conditions are automatically generated. Start conditions (including restart conditions) and stop conditions are detectable.
Slave address	• Up to three sets of slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.
Acknowledgment	• For transmission, the acknowledge bit is automatically loaded. — Transfer of the next data for transmission can be automatically suspended on detection of a no-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. — If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.	• For transmission, the acknowledge bit is automatically loaded. — Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. — If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.
Wait function	• In reception, the following periods of waiting can be obtained by holding the SCL clock at the low level. — Waiting between the eighth and ninth clock cycles — Waiting between the ninth clock cycle and the first clock cycle of the next transfer (WAIT function)	• In reception, the following periods of waiting can be obtained by holding the SCL line at the low level. — Waiting between the eighth and ninth clock cycles — Waiting between the ninth clock cycle and the first clock cycle of the next transfer
SDA output delay function	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.	Change timing of the output of transmitted data, including the acknowledge bit, can be delayed.

Item	RX62T (RIIC)	RX26T (RIICa)
Arbitration	• For multi-master operation — Operation to synchronize the SCL clock in cases of conflict with the SCL signal from another master is possible. — When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • When transmitting a no-acknowledge bit, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. • Loss of arbitration due to non-matching of internal and line levels for data is detectable in slave transmission.	• For multi-master operation — Operation to synchronize the SCL in cases of conflict with the SCL signal from another master is possible. — When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • When transmitting a not-acknowledge bit, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. • Loss of arbitration due to non-matching of internal and line levels for data is detectable in slave transmission.
Timeout function	The internal timeout function is capable of detecting long-interval stop of the SCL clock.	The internal timeout function is capable of detecting long-interval stop of the SCL.
Noise cancellation	The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable by programming.	The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable by software.
Interrupt sources	• 4 sources — Error in transfer or occurrence of events (Detection of AL, NACK, timeout, a start condition (including a restart condition), or a stop condition) — Receive data full (including matching with a slave address) — Transmit data empty (including matching with a slave address) — Transmit end	• 4 sources — Error in transfer or occurrence of events Detection of arbitration lost, NACK, timeout, a start condition including a restart condition, or a stop condition — Receive data full (including matching with a slave address) — Transmit data empty (including matching with a slave address) — Transmit end
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Item	RX62T (RIIC)	RX26T (RIICa)
RIIC operating modes	—	• 4 sources — Master transmit mode — Master receive mode — Slave transmit mode — Slave receive mode
Event link function (output)	—	• Four sources (RIIC0): — Error in transfer or occurrence of events Detection of arbitration lost, NACK, timeout, a start condition including a restart condition, or a stop condition — Receive data full (including matching with a slave address) — Transmit data empty (including matching with a slave address) — Transmit end

Table 2.44 Comparison of I²C Bus Interface Registers

Register	Bit	RX62T (RIIC)	RX26T (RIICa)
ICMR2	TMWE	Timeout internal counter write enable bit	—
ICIER	RIE	Receive data full interrupt enable bit 0: Receive data full interrupt (ICRXI) disabled 1: Receive data full interrupt (ICRXI) enabled	Receive data full interrupt request enable bit 0: Receive data full interrupt (RXI) request disabled 1: Receive data full interrupt (RXI) request enabled
	TEIE	Transmit end interrupt enable bit 0: Transmit end interrupt (ICTEI) disabled 1: Transmit end interrupt (ICTEI) enabled	Transmit end interrupt request enable bit 0: Transmit end interrupt (TEI) request disabled 1: Transmit end interrupt (TEI) request enabled
	TIE	Transmit data empty interrupt enable bit 0: Transmit data empty interrupt (ICTXI) disabled 1: Transmit data empty interrupt (ICTXI) enabled	Transmit data empty interrupt enable bit 0: Transmit data empty interrupt (TXI) request disabled 1: Transmit data empty interrupt (TXI) request enabled
TMOCNT	—	Timeout internal counter	—

2.22 CAN Module and CAN FD Module

Table 2.45 is Comparative Overview of CAN Module and CAN FD Module, and Table 2.46 is Comparison of CAN Module Registers and CAN FD Module Registers.

Table 2.45 Comparative Overview of CAN Module and CAN FD Module

Item	RX62T (CAN)	RX26T (CANFD)
Protocol	Conforming to the ISO 11898-1 standard (standard frame or extension frame)	Conforming to the ISO 11898-1:2015 specifications
Bit rate (RX62T) Data transfer rate (RX26T)	Programming is possible with a maximum bit rate of 1 Mbps (fCAN is equal to or larger than 8 MHz). fCAN: CAN clock source	Arbitration phase: Maximum of 1 Mbps Data phase: Maximum 8 Mbps*1
Operating frequency	PCLKB: 60 MHz (max.)	Register block: Maximum of 60 MHz (PCLKB) Message buffer RAM: Maximum of 120 MHz (PCLKA)
Operating clock (DLL clock) for data link layer	—	Maximum of 60 MHz (either CANFDMCLK or CANFDCLK can be selected)
Message box (RX62T) Message buffer (RX26T)	32 mailboxes: Two mailbox modes can be selected. • Normal mailbox mode: 32 mailboxes can be configured for transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for transmission or reception. Of the other mailboxes, four FIFO stages can be configured for transmission and four FIFO stages for reception.	• 32 receive message buffers • Four transmit message buffers • One transmit queue Automatic transfer of messages to the transmit queue is supported.
Frame type	• Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID) • Remote frame in base format (11-bit ID) • Remote frame in extended format (29-bit ID)	Classic CAN (CAN 2.0) • Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID) • Remote frame in base format (11-bit ID) • Remote frame in extended format (29-bit ID) CAN FD*1 • Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID)
Reception	• Data frames and remote frames can be received. • The ID format to be received (base ID only, extended ID only, or both base ID and extended ID) can be selected. • The one-shot receive function can be selected. • Overwrite mode (message is overwritten) or overrun mode (message is discarded) can be selected. • Reception end interrupt can be enabled or disabled individually for each mailbox.	• Data frames and remote frames can be received. • The ID format to be received (base ID only, extended ID only, or both base ID and extended ID) can be selected. • Receive message buffer interrupt can be enabled or disabled individually for each message buffer.
Data length	0 to 8 bytes	Classic CAN: 0 to 8 bytes CAN FD: 0 to 8, 12, 16, 20, 24, 32, 48, and 64 bytes*1

Item	RX62T (CAN)	RX26T (CANFD)
Acceptance filter	• Eight acceptance masks (an individual mask for every four mailboxes) • Mailbox masks can be enabled or disabled individually.	Filtering is possible in the following fields: • IDE bit (base format, extended format, or both) • ID field • RTR bit (data frame or remote frame) (only for Classic CAN) • DLC field Data (data length) The protection function when the payload size is exceeded is provided. Acceptance filter list (AFL) entries can be updated during communication.
Transmission	• Data frames and remote frames can be sent. • The ID format to be sent (base ID only, extended ID only, or both base ID and extended ID) can be selected. • The one-shot transmission function can be selected. • Either ID priority transmission mode or mailbox number priority transmission mode can be selected. • Transmission requests can be aborted (completion of abort can be confirmed with a flag). • Transmission end interrupt can be enabled or disabled individually for each mailbox.	• Data frames and remote frames can be sent. • The ID format to be sent (base ID only or extended ID only) can be selected. • The one-shot transmission function can be selected. • Either ID priority transmission mode or message buffer number priority transmission mode can be selected. • Transmission requests can be aborted (completion of abort can be confirmed with a flag). • Channel transmission interrupt can be enabled and disabled.
FIFO	• 24 mailboxes can be configured for transmission or reception. • Of the other mailboxes, four FIFO stages can be configured for transmission and four FIFO stages for reception.	The FIFO size is programmable. • Two receive FIFOs • One common FIFO (Whether to use the FIFO as a receive FIFO or transmit FIFO can be selected.)
Automatic transmission interval adjustment	—	Available when the common FIFO is configured as a transmit FIFO The interval between messages sent from the FIFO can be adjusted.
Bus-off recovery method	How to recover from the bus-off state can be selected. • Conforming to the ISO 11898-1 standard • The mode automatically changes to CAN Halt mode when bus off starts. • The mode automatically changes to CAN Halt mode when bus off ends. • A program causes a transition to CAN Halt mode. • A program causes a transition to error active state.	How to recover from the bus-off state can be selected. • Normal mode (ISO 11898-1 compliant) • Automatically enters CH_HALT mode when bus off starts. • Automatically enters CH_HALT mode when bus off ends. • Software causes a transition CH_HALT mode (during bus-off recovery period). • A program causes a transition to error active state.
Timestamp function	• Timestamp function with a 16-bit counter • The reference clock can be selected from 1, 2, 4, and 8 bit time.	Transmission and reception timestamp function
Interrupt function	• Five types of interrupt sources (reception end interrupt, transmission end interrupt, receive FIFO interrupt, transmit FIFO interrupt, and error interrupt)	Receive FIFO interrupt Global error interrupt Channel transmission interrupt Channel error interrupt Common FIFO reception interrupt Receive message buffer interrupt
CAN sleep mode	Current consumption can be reduced by stopping the CAN clock.	Module start/stop function for each CAN node (CH_SLEEP mode and GL_SLEEP mode)

Item	RX62T (CAN)	RX26T (CANFD)
Error status monitoring	• CAN bus errors (stack error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored. • Change of the error status can be detected (error warning, error passive, bus-off start, and bus-off recovery). • The error counter can be read.	—
Software support	—	Label information is automatically added to received messages.
Software support units	Three software support unis • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support	—
Test modes	Three test modes are provided for user evaluation: • Listen-only mode • Self test mode 0 (external loopback) • Self test mode 1 (internal loopback)	• Basic test mode • Listen-only mode • Self test mode 0 (external loopback mode) • Self test mode 1 (internal loopback mode)
Power down function	—	Module start/stop function for each CAN node (CH_SLEEP mode and GL_SLEEP mode) Ability to transition to module stop state
RAM	—	RAM with ECC protection

Note: 1. This is only available for products that support the CAN FD protocol.

Table 2.46 Comparison of CAN Module Registers and CAN FD Module Registers

Register	Bit	RX62T (CAN)	RX26T (CANFD)
CTLR	—	Control register	—
BCR	—	Bit configuration register	—
MKRk	—	Mask register k (k = 0 to 7)	—
FIDCR0 FIDCR1	—	FIFO receive ID comparison registers 0 and 1	—
MKIVLR	—	Mask disable register	—
MBj	—	Mailbox register j (j = 0 to 31)	—
MIER	—	Mailbox interrupt enable register	—
MCTLj	—	Message control register j (j = 0 to 31)	—
RFCR	—	Receive FIFO control register	—
RFPCR	—	Receive FIFO pointer control register	—
TFCR	—	Transmit FIFO control register	—
TFPCR	—	Transmit FIFO pointer control register	—
STR	—	Status register	—
MSMR	—	Mailbox search mode register	—
MSSR	—	Mailbox search status register	—
CSSR	—	Channel search support register	—
AFSR	—	Acceptance filter support register	—
EIER	—	Error interrupt enable register	—
EIFR	—	Error interrupt source decision register	—
RECR	—	Receive error count register	—
TECR	—	Transmit error count register	—

Register	Bit	RX62T (CAN)	RX26T (CANFD)
ECSR	—	Error code storage register	—
TSR	—	Timestamp register	—
TCR	—	Test control register	—
NBCR	—	—	Nominal bit rate configuration register
CHCR	—	—	Channel control register
CHSR	—	—	Channel status register
CHESR	—	—	Channel error status register
DBCR	—	—	Data bit rate configuration register
FDCFG	—	—	CAN FD configuration register
FDCTR	—	—	CAN FD control register
FDSTS	—	—	CAN FD status register
FDCRC	—	—	CAN FD CRC register
GCFG	—	—	Global configuration register
GCR	—	—	Global control register
GSR	—	—	Global status register
GESR	—	—	Global error status register
TISR	—	—	Transmit interrupt status register
TSCR	—	—	Timestamp counter register
AFCR	—	—	Acceptance filter list control register
AFCFG	—	—	Acceptance filter list configuration register
AFLn.IDR	—	—	Acceptance filter list n ID register (n = 0 to 15)
AFLn.MASK	—	—	Acceptance filter list n mask register (n = 0 to 15)
AFLn.PTR0	—	—	Acceptance filter list n pointer register 0 (n = 0 to 15)
AFLn.PTR1	—	—	Acceptance filter list n pointer register 1 (n = 0 to 15)
RMCR	—	—	Receive message buffer configuration register
RMNDR	—	—	Receive message buffer new data register
RFCRn	—	—	Receive FIFO n configuration register (n = 0, 1)
RFSRn	—	—	Receive FIFO n status register (n = 0, 1)
RFPCRn	—	—	Receive FIFO n pointer control register (n = 0, 1)
CFCR0	—	—	Common FIFO 0 configuration register
CFSR0	—	—	Common FIFO 0 status register
CFPCR0	—	—	Common FIFO 0 pointer control register
FESR	—	—	FIFO empty status register
FFSR	—	—	FIFO full status register
FMLSR	—	—	FIFO message lost status register
RFISR	—	—	Receive FIFO interrupt status register
DTCR	—	—	DMA transfer control register
DTSR	—	—	DMA transfer status register

Register	Bit	RX62T (CAN)	RX26T (CANFD)
TMCRn	—	—	Transmit message buffer n control register (n = 0 to 3)
TMSRn	—	—	Transmit message buffer n status register (n = 0 to 3)
TMTRSR0	—	—	Transmit message buffer transmission request status register 0
TMARSR0	—	—	Transmit message buffer transmission abort request status register 0
TMTCSR0	—	—	Transmit message buffer transmission completion status register 0
TMTASR0	—	—	Transmit message buffer transmission abort status register 0
TMIER0	—	—	transmission message buffer interrupt enable register 0
TQCR0	—	—	Transmit queue 0 configuration register
TQSR0	—	—	Transmit queue 0 status register
TQPCR0	—	—	Transmit queue 0 pointer control register
THCR	—	—	Transmission history configuration register
THSR	—	—	Transmission history status register
THACR0	—	—	Transmission history access register 0
THACR1	—	—	Transmission history access register 1
THPCR	—	—	Transmission history pointer control register
GRCR	—	—	Global reset control register
GTMCR	—	—	Global test mode configuration register
GTMER	—	—	Global test mode enable register
GFDCFG	—	—	Global CAN FD configuration register
GTMLKR	—	—	Global test mode lock key register
RTPARk	—	—	RAM test page access register k (k = 0 to 63)
AFIGSR	—	—	Acceptance filter list ignore entry setting register
AFIGER	—	—	Acceptance filter list ignore entry enable register
RMIER	—	—	Receive message buffer interrupt enable register
ECCSR	—	—	ECC control/status register
ECTMR	—	—	ECC test mode register
ECTDR	—	—	ECC decoder test data register
ECEAR	—	—	ECC error address register

2.23 Serial Peripheral Interface

Table 2.47 is Comparative Overview of Serial Peripheral Interfaces, and Table 2.48 is Comparison of Serial Peripheral Interface Registers.

Table 2.47 Comparative Overview of Serial Peripheral Interfaces

Item	RX62T (RSPI)	RX26T (RSPId)
Number of channels	1 channel	1 channel
RSPI transfer functions	• Use of MOSI (Master out/slave in), MISO (Master in/slave out), SSL (slave select), and RSPCK (R SPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Serial communication is possible in master/slave mode. • Switching of the polarity of the serial transfer clock • Switching of the phase of the serial transfer clock	• Use of MOSI (Master out/slave in), MISO (Master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Communication modes: Full-duplex or simplex (transmit-only or reception-only (in slave mode)) can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK
Data format	• Switching between MSB first and LSB first is possible. • Transfer bit length can be changed to 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission or reception (each frame consisting of up to 32 bits).	• Switching between MSB first and LSB first is possible. • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, and 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission or reception (each frame consisting of up to 32 bits). • Byte swapping of transmit and receive data is possible. • Ability to invert the logic level of transmit/receive data
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, it depends on the bit rate of the input clock regardless of the setting of the register and the SPCMDm.BRDV[1:0] bits (bit rate frequency division setting bits) (m = 0 to 7).	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4). — Width at high level: 2 cycles of PCLK — Width at low level: 2 cycles of PCLK
Buffer configuration	• Double buffer configuration for the transmit and receive buffers • 128-bit transmit/receive buffers	• Double buffer configuration for the transmit and receive buffers • 128 bits for the transmit and receive buffers

Item	RX62T (RSPI)	RX26T (RSPId)
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection
SSL control function	• Four SSL pins (SSL0 to SSL3) for each channel • In single-master mode, SSL0 to SSL3 pins are output. • In multi-master mode: SSL0 pin for input, and SSL1 to SSL3 pins for either output or high-impedance. • In slave mode: SSL0 pin for input, and SSL1 to SSL3 pins for high-impedance. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity
Control in master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • The following items can be specified for each command: — SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value can be specified in SSL negation.	• A transfer of up to eight commands can be executed sequentially in looped execution. • The following items can be specified for each command: — SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value can be specified in SSL negation. • RSPCK auto-stop function • The delay between data bytes can be shortened during burst transfers.

Item	RX62T (RSPI)	RX26T (RSPId)
Interrupt sources	• Maskable interrupt sources — RSPI receive interrupt (receive buffer full) — RSPI transmit interrupt (transmit buffer empty) — RSPI error interrupt (mode fault, overrun, or parity error) — RSPI idle interrupt (RSPI idle)	• Interrupt sources — Receive buffer full interrupt — Transmit buffer empty interrupt — Error interrupt (mode fault, overrun, underrun, or parity error) — Idle interrupt — Communication end interrupt
Event link function (output)	—	• The following events can be output to the event link controller. (RSPI0) — Receive buffer full events — Transmit buffer empty events — Error events (mode fault, overrun, underrun, and parity error) — Idle event — Communication completion events
Other functions	• RSPI disable (initialization) function • Loopback mode function	• Function for initializing the RSPI • Loopback mode function
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.48 Comparison of Serial Peripheral Interface Registers

Register	Bit	RX62T (RSPI)	RX26T (RSPId)
SPSR	UDRF	—	Underrun error flag
	SPCF	—	Communication completion flag
SPDR	—	RSPI data register Supported access sizes • Longword access (SPDCR.SPLW = 1) • Word access (SPDCR.SPLW = 0)	RSPI data register Supported access sizes • Longword access (SPDCR.SPLW = 1, SPDCR.SPBYT = 0) • Word access (SPDCR.SPLW = 0, SPDCR.SPBYT = 0) • Byte access (SPDCR.SPBYT = 1)
SPDCR	SLSEL[1:0]	SSL pin output selection bits	—
	SPBYT	—	RSPI byte access specification bit
SPCR2	SCKASE	—	RSPCK auto-stop function enable bit
SPDCR2	—	—	RSPI data control register 2
SPCR3	—	—	RSPI control register 3

2.24 CRC Calculator

Table 2.49 is Comparative Overview of CRC Calculators, and Table 2.50 is Comparison of CRC Calculator Registers.

Table 2.49 Comparative Overview of CRC Calculators

Item	RX62T (CRC)	RX26T (CRCA)	
Data size	8 bits	8 bits	32 bits
Data for CRC calculation	CRC codes are generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 32n-bit units (where n is a whole number)
CRC processor unit	8-bit parallel processing	8-bit parallel processing	32-bit parallel processing
CRC generating polynomial	One of three generating polynomials is selectable • 8-bit CRC: $X^8 + X^2 + X + 1$ • 16-bit CRC: $X^{16} + X^{15} + X^2 + 1$ $X^{16} + X^{12} + X^5 + 1$	One of three generating polynomials is selectable • 8-bit CRC: $X^8 + X^2 + X + 1$ • 16-bit CRC: $X^{16} + X^{15} + X^2 + 1$ $X^{16} + X^{12} + X^5 + 1$	One of two generating polynomials is selectable • 32-bit CRC: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$
CRC calculation switching	CRC code generation for LSB first transfer or MSB first transfer can be selected.	The order of the bits produced by CRC calculation can be switched for LSB first or MSB first communication	
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state	

Table 2.50 Comparison of CRC Calculator Registers

Register	Bit	RX62T (CRC)	RX26T (CRCA)
CRCCR	GPS[1:0] (RX62T) GPS[2:0] (RX26T)	CRC generating polynomial switching bits b1 b0 0 0: No calculation is executed. 0 1: 8-bit CRC ($X^8 + X^2 + X + 1$) 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$) 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$)	CRC generating polynomial switching bits b2 b0 0 0 0: No calculation is executed. 0 0 1: 8-bit CRC ($X^8 + X^2 + X + 1$) 0 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$) 0 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$) 1 0 0: 32-bit CRC ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1: 32-bit CRC ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) 1 1 0: No calculation is executed. 1 1 1: No calculation is executed.
	LMS	CRC calculation switching bit (b2)	CRC calculation switching bit (b6)
CRCDIR	—	CRC data input register Supported access sizes • Byte access	CRC data input register Supported access sizes • Longword access (32-bit CRC selected) • Byte access (16-bit or 8-bit CRC selected)
CRCDOR	—	CRC data output register Supported access sizes • Word access The lower byte (b7 to b0) is used when generating 8-bit CRC.	CRC data output register Supported access sizes • Longword access (32-bit CRC selected) • Word access (16-bit CRC selected) • Byte access (8-bit CRC selected)

2.25 12-Bit A/D Converter

Table 2.51 is Comparative Overview of 12-Bit A/D Converters, and Table 2.52 is Comparison of 12-Bit A/D Converter Registers.

Table 2.51 Comparative Overview of 12-Bit A/D Converters

Item	RX62T (S12ADA)	RX26T (S12ADHa)
Number of units	Two units (S12AD0 and S12AD1)	Three units (S12AD, S12AD1, and S12AD2) (for products with RAM capacity 64 KB) Two units (S12AD and S12AD2) (for products with RAM capacity 48 KB)
Input channels	S12AD0: 4 channels S12AD1: 4 channels	S12AD: 4 channels S12AD1: 4 channels S12AD2: 14 channels
Extended analog function	—	Temperature sensor output, internal reference voltage (S12AD2 only)
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	1.0 µs per channel (when A/D conversion clock (ADCLK) = 50 MHz, AVCC0 = 4.0 to 5.5 V) 2.0 µs per channel (when A/D conversion clock (ADCLK) = 25 MHz, AVCC0 = 3.0 to 3.6 V)	0.9 µs per channel (when A/D conversion clock (ADCLK) = 60 MHz)
A/D conversion clock	• Four types: PCLK, PCLK/2, PCLK/4, and PCLK/8	• Peripheral module clock PCLKB and A/D conversion clock ADCLK can be set so that the frequency division ratio should be one of the following. — PCLKB to ADCLK frequency ratio = 1:1, 2:1, 4:1, or 1:2 • ADCLK is set by using the clock generation circuit. • The A/D conversion clock (ADCLK) can operate at frequencies from a Maximum of 60 MHz to a minimum of 8 MHz.

Item	RX62T (S12ADA)	RX26T (S12ADHa)
Data register	• 10 registers for analog input • One register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • There are two AD data registers for input of AN000 and AN100, the conversion result storage destination is switched between them by the trigger type.	• One register per channel for analog input, one register per unit for A/D-converted data duplication in double trigger mode for each unit, and two registers per unit for A/D-converted data duplication during extended operation in double trigger mode for each unit • One register for temperature sensor output (S12AD2) • One register for internal reference voltage (S12AD2) • One register for self-diagnosis for each unit • The results of A/D conversion are stored in 12-bit A/D data registers. • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): — The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): — A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.
Operating mode	• Single mode: — Conversion is performed only once on the analog input of one channel. • Continuous scan mode: — Conversion is performed repeatedly on a maximum of 4 channels of analog input.	The operating mode can be set individually for each unit. • Single scan mode: — A/D conversion is performed only once on arbitrarily selected analog input channels. — A/D conversion is performed only once on the temperature sensor output (S12AD2). — A/D conversion is performed only once on the internal reference voltage. (S12AD2) • Continuous scan mode: — A/D conversion is performed repeatedly on arbitrarily selected analog input channels.

Item	RX62T (S12ADA)	RX26T (S12ADHa)
Operating mode	• One cycle scan mode: — Conversion is performed only once on a maximum of 4 channels of analog input. • Two channel scan mode: — Channels in the unit is divided into two groups, and two start causes can be set.	• Group scan mode: — Two (groups A and B) or three (groups A, B, and C) can be selected as the number of groups to be used. (Only the combination of groups A and B can be selected when the number of groups is two.) — Arbitrarily selected analog input channels, the temperature sensor output (S12AD2), and the internal reference voltage (S12AD2) are divided into two groups (group A and B) or three groups (group A, B, and C), and A/D conversion of the analog input selected on a group basis is performed only once. — The scanning start condition for groups A, B, and C (synchronous trigger) can be independently selected, allowing A/D conversion of each group to be started independently. • Group scan mode (with group priority control selected): — If a higher-priority group trigger is input during scanning of a lower-priority group, scanning of the lower-priority group stops and scanning of the higher-priority group starts. — The priority order is group A (highest) > group B > group C (lowest). — Whether or not to restart scanning (rescan) of the lower-priority group after processing for the higher-priority group completes, is selectable. Rescan can also be set to start either from the first selected channel or from the channel on which A/D conversion did not complete.

Item	RX62T (S12ADA)	RX26T (S12ADHa)
Conditions for A/D conversion start	• Software trigger • Synchronous trigger — Trigger by the multi-function timer pulse unit 3 (MTU3) or general PWM timer (GPT) • Asynchronous trigger — A/D conversion can be triggered by the external trigger ADTRG0#(S12AD0) and ADTRG1# (S12AD1) pins.	• Software trigger • Synchronous trigger — Trigger by the multi-function timer pulse unit (MTU), general purpose PWM timer (GPTW), 8-bit timer (TMR), or event link controller (ELC) • Asynchronous trigger — A/D conversion can be triggered by the external trigger ADTRG0# (S12AD), ADTRG1# (S12AD1), and ADTRG2# (S12AD2) pins (individually for each of unit).
Functions	• Sample & hold function (3 channels per unit) — A dedicated independent sample and hold circuit is incorporated for channel 0 to 2 (AN000 to AN002) of S12AD0 and channel 0 to 2 (AN100 to AN102) of S12AD1. This enables simultaneous sampling of multiple channels (maximum of three channels) for each unit. • Self-diagnosis of A/D converter • Input signal amplification function using the programmable gain amplifier (3 channels per unit) • Window comparator function (3 channels per unit)	• Sample & hold function dedicated to channels (three channels for each of S12AD and S12AD1) (Constant sampling can be set.) • Variable sampling time (settable on a per-channel basis) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection assist function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers • Compare function (window A and window B) • Order of channel conversion can be specified for each unit. • Input signal amplification function using the programmable gain amplifier (3 channels for each unit)

Item	RX62T (S12ADA)	RX26T (S12ADHa)
Interrupt sources	• For each unit, an interrupt request (S12ADI) is generated at the completion of A/D conversion. • The S12ADI interrupt can activate the data transfer controller (DTC). • An interrupt request (CMPI) is generated at comparator detection. (This can also be used as a POE source.)	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of single scan (individually for each unit). • In double trigger mode, A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of double scan (individually for each unit). • In group scan mode, an A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of group A scan, an A/D scan end interrupt request (S12GBADI, S12GBADI1, or S12GBADI2) for group B can be generated on completion of group B scan, and an A/D scan end interrupt request (S12GCADI, S12GCADI1, or S12GCADI2 for group C can be generated on completion of group C scan. • When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of a double scan of group A. A corresponding scan end interrupt request (S12GBADI/S12GCADI, S12GBADI1/S12GCADI1, or S12GBADI2/S12GCADI2) can be generated on completion of a group B or group C scan. • A compare interrupt request (S12CMPAI, S12CMPAI1, S12CMPAI2, S12CMPBI, S12CMPBI1, or S12CMPBI2) can be generated upon a match with the comparison condition for the digital compare function. • The S12ADI/S12ADI1/S12ADI2, S12GBADI/S12GBADI1/S12GBADI2, and S12GCADI/S12GCADI1/S12GCADI2 interrupts can activate the DMA controller (DMAC) or data transfer controller (DTC).

Item	RX62T (S12ADA)	RX26T (S12ADHa)
Event link function	—	• An event can be output upon completion of all scans. • In single scan mode, an event can be output when the compare function window condition is met. • Scan can be started by a trigger output by the ELC.
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Table 2.52 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX62T (S12ADA)	RX26T (S12ADHa)
ADDRn (RX62T) ADDRy (RX26T)	—	A/D data register n (n = 0A, 0B, 1 to 3)	A/D data register y (y = 0 to 11, 16, 17)
ADDBLDR	—	—	A/D data duplication register
ADDBLDRA	—	—	A/D data duplication register A
ADDBLDRB	—	—	A/D data duplication register B
ADTSDR	—	—	A/D temperature sensor data register
ADOCDR	—	—	A/D internal reference voltage data register
ADCSR	—	AD control register ADCSR is a 8-bit register.	AD control register ADCSR is a 16-bit register.
	DRLANS[4:0]	—	Double trigger target channel select bits
	GBADIE	—	Group B scan end interrupt enable bit
	DBLE	—	Double trigger mode select bit
	CKS[1:0]	Clock select bits	—
	ADCS[1:0]	A/D conversion mode select bits b6 b5 0 0: Single mode 0 1: One cycle scan mode 1 0: Continuous scan mode 1 1: Two channel scan mode	Scan mode select bits b14 b13 0 0: Single scan mode 0 1: Group scan mode 1 0: Continuous scan mode 1 1: Setting prohibited
ADANS	—	A/D channel select register	—
ADANSA0	—	—	A/D channel select register A0
ADANSA1	—	—	A/D channel select register A1
ADANSB0	—	—	A/D channel select register B0
ADANSB1	—	—	A/D channel select register B1
ADANSC0	—	—	A/D channel select register C0
ADANSC1	—	—	A/D channel select register C1
ADSCSn	—	—	A/D channel conversion order setting register n (n = 0 to 6)
ADADS0	—	—	A/D-converted value addition/average channel select register 0
ADADS1	—	—	A/D-converted value addition/average channel select register 1

Register	Bit	RX62T (S12ADA)	RX26T (S12ADHa)
ADADC	—	—	A/D-converted value addition/averaging count select register
ADCER	SHBYP	Dedicated sample-and-hold circuit select bit	—
	ADPRC[1:0]	A/D data register bit precision set bits	—
	ASE	—	A/D data register automatic setting enable bit
	ADIE2	2-channel scan interrupt select bit	—
	ADIEW	Double trigger interrupt select bit	—
ADSTRGR	ADSTRS0 [4:0]	A/D start trigger group 0 select bits	—
	TRSB[6:0]	—	Group B A/D conversion start trigger select bits
	ADSTRS1 [4:0]	A/D start trigger group 1 select bit	—
	TRSA[6:0]	—	A/D conversion start trigger select bits
ADEXICR	—	—	A/D conversion extended input control register
ADGCEXCR	—	—	A/D group C extended input control register
ADGCTRGR	—	—	A/D group C trigger select register
ADGCTRGR2	—	—	A/D group C trigger select register 2
ADSSTRn	—	—	A/D sampling state register n (n = 0 to 11, L, T, O)
ADSHCR	—	—	A/D sample and hold circuit control register
ADSHMSR	—	—	A/D sample and hold operating mode select register
ADDISCR	—	—	A/D disconnection detection control register
ADELCCR	—	—	A/D event link control register
ADGSPCR	—	—	A/D group scan priority control register
ADCMPCR	—	—	A/D compare function control register
ADCMPANSR0	—	—	A/D compare function window A channel select register 0
ADCMPANSR1	—	—	A/D compare function window A channel select register 1
ADCMPANSER	—	—	A/D compare function window A extended input select register
ADCMPLR0	—	—	A/D compare function window A compare condition setting register 0
ADCMPLR1	—	—	A/D compare function window A compare condition setting register 1
ADCMPLER	—	—	A/D compare function window A extended input compare condition setting register

Register	Bit	RX62T (S12ADA)	RX26T (S12ADHa)
ADCMPDR0	—	—	A/D compare function window A lower level setting register
ADCMPDR1	—	—	A/D compare function window A upper level setting register
ADCMPSR0	—	—	A/D compare function window A channel status register 0
ADCMPSR1	—	—	A/D compare function window A channel status register 1
ADCMPSER	—	—	A/D compare function window A extended input channel status register
ADWINMON	—	—	A/D compare function window A/B status monitoring register
ADCMPBNSR	—	—	A/D compare function window B channel select register
ADWINLLB	—	—	A/D compare function window B lower level setting register
ADWINULB	—	—	A/D compare function window B upper level setting register
ADCMPBSR	—	—	A/D compare function window B channel status register
ADPGACR	—	—	A/D programmable gain amplifier control register
ADPGAGS0	—	—	A/D programmable gain amplifier gain setting register 0
ADVMONCR	—	—	A/D internal reference voltage monitoring circuit enable register
ADVMONO	—	—	A/D internal reference voltage monitoring circuit output enable register
ADPG	—	A/D programmable gain amplifier register	—
ADCMPMD0	—	Comparator operating mode select register 0	—
ADCMPMD1	—	Comparator operating mode select register 1	—
ADCMPNR0	—	Comparator filter mode register 0	—
ADCMPNR1	—	Comparator filter mode register 1	—
ADCMPFR	—	Comparator detection flag register	—
ADCMPSEL	—	Comparator interrupt select register	—
ADSSTR	—	A/D sampling state register	—

2.26 RAM

Table 2.53 is Comparative Overview of RAM, and Table 2.54 is Comparison of RAM Registers.

Table 2.53 Comparative Overview of RAM

Item	RX62T	RX26T
RAM capacity	12 KB (RAM0: 12 KB)	64 KB/48 KB
RAM addresses	RAM0: 0000 0000h to 0000 27FFh 0000 4000h to 0000 4A7Fh	• For products with RAM capacity 64 KB 0000 0000h to 0000 FFFFh • For products with RAM capacity 48 KB 0000 0000h to 0000 BFFFh
Memory buses	Memory bus 1	Memory bus 1
Access	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.
Low power consumption function	The module stop state is selectable for RAM0.	Ability to transition to module stop state
Error checking	—	• Parity check: Detection of 1-bit errors • A non-maskable interrupt or an interrupt is generated when an error occurs.

Table 2.54 Comparison of RAM Registers

Register	Bit	RX62T	RX26T
RAMMODE	—	—	RAM operating mode control register
RAMSTS	—	—	RAM error status register
RAMECAD	—	—	RAM error address capture register
RAMPRCR	—	—	RAM protection register

2.27 Flash Memory

Table 2.55 is Comparative Overview of Flash Memory, and Table 2.56 is Comparison of Flash Memory Registers.

Table 2.55 Comparative Overview of Flash Memory

	RX62T		RX26T	
Item	**Code Flash Memory**	**Data Flash Memory**	**Code Flash Memory**	**Data Flash Memory**
Memory capacity	• 256 KB • 128 KB • 64 KB	• 32 KB • 8 KB	Max. 512 KB	16 KB
Addresses	• Products with capacity of 256 KB: — FFFC 0000h to FFFF FFFFh • Products with capacity of 128 KB: — FFFE 0000h to FFFF FFFFh • Products with capacity of 64 KB: — FFFF 0000h to FFFF FFFFh	• Products with capacity of 32 KB: — 0010 0000h to 0010 1FFFh • Products with capacity of 8 KB: — 0010 0000h to 0010 1FFFh	• Products with capacity of 512 KB: [Linear mode] — FFF8 0000h to FFFF FFFFh [Dual mode] Bank 1 — FFF8 0000h to FFFB FFFFh Bank 2 — FFFC 0000h to FFFF FFFFh • Products with capacity of 256 KB: — FFFC 0000h to FFFF FFFFh • Products with capacity of 128 KB: — FFFE 0000h to FFFF FFFFh	• Products with capacity of 16 KB: — 0010 0000h to 0010 3FFFh
Read cycles	Single-ICLK-cycle fast read is possible.	Word or byte read access requires 3 PCLK cycles.	One cycle	16-bit or 8-bit read access requires 8 FCLK clock cycles.
Value after erasure	ROM: FFh	Undefined	FFh	Undefined

Item	RX62T		RX26T	
	Code Flash Memory	**Data Flash Memory**	**Code Flash Memory**	**Data Flash Memory**
Programming/ erasing method	• A sequencer (FCU) dedicated to ROM rewrite is incorporated. • ROM write and erasure are possible by issuing a command to FCU. • If the ROM has been erased, 32-bit reading of FFFF FFFFh is possible.	• A sequencer (FCU) dedicated to data flash rewrite is incorporated. • Data flash write and erasure are possible by issuing a command to FCU.	• FACI commands specified in the FACI command issuing area (007E 0000h) can be used to program and erase the code flash memory and data flash memory. • Programming and erasure through serial interface transfer by a flash memory programmer (serial programming) • A user program can be used to program and erase the flash memory (self-programming).	
Security function	—	—	Protects against illicit tampering with or reading of data in flash memory.	
Protection function	• If an abnormal operation is detected during writing/erasing, writing/erasing is prohibited from that time. • Unintended rewrite can be prevented by the FENTRYR. FENTRY0 bit, the FWEPROR.FLWE [1:0] bits, and the lock bit.	• If an abnormal operation is detected during writing/erasing, writing/erasing is prohibited from that time. • Unintended rewrite can be prevented by the FENTRYR. FENTRYD bit, the FWEPROR.FLWE [1:0] bits, the DFLREk register, and the DFLWEk (k = 0, 1) register.	Protects against erroneous programming of the flash memory.	
Dual bank function	—	—	The dual bank configuration allows safe updating even upon interruption during a rewrite operation. • Linear mode: Code flash memory is used as one area. • Dual mode: Code flash memory is divided into two areas.	—
Trusted Memory (TM) function	—	—	Protects against illicit reading of code flash memory. • Linear mode: Blocks 8 and 9 • Dual mode: Blocks 8, 9, 30, and 31	—

Item	RX62T		RX26T	
	Code Flash Memory	**Data Flash Memory**	**Code Flash Memory**	**Data Flash Memory**
BGO (Background operation) function	• When writing/erasing of ROM is being executed, the CPU can execute a program that is allocated in an area other than those in ROM or data flash memory. • When writing/erasing of data flash memory is being executed, the CPU can execute a program that is allocated in ROM.	• When writing/erasing of ROM is being executed, the CPU can execute a program that is allocated in an area other than those in ROM or data flash memory. • When writing/erasing of data flash memory is being executed, the CPU can execute a program that is allocated in ROM.	• The code flash memory can be read while the code flash memory is being programmed or erased. • The data flash memory can be read while the code flash memory is being programmed or erased. • The code flash memory can be read while the data flash memory is being programmed or erased.	
Suspend/ resume function	• The CPU can suspend writing/erasing of ROM and execute a program in a ROM area (suspend). • After suspension, the CPU can resume writing/erasing of ROM (resume).	• The CPU can suspend writing/erasing of data flash memory and execute reading from a data flash memory area (suspend). • After suspension, the CPU can resume writing/erasing of ROM (resume).	—	
Units of programming and erasure	• Unit of programming for the user area: 256 bytes • Units of erasure for the user area: 4 KB (8 blocks), 16 KB (if ROM capacity is 256 KB: 14 blocks, if ROM capacity is 128 KB: 6 blocks, if ROM capacity is 64 KB: 2 blocks)	• Unit of programming for the data area: 8 bytes or 128 bytes • Unit of data area erasure: 2 KB (if the capacity of data flash memory is 32 KB: 16 blocks, if the capacity of data flash memory is 8 KB: 4 blocks)	• Programming: 128 bytes • Erasure: block units	• Programming: 4 bytes • Erasure: block units
Blank check function	—	• The blank check command can be executed to check the erasure condition of data flash memory. • The size of the area for blank check is 8 bytes or 2 KB.	—	—
Other functions	—	—	Interrupts can be accepted during self-programming.	

Item	RX62T		RX26T	
	Code Flash Memory	**Data Flash Memory**	**Code Flash Memory**	**Data Flash Memory**
On-board programming (serial programming and self-programming)	• Rewrite in boot mode — The asynchronous serial interface (SCI1) is used. — The communication speed is adjusted automatically. • Rewrite by a ROM rewrite routine in a user program — ROM can be rewritten without resetting the system.	• Rewrite in boot mode — The asynchronous serial interface (SCI1) is used. — The communication speed is adjusted automatically. • Rewrite by a data flash memory rewrite routine in a user program — Data flash memory can be rewritten without resetting the system.	• Programming/erasure in boot mode (SCI interface) — The asynchronous serial interface (SCI1) is used. — The communication speed is adjusted automatically.	
	—	—	• Programming/erasure in boot mode (FINE interface) — FINE is used. • Programming/erasure in single-chip mode — Programming and erasure are possible by using the code flash memory/data flash memory rewrite routine in the user program.	
Off-board programming (programming /erasure using a parallel programmer)	The user area can be rewritten using the PROM writer.	—	—	—
Unique ID	—	—	A unique 12-byte ID code is provided for each MCU.	

Table 2.56 Comparison of Flash Memory Registers

Register	Bit	RX62T	RX26T
FMODR	—	Flash mode register	—
FASTAT	DFLWPE	Data flash programing/erasure protection violation bit	—
	DFLRPE	Data flash read protection violation bit	—
	DFLAE (RX62T) DFAE (RX26T)	Data flash access violation bit	Data flash memory access violation flag
	ROMAE (RX62T) CFAE (RX26T)	ROM access violation bit	Code flash memory access violation flag
FAEINT	DFLWPEIE	Data flash programing/erasure protection violation interrupt enable bit	—
	DFLRPEIE	Data flash read protection violation interrupt enable bit	—
	DFLAEIE (RX62T) DFAEIE (RX26T)	Data flash access violation interrupt enable bit	Data flash memory access violation interrupt enable bit
	ROMAEIE (RX62T) CFAEIE (RX26T)	ROM access violation interrupt enable bit 0: A FIFERR interrupt request is not generated when the FASTAT.ROMAE bit =1. 1: A FIFERR interrupt request is generated when the FASTAT.ROMAE bit =1.	Code flash memory access violation interrupt enable bit 0: Generation of a FIFERR interrupt request is disabled when FASTAT.CFAE = 1. 1: Generation of a FIFERR interrupt request is enabled when FASTAT.CFAE = 1.
FCURAME	—	FCU RAM enable register	—
FSTATR0 (RX62T) FSTATR (RX26T)	—	Flash status register 0 FSTATR0 is an 8-bit register.	Flash status register FSTATR0 is a 16-bit register
	FLWEERR		Flash P/E protection error flag
	PRGSPD	Write suspension status bit (b0)	Program suspension status flag (b8)
	ERSSPD	Erasure suspension status bit (b1)	Erasure suspension status flag (b9)
	DBFULL	—	Data buffer full flag
	SUSRDY	Suspension ready bit (b3)	Suspension ready bit (b11)
	PRGERR	Write error bit (b4)	Program error flag (b12)
	ERSERR	Erasure error flag (b5)	Erasure error bit (b13)
	ILGLERR	Illegal command error bit (b6)	Illegal command error bit (b14)

Register	Bit	RX62T	RX26T
FSTATR0 (RX62T) FSTATR (RX26T)	FRDY	Flash ready flag (b7) 0: Executing write/erasure, write/erasure suspension processing, the lock bit read 2 command, the peripheral clock notification command, or blank check of data flash memory 1: None of the above processing is being performed.	Flash ready flag (b15) 0: Executing a command or programming, block erasure, P/E suspend, P/E resume, forced stop, blank check, or configuration setting 1: None of the above processing is being performed.
FSTATR1	—	Flash status register 1	—
FENTRYR	FENTRY0 (RX62T) FENTRYC (RX26T)	ROM P/E mode entry bit 0	Code flash memory P/E mode entry bit
	FEKEY[7:0] (RX62T) KEY[7:0] (RX26T)	Key code	Key code bit
FPROTR	—	Flash protection register	—
FRESETR	—	Flash reset register	—
FPESTAT	PEERRST [7:0]	P/E error status bit 01h: Write error for an area protected by the lock bit 02h: Write error by a cause other than lock bit protection 11h: Erasure error for an area protected by the lock bit 12h: Erasure error by a cause other than lock bit protection (Values other than above are reserved.)	P/E error status bit 00h: No error 02h: Program error 12h: Erase error
PCKAR	—	Peripheral clock notification register	—
FWEPROR	FLWE[1:0]	Flash programming/erasure enable bits b1 b0 0 0: Write/Erasure disabled 0 1: Write/Erasure enabled 1 0: Write/Erasure disabled (initial value) 1 1: Write/Erasure disabled	Flash programming/erasure enable bits b1 b0 0 0: Programming, block erase, and blank check are disabled. 0 1: Programming block erase, and blank check are enabled. 1 0: Programming, block erase, and blank check are disabled. 1 1: Programming, block erase, and blank check are disabled.
DFLRE0	—	Data flash read enable register 0	—
DFLRE1	—	Data flash read enable register 1	—
DFLWE0	—	Data flash write/erasure enable register 0	—
DFLWE1	—	Data flash write/erasure enable register 1	—

Register	Bit	RX62T	RX26T
DFLBCCNT (RX62T) FBCCNT (RX26T)	—	Data flash blank check control register	Data flash blank check control register
DFLBCSTAT (RX62T) FBCSTAT (RX26T)	—	Data flash blank check status register	Data flash blank check status register
FSADDR	—	—	FACI command start address register
FEADDR	—	—	FACI command end address register
FSUINITR	—	—	Flash sequencer set-up initialization register
FCMDR	—	—	FACI command register
FPSADDR	—	—	Data flash programming start address register
FAWMON	—	—	Flash access window monitor register
FPCKAR	—	—	Flash sequencer processing clock frequency notification register
FSUACR	—	—	Start-up area control register
UIDRn	—	—	Unique ID register n (n = 0 to 2)

2.28 Packages

As indicated in Table 2.57, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage.

Table 2.57 Packages

Package Type	RENESAS Code	
	RX62T	RX26T
112-pin LQFP	○	×
100-pin LFQFP	×	○
100-pin LQFP	○	×
80-pin LFQFP	×	○
80-pin LQFP	○	×
64-pin LFQFP	×	○
64-pin LFQFP	×	○
64-pin LQFP	○	×
48-pin LFQFP	×	○

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by **blue text**. Items that exist on both groups with different specifications are indicated by **red text**. **Black text** indicates there is no differences in the item's specifications between groups.

3.1 100 Pin Package

Table 3.1 is Comparative Listing of 100-Pin Package Pin Functions.

Table 3.1 Comparative Listing of 100-Pin Package Pin Functions

100-Pin	RX62T (100-pin LQFP)	RX26T (100-pin LFQFP)
1	PE5/IRQ0-B	PE5/MTIOC9D/MTIOC9D#/GTIOC3A/GTETRGB/GTIOC3A#/GTETRGD/SCK009/CTS009#/RTS009#/SS009#/TXDB009/IRQ0/ADST0
2	EMLE	EMLE/PN7/MTIOC9D/MTIOC9D#/IRQ5/ADST0
3	VSS	VSS
4	MDE	P00/MTIOC9A/MTIOC9A#/CACREF/GTIU/TIC3/RXD12/SMISO12/SSCL12/RXDX12/RXD009/SMISO009/SSCL009/IRQ2/ADST1/COMP0
5	VCL	VCL
6	MD1	MD/FINED/PN6
7	MD0	P01/MTIOC9C/MTIOC9C#/POE12#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/GTIW/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/TXD009/TXDA009/SMOSI009/SSDA009/IRQ4/ADST2/COMP1
8	PE4/MTCLKC-C/IRQ1-B/POE10#-B	PE4/MTCLKC/MTCLKC#/POE10#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/SCK009/TXDB009/IRQ1
9	PE3/MTCLKD-C/IRQ2-A/POE11#	PE3/MTCLKD/MTCLKD#/POE11#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/CTS009#/RTS009#/SS009#/DE009/IRQ2
10	RES#	RES#
11	XTAL	XTAL/P37/RXD5/SMISO5/SSCL5
12	VSS	VSS
13	EXTAL	EXTAL/P36/TXD5/SMOSI5/SSDA5
14	VCC	VCC
15	PE2/NMI/POE10#-A	PE2/POE10#/NMI/IRQ0
16	PE1/SSL3-C	PE1/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/CTS12#/RTS12#/SS12#/SSLA3/SSL03/IRQ15
17	PE0/CRX-C/SSL2-C	PE0/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/GTIV/RXD5/SMISO5/SSCL5/SSLA2/SSL02/CRX0/IRQ7

100-Pin	RX62T (100-pin LQFP)	RX26T (100-pin LFQFP)
18	PD7/GTIOC0A-B/CTX-C/SSL1-C/TRST#	TRST#/PD7/MTIOC9A/MTIOC9A#/TMRI1/ TMRI5/GTIOC0A/GTIOC3A/GTIOC0A#/ GTIOC3A#/GTIU/TXD5/SMOSI5/SSDA5/ SCK009/TXD008/TXDA008/SMOSI008/ SSDA008/TXDB009/SSLA1/SSL01/CTX0/ IRQ8
19	PD6/GTIOC0B-B/SSL0-C/TMS	TMS/PD6/MTIOC9C/MTIOC9C#/TMO1/ GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/ GTIW/CTS1#/RTS1#/SS1#/RXD12/ SMISO12/SSCL12/RXDX12/CTS011#/ RTS011#/SS011#/DE011/SSLA0/SSL00/ IRQ5/ADST0
20	PD5/GTIOC1A-B/RXD1/TDI	TDI/PD5/TMRI0/TMRI6/GTIOC1A/ GTETRGA/GTIOC1A#/GTIOC7A/RXD1/ SMISO1/SSCL1/RXD011/SMISO011/ SSCL011/SSL00/IRQ6
21	PD4/GTIOC1B-B/SCK1/TCK	TCK/PD4/TMCI0/TMCI6/GTIOC1B/ GTETRGB/GTIOC1B#/SCK1/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SCK011/TXDB011/SSL02/IRQ2
22	PD3/GTIOC2A-B/TXD1/TDO	TDO/PD3/TMO0/GTIOC2A/GTETRGC/ GTIOC2A#/GTIOC7B/TXD1/SMOSI1/ SSDA1/TXD011/TXDA011/SMOSI011/ SSDA011/MOSI0
23	PD2/GTIOC2B-B/MOSI-C/TRCLK	PD2/TMCI1/TMO4/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/SCK5/SCK008/ TXDB008/MOSIA/MOSI0
24	PD1/GTIOC3A/MISO-C/TRDATA3	PD1/TMO2/GTIOC3A/GTIOC0B/GTIOC3A#/ GTIOC0B#/RXD008/SMISO008/SSCL008/ MISOA/MISO0
25	PD0/GTIOC3B/RSPCK-C/TRDATA2	PD0/TMO6/GTIOC3B/GTIOC1A/GTIOC3B#/ GTIOC1A#/TXD008/TXDA008/SMOSI008/ SSDA008/RSPCKA/RSPCK0
26	PB7/SCK2-A/TRDATA1	PB7/GTIOC1B/GTIOC1B#/SCK5/SCK12/ SCK011/TXDB011/SSL03
27	PB6/CRX-A/RXD2-A/TRDATA0	PB6/GTIOC2A/GTIOC3A/GTIOC2A#/ GTIOC3A#/TOC0/RXD5/SMISO5/SSCL5/ RXD12/SMISO12/SSCL12/RXDX12/ RXD011/SMISO011/SSCL011/MISO0/CRX0/ IRQ2
28	PB5/CTX-A/TXD2-A/TRSYNC	PB5/GTIOC2B/GTIOC3B/GTIOC2B#/ GTIOC3B#/TIC0/TXD5/SMOSI5/SSDA5/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ TXD011/TXDA011/SMOSI011/SSDA011/ RSPCK0/CTX0
29	PLLVCC	VCC
30	PB4/GTETRG/IRQ3/POE8#	PB4/POE8#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/GTCPPO0/CTS5#/ RTS5#/SS5#/RXD12/SMISO12/SSCL12/ RXDX12/CTS011#/RTS011#/SS011#/ SCK011/TXDB011/MISOA/SSL01/CRX0/ IRQ3
31	PLLVSS	VSS

100-Pin	RX62T (100-pin LQFP)	RX26T (100-pin LFQFP)
32	PB3/MTIOC0A-A/SCK0	PB3/MTIOC0A/MTIOC0A#/CACREF/GTIU/TOC1/SCK6/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/CTS009#/RTS009#/SS009#/DE009/RSPCKA/CTX0/IRQ9
33	PB2/MTIOC0B-A/TXD0/SDA	PB2/MTIOC0B/MTIOC0B#/TMRI0/GTADSM0/GTIOC7A/GTIOC7A#/GTIV/TIC1/TXD6/SMOSI6/SSDA6/SDA0/SDA00/ADSM0
34	PB1/MTIOC0C/RXD0/SCL	PB1/MTIOC0C/MTIOC0C#/TMCI0/GTADSM1/GTIOC7B/GTIOC7B#/GTIW/TOC2/RXD6/SMISO6/SSCL6/SCL0/SCL00/IRQ4/ADSM1
35	PB0/MTIOC0D/MOSI-B	PB0/MTIOC0D/MTIOC0D#/TMO0/TIC2/TXD6/SMOSI6/SSDA6/TXD008/TXDA008/SMOSI008/SSDA008/CTS011#/RTS011#/SS011#/DE011/MOSIA/MOSI0/IRQ8/ADTRG2#
36	PA5/ADTRG1#-A/MTIOC1A/MISO-B	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/SMISO6/SSCL6/RXD008/SMISO008/SSCL008/MISOA/MISO0/IRQ1/ADTRG1#
37	PA4/ADTRG0#-A/MTIOC1B/RSPCK-B	PA4/MTIOC1B/MTIOC1B#/TMCI7/SCK6/TXD008/TXDA008/SMOSI008/SSDA008/RSPCKA/RSPCK0/ADTRG0#
38	PA3/MTIOC2A/SSL0-B	PA3/MTIOC2A/MTIOC2A#/TMRI7/GTADSM0/TXD009/TXDA009/SMOSI009/SSDA009/SCK008/TXDB008/SSLA0/SSL00
39	PA2/MTIOC2B/SSL1-B	PA2/MTIOC2B/MTIOC2B#/TMO7/GTADSM1/CTS6#/RTS6#/SS6#/RXD009/SMISO009/SSCL009/SSLA1/SSL01
40	PA1/MTIOC6A/SSL2-B	PA1/MTIOC6A/MTIOC6A#/TMO4/GTCPPO4/TXD009/TXDA009/SMOSI009/SSDA009/RXD011/SMISO011/SSCL011/SSLA2/SSL02/CRX0/IRQ14/ADTRG0#
41	PA0/MTIOC6C/SSL3-B	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK009/TXD011/TXDA011/SMOSI011/SSDA011/TXDB009/SSLA3/SSL03/CTX0
42	VCC	VCC
43	P96/IRQ4/POE4#	P96/POE4#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/GTCPPO4/CTS008#/RTS008#/SS008#/DE008/SSL03/RSPCK0/IRQ4
44	VSS	VSS
45	P95/MTIOC6B	P95/MTIOC6B/MTIOC1A/MTIOC6B#/MTIOC1A#/TMCI3/GTIOC4A/GTIOC7A/GTIOC4A#/GTIOC7A#/GTOUUP/RXD6/SMISO6/SSCL6/RXD008/SMISO008/SSCL008/MISOA/SSL02/MISO0/IRQ1/ADTRG1#
46	P94/MTIOC7A	P94/MTIOC7A/MTIOC2A/MTIOC7A#/MTIOC2A#/TMRI7/GTIOC5A/GTADSM0/GTIOC5A#/GTOVUP/TXD009/TXDA009/SMOSI009/SSDA009/SCK008/TXDB008/SSLA0/SSL00

100-Pin	RX62T (100-pin LQFP)	RX26T (100-pin LFQFP)
47	P93/MTIOC7B	P93/MTIOC7B/MTIOC6A/MTIOC7B#/ MTIOC6A#/TMO4/GTIOC6A/GTIOC6A#/ GTOWUP/TXD009/TXDA009/SMOSI009/ SSDA009/RXD011/SMISO011/SSCL011/ SSLA2/SSL02/MOSI0/CRX0/IRQ14/ ADTRG0#
48	P92/MTIOC6D	P92/MTIOC6D/MTIOC6C/MTIOC6D#/ MTIOC6C#/TMO2/GTIOC4B/GTIOC7B/ GTIOC4B#/GTIOC7B#/GTOULO/SCK009/ TXD011/TXDA011/SMOSI011/SSDA011/ TXDB009/SSLA3/SSL03/MISO0/CTX0
49	P91/MTIOC7C	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC5B#/GTOVLO/RXD5/SMISO5/SSCL5/ RSPCK0
50	P90/MTIOC7D	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC6B#/GTOWLO/TXD5/SMOSI5/ SSDA5/SSL01
51	P76/MTIOC4D/GTIOC2B-A	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC6B/GTIOC2B#/GTIOC6B#/GTOWLO/ SSL03
52	P75/MTIOC4C/GTIOC1B-A	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC5B/GTIOC1B#/GTIOC5B#/GTOVLO/ SSL02
53	P74/MTIOC3D/GTIOC0B-A	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC4B/GTIOC0B#/GTIOC4B#/GTOULO/ SSL01
54	P73/MTIOC4B/GTIOC2A-A	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC6A/GTIOC2A#/GTIOC6A#/GTOWUP/ SSL00
55	P72/MTIOC4A/GTIOC1A-A	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC5A/GTIOC1A#/GTIOC5A#/GTOVUP/ MOSI0
56	P71/MTIOC3B/GTIOC0A-A	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC4A/GTIOC0A#/GTIOC4A#/GTOUUP/ MISO0
57	P70/IRQ5/POE0#	P70/MTIOC0A/MTCLKC/MTIOC0A#/ MTCLKC#/TMRI6/POE0#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/ GTCPPO0/SCK5/CTS009#/RTS009#/ SS009#/DE009/SSLA0/RSPCK0/IRQ5
58	P33/MTIOC3A/MTCLKA-A/SSL3-A	P33/MTIOC3A/MTCLKA/MTIOC3A#/ MTCLKA#/TMO0/GTIOC3B/GTIOC7B/ GTIOC3B#/GTIOC7B#/GTCPPO0/SSLA3/ SSL03/IRQ13
59	P32/MTIOC3C/MTCLKB-A/SSL2-A	P32/MTIOC3C/MTCLKB/MTIOC3C#/ MTCLKB#/TMO6/GTIOC3A/GTIOC7A/ GTIOC3A#/GTIOC7A#/SSLA2/SSL02/IRQ12
60	VCC	VCC
61	P31/MTIOC0A-B/MTCLKC-A/SSL1-A	P31/MTIOC0A/MTCLKC/MTIOC0A#/ MTCLKC#/TMRI6/GTIU/SSLA1/SSL01/IRQ6
62	VSS	VSS
63	P30/MTIOC0B-B/MTCLKD-A/SSL0-A	P30/MTIOC0B/MTCLKD/MTIOC0B#/ MTCLKD#/TMCI6/GTIV/SCK008/CTS008#/ RTS008#/SS008#/DE008/SSLA0/SSL00/ IRQ7/COMP3

100-Pin	RX62T (100-pin LQFP)	RX26T (100-pin LFQFP)
64	P24/RSPCK-A	P27/MTIOC1A/MTIOC0C/MTIOC1A#/ MTIOC0C#/TMO2/TMO6/POE9#/RSPCKA/ RSPCK0/IRQ15
65	P23/CTX-B/LTX/MOSI-A	P24/MTIC5U/MTIC5U#/TMCI2/TMO6/ CTS008#/RTS008#/SS008#/SCK008/DE008/ RSPCKA/RSPCK0/IRQ4/COMP0
66	P22/ADTRG#/CRX-B/LRX/MISO-A	P23/MTIC5V/MTIC5V#/TMO2/CACREF/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ TXD008/TXDA008/SMOSI008/SSDA008/ MOSIA/MOSI0/CTX0/IRQ11/COMP1
67	P21/ADTRG1#-B/MTCLKA-B/IRQ6	P22/MTIC5W/MTCLKD/MTIC5W#/ MTCLKD#/TMRI2/TMO4/MTIOC9B/GTIV/ RXD12/SMISO12/SSCL12/RXDX12/ RXD008/SMISO008/SSCL008/SCK008/ TXDB008/MISOA/MISO0/CRX0/IRQ10/ ADTRG2#/COMP2
68	P20/ADTRG0#-B/MTCLKB-B/IRQ7	P21/MTIOC9A/MTCLKA/MTIOC9A#/ MTCLKA#/TMCI4/TMO6/GTIU/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ TXD008/TXDA008/SMOSI008/SSDA008/ MOSIA/MOSI0/IRQ6/AN217/ADTRG1#/ COMP5
69	P65/AN5	P20/MTIOC9C/MTCLKB/MTIOC9C#/ MTCLKB#/TMRI4/TMO2/GTIW/CTS008#/ RTS008#/SS008#/RXD008/SMISO008/ SSCL008/DE008/RSPCKA/RSPCK0/IRQ7/ AN216/ADTRG0#/COMP4
70	P64/AN4	P65/IRQ9/AN211/CMPC53/DA1
71	AVCC	P64/IRQ8/AN210/CMPC33/DA0
72	VREF	AVCC2
73	AVSS	AVSS2
74	P63/AN3	P63/IRQ7/AN209/CMPC23
75	P62/AN2	P62/IRQ6/AN208/CMPC43
76	P61/AN1	P61/IRQ5/AN207/CMPC13
77	P60/AN0	P60/IRQ4/AN206/CMPC03
78	P55/AN11	P55/IRQ3/AN203/CMPC32
79	P54/AN10	P54/IRQ2/AN202/CMPC22/CVREFC1
80	P53/AN9	P53/IRQ1/AN201/CMPC12/CVREFC0
81	P52/AN8	P52/IRQ0/AN200/CMPC02
82	P51/AN7	P51/AN205/CMPC52
83	P50/AN6	P50/AN204/CMPC42
84	P47/AN103/CVREFH	P47/AN103
85	P46/AN102	P46/AN102/CMPC50/CMPC51
86	P45/AN101	P45/AN101/CMPC40/CMPC41
87	P44/AN100	P44/AN100/CMPC30/CMPC31
88	P43/AN003/CVREFL	P43/AN003
89	P42/AN002	P42/AN002/CMPC20/CMPC21
90	P41/AN001	P41/AN001/CMPC10/CMPC11
91	P40/AN000	P40/AN000/CMPC00/CMPC01
92	AVCC0	AVCC1
93	VREFH0	AVCC0
94	VREFL0	AVSS0
95	AVSS0	AVSS1

100-Pin	RX62T (100-pin LQFP)	RX26T (100-pin LFQFP)
96	P82/MTIC5U/SCK2-B	P82/MTIC5U/MTIC5U#/TMO4/SCK6/SCK12/ IRQ3/COMP5
97	P81/MTIC5V/TXD2-B	P81/MTIC5V/MTIC5V#/TMCI4/TXD6/ SMOSI6/SSDA6/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/COMP4
98	P80/MTIC5W/RXD2-B	P80/MTIC5W/MTIC5W#/TMRI4/RXD6/ SMISO6/SSCL6/RXD12/SMISO12/SSCL12/ RXDX12/IRQ5/COMP3
99	P11/MTCLKC-B/IRQ1-A	P11/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/TMO3/POE9#/MTIOC9D/ GTIOC3B/GTETRGA/GTIOC3B#/GTETRGC/ GTCPPO0/TOC3/SCK009/SCK008/ TXDB009/IRQ1
100	P10/MTCLKD-B/IRQ0-A	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/TMRI3/POE12#/GTIOC3A/ GTETRGB/GTIOC3A#/GTETRGD/GTIV/ TIC3/CTS6#/RTS6#/SS6#/TXD009/ TXDA009/SMOSI009/SSDA009/IRQ0

3.2 80-Pin Package

Table 3.2 is Comparative Listing of 80-Pin Package Pin Functions, and Table 3.3 is Comparative Listing of 80-Pin (R5F562TxGDFF) Package Pin Functions.

Table 3.2 Comparative Listing of 80-Pin Package Pin Functions

80-Pin	RX62T (80-pin LQFP)	RX26T (80-pin LFQFP)
1	EMLE	EMLE/PN7/MTIOC9D/MTIOC9D#/IRQ5/ADST0
2	VSS	VSS
3	MDE	P00/MTIOC9A/MTIOC9A#/CACREF/GTIU/TIC3/RXD12/SMISO12/SSCL12/RXDX12/RXD009/SMISO009/SSCL009/IRQ2/ADST1/COMP0
4	VCL	VCL
5	MD1	MD/FINED/PN6
6	MD0	P01/MTIOC9C/MTIOC9C#/POE12#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/GTIW/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/TXD009/TXDA009/SMOSI009/SSDA009/IRQ4/ADST2/COMP1
7	PE4/MTCLKC-C/IRQ1-B/POE10#-B	PE4/MTCLKC/MTCLKC#/POE10#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/SCK009/TXDB009/IRQ1
8	PE3/MTCLKD-C/IRQ2-A/POE11#	PE3/MTCLKD/MTCLKD#/POE11#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/CTS009#/RTS009#/SS009#/DE009/IRQ2
9	RES#	RES#
10	XTAL	XTAL/P37/RXD5/SMISO5/SSCL5
11	VSS	VSS
12	EXTAL	EXTAL/P36/TXD5/SMOSI5/SSDA5
13	VCC	VCC
14	PE2/NMI/POE10#-A	PE2/POE10#/NMI/IRQ0
15	PE0/CRX-C	TRST#/PD7/MTIOC9A/MTIOC9A#/TMRI1/TMRI5/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/GTIU/TXD5/SMOSI5/SSDA5/SCK009/TXD008/TXDA008/SMOSI008/SSDA008/TXDB009/SSLA1/SSL01/CTX0/IRQ8
16	PD7/GTIOC0A-B/CTX-C/TRST#	TMS/PD6/MTIOC9C/MTIOC9C#/TMO1/GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/GTIW/CTS1#/RTS1#/SS1#/RXD12/SMISO12/SSCL12/RXDX12/CTS011#/RTS011#/SS011#/DE011/SSLA0/SSL00/IRQ5/ADST0
17	PD6/GTIOC0B-B/TMS	TDI/PD5/TMRI0/TMRI6/GTIOC1A/GTETRGA/GTIOC1A#/GTIOC7A/RXD1/SMISO1/SSCL1/RXD011/SMISO011/SSCL011/SSL00/IRQ6
18	PD5/GTIOC1A-B/RXD1/TDI	TCK/PD4/TMCI0/TMCI6/GTIOC1B/GTETRGB/GTIOC1B#/SCK1/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SCK011/TXDB011/SSL02/IRQ2

80-Pin	RX62T (80-pin LQFP)	RX26T (80-pin LFQFP)
19	PD4/GTIOC1B-B/SCK1/TCK	TDO/PD3/TMO0/GTIOC2A/GTETRGC/GTIOC2A#/GTIOC7B/TXD1/SMOSI1/SSDA1/TXD011/TXDA011/SMOSI011/SSDA011/MOSI0
20	PD3/GTIOC2A-B/TXD1/TDO	PD2/TMCI1/TMO4/GTIOC2B/GTIOC0A/GTIOC2B#/GTIOC0A#/SCK5/SCK008/TXDB008/MOSIA/MOSI0
21	PB7/SCK2-A	PB6/GTIOC2A/GTIOC3A/GTIOC2A#/GTIOC3A#/TOC0/RXD5/SMISO5/SSCL5/RXD12/SMISO12/SSCL12/RXDX12/RXD011/SMISO011/SSCL011/MISO0/CRX0/IRQ2
22	PB6/CRX-A/RXD2-A	PB5/GTIOC2B/GTIOC3B/GTIOC2B#/GTIOC3B#/TIC0/TXD5/SMOSI5/SSDA5/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/TXD011/TXDA011/SMOSI011/SSDA011/RSPCK0/CTX0
23	PB5/CTX-A/TXD2-A	VCC
24	PLLVCC	PB4/POE8#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/GTCPPO0/CTS5#/RTS5#/SS5#/RXD12/SMISO12/SSCL12/RXDX12/CTS011#/RTS011#/SS011#/SCK011/TXDB011/MISOA/SSL01/CRX0/IRQ3
25	PB4/GTETRG/IRQ3/POE8#	VSS
26	PLLVSS	PB3/MTIOC0A/MTIOC0A#/CACREF/GTIU/TOC1/SCK6/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/CTS009#/RTS009#/SS009#/DE009/RSPCKA/CTX0/IRQ9
27	PB3/MTIOC0A-A/SCK0	PB2/MTIOC0B/MTIOC0B#/TMRI0/GTADSM0/GTIOC7A/GTIOC7A#/GTIV/TIC1/TXD6/SMOSI6/SSDA6/SDA0/SDA00/ADSM0
28	PB2/MTIOC0B-A/TXD0/SDA	PB1/MTIOC0C/MTIOC0C#/TMCI0/GTADSM1/GTIOC7B/GTIOC7B#/GTIW/TOC2/RXD6/SMISO6/SSCL6/SCL0/SCL00/IRQ4/ADSM1
29	PB1/MTIOC0C/RXD0/SCL	PB0/MTIOC0D/MTIOC0D#/TMO0/TIC2/TXD6/SMOSI6/SSDA6/TXD008/TXDA008/SMOSI008/SSDA008/CTS011#/RTS011#/SS011#/DE011/MOSIA/MOSI0/IRQ8/ADTRG2#
30	PB0/MTIOC0D/MOSI-B	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/SMISO6/SSCL6/RXD008/SMISO008/SSCL008/MISOA/MISO0/IRQ1/ADTRG1#
31	PA3/MTIOC2A/SSL0-B	PA3/MTIOC2A/MTIOC2A#/TMRI7/GTADSM0/TXD009/TXDA009/SMOSI009/SSDA009/SCK008/TXDB008/SSLA0/SSL00
32	PA2/MTIOC2B/SSL1-B	VCC
33	VCC	P96/POE4#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/GTCPPO4/CTS008#/RTS008#/SS008#/DE008/SSL03/RSPCK0/IRQ4
34	P96/IRQ4/POE4#	VSS

80-Pin	RX62T (80-pin LQFP)	RX26T (80-pin LFQFP)
35	VSS	P95/MTIOC6B/MTIOC1A/MTIOC6B#/ MTIOC1A#/TMCI3/GTIOC4A/GTIOC7A/ GTIOC4A#/GTIOC7A#/GTOUUP/RXD6/ SMISO6/SSCL6/RXD008/SMISO008/ SSCL008/MISOA/SSL02/MISO0/IRQ1/ ADTRG1#
36	P95/MTIOC6B	P94/MTIOC7A/MTIOC2A/MTIOC7A#/ MTIOC2A#/TMRI7/GTIOC5A/GTADSM0/ GTIOC5A#/GTOVUP/TXD009/TXDA009/ SMOSI009/SSDA009/SCK008/TXDB008/ SSLA0/SSL00
37	P94/MTIOC7A	P93/MTIOC7B/MTIOC6A/MTIOC7B#/ MTIOC6A#/TMO4/GTIOC6A/GTIOC6A#/ GTOWUP/TXD009/TXDA009/SMOSI009/ SSDA009/RXD011/SMISO011/SSCL011/ SSLA2/SSL02/MOSI0/CRX0/IRQ14/ ADTRG0#
38	P93/MTIOC7B	P92/MTIOC6D/MTIOC6C/MTIOC6D#/ MTIOC6C#/TMO2/GTIOC4B/GTIOC7B/ GTIOC4B#/GTIOC7B#/GTOULO/SCK009/ TXD011/TXDA011/SMOSI011/SSDA011/ TXDB009/SSLA3/SSL03/MISO0/CTX0
39	P92/MTIOC6D	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC5B#/GTOVLO/RXD5/SMISO5/SSCL5/ RSPCK0
40	P91/MTIOC7C	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC6B#/GTOWLO/TXD5/SMOSI5/ SSDA5/SSL01
41	P76/MTIOC4D/GTIOC2B-A	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC6B/GTIOC2B#/GTIOC6B#/GTOWLO/ SSL03
42	P75/MTIOC4C/GTIOC1B-A	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC5B/GTIOC1B#/GTIOC5B#/GTOVLO/ SSL02
43	P74/MTIOC3D/GTIOC0B-A	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC4B/GTIOC0B#/GTIOC4B#/GTOULO/ SSL01
44	P73/MTIOC4B/GTIOC2A-A	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC6A/GTIOC2A#/GTIOC6A#/GTOWUP/ SSL00
45	P72/MTIOC4A/GTIOC1A-A	P72/MTIOC4A/MTIOC4A#/GTOC1A/ GTIOC5A/GTIOC1A#/GTIOC5A#/GTOVUP/ MOSI0
46	P71/MTIOC3B/GTIOC0A-A	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC4A/GTIOC0A#/GTIOC4A#/GTOUUP/ MISO0
47	P70/IRQ5/POE0#	P70/MTIOC0A/MTCLKC/MTIOC0A#/ MTCLKC#/TMRI6/POE0#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/ GTCPPO0/SCK5/CTS009#/RTS009#/ SS009#/DE009/SSLA0/RSPCK0/IRQ5
48	P33/MTIOC3A/MTCLKA-A/SSL3-A	VCC
49	P32/MTIOC3C/MTCLKB-A/SSL2-A	P31/MTIOC0A/MTCLKC/MTIOC0A#/ MTCLKC#/TMRI6/GTIU/SSLA1/SSL01/IRQ6
50	VCC	VSS

80-Pin	RX62T (80-pin LQFP)	RX26T (80-pin LFQFP)
51	P31/MTIOC0A-B/MTCLKC-A/SSL1-A	P30/MTIOC0B/MTCLKD/MTIOC0B#/ MTCLKD#/TMCI6/GTIV/SCK008/CTS008#/ RTS008#/SS008#/DE008/SSLA0/SSL00/ IRQ7/COMP3
52	VSS	P27/MTIOC1A/MTIOC0C/MTIOC1A#/ MTIOC0C#/TMO2/TMO6/POE9#/RSPCKA/ RSPCK0/IRQ15
53	P30/MTIOC0B-B/MTCLKD-A/SSL0-A	P22/MTIC5W/MTCLKD/MTIC5W#/ MTCLKD#/TMRI2/TMO4/MTIOC9B/GTIV/ RXD12/SMISO12/SSCL12/RXDX12/ RXD008/SMISO008/SSCL008/SCK008/ TXDB008/MISOA/MISO0/CRX0/IRQ10/ ADTRG2#/COMP2
54	P24/RSPCK-A	P21/MTIOC9A/MTCLKA/MTIOC9A#/ MTCLKA#/TMCI4/TMO6/GTIU/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ TXD008/TXDA008/SMOSI008/SSDA008/ MOSIA/MOSI0/IRQ6/AN217/ADTRG1#/ COMP5
55	P23/CTX-B/LTX/MOSI-A	P20/MTIOC9C/MTCLKB/MTIOC9C#/ MTCLKB#/TMRI4/TMO2/GTIW/CTS008#/ RTS008#/SS008#/RXD008/SMISO008/ SSCL008/DE008/RSPCKA/RSPCK0/IRQ7/ AN216/ADTRG0#/COMP4
56	P22/ADTRG#/CRX-B/LRX/MISO-A	P65/IRQ9/AN211/CMPC53/DA1
57	P21/ADTRG1#-B/MTCLKA-B/IRQ6	P64/IRQ8/AN210/CMPC33/DA0
58	P20/ADTRG0#-B/MTCLKB-B/IRQ7	AVCC2
59	AVCC	AVSS2
60	AVSS	P60/IRQ4/AN206/CMPC03
61	P63/AN3	P55/IRQ3/AN203/CMPC32
62	P62/AN2	P54/IRQ2/AN202/CMPC22/CVREFC1
63	P61/AN1	P53/IRQ1/AN201/CMPC12/CVREFC0
64	P60/AN0	P52/IRQ0/AN200/CMPC02
65	P47/AN103/CVREFH	P51/AN205/CMPC52
66	P46/AN102	P50/AN204/CMPC42
67	P45/AN101	P47/AN103
68	P44/AN100	P46/AN102/CMPC50/CMPC51
69	P43/AN003/CVREFL	P45/AN101/CMPC40/CMPC41
70	P42/AN002	P44/AN100/CMPC30/CMPC31
71	P41/AN001	P43/AN003
72	P40/AN000	P42/AN002/CMPC20/CMPC21
73	AVCC0	P41/AN001/CMPC10/CMPC11
74	VREFH0	P40/AN000/CMPC00/CMPC01
75	VREFL0	AVCC1
76	AVSS0	AVCC0
77	P11/MTCLKC-B/IRQ1-A	AVSS0
78	P10/MTCLKD-B/IRQ0-A	AVSS1
79	PA5/ADTRG1#-A/MTIOC1A/MISO-B	P11/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/TMO3/POE9#/MTIOC9D/ GTIOC3B/GTETRGA/GTIOC3B#/GTETRGC/ GTCPPO0/TOC3/SCK009/SCK008/ TXDB009/IRQ1

80-Pin	RX62T (80-pin LQFP)	RX26T (80-pin LFQFP)
80	PA4/ADTRG0#-A/MTIOC1B/RSPCK-B	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/TMRI3/POE12#/GTIOC3A/ GTETRGB/GTIOC3A#/GTETRGD/GTIV/ TIC3/CTS6#/RTS6#/SS6#/TXD009/ TXDA009/SMOSI009/SSDA009/IRQ0

Table 3.3 Comparative Listing of 80-Pin (R5F562TxGDFF) Package Pin Functions

80-Pin	RX62T (80-pin LQFP: R5F562TxGDFF)	RX26T (80-pin LFQFP)
1	EMLE	EMLE/PN7/MTIOC9D/MTIOC9D#/IRQ5/ ADST0
2	VSS	VSS
3	MDE	P00/MTIOC9A/MTIOC9A#/CACREF/GTIU/ TIC3/RXD12/SMISO12/SSCL12/RXDX12/ RXD009/SMISO009/SSCL009/IRQ2/ADST1/ COMP0
4	VCL	VCL
5	MD1	MD/FINED/PN6
6	MD0	P01/MTIOC9C/MTIOC9C#/POE12#/ GTETRGA/GTETRGB/GTETRGC/ GTETRGD/GTIW/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/TXD009/TXDA009/ SMOSI009/SSDA009/IRQ4/ADST2/COMP1
7	PE4/MTCLKC-C/IRQ1-B/POE10#-B	PE4/MTCLKC/MTCLKC#/POE10#/ GTETRGA/GTETRGB/GTETRGC/ GTETRGD/SCK009/TXDB009/IRQ1
8	PE3/MTCLKD-C/IRQ2-A/POE11#	PE3/MTCLKD/MTCLKD#/POE11#/ GTETRGA/GTETRGB/GTETRGC/ GTETRGD/CTS009#/RTS009#/SS009#/ DE009/IRQ2
9	RES#	RES#
10	XTAL	XTAL/P37/RXD5/SMISO5/SSCL5
11	VSS	VSS
12	EXTAL	EXTAL/P36/TXD5/SMOSI5/SSDA5
13	VCC	VCC
14	PE2/NMI/POE10#-A	PE2/POE10#/NMI/IRQ0
15	PD7/GTIOC0A-B/TRST#	TRST#/PD7/MTIOC9A/MTIOC9A#/TMRI1/ TMRI5/GTIOC0A/GTIOC3A/GTIOC0A#/ GTIOC3A#/GTIU/TXD5/SMOSI5/SSDA5/ SCK009/TXD008/TXDA008/SMOSI008/ SSDA008/TXDB009/SSLA1/SSL01/CTX0/ IRQ8
16	PD6/GTIOC0B-B/TMS	TMS/PD6/MTIOC9C/MTIOC9C#/TMO1/ GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/ GTIW/CTS1#/RTS1#/SS1#/RXD12/ SMISO12/SSCL12/RXDX12/CTS011#/ RTS011#/SS011#/DE011/SSLA0/SSL00/ IRQ5/ADST0
17	PD5/GTIOC1A-B/RXD1/TDI	TDI/PD5/TMRI0/TMRI6/GTIOC1A/ GTETRGA/GTIOC1A#/GTIOC7A/RXD1/ SMISO1/SSCL1/RXD011/SMISO011/ SSCL011/SSL00/IRQ6
18	PD4/GTIOC1B-B/SCK1/TCK	TCK/PD4/TMCI0/TMCI6/GTIOC1B/ GTETRGB/GTIOC1B#/SCK1/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SCK011/TXDB011/SSL02/IRQ2
19	PD3/GTIOC2A-B/TXD1/TDO	TDO/PD3/TMO0/GTIOC2A/GTETRGC/ GTIOC2A#/GTIOC7B/TXD1/SMOSI1/ SSDA1/TXD011/TXDA011/SMOSI011/ SSDA011/MOSI0

80-Pin	RX62T (80-pin LQFP: R5F562TxGDFF)	RX26T (80-pin LFQFP)
20	PD2/GTIOC2B-B	PD2/TMCI1/TMO4/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/SCK5/SCK008/ TXDB008/MOSIA/MOSI0
21	PB7/SCK2-A	PB6/GTIOC2A/GTIOC3A/GTIOC2A#/ GTIOC3A#/TOC0/RXD5/SMISO5/SSCL5/ RXD12/SMISO12/SSCL12/RXDX12/ RXD011/SMISO011/SSCL011/MISO0/CRX0/ IRQ2
22	PB6/CRX-A/RXD2-A	PB5/GTIOC2B/GTIOC3B/GTIOC2B#/ GTIOC3B#/TIC0/TXD5/SMOSI5/SSDA5/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ TXD011/TXDA011/SMOSI011/SSDA011/ RSPCK0/CTX0
23	PB5/CTX-A/TXD2-A	VCC
24	PLLVCC	PB4/POE8#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/GTCPPO0/CTS5#/ RTS5#/SS5#/RXD12/SMISO12/SSCL12/ RXDX12/CTS011#/RTS011#/SS011#/ SCK011/TXDB011/MISOA/SSL01/CRX0/ IRQ3
25	PB4/GTETRG/IRQ3/POE8#	VSS
26	PLLVSS	PB3/MTIOC0A/MTIOC0A#/CACREF/GTIU/ TOC1/SCK6/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTS009#/RTS009#/ SS009#/DE009/RSPCKA/CTX0/IRQ9
27	PB3/MTIOC0A-A/SCK0	PB2/MTIOC0B/MTIOC0B#/TMRI0/ GTADSM0/GTIOC7A/GTIOC7A#/GTIV/TIC1/ TXD6/SMOSI6/SSDA6/SDA0/SDA00/ADSM0
28	PB2/MTIOC0B-A/TXD0/SDA	PB1/MTIOC0C/MTIOC0C#/TMCI0/ GTADSM1/GTIOC7B/GTIOC7B#/GTIW/ TOC2/RXD6/SMISO6/SSCL6/SCL0/SCL00/ IRQ4/ADSM1
29	PB1/MTIOC0C/RXD0/SCL	PB0/MTIOC0D/MTIOC0D#/TMO0/TIC2/ TXD6/SMOSI6/SSDA6/TXD008/TXDA008/ SMOSI008/SSDA008/CTS011#/RTS011#/ SS011#/DE011/MOSIA/MOSI0/IRQ8/ ADTRG2#
30	PB0/MTIOC0D	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/ SMISO6/SSCL6/RXD008/SMISO008/ SSCL008/MISOA/MISO0/IRQ1/ADTRG1#
31	PA5/ADTRG1#-A/MTIOC1A	PA3/MTIOC2A/MTIOC2A#/TMRI7/ GTADSM0/TXD009/TXDA009/SMOSI009/ SSDA009/SCK008/TXDB008/SSLA0/SSL00
32	PA3/MTIOC2A	VCC
33	VCC	P96/POE4#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/GTCPPO4/CTS008#/ RTS008#/SS008#/DE008/SSL03/RSPCK0/ IRQ4
34	P96/IRQ4/POE4#	VSS
35	VSS	P95/MTIOC6B/MTIOC1A/MTIOC6B#/ MTIOC1A#/TMCI3/GTIOC4A/GTIOC7A/ GTIOC4A#/GTIOC7A#/GTOUUP/RXD6/ SMISO6/SSCL6/RXD008/SMISO008/ SSCL008/MISOA/SSL02/MISO0/IRQ1/ ADTRG1#

80-Pin	RX62T (80-pin LQFP: R5F562TxGDFF)	RX26T (80-pin LFQFP)
36	P95/MTIOC6B	P94/MTIOC7A/MTIOC2A/MTIOC7A#/ MTIOC2A#/TMRI7/GTIOC5A/GTADSM0/ GTIOC5A#/GTOVUP/TXD009/TXDA009/ SMOSI009/SSDA009/SCK008/TXDB008/ SSLA0/SSL00
37	P94/MTIOC7A	P93/MTIOC7B/MTIOC6A/MTIOC7B#/ MTIOC6A#/TMO4/GTIOC6A/GTIOC6A#/ GTOWUP/TXD009/TXDA009/SMOSI009/ SSDA009/RXD011/SMISO011/SSCL011/ SSLA2/SSL02/MOSI0/CRX0/IRQ14/ ADTRG0#
38	P93/MTIOC7B	P92/MTIOC6D/MTIOC6C/MTIOC6D#/ MTIOC6C#/TMO2/GTIOC4B/GTIOC7B/ GTIOC4B#/GTIOC7B#/GTOULO/SCK009/ TXD011/TXDA011/SMOSI011/SSDA011/ TXDB009/SSLA3/SSL03/MISO0/CTX0
39	P92/MTIOC6D	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC5B#/GTOVLO/RXD5/SMISO5/SSCL5/ RSPCK0
40	P91/MTIOC7C	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC6B#/GTOWLO/TXD5/SMOSI5/ SSDA5/SSL01
41	P90/MTIOC7D	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC6B/GTIOC2B#/GTIOC6B#/GTOWLO/ SSL03
42	P76/MTIOC4D/GTIOC2B-A	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC5B/GTIOC1B#/GTIOC5B#/GTOVLO/ SSL02
43	P75/MTIOC4C/GTIOC1B-A	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC4B/GTIOC0B#/GTIOC4B#/GTOULO/ SSL01
44	P74/MTIOC3D/GTIOC0B-A	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC6A/GTIOC2A#/GTIOC6A#/GTOWUP/ SSL00
45	P73/MTIOC4B/GTIOC2A-A	P72/MTIOC4A/MTIOC4A#/GTOC1A/ GTIOC5A/GTIOC1A#/GTIOC5A#/GTOVUP/ MOSI0
46	P72/MTIOC4A/GTIOC1A-A	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC4A/GTIOC0A#/GTIOC4A#/GTOUUP/ MISO0
47	P71/MTIOC3B/GTIOC0A-A	P70/MTIOC0A/MTCLKC/MTIOC0A#/ MTCLKC#/TMRI6/POE0#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/ GTCPPO0/SCK5/CTS009#/RTS009#/ SS009#/DE009/SSLA0/RSPCK0/IRQ5
48	P70/IRQ5/POE0#	VCC
49	P33/MTIOC3A/MTCLKA-A/SSL3-A	P31/MTIOC0A/MTCLKC/MTIOC0A#/ MTCLKC#/TMRI6/GTIU/SSLA1/SSL01/IRQ6
50	P32/MTIOC3C/MTCLKB-A/SSL2-A	VSS
51	VCC	P30/MTIOC0B/MTCLKD/MTIOC0B#/ MTCLKD#/TMCI6/GTIV/SCK008/CTS008#/ RTS008#/SS008#/DE008/SSLA0/SSL00/ IRQ7/COMP3

80-Pin	RX62T (80-pin LQFP: R5F562TxGDFF)	RX26T (80-pin LFQFP)
52	P31/MTIOC0A-B/MTCLKC-A/SSL1-A	P27/MTIOC1A/MTIOC0C/MTIOC1A#/ MTIOC0C#/TMO2/TMO6/POE9#/RSPCKA/ RSPCK0/IRQ15
53	VSS	P22/MTIC5W/MTCLKD/MTIC5W#/ MTCLKD#/TMRI2/TMO4/MTIOC9B/GTIV/ RXD12/SMISO12/SSCL12/RXDX12/ RXD008/SMISO008/SSCL008/SCK008/ TXDB008/MISOA/MISO0/CRX0/IRQ10/ ADTRG2#/COMP2
54	P30/MTIOC0B-B/MTCLKD-A/SSL0-A	P21/MTIOC9A/MTCLKA/MTIOC9A#/ MTCLKA#/TMCI4/TMO6/GTIU/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ TXD008/TXDA008/SMOSI008/SSDA008/ MOSIA/MOSI0/IRQ6/AN217/ADTRG1#/ COMP5
55	P24/RSPCK-A	P20/MTIOC9C/MTCLKB/MTIOC9C#/ MTCLKB#/TMRI4/TMO2/GTIW/CTS008#/ RTS008#/SS008#/RXD008/SMISO008/ SSCL008/DE008/RSPCKA/RSPCK0/IRQ7/ AN216/ADTRG0#/COMP4
56	P23/CTX-B/LTX/MOSI-A	P65/IRQ9/AN211/CMPC53/DA1
57	P22/ADTRG#/CRX-B/LRX/MISO-A	P64/IRQ8/AN210/CMPC33/DA0
58	P20/ADTRG0#-B/MTCLKB-B/IRQ7	AVCC2
59	AVCC	AVSS2
60	AVSS	P60/IRQ4/AN206/CMPC03
61	P63/AN3	P55/IRQ3/AN203/CMPC32
62	P62/AN2	P54/IRQ2/AN202/CMPC22/CVREFC1
63	P61/AN1	P53/IRQ1/AN201/CMPC12/CVREFC0
64	P60/AN0	P52/IRQ0/AN200/CMPC02
65	P47/AN103/CVREFH	P51/AN205/CMPC52
66	P46/AN102	P50/AN204/CMPC42
67	P45/AN101	P47/AN103
68	P44/AN100	P46/AN102/CMPC50/CMPC51
69	P43/AN003/CVREFL	P45/AN101/CMPC40/CMPC41
70	P42/AN002	P44/AN100/CMPC30/CMPC31
71	P41/AN001	P43/AN003
72	P40/AN000	P42/AN002/CMPC20/CMPC21
73	AVCC0	P41/AN001/CMPC10/CMPC11
74	VREFH0	P40/AN000/CMPC00/CMPC01
75	VREFL0	AVCC1
76	AVSS0	AVCC0
77	P82/MTIC5U/SCK2-B	AVSS0
78	P81/MTIC5V/TXD2-B	AVSS1
79	P80/MTIC5W/RXD2-B	P11/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/TMO3/POE9#/MTIOC9D/ GTIOC3B/GTETRGA/GTIOC3B#/GTETRGC/ GTCPPO0/TOC3/SCK009/SCK008/ TXDB009/IRQ1
80	P10/MTCLKD-B/IRQ0-A	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/TMRI3/POE12#/GTIOC3A/ GTETRGB/GTIOC3A#/GTETRGD/GTIV/ TIC3/CTS6#/RTS6#/SS6#/TXD009/ TXDA009/SMOSI009/SSDA009/IRQ0

3.3 64-Pin Package

Table 3.4 is Comparative Listing of 64-Pin Package Pin Functions.

Table 3.4 Comparative Listing of 64-Pin Package Pin Functions

64-Pin	RX62T (64-pin LQFP)	RX26T (64-pin LFQFP)
1	EMLE	EMLE/PN7/MTIOC9D/MTIOC9D#/IRQ5/ ADST0
2	MDE	P00/MTIOC9A/MTIOC9A#/CACREF/GTIU/ TIC3/RXD12/SMISO12/SSCL12/RXDX12/ RXD009*1/SMISO009*1/SSCL009*1/IRQ2/ ADST1*1/COMP0
3	VCL	VCL
4	MD1	MD/FINED/PN6
5	MD0	P01/MTIOC9C/MTIOC9C#/POE12#/ GTETRGA/GTETRGB/GTETRGC/ GTETRGD/GTIW/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/TXD009*1/TXDA009*1/ SMOSI009*1/SSDA009*1/IRQ4/ADST2/ COMP1
6	RES#	RES#
7	XTAL	XTAL/P37/RXD5/SMISO5/SSCL5
8	VSS	VSS
9	EXTAL	EXTAL/P36/TXD5/SMOSI5/SSDA5
10	VCC	VCC
11	PE2/NMI/POE10#-A	PE2/POE10#/NMI/IRQ0
12	PD7/GTIOC0A-B/TRST#	TRST#/PD7/MTIOC9A/MTIOC9A#/TMRI1/ TMRI5/GTIOC0A/GTIOC3A/GTIOC0A#/ GTIOC3A#/GTIU/TXD5/SMOSI5/SSDA5/ SCK009*1/TXD008*1/TXDA008*1/ SMOSI008*1/SSDA008*1/TXDB009*1/SSLA1/ SSL01*1/CTX0/IRQ8
13	PD6/GTIOC0B-B/TMS	TMS/PD6/MTIOC9C/MTIOC9C#/TMO1/ GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/ GTIW/CTS1#/RTS1#/SS1#/RXD12/ SMISO12/SSCL12/RXDX12/CTS011#*1/ RTS011#*1/SS011#*1/DE011*1/SSLA0/ SSL00*1/IRQ5/ADST0
14	PD5/GTIOC1A-B/RXD1/TDI	TDI/PD5/TMRI0/TMRI6/GTIOC1A/ GTETRGA/GTIOC1A#/GTIOC7A/RXD1/ SMISO1/SSCL1/RXD011*1/SMISO011*1/ SSCL011*1/SSL00*1/IRQ6
15	PD4/GTIOC1B-B/SCK1/TCK	TCK/PD4/TMCI0/TMCI6/GTIOC1B/ GTETRGB/GTIOC1B#/SCK1/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SCK011*1/TXDB011*1/SSL02*1/IRQ2
16	PD3/GTIOC2A-B/TXD1/TDO	TDO/PD3/TMO0/GTIOC2A/GTETRGC/ GTIOC2A#/GTIOC7B/TXD1/SMOSI1/ SSDA1/TXD011*1/TXDA011*1/SMOSI011*1/ SSDA011*1/MOSI0*1
17	PB7/SCK2-A	PB6/GTIOC2A/GTIOC3A/GTIOC2A#/ GTIOC3A#/TOC0/RXD5/SMISO5/SSCL5/ RXD12/SMISO12/SSCL12/RXDX12/ RXD011*1/SMISO011*1/SSCL011*1/MISO0*1/ CRX0/IRQ2

64-Pin	RX62T (64-pin LQFP)	RX26T (64-pin LFQFP)
18	PB6/CRX-A/RXD2-A	PB5/GTIOC2B/GTIOC3B/GTIOC2B#/ GTIOC3B#/TIC0/TXD5/SMOSI5/SSDA5/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ TXD011*1/TXDA011*1/SMOSI011*1/ SSDA011*1/RSPCK0*1/CTX0
19	PB5/CTX-A/TXD2-A	PB4/POE8#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/GTCPPO0/CTS5#/ RTS5#/SS5#/RXD12/SMISO12/SSCL12/ RXDX12/CTS011#*1/RTS011#*1/SS011#*1/ SCK011*1/TXDB011*1/MISOA/SSL01*1/ CRX0/IRQ3
20	PLLVCC	PB3/MTIOC0A/MTIOC0A#/CACREF/GTIU/ TOC1/SCK6/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTS009#*1/RTS009#*1/ SS009#*1/DE009*1/RSPCKA/CTX0/IRQ9
21	PB4/GTETRG/IRQ3/POE8#	PB2/MTIOC0B/MTIOC0B#/TMRI0/ GTADSM0/GTIOC7A/GTIOC7A#/GTIV/TIC1/ TXD6/SMOSI6/SSDA6/SDA0/SDA00*1/ ADSM0
22	PLLVSS	PB1/MTIOC0C/MTIOC0C#/TMCI0/ GTADSM1/GTIOC7B/GTIOC7B#/GTIW/ TOC2/RXD6/SMISO6/SSCL6/SCL0/SCL00*1/ IRQ4/ADSM1
23	PB3/MTIOC0A-A/SCK0	PB0/MTIOC0D/MTIOC0D#/TMO0/TIC2/ TXD6/SMOSI6/SSDA6/TXD008*1/ TXDA008*1/SMOSI008*1/SSDA008*1/ CTS011#*1/RTS011#*1/SS011#*1/DE011*1/ MOSIA/MOSI0*1/IRQ8/ADTRG2#
24	PB2/MTIOC0B-A/TXD0/SDA	VCC
25	PB1/MTIOC0C/RXD0/SCL	P96/POE4#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/GTCPPO4/ CTS008#*1/RTS008#*1/SS008#*1/DE008*1/ SSL03*1/RSPCK0*1/IRQ4
26	PB0/MTIOC0D/MOSI-B	VSS
27	PA3/MTIOC2A/SSL0-B	P95/MTIOC6B/MTIOC1A/MTIOC6B#/ MTIOC1A#/TMCI3/GTIOC4A/GTIOC7A/ GTIOC4A#/GTIOC7A#/GTOUUP/RXD6/ SMISO6/SSCL6/RXD008*1/SMISO008*1/ SSCL008*1/MISOA/SSL02*1/MISO0*1/IRQ1/ ADTRG1#*1
28	PA2/MTIOC2B/SSL1-B	P94/MTIOC7A/MTIOC2A/MTIOC7A#/ MTIOC2A#/TMRI7/GTIOC5A/GTADSM0/ GTIOC5A#/GTOVUP/TXD009*1/TXDA009*1/ SMOSI009*1/SSDA009*1/SCK008*1/ TXDB008*1/SSLA0/SSL00*1
29	P94/MTIOC7A	P93/MTIOC7B/MTIOC6A/MTIOC7B#/ MTIOC6A#/TMO4/GTIOC6A/GTIOC6A#/ GTOWUP/TXD009*1/TXDA009*1/ SMOSI009*1/SSDA009*1/RXD011*1/ SMISO011*1/SSCL011*1/SSLA2/SSL02*1/ MOSI0*1/CRX0/IRQ14/ADTRG0#

64-Pin	RX62T (64-pin LQFP)	RX26T (64-pin LFQFP)
30	P93/MTIOC7B	P92/MTIOC6D/MTIOC6C/MTIOC6D#/ MTIOC6C#/TMO2/GTIOC4B/GTIOC7B/ GTIOC4B#/GTIOC7B#/GTOULO/SCK009*1/ TXD011*1/TXDA011*1/SMOSI011*1/ SSDA011*1/TXDB009*1/SSLA3/SSL03*1/ MISO0*1/CTX0
31	P92/MTIOC6D	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC5B#/GTOVLO/RXD5/SMISO5/SSCL5/ RSPCK0*1
32	P91/MTIOC7C	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC6B#/GTOWLO/TXD5/SMOSI5/ SSDA5/SSL01*1
33	P76/MTIOC4D/GTIOC2B-A	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC6B/GTIOC2B#/GTIOC6B#/GTOWLO/ SSL03*1
34	P75/MTIOC4C/GTIOC1B-A	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC5B/GTIOC1B#/GTIOC5B#/GTOVLO/ SSL02*1
35	P74/MTIOC3D/GTIOC0B-A	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC4B/GTIOC0B#/GTIOC4B#/GTOULO/ SSL01*1
36	P73/MTIOC4B/GTIOC2A-A	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC6A/GTIOC2A#/GTIOC6A#/GTOWUP/ SSL00*1
37	P72/MTIOC4A/GTIOC1A-A	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC5A/GTIOC1A#/GTIOC5A#/GTOVUP/ MOSI0*1
38	P71/MTIOC3B/GTIOC0A-A	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC4A/GTIOC0A#/GTIOC4A#/GTOUUP/ MISO0*1
39	P70/IRQ5/POE0#	P70/MTIOC0A/MTCLKC/MTIOC0A#/ MTCLKC#/TMRI6/POE0#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/ GTCPPO0/SCK5/CTS009#*1/RTS009#*1/ SS009#*1/DE009*1/SSLA0/RSPCK0*1/IRQ5
40	P33/MTIOC3A/MTCLKA-A/SSL3-A	VCC
41	P32/MTIOC3C/MTCLKB-A/SSL2-A	VSS
42	VCC	P22/MTIC5W/MTCLKD/MTIC5W#/ MTCLKD#/TMRI2/TMO4/MTIOC9B/GTIV/ RXD12/SMISO12/SSCL12/RXDX12/ RXD008*1/SMISO008*1/SSCL008*1/ SCK008*1/TXDB008*1/MISOA/MISO0*1/ CRX0/IRQ10/ADTRG2#/COMP2
43	P31/MTIOC0A-B/MTCLKC-A/SSL1-A	P21/MTIOC9A/MTCLKA/MTIOC9A#/ MTCLKA#/TMCI4/TMO6/GTIU/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ TXD008*1/TXDA008*1/SMOSI008*1/ SSDA008*1/MOSIA/MOSI0*1/IRQ6/AN217/ ADTRG1#*1/COMP5
44	VSS	P20/MTIOC9C/MTCLKB/MTIOC9C#/ MTCLKB#/TMRI4/TMO2/GTIW/CTS008#*1/ RTS008#*1/SS008#*1/RXD008*1/ SMISO008*1/SSCL008*1/DE008*1/ RSPCKA/RSPCK0*1/IRQ7/AN216/ADTRG0#/ COMP4

64-Pin	RX62T (64-pin LQFP)	RX26T (64-pin LFQFP)
45	P30/MTIOC0B-B/MTCLKD-A/SSL0-A	P65/IRQ9/AN211/CMPC53/DA1
46	P24/RSPCK-A	P64/IRQ8/AN210/CMPC33*1/CMPC52*2/DA0
47	P23/CTX-B/LTX/MOSI-A	AVCC2
48	P22/CRX-B/LRX/MISO-A	AVSS2
49	P47/AN103/CVREFH	P54/IRQ2/AN202/CMPC22/CVREFC1
50	P46/AN102	P53/IRQ1/AN201/CMPC12/CVREFC0
51	P45/AN101	P52/IRQ0/AN200/CMPC02
52	P44/AN100	P47/AN103*1/AN206*2/CMPC03*2
53	P43/AN003/CVREFL	P46/AN102*1/AN006*2/CMPC50*1/ CMPC51*1/CMPC21*2
54	P42/AN002	P45/AN101*1/AN005*2/CMPC40*1/ CMPC41*1/CMPC11*2
55	P41/AN001	P44/AN100*1/AN004*2/CMPC30*1/ CMPC31*1/CMPC01*2
56	P40/AN000	P43/AN003/CMPC23*2/CMPC50*2
57	AVCC0	P42/AN002/CMPC20/CMPC21*1
58	VREFH0	P41/AN001/CMPC10/CMPC11*1
59	VREFL0	P40/AN000/CMPC00/CMPC01*1/CMPC13*2
60	AVSS0	AVCC1*1/NC*2
61	P11/MTCLKC-B/IRQ1-A	AVCC0
62	P10/MTCLKD-B/IRQ0-A	AVSS0
63	PA5/ADTRG1#-A/MTIOC1A/MISO-B	AVSS1*1/NC*2
64	PA4/ADTRG0#-A/MTIOC1B/RSPCK-B	P11/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/TMO3/POE9#/MTIOC9D/ GTIOC3B/GTETRGA/GTIOC3B#/GTETRGC/ GTCPPO0/TOC3/SCK009*1/SCK008*1/ TXDB009*1/IRQ1

Notes: 1. There is no product whose RAM size is 48 KB.
2. There is no product whose RAM size is 64 KB.

4. Important Information when Migrating Between MCUs

This section presents important information on differences between the RX26T Group and the RX62T Group.

4.1, Notes on Pin Design presents notes regarding hardware. 4.2, Notes on Functional Design presents notes regarding software.

4.1 Notes on Pin Design

4.1.1 VCL Pin (External Capacitor)

When connecting a smoothing capacitor to the VCL pin to stabilize the internal power supply, select a capacitor rated at 0.1 µF for the RX62T Groups, and 0.47 µF on the RX26T Group.

4.1.2 Method of Inputting External Clock

On the RX62T Group, when inputting an external clock, the counter phase of the clock input to the EXTAL pin is allowed to be input to the XTAL pin. However, note that this is not allowed for the RX26T Group.

4.1.3 Main Clock Oscillator

When connecting an oscillator to the EXTAL or XTAL pin of the RX26T Group, use an oscillator whose resonator frequency is 8 MHz to 24 MHz.

4.1.4 Transition to Boot Mode (FINE Interface)

In the RX26T Group, transition to boot mode (FINE interface) is made if reset cancellation is made when the MD pin is Low and then it is switched to High after 20 to 100 ms.

For further information on operation modes, refer to the RX26T Group User's Manual: Hardware listed in section 5, Reference Documents.

4.1.5 Mode Setting Pins

The mode setting pins at the time of reset cancellation are only the MD pin for the RX26T Group, and the MD1 and MD0 pins for the RX62T Group.

4.1.6 PLLVCC Pin

The RX26T Group does not have the PLLVCC pin.

4.1.7 Capacitors Connected to Analog Power Supply Pins

When using an A/D conversion clock frequency higher than 40 MHz on the RX26T Group, add a 0.01 µF-capacitor between the 0.1 µF capacitor and the power supply pin.

4.2 Notes on Functional Design

Some software that runs on the RX62T Group is compatible with the RX26T Group. Nevertheless, appropriate caution must be exercised due to differences in aspects such as operation timing and electrical characteristics.

This section describes software-related considerations regarding function settings that differ between the RX26T Group and RX62T Group.

For differences between modules and functions, see section 2, Comparative Overview of Specifications. For further information, refer to the User's Manual: Hardware listed in section 5, Reference Documents.

4.2.1 Changing the Option-Setting Memory Though Self-Programming

In the RX26T Group, when changing the option setting memory through self-programming, use the configuration setting command to program the option setting memory to the configuration setting area.

For details on the configuration setting command, refer to the RX26T Group User's Manual: Hardware listed in section 5, Reference Documents.

4.2.2 Software Configurable Interrupt

On the RX62T Group, the interrupt sources have fixed vector numbers, but on the RX26T Group, the MTU, GPTW, RSPI, RSCI, and CANFD interrupt sources are classified as software configurable interrupt A and set in software configurable interrupt A source select register n (SLIARn), allowing interrupt sources to be allocated to 208 to 255 in the interrupt vector table.

4.2.3 Transfer of firmware to FCU RAM

In order to use the FCU command, the RX62T Group needs the firmware for FCU to be stored in FCU RAM, but the RX26T Group does not require it.

4.2.4 Using Flash Memory Commands

On the RX62T Group, programming and erasing of the flash memory is accomplished by first transitioning to the dedicated sequencer mode for ROM programming and erasing and then issuing software commands. On the RX26T Group, programming and erasing of the flash memory is accomplished by setting FACI commands in the FACI command-issuing area to control the FCU.

Table 4.1 is Comparison of Specifications of FCU Command and FACI Command.

Table 4.1 Comparison of Specifications of FCU Command and FACI Command

Item	FCU command (RX62T)	FACI command (RX26T)
Command-issuing area	Address for writing and erasure (0010 0000h to 0010 7FFFh) (In the case of 32 KB) (0010 0000h to 0010 1FFFh) (In the case of 8 KB)	FACI command issuing area (007E 0000h)

Item	FCU command (RX62T)	FACI command (RX26T)
Usable commands	• Transition to P/E normal mode • Transition to status read mode • Transition to lock bit read mode • Programming • Block erase • P/E suspend • P/E resume • Status register clear • Blank check • Lock bit read 2 • Lock bit programming	• Programming • Block erase • P/E suspend • P/E resume • Status clear • Forced stop • Blank check • Configuration setting

4.2.5 Clock Frequency Settings

The restrictions on clock frequency settings differ between the RX62T Group and RX26T Group.

For details, see Table 4.2.

Table 4.2 Comparison of Restrictions on Clock Frequency Settings

Item	FCU command (RX62T)	FACI command (RX26T)
Restrictions on clock frequency settings	ICLK ≥ PCLK	PCLKC ≥ PCLKA ≥ PCLKB
Clock frequency setting restrictions when using CANFD	—	PCLKB:PCLKB = 2:1 PCLKB ≥ CANFDCLK PCLKB ≥ CANFDMCLK
Clock frequency ratio restrictions	—	ICLK:FCLK = N:1 or 1:N ICLK:PCLKA = N:1 or 1:N ICLK:PCLKB = N:1 or 1:N ICLK:PCLKC = N:1 or 1:N ICLK:PCLKD = N:1 or 1:N PCLKA:PCLKC = 1:1 or 1:2 PCLKB:PCLKD = 1:1 or 2:1 or 4:1 or 1:2

4.2.6 RIIC Operating Voltage Setting

When using the RIIC on the RX26T Group, it is necessary to specify the power supply voltage range to preserve the slope characteristics. VCC is set to a value of 4.5 V or greater by default. If it is set to a value less than 4.5 V, make sure to change the voltage range before activating the RIIC.

For details, refer to the description of the VOLSR.RICVLS bit in RX26T Group User's Manual: Hardware.

4.2.7 Voltage Level Setting

On the RX26T Group, the operating mode setting in the voltage level setting register (VOLSR), the voltage detection circuit setting in the voltage detection level select register (LVDLVLR), and the option-setting memory setting in the option function select register 1 (OFS1) need to be changed as appropriate to match the operating voltage. Use a program to set these values.

4.2.8 Option-Setting Memory

On the RX62T Group, the ID code protection codes and ID code protection codes for the on-chip debugger are located in the ROM, but on the RX26T Group, they are located in the option-setting memory. Note that the setting configuration procedures are different.

4.2.9 Main Clock Oscillator

On the RX62T Group, the main clock starts oscillation after reset cancellation. On the RX26T Group, however, a program is required to start the main clock oscillation because operation is made by the LOCO clock after reset cancellation.

4.2.10 PLL Circuit

The frequency multiplication factor of the PLL circuit is ×8 on the RX62T Group and ×10 to ×30 (in ×0.5 increments) on the RX26T Group. To use the PLL circuit, change the setting of the PLLCR.STC bits to an appropriate value. Also, on the RX26T Group, use a program to switch the PLL clock.

4.2.11 MTU/GPTW Operating Frequency

On the RX26T Group, the PCLKC is used as the MTU/GPTW count clock, and PCLKA is used as the bus clock. Note that limitations apply regarding the usable frequency combinations.

4.2.12 DMAC Activation by MTU

When the DMAC is activated by the MTU on the RX26T Group, the activation source is cleared when the DMAC requests ownership of the internal bus. Accordingly, the state of the internal bus may delay the start of a DMAC transfer, even if the activation source has been cleared.

4.2.13 Exception Vector Table

On the RX62T Group, the vector table is allocated at a fixed address. On the RX26T Group, the vector table allocation address is configurable and the start address is set in the exception table register (EXTB).

4.2.14 Endian

On the RX62T Group, endian setting is made by the MDE pin, but on the RX26T Group, endian setting is made by the MDE register allocated in the option-setting memory.

4.2.15 Register Write Protection Function

For the RX26T Group, the register write protection function has been added to prevent important registers from being rewritten when a program runs out of control. Important registers are protected in the initial setting. When using a protected function, change the protection bit of the function.

4.2.16 Priority Order of Buses

On the RX62T Group, the priority order of buses is internal main bus 2 > internal main bus 1, and this order is fixed. On the RX26T Group, the priority order is configurable by the bus priority control register (BUSPRI).

4.2.17 Pin Allocation Function

On the RX62T Group, the port function register, explained in the section of I/O Ports, allocates pins to module functions corresponding to the register. On the RX26T Group, the pin function control register, explained in the section of Multi-pin Function Controller, allocates a module function from among multiple modules to each pin corresponding to the register. The pin function control register is protected by the write protect register. To rewrite the register, cancel the protection.

4.2.18 Independent Watchdog Timer

On the RX62T Group, the independent watchdog timer can only be reset, but on the RX26T Group, either reset or interrupt (maskable interrupt or non-maskable interrupt) can be selected.

4.2.19 Performing RAM Self-Diagnostics on Save Register Banks

On the RX26T Group save register banks are configured in the RAM. The save register banks are provided with a buffer, so when a SAVE instruction is used to write data to a register and then a RSTR instruction is used to read data from the same register, the data is actually read from the buffer and not from the RAM memory cells. When performing self-diagnostics on the RAM in a save register bank, use the following sequence of steps for checking the written data in order to prevent the data from being read from the buffer:

(1) Use the SAVE instruction to write data to the bank that is the target of the diagnostic test.
(2) Use the SAVE instruction to write data to a bank other than that written to in step 1.
(3) Use the RSTR instruction to read data from the bank written to in step 1.

4.2.20 Restrictions on Compare Function

The compare function of the 12-bit A/D converter on the RX26T Group is subject to the following restrictions.

(1) The compare function cannot be used together with the self-diagnosis function or double trigger mode. (The compare function is not available for the ADRD, ADDBLDR, ADDBLDRA, and ADDBLDRB registers.)
(2) It is necessary to specify single scan mode when using match or mismatch event outputs.
(3) When the temperature sensor or internal reference voltage is selected for window A, window B operations are disabled.
(4) When the temperature sensor or internal reference voltage is selected for window B, window A operations are disabled.
(5) It is not possible to set the same channel for window A and window B.
(6) It is necessary to set the reference voltage values such that the high-side reference voltage value is equal to or larger than the low-side reference voltage value.

4.2.21 Eliminating I^2C Bus Interface Noise

The RX62T Group has integrated analog noise filters on the SCL and SDA lines, but the RX26T Group has no integrated analog noise filters.

4.2.22 Buffer Register Setting Values in Complementary PWM Mode

On the RX62T Group, when the double buffer function is used in complementary PWM mode of multi-function timer pulse unit 3, set buffer registers (MTU3.TGRE, MTU4.TGRE, and MTU4.TGRF) to "PWM-output duty value - 1". On the RX26T Group, set buffer registers to "PWM-output duty value".

4.2.23 Control When a Port Output Enable 3 Output Stop Request Is Generated

When an output stop request is generated on the RX26T group, the pins for which the corresponding bit is set to 1 in the POECR1 to POECR3 and POECR7 registers are placed in the high-impedance state, and the pins for which the corresponding bit is set to 1 in the PMMCR0 to PMMCR2 registers are switched to the general I/O port.

If both bits are set to 1 for the same pin, the settings on the POECR1 to POECR3 and POECR7 registers have priority and the pin is placed in the high-impedance state. After switching to the general I/O port, the pin status is determined by the settings on the PDR and PODR registers.

The corresponding bits in the POECRn registers (n = 0 to 3) should be cleared to 0 beforehand.

4.2.24 Comparator C Operation with 12-Bit A/D Converter in Module Stop Mode

On the RX26T Group, the programmable gain amplifier (PGA) and 12-bit A/D converter are controlled by the same module stop signal, so it is not possible to compare the following PGA outputs when the 12-bit A/D converter is in the module stop state:

- AN000 pin PGA output
- AN001 pin PGA output
- AN002 pin PGA output
- AN100 pin PGA output
- AN101 pin PGA output
- AN102 pin PGA output

It is not possible to compare the following analog pins when the 12-bit A/D converter is in the module stop state:

- AN000 pin
- AN001 pin
- AN002 pin
- AN100 pin
- AN101 pin
- AN102 pin

4.2.25 Operation of Main Clock Oscillation Stop Detection Function

The oscillation stop detection function detects the stoppage of the main clock oscillator, and supplies a low-speed clock of the low-speed on-chip oscillator as the clock source of the system clock, instead of the main clock.

On the RX26T Group, note that the system clock does not switch to the LOCO clock at the detection of oscillation stoppage of the main clock if the HOCO clock is selected as the clock source of PLL and the PLL clock is selected as the clock source of the system clock.

4.2.26 Initialization of Port Direction Register (PDR)

The method of initializing the PDR register differs between the RX62T Group and RX26T Group, even on products with the same pin count.

4.2.27 Output Level of MTIOC Pin When Counter Is Stopped

When the MTIOC pin operates in output mode, the counter stops when "0" is written in the CSTn bit of TSTRA or TSTR. At that time, in complementary PWM mode or reset-synchronized PWM mode of the RX26T Group, the MTIOC pin outputs the initial output level configured by the TOCR1A or TOCR2A register.

The output compare output level of the MTIOC pin is retained in a mode other than the complementary PWM mode and the reset-synchronized PWM mode. When the CSTn bit is "0", writing a value in the TIOR register updates the output level of the pin to the configured initial output value.

4.2.28 Pulse Width of Count Clock Source

The pulse width of the MTU's count clock source differs between the RX62T Group and RX26T Group. For details, see Table 4.2. Correct operation cannot be achieved if the pulse width is less than the appropriate value listed below.

Table 4.3 Comparison of Count Clock Source Pulse Widths

Item		RX62T	RX26T
Single edge		3 states or more	1.5 or more PCLKC cycles
Both edges		5 states or more	2.5 or more PCLKC cycles
Phase counting mode	Phase difference and overlap	3 states or more	1.5 or more PCLKC cycles
	Pulse width	5 states or more	2.5 or more PCLKC cycles

4.2.29 Generation of A/D Scan Conversion End Interrupt

On the RX26T Group, if scan starts by a software trigger, A/D scan conversion end interrupt is generated if the ADCSR.ADIE bit is "1" at the time of scan end, even if the double trigger mode has been selected.

4.2.30 Scan Conversion Time of 12-Bit A/D Converter

The scan conversion times differ between the RX62T Group and RX26T Group. When the number of selected channels is n, the scan conversion time (t_{SCAN}) of single scan for these groups is expressed in the formulas below. For details, refer to the User's Manual: Hardware of the RX62T and RX26T Groups listed in 5, Reference Documents to learn the sampling time and the scan conversion time for analog input of the 12-bit A/D converter.

RX62T: **(1) For AN000 to AN002 and AN100 to AN102**

- When the channel-dedicated sample-and-hold circuit is not used and self-diagnosis is not used
  $t_{SCAN} = t_D + (t_{CONV} \times n) + t_{ED}$
- When the channel-dedicated sample-and-hold circuit is not used and self-diagnosis is used
  $t_{SCAN} = t_D + t_{DIAG} + (t_{CONV} \times n) + t_{ED}$
- When the channel-dedicated sample-and-hold circuit is used and self-diagnosis is not used
  $t_{SCAN} = t_D + t_{SPLSH} + (t_{CONV} \times n) + t_{ED}$
- When the channel-dedicated sample-and-hold circuit is used and self-diagnosis is used
  $t_{SCAN} = t_D + t_{SPLSH} + t_{DIAG} + (t_{CONV} \times n) + t_{ED}$

(2) For AN003 and AN103

- When self-diagnosis is not used
  $t_{SCAN} = t_D + (t_{CONV} \times n) + t_{ED}$
- When self-diagnosis is used
  $t_{SCAN} = t_D + t_{DIAG} + (t_{CONV} \times n) + t_{ED}$

RX26T: $t_{SCAN} = t_D + t_{SPLSH} + (t_{DIS} \times n) + t_{DIAG} + (t_{CONV} \times n) + t_{ED}$
t_{SCAN} (temperature sensor output, at the time of internal reference voltage conversion)
$= t_D + (t_{ADIS} \times m) + (t_{CONV} \times m) + t_{ED}$

t_D	Scan conversion start delay time
t_{SPLSH}	Channel-dedicated sample-and-hold circuit sampling time
t_{SPL}	Sampling time
t_{DIS}	Disconnection detection assist processing time
t_{DIAG}	Self-diagnosis conversion time
t_{CONV}	A/D conversion processing time
t_{ED}	Scan conversion end delay time
t_{ADIS}	Auto discharge processing time for A/D conversion of the temperature sensor output and the internal reference voltage

4.2.31 Comparator C Operation in Module Stop State

On the RX26T Group, if the module stop state takes place when comparator C is operating, the analog circuit of comparator C does not stop, so that the current of the analog power supply stays the same as when comparator C is used. If the analog power supply current needs to be lowered in the module stop state, set the CMPCTL.HCMPON bit to "0" to stop comparator C.

4.2.32 Operation of Comparator C in Software Standby Mode

On the RX26T Group, if the software standby mode takes place when comparator C is operating, the analog circuit of comparator C does not stop, so that the current of the analog power supply stays the same as when comparator C is used. If the analog power supply current needs to be lowered in the software standby mode, set the CMPCTL.HCMPON bit to "0" to stop comparator C.

4.2.33 Note on General I/O Port Switching Using POE3

When an output disabling request specified by the POE3 is generated on the RX26T Group, pins for which the corresponding bits in the PMMCRn registers (n = 0 to 3) are set to 1 are switched to general I/O port pins. The corresponding bits in the POECRn registers (n = 0 to 3) should be cleared to 0 beforehand.

4.2.34 Timer Mode Register Setting for ELC Event Input

To set the MTU to ELC action operation on the RX26T Group, set the timer mode register (TMDR) of the relevant channel to its initial value (00h).

4.2.35 Active Level Setting for MTU/GPTW Inverted Output

On the RX26T Group, either normal output or inverted output can be selected for MTU and GPTW outputs by making settings in the MPC.PmnPFS registers.

When MTU inverted output is selected, the active level specified in the MTU.TOCR1j and MTU.TOCR2j registers (j = A or B) and the active level of the signals output to the pins are inverted. To use output short detection in this case, specify active levels in the ALR1 and ALR2 registers based on the signals actually output to the pins.

When GPTW inverted output is selected, the active level of the signals output to the pins is inverted. To use output short detection in this case, specify active levels in the ALR3 to ALR5 registers based on the signals actually output to the pins.

4.2.36 Note on Using Both POE and POEG

When using the POE and POEG together on the RX26T Group, do not use both the POE and POEG to control output disabling for the same GPTW output pins.

4.2.37 Reading Pins in High-Impedance State

When pins are put into the high-impedance state by the POE on the RX26T Group, the level of those pins cannot be read. The value when read is undefined. To read the level of the pins, release them from the high-impedance state.

This restriction does not apply when port switching control is selected instead of high-impedance control.

5. Reference Documents

User's manuals: Hardware

RX62T Group User’s Manual: Hardware Rev.1.10 (R01UH0520EJ0110)
(The latest version can be downloaded from the Renesas Electronics website.)

RX26T Group User’s Manual: Hardware Rev.1.01 (R01AN6752EJ0101)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical updates and technical news
(The latest information can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This module reflects the content of the following technical updates:

TN-RX*-A0231A/E
TN-RX*-A185B/E
TN-RX*-A185A/E
TN-RX*-A193A/E
TN-RX*-A161A/E
TN-RX*-A152A/E
TN-RX*-A121A/E
TN-RX*-A119A/E
TN-RX*-A099A/E
TN-RX*-A098A/E
TN-RX*-A096A/E
TN-RX*-A095A/E
TN-RX*-A094A/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jan.27.23	—	First edition issued
1.01	Sep.27.23	125	Modified typos

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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