RX23E-B Group, RX23E-A Group

Differences Between the RX23E-B Group and the RX23E-A Group

Introduction

This application note is intended as a reference to points of difference between the peripheral modules, I/O registers, and pin functions of the RX23E-B Group and RX23E-A Group, as well as a guide to key points to consider when migrating between the two groups.

Unless specifically otherwise noted, the information in this application note applies to the 48-pin package versions of the RX23E-B Group and RX23E-A Group. To confirm the differences in electrical specifications, usage notes, and setting procedures, refer to the User's Manual: Hardware for the product in question.

Target Device

RX23E-B Group and RX23E-A Group

Contents

1. Comparison of Built-In Functions of RX23E-B Group and RX23E-A Group

A comparison of the built-in functions of the RX23E-B Group and RX23E-A Group is provided below. For details of the functions, refer to section 2, Comparative Overview of Specifications and section 5, Reference Documents.

Table 1.1 is Comparison of Built-In Functions of RX23E-A Group and RX23E-B Group.

Table 1.1 Comparison of Built-In Functions of RX23E-A Group and RX23E-B Group

Function	RX23E-A	RX23E-B
CPU	○	
Operating Mode	○	
Address Space	○	
Reset	○	
Option-Setting Memory (OFSM)	○	
Voltage Detection Circuit (LVDAb)	●	
Clock generation circuit	●	
Clock Frequency Accuracy Measurement Circuit (CAC)	●	
Low power consumption	●/▲	
Register write protection function	●	
Exception Handling	○	
Interrupt controller (ICUb)	●	
Buses	●/▲	
Memory-Protection Unit (MPU)	○	
DMA Controller (DMACA)	○	
Data Transfer Controller (DTCa)	○	
Event Link Controller (ELC)	●/■	
I/O ports	●/▲	
Multi-Function Pin Controller (MPC)	●/▲/■	
Multi-function timer pulse unit 2 (MTU2a)	○	
Port Output Enable 2 (POE2a)	○	
8-bit Timer (TMRa)	○	
Compare Match Timer (CMT)	○	
Realtime Clock (RTCc)	×	○
Low-Power Timer (LPT)	●	
Independent Watchdog Timer (IWDTa)	○	
Serial Communication Interface (SCIg and SCIh)	●	
I^2C Bus Interface (RIICa)	○	
CAN Module (RSCAN)	○	
Serial Peripheral Interface (RSPIb for RX23E-A and RSPIc for RX23E-B)	●/▲	
CRC Calculator (CRC)	○	
LCD Controller/Driver (LCDC)	×	○
Analog Front-End (AFE for RX23E-A and AFEA for RX23E-B)	●/▲/■	
24-Bit Delta-Sigma A/D Converter (DSADA for RX23E-A and DSADB for RX23E-B)	●/▲/■	
12-Bit A/D Converter (S12ADE)	●	
16-Bit D/A Converter (R16DA)	×	○
Data Operation Circuit (DOC)	○	
RAM	○	
Flash Memory (FLASH)	○	
Packages	●	

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Only differences in register specifications are listed.

2.1 Voltage Detection Circuit

Table 2.1 is Comparative Overview of Voltage Detection Circuits, and Table 2.2 is Comparison of Voltage Detection Circuit Registers.

Table 2.3 is Comparison of Vdet2 Monitor Configuration Procedures, and Table 2.4 is Comparison of Operation Configuration Procedures for the Bits Related to Voltage Monitoring 2 Interrupt and Voltage Monitoring 2 Reset.

Table 2.1 Comparative Overview of Voltage Detection Circuits

Item		RX23E-A (LVDAb)			RX23E-B (LVDAb)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	When voltage drops below Vdet0	When voltage rises above or drops past Vdet1	When voltage rises above or drops past Vdet2	When voltage drops below Vdet0	When voltage rises above or drops past Vdet1	When voltage rises above or drops past Vdet2
							LVCMPCR. Switching between VCC and the voltage input on the CMPA2 pin can be accomplished using the LVCMPCR.EXVCCINP2 bit.
	Detection voltage	Selectable from four levels using the OFS1 register	Selectable from 14 levels using LVDLVLR.LVD1LVL[3:0] bits	Selectable from four levels using LVDLVLR.LVD2LVL[1:0] bits	Selectable from four levels using the OFS1 register	Selectable from 14 levels using LVDLVLR.LVD1LVL[3:0] bits	Selectable from four levels using LVDLVLR.LVD2LVL[1:0] bits
	Monitoring flag	—	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2	—	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2
			LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2DET flag: Vdet2 passage detection		LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2DET flag: Vdet2 passage detection

Item		RX23E-A (LVDAb)			RX23E-B (LVDAb)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
Voltage detection processing	Reset	Voltage Monitoring 0 Reset	Voltage Monitoring 1 Reset	Voltage Monitoring 2 Reset	Voltage Monitoring 0 Reset	Voltage Monitoring 1 Reset	Voltage Monitoring 2 Reset
		Reset triggered when Vdet0 > VCC: CPU restarts when a specified time elapses after the following condition is met: VCC > Vdet0	Reset triggered when Vdet1 > VCC: CPU restarts when a specified time elapses after the following condition is met: VCC > Vdet1 or Vdet1 > VCC (selectable)	Reset triggered when Vdet2 > VCC: CPU restarts when a specified time elapses after the following condition is met: VCC > Vdet2 or Vdet2 > VCC (selectable)	Reset triggered when Vdet0 > VCC: CPU restarts when a specified time elapses after the following condition is met: VCC > Vdet0	Reset triggered when Vdet1 > VCC: CPU restarts when a specified time elapses after the following condition is met: VCC > Vdet1 or Vdet1 > VCC (selectable)	Reset triggered when Vdet2 > VCC or CMPA2 pin: CPU restarts when a specified time elapses after the following condition is met: VCC or CMPA2 pin > Vdet2 or Vdet2 > VCC or CMPA2 pin (selectable)
	Interrupt	—	Voltage Monitoring 1 Interrupt	Voltage Monitoring 2 Interrupt	—	Voltage Monitoring 1 Interrupt	Voltage Monitoring 2 Interrupt
			Selectable between non-maskable or maskable interrupt	Selectable between non-maskable or maskable interrupt		Selectable between non-maskable or maskable interrupt	Selectable between non-maskable or maskable interrupt
			Condition "Vdet1 > VCC" or "VCC > Vdet1", or both, can be used as a trigger to issue an interrupt request	Condition "Vdet2 > VCC" or "VCC > Vdet2", or both, can be used as a trigger to issue an interrupt request		Condition "Vdet1 > VCC" or "VCC > Vdet1", or both, can be used as a trigger to issue an interrupt request	Condition "Vdet2 > VCC or CMPA2 pin" or "VCC or CMPA2 pin > Vdet2", or both, can be used as a trigger to issue an interrupt request
Event link function		—	Available: Event output at Vdet1 passage detection	Available: Event output at Vdet2 passage detection	—	Available: Event output at Vdet1 passage detection	Available: Event output at Vdet2 passage detection

Table 2.2 Comparison of Voltage Detection Circuit Registers

Register	Bit	RX23E-A (LVDAb)	RX23E-B (LVDAb)
LVD2CR1	LVD2IDTSEL [1:0]	Bit for selecting the condition in which the voltage monitoring 2 interrupt ELC event is generated b1 b0 0 0: When VCC ≥ Vdet2 (rise) is detected 0 1: When VCC < Vdet2 (drop) is detected 1 0: When drop or rise is detected 1 1: Setting prohibited.	Bit for selecting the condition in which the voltage monitoring 2 interrupt ELC event is generated b1 b0 0 0: When the following condition is detected: VCC or CMPA2 pin ≥ Vdet2 (rise) 0 1: When the following condition is detected: VCC or CMPA2 pin < Vdet2 (drop) 1 0: When drop or rise is detected 1 1: Setting prohibited.
LVD2SR	LVD2MON	Voltage monitoring 2 signal monitor flag 0: VCC < Vdet2 1: VCC ≥ Vdet2 or LVD2MON is disabled	Voltage monitoring 2 signal monitor flag 0: VCC or CMPA2 pin < Vdet2 1: VCC or CMPA2 pin ≥ Vdet2 or LVD2MON is disabled
LVCMPCR	EXVCCINP2	—	Voltage detection 2 comparison voltage external input select bit
LVD2CR0	LVD2RN	Voltage monitoring 2 reset negation select bit 0: Negation follows a specified time (tLVD2) after detecting the "VCC > Vdet2" state. 1: Negation follows a specified time (tLVD2) after assertion of the voltage monitoring 2 reset.	Voltage monitoring 2 reset negation select bit 0: Negation follows a specified time (tLVD2) after detecting the "VCC or CMPA2 pin > Vdet2" condition. 1: Negation follows a specified time (tLVD2) after assertion of the voltage monitoring 2 reset.

Table 2.3 Comparison of Vdet2 Monitor Configuration Procedures

Item		RX23E-A (LVDAb)	RX23E-B (LVDAb)
Vdet2 monitor configuration procedure	1	Set the LVDLVLR.LVD2LVL[1:0] bit (detection voltage for voltage detection 2).	Set the LVDLVLR.LVD2LVL[1:0] bit (detection voltage for voltage detection 2).
	2	—	Set the LVCMPCR.EXVCCINP2 bit to "0" (VCC voltage) or "1" (CMPA2 pin input voltage).
	3	Set the LVCMPCR.LVD2E bit to "1" (enable the voltage detection 2 circuit).	Set the LVCMPCR.LVD2E bit to "1" (enable the voltage detection 2 circuit).
	4	Wait for at least td(E-A).	Wait for at least td(E-A).
	5	Set the LVD2CR0.LVD2CMPE bit to "1" (enable output of comparison results for the voltage monitoring 2 circuit).	Set the LVD2CR0.LVD2CMPE bit to "1" (enable output of comparison results for the voltage monitoring 2 circuit).

Table 2.4 Comparison of Operation Configuration Procedures for the Bits Related to Voltage Monitoring 2 Interrupt and Voltage Monitoring 2 Reset

Item		RX23E-A (LVDAb)	RX23E-B (LVDAb)
Voltage monitoring 2 interrupt	1	Use the LVDLVLR.LVD2LVL[1:0] bit to select the detection voltage.	Use the LVDLVLR.LVD2LVL[1:0] bit to select the detection voltage.
Output of the voltage monitoring 2 ELC event	2	—	Set the LVCMPCR.EXVCCINP2 bit to "0" (VCC voltage) or "1" (CMPA2 pin input voltage).
	3	Set the LVD2CR0.LVD2RI bit to "0" (voltage monitoring 2 interrupt).	Set the LVD2CR0.LVD2RI bit to "0" (voltage monitoring 2 interrupt).
	4	Use the LVD2CR1.LVD2IDTSEL[1:0] bit to select the interrupt request timing. Use the LVD2CR1.LVD2IRQSEL bit to select the interrupt type.	Use the LVD2CR1.LVD2IDTSEL[1:0] bit to select the interrupt request timing. Use the LVD2CR1.LVD2IRQSEL bit to select the interrupt type.
	5	Set the LVCMPCR.LVD2E bit to "1" (enable the voltage detection 2 circuit).	Set the LVCMPCR.LVD2E bit to "1" (enable the voltage detection 2 circuit).
	6	Wait for at least td(E-A).	Wait for at least td(E-A).
	7	Set the LVD2CR0.LVD2CMPE bit to "1" (enable output of comparison results for the voltage monitoring 2 circuit).	Set the LVD2CR0.LVD2CMPE bit to "1" (enable output of comparison results for the voltage monitoring 2 circuit).
	8	Wait for at least 2 µs.	Wait for at least 2 µs.
	9	Set the LVD2SR.LVD2DET bit to "0".	Set the LVD2SR.LVD2DET bit to "0".
	10	Set the LVD2CR0.LVD2RIE bit to "1" (enable voltage monitoring 2 interrupt/reset).	Set the LVD2CR0.LVD2RIE bit to "1" (enable voltage monitoring 2 interrupt/reset).
Voltage monitoring 2 reset	1	Use the LVDLVLR.LVD2LVL[1:0] bit to select the detection voltage.	Use the LVDLVLR.LVD2LVL[1:0] bit to select the detection voltage.
	2	—	Set the LVCMPCR.EXVCCINP2 bit to "0" (VCC voltage) or "1" (CMPA2 pin input voltage).
	3	Set the LVD2CR0.LVD2RI bit to "1" (voltage monitoring 2 reset). Use the LVD2CR0.LVD2RN bit to select the reset negation type.	Set the LVD2CR0.LVD2RI bit to "1" (voltage monitoring 2 reset). Use the LVD2CR0.LVD2RN bit to select the reset negation type.
	4	Set the LVD2CR0.LVD2RIE bit to "1" (enable voltage monitoring 2 interrupt/reset).	Set the LVD2CR0.LVD2RIE bit to "1" (enable voltage monitoring 2 interrupt/reset).
	5	Set the LVCMPCR.LVD2E bit to "1" (enable the voltage detection 2 circuit).	Set the LVCMPCR.LVD2E bit to "1" (enable the voltage detection 2 circuit).
	6	Wait for at least td(E-A).	Wait for at least td(E-A).
	7	Set the LVD2CR0.LVD2CMPE bit to "1" (enable output of comparison results for the voltage monitoring 2 circuit).	Set the LVD2CR0.LVD2CMPE bit to "1" (enable output of comparison results for the voltage monitoring 2 circuit).

2.2 Clock Generation Circuit

Table 2.5 is Comparative Overview of Clock Generation Circuits, and Table 2.6 is Comparison of Clock Generation Circuit Registers.

Table 2.5 Comparative Overview of Clock Generation Circuits

Item	RX23E-A	RX23E-B
Use	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, ROM, and RAM. • Generates peripheral module clocks PCLKA, PCLKB, and PCLKD supplied to the peripheral modules. Peripheral module clock PCLKA is the operating clock for the MTU2. Peripheral module clock PCLKD is the operating clock for the S12AD. Peripheral module clock PCLKB is the operating clock for peripheral modules other than the MTU2 and S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the LPT clock (LPTCLK) to be supplied to the LPT.	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, ROM, and RAM. • Generates peripheral module clocks PCLKA, PCLKB, PCLKC, and PCLKD supplied to peripheral modules. Peripheral module clock PCLKA is the operating clock for the MTU2. Peripheral module clock PCLKC is the operating clock for the DSAD. Peripheral module clock PCLKD is the operating clock for the S12AD. Peripheral module clock PCLKB is the operating clock for peripheral modules other than the MTU2, DSAD, and S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the RTC-dedicated subclock (RTCSCLK) to be supplied to the RTC. • Generates the LPT clock (LPTCLK) to be supplied to the LPT. • Generates the LCD source clock (LCDSRCCLK) to be supplied to the LCD.

Item	RX23E-A	RX23E-B
Operating frequency	• ICLK: 32 MHz (max) • PCLKA: 32 MHz (max) • PCLKB: 32 MHz (max) • PCLKD: 32 MHz (max) • FCLK: — 1 to 32 MHz (for programming and erasing the ROM and E2 DataFlash) — 32 MHz (max) (at a read from the E2 DataFlash) • CACCLK: Same as clock from respective oscillators • IWDTCLK: 15 kHz • CANMCLK: 20 MHz (max) • LPTCLK: Same as clock from selected oscillator	• ICLK: 32 MHz (max) • PCLKA: 32 MHz (max) • PCLKB: 32 MHz (max) • PCLKC: 32 MHz (max) • PCLKD: 32 MHz (max) • FCLK: — 1 to 32 MHz (for programming and erasing the ROM and E2 DataFlash) — 32 MHz (max) (at a read from the E2 DataFlash) • CACCLK: Same as clock from respective oscillators • IWDTCLK: 15 kHz • CANMCLK: 20 MHz (max) • RTCSCLK: 32.768 kHz • LPTCLK: Same as clock from selected oscillator • LCDSRCCLK: Same as clock from respective oscillators
Main clock oscillator	• Resonator frequency: 1 to 20 MHz (VCC ≥ 2.4 V), 1 to 8 MHz (VCC < 2.4 V) • External clock input frequency: 20 MHz (max) • Connectable resonator or additional circuit: Ceramic resonator, crystal • Connection pins: EXTAL and XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and the MTU pin can be forcedly driven to high-impedance. • Drive capacity switching function	• Resonator frequency: 1 to 20 MHz (VCC ≥ 2.4 V) 1 to 8 MHz (VCC < 2.4 V) • External clock input frequency: 20 MHz (max) • Connectable resonator or additional circuit: Ceramic resonator, crystal • Connection pins: EXTAL and XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and the MTU pin can be forcedly driven to high-impedance. • Drive capacity switching function
Subclock oscillator	—	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: Crystal • Connection pins: XCIN and XCOUT
PLL Circuit	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 to 8 MHz • Frequency multiplication ratio: Selectable from 4 to 8 (increments of 0.5) • Oscillation frequency: 24 to 32 MHz (VCC ≥ 2.4 V)	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 to 8 MHz • Frequency multiplication ratio: Selectable from 4 to 8 (increments of 0.5) • Oscillation frequency: 24 to 32 MHz (VCC ≥ 2.4 V)
High-speed on-chip oscillator (HOCO)	Oscillation frequency: 32 MHz	Oscillation frequency: 32 MHz

Item	RX23E-A	RX23E-B
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 4 MHz	Oscillation frequency: 4 MHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 15 kHz	Oscillation frequency: 15kHz

Table 2.6 Comparison of Clock Generation Circuit Registers

Register	Bit	RX23E-A	RX23E-B
SCKCR	—	System clock control register	System clock control register
		Initial value after a reset differs.	
	PCKC[3:0]	—	Peripheral module clock (PCLKC) select bit
SCKCR3	CKSEL[2:0]	Clock source select bit b10 b8 0 0 0: LOCO is selected. 0 0 1: HOCO is selected 0 1 0: Main clock oscillator is selected. 1 0 0: PLL circuit is selected. Settings other than the above are prohibited.	Clock source select bit b10 b8 0 0 0: LOCO is selected 0 0 1: HOCO is selected 0 1 0: Main clock oscillator is selected. 0 1 1: Subclock oscillator is selected. 1 0 0: PLL circuit is selected. Settings other than the above are prohibited.
SOSCCR	—	—	Subclock oscillator control register
LCDSCLKCR	—	—	LCD source clock control register
LCDSCLKCR2	—	—	LCD source clock control register 2
CKOCR	CKOSEL[3:0]	CLKOUT output source select bit b11 b8 0 0 0 0: LOCO clock 0 0 0 1: HOCO clock 0 0 1 0: Main clock 0 1 0 0: PLL Settings other than the above are prohibited.	CLKOUT output source select bit b11 b8 0 0 0 0: LOCO clock 0 0 0 1: HOCO clock 0 0 1 0: Main clock 0 0 1 1: Subclock 0 1 0 0: PLL Settings other than the above are prohibited.

2.3 Clock Frequency Accuracy Measurement Circuit

Table 2.7 is Comparative Overview of Clock Frequency Accuracy Measurement Circuits, and Table 2.8 is Comparison of Clock Frequency Accuracy Measurement Registers.

Table 2.7 Comparative Overview of Clock Frequency Accuracy Measurement Circuits

Item	RX23E-A (CAC)	RX23E-B (CAC)
Measurement target clocks	The frequency of the following clocks can be measured: • Main clock • HOCO clock • LOCO clock • IWDT-dedicated clock (IWDTCLK) • Peripheral module clock B (PCLKB)	The frequency of the following clocks can be measured: • Main clock • Subclock • HOCO clock • LOCO clock • IWDT-dedicated clock (IWDTCLK) • Peripheral module clock B (PCLKB)
Measurement reference clocks	• External clock input to the CACREF pin • Main clock • HOCO clock • LOCO clock • IWDT-dedicated clock (IWDTCLK) • Peripheral module clock B (PCLKB)	• External clock input to the CACREF pin • Main clock • Subclock • HOCO clock • LOCO clock • IWDT-dedicated clock (IWDTCLK) • Peripheral module clock B (PCLKB)
Selectable functions	Digital filter function	Digital filter function
Interrupt sources	• Measurement end interrupt • Frequency error interrupt • Overflow interrupt	• Measurement end interrupt • Frequency error interrupt • Overflow interrupt
Low power consumption function	Ability to transition to module stop state	Ability to specify module stop state

Table 2.8 Comparison of Clock Frequency Accuracy Measurement Registers

Register	Bit	RX23E-A (CAC)	RX23E-B (CAC)
CACR1	FMCS[2:0]	Measurement target clock select bits b3 b1 0 0 0: Main clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock B (PCLKB) Settings other than the above are prohibited.	Measurement target clock select bits b3 b1 0 0 0: Main clock 0 0 1: Subclock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock B (PCLKB) Settings other than the above are prohibited.
CACR2	RSCS[2:0]	Measurement reference clock select bits b3 b1 0 0 0: Main clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock B (PCLKB) Settings other than the above are prohibited.	Measurement reference clock select bits b3 b1 0 0 0: Main clock 0 0 1: Subclock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock B (PCLKB) Settings other than the above are prohibited.

2.4 Low Power Consumption

Table 2.9 is Comparative Overview of Low Power Consumption Functions, Table 2.10 is Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode, and Table 2.11 is Comparison of Low Power Consumption Registers.

Table 2.9 Comparative Overview of Low Power Consumption Functions

Item	RX23E-A	RX23E-B
Reducing power consumption by switching clock signals	The frequency division ratio can be set independently for the system clock (ICLK), high-speed peripheral module clock (PCLKA), peripheral module clock (PCLKB), S12AD clock (PCLKD), and FlashIF clock (FCLK).	The frequency division ratio can be set independently for the system clock (ICLK), high-speed peripheral module clock (PCLKA), peripheral module clock (PCLKB), DSAD clock (PCLKC), S12AD clock (PCLKD), and FlashIF clock (FCLK).
Module stop function	Each peripheral module can be stopped independently by the module stop control register.	Each peripheral module can be stopped independently by the module stop control register.
Function for transition to the power down state	Transition to the power down state in which the CPU, peripheral modules, or oscillators are stopped is enabled.	Transition to the power down state in which the CPU, peripheral modules, or oscillators are stopped is enabled.
Power down state	• Sleep mode • Deep sleep mode • Software standby mode	• Sleep mode • Deep sleep mode • Software standby mode
Function for lower operating power consumption	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Two operating power control modes are available — High-speed operating mode — Middle-speed operating mode	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Three operating power control modes are available — High-speed operating mode — Middle-speed operating mode — Low-speed operating mode

Table 2.10 Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX23E-A	RX23E-B
Sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupts	Interrupts
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Subclock oscillator	—	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible

mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX23E-A	RX23E-B
Sleep mode	CPU	Stopped (retained)	Stopped (retained)
	RAM: 0000 0000h to 0000 FFFFh	Operation possible (retained)	Operation possible (retained)
	DMAC	Operation possible	Operation possible
	DTC	Operation possible	Operation possible
	Flash memory	Operation	Operation
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	—	Operation possible
	Low-Power Timer (LPT)	Operation possible	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Operation possible	Operation possible
	I/O ports	Operation	Operation
	RTCOUT output	—	Operation possible
	CLKOUT output	Operation possible	Operation possible
	LCD controller/driver	—	Operation possible
Deep sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupts	Interrupts
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Subclock oscillator	—	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM: 0000 0000h to 0000 FFFFh	Stopped (retained)	Stopped (retained)
	DMAC	Stopped (retained)	Stopped (retained)
	DTC	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	—	Operation possible
	Low-Power Timer (LPT)	Operation possible	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Operation possible	Operation possible
	I/O ports	Operation	Operation
	RTCOUT output	—	Operation possible
	CLKOUT output	Operation possible	Operation possible
	LCD controller/driver	—	Operation possible

mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX23E-A	RX23E-B
Software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupts	Interrupts
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Stopped	Stopped
	Subclock oscillator	—	Operation possible
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Stopped
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Stopped	Stopped
	CPU	Stopped (retained)	Stopped (retained)
	RAM: 0000 0000h to 0000 FFFFh	Stopped (retained)	Stopped (retained)
	DMAC	Stopped (retained)	Stopped (retained)
	DTC	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	—	Operation possible
	Low-Power Timer (LPT)	Operation possible	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained
	RTCOUT output	—	Operation possible
	CLKOUT output	Stopped	Operation possible
	LCD controller/driver	—	Operation possible

“Operation possible” means that whether the state is operating or stopped is controlled by the control register setting.

“Stopped (retained)” means that internal register values are retained and internal operations are suspended.

Table 2.11 Comparison of Low Power Consumption Registers

Register	Bit	RX23E-A	RX23E-B
MSTPCRA	MSTPA19	—	16-bit D/A converter 0 module stop bit
	MSTPA26	DSAD1 module stop bit	—
MSTPCRB	MSTPB31	—	Serial communication interface 0 module stop bit
MSTPCRC	MSTPC26	—	Serial communication interface 9 module stop bit
	MSTPC27	—	Serial communication interface 8 module stop bit
MSTPCRD	—	—	Module stop control register D
SOPCCR	—	—	Sub operating power control register

2.5 Register Write Protection Function

Table 2.12 is Comparative Overview of Register Write Protection Functions.

Table 2.12 Comparative Overview of Register Write Protection Functions

Item	RX23E-A	RX23E-B
PRC0 bit	• Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, CKOCR, LOCOTRR, ILOCOTRR, HOCOTRR0	• Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, CKOCR, LCDSCLKCR, LCDSCLKCR2, LOCOTRR, ILOCOTRR, HOCOTRR0
PRC1 bit	• Registers related to the operating modes: SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR • Registers related to the clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR	• Registers related to the operating modes: SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, SOPCCR, RSTCKCR • Registers related to the clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR
PRC2 bit	• Registers related to the low power timer: LPTCR1, LPTCR2, LPTCR3, LPTPRD, LPCMR0, LPWUCR	• Registers related to the low power timer: LPTCR1, LPTCR2, LPTCR3, LPTPRD, LPCMR0, LPWUCR
PRC3 bit	• Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	• Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

2.6 Interrupt Controller

Table 2.13 is Comparative Overview of Interrupt Controllers.

Table 2.13 Comparative Overview of Interrupt Controllers

Item		RX23E-A (ICUb)	RX23E-B (ICUb)
Interrupts	Peripheral module interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection The detection method is fixed for each connected peripheral module source.	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection The detection method is fixed for each connected peripheral module source.
	External pin interrupts	• Interrupts from pins IRQ0 to IRQ7 • Number of sources: 8 • Interrupt detection: Detection of low level, falling edge, rising edge, or both (rising and falling) edges can be set for each detection source. • Digital filter function: Supported	• Interrupts from pins IRQ0 to IRQ7 • Number of sources: 8 • Interrupt detection: Detection of low level, falling edge, rising edge, or both (rising and falling) edges can be set for each detection source. • Digital filter function: Supported
	Software interrupts	• Interrupt generated by writing to a register • Number of sources: 1	• Interrupt generated by writing to a register • Number of sources: 1
	Event link interrupts	An ELSR8I, ELSR18I, or ELSR19I interrupt can be generated by an ELC event.	An ELSR8I, ELSR18I, or ELSR19I interrupt can be generated by an ELC event.
	Interrupt priority level	Specified by registers.	Specified by registers.
	Fast interrupt function	Faster interrupt handling by the CPU can be specified for a single interrupt source only.	Faster interrupt handling by the CPU can be specified for a single interrupt source only.
	DTC/DMAC control	The DTC and DMAC can be activated by an interrupt source.	The DTC and DMAC can be activated by an interrupt source.
Non-maskable interrupts	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection: Falling edge or rising edge • Digital filter function: Supported	• Interrupt from the NMI pin • Interrupt detection: Falling edge or rising edge • Digital filter function: Supported
	Oscillation stop detection interrupts	Interrupt on detection of oscillation having stopped	Interrupt on detection of oscillation having stopped
	IWDT underflow/refresh error interrupt	Interrupt on an underflow of the down counter or occurrence of a refresh error	Interrupt on an underflow of the down counter or occurrence of a refresh error
	Voltage monitoring 1 interrupt	Voltage monitoring interrupt of voltage detection circuit 1 (LVD1)	Voltage monitoring interrupt of voltage detection circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Voltage monitoring interrupt of voltage detection circuit 2 (LVD2)	Voltage monitoring interrupt of voltage detection circuit 2 (LVD2)

Item		RX23E-A (ICUb)	RX23E-B (ICUb)
Exit from the power down state	Sleep mode Deep sleep mode	The system exits the mode by all non-maskable interrupts and all interrupts.	The system exits the mode by all non-maskable interrupts and all interrupts.
	Software standby mode	The system exits the mode by the following interrupts (except oscillation stop detection interrupts): non-maskable interrupts, external pin interrupts (IRQ0 to IRQ7), peripheral module interrupts (voltage monitoring 1 and voltage monitoring 2), and ELSR8I interrupts (LPT-dedicated interrupts)	The system exits the mode by the following interrupts (except oscillation stop detection interrupts): non-maskable interrupts, external pin interrupts (IRQ0 to IRQ7), peripheral module interrupts (voltage monitoring 1, voltage monitoring 2, and RTC alarm/cycle), and ELSR8I interrupts (LPT-dedicated interrupts)

2.7 Buses

Table 2.14 is Comparative Overview of Buses.

Table 2.14 Comparative Overview of Buses

Item		RX23E-A	RX23E-B
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
	Operand Buses	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	• Connected to RAM	• Connected to RAM
	Memory bus 2	• Connected to ROM	• Connected to ROM
Internal main buses	Internal main bus 1	• Connected to CPU • Operates in synchronization with the system clock (ICLK)	• Connected to CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DTC and DMAC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the DTC and DMAC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules (peripheral modules other than those connected to internal peripheral buses 1, 3, and 4) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1, 3, and 4) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 3	• Connected to peripheral modules (RSCAN, DSAD0, DSAD1, and AFE) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (RSCAN, DSAD, AFE, LCDC, and R16DA) • Operates in synchronization with the peripheral-module clock (PCLKB)

Item		RX23E-A	RX23E-B
Internal peripheral buses	Internal peripheral bus 4	• Connected to a peripheral module (MTU2) • Operates in synchronization with the peripheral-module clock (PCLKA)	• Connected to a peripheral module (MTU2) • Operates in synchronization with the peripheral-module clock (PCLKA)
	Internal peripheral bus 6	• Connected to flash control module and E2 data flash memory • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to flash control module and E2 data flash memory • Operates in synchronization with the FlashIF clock (FCLK)

2.8 Event link controller

Table 2.15 is Comparative Overview of Event Link Controllers, Table 2.16 is Comparison of Event Link Controller Registers, Table 2.17 is Correspondence between ELSRn Registers and Peripheral Modules, and Table 2.18 is Correspondence Between Values Set in ELSRn.ELS[7:0] Bits and Event Signal Names.

Table 2.15 Comparative Overview of Event Link Controllers

Item	RX23E-A (ELC)	RX23E-B (ELC)
Event link function	• 56 types of event signals can be directly connected to peripheral modules. • How peripheral timer modules behave when an event signal is input is selectable. • Event link operation is possible for port B. — Single port*1: Event link operation can be enabled for a single specified port	• 61 types of event signals can be directly connected to peripheral modules. • How peripheral timer modules behave when an event signal is input is selectable. • Event link operation is possible for port B and port E. — Single port*1: Event link operation can be enabled for a single specified port — Port group*1: Event link operation can be enabled for multiple specified ports within a group of up to eight ports.
Low power consumption function	Transition to the module stop state is possible.	Transition to the module stop state is possible.

Note: 1. For a single port or port group that is set for input use, an event is generated when the signal input to the corresponding pin changes. For an 80-pin or 64-pin package product of the RX23E-B Group, if PC2 is selected for the port switching register B (PSRB), event link operation with PB1 is not possible.

Table 2.16 Comparison of Event Link Controller Registers

Register	Bit	RX23E-A (ELC)	RX23E-B (ELC)
ELSRn	—	Event link setting register n (n = 1 to 4, 7, 8, 10, 12, 15, 18, 19, 24, 25, 28, 29, 46, or 47)	Event link setting register n (n = 1 to 4, 7, 8, 10, 12, 15, 16, 18 to 29, or 46)
PGRn	—	—	Port group specification register n (n = 1 or 2)
PGCn	—	—	Port group control register n (n = 1 to 2)
PDBFn	—	—	Port buffer register n (n = 1 or 2)
PELm	—	Event connection port specification register n (m = 0 or 1)	Event connection port specification register n (m = 0 to 3)
	PSP[1:0]	Port number specification bit b4 b3 0 0: Setting disabled. 0 1: Port B (corresponding to the PGR1 register) 1 0: Setting prohibited. 1 1: Setting prohibited.	Port number specification bit b4 b3 0 0: Setting disabled. 0 1: Port B (corresponding to the PGR1 register) 1 0: Port E (corresponding to the PGR2 register) 1 1: Setting prohibited.

Table 2.17 Correspondence between ELSRn Registers and Peripheral Modules

Register	RX23E-A (ELC)	RX23E-B (ELC)
ELSR1	MTU1	MTU1
ELSR2	MTU2	MTU2
ELSR3	MTU3	MTU3
ELSR4	MTU4	MTU4
ELSR7	CMT1	CMT1
ELSR8	ICU (LPT-dedicated interrupt)*1	ICU (LPT-dedicated interrupt)*1
ELSR10	TMR0	TMR0
ELSR12	TMR2	TMR2
ELSR15	S12AD	S12AD
ELSR16	—	DA0
ELSR18	ICU (interrupt 1)*2	ICU (interrupt 1)*2
ELSR19	ICU (interrupt 2)*2	ICU (interrupt 2)*2
ELSR20	—	Output port group 1
ELSR21	—	Output port group 2
ELSR22	—	Input port group 1
ELSR23	—	Input port group 2
ELSR24	Single port 0*3	Single port 0*3
ELSR25	Single port 1*3	Single port 1*3
ELSR26	—	Single port 2*3
ELSR27	—	Single port 3*3
ELSR28	Clock source switching to LOCO	Clock source switching to LOCO
ELSR29	POE	POE
ELSR46	DSAD0	DSAD0
ELSR47	DSAD1	—

Notes: 1. Specify an event signal of 32h (LPT compare match).
2. For the RX23E-A Group, specify an event signal in the range from 65h to 6Ah. For the RX23E-B Group, specify an event signal in the range from 63h to 6Ah. Do not set any values other than the above.
3. For the RX23E-A Group, do not set a the 6Ah signal, which indicates that the DOC data operation condition was met, in the ELSR24 and ELSR25 registers. For the RX23E-B Group, do not set the 6Ah signal in the ELSR24, ELSR25, ELSR26, and ELSR27 registers.

Table 2.18 Correspondence Between Values Set in ELSRn.ELS[7:0] Bits and Event Signal Names

Value of ELS[7:0] bits	Peripheral modules	RX23E-A (ELC)	RX23E-B(ELC)
08h	Multi-function timer pulse unit 2	MTU1 compare match 1A	MTU1 compare match 1A
09h		MTU1 compare match 1B	MTU1 compare match 1B
0Ah		MTU1 overflow	MTU1 overflow
0Bh		MTU1 underflow	MTU1 underflow
0Ch		MTU2 compare match 2A	MTU2 compare match 2A
0Dh		MTU2 compare match 2B	MTU2 compare match 2B
0Eh		MTU2 overflow	MTU2 overflow
0Fh		MTU2 underflow	MTU2 underflow
10h		MTU3 compare match 3A	MTU3 compare match 3A
11h		MTU3 compare match 3B	MTU3 compare match 3B
12h		MTU3 compare match 3C	MTU3 compare match 3C
13h		MTU3 compare match 3D	MTU3 compare match 3D
14h		MTU3 overflow	MTU3 overflow
15h		MTU4 compare match 4A	MTU4 compare match 4A
16h		MTU4 compare match 4B	MTU4 compare match 4B
17h		MTU4 compare match 4C	MTU4 compare match 4C
18h		MTU4 compare match 4D	MTU4 compare match 4D
19h		MTU4 overflow	MTU4 overflow
1Ah		MTU4 underflow	MTU4 underflow
1Fh	Compare match timer	CMT1 compare match 1	CMT1 compare match 1
22h	8-bit timer	TMR0 compare match A0	TMR0 compare match A0
23h		TMR0 compare match B0	TMR0 compare match B0
24h		TMR0 overflow	TMR0 overflow
28h		TMR2 compare match A2	TMR2 compare match A2
29h		TMR2 compare match B2	TMR2 compare match B2
2Ah		TMR2 overflow	TMR2 overflow
2Eh	Realtime clock	—	RTC periodic event (select 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/32, 1/16, 1/8, 1/4, 1/2, 1, or 2 seconds)
31h	Independent watchdog timer	IWDT underflow or refresh error	IWDT underflow or refresh error
32h	Low-power timer (LPT)	LPT compare match	LPT compare match
34h	12-bit A/D converter	S12AD comparison conditions are met	S12AD comparison conditions are met
35h		S12AD comparison conditions are not met	S12AD comparison conditions are not met
3Ah	Serial communication interface	SCI5 error (receive error or error signal detection)	SCI5 error (receive error or error signal detection)
3Bh		SCI5 receive data full	SCI5 receive data full
3Ch		SCI5 transmit data empty	SCI5 transmit data empty
3Dh		SCI5 transmit end	SCI5 transmit end

Value of ELS[7:0] bits	Peripheral modules	RX23E-A (ELC)	RX23E-B(ELC)
4Eh	I^2C bus interface	RIIC0 communication error or event generation	RIIC0 communication error or event generation
4Fh		RIIC0 receive data full	RIIC0 receive data full
50h		RIIC0 transmit data empty	RIIC0 transmit data empty
51h		RIIC0 transmit end	RIIC0 transmit end
52h	Serial peripheral interface	RSPI0 error (mode fault, overrun, or parity error)	RSPI0 error (mode fault, overrun, or parity error)
53h		RSPI0 idle	RSPI0 idle
54h		RSPI0 receive buffer full	RSPI0 receive buffer full
55h		RSPI0 transmit buffer empty	RSPI0 transmit buffer empty
56h		RSPI0 transmit end	RSPI0 transmit end
58h	12-bit A/D converter	S12AD A/D conversion end	S12AD A/D conversion end
5Bh	Voltage detection circuit	LVD1 voltage detection	LVD1 voltage detection
5Ch		LVD2 voltage detection	LVD2 voltage detection
5Dh	DMA controller	DMAC0 transfer end	DMAC0 transfer end
5Eh		DMAC1 transfer end	DMAC1 transfer end
5Fh		DMAC2 transfer end	DMAC2 transfer end
60h		DMAC3 transfer end	DMAC3 transfer end
61h	Data transfer controller	DTC transfer end	DTC transfer end
62h	Clock generation circuit	Oscillation stop detection of the clock generation circuit	Oscillation stop detection of the clock generation circuit
63h	I/O ports	—	Input edge detection of input port group 1
64h		—	Input edge detection of input port group 2
65h		Input edge detection of single input port 0	Input edge detection of single input port 0
66h		Input edge detection of single input port 1	Input edge detection of single input port 1
67h		—	Input edge detection of single input port 2
68h		—	Input edge detection of single input port 3
69h	Event link controller	Software event	Software event
6Ah	Data operation circuit	DOC data operation condition met	DOC data operation condition met
Settings other than the above are prohibited.			

2.9 I/O ports

Table 2.19 to Table 2.20 provide comparative overviews of I/O ports. Table 2.21 shows Comparison of I/O Port Functions. Table 2.22 shows Comparison of I/O Port Registers.

Table 2.19 Comparative Overview of I/O Ports (48-Pin)

Port symbol	RX23E-A (48-pin)	RX23E-B (48-pin)
PORT1	P14 to P17	P14 to P17
PORT2	P26 and P27	P26 and P27
PORT3	P30, P31, and P35 to P37	P30, P31, and P35 to P37
PORT5	—	P54 and P55
PORT6	—	P66 and P67
PORTB	PB0 and PB1	PB0 and PB1
PORTC	PC4 to PC7	PC7
PORTH	PH0 to PH3	—

Table 2.20 Comparative Overview of I/O Ports (40-Pin)

Port symbol	RX23E-A (40-pin)	RX23E B (40-pin)	
		High voltage input pins included	High voltage input pins not included
PORT1	P14 to P17	P14 to P17	P14 to P17
PORT2	P26 and P27	P26 and P27	P26 and P27
PORT3	P30, P31, and P35 to P37	P30, P31, and P35 to P37	P30, P31, and P35 to P37
PORTB	PB0 and PB1	PB0 and PB1	PB0 and PB1
PORTC	PC4 and PC5	PC7	PC7
PORTE	—	—	PE0
PORTH	PH0 and PH1	—	—

Table 2.21 Comparison of I/O Port Functions

Item	Port symbol	RX23E-A	RX23E-B
Input pull-up function	PORT1	P14 to P17	P12 to P17
	PORT2	P26 and P27	P20 to P27
	PORT3	P30, P31, P36, and P37	P30, P31, P36, and P37
	PORT5	—	P54 and P55
	PORT6	—	P66 and P67
	PORTB	PB0 and PB1	PB0 and PB1
	PORTC	PC4 to PC7	PC0 to PC7
	PORTH	PH0 to PH3	—
Open-drain output function	PORT1	P14 to P17	P12 to P17
	PORT2	P26 and P27	P20 to P27
	PORT3	P30, P31, P36, and P37	P30, P31, P36, and P37
	PORT5	—	P54 and P55
	PORT6	—	P66 and P67
	PORTB	PB0 and PB1	PB0 and PB1
	PORTC	PC4 to PC7	PC0 to PC7
	PORTH	PH0 to PH3	—
Driving ability switching function	PORT1	P14 to P17	P12 to P17
	PORT2	P26 and P27	P20 to P27
	PORT3	P30, P31, P36, and P37	P30, P31, P36, and P37
	PORT5	—	P54 and P55
	PORT6	—	P66 and P67
	PORTB	PB0 and PB1	PB0 and PB1
	PORTC	PC4 to PC7	PC0 to PC7
	PORTH	PH0 to PH3	—
5 V tolerant	PORT1	P16 and P17	P16 and P17
	PORT6	—	P60 and P61

Table 2.22 Comparison of I/O Port Registers

Register	Bit	RX23E-A	RX23E-B
PDR	B0 to B7	Pm0 to 7 I/O select bits (m = 1 to 3, B, C, or H)	Pm0 to 7 I/O select bits (m = 1 to 3, 5 to 7, or A to E)
PODR	B0 to B7	Pm0 to Pm7 output data storage bits (m = 1 to 3, B, C, or H)	Pm0 to Pm7 output data storage bits (m = 1 to 3, 5 to 7, or A to E)
PIDR	B0 to B7	Pm0 to Pm7 bits (m = 1 to 3, B, C, or H)	Pm0 to Pm7 bits (m = 1 to 3, 5 to 7, or A to E)
PMR	B0 to B7	Pm0 to Pm7 pin mode control bits (m = 1 to 3, B, C, or H)	Pm0 to Pm7 pin mode control bits (m = 1 to 3, 5 to 7, or A to E)
ODR0	B0	Pm0 output type select bits (m = 3, B, H)	Pm0 output type select bits (m = 1 to 3, 6, 7, or A to E)
	B2	Pm1 output type select bits (m = 3, B, H) • P31, PH1 b2 0: CMOS output 1: N-channel open drain b3 This bit is read as 0. The write value should be 0. • PB1 b3 b2 0 0: CMOS output 0 1: N-channel open drain 1 0: P-channel open drain 1 1: Setting prohibited.	Pm1 output type select bits (m = 1 to 3, 6, 7, or A to E) 0: CMOS output 1: N-channel open drain
	B3		Reserved bit
	B4	Pm2 output type select bits (m = 3, B ,H)	Pm2 output type select bits (m = 1 to 3, 6, 7, or A to E)
	B6	Pm3 output type select bits (m = 3, B, H)	Pm3 output type select bits (m = 1 to 3, 6, 7, or A to E)
ODR1	B0	Pm4 output type select bits (m = 1 to 3, or C)	Pm4 output type select bits (m = 1 to 3, 5 to 7, A, or C to E)
	B2	Pm5 output type select bits (m = 1 to 3, or C)	Pm5 output type select bits (m = 1 to 3, 5 to 7, A, or C to E) • P15,P55,P65,PC5 b2 0: CMOS output 1: N-channel open drain b3 This bit is read as 0. The write value should be 0. • P25 b3 b2 0 0: CMOS output 0 1: N-channel open drain 1 0: P-channel open drain 1 1: Setting prohibited.
	B3	Reserved bit	

Register	Bit	RX23E-A	RX23E-B
ODR1	B4	Pm6 output type select bits (m = 1 to 3, or C)	Pm6 output type select bits (m = 1 to 3, 5 to 7, A, or C to E)
	B6	Pm7 output type select bits (m = 1 to 3, or C)	Pm7 output type select bits (m = 1 to 3, 5 to 7, A, or C to E) • P27,P37,P67,PC7 b2 0: CMOS output 1: N-channel open drain b3 This bit is read as 0. The write value should be 0. • P17 b7 b6 0 0: CMOS output 0 1: N-channel open drain 1 0: P-channel open drain 1 1: Setting prohibited.
	B7	Reserved bit	
PCR	B0 to B7	Pm0 to Pm7 input pull-up resistance control bits (m = 1 to 3, B, C, or H)	Pm0 to Pm7 input pull-up resistance control bits (m = 1 to 3, 5 to 7, or A to E)
PSRB	—	—	Port switching register B
DSCR	B0 to B7	Pm0 to 7 driving ability control bits (m = 1 to 3, B, C, or H)	Pm0 to 7 driving ability control bits (m = 1 to 3, 5 to 7, or A to E)

2.10 Multi-Function Pin Controller

Table 2.23 shows Comparison of Multiplexed Pin Assignments. Table 2.24 to Table 2.35 shows comparisons of the multi-function pin controller registers between the RX23E-B and RX23E-A Groups.

In the multiplexed-pin assignment comparison table below, the pins indicated in **blue** exist on the RX23E-B Group only and the pins indicated in **orange** exist on the RX23E-A Group only. A circle (O) indicates that a function is assigned, a cross (×) that the pin does not exist or that no function is assigned, and grayed out items mean that the function is not implemented.

In the comparison tables for pin function control registers, a pin for which different values are set between the groups is indicated in **green**.

Table 2.23 Comparison of Multiplexed Pin Assignments

Module/Function	Pin Function	Port Allocation	RX23E-A		RX23E-B	
			48-Pin	40-Pin	48-Pin	40-Pin
Interrupts	NMI (input)	P35	○	○	○	○
	IRQ0 (input)	P30	○	○	○	○
		PH1	○	○	×	×
	IRQ1 (input)	P31	○	○	○	○
		PH2	○	×	×	×
	IRQ2 (input)	P26	○	○	○	○
	IRQ3 (input)	P27	○	○	○	○
	IRQ4 (input)	PB0	○	○	×	×
		P14	○	○	○	○
	IRQ5 (input)	P15	○	○	○	○
	IRQ6 (input)	P16	○	○	○	○
	IRQ7 (input)	P17	○	○	○	○
		PC7	×	×	○	○
Clock generation circuit	CLKOUT (output)	PH1	○	○	×	×
		P14	×	×	○	○
Multi-function timer unit 2	MTIOC0A (input/output)	P30	○	○	×	×
		P26	×	×	○	○
	MTIOC0B (input/output)	P15	○	○	×	×
		P14	×	×	○	○
	MTIOC0C (input/output)	PB0	○	○	×	×
		P15	×	×	○	○
	MTIOC0D (input/output)	PH0	○	○	×	×
		P17	×	×	○	○
	MTIOC1A (input/output)	P31	○	○	○	○
	MTIOC1B (input/output)	PB1	○	○	×	×
		PB0	×	×	○	○
	MTIOC2A (input/output)	P26	○	○	×	×
		PB1	○	○	×	×
		P30	×	×	○	○
	MTIOC2B (input/output)	P27	○	○	○	○
	MTIOC3A (input/output)	P14	○	○	×	×
		P17	○	○	○	○
		PC7	○	×	×	×
		PB1	×	×	○	○

Module/Function	Pin Function	Port Allocation	RX23E-A		RX23E-B	
			48-Pin	40-Pin	48-Pin	40-Pin
Multi-function timer unit 2	MTIOC3B (input/output)	P17	○	○	○	○
		PC5	○	○	×	×
		P14	×	×	○	○
	MTIOC3C (input/output)	P16	○	○	○	○
	MTIOC3C (input/output)	PC6	○	×	×	×
		PB0	×	×	○	○
	MTIOC3D (input/output)	P16	○	○	○	○
		PC4	○	○	×	×
		PC7	×	×	○	○
	MTIOC4A (input/output)	P27	○	○	○	○
		P67	×	×	○	×
	MTIOC4B (input/output)	P30	○	○	○	○
		PC7	×	×	○	○
	MTIOC4C (input/output)	P26	○	○	○	○
		P66	×	×	○	×
		PB1	×	×	○	○
	MTIOC4D (input/output)	P31	○	○	○	○
		P15	×	×	○	○
	MTIC5U (input)	PH1	○	×	×	×
		PC7	×	×	○	○
	MTIC5V (input)	PH2	○	×	×	×
		P54	×	×	○	×
		PB1	×	×	○	○
	MTIC5W (input)	PH3	○	×	×	×
		P55	×	×	○	×
		PB0	×	×	○	○
	MTCLKA (input)	P14	○	○	○	○
		PH2	○	×	×	×
		PC6	○	×	×	×
		PE0	×	×	×	○ *1
	MTCLKB (input)	P15	○	○	○	○
		PH3	○	×	×	×
		PC7	○	×	×	×
		P31	×	×	○	○
	MTCLKC (input)	PH0	○	○	×	×
		PC4	○	○	×	×
		P26	×	×	○	○
	MTCLKD (input)	PH1	○	○	×	×
		PC5	○	○	×	×
		P30	×	×	○	○
Port output enable 2	POE0# (input)	PC4	○	○	×	×
		PC7	×	×	○	○
	POE1# (input)	PB1	○	○	○	○
	POE2# (input)	PH1	○	○	×	×
		PH3	○	×	×	×
		P27	×	×	○	○
	POE3# (input)	PB0	○	○	○	○

Module/Function	Pin Function	Port Allocation	RX23E-A		RX23E-B	
			48-Pin	40-Pin	48-Pin	40-Pin
Port output enable 2	POE8# (input)	P17	○	○	×	×
		P30	○	○	○	○
8-bit timer	TMO0 (output)	P26	○	○	○	○
		PH1	○	○	×	×
		P55	×	×	○	×
	TMCI0 (input)	PB0	○	○	×	×
		PH3	○	×	×	×
		PC7	×	×	○	○
	TMRI0 (input)	PH0	○	○	×	×
		PH2	○	×	×	×
		P54	×	×	○	×
		PB1	×	×	○	○
	TMO1 (output)	P17	○	○	○	○
	TMCI1 (input)	PC4	○	○	×	×
		PB1	×	×	○	○
	TMRI1 (input)	PB1	○	○	×	×
		PB0	×	×	○	○
	TMO2 (output)	P16	○	○	○	○
		PC7	○	×	×	×
	TMCI2 (input)	P15	○	○	○	○
		PC6	○	×	×	×
		P66	×	×	○	×
	TMRI2 (input)	P14	○	○	○	○
		PC5	○	○	×	×
		P67	×	×	○	×
	TMO3 (output)	P31	○	○	○	○
	TMCI3 (input)	P30	○	○	○	○
	TMRI3 (input)	P27	○	○	○	○
Serial communication interface	RXD1 (input) SMISO1 (input/output) SSCL1 (input/output)	P15	○	○	×	×
		P30	○	○	○	○
		PB1	×	×	○	○
	TXD1 (output) SMOSI1 (input/output) SSDA1 (input/output)	P16	○	○	×	×
		P26	○	○	○	○
		PC7	×	×	○	○
	SCK1 (input/output)	P17	○	○	×	×
		P27	○	○	×	×
		P14	×	×	○	○
	CTS1# (input) / RTS1# (output) / SS1# (input)	P14	○	○	×	×
		P31	○	○	×	×
		P15	×	×	○	○
	RXD5 (input) SMISO5 (input/output) SSCL5 (input/output)	PH0	○	○	×	×
		P30	×	×	○	○
	TXD5 (output) SMOSI5 (input/output) SSDA5 (input/output)	PH1	○	○	×	×
		P31	×	×	○	○
	SCK5 (input/output)	PH2	○	×	×	×
		PC5	○	○	×	×
		P27	×	×	○	○

Module/Function	Pin Function	Port Allocation	RX23E-A		RX23E-B	
			48-Pin	40-Pin	48-Pin	40-Pin
Serial communication interface	CTS5# (input) / RTS5# (output) / SS5# (input)	PC4	○	○	×	×
		P26	×	×	○	○
	RXD6 (input) SMISO6 (input/output) SSCL6 (input/output)	PC6	○	×	×	×
		P66	×	×	○	×
	TXD6 (output) SMOSI6 (input/output) SSDA6 (input/output)	PC7	○	×	×	×
		P67	×	×	○	×
	SCK6 (input/output)	PC5	○	×	×	×
		P54	×	×	○	×
	CTS6# (input) / RTS6# (output) / SS6# (input)	PH3	○	×	×	×
		P55	×	×	○	×
	RXD12 (input) SMISO12 (input/output) SSCL12 (input/output) RXDX12 (input)	PB0	○	○	×	×
		P16	×	×	○	○
	TXD12 (output) SMOSI12 (input/output) SSDA12 (input/output) TXDX12 (output) SIOX12 (input/output)	PB1	○	○	×	×
		P17	×	×	○	○
	SCK12 (input/output)	PC5	○	○	×	×
		P26	×	×	○	○
	CTS12# (input) RTS12# (output) SS12# (input)	PC4	○	○	×	×
		P27	×	×	○	○
I²C bus interface	SCL (input/output)	P16	○	○	○	○
	SDA (input/output)	P17	○	○	○	○
Serial peripheral interface	RSPCKA (input/output)	PH3	○	×	×	×
		PC5	○	○	×	×
		P31	×	×	○	○
		PB0	×	×	○	○
	MOSIA (input/output)	P16	○	○	○	○
		PH2	○	×	×	×
		PC6	○	×	×	×
	MISOA (input/output)	P17	○	○	○	○
		PC7	○	×	×	×
	SSLA0 (input/output)	PH1	○	○	×	×
		PC4	○	○	×	×
		P15	×	×	○	○
	SSLA1 (input/output)	P15	○	○	×	×
		PC7	×	×	○	○
	SSLA2 (input/output)	PH0	○	○	×	×
		PB1	×	×	○	○
	SSLA3 (input/output)	P14	○	○	×	×
		P54	×	×	○	×
		PE0	×	×	×	○ *1
12-bit A/D converter	ADTRG0# (input)	P16	○	○	○	○

Module/Function	Pin Function	Port Allocation	RX23E-A		RX23E-B	
			48-Pin	40-Pin	48-Pin	40-Pin
Clock frequency accuracy measurement circuit	CACREF (input)	PC7	○	×	×	×
		PH0	○	○	×	×
		P31	×	×	○	○
		PE0	×	×	×	○ *1
RSCAN(RX23E-A) CAN module (RX23E-B)	CTXD0 (output)	P14	○	○	○	○
	CRXD0 (input)	P15	○	○	○	○
LVD voltage detection input	CMPA2 (input)	PB0			○	○

Note: 1. This pin does not exist on a 40-pin product provided with high-voltage input pins.

Table 2.24 Comparison of P1n Pin Function Control Registers (P1nPFS)

Register	Bit	RX23E-A (n = 4 to 7)	RX23E-B (n = 2 to 7)
P12PFS	—	—	P12 pin function select bits
P13PFS	—	—	P13 pin function select bits
P14PFS	PSEL[4:0]	Pin function select bits 00001b: MTIOC3A 00010b: MTCLKA 01011b: CTS1#/RTS1#/SS1# 01101b: SSLA3	Pin function select bits 00001b: MTIOC0B 00010b: MTIOC3B 00011b: MTCLKA 01001b: CLKOUT 01010b: SCK1 11000b: SEG15
P15PFS	PSEL[4:0]	Pin function select bits 00001b: MTIOC0B 00010b: MTCLKB 01010b: RXD1/SMISO1/SSCL1 01101b: SSLA1	Pin function select bits 00001b: MTIOC0C 00010b: MTIOC4D 00011b: MTCLKB 01010b: CTS1#/RTS1#/SS1# 01101b: SSLA0 11000b: SEG14
P16PFS	PSEL[4:0]	Pin function select bits 00001b: MTIOC3C 00010b: MTIOC3D 01010b: TXD1/SMOSI1/SSDA1	Pin function select bits 00010b: MTIOC3C 00011b: MTIOC3D 01100b: RXD12/SMISO12/ SSCL12/RXDX12 11000b: SEG13
P17PFS	PSEL[4:0]	Pin function select bits 00001b: MTIOC3A 00010b: MTIOC3B 00111b: POE8# 01010b: SCK1	Pin function select bits 00001b: MTIOC0D 00010b: MTIOC3A 00011b: MTIOC3B 01100b: TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12 11000b: SEG12

Table 2.25 Comparison of P2n Pin Function Control Registers (P2nPFS)

Register	Bit	RX23E-A (n = 6, 7)	RX23E-B (n = 0 to 7)
P20PFS	—	—	P20 pin function select bits
P21PFS	—	—	P21 pin function select bits
P22PFS	—	—	P22 pin function select bits
P23PFS	—	—	P23 pin function select bits
P24PFS	—	—	P24 pin function select bits
P25PFS	—	—	P25 pin function select bits
P26PFS	PSEL[4:0]	Pin function select bits 00001b: MTIOC2A	Pin function select bits 00001b: MTIOC0A 00011b: MTCLKC 01011b: CTS5#/RTS5#/SS5# 01100b: SCK12
P27PFS	PSEL[4:0]	Pin function select bits 01010b: SCK1	Pin function select bits 00111b: POE2# 01011b: SCK5 01100b: CTS12#/RTS12#/SS12#
P2nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P26: IRQ2 P27: IRQ3	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P22: IRQ4 (100/80-pin) P23: IRQ5 (100/80-pin) P24: IRQ6 (100/80-pin) P25: IRQ7 (100/80-pin) P26: IRQ2 (100/80/64/48/40pin) P27: IRQ3 (100/80/64/48/40pin)

Table 2.26 Comparison of P3n Pin Function Control Registers (P3nPFS)

Register	Bit	RX23E-A (n = 0, 1)	RX23E-B (n = 0, 1)
P30PFS	PSEL[4:0]	Pin function select bits 00001b: MTIOC4B 00010b: MTIOC0A	Pin function select bits 00001b: MTIOC2A 00010b: MTIOC4B 00011b: MTCLKD 01011b: RXD5/SMISO5/SSCL5
P31PFS	PSEL[4:0]	Pin function select bits 00001b: MTIOC4D 00010b: MTIOC1A 01011b: CTS1#/RTS1#/SS1#	Pin function select bits 00001b: MTIOC1A 00010b: MTIOC4D 00011b: MTCLKB 00111b: CACREF 01011b: TXD5/SMOSI5/SSDA5 01101b: RSPCKA

Table 2.27 Comparison of P5n Pin Function Control Registers (P5nPFS)

Register	Bit	RX23E-A	RX23E-B (n = 4, 5)
P5nPFS	—	—	P5n pin function control register

Table 2.28 Comparison of P6n Pin Function Control Registers (P6nPFS)

Register	Bit	RX23E-A	RX23E-B (n = 0 to 7)
P6nPFS	—	—	P6n pin function control register

Table 2.29 Comparison of P7n Pin Function Control Registers (P7nPFS)

Register	Bit	RX23E-A	RX23E-B (n = 0 to 4)
P7nPFS	—	—	P7n pin function control register

Table 2.30 Comparison of PAn Pin Function Control Registers (PAnPFS)

Register	Bit	RX23E-A	RX23E-B (n = 0 to 4)
PAnPFS	—	—	PAn pin function control register

Table 2.31 Comparison of PBn Pin Function Control Registers (PBnPFS)

Register	Bit	RX23E-A (n = 0, 1)	RX23E-B (n = 0, 1)
PB0PFS	PSEL[4:0]	Pin function select bits 00001b: MTIOC0C 00101b: TMCI0 01100b: RXD12/RXDX12/ SMISO12/SSCL12	Pin function select bits 00001b: MTIOC1B 00010b: MTIOC3C 00011b: MTIC5W 00110b: TMRI1 01101b: RSPCKA
PB1PFS	PSEL[4:0]	Pin function select bits 00001b: MTIOC2A 00010b: MTIOC1B 00101b: TMRI1 01100b: TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12	Pin function select bits 00001b: MTIOC4C 00010b: MTIOC3A 00011b: MTIC5V 00101b: TMRI0 00110b: TMCI1 01010b: RXD1/SMISO1/SSCL1 01101b: SSLA2
PBnPFS	—	Interrupt input function select bit	—
	—	—	Analog function select bit

Table 2.32 Comparison of PCn Pin Function Control Registers (PCnPFS)

Register	Bit	RX23E-A (n = 4 to 7)	RX23E-B (n = 0 to 7)
PC0PFS	—	—	PC0 pin function select bits
PC1PFS	—	—	PC1 pin function select bits
PC2PFS	—	—	PC2 pin function select bits
PC3PFS	—	—	PC3 pin function select bits
PC4PFS	PSEL[4:0]	Pin function select bits 00001b: MTIOC3D 00010b: MTCLKC 00101b: TMCI1 00111b: POE0# 01011b: CTS5#/RTS5#/SS5# 01100b: CTS12#/RTS12#/SS12# 01101b: SSLA0	Pin function select bits 00001b: MTIOC4B 00111b: POE3# 01011b: RXD8/SMISO8/SSCL8 11000b: SEG23
PC5PFS	PSEL[4:0]	Pin function select bits 00001b: MTIOC3B 00010b: MTCLKD 00101b: TMRI2 01010b: SCK5 01011b: SCK6 01100b: SCK12 01101b: RSPCKA	Pin function select bits 00001b: MTIOC4C 00111b: POE2# 01011b: TXD8/SMOSI8/SSDA8 11000b: SEG22
PC6PFS	PSEL[4:0]	Pin function select bits 00001b: MTIOC3C 00010b: MTCLKA 00101b: TMCI2 01011b: RXD6/SMISO6/SSCL6 01101b: MOSIA	Pin function select bits 00001b: MTIOC4A 00111b: POE1# 01010b: RXD1/SMISO1/SSCL1 11000b: SEG21
PC7PFS	PSEL[4:0]	Pin function select bits 00001b: MTIOC3A 00010b: MTCLKB 00101b: TMO2 00111b: CACREF 01011b: TXD6/SMOSI6/SSDA6 01101b: MISOA	Pin function select bits 00001b: MTIOC4B 00010b: MTIOC3D 00011b: MTIC5U 00101b: TMCI0 00111b: POE0# 01010b: TXD1/SMOSI1/SSDA1 01101b: SSLA1
PCnPFS	—	—	Interrupt input function select bit

Table 2.33 Comparison of PDn Pin Function Control Registers (PDnPFS)

Register	Bit	RX23E-A	RX23E-B (n = 0 to 4)
PDnPFS	—	—	PDn pin function select registers

Table 2.34 Comparison of PEn Pin Function Control Registers (PEnPFS)

Register	Bit	RX23E-A	RX23E-B (n = 0 to 4)
PEnPFS	—	—	PEn pin function select registers

Table 2.35 Comparison of PHn Pin Function Control Registers (PHnPFS)

Register	Bit	RX23E-A (n = 0 to 3)	RX23E-B (n = 0 to 4)
PHnPFS	—	PHn pin function select registers	—

2.11 Low-Power Timer

Table 2.36 is Comparative Overview of Low-Power Timer, and Table 2.37 is Comparison of Low-Power Timer Registers.

Table 2.36 Comparative Overview of Low-Power Timer

Item	RX23E-A (LPT)	RX23E-B (LPT)
Number of channels	1 channel	1 channel
Clock source	IWDT-dedicated clock	Subclock and IWDT-dedicated clock
Clock division ratio	1/2, 1/4, 1/8, 1/16, and 1/32	1/2, 1/4, 1/8, 1/16, and 1/32
Counter operation	• Counting-up using a 16-bit up-counter • Counting continues even in software standby mode.	• Counting-up using a 16-bit up-counter • Counting continues even in software standby mode.
Compare match	Compare match 0 (Compare match signals occur in only software standby mode.)	Compare match 0 (Compare match signals occur in only software standby mode.)
Event link function (output)	Compare match 0 (Compare match signals occur in only software standby mode.)	Compare match 0 (Compare match signals occur in only software standby mode.)

Table 2.37 Comparison of Low-Power Timer Registers

Register	Bit	RX23E-A (LPT)	RX23E-B (LPT)
LPTCR1	LPCNTCKSEL	Clock source select bit 0: No clock 1: IWDT-dedicated clock (IWDTCLK)	Clock source select bit 0: Subclock 1: IWDT-dedicated clock

2.12 Serial communication interface

Table 2.38 is Comparative Overview of Serial Communication Interfaces, and Table 2.39 is Comparison of Channels for Serial Communication Interfaces.

Table 2.38 Comparative Overview of Serial Communication Interfaces

Item		RX23E-A (SCIg, SCIh)	RX23E-B (SCIg, SCIh)
Number of channels		• SCIg: 3 channels • SCIh: 1 channel	• SCIg: 6 channels • SCIh: 1 channel
Serial communications modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable as LSB first or MSB first transfer.	Selectable as LSB first or MSB first transfer.
Interrupt sources		Transmission ended, transmit data empty, receive data full, receive error, or completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)	Transmission ended, transmit data empty, receive data full, receive error, or completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)
Low power consumption function		Transition to the module stop state can be set for each channel.	Transition to the module stop state can be set for each channel.
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection function	Parity error, overrun error, or framing error	Parity error, overrun error, or framing error
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Start-bit detection	Low level or falling edge is selectable.	Low level or falling edge is selectable.
	Break detection	When a framing error occurs, a break can be detected by directly reading the level of the RXDn pin.	When a framing error occurs, a break can be detected by directly reading the level of the RXDn pin.
	Clock source	• An internal or external clock can be selected. • The transfer rate clock can be input from the TMR (SCI5 or SCI6).	• An internal or external clock can be selected. • The transfer rate clock can be input from the TMR (SCI5 or SCI6).

Item		RX23E-A (SCIg, SCIh)	RX23E-B (SCIg, SCIh)
Asynchronous mode	Double-speed mode	Double-speed mode can be selected for the baud rate generator.	Double-speed mode can be selected for the baud rate generator.
	Multi-processor communication function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
Smart card interface mode	Error handling	• An error signal can be automatically transmitted when detecting a parity error during reception. • Data can be automatically retransmitted when receiving an error signal during transmission.	• An error signal can be automatically transmitted when detecting a parity error during reception. • Data can be automatically retransmitted when receiving an error signal during transmission.
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	I^2C bus format	I^2C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer speed	Fast-mode supported	Fast-mode supported
	Noise cancellation	• The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters. • The interval for noise cancellation is adjustable.	• The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters. • The interval for noise cancellation is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.

Item		RX23E-A (SCIg, SCIh)	RX23E-B (SCIg, SCIh)
Extended serial mode (supported by SCI12 only)	Start frame transmission	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection
	Start frame reception	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two kinds of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two kinds of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates
	I/O control function	• Ability to select polarity or TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select receive data sampling timing of RXDX12 pin	• Ability to select polarity or TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select receive data sampling timing of RXDX12 pin
	Timer function	Usable as reloading timer	Usable as reloading timer
Bit rate modulation function		Correction of outputs from the on-chip baud rate generator can reduce errors.	Correction of outputs from the on-chip baud rate generator can reduce errors.
Event link function (supported by SCI5 only)		• Output of error events (receive error or error signal detection) • Output of receive buffer full events	• Output of error events (receive error or error signal detection) • Output of receive buffer full events
		• Output of transmit data empty events • Output of transmit end events	• Output of transmit data empty events • Output of transmit end events

Table 2.39 Comparison of Channels for Serial Communication Interfaces

Item	RX23E-A (SCIg, SCIh)	RX23E-B (SCIg, SCIh)
Asynchronous mode	SCI1, SCI5, SCI6, SCI12	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12
Clock synchronous mode	SCI1, SCI5, SCI6, SCI12	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12
Smart card interface mode	SCI1, SCI5, SCI6, SCI12	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12
Simple I^2C mode	SCI1, SCI5, SCI6, SCI12	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12
Simple SPI mode	SCI1, SCI5, SCI6, SCI12	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12
Extended serial mode	SCI12	SCI12
TMR clock input	SCI5, SCI6, SCI12	SCI5, SCI6, SCI12
Event link function	SCI5	SCI5

2.13 Serial peripheral interface

Table 2.40 is Comparative Overview of Serial Peripheral Interfaces, and Table 2.41 is Comparison of Serial Peripheral Interface Registers.

Table 2.40 Comparative Overview of Serial Peripheral Interfaces

Item	RX23E-A (RSPIb)	RX23E-B (RSPIc)
Number of channels	1 channel	1 channel
RSPI transfer functions	• Use of MOSI (Master out/slave in), MISO (Master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Communication mode: Full-duplex or simplex (transmit-only) can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK	• Use of MOSI (Master out/slave in), MISO (Master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Communication mode: Full-duplex or simplex (transmit-only) can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK
Data format	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits).	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits). • Byte swapping of transmit and receive data is selectable
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from 1/2 to 1/4096). • In slave mode, the minimum PCLK clock divided by 6 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 6). Width at high level: 3 cycles of PCLK Width at low level: 3 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from 1/2 to 1/4096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4). Width at high level: 2 cycles of PCLK Width at low level: 2 cycles of PCLK
Buffer configuration	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers
Error detection	• Mode fault error detection • Overrun error detection*1 • Parity error detection • Underrun error detection	• Mode fault error detection • Overrun error detection*1 • Parity error detection • Underrun error detection

Item	RX23E-A (RSPIb)	RX23E-B (RSPIc)
SSL control function	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin is used for input, and SSLA1 to SSLA3 pins are used for output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Range: 1 to 8 RSPCK cycles — (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Range: 1 to 8 RSPCK cycles — (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) — Range: 1 to 8 RSPCK cycles — (set in RSPCK-cycle units) • Function for changing SSL polarity	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin is used for input, and SSLA1 to SSLA3 pins are used for output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Range: 1 to 8 RSPCK cycles — (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Range: 1 to 8 RSPCK cycles — (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) — Range: 1 to 8 RSPCK cycles — (set in RSPCK-cycle units) • Function for changing SSL polarity
Control in master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • The following items can be set in each command: — SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function	• A transfer of up to eight commands can be executed sequentially in looped execution. • The following items can be set in each command: — SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function
Interrupt sources	• Interrupt sources Receive buffer full interrupt Transmit buffer empty interrupt Error interrupt (mode fault, overrun, underrun, or parity error) Idle interrupt	• Interrupt sources Receive buffer full interrupt Transmit buffer empty interrupt Error interrupt (mode fault, overrun, underrun, or parity error) Idle interrupt

Item	RX23E-A (RSPIb)	RX23E-B (RSPIc)
Event link function (output)	• The following events can be output to the event link controller (RSPI0): Receive buffer full event Transmit buffer empty event Error event (mode fault, overrun, underrun, or parity error) Idle event Transmission completion event	• The following events can be output to the event link controller (RSPI0): Receive buffer full event Transmit buffer empty event Error event (mode fault, overrun, underrun, or parity error) Idle event Transmission completion event
Other functions	• Function for initializing the RSPI • Loop back mode	• Function for initializing the RSPI • Loop back mode
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Note: 1. During master reception with the RSPCK auto-stop function enabled, no overrun error occurs because the transfer clock stops when an overrun error is detected.

Table 2.41 Comparison of Serial Peripheral Interface Registers

Register	Bit	RX23E-A (RSPIb)	RX23E-B (RSPIc)
SPDR	—	RSPI data register Supported access sizes • Longword (SPDCR.SPLW=1) • Word access (SPDCR.SPLW=0)	RSPI data register Supported access sizes • Longword (SPDCR.SPLW=1, SPDCR.SPBYT=0) • Word access (SPDCR.SPLW=0, SPDCR.SPBYT=0) • Byte access (SPDCR.SPBYT=1)
SPDCR	SPBYT	—	RSPI byte access specification bit
SPDCR2	—	—	RSPI data control register 2

2.14 Analog Front-End

Table 2.42 is Comparative Overview of Analog Front-End, and Table 2.43 is Comparison of Analog Front-End Registers.

Table 2.42 Comparative Overview of Analog Front-End

Item	RX23E-A (AFE)	RX23E-B (AFEA)
Number of channels	6 channel	8 channels
24 bit delta-sigma A/D converter (DSAD)	• 2 circuits (DSAD0 and DSAD1) • Fourth-order sinc filter • On-board programmable gain amplifier (PGA) • Operating mode: single scan, continuous scan, or one-shot • High-speed conversion: 15.625 kSPS • Low noise: 30 nVRMS (typ.) (equivalent input noise) (fMOD= 500 kHz, DR = 7.6 SPS, Gain = 128) • Oversampling ratio: 32 to 65,536 (only a multiple of 16)	• 1 circuit (DSAD0) • Fourth-order sinc filter, fourth-order sinc filter + fourth order sinc filter, fifth-order sinc filter, or fifth-order sinc filter + first-order sinc filter • On-board programmable gain amplifier (PGA) • Operating mode: single scan, continuous scan, or one-shot • High-speed conversion: 125 kSPS, maximum • Low noise: 7 nVRMS (typ.) (equivalent input noise) (fMOD= 4 MHz, DR = 3.814 SPS, Gain = 128) • Oversampling ratio: First stage: 32 to 256 (only a multiple of 16) Second stage: 1 to 4,096
12-bit successive approximation type A/D converter (S12AD)	• Analog signal input select circuit (up to 6 pins) • Maximum conversion clock frequency: 32 MHz (conversion rate: 1.4 µs) • Operating mode: single scan, continuous scan, or group scan • Reference voltage is selectable. High potential side: VREFH0 or AVCC0 Low potential side: VREFL0 or AVSS0	• Analog signal input select circuit (up to 8 pins) • Maximum conversion clock frequency: 32 MHz (conversion rate: 1.4 µs) • Operating mode: single scan, continuous scan, or group scan • Reference voltage is selectable. High potential side: VREFH0 or AVCC0 Low potential side: VREFL0 or AVSS0
16-bit D/A converter (R16DA)	—	• 16-bit resolution • Low-impedance output (with an output buffer)

Item	RX23E-A (AFE)	RX23E-B (AFEA)
Operation control circuit	Operation of the following circuits can be controlled individually: • 24-bit delta-sigma A/D converter (DSAD0, DSAD1) • Excitation current source (IEXC) • Bias voltage generation circuit (VBIAS) • Reference voltage source (VREF) • Temperature sensor (TEMPS) The DSAD operating voltage can be set.	Operation of the following circuits can be controlled individually: • 24-bit delta-sigma A/D converter (DSAD0) • Excitation current source (IEXC) • Bias current source (IREF) • Bias voltage generation circuit (VBIAS) • Reference voltage source (VREF) • Temperature sensor (TEMPS)
High-voltage analog signal input circuit (HVAC)	—	Signals at ±10 V can be input. A resistor divider with a division ratio of 10:1 is built into the board. Input impedance: 1 MΩ (min.)
Analog multiplexer (AMUX)	For DSAD0 and DSAD1, the following items can be selected for each channel: positive-side input signal (ANDSnmP), negative-side input signal (ANDSnmN), positive-side reference voltage (VRnmP), and negative-side reference voltage (VRnmN) (n = 0 or 1, m = 0 to 5) • ANDSnmP and ANDSnmN are selected from the AIN0 to AIN11 pins. • VRnmP is selected from the REF0P pin, the REF1P pin*1, AVCC0 or REFOUT. • VRnmN is selected from the REF0N pin, the REF1N pin*1, or AVSS0. • TEMPS can be selected as the input to DSAD0.	For DSAD0, the following items can be selected for each channel (m = 0 to 7): positive-side input signal (ANDS0mP), negative-side input signal (ANDS0mN), positive-side reference voltage (VR0mP), and negative-side reference voltage (VR0mN). • ANDS0mP and ANDS0mN are selectable from among those on the AIN0 to AIN15, HVAIN0 to HVAIN3, AVSS0, HVCOM, and DA0 pins and AVSS0 voltage for 16-bit D/A converter. • VR0mP is selected from the REF0P pin, the REF0N pin, the REF1P pin, the REF1N pin*1, AVCC0 and REFOUT*2. • VR0mN is selected from the REF0P pin, the REF0N pin, the REF1P pin, the REF1N pin*1, and AVSS0. • TEMPS can be selected as the input to DSAD0.
Low-side switch circuit (LSW)	Switch connecting the LSW pin and AVSS0 On-resistance: 10 Ω (max.)	Switch connecting the LSW pin and AVSS0 On-resistance: 10 Ω (max.)
Reference voltage source (VREF)*3	Generation voltage: 2.5 V Maximum load current: ±10 mA Output from the REFOUT pin	Generation voltage: 2.5 V Maximum load current: ±10 mA Output from the REFOUT pin

Item		RX23E-A (AFE)	RX23E-B (AFEA)
Bias voltage generation circuit (VBIAS)		Output voltage: (AVCC0 + AVSS0) / 2 Generated voltage can be output from any of the AIN0 to AIN11 pins.	Output voltage: (AVCC0 + AVSS0) / 2 Generated voltage can be output from the AIN2 or AIN10 pin.
Temperature sensor (TEMPS)		Temperature measured and calculated for each chip at the time of shipment from the factory is stored in a register.	Temperature measured and calculated for each chip at the time of shipment from the factory is stored in a register.
Excitation current source (IEXC)		2-channel or 4-channel fixed currents can be output from the AIN0 to AIN11 pins. • 2-channel output mode: IEXC0 and IEXC1 are output from any two of the AIN0 to AIN11 pins. Output current: 50 µA, 100 µA, 250 µA, 500 µA, 750 µA, or 1,000 µA • 4-channel output mode: IEXC0 and IEXC3 are output from any four of the AIN0 to AIN11 pins. Output current: 50 µA, 100 µA, 250 µA, or 500 µA	2-channel fixed currents (IEXC0 and IEXC1) are output either from the AIN2 and AIN3 pins or from the AIN8 and AIN9 pins. Output current: 50 µA, 100 µA, 250 µA, 500 µA, 750 µA, or 1,000 µA
Bias current source (IREF)		—	High-precision bias current is generated for the 16-bit D/A converter.
Voltage detection circuit (VDET)	Low power-supply voltage detection circuit (LVDET)	Voltage reduction of AVCC0 was detected. 2 circuits (LVDET0 and LVDET1) are provided for each detection level. The detection level can be changed by using a register.	Voltage reduction of AVCC0 was detected. 2 circuits (LVDET0 and LVDET1) are provided for each detection level. The detection level for LVDET0 can be changed by using a register. The detection level for LVDET1 is fixed at 3.80 V.
	DSAD input voltage error detection circuit (DSIDET)	Voltage errors on the positive and negative sides are detected for DSAD0 and DSAD1. 4 circuits (DS0PDET, DS0NDET, DS1PDET, and DS1NDET)	Voltage errors on the positive and negative sides are detected for DSAD0. 2 circuits (DS0PDET and DS0NDET)
	DSAD reference voltage error detection circuit (DSRDET)	Reference voltage errors on the positive and negative sides are detected for DSAD0 and DSAD1. Detection of disconnection between the external reference voltage source and MCU is assisted. 2 circuits (DS0RDET and DS1RDET)	Reference voltage errors on the positive and negative sides are detected for DSAD0. Detection of disconnection between the external reference voltage source and MCU is assisted. 1 circuit (DS0RDET)
	Excitation current source disconnection detection circuit (IEXCDET)	Detection of disconnection between the external sensor and MCU is assisted. 4 circuits (IEXC0DET, IEXC1DET, IEXC2DET, and IEXC3DET)	Detection of disconnection between the external sensor and MCU is assisted. 2 circuits (IEXC0DET and IEXC1DET)

Item		RX23E-A (AFE)	RX23E-B (AFEA)
Voltage detection circuit (VDET)	High-voltage analog common input disconnection detection circuit (HVCOMDET)	—	Detection of disconnection with the common voltage input pin of the high-voltage analog signal input circuit is assisted. 1 circuit

Notes: 1. For the RX23E-A Group, the REF1P pin is also used as the AIN5 pin. The REF1N pin is also used as the AIN4 pin. For the RX23E-B Group, the REF1P pin is also used as the AIN13 pin. The REF1N pin is also used as the AIN12 pin.
2. REFOUT is used to output the reference voltage (VREF).
3. To use the reference voltage, connect the REFOUT pin to AVSS0 via a 0.47 µF capacitor.

Table 2.43 Comparison of Analog Front-End Registers

Register	Bit	RX23E-A (AFE)	RX23E-B (AFEA)
OPCR	DSAD1EN	DSAD1 operation enable bit	—
	CLKSEL[3:0]	—	Peripheral clock frequency select bits
	DSADLVM	DSAD operation voltage select bits	—
VDETCR	—	Voltage detection circuit register	Voltage detection circuit register
		Initial value after a reset differs.	
	DET1LVL[1:0]	LVDET1 detection level setting bits	—
	VR1PDISA	Disconnection detection assist bit	—
	VR1PDISC	VR1P disconnection detection charge mode setting bit	—
	VR1NDISA	VR1N disconnection detection assist bit	—
	VR1NDISC	VR1N disconnection detection charge mode setting bit	—
VDETER	IEXC2DET	IEXC2DET operation enable bit	—
	IEXC3DET	IEXC3DET operation enable bit	—
	DS1PDET	DS1PDET operation enable bit	—
	DS1NDET	DS1NDET operation enable bit	—
	DS1RDET	DS1RDET operation enable bit	—
	HVCOMDET	—	HVCOMDET operation enable bit
VBOSR	VBIASEN0	AIN0 pin VBIAS output control bit	—
	VBIASEN1	AIN1 pin VBIAS output control bit	—
	VBIASEN3	AIN3 pin VBIAS output control bit	—
	VBIASEN4	AIN4 pin VBIAS output control bit	—
	VBIASEN5	AIN5 pin VBIAS output control bit	—
	VBIASEN6	AIN6 pin VBIAS output control bit	—
	VBIASEN7	AIN7 pin VBIAS output control bit	—
	VBIASEN8	AIN8 pin VBIAS output control bit	—
	VBIASEN9	AIN9 pin VBIAS output control bit	—
	VBIASEN11	AIN11 pin VBIAS output control bit	—
DS0mISR*1	—	DSAD0 channel m input select register (m = 0 to 5)	DSAD0 channel m input select register (m = 0 to 7)
		Initial value after a reset differs.	

Register	Bit	RX23E-A (AFE)	RX23E-B (AFEA)
DS0mISR*1	PSEL[3:0] (RX23E-A) PSEL[4:0] (RX23E-B)	Positive-side input signal select bit b3 b0 0 0 0 0: AIN0 pin 0 0 0 1: AIN1 pin 0 0 1 0: AIN2 pin 0 0 1 1: AIN3 pin 0 1 0 0: AIN4 pin 0 1 0 1: AIN5 pin 0 1 1 0: AIN6 pin 0 1 1 1: AIN7 pin 1 0 0 0: AIN8 pin 1 0 0 1: AIN9 pin 1 0 1 0: AIN10 pin 1 0 1 1: AIN11 pin 1 1 0 0: Offset error measurement setting*2 1 1 1 1: No connection Other than above: Setting prohibited.	Positive-side input signal select bit b4 b0 0 0 0 0 0: AIN0 pin 0 0 0 0 1: AIN1 pin 0 0 0 1 0: AIN2 pin 0 0 0 1 1: AIN3 pin 0 0 1 0 0: AIN4 pin 0 0 1 0 1: AIN5 pin 0 0 1 1 0: AIN6 pin 0 0 1 1 1: AIN7 pin 0 1 0 0 0: AIN8 pin 0 1 0 0 1: AIN9 pin 0 1 0 1 0: AIN10 pin 0 1 0 1 1: AIN11 pin 0 1 1 0 0: AIN12 pin 0 1 1 0 1: AIN13 pin 0 1 1 1 0: AIN14 pin 0 1 1 1 1: AIN15 pin 1 0 0 0 0: HVAIN0 pin 1 0 0 0 1: HVAIN1 pin 1 0 0 1 0: HVAIN2 pin 1 0 0 1 1: HVAIN3 pin 1 1 0 0 0: AVSS0 pin 1 1 0 0 1: HVCOM pin 1 1 0 1 0: AVSS0 voltage for the 16-bit D/A converter 1 1 0 1 1: DA0 pin 1 1 1 0 0: Offset error measurement setting*2 1 1 1 1 1: No connection Other than above: Setting prohibited.

Register	Bit	RX23E-A (AFE)	RX23E-B (AFEA)
DS0mISR*1	NSEL[3:0] (RX23E-A) NSEL[4:0] (RX23E-B)	Negative-side input signal select bit b7 b4 0 0 0 0: AIN0 pin 0 0 0 1: AIN1 pin 0 0 1 0: AIN2 pin 0 0 1 1: AIN3 pin 0 1 0 0: AIN4 pin 0 1 0 1: AIN5 pin 0 1 1 0: AIN6 pin 0 1 1 1: AIN7 pin 1 0 0 0: AIN8 pin 1 0 0 1: AIN9 pin 1 0 1 0: AIN10 pin 1 0 1 1: AIN11 pin 1 1 1 1: No connection Other than above: Setting prohibited.	Negative-side input signal select bit b12 b8 0 0 0 0 0: AIN0 pin 0 0 0 0 1: AIN1 pin 0 0 0 1 0: AIN2 pin 0 0 0 1 1: AIN3 pin 0 0 1 0 0: AIN4 pin 0 0 1 0 1: AIN5 pin 0 0 1 1 0: AIN6 pin 0 0 1 1 1: AIN7 pin 0 1 0 0 0: AIN8 pin 0 1 0 0 1: AIN9 pin 0 1 0 1 0: AIN10 pin 0 1 0 1 1: AIN11 pin 0 1 1 0 0: AIN12 pin 0 1 1 0 1: AIN13 pin 0 1 1 1 0: AIN14 pin 0 1 1 1 1: AIN15 pin 1 0 0 0 0: HVAIN0 pin 1 0 0 0 1: HVAIN1 pin 1 0 0 1 0: HVAIN2 pin 1 0 0 1 1: HVAIN3 pin 1 1 0 0 0: AVSS0 pin 1 1 0 0 1: HVCOM pin 1 1 0 1 0: AVSS0 voltage for the 16-bit D/A converter 1 1 0 1 1: DA0 pin 1 1 1 1 1: No connection Other than above: Setting prohibited.
	RSEL[3:0] (RX23E-A) RSEL[4:0] (RX23E-B)	Reference voltage select bits b8 0: Positive-side reference buffer disabled 1: Positive-side reference buffer enabled	Reference voltage select bits b16 0: Positive-side reference buffer disabled 1: Positive-side reference buffer enabled
		b9 0: Negative-side reference buffer disabled 1: Negative-side reference buffer enabled	b17 0: Negative-side reference buffer disabled 1: Negative-side reference buffer enabled
		b11 b10 0 0: AVCC0/AVSS0*3 0 1: REFOUT/AVSS0*3 1 0: REF0P/REF0N 1 1: REF1P/REF1N	b20 b18 0 0 0: AVCC0/AVSS0*3 0 0 1: REFOUT/AVSS0*3 0 1 0: REF0P/REF0N 0 1 1: REF1P/REF1N 1 0 0: REF0N/REF0P 1 0 1: REF1N/REF1P Other than above: Setting prohibited.

Register	Bit	RX23E-A (AFE)	RX23E-B (AFEA)
DS1mISR	—	DSAD1 channel m input select register (m = 0 to 5)	—
EXCCR	MODE	Operating mode select bit	—
EXCOSR	—	Excitation current output select register	Excitation current output select register
		Initial value after a reset differs.	
	IEXC0SEL[3:0]	IEXC0 to IEXC3 output pin select bits These bits select the pins to be used for output from the excitation current sources. b3 b0 0 0 0 0: AIN0 pin 0 0 0 1: AIN1 pin 0 0 1 0: AIN2 pin 0 0 1 1: AIN3 pin 0 1 0 0: AIN4 pin 0 1 0 1: AIN5 pin 0 1 1 0: AIN6 pin 0 1 1 1: AIN7 pin 1 0 0 0: AIN8 pin 1 0 0 1: AIN9 pin 1 0 1 0: AIN10 pin 1 0 1 1: AIN11 pin 1 1 1 1: Output stop Other than above: Setting prohibited.	IEXC0 output pin select bits These bits select the pins to be used for output from the excitation current sources. b3 b0 0 0 1 0: AIN2 pin 1 0 0 0: AIN8 pin 1 1 1 1: Output stop Other than above: Setting prohibited.
	IEXC1SEL[3:0]		IEXC1 output pin select bits These bits select the pins to be used for output from the excitation current sources. b7 b4 0 0 1 1: AIN3 pin 1 0 0 1: AIN9 pin 1 1 1 1: Output stop Other than above: Setting prohibited.
	IEXC2SEL[3:0]		—
	IEXC3SEL[3:0]		—

Notes: 1. Before programming this register, set the OPCR.DSAD0EN bit to "1" (DSAD0 operation enable).For the RX23E-B Group, do not program the register that corresponds to the channel that is being used for A/D conversion.

2. For the RX23E-A Group, a voltage of (AVCC0 + AVSS0) / 2 is applied to the positive-side and negative-side input pins for DSAD0 if the PSEL[3:0] bits are set to "11100b". For the RX23E-B Group, this occurs if the PSEL[4:0] bits are set to "11100b".If A/D conversion is performed in this state, the offset error can be measured. At this time, for the RX23E-A Group, make sure that the NSEL[3:0] bits are set to "11111b". For the RX23E-B Group, make sure that the NSEL[4:0] bits are set to "11111b".

3. If AVCC0/AVSS0 and REFOUT/AVSS0 are selected, the reference buffer is disabled.

2.15 24-Bit Delta-Sigma A/D Converter

Table 2.44 is Comparative Overview of 24-Bit Delta-Sigma A/D Converters, and Table 2.45 is Comparison of 24-Bit Delta-Sigma A/D Converter Registers.

Table 2.44 Comparative Overview of 24-Bit Delta-Sigma A/D Converters

Item	RX23E-A (DSADA)	RX23E-B (DSADB)
Number of units	2 units	1 unit
Input channels	6 channels (12 input channels in total)	8 channels (16 input channels in total)
A/D conversion method	Delta-sigma type	Delta-sigma type
Resolution	24-bit	24 bits
Analog input	The input method can be selected for each channel by using an analog multiplexer (AMUX). • Differential operation input • Pseudo-differential operation input • Single-end input	The input method can be selected for each channel by using an analog multiplexer (AMUX). • Differential operation input • Pseudo-differential operation input • Single-end input
Modulator clock frequency (fMOD)	• Normal mode: 500 kHz • Low-power mode: 125 kHz	125 kHz to 4 MHz
Programmable gain amplifier (PGA)	• The PGA gain can be set for each channel (x1, x2, x4, x8, x16, x32, x64, x128) • Direct input to DSAD bypassing PGA is possible. • Input to DSAD via an analog input buffer (BUF) bypassing PGA is possible.	• The PGA gain can be set for each channel (x1, x2, x4, x8, x16, x32, x64, x128) • Direct input to DSAD bypassing PGA is possible. • Input to DSAD via an analog input buffer (BUF) bypassing PGA is possible.
Data register	A/D conversion result register x 1, average-value calculation result data register x 1 • The channel number corresponding to the A/D conversion result can be checked by using a register that is provided for its use only. • An overflow flag for the A/D conversion result is provided. • The format of the output code can be selected from the following: 2's complement or straight binary.	A/D conversion result register x 1 • The channel number corresponding to the A/D conversion result can be checked by using a register that is provided for its use only. • An overflow flag for the A/D conversion result is provided. • The format of the output code can be selected from the following: 2's complement or straight binary.
Operating clock	• Normal mode: 4 MHz • Low-power mode: 1 MHz The clock is generated by dividing PCLKB by 1, 2, 3, 4, 5, 6, 7.5, or 8.	500 kHz to 16 MHz The clock is generated by dividing PCLKC by 1, 2, 3, 4, 5, 6, 8, 12, 16, 20, or 32.
Conversion start condition	• Software trigger • Hardware trigger	• Software trigger • Hardware trigger
Inter-unit synchronous start	Units 0 and 1 can synchronously start.	—

Item	RX23E-A (DSADA)	RX23E-B (DSADB)
Operating mode	• Continuous scan mode (Operation continues until auto-scan stops.) • Single scan mode (Operation stops each time an auto-scan cycle ends.) • One-shot operation (Operation stops after A/D conversion ends.)	• Continuous scan mode (Operation continues until auto-scan stops.) • Single scan mode (Operation stops each time an auto-scan cycle ends.) • One-shot operation (Operation stops after A/D conversion ends.)
Conversion mode	• Normal operation • Single-cycle settling	• Normal operation • Single-cycle settling
Oversampling ratio (OSR)	• Selectable from 64, 128, 256, 512, 1024, 2048, or a user-defined value. • [User-defined value] 32 to 65,536 (only a multiple of 16) • Settable on a per-channel basis	• First stage sinc filter: 16 to 256 (only a multiple of 16) • Second stage sinc filter: Bypass or 2 to 4,096 • Total oversampling ratio: 32 to 1,048,576 • Settable on a per-channel basis
Number of times A/D conversion is performed	The number of times A/D conversion is performed per auto-scan cycle can be set for each channel. • 1 to 8,032 or 1 to 255 can be set by configuring the register. • Setting 0 enables one-shot operation.	The number of times A/D conversion is performed per auto-scan cycle can be set for each channel. • 1 to 8,191 can be set by configuring the register. • Setting 0 enables one-shot operation.
Averaging of A/D conversion results	• One of the following averaging-related operations can be selected: — Do not perform averaging. — Perform averaging and end A/D conversion. An interrupt is generated each time A/D conversion is performed. — Perform averaging and end A/D conversion. An interrupt is generated when the average value is stored. The number of data pieces to be averaged can be selected (8, 16, 32, or 64) for each channel.	—
Interrupt sources	• A/D conversion end interrupt (ADI0 or ADI1) • Scan end interrupt (SCANEND0 or SCANEND1)	• A/D conversion end interrupt (ADI0) • Channel switching interrupt (CHCHG0) • Scan end interrupt (SCANEND0)
Scan operation	Only the channels for which A/D conversion is permitted are subject to conversion (from the channel with the smallest channel number).	Only the channels for which A/D conversion is permitted are subject to conversion (from the channel with the smallest channel number).
Digital filter	Fourth-order sinc filter	One of the following configurations can be selected: — Fourth-order sinc filter — Fourth-order sinc filter + fourth-order sinc filter — Fifth-order sinc filter — Fifth-order sinc filter + first-order sinc filter

Item	RX23E-A (DSADA)	RX23E-B (DSADB)
Sinc filter gain correction	—	Automatically corrects the gain generated by the Sinc filter using the value set in the register.
Correction of offset errors and gain errors	Offset errors and gain errors are automatically corrected by using the value set in a register.	Offset errors and gain errors are automatically corrected by using the value set in a register.
Disconnection detection assist	The disconnection detection assist function for input signals can be used. • The disconnection detection current (0.5, 2, 4, or 20 µA) can be set for each channel.	The disconnection detection assist function for input signals can be used. • The disconnection detection current (0.5, 2, 4, or 20 µA) can be set for each channel.
Error detection	If an error occurs in an A/D conversion result, the error is reported when the result is returned.	If an error occurs in an A/D conversion result, the error is reported when the result is returned.
Event link function	A/D conversion is started by a trigger from ELC (hardware trigger)	A/D conversion is started by a trigger from ELC (hardware trigger)
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Table 2.45 Comparison of 24-Bit Delta-Sigma A/D Converter Registers

Register	Bit	RX23E-A (DSADA)	RX23E-B (DSADB)
CCR	—	DSAD operating clock control register	DSAD operating clock control register
		Initial value after a reset differs.	
	CLKDIV[3:0]	Operating clock division ratio setting bits b3 b0 0 0 0 0: PCLKB (no division) 0 0 0 1: PCLKB/2 (division by 2) 0 0 1 0: PCLKB/3 (division by 3) 0 0 1 1: PCLKB/4 (division by 4) 0 1 0 0: PCLKB/5 (division by 5) 0 1 0 1: PCLKB/6 (division by 6) 0 1 1 0: PCLKB/7.5 (division by 7.5) 0 1 1 1: PCLKB/8 (division by 8) 1 1 0 0: PCLKB (no division) 1 1 0 1: PCLKB/2 (division by 2) Settings other than the above are prohibited.	Operating clock division ratio setting bits b3 b0 0 0 0 0: PCLKC (no division) 0 0 0 1: PCLKC/2 (division by 2) 0 0 1 0: PCLKC/3 (division by 3) 0 0 1 1: PCLKC/4 (division by 4) 0 1 0 0: PCLKC/5 (division by 5) 0 1 0 1: PCLKC/6 (division by 6) 0 1 1 1: PCLKC/8 (division by 8) 1 0 0 0: PCLKC/12 (division by 12) 1 0 0 1: PCLKC/16 (division by 16) 1 0 1 0: PCLKC/20 (division by 20) 1 0 1 1: PCLKC/32 (division by 32) Settings other than the above are prohibited.
	LPMD	Low-power mode setting bit	—
MR	SYNCST	Inter-unit synchronous start enable bit	—
	CH6EN	—	Channel 6 A/D conversion enable bit
	CH7EN	—	Channel 7 A/D conversion enable bit
MRm	—	Channel m operating mode register (m = 0 to 5)	Channel m operating mode register (m = 0 to 7)
		Initial value after a reset differs.	
	OSR[2:0]	Oversampling ratio setting bits	—
	DISAP	Positive-side input signal disconnection detection assist bit	—
	DISAN	Negative-side input signal disconnection detection assist bit	—
	DISA[1:0]	—	Disconnection detection assist bits
	AVMD[1:0]	Averaging mode setting bits	—
	AVDN[1:0]	Averaging target data count select bits	—
	FSEL	—	Sinc filter select bit

Register	Bit	RX23E-A (DSADA)	RX23E-B (DSADB)
CRm	—	Channel m control register (m = 0 to 5)	Channel m control register (m = 0 to 7)
	CNY[4:0]	A/D conversion count setting bits Y	—
	CNX[2:0]	A/D conversion count setting bits X A	—
	CNMD	A/D conversion count calculation mode bit	—
	CNT[12:0]	—	A/D conversion count setting bits
ADST	ADCE	—	A/D converter operation enable bit
DR	CCH[2:0] (RX23-A) CCH[3:0] (RX23-B)	Conversion channel display bits b31 b29 0 0 0: No conversion or invalid data 0 0 1: Channel 0 0 1 0: Channel 1 0 1 1: Channel 2 1 0 0: Channel 3 1 0 1: Channel 4 1 1 0: Channel 5	Conversion channel display bits b31 b28 0 0 0 0: No conversion or invalid data 0 0 0 1: Channel 0 0 0 1 0: Channel 1 0 0 1 1: Channel 2 0 1 0 0: Channel 3 0 1 0 1: Channel 4 0 1 1 0: Channel 5 0 1 1 1: Channel 6 1 0 0 0: Channel 7
AVDR	—	Average value data register	—
SR	INIT	—	A/D conversion initialization completion flag
OSRm	—	Channel m oversampling ratio setting register (m = 0 to 5)	Channel m oversampling ratio setting register (m = 0 to 7)
	OSR1[3:0]	—	First stage sinc filter oversampling ratio setting bits
	OSR2[11:0]	—	Second stage sinc filter oversampling ratio setting bits
SGCRm	—	—	Channel m sinc filter gain correction register (m = 0 to 7)
GCRm	—	Channel m gain correction register (m = 0 to 5)	Channel m gain correction register (m = 0 to 7)
OFCRm	—	Channel m offset correction register (m = 0 to 5)	Channel m offset correction register (m = 0 to 7)

2.16 12-bit A/D converter

Table 2.46 is Comparative Overview of 12-Bit A/D Converters, and Table 2.47 is Comparison of 12-Bit A/D Converter Registers.

Table 2.46 Comparative Overview of 12-Bit A/D Converters

Item	RX23E-A (S12ADE)	RX23E-B (S12ADE)
Number of units	1 unit	1 unit
Input channels	6 channel	8 channels
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12-bit	12-bit
Conversion time	1.4 µs per channel (when A/D conversion clock (ADCLK) = 32 MHz)	1.4 µs per channel (when A/D conversion clock (ADCLK) = 32 MHz)
A/D conversion clock	Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency division ratio should be one of the following. — PCLKB to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, or 8:1 ADCLK is set using the clock generation circuit.	Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency division ratio should be one of the following. — PCLKB to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, or 8:1 ADCLK is set using the clock generation circuit.
Data register	• 6 registers for analog input and one register for A/D-converted data duplication in double trigger mode • One register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • 12-bit accuracy output for A/D conversion results • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.	• 8 registers for analog input and one register for A/D-converted data duplication in double trigger mode • One register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • 12-bit accuracy output for A/D conversion results • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.

Item	RX23E-A (S12ADE)	RX23E-B (S12ADE)
Operating mode	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 6 channels arbitrarily selected. • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs of up to 6 channels arbitrarily selected. • Group scan mode: — Analog input of up to 6 channels arbitrarily selected is divided into two groups (groups A and B), and A/D conversion is performed only once for the analog input selected by group. — For groups A and B, conversion can be independently started at different times by selecting a different conversion start condition (synchronization trigger) for each group. • Group scan mode (when group A priority control is selected) — If a group A trigger is input during A/D conversion on group B, the A/D conversion on group B is stopped and A/D conversion is performed on group A. — Restart (rescan) of A/D conversion on group B after completion of A/D conversion on group A can be specified.	• Single scan mode: — A/D conversion is performed only once on the analog input of up to 8 channels arbitrarily selected. • Continuous scan mode: — A/D conversion is performed repeatedly on the analog input of up to 8 channels arbitrarily selected. • Group scan mode: — Analog input of up to 8 channels arbitrarily selected is divided into two groups (groups A and B), and A/D conversion is performed only once for the analog input selected by group. — For groups A and B, conversion can be independently started at different times by selecting a different conversion start condition (synchronization trigger) for each group. • Group scan mode (when group A priority control is selected) — If a group A trigger is input during A/D conversion on group B, the A/D conversion on group B is stopped and A/D conversion is performed on group A. — Restart (rescan) of A/D conversion on group B after completion of A/D conversion on group A can be specified.
Conditions for A/D conversion start	• Software trigger • Synchronous trigger — Trigger by the multi-function timer pulse unit (MTU) or event link controller (ELC) • Asynchronous trigger — A/D conversion can be triggered by the external trigger ADTRG0# pin.	• Software trigger • Synchronous trigger — Trigger by the multi-function timer pulse unit (MTU) or event link controller (ELC) • Asynchronous trigger — A/D conversion can be triggered by the external trigger ADTRG0# pin.

Item	RX23E-A (S12ADE)	RX23E-B (S12ADE)
Functions	• Variable sampling state count • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function for A/D data registers • Compare function (window A and window B) • Ring buffer for when the compare function is used (x 16)	• Variable sampling state count • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function for A/D data registers • Compare function (window A and window B) • Ring buffer for when the compare function is used (x 16)
Interrupt sources	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan. • In group scan mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of group A scan. An A/D scan end interrupt request (GBADI) for group B can be generated on completion of group B scan. • When double trigger mode is selected in group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan of group A. An A/D scan end interrupt request (GBADI) for group B can be generated on completion of group B scan. • Startup of the DMA controller (DMAC) or data transfer controller (DTC) can be triggered by an S12ADI0 or GBADI interrupt.	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan. • In group scan mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of group A scan. An A/D scan end interrupt request (GBADI) for group B can be generated on completion of group B scan. • When double trigger mode is selected in group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan of group A. An A/D scan end interrupt request (GBADI) for group B can be generated on completion of group B scan. • Startup of the DMA controller (DMAC) or data transfer controller (DTC) can be triggered by an S12ADI0 or GBADI interrupt.

Item	RX23E-A (S12ADE)	RX23E-B (S12ADE)
Event link function	• An ELC event is generated on completion of scans other than group B scan in group scan mode. • An ELC event is generated on completion of group B scan in group scan mode. • An ELC event is generated on completion of all scans. • Scan can be started by a trigger output by the ELC. • An ELC event is generated according to the event conditions of the window compare function in single scan mode.	• An ELC event is generated on completion of scans other than group B scan in group scan mode. • An ELC event is generated on completion of group B scan in group scan mode. • An ELC event is generated on completion of all scans. • Scan can be started by a trigger output by the ELC. • An ELC event is generated according to the event conditions of the window compare function in single scan mode.
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.47 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX23E-A (S12ADE)	RX23E-B (S12ADE)
ADDRy	—	A/D data register y (y = 0 to 5)	A/D data register y (y = 0 to 7)
ADCSR	DBLANS[4:0]	Double-trigger target channel select bits One double-trigger target analog input channel is selected. These bit settings take effect only when double trigger mode is selected. b4 b0 0 0 0 0 0: AN000 0 0 0 0 1: AN001 0 0 0 1 0: AN002 0 0 0 1 1: AN003 0 0 1 0 0: AN004 0 0 1 0 1: AN005	Double-trigger target channel select bits One double-trigger target analog input channel is selected. These bit settings take effect only when double trigger mode is selected. b4 b0 0 0 0 0 0: AN000 0 0 0 0 1: AN001 0 0 0 1 0: AN002 0 0 0 1 1: AN003 0 0 1 0 0: AN004 0 0 1 0 1: AN005 0 0 1 1 0: AN006 0 0 1 1 1: AN007
ADANSA0	ANSA006	—	A/D conversion channel select bits
	ANSA007	—	A/D conversion channel select bits
ADANSB0	ANSB006	—	A/D conversion channel select bits
	ANSB007	—	A/D conversion channel select bits
ADADS0	ADS006	—	A/D-converted value addition/average function select bits
	ADS007	—	A/D-converted value addition/average function select bits
ADSSTRn	—	A/D sampling state register n (n = 0 to 5)	A/D sampling state register n (n = 0 to 7)

Register	Bit	RX23E-A (S12ADE)	RX23E-B (S12ADE)
ADCMPANSR0	CMPCHA006	—	Compare window A channel select bit
	CMPCHA007	—	Compare window A channel select bit
ADCMPLR0	CMPLCHA006	—	Compare window A comparison condition select bit
	CMPLCHA007	—	Compare window A comparison condition select bit
ADCMPSR0	CMPSTCHA006	—	Compare window A flag
	CMPSTCHA007	—	Compare window A flag
ADCMPBNSR	CMPCHB[5:0]	Compare window B channel select bits These bits are used to select the channels to be compared under the compare window B conditions. b5 b0 0 0 0 0 0 0: AN000 0 0 0 0 0 1: AN001 0 0 0 0 1 0: AN002 : 0 0 0 1 0 1: AN005 Settings other than the above are prohibited.	Compare window B channel select bits These bits are used to select the channels to be compared under the compare window B conditions. b5 b0 0 0 0 0 0 0: AN000 0 0 0 0 0 1: AN001 0 0 0 0 1 0: AN002 : : 0 0 0 1 1 0: AN006 0 0 0 1 1 1: AN007 Settings other than the above are prohibited.

2.17 Packages

As indicated in Table 2.48, there are discrepancies in the package drawing codes and availability of some package types, and this should be considered at the board design stage.

Table 2.48 Packages

Package type	RENESAS Code	
	RX23E-A	RX23E-B
100-pin LFQFP	×	○
100-pin TFBGA	×	○
80-pin LFQFP	×	○
64-pin LFQFP	×	○

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by **blue text**. Items that exist on both groups with different specifications are indicated by **red text**. Black text indicates there are no differences in item specifications between groups.

3.1 48-Pin Packages

Table 3.1 is a Comparative Listing of 48-Pin Package Pin Functions.

Table 3.1 Comparative Listing of 48-Pin Package Pin Functions

48-Pin LFQFP	RX23E-A	RX23E-B
1	AIN10/AN004/IEXC0 to IEXC3	DA0
2	AIN11/AN005/IEXC0 to IEXC3	AVSS0
3	AVSS0	AVCC0
4	AVCC0	MD/FINED
5	RES#	RES#
6	XTAL/P37	XTAL/P37
7	VSS	VSS
8	EXTAL/P36	EXTAL/P36
9	VCC	VCC
10	VCL	VCL
11	MD/FINED	P67/MTIOC4A/TMRI2/TXD6/SMOSI6/SSDA6
12	P35/NMI	P66/MTIOC4C/TMCI2/RXD6/SMISO6/SSCL6
13	P31/MTIOC1A/MTIOC4D/TMO3/CTS1#/ RTS1#/SS1#/IRQ1	P35/NMI
14	P30/MTIOC0A/MTIOC4B/TMCI3/POE8#/ RXD1/SMISO1/SSCL1/IRQ0	P31/MTIOC1A/MTIOC4D/MTCLKB/TMO3/ CACREF/TXD5/SMOSI5/SSDA5/RSPCKA/ IRQ1
15	P27/MTIOC2B/MTIOC4A/TMRI3/SCK1/IRQ3	P30/MTIOC2A/MTIOC4B/MTCLKD/TMCI3/ POE8#/RXD1/SMISO1/SSCL1/RXD5/ SMISO5/SSCL5/IRQ0
16	P26/MTIOC2A/MTIOC4C/TMO0/TXD1/ SMOSI1/SSDA1/IRQ2	P27/MTIOC2B/MTIOC4A/TMRI3/POE2#/ SCK5/CTS12#/RTS12#/SS12#/IRQ3
17	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ SCK1/MISOA/SDA/IRQ7	P26/MTIOC0A/MTIOC4C/MTCLKC/TMO0/ TXD1/SMOSI1/SSDA1/CTS5#/RTS5#/SS5#/ SCK12/IRQ2
18	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/ SMOSI1/SSDA1/MOSIA/SCL/IRQ6/ADTRG0#	P17/MTIOC0D/MTIOC3A/MTIOC3B/TMO1/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ MISOA/SDA/IRQ7
19	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/SSLA1/CRXD0/IRQ5	P16/MTIOC3C/MTIOC3D/TMO2/RXD12/ SMISO12/SSCL12/RXDX12/MOSIA/SCL/ ADTRG0#/IRQ6
20	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/SSLA3/CTXD0/IRQ4	P15/MTIOC0C/MTIOC4D/MTCLKB/TMCI2/ CTS1#/RTS1#/SS1#/SSLA0/CRXD0/IRQ5
21	PH3/MTIC5W/MTCLKB/TMCI0/POE2#/ CTS6#/RTS6#/SS6#/RSPCKA	P14/MTIOC0B/MTIOC3B/MTCLKA/TMRI2/ SCK1/CTXD0/CLKOUT/IRQ4
22	PH2/MTIC5V/MTCLKA/TMRI0/SCK5/MOSIA/ IRQ1	P55/MTIC5W/TMO0/CTS6#/RTS6#/SS6#
23	PH1/MTIC5U/MTCLKD/TMO0/POE2#/TXD5/ SMOSI5/SSDA5/SSLA0/IRQ0/CLKOUT	P54/MTIC5V/TMRI0/SSLA3/SCK6

48-Pin LFQFP	RX23E-A	RX23E-B
24	PH0/MTIOC0D/MTCLKC/TMRI0/CACREF/ RXD5/SMISO5/SSCL5/SSLA2	PC7/MTIOC4B/MTIOC3D/MTIC5U/TMCI0/ POE0#/TXD1/SMOSI1/SSDA1/SSLA1/IRQ7
25	PC7/MTIOC3A/MTCLKB/TMO2/CACREF/ TXD6/SMOSI6/SSDA6/MISOA	PB1/MTIOC4C/MTIOC3A/MTIC5V/TMRI0/ TMCI1/POE1#/RXD1/SMISO1/SSCL1/SSLA2
26	PC6/MTIOC3C/MTCLKA/TMCI2/RXD6/ SMISO6/SSCL6/MOSIA	VCC
27	PC5/MTIOC3B/MTCLKD/TMRI2/SCK5/SCK6/ SCK12/RSPCKA	PB0/MTIOC1B/MTIOC3C/MTIC5W/TMRI1/ POE3#/RSPCKA/CMPA2
28	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/ CTS5#/RTS5#/SS5#/CTS12#/RTS12#/ SS12#/SSLA0	VSS
29	PB1/MTIOC1B/MTIOC2A/TMRI1/POE1#/ TXD12/TXDX12/SIOX12/SMOSI12/SSDA12	AVCC0
30	VCC	AVSS0
31	PB0/MTIOC0C/TMCI0/POE3#/RXD12/ RXDX12/SMISO12/SSCL12/IRQ4	REFOUT
32	VSS	AIN0/AN000
33	AVCC0	AIN1/AN001
34	AVSS0	VREFL0/AIN2/IEXC0/VBIAS
35	REFOUT	VREFH0/AIN3/IEXC1
36	LSW	LSW
37	REF0N	REF0N
38	REF0P	REF0P
39	AIN0/IEXC0 to IEXC3	AIN4/AN002
40	AIN1/IEXC0 to IEXC3	AIN5/AN003
41	AIN2/IEXC0 to IEXC3	AIN8/IEXC0
42	AIN3/IEXC0 to IEXC3	AIN9/IEXC1
43	AIN4/IEXC0 to IEXC3/REF1N	AIN10/AN004/VBIAS
44	AIN5/IEXC0 to IEXC3/REF1P	AIN11/AN005
45	AIN6/AN000/IEXC0 to IEXC3	AIN12/AN006/REF1N
46	AIN7/AN001/IEXC0 to IEXC3	AIN13/AN007/REF1P
47	VREFL0/AIN8/AN002/IEXC0 to IEXC3	VREFH
48	VREFH0/AIN9/AN003/IEXC0 to IEXC3	VREFL

3.2 40-Pin Packages

Table 3.2 is a Comparative Listing of 40-Pin Package Pin Functions.

Table 3.2 Comparative Listing of 40-Pin Package Pin Functions

40-Pin HWQFN	RX23E-A	RX23E-B
1	AVSS0	DA0
2	AVCC0	AVSS0
3	RES#	AVCC0
4	XTAL/P37	MD/FINED
5	VSS	RES#
6	EXTAL/P36	XTAL/P37
7	VCC	VSS
8	VCL	EXTAL/P36
9	MD/FINED	VCC
10	P35/NMI	VCL
11	P31/MTIOC1A/MTIOC4D/TMO3/CTS1#/ RTS1#/SS1#/IRQ1	P35/NMI
12	P30/MTIOC0A/MTIOC4B/TMCI3/POE8#/ RXD1/SMISO1/SSCL1/IRQ0	P31/MTIOC1A/MTIOC4D/MTCLKB/TMO3/ CACREF/TXD5/SMOSI5/SSDA5/RSPCKA/ IRQ1
13	P27/MTIOC2B/MTIOC4A/TMRI3/SCK1/IRQ3	P30/MTIOC2A/MTIOC4B/MTCLKD/TMCI3/ POE8#/RXD1/SMISO1/SSCL1/RXD5/ SMISO5/SSCL5/IRQ0
14	P26/MTIOC2A/MTIOC4C/TMO0/TXD1/ SMOSI1/SSDA1/IRQ2	P27/MTIOC2B/MTIOC4A/TMRI3/POE2#/ SCK5/CTS12#/RTS12#/SS12#/IRQ3
15	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ SCK1/MISOA/SDA/IRQ7	P26/MTIOC0A/MTIOC4C/MTCLKC/TMO0/ TXD1/SMOSI1/SSDA1/CTS5#/RTS5#/SS5#/ SCK12/IRQ2
16	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/ SMOSI1/SSDA1/MOSIA/SCL/IRQ6/ADTRG0#	P17/MTIOC0D/MTIOC3A/MTIOC3B/TMO1/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ MISOA/SDA/IRQ7
17	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/SSLA1/CRXD0/IRQ5	P16/MTIOC3C/MTIOC3D/TMO2/RXD12/ SMISO12/SSCL12/RXDX12/MOSIA/SCL/ ADTRG0#/IRQ6
18	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/SSLA3/CTXD0/IRQ4	P15/MTIOC0C/MTIOC4D/MTCLKB/TMCI2/ CTS1#/RTS1#/SS1#/SSLA0/CRXD0/IRQ5
19	PH1/MTCLKD/TMO0/POE2#/TXD5/SMOSI5/ SSDA5/SSLA0/IRQ0/CLKOUT	P14/MTIOC0B/MTIOC3B/MTCLKA/TMRI2/ SCK1/CTXD0/CLKOUT/IRQ4
20	PH0/MTIOC0D/MTCLKC/TMRI0/CACREF/ RXD5/SMISO5/SSCL5/SSLA2	PC7/MTIOC4B/MTIOC3D/MTIC5U/TMCI0/ POE0#/TXD1/SMOSI1/SSDA1/SSLA1/IRQ7
21	PC5/MTIOC3B/MTCLKD/TMRI2/SCK5/ SCK12/RSPCKA	PB1/MTIOC4C/MTIOC3A/MTIC5V/TMRI0/ TMCI1/POE1#/RXD1/SMISO1/SSCL1/SSLA2
22	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/ CTS5#/RTS5#/SS5#/CTS12#/RTS12#/ SS12#/SSLA0	VCC
23	PB1/MTIOC1B/MTIOC2A/TMRI1/POE1#/ TXD12/TXDX12/SIOX12/SMOSI12/SSDA12	PB0/MTIOC1B/MTIOC3C/MTIC5W/TMRI1/ POE3#/RSPCKA/CMPA2
24	VCC	VSS
25	PB0/MTIOC0C/TMCI0/POE3#/RXD12/ RXDX12/SMISO12/SSCL12/IRQ4	PE0/MTCLKA/CACREF/SSLA3
26	VSS	AVCC0
27	AVCC0	AVSS0

40-Pin HWQFN	RX23E-A	RX23E-B
28	AVSS0	REFOUT
29	REFOUT	VREFL0/AIN2/IEXC0/VBIAS
30	LSW	VREFH0/AIN3/IEXC1
31	REF0N	REF0N
32	REF0P	REF0P
33	AIN0/IEXC0 to IEXC3	AIN4/AN002
34	AIN1/IEXC0 to IEXC3	AIN5/AN003
35	AIN4/IEXC0 to IEXC3/REF1N	AIN10/AN004/VBIAS
36	AIN5/IEXC0 to IEXC3/REF1P	AIN11/AN005
37	AIN6/AN000/IEXC0 to IEXC3	AIN12/AN006/REF1N
38	AIN7/AN001/IEXC0 to IEXC3	AIN13/AN007/REF1P
39	VREFL0/AIN8/AN002/IEXC0 to IEXC3	VREFH
40	VREFH0/AIN9/AN003/IEXC0 to IEXC3	VREFL

4. Important Information when Migrating Between MCUs

This section presents important information on differences between the RX23E-A Group and the RX23E-B Group.

Section 4.1, Notes on Function Configuration, presents information regarding the software.

4.1 Notes on Function Configuration

Some software that runs on the RX23E-A Group is compatible with the RX23E-B Group. Nevertheless, appropriate caution must be exercised due to differences in aspects such as operation timing and electrical characteristics.

This section provides software-related considerations regarding function settings that differ between the RX23E-A Group and RX23E-B Group.

For differences of modules and functions, refer to 2, Comparative Overview of Specifications. For further information, refer to the User's Manual: Hardware of the relevant MCU group, listed in 5, Reference Documents.

4.1.1 Initialization of Port Direction Register (PDR)

The method of initializing the PDR register differs between the RX130 Group and RX660 Group, even on products with the same pin count.

4.1.2 Operating Clock for DSAD

On the RX23E-B group, when the DSAD0 is to be used, set the frequency of peripheral module clock C (PCLKC) to divide by 2.

5. Reference Documents

User's Manual: Hardware

RX23E-A Group User's Manual: Hardware Rev.1.20 (R01UH0801EJ0120)
(The latest version can be downloaded from the Renesas Electronics website.)

RX23E-B Group User's Manual: Hardware Rev.1.00 (R01UH0972EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This module reflects the content of the following technical updates:

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Oct.10.23	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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