RX140 Group, RX210 Group

Differences Between the RX140 Group and the RX210 Group

Introduction

This application note is intended as a reference to points of difference between the peripheral functions, I/O registers, and pin functions of the RX140 Group and RX210 Group, as well as a guide to key points to consider when migrating between the two groups.

Unless specifically otherwise noted, the information in this application note applies to the 80-pin package version of the RX140 Group and the 145-pin package version of the RX210 Group (chip version B) as the maximum specifications. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the User's Manual: Hardware of the products in question.

Target Devices

RX140 Group and RX210 Group

Contents

1. Comparison of Built-In Functions of RX140 Group and RX210 Group

A comparison of the built-in functions of the RX140 Group and RX210 Group is provided below. For details of the functions, see section 2, Comparative Overview of Specifications and section 5, Reference Documents.

Table 1.1 is a comparison of built-in functions of RX140 Group and RX210 Group.

Table 1.1 Comparison of Built-In Functions of RX140 Group and RX210 Group

Function	RX210	RX140
CPU	●	
Operating modes	■	
Address space	▲	
Resets	■	
Option-setting memory (OFSM)	▲	
Voltage detection circuit (LVDAa): RX210, (LVDAb): RX140	■/▲	
Clock generation circuit	●/▲	
Clock frequency accuracy measurement circuit	●/▲	
Low power consumption	■/▲	
Register write protection function	●/▲	
Exception handling	●	
Interrupt controller (ICUb)	●/■	
Buses	●/■	
DMA controller (DMACA)	○	×
Data transfer controller (DTCa): RX210, (DTCb): RX140	●	
Event link controller (ELC)	■	
I/O ports	■/▲	
Multi-function pin controller (MPC)	●/▲	
Multi-function timer pulse unit 2 (MTU2a)	○	
Port output enable 2 (POE2a)	■	
16-bit timer pulse unit (TPUa)	○	×
8-bit timer (TMR): RX210, (TMRa): RX140	○	
Compare match timer (CMT)	■	
Realtime clock (RTCB): RX140, (RTCb): RX210	●	
Low-power timer (LPTa)	×	○
Watchdog timer (WDTA)	○	×
Independent watchdog timer (IWDTa)	▲	
Serial communications interface (SGIg, SCIk, SCIh): RX140, (SCIc, SCId): RX210	●/▲	
I^{2}C bus interface (RIICa): RX140, (RIIC): RX210	▲	
CAN module (RSCAN)	×	○
Serial peripheral interface (RSPIc): RX140, (RSPI): RX210	■/▲	
CRC calculator (CRC)	○	
Capacitive touch sensing unit (CTSU2SL, CTSU2L)	×	○
AESA	×	○
RNGA	×	○
12-bit A/D converter (S12ADE): RX140, (S12ADb): RX210	●/▲	
D/A converter (DAa): RX140, (DA): RX210	●/▲	
Temperature sensor (TEMPSA): RX140, (TEMPSa): RX210	▲	
Comparator A (CMPA)	○	×
Comparator B (CMPBa): RX140, (CMPB): RX210	●	
Data operation circuit (DOC)	○	
RAM	▲	

<table>
<tr><th>Function</th><th>RX210</th><th>RX140</th></tr>
<tr><td>E2 DataFlash (flash memory for data storage) (RX210)
ROM (flash memory for code storage) (RX210)
Flash memory (FLASH) (RX140)</td><td colspan="2">▲</td></tr>
<tr><td>Packages</td><td colspan="2">▲</td></tr>
</table>

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Differences in register specifications are not listed.

2.1 CPU

Table 2.1 is a comparative overview of CPU.

Table 2.1 Comparative Overview of CPU

Item	RX210	RX140
CPU	• Maximum operating frequency: 50 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Eight 32-bit registers — Accumulator: One 64-bit register • Basic instructions: 73 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits	• Maximum operating frequency: 48 MHz • 32-bit RX CPU (RXv2) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • Basic instructions: 75, variable-length instruction format • Floating point instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits
FPU	—	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard

2.2 Operating Modes

Table 2.2 is a comparative overview of operating modes, and Table 2.3 is a comparison of operating mode registers.

Table 2.2 Comparative Overview of Operating Modes

Item	RX210	RX140
Operating modes specified by mode setting pins	Single-chip mode	Single-chip mode
	Boot mode	Boot mode (SCI interface)
		Boot mode (FINE interface)
	User boot mode	—
Operating modes selected by register settings	Single-chip mode	—
	On-chip ROM disabled extended mode	—
	On-chip ROM enabled extended mode	—

Table 2.3 Comparison of Operating Mode Registers

Register	Bit	RX210	RX140
MDSR	—	Mode status register	—
SYSCR0	—	System control register 0	—

2.3 Address Space

Figure 2.1 is a comparative memory map of single-chip mode.

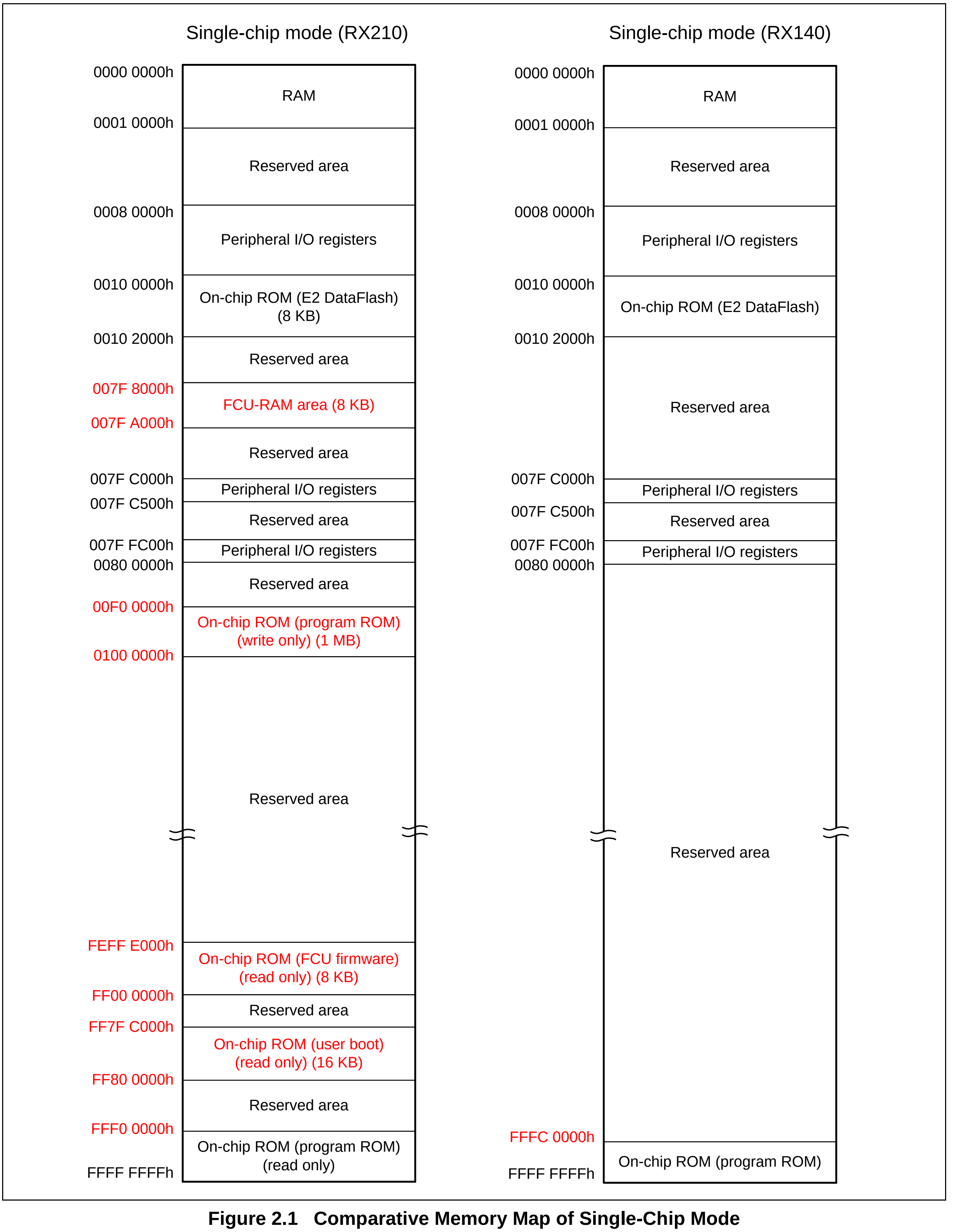

Figure 2.1 Comparative Memory Map of Single-Chip Mode

2.4 Resets

Table 2.4 is a comparative overview of resets, and Table 2.5 is a comparison of reset-related registers.

Table 2.4 Comparative Overview of Resets

Item	RX210	RX140
RES# pin reset	Voltage input to the RES# pin is driven low.	Voltage input to the RES# pin is driven low.
Power-on reset	VCC rises (voltage detection: VPOR).	VCC rises (voltage detection: VPOR).
Voltage monitoring 0 reset	VCC falls (voltage detection: Vdet0).	VCC falls (voltage detection: Vdet0).
Voltage monitoring 1 reset	VCC falls (voltage detection: Vdet1).	VCC falls (voltage detection: Vdet1).
Voltage monitoring 2 reset	VCC falls (voltage detection: Vdet2).	VCC falls (voltage detection: Vdet2).
Deep software standby reset	Deep software standby mode is canceled by an interrupt.	—
Independent watchdog timer reset	The independent watchdog timer underflows or a refresh error occurs.	The independent watchdog timer underflows or a refresh error occurs.
Watchdog timer reset	Watchdog timer underflow, or refresh error	—
Software reset	Register setting	Register setting

Table 2.5 Comparison of Reset-Related Registers

Register	Bit	RX210	RX140
RSTSR0	DPSRSTF	Deep software standby reset detect flag	—
RSTSR2	WDTRF	Watchdog timer reset detect flag	—

2.5 Option-Setting Memory

Figure 2.2 is a comparison of option-setting memory areas, and Table 2.6 is a comparison of option-setting memory registers.

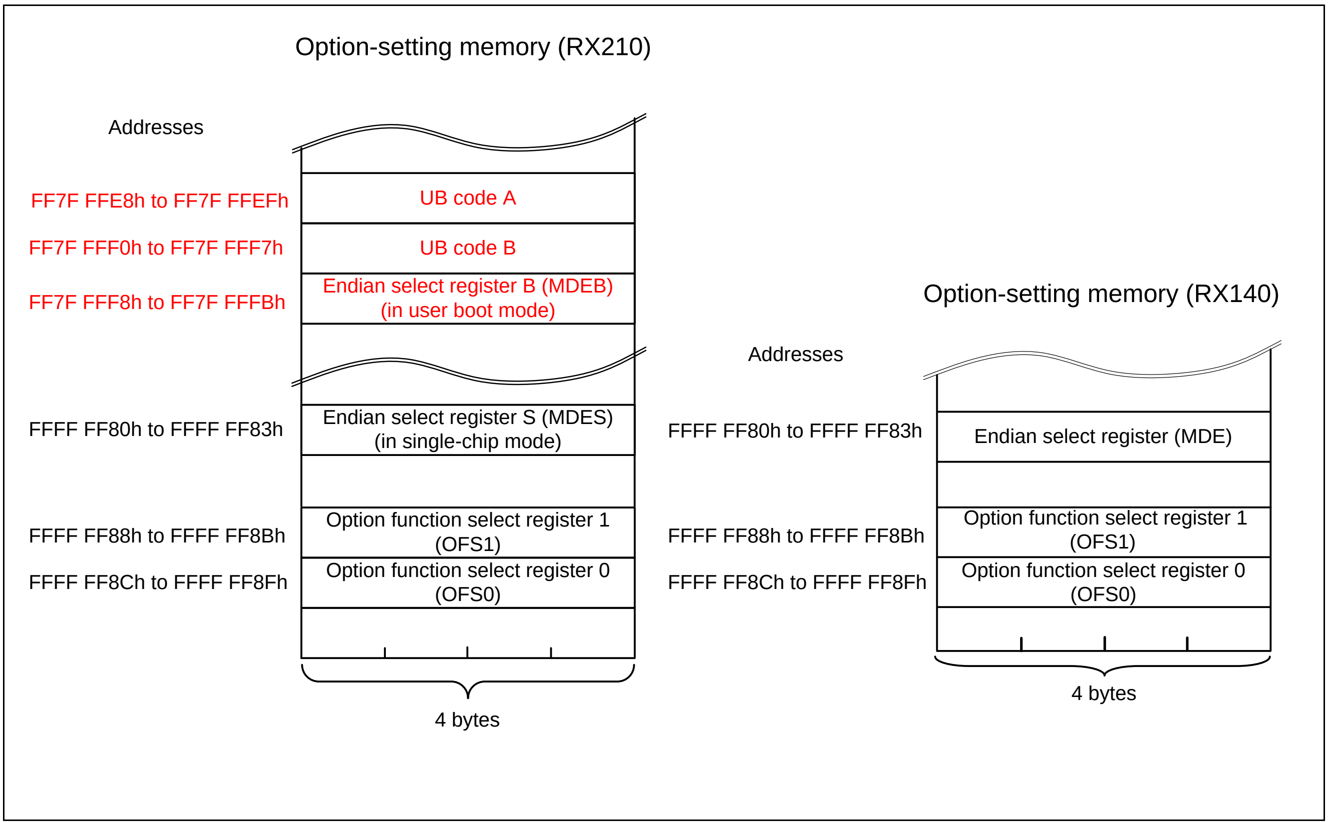

Figure 2.2 Comparison of Option-Setting Memory Areas

Table 2.6 Comparison of Option-Setting Memory Registers

Register	Bit	RX210 (OFSM)	RX140 (OFSM)
OFS0	IWDTTOPS[1:0]	IWDT timeout period select bits b3 b2 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh)	IWDT timeout period select bits b3 b2 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1,024 cycles (03FFh) 1 1: 2,048 cycles (07FFh)
	IWDTSLCSTP	IWDT sleep mode count stop control bit 0: Counting stop is disabled. 1: Counting stop is enabled when entering sleep, software standby, deep software standby, or all-module clock stop mode.	IWDT sleep mode count stop control bit 0: Counting stop is disabled. 1: Counting stop is enabled when entering sleep, software standby, or deep sleep mode.
	WDTSTRT	WDT start mode select bit	—
	WDTTOPS[1:0]	WDT timeout period select bits	—
	WDTCKS[3:0]	WDT clock frequency division ratio select bits	—
	WDTRPES[1:0]	WDT window end position select bits	—
	WDTRPSS[1:0]	WDT window start position select bits	—
	WDTRSTIRQS	WDT reset interrupt request select bit	—
OFS1	VDSEL[1:0]	Voltage detection 0 level select bits b1 b0 0 0: 3.80 V is selected 0 1: 2.80 V is selected 1 0: 1.90 V is selected 1 1: 1.72 V is selected	Voltage detection 0 level select bits b1 b0 0 0: 3.85 V is selected 0 1: 2.85 V is selected 1 0: 2.53 V is selected 1 1: 1.90 V is selected
	FASTSTUP	—	Power-on fast startup time bit
	HOCOFRQ[1:0]	—	HOCO frequency selection bits
MDEB MDES (RX210) MDE (RX140)	—	Endian select register B Endian select register S	Endian select register

2.6 Voltage Detection Circuit

Table 2.7 is a comparative overview of the voltage detection circuits, and Table 2.8 is a comparison of voltage detection circuit registers.

Table 2.7 Comparative Overview of Voltage Detection Circuits

Item		RX210 (LVDAb)			RX140 (LVDAb)		
		Voltage Monitoring 0	Voltage Monitoring 1	Voltage Monitoring 2	Voltage Monitoring 0	Voltage Monitoring 1	Voltage Monitoring 2
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	When voltage drops below Vdet0	When voltage rises above or drops past Vdet1	When voltage rises above or drops past Vdet2 Switching between VCC and the voltage input on the CMPA2 pin can be accomplished using the LVCMPCR.EXVCCINP2 bit.	When voltage drops below Vdet0	When voltage rises above or drops past Vdet1	When voltage rises above or drops past Vdet2 Switching between VCC and the voltage input on the CMPA2 pin can be accomplished using the LVCMPCR.EXVCCINP2 bit.
	Detection voltage	Selectable from four levels using the OFS1 register	Selectable from 16 levels using LVDLVLR.LVD1LVL[3:0] bits	Varies according to whether VCC or the CMPA2 pin input voltage is selected. Selectable from 16 levels using LVDLVLR.LVD2LVL[3:0] bits	Selectable from four levels using the OFS1 register	Selectable from 14 levels using LVDLVLR.LVD1LVL[3:0] bits	Selectable from four levels using LVDLVLR.LVD2LVL[1:0] bits
	Monitoring flags	—	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1 LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2 LVD2SR.LVD2DET flag: Vdet2 passage detection	—	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1 LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2 LVD2SR.LVD2DET flag: Vdet2 passage detection

Item		RX210 (LVDAb)			RX140 (LVDAb)		
		Voltage Monitoring 0	Voltage Monitoring 1	Voltage Monitoring 2	Voltage Monitoring 0	Voltage Monitoring 1	Voltage Monitoring 2
Voltage detection processing	Reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet0 > VCC: CPU restart timing after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable between after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC: CPU restart timing selectable between after specified time with VCC > Vdet2 or Vdet2 > VCC	Reset when Vdet0 > VCC: CPU restart timing after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable between after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC or CMPA2 pin: CPU restart timing selectable among after specified time with VCC or CMPA2 pin > Vdet2 or after specified time with Vdet2 > VCC or CMPA2 pin
	Interrupts	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
			Selectable between non-maskable or maskable interrupt	Selectable between non-maskable or maskable interrupt		Selectable between non-maskable or maskable interrupt	Selectable between non-maskable or maskable interrupt
			Interrupt request issued when Vdet1 > VCC, VCC > Vdet1, or both	Interrupt request issued when Vdet2 > VCC, VCC > Vdet2, or both		Interrupt request issued when Vdet1 > VCC, VCC > Vdet1, or both	Interrupt request issued when Vdet2 > VCC or CMPA2 pin, VCC or CMPA2 pin > Vdet2, or both
Digital filter	Enable/ disable switching	Digital filter function not available.	Available	Available	—	—	—
	Sampling time	—	1/n LOCO frequency × 2 (n: 1, 2, 4, 8)	1/n LOCO frequency × 2 (n: 1, 2, 4, 8)	—	—	—
Event link function		—	Available: Event output at Vdet1 passage detection	Available: Event output at Vdet1 passage detection	—	Available: Event output at Vdet1 passage detection	—

Table 2.8 Comparison of Voltage Detection Circuit Registers

Register	Bit	RX210 (LVDAb)	RX140 (LVDAb)
LVD1CR1	—	Voltage monitoring 1 circuit/ comparator A1 control register 1	Voltage monitoring 1 circuit control register 1
LVD1SR	—	Voltage monitoring 1 circuit/ comparator A1 status register	Voltage monitoring 1 circuit status register
LVD2CR1	—	Voltage monitoring 2 circuit/ comparator A2 control register 1	Voltage monitoring 2 circuit control register 1
LVD2SR	—	Voltage monitoring 2 circuit/ comparator A2 status register	Voltage monitoring 2 circuit status register
LVCMPCR	—	Voltage monitoring circuit/ comparator A control register	Voltage monitoring circuit control register
	EXVREFINP1	Comparator A1 reference voltage external input select bit	—
	EXVCCINP1	Comparator A1 comparison voltage external input select bit	—
	EXVREFINP2	Comparator A2 reference voltage external input select bit	—
	EXVCCINP2	Comparator A2 comparison voltage external input select bit	Voltage detection 2 comparison voltage external input select bit
	LVD1E	Voltage detection 1/comparator A1 enable bit 0: Voltage detection 1/comparator A1 circuit disabled 1: Voltage detection 1/comparator A1 circuit enabled	Voltage detection 1 enable bit 0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled
	LVD2E	Voltage detection 2/comparator A2 enable bit 0: Voltage detection 2/comparator A2 circuit disabled 1: Voltage detection 2/comparator A2 circuit enabled	Voltage detection 2 enable bit 0: Voltage detection 2 circuit disabled 1: Voltage detection 2 circuit enabled

Register	Bit	RX210 (LVDAb)	RX140 (LVDAb)
LVDLVLR	LVD1LVL[3:0]	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 0 0 0: 4.15 V 0 0 0 1: 4.00 V 0 0 1 0: 3.85 V 0 0 1 1: 3.70 V 0 1 0 0: 3.55 V 0 1 0 1: 3.40 V 0 1 1 0: 3.25 V 0 1 1 1: 3.10 V 1 0 0 0: 2.95 V 1 0 0 1: 2.80 V 1 0 1 0: 2.65 V 1 0 1 1: 2.50 V 1 1 0 0: 2.35 V 1 1 0 1: 2.20 V 1 1 1 0: 2.05 V 1 1 1 1: 1.90 V Settings other than the above are prohibited.	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 0 0 0: 4.29 V 0 0 0 1: 4.16 V 0 0 1 0: 4.03 V 0 0 1 1: 3.86 V 0 1 0 0: 3.10 V 0 1 0 1: 3.00 V 0 1 1 0: 2.90 V 0 1 1 1: 2.80 V 1 0 0 0: 2.68 V 1 0 0 1: 2.59 V 1 0 1 0: 2.48 V 1 0 1 1: 2.20 V 1 1 0 0: 1.96 V 1 1 0 1: 1.86 V Settings other than the above are prohibited.

Register	Bit	RX210 (LVDAb)	RX140 (LVDAb)
LVDLVLR	LVD2LVL[3:0] (RX210) LVD2LVL[1:0] (RX140)	Voltage detection 2 level select bits (Standard voltage during drop in voltage) (b7 to b4) (When LVCMPCR.EXVCCINP2 = 0 (VCC selected)) b7 b4 0 0 0 0: 4.15 V 0 0 0 1: 4.00 V 0 0 1 0: 3.85 V 0 0 1 1: 3.70 V 0 1 0 0: 3.55 V 0 1 0 1: 3.40 V 0 1 1 0: 3.25 V 0 1 1 1: 3.10 V 1 0 0 0: 2.95 V 1 0 0 1: 2.80 V 1 0 1 0: 2.65 V 1 0 1 1: 2.50 V 1 1 0 0: 2.35 V 1 1 0 1: 2.20 V 1 1 1 0: 2.05 V 1 1 1 1: 1.90 V (When LVCMPCR.EXVCCINP2 = 1 (CMPA2 selected)) b7 b4 0 0 0 1: 1.33 V Settings other than the above are prohibited.	Voltage detection 2 level select bits (Standard voltage during drop in voltage) (b5, b4) b5 b4 0 0: 4.32 V 0 1: 4.17 V 1 0: 4.03 V 1 1: 3.84 V
LVD1CR0	—	Voltage monitoring 1 circuit/ comparator A1 control register 0	Voltage monitoring 1 circuit control register 0
	LVD1RIE	Voltage monitoring 1/comparator A1 interrupt/reset enable bit	Voltage monitoring 1 interrupt/reset enable bit
	LVD1DFDIS	Voltage monitoring 1/comparator A1 digital filter disable mode select bit	—
	LVD1CMPE	Voltage monitoring 1 circuit/ comparator A1 comparison result output enable bit	Voltage monitoring 1 circuit comparison result output enable bit
	LVD1FSAMP [1:0]	Sampling clock select bits	—
	LVD1RI	Voltage monitoring 1 circuit/ comparator A1 mode select bit	Voltage monitoring 1 circuit mode select bit
	LVD1RN	Voltage monitoring 1/comparator A1 reset negation select bit	Voltage monitoring 1 reset negation select bit

Register	Bit	RX210 (LVDAb)	RX140 (LVDAb)
LVD2CR0	—	Voltage monitoring 2 circuit/ comparator A2 control register 0	Voltage monitoring 2 circuit control register 0
	LVD2RIE	Voltage monitoring 2/comparator A2 interrupt/reset enable bit	Voltage monitoring 2 interrupt/reset enable bit
	LVD2DFDIS	Voltage monitoring 2/comparator A2 digital filter disable mode select bit	—
	LVD2CMPE	Voltage monitoring 2 circuit/ comparator A2 comparison result output enable bit	Voltage monitoring 2 circuit comparison result output enable bit
	LVD2FSAMP [1:0]	Sampling clock select bits	—
LVD2CR0	LVD2RI	Voltage monitoring 2 circuit/ comparator A2 mode select bit	Voltage monitoring 2 circuit mode select bit
	LVD2RN	Voltage monitoring 2/comparator A2 reset negation select bit	Voltage monitoring 2 reset negation select bit

2.7 Clock Generation Circuit

Table 2.9 is a comparative overview of the clock generation circuits, and Table 2.10 is a comparison of clock generation circuit registers.

Table 2.9 Comparative Overview of Clock Generation Circuits

Item	RX210	RX140
Use	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, ROM, and RAM. • Of the peripheral module clocks (PCLKB and PCLKD) supplied to the peripheral modules, PCLKD is the operating clock for the S12AD, and PCLKB is the operating clock for modules other than S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the RTC-dedicated sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.	• Generates the system clock (ICLK) to be supplied to the CPU, DTC, ROM, and RAM. • Of the peripheral module clocks (PCLKB and PCLKD) supplied to the peripheral modules, PCLKD is the operating clock for the S12AD, and PCLKB is the operating clock for modules other than S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the RTC-dedicated sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT • Generates the LPT clock (LPTCLK) to be supplied to the LPT.
Operating frequency	• ICLK: 50 MHz (max.) • PCLKB: 32 MHz (max.) • PCLKD: 54 MHz (max.) • FCLK: — 4 MHz to 32 MHz (for programming and erasing the ROM and E2 DataFlash) — 32 MHz (max.) (for reading from the E2 DataFlash) • BCLK: 25 MHz (max.) • BCLK pin output: 12.5 MHz (max.) • CACCLK: Same as clock from respective oscillators • RTCSCLK: 32.768 kHz • IWDTCLK: 125 kHz	• ICLK: 48 MHz (max.) • PCLKB: 32 MHz (max.) • PCLKD: 48 MHz (max.) • FCLK: — 1 MHz to 48 MHz (for programming and erasing the ROM and E2 DataFlash) — 48 MHz (max.) (for reading from the E2 DataFlash) • CACCLK: Same as clock from respective oscillators • CANMCLK: 20 MHz (max.) • RTCSCLK: 32.768 kHz • IWDTCLK: 15 kHz • LPTCLK: Same as clock from selected oscillator

Item	RX210	RX140
Main clock oscillator	• Resonator frequency: 1 MHz to 20 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and MTU pin can be forcedly driven to high-impedance. • Drive capacity switching function	• Resonator frequency: 1 MHz to 20 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and MTU pin can be forcedly driven to high-impedance. • Drive capacity switching function
Sub-clock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal • Connection pin: XCIN, XCOUT • Drive capacity switching function	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal • Connection pins: XCIN and XCOUT • Drive capacity switching function
PLL circuit	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 12.5 MHz • Frequency multiplication ratio: Selectable from 8, 10, 12, 16, 20, 24, and 25 • VCO oscillation frequency: 50 MHz to 100 MHz	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 12 MHz • Frequency multiplication ratio: Selectable from 4 to 12 (increments of 0.5) • Oscillation frequency: 24 MHz to 48 MHz
High-speed on-chip oscillator (HOCO)	• Oscillation frequency: 32 MHz/36.864 MHz/40 MHz/50 MHz • HOCO power supply control	Oscillation frequency: 24 MHz, 32 MHz, 48 MHz
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 125 kHz	Oscillation frequency: 4 MHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 125 kHz	Oscillation frequency: 15 kHz
BCLK pin output control function	• Selectable between BCLK clock output or high-level output. • Output clock selectable between BCLK or BCLK/2.	—

Table 2.10 Comparison of Clock Generation Circuit Registers

Register	Bit	RX210	RX140
SCKCR	BCK[3:0]	External bus clock (BCLK) select bits	—
	PSTOP1	BCLK pin output control bit	—
SCKCR3	CKSEL[2:0]	Clock source select bits [Chip version A] b10 b8 0 0 0: LOCO 0 0 1: HOCO 0 1 1: Sub-clock oscillator 1 0 0: PLL circuit [Chip versions B and C] b10 b8 0 0 0: LOCO 0 0 1: HOCO 0 1 0: Main clock oscillator 0 1 1: Sub-clock oscillator 1 0 0: PLL circuit Settings other than above are prohibited.	Clock source select bits b10 b8 0 0 0: LOCO 0 0 1: HOCO 0 1 0: Main clock oscillator 0 1 1: Sub-clock oscillator 1 0 0: PLL circuit Settings other than above are prohibited.
VRCR	—	Voltage regulator control register	—
PLLCR	STC[4:0] (RX210) STC[5:0] (RX140)	Frequency multiplication factor select bits b12 b8 0 0 1 1 1: ×8 0 1 0 0 1: ×10 0 1 0 1 1: ×12 0 1 1 1 1: ×16 1 0 0 1 1: ×20 1 0 1 1 1: ×24 1 1 0 0 0: ×25 Settings other than above are prohibited.	Frequency multiplication factor select bits b13 b8 0 0 0 1 1 1: ×4 0 0 1 0 0 0: ×4.5 0 0 1 0 0 1: ×5 0 0 1 0 1 0: ×5.5 0 0 1 0 1 1: ×6 0 0 1 1 0 0: ×6.5 0 0 1 1 0 1: ×7 0 0 1 1 1 0: ×7.5 0 0 1 1 1 1: ×8 0 1 0 0 0 0: ×8.5 0 1 0 0 0 1: ×9 0 1 0 0 1 0: ×9.5 0 1 0 0 1 1: ×10 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12 Settings other than above are prohibited.
BCKCR	—	External bus clock control register	—

Register	Bit	RX210	RX140
SOSCCR	SOSTP	Sub-clock oscillator stop bit	Sub-clock oscillator stop bit This bit is not initialized by reset sources other than a power-on reset.
		Initial value after a reset differs.	
HOCOCR2	—	High-speed on-chip oscillator control register 2	—
OSCOVFSR	—	—	Oscillation stabilization flag register
MOSCWTCR	—	—	Main clock oscillator wait control register
LOFCR	—	—	Low-speed on-chip oscillator forced oscillation control register
CKOCR	—	—	CLKOUT output control register
MOFCR	MODRV[2:0]	Main clock oscillator drive capability switch bits	—
	MODRV21	—	Main clock oscillator drive capability switch bit
	MODRV2 [1:0]	Main clock oscillator drive capability switch 2 bits	—
LOCOTRR2	—	—	Low-speed on-chip oscillator trimming register 2
ILOCOTRR	—	—	IWDT-dedicated on-chip oscillator trimming register
HOCOPCR	—	High-speed on-chip oscillator power supply control register	—
HOCOTRRn	—	High-speed on-chip oscillator trimming register n (n = 0 to 3)	High-speed on-chip oscillator trimming register n (n = 0)
PLLPCR	—	PLL power control register	—
SOMCR	—	—	Sub-clock oscillator mode control register

2.8 Clock Frequency Accuracy Measurement Circuit

Table 2.11 is a comparative overview of clock frequency accuracy measurement circuits, and Table 2.12 is a comparison of clock frequency accuracy measurement circuit registers.

Table 2.11 Comparative Overview of Clock Frequency Accuracy Measurement Circuits

Item	RX210 (CAC)	RX140 (CAC)
Measurement target clocks	The frequency of the following clocks can be measured. • Clock output from main clock oscillator (main clock) • Clock output from sub-clock oscillator (sub-clock) • Clock output from high-speed on-chip oscillator (HOCO clock) • Clock output from low-speed on-chip oscillator (LOCO clock) • Clock output from IWDT-dedicated on-chip oscillator (IWDTCLK clock)	The frequency of the following clocks can be measured. • Main clock • Sub-clock • HOCO clock • LOCO clock • IWDT-dedicated clock • Peripheral module clock B (PCLKB)
Measurement reference clocks	—	• External clock input on CACREF pin • Main clock • Sub-clock • HOCO clock • LOCO clock • IWDT-dedicated clock (IWDTCLK) • Peripheral module clock B (PCLKB)
Selectable function	Digital filter function	Digital filter function
Interrupt sources	• Measurement end interrupt • Frequency error interrupt • Overflow interrupt	• Measurement end interrupt • Frequency error interrupt • Overflow interrupt
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Table 2.12 Comparison of Clock Frequency Accuracy Measurement Circuit Registers

Register	Bit	RX210 (CAC)	RX140 (CAC)
CACR1	FMCS[2:0]	Frequency measurement clock select bits [Chip version A] b3 b1 0 0 1: Clock output from sub-clock oscillator 0 1 0: Clock output from high-speed on-chip oscillator 0 1 1: Clock output from low-speed on-chip oscillator 1 0 0: Clock output from IWDT-dedicated on-chip oscillator [Chip versions B and C] b3 b1 0 0 0: Clock output from main clock oscillator 0 0 1: Clock output from sub-clock oscillator 0 1 0: Clock output from high-speed on-chip oscillator 0 1 1: Clock output from low-speed on-chip oscillator 1 0 0: Clock output from IWDT-dedicated on-chip oscillator Settings other than the above are prohibited.	Measurement target clock select bits b3 b1 0 0 0: Main clock 0 0 1: Sub-clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock B (PCLKB) Settings other than the above are prohibited.

Register	Bit	RX210 (CAC)	RX140 (CAC)
CACR2	RSCS[2:0]	Reference signal generation clock select bits [Chip version A] b3 b1 0 0 1: Clock output from sub-clock oscillator 0 1 0: Clock output from high-speed on-chip oscillator 0 1 1: Clock output from low-speed on-chip oscillator 1 0 0: Clock output from IWDT-dedicated on-chip oscillator [Chip versions B and C] b3 b1 0 0 0: Clock output from main clock oscillator 0 0 1: Clock output from sub-clock oscillator 0 1 0: Clock output from high-speed on-chip oscillator 0 1 1: Clock output from low-speed on-chip oscillator 1 0 0: Clock output from IWDT-dedicated on-chip oscillator Settings other than the above are prohibited.	Measurement reference clock select bits b3 b1 0 0 0: Main clock 0 0 1: Sub-clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock B (PCLKB) Settings other than the above are prohibited.

2.9 Low Power Consumption

Table 2.13 is a comparative overview of the low power consumption functions, Table 2.14 is a comparison of procedures for entering and exiting low power consumption modes and operating states in each mode, and Table 2.15 is a comparison of low power consumption registers.

Table 2.13 Comparative Overview of Low Power Consumption Functions

Item	RX210	RX140
Reducing power consumption by switching clock signals	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKB), S12AD clock (PCLKD), external bus clock (BCLK), and FlashIF clock (FCLK).	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKB), S12AD clock (PCLKD), and FlashIF clock (FCLK).
BCLK output control function	BCLK output or high-level output can be selected.	—
Module stop function	Each peripheral module can be stopped independently by the module stop control register.	Each peripheral module can be stopped independently by the module stop control register.
Function for transition to low power consumption mode	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.
Low power consumption modes	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode	• Sleep mode • Deep sleep mode • Software standby mode • Snooze mode
Function for lower operating power consumption	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. [Chip versions A and C] • Five operating power control modes are available — High-speed operating mode — Middle-speed operating mode 1A — Middle-speed operating mode 1B — Low-speed operating mode 1 — Low-speed operating mode 2 [Chip version B] • Seven operating power control modes are available — High-speed operating mode — Middle-speed operating mode 1A — Middle-speed operating mode 1B — Middle-speed operating mode 2A — Middle-speed operating mode 2B — Low-speed operating mode 1 — Low-speed operating mode 2	• Power consumption can be reduced in normal operation, sleep mode, deep sleep mode, and snooze mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Four operating power control modes are available — High-speed operating mode — Middle-speed operating mode — Middle-speed operating mode 2 — Low-speed operating mode

Table 2.14 Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX210	RX140
Sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	USB-dedicated PLL	Operation possible	—
	CPU	Stopped (retained)	Stopped (retained)
	RAM0 (0000 0000h to 0000 FFFFh) RAM1 (0001 0000h to 0001 7FFFh): RX210	Operation possible (retained)	Operation possible (retained)
	DTC	—	Operation possible
	Flash memory	Operation	Operation
	Watchdog timer (WDT)	Stopped (retained)	—
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	8-bit timer (unit 0, unit 1) (TMR)	Operation possible	—
	Low-power timer (LPT)	—	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Operation possible	Operation possible
	I/O ports	Operation	Operation
	RTCOUT output	—	Operation possible
	CLKOUT output	—	Operation possible
	Comparator B	—	Operation possible
All-module clock stop mode	Transition method	Control register + instruction	—
	Method of cancellation other than reset	Interrupt	—
	State after cancellation	Program execution state (interrupt processing)	—
	Main clock oscillator	Operation possible	—
	Sub-clock oscillator	Operation possible	—
	High-speed on-chip oscillator	Operation possible	—
	Low-speed on-chip oscillator	Operation possible	—
	IWDT-dedicated on-chip oscillator	Operation possible	—
	PLL	Operation possible	—
	CPU	Stopped (retained)	—

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX210	RX140
All-module clock stop mode	RAM0 (0000 0000h to 0000 FFFFh) RAM1 (0001 0000h to 0001 7FFFh):	Stopped (retained)	—
	Flash memory	Stopped (retained)	—
	Watchdog timer (WDT)	Stopped (retained)	—
	Independent watchdog timer (IWDT)	Operation possible	—
	Realtime clock (RTC)	Operation possible	—
	8-bit timer (unit 0, unit 1) (TMR)	Operation possible	—
	Voltage detection circuit (LVD)	Operation possible	—
	Power-on reset circuit	Operation	—
	Peripheral modules	Stopped (retained)	—
	I/O ports	Retained	—
Deep sleep mode	Transition method	—	Control register + instruction
	Method of cancellation other than reset	—	Interrupt
	State after cancellation	—	Program execution state (interrupt processing)
	Main clock oscillator	—	Operation possible
	Sub-clock oscillator	—	Operation possible
	High-speed on-chip oscillator	—	Operation possible
	Low-speed on-chip oscillator	—	Operation possible
	IWDT-dedicated on-chip oscillator	—	Operation possible
	PLL	—	Operation possible
	CPU	—	Stopped (retained)
	RAM0 (0000 0000h to 0000 FFFFh)	—	Stopped (retained)
	DTC	—	Stopped (retained)
	Flash memory	—	Stopped (retained)
	Independent watchdog timer (IWDT)	—	Operation possible
	Realtime clock (RTC)	—	Operation possible
	Low-power timer (LPT)	—	Operation possible
	Voltage detection circuit (LVD)	—	Operation possible
	Power-on reset circuit	—	Operation
	Peripheral modules	—	Operation possible
	I/O ports	—	Operation
	RTCOUT output	—	Operation possible
	CLKOUT output	—	Operation possible
	Comparator B	—	Operation possible
Software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX210	RX140
Software standby mode	Main clock oscillator	Stopped	Stopped
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Stopped	Stopped
	CPU	Stopped (retained)	Stopped (retained)
	RAM0 (0000 0000h to 0000 FFFFh) RAM1 (0001 0000h to 0001 7FFFh): RX210	Stopped (retained)	Stopped (retained)
	DTC	—	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	Watchdog timer (WDT)	Stopped (retained)	—
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	Low-power timer (LPT)	—	Operation possible
	8-bit timer (unit 0, unit 1) (TMR)	Stopped (retained)	—
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained
	RTCOUT output	—	Operation possible
	CLKOUT output	—	Operation possible
	Comparator B	—	Operation possible
Snooze mode	Transition method	—	When snooze transition conditions are met while in software standby mode
	Method of cancellation other than reset	—	Interrupt or occurrence of snooze end condition
	State after cancellation	—	Program execution state (interrupt processing) or software standby mode
	Main clock oscillator	—	Operation possible
	Sub-clock oscillator	—	Operation possible
	High-speed on-chip oscillator	—	Operation possible
	Low-speed on-chip oscillator	—	Operation possible
	IWDT-dedicated on-chip oscillator	—	Operation possible
	PLL	—	Operation possible
	CPU	—	Stopped (retained)
	RAM0 (0000 0000h to 0000 FFFFh)	—	Operation possible (retained)

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX210	RX140
Snooze mode	DTC	—	Operation possible
	Flash memory	—	Stopped (retained)
	Independent watchdog timer (IWDT)	—	Operation possible
	Realtime clock (RTC)	—	Operation possible
	Low-power timer (LPT)	—	Operation possible
	Voltage detection circuit (LVD)	—	Operation possible
	Power-on reset circuit	—	Operation
	Peripheral modules	—	Operation possible
	I/O ports	—	Operation
	RTCOUT output	—	Operation possible
	CLKOUT output	—	Operation possible
	Comparator B	—	Operation possible
Deep software standby mode	Transition method	Control register + instruction	—
	Method of cancellation other than reset	Interrupt	—
	State after cancellation	Program execution state (reset processing)	—
	Main clock oscillator	Stopped	—
	Sub-clock oscillator	Operation possible	—
	High-speed on-chip oscillator	Stopped	—
	Low-speed on-chip oscillator	Stopped	—
	IWDT-dedicated on-chip oscillator	Stopped (undefined)	—
	PLL	Stopped	—
	CPU	Stopped (undefined)	—
	RAM0 (0000 0000h to 0000 FFFFh) RAM1 (0001 0000h to 0001 7FFFh): RX210	Stopped (undefined)	—
	Flash memory	Stopped (retained)	—
	Watchdog timer (WDT)	Stopped (undefined)	—
	Independent watchdog timer (IWDT)	Stopped (undefined)	—
	Realtime clock (RTC)	Operation possible	—
	8-bit timer (unit 0, unit 1) (TMR)	Stopped (undefined)	—
	Voltage detection circuit (LVD)	Operation possible	—
	Power-on reset circuit	Operation	—
	Peripheral modules	Stopped (undefined)	—
	I/O ports	Retained	—

Note: "Operation possible" means that whether the state is operating or stopped is controlled by the control register setting.
"Stopped (retained)" means that internal register values are retained and internal operations are suspended.
"Stopped (undefined)" means that internal register values are undefined and power is not supplied to the internal circuit.

Table 2.15 Comparison of Low Power Consumption Registers

Register	Bit	RX210	RX140
SBYCR	—	Standby control register	Standby control register
		Initial value after a reset differs.	
	OPE	Output port enable bit	—
MSTPCRA	MSTPA13	16-bit timer pulse unit module stop bit	—
	MSTPA14	Compare match timer (unit 1) module stop bit	—
	MSTPA24	Module stop A24 bit	—
	MSTPA27	Module stop A27 bit	—
	MSTPA28	DMA controller/data transfer controller module stop bit Target module: DMAC/DTC	Data transfer controller module stop bit Target module: DTC
	MSTPA29	Module stop A29 bit	—
	ACSE	All-module clock stop mode enable bit	—
MSTPCRB	MSTPB0	—	CAN module module stop bit
	MSTPB8	Temperature sensor module stop bit	—
	MSTPB24	Serial communication interface 7 module stop bit	—
	MSTPB27	Serial communication interface 4 module stop bit	—
	MSTPB28	Serial communication interface 3 module stop bit	—
	MSTPB29	Serial communication interface 2 module stop bit	—
	MSTPB31	Serial communication interface 0 module stop bit	—
MSTPCRC	MSTPC1	RAM1 module stop bit	—
	MSTPC24	Serial communication interface 11 module stop bit	—
	MSTPC25	Serial communication interface 10 module stop bit	—
	DSLPE	—	Deep sleep mode enable bit
MSTPCRD	—	—	Module stop control register D

Register	Bit	RX210	RX140
OPCCR	OPCM [2:0]	Operating power control mode select bits [Chip versions A and C] b2 b0 0 0 0: High-speed operating mode 0 1 0: Middle-speed operating mode 1A 0 1 1: Middle-speed operating mode 1B 1 1 0: Low-speed operating mode 1 1 1 1: Low-speed operating mode 2 [Chip version B] b2 b0 0 0 0: High-speed operating mode 0 1 0: Middle-speed operating mode 1A 0 1 1: Middle-speed operating mode 1B 1 0 0: Middle-speed operating mode 2A 1 0 1: Middle-speed operating mode 2B 1 1 0: Low-speed operating mode 1 1 1 1: Low-speed operating mode 2 Settings other than the above are prohibited.	Operating power control mode select bits b2 b0 0 0 0: High-speed operating mode 0 1 0: Middle-speed operating mode 1 0 0: Middle-speed operating mode 2 Settings other than the above are prohibited.
SOPCCR	—	—	Sub operating power control register
RSTCKCR	RSTCKSEL [2:0]	Sleep mode return clock source select bits [Chip version A] b2 b0 0 0 1: HOCO is selected. [Chip versions B and C] b2 b0 0 0 1: HOCO is selected. 0 1 0: Main clock oscillator is selected. Settings other than above are prohibited while the RSTCKEN bit is set to 1.	Sleep mode return clock source select bits b2 b0 0 0 0: LOCO is selected. 0 0 1: HOCO is selected.*1 0 1 0: Main clock oscillator is selected. Settings other than above are prohibited while the RSTCKEN bit is set to 1.
SNZCR	—	—	Snooze control register
SNZCR2	—	—	Snooze control register 2
MOSCWTCR	—	Main clock oscillator wait control register	—
SOSCWTCR	—	Sub-clock oscillator wait control register	—
PLLWTCR	—	PLL wait control register	—

Register	Bit	RX210	RX140
HOCOWTCR2	—	HOCO wait control register 2	—
DPSBYCR	—	Deep standby control register	—
DPSIER0	—	Deep standby interrupt enable register 0	—
DPSIER2	—	Deep standby interrupt enable register 2	—
DPSIFR0	—	Deep standby interrupt flag register 0	—
DPSIFR2	—	Deep standby interrupt flag register 2	—
DPSIEGR0	—	Deep standby interrupt edge register 0	—
DPSIEGR2	—	Deep standby interrupt edge register 2	—
FHSSBYCR	—	Flash HOCO software standby control register	—
DPSBKRy	—	Deep standby backup register (y = 0 to 31)	—

Note: 1. Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

2.10 Register Write Protection Function

Table 2.16 is a comparative overview of the register write protection functions, and Table 2.17 is a comparison of register write protection function registers.

Table 2.16 Comparative Overview of Register Write Protection Functions

Item	RX210	RX140
PRC0 bit	Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, HOCOCR2 HOCOTRR0, HOCOTRR1, HOCOTRR2, HOCOTRR3	Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, LOFCR, OSTDCR, OSTDSR, CKOCR, LOCOTRR2, ILOCOTRR2, HOCOTRR0,SOMCR
PRC1 bit	• Register related to the operating modes: SYSCR0, SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR, RSTCKCR, MOSCWTCR, SOSCWTCR, PLLWTCR, DPSBYCR, DPSIER0, DPSIER2, DPSIFR0, DPSIFR2, DPSIEGR0, DPSIEGR2, HSSYCR, HOCOWTCR2 • Registers related to the clock generation circuit: MOFCR, HOCOPCR, PLLPCR (Chip version B) • Software reset register: SWRR	• Register related to the operating modes: SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, SOPCCR, SNZCR, SNZCR2 • Registers related to the clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR
PRC2 bit	VRCR register	Registers related to the low power timer: LPTCR1, LPTCR2, LPTCR3, LPTPRD, LPCMR0, LPCMR1, LPWUCR
PRC3 bit	Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

Table 2.17 Comparison of Register Write Protection Function Registers

Register	Bit	RX210	RX140
PRCR	PRC1	Protect bit 1 Enables writing to the registers related to operating modes, low power consumption functions, and software reset.	Protect bit 1 Enables writing to the registers related to operating modes, low power consumption functions, the clock generation circuit, and software reset.
	PRC2	Protect bit 2 Enables writing to the VRCR register.	Protect bit 2 Enables writing to the registers related to the low-power timer.

2.11 Exception Handling

Table 2.18 is a comparative overview of exception handling, Table 2.19 is a comparative listing of vectors, and Table 2.20 is a comparative listing of instructions for returning from exception handling routines.

Table 2.18 Comparative Overview of Exception Handling

Item	RX210	RX140
Exception events	• Undefined instruction exception • Privileged instruction exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap	• Undefined instruction exception • Privileged instruction exception • Floating-point exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap

Table 2.19 Comparative Listing of Vectors

Item		RX210	RX140
Undefined instruction exception		Fixed vector table	Exception vector table (EXTB)
Privileged instruction exception		Fixed vector table	Exception vector table (EXTB)
Floating-point exception		—	Exception vector table (EXTB)
Reset		Fixed vector table	Exception vector table (EXTB)
Non-maskable interrupt		Fixed vector table	Exception vector table (EXTB)
Interrupt	Fast interrupt	FINTV	FINTV
	Other than fast interrupt	Relocatable vector table (INTB)	Relocatable vector table (INTB)
Unconditional trap		Relocatable vector table (INTB)	Relocatable vector table (INTB)

Table 2.20 Comparative Listing of Instructions for Returning from Exception Handling Routines

Item		RX210	RX140
Undefined instruction exception		RTE	RTE
Privileged instruction exception		RTE	RTE
Floating-point exception		—	RTE
Reset		Return not possible	Return not possible
Non-maskable interrupt		Return not possible	Prohibited
Interrupt	Fast interrupt	RTFI	RTFI
	Other than fast interrupt	RTE	RTE
Unconditional trap		RTE	RTE

2.12 Interrupt Controller

Table 2.21 is a comparative overview of the interrupt controllers, and Table 2.22 is a comparison of interrupt controller registers.

Table 2.21 Comparative Overview of Interrupt Controllers

Item		RX210 (ICUb)	RX140 (ICUb)
Interrupts	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection The detection method is fixed for each connected peripheral module source.	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection The detection method is fixed for each connected peripheral module source.
	External pin interrupts	• Interrupts from pins IRQ0 to IRQ7 • Number of sources: 8 • Interrupt detection: Ability to set as source detection of low level, falling edge, rising edge, or rising and falling edges • Digital filter function: Supported	• Interrupts from pins IRQ0 to IRQ7 • Number of sources: 8 • Interrupt detection: Ability to set as source detection of low level, falling edge, rising edge, or rising and falling edges • Digital filter function: Supported
	Software interrupts	• Interrupt generated by writing to a register • Number of sources: 1	• Interrupt generated by writing to a register • Number of sources: 1
	Event link interrupts	An ELSR18I or ELSR19I interrupt can be generated by an ELC event.	An ELSR8I or ELSR18I interrupt can be generated by an ELC event.
	Interrupt priority	Specified by registers.	Specified by registers.
	Fast interrupt function	Faster interrupt handling by the CPU can be specified for a single interrupt source only.	Faster interrupt handling by the CPU can be specified for a single interrupt source only.
	DTC and DMAC control (RX210) DTC control (RX140)	The DTC and DMAC can be activated by an interrupt source.	The DTC can be activated by an interrupt source.
Non-maskable interrupts	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection: Falling edge or rising edge • Digital filter function: Supported	• Interrupt from the NMI pin • Interrupt detection: Falling edge or rising edge • Digital filter function: Supported
	Oscillation stop detection interrupt	Interrupt on detection of oscillation having stopped	Interrupt on detection of oscillation having stopped
	WDT underflow/ refresh error interrupt	Interrupt on an underflow of the down counter or occurrence of a refresh error	—
	IWDT underflow/ refresh error interrupt	Interrupt on an underflow of the down counter or occurrence of a refresh error	Interrupt on an underflow of the down counter or occurrence of a refresh error
	Voltage monitoring 1 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)

Item		RX210 (ICUb)	RX140 (ICUb)
Non-maskable interrupts	Voltage monitoring 2 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)
Return from low power consumption state		• Sleep mode: Return is initiated by a non-maskable interrupt or any other interrupt source. • All-module clock stop mode: Return is initiated by non-maskable interrupts, IRQ0 to IRQ7 interrupts, TMR interrupts, or RTC alarm/periodic interrupts. • Software standby mode: Return is initiated by a non-maskable interrupt, interrupt IRQ0 to IRQ7, or an RTC alarm or periodic interrupt.	• Sleep mode and deep sleep mode: Return is initiated by a non-maskable interrupt or any other interrupt source. • Software standby mode: Return is initiated by non-maskable interrupts (excluding oscillation stop detection interrupts), external pin interrupts (IRQ0 to IRQ7), peripheral interrupts (voltage monitoring 1, voltage monitoring 2, RTC alarm/periodic), or the ELSR8I interrupt (LPT dedicated interrupt). • Snooze mode: Return is initiated by non-maskable interrupts (excluding oscillation stop detection interrupts), external pin interrupts (IRQ0 to IRQ7), peripheral interrupts (voltage monitoring 1, voltage monitoring 2, RTC alarm/periodic), or the SNZI interrupt (snooze release interrupt).

Table 2.22 Comparison of Interrupt Controller Registers

Register	Bit	RX210 (ICUb)	RX140 (ICUb)
DTCERn	DTCE	DTC activation enable bit 0: DTC activation is disabled. 1: DTC activation is enabled.	DTC transfer request enable bit 0: Source of interrupt to CPU selected. 1: DTC activation source selected.
DMRSRm	—	DMAC activation request select register m (DMRSRm) (m = DMAC channel number)	—
NMISR	WDTST	WDT underflow/refresh error status flag	—
NMIER	WDTEN	WDT underflow/refresh error enable bit	—
NMICLR	WDTCLR	WDT clear bit	—

2.13 Buses

Table 2.23 is a comparative overview of the buses, and Table 2.24 is a comparison of bus registers.

Table 2.23 Comparative Overview of Buses

Bus Type		RX210	RX140
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	Connected to RAM	Connected to RAM
	Memory bus 2	Connected to ROM	Connected to ROM
Internal main buses	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DTC and DMAC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules (modules other than those connected to internal peripheral bus 1) • Operates in synchronization with the peripheral-module clock (PCLKB, PCLKD)	• Connected to peripheral modules • Operates in synchronization with the peripheral-module clock (PCLKB, PCLKD)
	Internal peripheral bus 3	—	• Connected to peripheral modules (CTSU, RSCAN) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 6	• Connected to ROM (P/E) and E2 DataFlash • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to ROM (P/E) and E2 DataFlash • Operates in synchronization with the FlashIF clock (FCLK)

Bus Type		RX210	RX140
External bus	CS area	• Connected to the external devices • Operates in synchronization with the external-bus clock (BCLK)	—

Table 2.24 Comparison of Bus Registers

Register	Bit	RX210	RX140
CSnCR	—	CSn control register (n = 0 to 3)	—
CSnREC	—	CSn recovery cycle register (n = 0 to 3)	—
CSRECEN	—	CS recovery cycle insertion enable register	—
CSnMOD	—	CSn mode register (n = 0 to 3)	—
CSnWCR1	—	CSn wait control register 1 (n = 0 to 3)	—
CSnWCR2	—	CSn wait control register 2 (n = 0 to 3)	—
BERSR1	MST[2:0]	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved
BUSPRI	BPEB[1:0]	External bus priority control bits	—

2.14 Data Transfer Controller

Table 2.25 is a comparative overview of the data transfer controllers, and Table 2.26 is a comparison of data transfer controller registers.

Table 2.25 Comparative Overview of Data Transfer Controllers

Item	RX210 (DTCa)	RX140 (DTCb)
Number of transfer channels	—	Equal to number of all interrupt sources that can start a DTC transfer.
Transfer modes	• Normal transfer mode — A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address returns to the transfer start address when the number of data transfers equals the repeat size. — The maximum repeat size is 256 data units. • Block transfer mode — A single activation leads to the transfer of a single block of data. — The maximum block size is 256 data units.	• Normal transfer mode — A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address returns to the transfer start address when the number of data transfers equals the repeat size. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, or 1,024 bytes. • Block transfer mode — A single activation leads to the transfer of a single block of data. — The maximum block size is 256 × 32 bits = 1,024 bytes.
Transfer channels	Channel transfer corresponding to the interrupt source is possible (transferred by DTC activation request from the ICU).	—
Chain transfer function	• Multiple data transfer types can be executed sequentially in response to a single transfer request. • Either "performed only when the transfer counter becomes 0" or "every time" can be selected for chain transfer.	• Multiple data transfer types can be executed sequentially in response to a single transfer request. • Either "performed only when the transfer counter reaches 0" or "every time" can be selected.
Sequence transfer	—	A complex series of transfers can be registered as a sequence. Any sequence can be selected by the transfer data and executed. • Only one sequence transfer trigger source can be selected at a time. • Up to 256 sequences can correspond to a single trigger source. • The data that is initially transferred in response to a transfer request determines the sequence. • The entire sequence can be executed on a single request, or the sequence can be suspended in the middle and resumed on the next transfer request (sequence division).

Item	RX210 (DTCa)	RX140 (DTCb)
Transfer space	• 16 MB in short-address mode (within 0000 0000h to 007F FFFFh or FF80 0000h to FFFF FFFFh, excluding reserved areas) • 4 GB in full-address mode (within 0000 0000h to FFFF FFFFh, excluding reserved areas)	• 16 MB in short-address mode (within 0000 0000h to 007F FFFFh or FF80 0000h to FFFF FFFFh, excluding reserved areas) • 4 GB in full-address mode (within 0000 0000h to FFFF FFFFh, excluding reserved areas)
Data transfer units	• Single data unit: 8 bits, 16 bits, or 32 bits • Single block size: 1 to 256 data units	• Single data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data units
CPU interrupt requests	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.
Event link function	An event link request is generated after one data transfer (for block transfers, after one block).	An event link request is generated after one data transfer (for block transfers, after one block).
Read skip	Transfer data read skip can be specified.	Reading of the transfer information can be skipped when the same transfer is repeated.
Write-back skip	Writeback skip can be enabled when “fixed” is selected for the transfer source address and/or transfer destination address.	Write-back of transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.
Write-back disable	—	Ability to disable write-back of transfer information
Displacement addition	—	Ability to add displacement to the transfer source address (selectable by each transfer information)
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Table 2.26 Comparison of Data Transfer Controller Registers

Register	Bit	RX210 (DTCa)	RX140 (DTCb)
MRA	WBDIS	—	Write-back disable bit*1
MRB	SQEND	—	Sequence transfer end bit
	INDX	—	Index table reference bit
	DISEL	DTC interrupt select bit 0: An interrupt request to the CPU is generated when the specified data transfer is completed. 1: An interrupt request to the CPU is generated each time DTC data transfer is performed.	DTC interrupt select bit 0: An interrupt request to the CPU is generated on completion of the specified number of data transfers. 1: An interrupt request to the CPU is generated for each data transfer.
	CHNS	DTC chain transfer select bit 0: Chain transfer is performed continuously. 1: Chain transfer is performed when the transfer counter changes from 1 to 0 or from 1 to CRAH.	DTC chain transfer select bit 0: Chain transfer is performed on completion of each transfer. 1: Chain transfer is performed when the transfer counter changes from 1 to 0 or from 1 to CRAH.
MRC	—	—	DTC mode register C
DTCIBR	—	—	DTC index table base register
DTCOR	—	—	DTC operation register
DTCSQE	—	—	DTC sequence transfer enable register
DTCDISP	—	—	DTC address displacement register

Note: 1. Transfer information is usually allocated to a RAM area, but it can be allocated to a ROM area by setting the MRA.WBDIS bit to 1 (no write-back).

2.15 Event Link Controller

Table 2.27 is a comparative overview of the event link controllers, Table 2.28 is a comparison of event link controller registers, Table 2.29 lists correspondences between values set in ELSRn.ELS[7:0] and event signal names and numbers.

Table 2.27 Comparative Overview of Event Link Controllers

Item	RX210 (ELC)	RX140 (ELC)
Event link function	• 59 types of event signals can be directly connected to peripheral modules. • The operation of peripheral timer modules at event input is selectable. • Event link operation is possible for port B and port E. — Single port: Event link operation can be enabled for a single specified port. — Port group: Event link operation can be enabled for a group of specified bits within an 8-bit port.	• 48 types of event signals can be directly connected to peripheral modules. • The operation of peripheral timer modules at event signal input is selectable. • Event link operation on port B is supported. — Single port: Event link operation can be enabled for a single specified port. — Port group: Event link operation can be enabled for multiple specified ports within a group of up to eight ports.
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Table 2.28 Comparison of Event Link Controller Registers

Register	Bit	RX210 (ELC)	RX140 (ELC)
ELSRn	—	Event link setting register n (n = 1 to 4, 7, 10, 12, 15, 16, 18 to 29)	Event link setting register n (n = 1 to 4, 7, 8, 10, 12, 14 to 16, 18, 20, 22, 24, 25)
ELOPC	LPTMD[1:0]	—	LPT operation select bits
PGRn (RX210) PGR1 (RX140)	—	Port group setting register n (n = 1, 2)	Port group setting register 1
PGCn (RX210) PGC1 (RX140)	—	Port group control register n (n = 1, 2)	Port group control register 1
PDBFn (RX210) PDBF1 (RX140)	—	Port buffer register n (n = 1, 2)	Port buffer register 1
PELm	—	Event link port setting register m (m = 0 to 3)	Event link port setting register m (m = 0, 1)
	PSP[1:0]	Port number specification bits b4 b3 0 0: Setting disabled. 0 1: Port B (corresponding to PGR1) 1 0: Port E (corresponding to PGR2) 1 1: Setting prohibited.	Port number specification bits b4 b3 0 0: Setting disabled. 0 1: Port B (corresponding to PGR1) 1 0: Setting prohibited. 1 1: Setting prohibited.

Table 2.29 Correspondences between Values Set in ELSRn.ELS[7:0] and Event Signal Names and Numbers

Value of ELS[7:0] Bits	Peripheral Module	RX210 (ELC)	RX140 (ELC)
08h	Multi-function timer pulse unit 2	MTU1 compare match 1A	MTU1 compare match 1A
09h		MTU1 compare match 1B	MTU1 compare match 1B
0Ah		MTU1 overflow	MTU1 overflow
0Bh		MTU1 underflow	MTU1 underflow
0Ch		MTU2 compare match 2A	MTU2 compare match 2A
0Dh		MTU2 compare match 2B	MTU2 compare match 2B
0Eh		MTU2 overflow	MTU2 overflow
0Fh		MTU2 underflow	MTU2 underflow
10h		MTU3 compare match 3A	MTU3 compare match 3A
11h		MTU3 compare match 3B	MTU3 compare match 3B
12h		MTU3 compare match 3C	MTU3 compare match 3C
13h		MTU3 compare match 3D	MTU3 compare match 3D
14h		MTU3 overflow	MTU3 overflow
15h		MTU4 compare match 4A	MTU4 compare match 4A
16h		MTU4 compare match 4B	MTU4 compare match 4B
17h		MTU4 compare match 4C	MTU4 compare match 4C
18h		MTU4 compare match 4D	MTU4 compare match 4D
19h		MTU4 overflow	MTU4 overflow
1Ah		MTU4 underflow	MTU4 underflow
1Fh	Compare match timer	CMT1 compare match 1	CMT1 compare match 1
22h	8-bit timer	TMR0 compare match A0	TMR0 compare match A0
23h		TMR0 compare match B0	TMR0 compare match B0
24h		TMR0 overflow	TMR0 overflow
28h		TMR2 compare match A2	TMR2 compare match A2
29h		TMR2 compare match B2	TMR2 compare match B2
2Ah		TMR2 overflow	TMR2 overflow
2Eh	—	RTC periodic	—
31h	—	IWDT underflow or refresh error	—
32h	Low-power timer	—	LPT compare match 0
33h		—	LPT compare match 1
34h	12-bit A/D converter	—	S12AD comparison conditions are met
35h		—	S12AD comparison conditions are not met
3Ah	Serial communications interface	SCI5 error (receive error or error signal detection)	SCI5 error (receive error or error signal detection)
3Bh		SCI5 receive data full	SCI5 receive data full
3Ch		SCI5 transmit data empty	SCI5 transmit data empty
3Dh		SCI5 transmit end	SCI5 transmit end
4Eh	I^2C bus interface	RIIC0 communication error or event generation	RIIC0 communication error or event generation
4Fh		RIIC0 receive data full	RIIC0 receive data full
50h		RIIC0 transmit data empty	RIIC0 transmit data empty
51h		RIIC0 transmit end	RIIC0 transmit end

Value of ELS[7:0] Bits	Peripheral Module	RX210 (ELC)	RX140 (ELC)
52h	Serial peripheral interface	RSPI0 error (mode fault, overrun, or parity error)	—
53h		RSPI0 idle	—
54h		RSPI0 receive data full	—
55h		RSPI0 transmit data empty	—
56h		RSPI0 transmit end (except during clock synchronous operation in slave mode)	—
58h	12-bit A/D converter	A/D conversion end signal of 12-bit A/D converter	S12AD A/D conversion end
59h	Comparator B0	Comparator B0 comparison result change	Comparator B0 comparison result change
5Ah	Comparator B0 and B1	Comparator B0/B1 common comparison result change	Comparator B0/B1 common comparison result change
5Bh	Voltage detection circuit	LVD1 voltage detection	LVD1 voltage detection
5Ch		LVD2 voltage detection	—
5Dh	DMA controller	DMAC0 transfer end	—
5Eh		DMAC1 transfer end	—
5Fh		DMAC2 transfer end	—
60h		DMAC3 transfer end	—
61h	Data transfer controller	DTC transfer end	DTC transfer end
62h	Clock generation circuit	Clock generation circuit oscillation stop detection	—
63h	I/O ports	Input port group 1 input edge detection	Input port group 1 input edge detection
64h		Input port group 2 input edge detection	—
65h		Single input port 0 input edge detection	Single input port 0 input edge detection
66h		Single input port 1 input edge detection	Single input port 1 input edge detection
67h		Single input port 2 input edge detection	—
68h		Single input port 3 input edge detection	—
69h	Event link controller	Software event	Software event
6Ah	Data operation circuit	—	DOC data operation condition met
Settings other than the above are prohibited.			

2.16 I/O Ports

Table 2.30 to Table 2.32 are comparative overviews of the I/O ports, Table 2.33 is a comparison of I/O port functions, and Table 2.34 is a comparison of I/O port registers.

Table 2.30 Comparative Overview of I/O Ports (80-Pin)

Port Symbol	RX210 (80-Pin)	RX140 (80-Pin)
PORT0	P03, P05, P07	P03 to P07
PORT1	P12 to P17	P12 to P17
PORT2	P20, P21, P26, P27	P20, P21, P26, P27
PORT3	P30 to P32, P34 to P37	P30 to P32, P34 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P54, P55	P54, P55
PORTA	PA0 to PA6	PA0 to PA6
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC2 to PC7	PC0 to PC7
PORTD	PD0 to PD2	PD0 to PD2
PORTE	PE0 to PE5	PE0 to PE5
PORTG	—	PG7
PORTH	PH0 to PH3	PH0 to PH3, PH6, PH7
PORTJ	PJ1	PJ1, PJ6, PJ7

Table 2.31 Comparative Overview of I/O Ports (64-Pin)

Port Symbol	RX210 (64- and 69-Pin)	RX140 (64-Pin)
PORT0	P03, P05	P03, P05
PORT1	P14 to P17	P14 to P17
PORT2	P26, P27	P26, P27
PORT3	P30 to P32, P35 to P37	P30 to P32, P35 to P37
PORT4	P40 to P44, P46	P40 to P47
PORT5	P54, P55	P54, P55
PORTA	PA0, PA1, PA3, PA4, PA6	PA0, PA1, PA3, PA4, PA6
PORTB	PB0, PB1, PB3, PB5 to PB7	PB0, PB1, PB3, PB5 to PB7
PORTC	PC2 to PC7	PC0 to PC7
PORTD	—	—
PORTE	PE0 to PE5	PE0 to PE5
PORTG	—	PG7
PORTH	PH0 to PH3	PH0 to PH3, PH6*1, PH7*1
PORTJ	—	PJ6, PJ7

Note: 1. A product with a ROM capacity of 64 KB is not equipped with this pin.

Table 2.32 Comparative Overview of I/O Ports (48-Pin)

Port Symbol	RX210 (48-Pin)	RX140 (48-Pin)
PORT0	—	—
PORT1	P14 to P17	P14 to P17
PORT2	P26, P27	P26, P27
PORT3	P30, P31, P35 to P37	P30, P31, P35 to P37
PORT4	P40 to P42, P46	P40 to P42, P45 to P47
PORTA	PA1, PA3, PA4, PA6	PA1, PA3, PA4, PA6
PORTB	PB0, PB1, PB3, PB5	PB0, PB1, PB3, PB5
PORTC	PC4 to PC7	PC0 to PC7
PORTE	PE1 to PE4	PE1 to PE4
PORTG	—	PG7
PORTH	PH0 to PH3	PH0 to PH3
PORTJ	—	PJ6, PJ7

Table 2.33 Comparison of I/O Port Functions

Item	Port Symbol	RX210	RX140
Input pull-up function	PORT0	P00 to P03, P05, P07	P03 to P07
	PORT1	P12 to P17	P12 to P17
	PORT2	P20 to P27	P20, P21, P26, P27
	PORT3	P30 to P34, P36, P37	P30 to P32, P34, P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P56	P54, P55
	PORT6	P60 to P67	—
	PORT7	P70 to P77	—
	PORT8	P80 to P83, P86, P87	—
	PORT9	P90 to P93	—
	PORTA	PA0 to PA7	PA0 to PA6
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC2 to PC7
	PORTD	PD0 to PD7	PD0 to PD2
	PORTE	PE0 to PE7	PE0 to PE5
	PORTF	PF5	—
	PORTG	—	PG7
	PORTH	PH0 to PH3	PH0 to PH3
	PORTJ	PJ1, PJ3, PJ5	PJ1, PJ6, PJ7
	PORTK	PK2 to PK5	—
	PORTL	PL0, PL1	—
Open drain output function	PORT0	P00 to P02	—
	PORT1	P12 to P17	P12 to P17
	PORT2	P20 to P27	P20, P21, P26, P27
	PORT3	P30 to P34, P36, P37	P30 to P32, P34, P36, P37
	PORT5	P50 to P52, P54	—
	PORT6	P60, P61	—
	PORT7	P70, P74 to P77	—
	PORT8	P80 to P83	—
	PORT9	P90 to P93	—
	PORTA	PA0 to PA7	PA0 to PA6
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC2 to PC7
	PORTD	—	PD0 to PD2

Item	Port Symbol	RX210	RX140
Open drain output function	PORTE	PE0 to PE7	PE0 to PE3
	PORTG	—	PG7
	PORTK	PK2 to PK5	—
Drive capacity switching function	PORT0	P00 to P03, P05, P07	—
	PORT1	P12 to P17	—
	PORT2	P20 to P27	—
	PORT3	P30 to P34, P36, P37	—
	PORT4	P40 to P47	—
	PORT5	P50 to P56	—
	PORT6	P60 to P67	—
	PORT7	P70, P71 to P77	—
	PORT8	P80 to P83, P86, P87	—
	PORT9	P90 to P93	—
	PORTA	PA0 to PA7	—
	PORTB	PB0 to PB7	—
	PORTC	PC0 to PC7	—
	PORTD	PD0 to PD7	—
	PORTE	PE0 to PE7	—
	PORTF	PF5	—
	PORTH	PH0 to PH3	—
	PORTJ	PJ1, PJ3, PJ5	—
	PORTK	PK2 to PK5	—
	PORTL	PL0, PL1	—
5 V tolerant	PORT1	P12, P13, P16, P17	P12, P13, P16, P17

Table 2.34 Comparison of I/O Port Registers

Register	Bit	RX210	RX140
PDR	B0 to B7	Pm0 to Pm7 I/O select bits (m = 0 to 9, A to F, H, J to L)	Pm0 to Pm7 I/O select bits (m = 0 to 5, A to E, G, H, J)
PODR	B0 to B7	Pm0 to Pm7 output data store bits (m = 0 to 9, A to F, H, J to L)	Pm0 to Pm7 output data store bits (m = 0 to 5, A to E, G, H, J)
PIDR	B0 to B7	Pm0 to Pm7 bits (m = 0 to 9, A to F, H, J to L)	Pm0 to Pm7 bits (m = 0 to 5, A to E, G, H, J)
PMR	B0 to B7	Pm0 pin mode control bits (m = 0 to 9, A to F, H, J to L) 0: Use pin as general I/O port. 1: Use pin as I/O port for peripheral function.	Pm0 to Pm7 pin mode control bits (m = 0 to 5, A to E, G, H, J) 0: Use pin as general I/O port. 1: Use pin as I/O port for peripheral function. PG7 only 0: Use pin as general I/O port. 1: Use pin as I/O port for MD function (initial value).

Register	Bit	RX210	RX140
ODR0	B2, B3	Pm1 output type select bits (m = 0 to 3, 6 to 9, A to C, E, K) • P01, P21, P31, P51, P61, P81, P91, PA1, PB1, and PC1 b2 0: CMOS output 1: N-channel open-drain b3 This bit is read as 0. The write value should be 0. • PE1 b3 b2 0 0: CMOS output 0 1: N-channel open-drain 1 0: P-channel open-drain 1 1: Hi-Z	Pm1 output type select bits (m = 1 to 3, A to E, J) • P21, P31, PA1, PB1, and PD1 b2 0: CMOS output 1: N-channel open-drain b3 This bit is read as 0. The write value should be 0. • PE1 b3 b2 0 0: CMOS output 0 1: N-channel open-drain 1 0: P-channel open-drain 1 1: Hi-Z
ODR1	B0, B2, B4, B6	Pm4, Pm5, Pm6, and Pm7 output type select bits (m = 1 to 3, 5, 7, A to C, E, K)	Pm4, Pm5, Pm6, and Pm7 output type select bits (m =1 to 3, A to C, G)
PCR	B0 to B7	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A to F, H, J to L)	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 5, A to E, G, H, J)
DSCR	—	Drive capacity control register	—
PSRA	—	—	Port switching register A
PSRB	—	—	Port switching register B
PRWCNTR	—	—	Port read wait control register

2.17 Multi-Function Pin Controller

Table 2.35 is a comparison of the assignments of multiplexed pins, and Table 2.36 to Table 2.54 are comparisons of multi-function pin controller registers.

In the following comparison of the assignments of multiplexed pins, **blue text** designates pins that exist on the RX140 Group only and **orange text** pins that exist on the RX210 Group only. A circle (○) indicates that a function is assigned, a cross (×) that the pin does not exist or that no function is assigned, and grayed out items mean that the function is not implemented.

Table 2.35 Comparison of Multiplexed Pin Assignments

Module/ Function	Pin Function	Port Allocation	RX210			RX140		
			80-Pin	64-Pin	48-Pin	80-Pin	64-Pin	48-Pin
Interrupt	NMI (input)	P35	○	○	○	○	○	○
	IRQ0-DS (input)	P30	○	○	○			
	IRQ0 (input)	P30	×	×	×	○	○	○
		PD0	○	×	×	○	×	×
		PH1	○	○	○	○	○	○
	IRQ1-DS (input)	P31	○	○	○			
	IRQ1 (input)	P31	×	×	×	○	○	○
		PD1	○	×	×	○	×	×
		PH2	○	○	○	○	○	○
	IRQ2-DS (input)	P32	○	○	×			
	IRQ2 (input)	P12	○	×	×	○	×	×
		P32	×	×	×	○	○	×
		P36	×	×	×	○	○	○
		PD2	○	×	×	○	×	×
	IRQ3 (input)	P13	○	×	×	○	×	×
	IRQ4-DS (input)	PB1	○	○	○			
	IRQ4 (input)	P14	○	○	○	○	○	○
		P34	○	×	×	○	×	×
		P37	×	×	×	○	○	○
		PB1	×	×	×	○	○	○
	IRQ5-DS (input)	PA4	○	○	○			
	IRQ5 (input)	P15	○	○	○	○	○	○
		PA4	×	×	×	○	○	○
		PE5	○	○	×	○	○	×
	IRQ6-DS (input)	PA3	○	○	○			
	IRQ6 (input)	P16	○	○	○	○	○	○
		PA3	×	×	×	○	○	○
	IRQ7-DS (input)	PE2	○	○	○			
	IRQ7 (input)	P17	○	○	○	○	○	○
		PE2	×	×	×	○	○	○
Multi-function timer unit 2	MTIOC0A (input/output)	P34	○	×	×	○	×	×
		PB3	○	○	○	○	○	○
		PC4	×	×	×	○	○	○
	MTIOC0B (input/output)	P13	○	×	×	○	×	×
		P15	○	○	○	○	○	○
		PA1	○	○	○	○	○	○
	MTIOC0C (input/output)	P32	○	○	×	○	○	×
		PB1	○	○	○	○	○	○
		PC5	×	×	×	○	○	○

Module/ Function	Pin Function	Port Allocation	RX210			RX140		
			80-Pin	64-Pin	48-Pin	80-Pin	64-Pin	48-Pin
Multi-function timer unit 2	MTIOC0D (input/output)	PA3	○	○	○	○	○	○
	MTIOC1A (input/output)	P20	○	×	×	○	×	×
		PE4	○	○	○	○	○	○
	MTIOC1B (input/output)	P21	○	×	×	○	×	×
		PB5	○	○	○	○	○	○
		PE3	×	×	×	○	○	○
	MTIOC2A (input/output)	P26	○	○	○	○	○	○
		PB5	○	○	○	○	○	○
	MTIOC2B (input/output)	P27	○	○	○	○	○	○
		PE5	○	○	×	○	○	×
	MTIOC3A (input/output)	P14	○	○	○	○	○	○
		P17	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
		PJ1	○	×	×	○	×	×
	MTIOC3B (input/output)	P17	○	○	○	○	○	○
		PA1	×	×	×	○	○	○
		PB7	○	○	×	○	○	×
		PC5	○	○	○	○	○	○
		PH0	×	×	×	○	○	○
	MTIOC3C (input/output)	P16	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	MTIOC3D (input/output)	P16	○	○	○	○	○	○
		PA6	×	×	×	○	○	○
		PB0	×	×	×	○	○	○
		PB6	○	○	×	○	○	×
		PC4	○	○	○	○	○	○
		PH1	×	×	×	○	○	○
	MTIOC4A (input/output)	P55	×	×	×	○	○	×
		PA0	○	○	×	○	○	×
		PB3	○	○	○	○	○	○
		PE2	○	○	○	○	○	○
		PE4	×	×	×	○	○	○
	MTIOC4B (input/output)	P30	○	○	○	○	○	○
		P54	○	○	×	○	○	×
		PC2	○	○	×	○	○	×
		PD1	○	×	×	○	×	×
		PE3	○	○	○	○	○	○
	MTIOC4C (input/output)	PA4	×	×	×	○	○	○
		PB1	○	○	○	○	○	○
		PE1	○	○	○	○	○	○
		PE5	○	○	×	○	○	×
		PH2	×	×	×	○	○	○
	MTIOC4D (input/output)	P31	○	○	○	○	○	○
		P55	○	○	×	○	○	×
		PA3	×	×	×	○	○	○
		PC3	○	○	×	○	○	×
		PD2	○	×	×	○	×	×
		PE4	○	○	○	○	○	○
		PH3	×	×	×	○	○	○

Module/ Function	Pin Function	Port Allocation	RX210			RX140		
			80-Pin	64-Pin	48-Pin	80-Pin	64-Pin	48-Pin
Multi-function timer unit 2	MTIC5U (input)	PA4	○	○	○	○	○	○
	MTIC5V (input)	PA6	○	○	○	○	○	○
	MTIC5V (input)	PA3	×	×	×	○	○	○
	MTIC5W (input)	PB0	○	○	○	○	○	○
	MTCLKA (input)	P14	○	○	○	○	○	○
		PA4	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	MTCLKB (input)	P15	○	○	○	○	○	○
		PA6	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	MTCLKC (input)	PA1	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	MTCLKD (input)	PA3	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
Port output enable 2	POE0# (input)	PC4	○	○	○	○	○	○
	POE1# (input)	PB5	○	○	○	○	○	○
	POE2# (input)	P34	○	×	×	○	×	×
		PA6	○	○	○	○	○	○
	POE3# (input)	PB3	○	○	○	○	○	○
	POE8# (input)	P17	○	○	○	○	○	○
		P30	○	○	○	○	○	○
		PE3	○	○	○	○	○	○
8-bit timer	TMO0 (output)	PB3	○	○	○	○	○	○
		PH1	○	○	○	○	○	○
	TMCI0 (input)	P21	○	×	×	○	×	×
		PB1	○	○	○	○	○	○
		PH3	○	○	○	○	○	○
	TMRI0 (input)	P20	○	×	×	○	×	×
		PA4	○	○	○	○	○	○
		PH2	○	○	○	○	○	○
	TMO1 (output)	P17	○	○	○	○	○	○
		P26	○	○	○	○	○	○
	TMCI1 (input)	P12	○	×	×	○	×	×
		P54	○	○	×	○	○	×
		PC4	○	○	○	○	○	○
	TMRI1 (input)	PB5	○	○	○	○	○	○
	TMO2 (output)	P16	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	TMCI2 (input)	P15	○	○	○	○	○	○
		P31	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	TMRI2 (input)	P14	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
	TMO3 (output)	P13	○	×	×	○	×	×
		P32	○	○	×	○	○	×
		P55	○	○	×	○	○	×
	TMCI3 (input)	P27	○	○	○	○	○	○
		P34	○	×	×	○	×	×
		PA6	○	○	○	○	○	○
	TMRI3 (input)	P30	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX210			RX140		
			80-Pin	64-Pin	48-Pin	80-Pin	64-Pin	48-Pin
Serial communications interface	RXD0 (input) / SMISO0 (input/output) / SSCL0 (input/output)	P21	○*2	×	×			
	TXD0 (output) / SMOSI0 (input/output) / SSDA0 (input/output)	P20	○*1	×	×			
	RXD1 (input) / SMISO1 (input/output) / SSCL1 (input/output)	P15	○	○	○	○	○	○
		P30	○	○	○	○	○	○
	TXD1 (output) / SMOSI1 (input/output) / SSDA1 (input/output)	P16	○	○	○	○	○	○
		P26	○	○	○	○	○	○
	SCK1 (input/output)	P17	○	○	○	○	○	○
		P27	○	○	○	○	○	○
	CTS1# (input) / RTS1# (output) / SS1# (input)	P14	○	○	○	○	○	○
		P31	○	○	○	○	○	○
	RXD5 (input) / SMISO5 (input/output) / SSCL5 (input/output)	PA2	○	×	×	○	×	×
		PA3	○	○	○	○	○	○
		PC2	○	○	×	○	○	×
	TXD5 (output) / SMOSI5 (input/output) / SSDA5 (input/output)	PA4	○	○	○	○	○	○
		PC3	○	○	×	○	○	×
	SCK5 (input/output)	PA1	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	CTS5# (input) / RTS5# (output) / SS5# (input)	PA6	○	○	○	○	○	○
	RXD6 (input) / SMISO6 (input/output) / SSCL6 (input/output)	PB0	○	○	○	○	○	○
		PD1	×	×	×	○	×	×
	TXD6 (output) / SMOSI6 (input/output) / SSDA6 (input/output)	P32	○	○	×	○	○	×
		PB1	○	○	○	○	○	○
		PD0	×	×	×	○	×	×
	SCK6 (input/output)	P34	○	×	×	○	×	×
		PB3	○	○	○	○	○	○
		PD2	×	×	×	○	×	×

Module/ Function	Pin Function	Port Allocation	RX210			RX140		
			80-Pin	64-Pin	48-Pin	80-Pin	64-Pin	48-Pin
Serial communications interface	CTS6# (input) / RTS6# (output) / SS6# (input)	PB2	○	×	×	○	×	×
	RXD8 (input) / SMISO8 (input/output) / SSCL8 (input/output)	PC6	○	○	○	○	○	○
	TXD8 (output) / SMOSI8 (input/output) / SSDA8 (input/output)	PC7	○	○	○	○	○	○
	SCK8 (input/output)	PC5	○	○	○	○	○	○
	CTS8# (input) / RTS8# (output) / SS8# (input)	PC4	○	○	○	○	○	○
	RXD9 (input) / SMISO9 (input/output) / SSCL9 (input/output)	PB6	○	○	×	○	○	×
	TXD9 (output) / SMOSI9 (input/output) / SSDA9 (input/output)	PB7	○	○	×	○	○	×
	SCK9 (input/output)	PB5	○	○	×	○	○	×
	CTS9# (input) / RTS9# (output) / SS9# (input)	PB4	○	×	×	○	○	×
	RXD12 (input) / SMISO12 (input/output) / SSCL12 (input/output) / RXDX12 (input)	PE2	○	○	○ *3	○	○	○ *3
	TXD12 (output) / SMOSI12 (input/output) / SSDA12 (input/output) / TXDX12 (output) / SIOX12 (input/output)	PE1	○	○	○ *4	○	○	× *4
	SCK12 (input/output)	PE0	○	○	×	○	○	×
	CTS12# (input) / RTS12# (output) / SS12# (input)	PE3	○	○	○ *5	○	○	○ *5

Module/ Function	Pin Function	Port Allocation	RX210 80-Pin	RX210 64-Pin	RX210 48-Pin	RX140 80-Pin	RX140 64-Pin	RX140 48-Pin
I^2C bus interface	SCL-DS (input/output)	P16	○	○	○			
	SCL (input/output)	P12	○	×	×			
	SDA-DS (input/output)	P17	○	○	○			
	SDA (input/output)	P13	○	×	×			
	SCL0 (input/output)	P12				○	×	×
		P16				○	○	○
	SDA0 (input/output)	P13				○	×	×
		P17				○	○	○
Serial peripheral interface	RSPCKA (input/output)	PA5	○	×	×	○	×	×
		PB0	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
	MOSIA (input/output)	P16	○	○	○	○	○	○
		PA6	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	MISOA (input/output)	P17	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	SSLA0 (input/output)	PA4	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	SSLA1 (output)	PA0	○	○	×	○	○	×
	SSLA2 (output)	PA1	○	○	○	○	○	○
	SSLA3 (output)	PA2	○	×	×	○	×	×
		PC2	○	○	×	○	○	×
Realtime clock	RTCOUT (output)	P16	○	○	×	○	○	○
		P32	○	○	×	○	○	×
	RTCIC0 (input)*6	P30	○	○	×			
	RTCIC1 (input)*6	P31	○	○	×			
	RTCIC2 (input)*6	P32	○	○	×			
12-bit A/D converter	AN000 (input)*6	P40	○	○	○	○	○	○
	AN001 (input)*6	P41	○	○	○	○	○	○
	AN002 (input)*6	P42	○	○	○	○	○	○
	AN003 (input)*6	P43	○	○	×	○	○	×
	AN004 (input)*6	P44	○	○	×	○	○	×
	AN005 (input)*6	P45	○	×	×	○	○	○
	AN006 (input)*6	P46	○	○	○	○	○	○
	AN007 (input)*6	P47	○	×	×	○	○	○
	AN008 (input)*6	PE0	○	○	×			
	AN009 (input)*6	PE1	○	○	○			
	AN010 (input)*6	PE2	○	○	○			
	AN011 (input)*6	PE3	○	○	○			
	AN012 (input)*6	PE4	○	○	○			
	AN013 (input)*6	PE5	○	○	×			
	AN016 (input)	PE0				○	○	×
	AN017 (input)	PE1				○	○	○
	AN018 (input)	PE2				○	○	○
	AN019 (input)	PE3				○	○	○
	AN020 (input)	PE4				○	○	○

Module/ Function	Pin Function	Port Allocation	RX210			RX140		
			80-Pin	64-Pin	48-Pin	80-Pin	64-Pin	48-Pin
12-bit A/D converter	AN021 (input)	PE5				○	○	×
	AN024 (input)	PD0				○	×	×
	AN025 (input)	PD1				○	×	×
	AN026 (input)	PD2				○	×	×
	ADTRG0# (input)	P07	○	×	×	○	×	×
		P16	○	○	○	○	○	○
D/A converter	DA0 (output)*6	P03	○	○	×	○	○	×
	DA1 (output)*6	P05	○	○	×	○	○	×
Clock frequency accuracy measurement circuit	CACREF (input)	PA0	○	○	×	○	○	×
		PC7	○	○	○	○	○	○
		PH0	○	○	○	○	○	○
Clock generation circuit	CLKOUT (output)	PE3				○	○	○
		PE4				○	○	○
Comparator A	CMPA1 (input)*6	PE3	○	○	○			
	CMPA2 (input)*6	PE4	○	○	○			
	CVREFA (input)*6	PA1	○	○	○			
	CMPB0 (input)*6	PE1	○	○	○	○	○	○
	CVREFB0 (input)*6	PE2	○	○	○	○	○	○
	CMPOB0 (output)	PE5				○	○	×
	CMPB1 (input)*6	PA3	○	○	○	○	○	○
	CVREFB1 (input)*6	PA4				○	○	○
	CMPOB1 (output)	PB1				○	○	○
Low-power timer	LPTO (output)	P26				○	○	○
		PB3				○	○	○
		PC7				○	○	○
CAN module	CTXD0 (output)	P14				○	○	○
		P54				○	○	×
	CRXD0 (input)	P15				○	○	○
		P55				○	○	×
LVD voltage detection input	CMPA2 (input)	PE4				○	○	○
CTSU	TS0 (input/output)	P32				○	○	×
	TS1 (input/output)	P31				○	○	○
	TS2 (input/output)	P30				○	○	○
	TS3 (input/output)	P27				○	○	○
	TS4 (input/output)	P26				○	○	○
	TS5 (input/output)	P15				○	○	○
	TS6 (input/output)	P14				○	○	○
	TS7 (input/output)	PH3				○	○	○

Module/ Function	Pin Function	Port Allocation	RX210 80-Pin	RX210 64-Pin	RX210 48-Pin	RX140 80-Pin	RX140 64-Pin	RX140 48-Pin
CTSU	TS8 (input/output)	PH2				○	○	○
	TS9 (input/output)	PH1				○	○	○
	TS10 (input/output)	PH0				○	○	○
	TS11 (input/output)	P55				○	○	×
	TS12 (input/output)	P54				○	○	×
	TS13 (input/output)	PC7				○	○	○
	TS14 (input/output)	PC6				○	○	○
	TS15 (input/output)	PC5				○	○	○
	TS16 (input/output)	PC3				○	○	×
	TS17 (input/output)	PC2				○	○	×
	TS18 (input/output)	PB7				○	○	×
	TS19 (input/output)	PB6				○	○	×
	TS20 (input/output)	PB5				○	○	○
	TS21 (input/output)	PB4				○	×	×
	TS22 (input/output)	PB3				○	○	○
	TS23 (input/output)	PB2				○	×	×
	TS24 (input/output)	PB1				○	○	○
	TS25 (input/output)	PB0				○	○	○
	TS26 (input/output)	PA6				○	○	○
	TS27 (input/output)	PA5				○	×	×
	TS28 (input/output)	PA4				○	○	○
	TS29 (input/output)	PA3				○	○	○
	TS30 (input/output)	PA2				○	×	×
	TS31 (input/output)	PA1				○	○	○
	TS32 (input/output)	PA0				○	○	×
	TS33 (input/output)	PE4				○	○	○

Module/ Function	Pin Function	Port Allocation	RX210			RX140		
			80-Pin	64-Pin	48-Pin	80-Pin	64-Pin	48-Pin
CTSU	TS34 (input/output)	PE3				○	○	○
	TS35 (input/output)	PE2				○	○	○
	TSCAP (—)	PC4				○	○	○

Notes: 1. SMOSI0 function not implemented.
2. SMISO0 function not implemented.
3. SMISO12 function not implemented.
4. SMOSI12 function not implemented.
5. SS12# function not implemented.
6. Select general input for the relevant pin if this pin function is to be used.

Table 2.36 Comparison of P0n Pin Function Control Register (P0nPFS)

Register	Bit	RX210 (n = 0 to 3, 5, 7)	RX140 (n = 3, 5, 7)
P00PFS	—	P00 pin function control register	—
P01PFS	—	P01 pin function control register	—
P02PFS	—	P02 pin function control register	—

Table 2.37 Comparison of P1n Pin Function Control Register (P1nPFS)

Register	Bit	RX210 (n = 2 to 7)	RX140 (n = 2 to 7)
P12PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0101b: TMCL1 1010b: RXD2/SMISO2/SSCL2 1111b: SCL	Pin function select bits 00000b: Hi-Z 00101b: TMCL1 01111b: SCL
P13PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC0B 0011b: TIOCA5 0101b: TMO3 1010b: TXD2/SMOSI2/SSDA2 1111b: SDA	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0B 00101b: TMO3 01111b: SDA
P14PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC3A 0010b: MTCLKA 0011b: TIOCB5 0100b: TCLKA 0101b: TMRI2 1011b: CTS1#/RTS1#/SS1#	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKA 00101b: TMRI2 01011b: CTS1#/RTS1#/SS1# 10000b: CTXD0 11001b: TS6
P15PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC0B 0010b: MTCLKB 0011b: TIOCB2 0100b: TCLKB 0101b: TMCI2 1010b: RXD1/SMISO1/SSCL1 1011b: SCK3	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKB 00101b: TMCI2 01010b: RXD1/SMISO1/SSCL1 10000b: CRXD0 11001b: TS5

Register	Bit	RX210 (n = 2 to 7)	RX140 (n = 2 to 7)
P16PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC3C 0010b: MTIOC3D 0011b: TIOCB1 0100b: TCLKC 0101b: TMO2 0111b: RTCOUT 1001b: ADTRG0# 1010b: TXD1/SMOSI1/SSDA1 1011b: RXD3/SMISO3/SSCL3 1101b: MOSIA 1111b: SCL-DS	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTIOC3D 00101b: TMO2 00111b: RTCOUT 01001b: ADTRG0# 01010b: TXD1/SMOSI1/SSDA1 01101b: MOSIA 01111b: SCL
P17PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC3A 0010b: MTIOC3B 0011b: TIOCB0 0100b: TCLKD 0101b: TMO1 0111b: POE8# 1010b: SCK1 1011b: TXD3/SMOSI3/SSDA3 1101b: MISOA 1111b: SDA-DS	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTIOC3B 00101b: TMO1 00111b: POE8# 01010b: SCK1 01101b: MISOA 01111b: SDA

Table 2.38 Comparison of P2n Pin Function Control Register (P2nPFS)

Register	Bit	RX210 (n = 0 to 7)	RX140 (n = 0, 1, 6, 7)
P20PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC1A 0011b: TIOCB3 0101b: TMRI0 1010b: TXD0/SMOSI0/SSDA0	Pin function select bits 00000b: Hi-Z 00001b: MTIOC1A 00101b: TMRI0
P21PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC1B 0011b: TIOCA3 0101b: TMCI0 1010b: RXD0/SMISO0/SSCL0	Pin function select bits 00000b: Hi-Z 00001b: MTIOC1B 00101b: TMCI0
P22PFS	—	P22 pin function control register	—
P23PFS	—	P23 pin function control register	—
P24PFS	—	P24 pin function control register	—
P25PFS	—	P25 pin function control register	—

Register	Bit	RX210 (n = 0 to 7)	RX140 (n = 0, 1, 6, 7)
P26PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC2A 0101b: TMO1 1010b: TXD1/SMOSI1/SSDA1 1011b: CTS3#/RTS3#/SS3#	Pin function select bits 00000b: Hi-Z 00001b: MTIOC2A 00101b: TMO1 01010b: TXD1/SMOSI1/SSDA1 11001b: TS4 11011b: LPTO
P27PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC2A 0101b: TMO1 1010b: SCK1	Pin function select bits 00000b: Hi-Z 00001b: MTIOC2B 00101b: TMCI3 01010b: SCK1 11001b: TS3

Table 2.39 Comparison of P3n Pin Function Control Register (P3nPFS)

Register	Bit	RX210 (n = 0 to 4)	RX140 (n = 0 to 2, 4, 6, 7)
P30PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC4B 0101b: TMRI3 0111b: POE8# 1010b: RXD1/SMISO1/SSCL1	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 00101b: TMRI3 00111b: POE8# 01010b: RXD1/SMISO1/SSCL1 11001b: TS2
P31PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC4D 0101b: TMCI2 1011b: CTS1#/RTS1#/SS1#	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 00101b: TMCI2 01010b: RXD1/SMISO1/SSCL1 11001b: TS1
P32PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC0C 0011b: TIOCC0 0101b: TMO3 1010b: TXD0/SMOSI0/SSDA0 1011b: TXD6/SMOSI6/SSDA6	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0C 00101b: TMO3 00111b: RTCOUT 01011b: TXD6/SMOSI6/SSDA6 11001b: TS0
P33PFS	—	P33 pin function control register	—

Register	Bit	RX210 (n = 0 to 4)	RX140 (n = 0 to 2, 4, 6, 7)
P34PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC0A 0101b: TMCI3 0111b: POE2# 1010b: SCK0 1011b: SCK6	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0A 00101b: TMCI2 00111b: POE2# 01011b: SCK6
P3nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0-DS (145/144/100/80/69/64/48-pin) P31: IRQ1-DS (145/144/100/80/69/64/48-pin) P32: IRQ2-DS (145/144/100/80/69/64-pin) P33: IRQ3-DS (145/144/100-pin) P34: IRQ4 (145/144/100/80-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0 (80/64/48/32-pin) P31: IRQ1 (80/64/48/32-pin) P32: IRQ2 (80/64-pin) P34: IRQ4 (80-pin) P36: IRQ2 (80/64/48/32-pin) P37: IRQ4 (80/64/48-pin)

Table 2.40 Comparison of P5n Pin Function Control Register (P5nPFS)

Register	Bit	RX210 (n = 0 to 2, 4 to 6)	RX140 (n = 4, 5)
P50PFS	—	P50 pin function control register	—
P51PFS	—	P51 pin function control register	—
P52PFS	—	P52 pin function control register	—
P53PFS	—	P53 pin function control register	—
P54PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC4B 0101b: TMCI1 1011b: CTS2#/RTS2#/SS2#	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 00101b: TMCI1 10000b: CTXD0 11001b: TS12
P55PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0101b: TMO3	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 00101b: TMO3 10000b: CRXD0 11001b: TS11

Table 2.41 Comparison of P6n Pin Function Control Register (P6nPFS)

Register	Bit	RX210 (n = 0, 1)	RX140
P6nPFS	—	P6n pin function control register	—

Table 2.42 Comparison of P7n Pin Function Control Register (P7nPFS)

Register	Bit	RX210 (n = 0, 4 to 7)	RX140
P7nPFS	—	P7n pin function control register	—

Table 2.43 Comparison of P8n Pin Function Control Register (P8nPFS)

Register	Bit	RX210 (n = 0 to 3, 6, 7)	RX140
P8nPFS	—	P8n pin function control register	—

Table 2.44 Comparison of P9n Pin Function Control Register (P9nPFS)

Register	Bit	RX210 (n = 0 to 3)	RX140
P9nPFS	—	P9n pin function control register	—

Table 2.45 Comparison of PAn Pin Function Control Register (PAnPFS)

Register	Bit	RX210 (n = 0 to 7)	RX140 (n = 0 to 6)
PA0PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC4A 0011b: TIOCA0 0111b: CACREF 1101b: SSLA1	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4A 00111b: CACREF 01101b: SSLA1 11001b: TS32
PA1PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC0B 0010b: MTCLKC 0011b: TIOCB0 1010b: SCK5 1101b: SSLA2	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKC 00011b: MTIOC3B 01010b: SCK5 01101b: SSLA2 11001b: TS31
PA2PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 1010b: RXD5/SMISO5/SSCL5 1101b: SSLA3	Pin function select bits 00000b: Hi-Z 01010b: RXD5/SMISO5/SSCL5 01101b: SSLA3 11001b: TS30
PA3PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC0D 0010b: MTCLKD 0011b: TIOCD0 0100b: TCLKB 1010b: RXD5/SMISO5/SSCL5	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0D 00010b: MTCLKD 00011b: MTIOC4D 00100b: MTIC5V 01010b: RXD5/SMISO5/SSCL5 11001b: TS29

Register	Bit	RX210 (n = 0 to 7)	RX140 (n = 0 to 6)
PA4PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIC5U 0010b: MTCLKA 0011b: TIOCA1 0101b: TMRI0 1010b: TXD5/SMOSI5/SSDA5 1101b: SSLA0	Pin function select bits 00000b: Hi-Z 00001b: MTIC5U 00010b: MTCLKA 00011b: MTIOC4C 00101b: TMRI0 01010b: TXD5/SMOSI5/SSDA5 01101b: SSLA0 11001b: TS28
PA5PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0011b: TIOCB1 1101b: RSPCKA	Pin function select bits 00000b: Hi-Z 01101b: RSPCKA 11001b: TS27
PA6PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIC5V 0010b: MTCLKB 0011b: TIOCA2 0101b: TMCI3 0111b: POE2# 1011b: CTS5#/RTS5#/SS5# 1101b: MOSIA	Pin function select bits 00000b: Hi-Z 00001b: MTIC5V 00010b: MTCLKB 00011b: MTIOC3D 00101b: TMCI3 00111b: POE2# 01011b: CTS5#/RTS5#/SS5# 01101b: MOSIA 11001b: TS26
PA7PFS	—	PA7 pin function control register	—

Table 2.46 Comparison of PBn Pin Function Control Register (PBnPFS)

Register	Bit	RX210 (n = 0 to 7)	RX140 (n = 0 to 7)
PB0PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIC5W 0011b: TIOCA3 1010b: RXD4/SMISO4/SSCL4 1011b: RXD6/SMISO6/SSCL6 1101b: RSPCKA	Pin function select bits 00000b: Hi-Z 00001b: MTIC5W 00010b: MTIOC3D 01011b: RXD6/SMISO6/SSCL6 01101b: RSPCKA 11001b: TS25
PB1PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC0C 0010b: MTIOC4C 0011b: TIOCB3 0101b: TMCI0 1010b: TXD4/SMOSI4/SSDA4 1011b: TXD6/SMOSI6/SSDA6	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0C 00010b: MTIOC4C 00101b: TMCI0 01011b: TXD6/SMOSI6/SSDA6 10000b: CMPOB1 11001b: TS24

Register	Bit	RX210 (n = 0 to 7)	RX140 (n = 0 to 7)
PB2PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0011b: TIOCC3 0100b: TCLKC 1011b: CTS4#/RTS4#/SS4# 1011b: CTS6#/RTS6#/SS6#	Pin function select bits 00000b: Hi-Z 01011b: CTS6#/RTS6#/SS6# 11001b: TS23
PB3PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC0A 0010b: MTIOC4A 0011b: TIOCD3 0100b: TCLKD 0101b: TMO0 0111b: POE3# 1010b: SCK4 1011b: SCK6	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0A 00010b: MTIOC4A 00101b: TMO0 00111b: POE3# 01011b: SCK6 11001b: TS22 11011b: LPTO
PB4PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0011b: TIOCA4 1011b: CTS9#/RTS9#/SS9#	Pin function select bits 00000b: Hi-Z 01011b: CTS9#/RTS9#/SS9# 11001b: TS21
PB5PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC2A 0010b: MTIOC1B 0011b: TIOCB4 0101b: TMRI1 0111b: POE1# 1010b: SCK9	Pin function select bits 00000b: Hi-Z 00001b: MTIOC2A 00010b: MTIOC1B 00101b: TMRI1 00111b: POE1# 01010b: SCK9 11011b: TS20
PB6PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC3D 0011b: TIOCA5 1010b: RXD9/SMISO9/SSCL9	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3D 01010b: RXD9/SMISO9/SSCL9 11001b: TS19
PB7PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC3B 0011b: TIOCB5 1010b: TXD9/SMOSI9/SSDA9	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3B 01010b: TXD9/SMOSI9/SSDA9 11001b: TS18

Table 2.47 Comparison of PCn Pin Function Control Register (PCnPFS)

Register	Bit	RX210 (n = 0 to 7)	RX140 (n = 2 to 7)
PC0PFS	—	PC0 pin function select register	—
PC1PFS	—	PC1 pin function select register	—
PC2PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC4B 0011b: TCLKA 1010b: RXD5/SMISO5/SSCL5 1101b: SSLA3	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 01010b: RXD5/SMISO5/SSCL5 01101b: SSLA3 11001b: TS17
PC3PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC4D 0011b: TCLKB 1010b: TXD5/SMOSI5/SSDA5	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 01010b: TXD5/SMOSI5/SSDA5 11001b: TS16
PC4PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC3D 0010b: MTCLKC 0101b: TMCI1 0111b: POE0# 1010b: SCK5 1011b: CTS8#/RTS8#/SS8# 1101b: SSLA0	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3D 00010b: MTCLKC 00011b: MTIOC0A 00101b: TMCI1 00111b: POE0# 01010b: SCK5 01011b: CTS8#/RTS8#/SS8# 01101b: SSLA0 11001b: TSCAP
PC5PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC3B 0010b: MTCLKD 0101b: TMRI2 1010b: SCK8 1101b: RSPCKA	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3B 00010b: MTCLKD 00011b: MTIOC0C 00101b: TMRI2 01010b: SCK8 01101b: RSPCKA 11001b: TS15
PC6PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC3C 0010b: MTCLKA 0101b: TMCI2 1010b: RXD8/SMISO8/SSCL8 1101b: MOSIA	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTCLKA 00101b: TMCI2 01010b: RXD8/SMISO8/SSCL8 01101b: MOSIA 11001b: TS14

Register	Bit	RX210 (n = 0 to 7)	RX140 (n = 2 to 7)
PC7PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC3A 0010b: MTCLKB 0101b: TMO2 0111b: CACREF 1010b: TXD8/SMOSI8/SSDA8 1101b: MISOA	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKB 00101b: TMO2 00111b: CACREF 01010b: TXD8/SMOSI8/SSDA8 01101b: MISOA 11001b: TS13 11011b: LPTO

Table 2.48 Comparison of PDn Pin Function Control Register (PDnPFS)

Register	Bit	RX210 (n = 0 to 7)	RX140 (n = 0 to 2)
PD0PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	—	PD0 pin function select register
PD1PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC4B	Pin function select bits 00000b: Hi-Z 01011b: TXD6/SMOSI6/SSDA6
PD2PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 01011b: SCK6
PD3PFS	—	PD3 pin function select register	—
PD4PFS	—	PD4 pin function select register	—
PD5PFS	—	PD5 pin function select register	—
PD6PFS	—	PD6 pin function select register	—
PD7PFS	—	PD7 pin function select register	—
PDnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PD0: IRQ0 (145/144/100/80-pin) PD1: IRQ1 (145/144/100/80-pin) PD2: IRQ2 (145/144/100/80-pin) PD3: IRQ3 (145/144/100-pin) PD4: IRQ4 (145/144/100-pin) PD5: IRQ5 (145/144/100-pin) PD6: IRQ6 (145/144/100-pin) PD7: IRQ7 (145/144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PD0: IRQ0 (80-pin) PD1: IRQ1 (80-pin) PD2: IRQ2 (80-pin)
PDnPFS	ASEL	—	Analog function select bit

Table 2.49 Comparison of PEn Pin Function Control Register (PEnPFS)

Register	Bit	RX210 (n = 0 to 7)	RX140 (n = 0 to 5)
PE3PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC4B 0111b: POE8# 1100b: CTS12#/RTS12#/SS12#	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 00010b: MTIOC1B 00111b: POE8# 01001b: CLKOUT 01100b: CTS12#/RTS12#/SS12# 11001b: TS34
PE4PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC4D 0010b: MTIOC1A	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 00010b: MTIOC1A 00011b: MTIOC4A 01001b: CLKOUT 11001b: TS33
PE5PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0001b: MTIOC4C 0010b: MTIOC2B	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4C 00010b: MTIOC2B 10000b: CMPOB0
PE6PFS	—	PE6 pin function control register	—
PEnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE2: IRQ7-DS (145/144/100/80/69/64/48-pin) PE5: IRQ5 (145/144/100/80/69/64-pin) PE6: IRQ6 (145/144/100-pin) PE7: IRQ7 (145/144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE2: IRQ7 (80/64/48/32-pin) PE5: IRQ5 (80/64-pin)

Register	Bit	RX210 (n = 0 to 7)	RX140 (n = 0 to 5)
PEnPFS	ASEL	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin PE0: AN008 (145/144/100/80/69/64-pin) PE1: AN009, CMPB0 (145/144/100/80/69/64/48-pin) PE2: AN010, CVREFB0 (145/144/100/80/69/64/48-pin) PE3: AN011, CMPA1 (145/144/100/80/69/64/48-pin) PE4: AN012, CMPA2 (145/144/100/80/69/64/48-pin) PE5: AN013 (145/144/100/80/69/64-pin) PE6: AN014 (145/144/100-pin) PE7: AN015 (145/144/100-pin)	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin PE0: AN016 (80/64-pin) PE1: AN017, CMPB0 (80/64/48/32-pin) PE2: AN018, CVREFB0 (80/64/48/32-pin) PE3: AN019 (80/64/48/32-pin) PE4: AN020, CMPA2 (80/64/48/32-pin) PE5: AN021 (80/64-pin)

Table 2.50 Comparison of PF5 Pin Function Control Register (PFnPFS)

Register	Bit	RX210 (n = 0 to 3)	RX140
PF5PFS	—	PF5 pin function control register	—

Table 2.51 Comparison of PHn Pin Function Control Register (PHnPFS)

Register	Bit	RX210 (n = 0 to 3)	RX140 (n = 0 to 3)
PH0PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0111b: CACREF	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3B 00111b: CACREF 11001b: TS10
PH1PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0101b: TMO0	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3D 00101b: TMO0 11001b: TS9
PH2PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0101b: TMRI0	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4C 00101b: TMRI0 11001b: TS8
PH3PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX140)	Pin function select bits 0000b: Hi-Z 0101b: TMCI0	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 00101b: TMCI0 11001b: TS7

Table 2.52 Comparison of PJn Pin Function Control Register (PJnPFS)

Register	Bit	RX210 (n = 1, 3)	RX140 (n = 1, 6, 7)
PJ3PFS	—	PJ3 pin function control register	—
PJ3PFS	ASEL	—	Analog function select bit

Table 2.53 Comparison of PKn Pin Function Control Register (PKnPFS)

Register	Bit	RX210 (n = 1, 3)	RX140 (n = 1, 6, 7)
PKnPFS	—	PKn pin function control register	—

Table 2.54 Comparisons of Multi-Function Pin Controller Registers

Register	Bit	RX210	RX140
PFCSE	—	CS output enable register	—
PFAOE0	—	Address output enable register 0	—
PFAOE1	—	Address output enable register 1	—
PFBCR0	—	External bus control register 0	—
PFBCR1	—	External bus control register 1	—

2.18 Port Output Enable 2

Table 2.55 is a comparative overview of the port output enable 2 modules.

Table 2.55 Comparative Overview of Port Output Enable 2 Modules

Item	RX210 (POE2a)	RX140 (POE2a)
High-impedance control by input level detection	• Ability to specify falling-edge detection or sampling of the low level 16 times at PCLK/8, PCLK/16, or PCLK/128 clock cycles for each of the POE0# to POE3# and POE8# input pins • Ability to put pins for complementary PWM output from the MTU in the high-impedance state on detection of falling edges or sampling of the low level on the POE0# to POE3# pins • Ability to put pins for output from MTU0 in the high-impedance state on detection of falling edges or sampling of the low level on the POE8# pin.	• Ability to specify falling-edge detection or sampling of the low level 16 times at PCLK/8, PCLK/16, or PCLK/128 clock cycles for each of the POE0# to POE3#, and POE8# input pins • Ability to put pins for complementary PWM output from the MTU in the high-impedance state on detection of falling edges or sampling of the low level on the POE0# to POE3# pins • Ability to put pins for output from MTU0 in the high-impedance state on detection of falling edges or sampling of the low level on the POE8# pin.
High-impedance control by output level comparison	Ability to compare levels output on pins for complementary PWM output from the MTU and put them in the high-impedance state when simultaneous output of the active level continues for one or more cycles of the PCLK clock	Ability to compare levels output on pins for complementary PWM output from the MTU and put them in the high-impedance state when simultaneous output of the active level continues for one or more cycles of the PCLK clock
High-impedance control by oscillation stop detection	Ability to put pins for complementary PWM output from the MTU and output pins for MTU0 in the high-impedance state when oscillation by the clock generation circuit stops	Ability to put pins for complementary PWM output from the MTU and output pins for MTU0 in the high-impedance state when oscillation by the clock generation circuit stops
High-impedance control by software (registers)	Ability to put pins for complementary PWM output from the MTU and output pins for MTU0 in the high-impedance state by writing to the POE registers	Ability to put pins for complementary PWM output from the MTU and output pins for MTU0 in the high-impedance state by writing to the POE registers
High-impedance control by event signals	Ability to put pins for complementary PWM output from the MTU and output pins for MTU0 in the high-impedance state in response to an event signal from the event link controller (ELC)	—
Interrupts	Ability to generate interrupts in response to the results of POE0# to POE3# and POE8# input-level detection or MTU complementary PWM output-level comparison	Ability to generate interrupts in response to the results of POE0# to POE3#, and POE8# input-level detection or MTU complementary PWM output-level comparison

2.19 Compare Match Timer

Table 2.56 is a comparative overview of the compare match timers, and Table 2.57 is a comparison of compare match timer registers.

Table 2.56 Comparative Overview of Compare Match Timers

Item	RX210 (CMT)	RX140 (CMT)
Number of channels	4 channels	2 channels
Count clocks	Four frequency-divided clocks: One clock from among PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected individually for each channel.	Four frequency-divided clocks: One clock from among PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected individually for each channel.
Interrupt	A compare match interrupt can be requested for each channel.	A compare match interrupt can be requested for each channel.
Event link function (output)	Event signal output at CMT1 compare match	Event signal output at CMT1 compare match
Event link function (input)	• Support for linked operation of specified module • Support for CMT1 counter start, event counter, and count restart	• Support for linked operation of specified module • Support for CMT1 counter start, event counter, and count restart
Low power consumption function	Ability to specify module stop state for each unit	Ability to specify module stop state for each unit

Table 2.57 Comparison of Compare Match Timer Registers

Register	Bit	RX210 (CMT)	RX140 (CMT)
CMSTR1	—	Compare match timer start register 1	—

2.20 Realtime Clock

Table 2.58 is a comparative overview of realtime clocks, and Table 2.59 is a comparison of realtime clock registers.

Table 2.58 Comparative Overview of Realtime Clocks

Item	RX210 (RTCb)	RX140 (RTCB)
Count modes	Calendar count mode	Calendar count mode/binary count mode
Count source	Sub-clock (XCIN)	Sub-clock (XCIN)
Clock and calendar functions	• Year, month, date, day-of-week, hour, minute, second are counted, BCD display • Indicates the state of the sub-seconds range as 1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, or 64 Hz in binary. • 12 hours/24 hours mode switching function • Start/stop function • 30-second adjustment function (Fewer than 30 seconds is rounded down to 00 seconds, and 30 seconds or more is rounded up to one minute.) • Automatic leap year adjustment function • 1 Hz clock output • Time error adjustment function	• Calendar count mode — Year, month, date, day-of-week, hour, minute, second are counted, BCD display — 12 hours/24 hours mode switching function — 30 seconds adjustment function (a number less than 30 is rounded down to 00 seconds, and 30 seconds or more are rounded up to one minute) — Automatic adjustment function for leap years • Binary count mode Count seconds in 32 bits, binary display • Common to both modes — Start/stop function — The sub-second digit is displayed in binary units (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, or 64 Hz). — Clock error correction function — Clock (1 Hz/64 Hz) output
Interrupts	• Alarm interrupt (ALM) Comparison with year, month, date, day of the week, hour, minute, or second can be selected as the condition for the alarm interrupt. • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, or 1/256 second can be selected as an interrupt period.	• Alarm interrupt (ALM) As an alarm interrupt condition, selectable which of the below is compared with: — Calendar count mode: Year, month, date, day-of-week, hour, minute, or second can be selected — Binary count mode: Each bit of the 32-bit binary counter • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, or 1/256 second can be selected as an interrupt period.

Item	RX210 (RTCb)	RX140 (RTCB)
Interrupts	• Carry interrupt (CUP) Indicates occurrence of a carry to the seconds counter or a carry to the 64 Hz counter during reading of the 64 Hz counter. • Recovery from software standby mode or deep software standby mode can be performed by an alarm interrupt or periodic interrupt.	• Carry interrupt (CUP) An interrupt is generated at either of the following timings: — When a carry from the 64 Hz counter to the second counter is generated. — When the 64-Hz counter is changed and the R64CNT register is read at the same time. • Recovery from software standby mode can be performed by an alarm interrupt or periodic interrupt
Time-capture function	The times when any of three event signals are input can be captured. The month, date, hour, minute, and second are captured for each event.	—
Event link function	Periodic event output	—

Table 2.59 Comparison of Realtime Clock Registers

Register	Bit	RX210 (RTCe)	RX140 (RTCc)
RSECCNT/ BCNT0	—	Second counter	Second counter/binary counter 0
RMINCNT/ BCNT1	—	Minute counter	Minute counter/binary counter 1
RHRCNT/ BCNT2	—	Hour counter	Hour counter/binary counter 2
RWKCNT/ BCNT3	—	Day-of-week counter	Day-of-week counter/binary counter 3
RSECAR/ BCNT0AR	—	Second alarm register	Second alarm register/binary counter 0 alarm register
RMINAR/ BCNT1AR	—	Minute alarm register	Minute alarm register/binary counter 1 alarm register
RHRAR/ BCNT2AR	—	Hour alarm register	Hour alarm register/binary counter 2 alarm register
RWKAR/ BCNT3AR	—	Day-of-week alarm register	Day-of-week alarm register/binary counter 3 alarm register
RDAYAR/ BCNT0AER	—	Date alarm register	Date alarm register/binary counter 0 alarm enable register
RMONAR/ BCNT1AER	—	Month alarm register	Month alarm register/binary counter 1 alarm enable register
RYRAR/ BCNT2AER	—	Year alarm register	Year alarm register/binary counter 2 alarm enable register
RYRAREN/ BCNT3AER	—	Year alarm enable register	Year alarm enable register/binary counter 3 alarm enable register
RCR2	CNTMD	—	Count mode select bit
RCR3	—	RTC control register 3	—
RTCCRy	—	Time capture control register y (y = 0 to 2)	—
RSECCPy	—	Second capture register y (y = 0 to 2)	—
RMINCPy	—	Minute capture register y (y = 0 to 2)	—
RHRCPy	—	Hour capture register y (y = 0 to 2)	—
RDAYCPy	—	Date capture register y (y = 0 to 2)	—
RMONCPy	—	Month capture register y (y = 0 to 2)	—

2.21 Independent Watchdog Timer

Table 2.60 is a comparative overview of the independent watchdog timers, and Table 2.61 is a comparison of independent watchdog timer registers.

Table 2.60 Comparative Overview of Independent Watchdog Timers

Item	RX210 (IWDTa)	RX140 (IWDTa)
Count source	IWDT-dedicated clock (IWDTCLK)	IWDT-dedicated clock (IWDTCLK)
Clock division ratio	Divide by1, 16, 32, 64, 128, or 256	Divide by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Counting automatically starts after a reset (auto-start mode) • Counting is started (register start mode) by refreshing the counter (writing 00h and then FFh to the IWDTRR register).	• Auto-start mode: Counting starts automatically after a reset. • Register start mode: Counting is started by refreshing the counter (writing 00h and then FFh to the IWDTRR register).
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error is generated Counting restarts (in auto-start mode, counting automatically restarts after a reset or after a non-maskable interrupt request is output. In register start mode, counting restarts after refreshing.)	• Reset (the down-counter and other registers return to their initial values) • Low power consumption state (by means of register setting) • Underflow or refresh error (register start mode only)
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Reset output sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt sources	• A non-maskable interrupt (WUNI) is generated when the down-counter underflows. • When refreshing is done outside the refresh-permitted period (refresh error)	• Down-counter underflows • When refreshing is done outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read by the IWDTSR register.	The down-counter value can be read by the IWDTSR register.
Event link function (output)	• Down-counter underflow event output • Refresh error event output	—
Output signals (internal signals)	• Reset output • Interrupt request output • Sleep mode count stop control output	• Reset output • Interrupt request output • Sleep mode count stop control output

Item	RX210 (IWDTa)	RX140 (IWDTa)
Auto-start mode (controlled by option function select register 0 (OFS0))	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the watchdog timer (OFS0.IWDTRPSS[1:0]bits) • Selecting the window end position in the watchdog timer (OFS0.IWDTRPES[1:0]bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0]bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0]bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (OFS0.IWDTSLCSTP bit)
Register start mode (controlled by the IWDT registers)	• Selecting the clock frequency division ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)	• Selecting the clock frequency division ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (IWDTCSTPR.SLCSTP bit)

Table 2.61 Comparison of Independent Watchdog Timer Registers

Register	Bit	RX210 (IWDTCR)	RX140 (IWDTCR)
IWDTCR	TOPS[1:0]	Time-out period selection bits b1 b0 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh)	Time-out period selection bits b1 b0 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1,024 cycles (03FFh) 1 1: 2,048 cycles (07FFh)
IWDTCSTPR	SLCSTP	Sleep mode count stop control bit 0: Count stop is disabled. 1: Counting is stopped at a transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode.	Sleep mode count stop control bit 0: Count stop is disabled. 1: Counting is stopped at a transition to sleep mode, software standby mode, or deep sleep mode.

2.22 Serial Communications Interface

Table 2.62 is a comparative overview of the serial communications interfaces, and Table 2.63 is a comparison of serial communications interface channel specifications, and Table 2.64 is a comparison of serial communications interface registers.

Table 2.62 Comparative Overview of Serial Communications Interfaces

Item		RX210 (SCIc, SCId)	RX140 (SCIg, SCIk, SCIh)
Number of channels		• SCIc: 12 channels • SCId: 1 channel	• SCIg: 3 channels • SCIk: 2 channels • SCIh: 1 channel
Serial communications modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable as LSB first or MSB first transfer.	Selectable as LSB first or MSB first transfer.
I/O signal level inversion		—	The levels of input and output signals can be inverted independently (SCI1 and SCI5).
Interrupt sources		Transmit end, transmit data empty, receive data full, and receive error, completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)	Transmit end, transmit data empty, receive data full, receive error, and data match (SCI1 and SCI5), completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)
Low power consumption function		Individual channels can be transitioned to the module stop state.	Individual channels can be transitioned to the module stop state.
Asynchronous mode	Data length	7 or 8 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection function	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	CTSn and RTSn pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.

Item		RX210 (SCIc, SCId)	RX140 (SCIg, SCIk, SCIh)
Asynchronous mode	Data match detection	—	Compares receive data and comparison data, and generates interrupt when they are matched (SCI1 and SCI5)
	Start-bit detection	—	Low level or falling edge is selectable.
	Receive data sampling timing adjustment	—	The receive data sampling point can be shifted from the center of the data forward or backward to a base point (SCI1 and SCI5).
	Transmit signal change timing adjustment	—	Either the falling or rising edge of the transmit data can be delayed (SCI1 and SCI5).
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly or by reading the SPTR.RXDMON flag (SCI1 or SCI5).
	Clock source	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5, SCI6, and SCI12).	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5, SCI6, and SCI12).
	Double-speed mode	—	Baud rate generator double-speed mode is selectable.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	CTSn and RTSn pins can be used in controlling transmission/ reception.	CTSn# and RTSn# pins can be used in controlling transmission/ reception.
Smart card interface mode	Error processing	• An error signal can be automatically transmitted when detecting a parity error during reception • Data can be automatically retransmitted when receiving an error signal during transmission	• An error signal can be automatically transmitted when detecting a parity error during reception • Data can be automatically retransmitted when receiving an error signal during transmission
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.

Item		RX210 (SCIc, SCId)	RX140 (SCIg, SCIk, SCIh)
Simple I²C mode	Communication format	I²C bus format (MSB-first transfer only)	I²C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer rate	Up to 384 kbps	Fast mode is supported.
	Noise cancellation	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.
Extended serial mode (supported by SCI12 only)	Start frame transmission	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection
	Start frame reception	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two kinds of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two kinds of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates

Item		RX210 (SCIc, SCId)	RX140 (SCIg, SCIk, SCIh)
Extended serial mode (supported by SCI12 only)	I/O control function	• Ability to select polarity or TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select receive data sampling timing of RXDX12 pin • Signals received on RXDX12 can be passed through to SCIc when the extended serial mode control section is turned off.	• Ability to select polarity or TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select receive data sampling timing of RXDX12 pin
	Timer function	Usable as reloading timer	Usable as reloading timer
Bit rate modulation function		—	Correction of outputs from the on-chip baud rate generator can reduce errors.
Event link function (supported by SCI5 only)		• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output	• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output

Table 2.63 Comparison of Serial Communications Interface Channel Specifications

Item	RX210 (SCIc, SCId)	RX140 (SCIg, SCIk, SCIh)
Synchronous mode	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12	SCI1, SCI5, SCI6, SCI8, SCI9, SCI12
Clock synchronous mode	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12	SCI1, SCI5, SCI6, SCI8, SCI9, SCI12
Smart card interface mode	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12	SCI1, SCI5, SCI6, SCI8, SCI9, SCI12
Simple I^2C mode	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12	SCI1, SCI5, SCI6, SCI8, SCI9, SCI12
Simple SPI mode	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12	SCI1, SCI5, SCI6, SCI8, SCI9, SCI12
Data match detection	—	SCI1, SCI5
Extended serial mode	SCI12	SCI12
TMR clock input	SCI5, SCI6, SCI12	SCI5, SCI6, SCI12
Event link function	SCI5	SCI5
Peripheral module clock	PCLKB: SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12	PCLKB: SCI1, SCI5, SCI6, SCI8, SCI9, SCI12

Table 2.64 Comparison of Serial Communications Interface Registers

Register	Bit	RX210 (SCIc, SCId)	RX140 (SCIg, SCIk, SCIh)
RDRH, RDRL, RDRHL	—	—	Receive data registers H, L, and HL
TDRH, TDRL, TDRHL	—	—	Transmit data registers H, L, and HL
SMR	CHR	Character length bit (Valid only in asynchronous mode.) 0: Transmit/receive in 8-bit data length 1: Transmit/receive in 7-bit data length	Character length bit (Valid only in asynchronous mode.) Selects in combination with the SCMR.CHR1 bit. CHR1 CHR 0 0: Transmit/receive in 9-bit data length 0 1: Transmit/receive in 9-bit data length 1 0: Transmit/receive in 8-bit data length (initial value) 1 1: Transmit/receive in 7-bit data length
	CM	Communications mode bit 0: Asynchronous mode 1: Clock synchronous mode	Communications mode bit 0: Asynchronous mode or simple I^2C mode 1: Clock synchronous mode or simple SPI mode

Register	Bit	RX210 (SCIc, SCId)	RX140 (SCIg, SCIk, SCIh)
SCR	CKE[1:0]	Clock enable bits (Asynchronous mode) b1 b0 0 0: On-chip baud rate generator The SCKn pin is available for use as an I/O port in accord with the I/O port settings. 0 1: On-chip baud rate generator A clock with the same frequency as the bit rate is output on the SCKn pin. 1 x: External clock or TMR clock*1 When using an external clock, input a clock with a frequency 16 times the bit rate on the SCKn pin. When the SEMR.ABCS bit is set to 1, input a clock with a frequency eight times the bit rate. The TMR clock may be used. (Clock synchronous mode) b1 b0 0 x: Internal clock: The SCKn pin functions as the clock output pin. 1 x: External clock: The SCKn pin functions as the clock input pin.	Clock enable bits (Asynchronous mode) b1 b0 0 0: On-chip baud rate generator The SCKn pin is in the high-impedance state. 0 1: On-chip baud rate generator A clock with the same frequency as the bit rate is output on the SCKn pin. 1 x: External clock or TMR clock*1 When using an external clock, input a clock with a frequency 16 times the bit rate on the SCKn pin. When the SEMR.ABCS bit is set to 1, input a clock with a frequency eight times the bit rate. When using the TMR clock, the SCKn pin is in the high-impedance state. (Clock synchronous mode) b1 b0 0 x: Internal clock: The SCKn pin functions as the clock output pin. 1 x: External clock: The SCKn pin functions as the clock input pin.
	MPIE	Multi-processor interrupt enable bit (Valid in asynchronous mode when the SMR.MP bit is set to 1.) 0: Normal reception 1: When data with the multi-processor bit set to 0 is received, the data is not read, and setting the status flags ORER and FER in SSR to 1 is disabled. When data with the multiprocessor bit set to 1 is received, the MPIE bit is automatically cleared to 0, and normal reception resumes.	Multi-processor interrupt enable bit (Valid in asynchronous mode when the SMR.MP bit is set to 1.) 0: Normal reception 1: When data with the multi-processor bit set to 0 is received, the data is not read, and setting the status flags RDRF, ORER, and FER in the SSR register to 1 is disabled. When data with the multi-processor bit set to 1 is received, the MPIE bit is automatically cleared to 0, and normal reception resumes.
SCMR	CHR1	—	Character length bit 1
MDDR	—	—	Modulation duty register

Register	**Bit**	**RX210 (SCIc, SCId)**	**RX140 (SCIg, SCIk, SCIh)**
SEMR	ACS0	Asynchronous mode clock source select bit (Valid only in asynchronous mode.) 0: External clock input 1: TMR clock input (valid only for SCI5, SCI6, and SCI12)	Asynchronous mode clock source select bit (Valid only in asynchronous mode.) 0: External clock input 1: Logical AND of two compare matches output from TMR (valid for SCI5, SCI6, and SCI12 only) Available compare match output varies per SCI channel.
	ITE	—	Immediate transmission enable bit
	BRME	—	Bit rate modulation enable bit
	ABCSE	—	Asynchronous mode base clock select extended bit
	BGDM	—	Baud rate generator double-speed mode select bit
	RXDESEL	—	Asynchronous start bit edge detection select bit
SIMR1	IICM	Simple I²C mode select bit SMIF IICM 0 0: Serial interface mode (in asynchronous, synchronous, or simple SPI mode) 0 1: Simple I²C mode 1 0: Smart card interface mode 1 1: Setting prohibited.	Simple I²C mode select bit SMIF IICM 0 0: Asynchronous mode, multi-processor mode, or clock synchronous mode (in asynchronous, synchronous, or simple SPI mode) 0 1: Simple I²C mode 1 0: Smart card interface mode 1 1: Setting prohibited.
SPMR	MSS	Master slave select bit 0: TXDn pin: transmission, RXDn pin: reception (master mode) 1: TXDn pin: reception, RXDn pin: transmission (slave mode)	Master slave select bit 0: SMOSIn pin: transmission, SMISOn pin: reception (master mode) 1: SMOSIn pin: reception, SMISOn pin: transmission (slave mode)
CDR	—	—	Comparison data register
DCCR	—	—	Data comparison control register
SPTR	—	—	Serial port register
TMGR	—	—	Transmit/receive timing select register

Register	Bit	RX210 (SCIc, SCId)	RX140 (SCIg, SCIk, SCIh)
CR2	BCCS [1:0]	Bus collision detection clock select bits b5 b4 0 0: SCI Base clock 0 1: SCI Base clock frequency divided by 2 1 0: SCI Base clock frequency divided by 4 1 1: Setting prohibited.	Bus collision detection clock select bits • When SEMR.BGDM = 0, or SEMR.BGDM = 1 and SMR.CKS[1:0] = other than 00b b5 b4 0 0: Base clock 0 1: Base clock frequency divided by 2 1 0: Base clock frequency divided by 4 1 1: Setting prohibited. • When SEMR.BGDM = 1 and SMR.CKS[1:0] = 00b b5 b4 0 0: Base clock frequency divided by 2 0 1: Base clock frequency divided by 4 1 0: Setting prohibited. 1 1: Setting prohibited.

Note: 1. Selectable on SCI5, SCI6, and SCI12 only.

2.23 I^{2}C Bus Interface

Table 2.65 is a comparison of I^{2}C bus interface registers.

Table 2.65 Comparison of I^{2}C Bus Interface Registers

Register	Bit	RX210 (RIIC)	RX140 (RIICa)
ICMR2	TMWE	Timeout internal counter write enable bit	—
TMOCNT	—	Timeout internal counter	—

2.24 Serial Peripheral Interface

Table 2.66 is a comparative overview of serial peripheral interfaces, and Table 2.67 is a comparison of serial peripheral interface registers.

Table 2.66 Comparative Overview of Serial Peripheral Interfaces

Item	RX210 (RSPI)	RX140 (RSPIc)
Number of channels	1 channel	1 channel
RSPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Capable of serial communication in master/slave mode. • Capable of switching the polarity of the serial transfer clock. • Capable of switching the phase of the serial transfer clock.	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK
Data format	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits).	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits). • Byte swapping of transmit and receive data is selectable
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the maximum divisor is 4096). • In slave mode, the externally input clock is used as the serial clock (the maximum frequency is that of PCLK divided by 8). — Width at high level: 4 cycles of PCLK Width at low level: 4 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4). — Width at high level: 2 cycles of PCLK Width at low level: 2 cycles of PCLK
Buffer configuration	• Double buffer configuration for the transmit/receive buffers	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers

Item	RX210 (RSPI)	RX140 (RSPIc)
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection
SSL control function	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) — Range:1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) — Range:1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity
Control in master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function
Interrupt sources	• RSPI receive interrupt (receive buffer full) • RSPI transmit interrupt (transmit buffer empty) • RSPI error interrupt (mode fault, overrun, or parity error) • RSPI idle interrupt (RSPI idle)	• Receive buffer full interrupt • Transmit buffer empty interrupt • Error interrupt (mode fault, overrun, underrun, or parity error) • Idle interrupt

Item	RX210 (RSPI)	RX140 (RSPIc)
Event link function (output)	The following five types of events can be output to the event link controller. • Reception buffer full event output • Transmission buffer empty event output • Mode fault, overrun, or parity error event output • RSPI idle event output • Transmission-completed event output	—
Other functions	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode	• Function for initializing the RSPI • Loopback mode
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.67 Comparison of Serial Peripheral Interface Registers

Register	Bit	RX210 (RSPI)	RX140 (RSPIc)
SPSR	UDRF	—	Underrun error flag
SPDCR	SPBYT	—	RSPI byte access specification bit
SPCR2	SPPE	Parity enable bit 0: A parity bit is not added to transmit data, and no parity checking of receive data is performed. 1: A parity bit is added to transmit data, and parity checking of receive data is performed (when SPCR.TXMD = 0). A parity bit is added to transmit data, but no parity checking of receive data is performed (when SPCR.TXMD = 1).	Parity enable bit 0: A parity bit is not added to transmit data, and no parity checking of receive data is performed. 1: A parity bit is added to transmit data, and parity checking of receive data is performed.
	SCKASE	—	RSPCK auto-stop function enable
SPDCR2	—	—	RSPI data control register 2

2.25 12-Bit A/D Converter

Table 2.68 is a comparative overview of the 12-bit A/D converters, and Table 2.69 is a comparison of 12-bit A/D converter registers.

Table 2.68 Comparative Overview of 12-Bit A/D Converters

Item	RX210 (S12ADb)	RX140 (S12ADE)
Number of units	1 unit	1 unit
Input channels	16 channels	18 channels
Extended analog function	Temperature sensor output, internal reference voltage	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	1.0 μs per channel (when A/D conversion clock ADCLK = 50 MHz)	0.88 μs per channel (ADCCR.CCS bit = 0), 0.67 μs per channel (ADCCR.CCS bit = 1) (when A/D conversion clock ADCLK = 48 MHz)
A/D conversion clock	Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency division ratio should be one of the following. PCLK to ADCLK frequency division ratio = 1:1, 1:2, 1:4, 1:8, 2:1, 4:1 ADCLK is set using the clock generation circuit.	Peripheral module clock PCLKB and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. PCLKB to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.
Data registers	• 16 registers for analog input and one for A/D-converted data duplication in double trigger mode • One register for temperature sensor output • One register for internal reference • The results of A/D conversion are stored in 12-bit A/D data registers. • In addition mode, A/D conversion results are added and stored in A/D data registers as 14-bit data. • Duplication of A/D conversion data A/D conversion data of one selected analog input channel is stored in A/D data register y when conversion is started by the first trigger and in the duplication register when started by the second trigger. Duplication is available only when double trigger mode is selected in single scan mode or group scan mode.	• 18 registers for analog input, one for A/D-converted data duplication in double trigger mode • One register for temperature sensor output • One register for internal reference • One register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • 12-bit accuracy output for the results of A/D conversion • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.

Item	RX210 (S12ADb)	RX140 (S12ADE)
Operating modes	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 16 channels arbitrarily selected. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of up to 16 channels arbitrarily selected. • Group scan mode: — Analog inputs of up to 24 arbitrarily selected channels are divided into group A and group B, and A/D conversion of the analog inputs selected on a group basis is performed only once. — Conversion start conditions (synchronous trigger) can be selected independently for group A and group B, allowing A/D conversion of the groups to start at different times.	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 18 channels arbitrarily selected. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of up to 18 channels arbitrarily selected. • Group scan mode: — Analog inputs of up to 18 arbitrarily selected channels are divided into group A and group B, and A/D conversion of the analog inputs selected on a group basis is performed only once. — Conversion start conditions (synchronous trigger) can be selected independently for group A and group B, allowing A/D conversion of the groups to start at different times. • Group scan mode (when group A is given priority): — If a group A trigger is input during A/D conversion on group B, A/D conversion on group B is stopped and A/D conversion is performed on group A. — Restart (rescan) of A/D conversion on group B after completion of A/D conversion on group A can be enabled.
Conditions for A/D conversion start	• Software trigger • Synchronous trigger Trigger by MTU, ELC or temperature sensor. • Asynchronous trigger A/D conversion can be triggered by the ADTRG0# pin.	• Software trigger • Synchronous trigger Trigger by the multi-function timer pulse unit (MTU) or event link controller (ELC) • Asynchronous trigger A/D conversion can be triggered by the external trigger ADTRG0# pin.

Item	RX210 (S12ADb)	RX140 (S12ADE)
Functions	• Sample-and-hold function • Channel-dedicated sample-and-hold function (0.25 V ≤ analog voltage input ≤ AVCC0 to 0.25 V) • Variable sampling state count • Self-diagnosis of 12-bit A/D converter • A/D-converted value addition mode • Analog input disconnection detection assist • Double trigger mode (duplication of A/D conversion data)	• Variable sampling state count • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers • Compare function (window A and window B) • 16 ring buffers when the compare function is used
Interrupt sources	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan. • In group scan mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of group A scan, whereas an A/D scan end interrupt request (GBADI) for group B can be generated on completion of group B scan. • When double trigger mode is selected in group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan of group A, whereas A/D scan end interrupt request (GBADI) specially for group B can be generated on completion of group B scan. • The S12ADI0 or GBADI interrupts can activate the DMA controller (DMAC) or the data transfer controller (DTC).	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan. • In group scan mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of group A scan, whereas an A/D scan end interrupt request (GBADI) for group B can be generated on completion of group B scan. • When double trigger mode is selected in group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan of group A, whereas A/D scan end interrupt request (GBADI) specially for group B can be generated on completion of group B scan. • The S12ADI0 and GBADI interrupts can activate the data transfer controller (DTC).

Item	RX210 (S12ADb)	RX140 (S12ADE)
Event link function	• An ELC event can be generated on completion of scans other than group B scan in group scan mode. • A/D conversion can be started by a trigger from the ELC.	• An ELC event is generated on completion of scans other than group B scan in group scan mode. • An ELC event is generated on completion of group B scan in group scan mode. • An ELC event is generated on completion of all scans. • Scan can be started by a trigger output by the ELC. • An ELC event is generated according to the event conditions of the window compare function in single scan mode.
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.69 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX210 (S12ADb)	RX140 (S12ADE)
ADDRy	—	A/D data register y (y = 0 to 15)	A/D data register y (y = 0 to 8, 16 to 21, 24 to 26)
ADRD	DIAGST[1:0]	Self-diagnosis status bits	—
ADCSR	ADHSC	—	A/D conversion select bit
ADANSA	—	A/D channel select register A	—
ADANSA0	—	—	A/D channel select register A0
ADANSA1	—	—	A/D channel select register A1
ADANSB	—	A/D channel select register B	—
ADANSB0	—	—	A/D channel select register B0
ADANSB1	—	—	A/D channel select register B1
ADADS	—	A/D-converted value addition mode select register	—
ADADS0	—	—	A/D-converted value addition/ average function select register 0
ADADS1	—	—	A/D-converted value addition/ average function select register 1
ADADC	ADC[1:0] (RX210) ADC[2:0] (RX140)	Addition count select bits b1 b0 0 0: 1-time conversion (no addition, same as normal conversion) 0 1: 2-time conversion (addition once) 1 0: 3-time conversion (addition twice) 1 1: 4-time conversion (addition 3 times)	Addition count select bits b2 b0 0 0 0: 1-time conversion (no addition, same as normal conversion) 0 0 1: 2-time conversion (addition once) 0 1 0: 3-time conversion (addition twice) 0 1 1: 4-time conversion (addition three times) 1 0 1: 16-time conversion (addition 15 times) Settings other than the above are prohibited.
	AVEE	—	Average mode enable bit

Register	Bit	RX210 (S12ADb)	RX140 (S12ADE)
ADSTRGR	TRSB[3:0] (RX210) TRSB[5:0] (RX140)	A/D conversion start trigger select for group B bits	A/D conversion start trigger select for group B bits
	TRSA[3:0] (RX210) TRSA[5:0] (RX140)	A/D conversion start trigger select bits	A/D conversion start trigger select bits
ADEXICR	TSSAD	—	Temperature sensor output A/D converted value addition/ average mode select bit
	OCSAD	Internal reference voltage A/D-converted value addition mode select bit 0: Internal reference voltage A/D-converted value addition mode is not selected. 1: Internal reference voltage A/D-converted value addition mode is selected.	Internal reference voltage A/D-converted value addition/ average mode select bit 0: Internal reference voltage A/D-converted value addition/ average mode is not selected. 1: Internal reference voltage A/D-converted value addition/ average mode is selected.
	TSS(RX210) TSSA(RX140)	Temperature sensor output A/D conversion select bits	Temperature sensor output A/D conversion select bits
	OCS(RX210) OCSA(RX140)	Internal reference voltage A/D conversion select bits	Internal reference voltage A/D conversion select bits
ADSSTRn	—	A/D sampling state register n (n = 0 to 7, L, T, O)	A/D sampling state register n (n = 0 to 8, L, T, O)
ADSHCR	—	A/D sample and hold circuit control register	—
ADELCCR	—	—	A/D event link control register
ADGSPCR	—	—	A/D group scan priority control register
ADCMPCR	—	—	A/D compare function control register
ADCMPANSR0	—	—	A/D compare function window A channel select register 0
ADCMPANSR1	—	—	A/D compare function window A channel select register 1
ADCMPANSER	—	—	A/D compare function window A extended input select register
ADCMPLR0	—	—	A/D compare function window A comparison condition setting register 0
ADCMPLR1	—	—	A/D compare function window A comparison condition setting register 1
ADCMPLER	—	—	A/D compare function window A extended input comparison condition setting register
ADCMPDR0	—	—	A/D compare function window A lower-side level setting register
ADCMPDR1	—	—	A/D compare function window A upper-side level setting register

Register	Bit	RX210 (S12ADb)	RX140 (S12ADE)
ADCMPSR0	—	—	A/D compare function window A channel status register 0
ADCMPSR1	—	—	A/D compare function window A channel status register 1
ADCMPSER	—	—	A/D compare function window A extended input channel status register
ADHVREFCNT	—	—	A/D high-potential/low-potential reference voltage control register
ADWINMON	—	—	A/D compare function window A/B status monitor register
ADCMPBNSR	—	—	A/D compare function window B channel select register
ADWINLLB	—	—	A/D compare function window B lower-side level setting register
ADWINULB	—	—	A/D compare function window B upper-side level setting register
ADCMPBSR	—	—	A/D compare function window B channel status register
ADBUFn	—	—	A/D data storage buffer register n (n = 0 to 15)
ADBUFEN	—	—	A/D data storage buffer enable register
ADBUFPTR	—	—	A/D data storage buffer pointer register
ADCCR	—	—	A/D convert cycle control register

2.26 D/A Converter

Table 2.70 is a comparative overview of the D/A converters, and Table 2.71 is a comparison of D/A converter registers.

Table 2.70 Comparative Overview of D/A Converters

Item	RX210 (DA)	RX140 (DAa)
Resolution	10 bits	8 bits
Output channels	2 channels	2 channels
Measure against interference between analog modules	—	Measure against interference between D/A and A/D converters: D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable signal output by the 12-bit A/D converter. This reduces degradation of A/D conversion accuracy due to interference by controlling the timing of the 8-bit D/A converter inrush current with the enable signal.
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state
Event link function (input)	Ability to start D/A conversion on channel 0 when an event signal is input	Ability to start D/A conversion on channel 0 when an event signal is input

Table 2.71 Comparison of D/A Converter Registers

Register	Bit	RX210 (DA)	RX140 (DAa)
DACR	DAE	D/A enable bit	—
DAADSCR	—	—	D/A A/D synchronous start control register

2.27 Temperature Sensor

Table 2.72 is a comparative overview of temperature sensor, and Table 2.73 is a comparison of temperature sensor registers.

Table 2.72 Comparative Overview of Temperature Sensor

Item	RX210 (TEMPSa)	RX140 (TEMPSA)
Temperature sensor voltage output	Temperature sensor outputs a voltage to the 12-bit A/D converter via a programmable gain amplifier (PGA).	The temperature sensor voltage is output to the 12-bit A/D converter.
Low power consumption function	Ability to specify module stop state	—

Table 2.73 Comparison of Temperature Sensor Registers

Register	Bit	RX210 (TEMPSa)	RX140 (TEMPSA)
TSCR	—	Temperature sensor control register	—
TSCDR	—	—	Temperature sensor calibration data register

2.28 Comparator B

Table 2.74 is a comparative overview of the comparator B modules, and Table 2.75 is a comparison of comparator B registers.

Table 2.74 Comparative Overview of Comparator B Modules

Item	RX210 (CMPB)	RX140 (CMPBa)
Analog input voltage	Voltage input to CMPBn pin (n = 0 or 1)	Voltage input to CMPBn pin
Reference input voltage	Voltage input to CVREFBn pin (n = 0 or 1)	Voltage input to CVREFBn pin or internal reference voltage
Comparison result	Read from the CPBFLG.CPBnOUT flag (n = 0 or 1)	• Read from the CPBFLG.CPBnOUT flag • Ability to output comparison result to CMPOBn pin.
Interrupt request generation timing	• When comparator B0 comparison result changes • When comparator B1 comparison result changes	• When comparator B0 comparison result changes • When comparator B1 comparison result changes
Timing of event generation to ELC	• When comparator B0 comparison result changes • When comparator B0 or comparator B1 comparison result changes	• When comparator B0 comparison result changes • When comparator B0 or comparator B1 comparison result changes
Selectable functions	Digital filter function Ability to specify whether or not the digital filter is applied and to select the sampling frequency	• Digital filter function Ability to specify whether or not the digital filter is applied and to select the sampling frequency • Window function Ability to specify whether or the window function is enabled or disabled (VRFL < CMPBn (n = 0 or 1) < VRFH) • Reference input voltage Ability to select CVREFBn pin (n = 0 or 1) input or internal reference voltage (generated internally) • Comparator B response speed Ability to select high-speed or low-speed mode
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Table 2.75 Comparison of Comparator B Registers

Register	Bit	RX210 (CMPBa)	RX140 (CMPBa)
CPB1CNT2	—	—	Comparator B1 control register 2
CPBFLG	CPB0OUT	Comparator B0 monitor flag 0: CMPB0 < CVREFB0 1: CMPB0 > CVREFB0	Comparator B0 monitor flag (When the window function is disabled) 0: CMPB0 < CVREFB0, CMPB0 < internal reference voltage, or comparator B0 operation disabled 1: CMPB0 > CVREFB0, or CMPB0 > internal reference voltage (When the window function is enabled) 0: CMPB0 < VRFL, CMPB0 > VRFH, or comparator B0 operation disabled 1: VRFL < CMPB0 < VRFH
	CPB1OUT	Comparator B1 monitor flag 0: CMPB1 < CVREFB1 1: CMPB1 > CVREFB1	Comparator B1 monitor flag (When the window function is disabled) 0: CMPB1 < CVREFB1, CMPB1 < internal reference voltage, or comparator B1 operation disabled 1: CMPB1 > CVREFB1, or CMPB1 > internal reference voltage (When the window function is enabled) 0: CMPB1 < VRFL, CMPB1 > VRFH, or comparator B1 operation disabled 1: VRFL < CMPB1 < VRFH
CPBMD	—	—	Comparator B1 mode select register
CPBREF	—	—	Comparator B reference input voltage select register
CPBOCR	—	—	Comparator B output control register

2.29 RAM

Table 2.76 is a comparative overview of RAM.

Table 2.76 Comparative Overview of RAM

Item	RX210	RX140
RAM capacity	Max. 96 KB (RAM0: 64 KB, RAM1: 32 KB)	Max. 64 KB
RAM address	• RAM capacity 96 KB RAM0: 0000 0000h to 0000 FFFFh RAM1: 0001 0000h to 0001 7FFFh • RAM capacity 64 KB RAM0: 0000 0000h to 0000 FFFFh • RAM capacity 32 KB RAM0: 0000 0000h to 0000 7FFFh • RAM capacity 20 KB RAM0: 0000 0000h to 0000 4FFFh • RAM capacity 16 KB RAM0: 0000 0000h to 0000 3FFFh • RAM capacity 12 KB RAM0: 0000 0000h to 0000 2FFFh	• RAM capacity 64 KB RAM0: 0000 0000h to 0000 FFFFh • RAM capacity 32 KB RAM0: 0000 0000h to 0000 7FFFh • RAM capacity 16 KB RAM0: 0000 0000h to 0000 3FFFh
Access	• Single-cycle access is possible for both reading and writing. • RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. • RAM can be enabled or disabled.
Low power consumption function	Ability to specify module stop state independently for RAM0 and RAM1.	Ability to specify module stop state

2.30 Flash Memory

Table 2.77 is a comparative overview of flash memory, and Table 2.78 is a comparison of flash memory registers.

Table 2.77 Comparative Overview of Flash Memory

Item	RX210	RX140 (FLASH)
Memory capacity	• User area: Up to 1 MB • Data area: 8 KB • User boot area: 16 KB	• User area: Up to 256 KB • Data area: Up to 8 KB • Extra area: Stores the start-up area information, access window information, and unique ID
Addresses	• Products with capacity of 1 MB FFF0 0000h to FFFF FFFFh • Products with capacity of 768 KB FFF4 0000h to FFFF FFFFh • Products with capacity of 512 KB FFF8 0000h to FFFF FFFFh • Products with capacity of 384 KB FFFA 0000h to FFFF FFFFh • Products with capacity of 256 KB FFFC 0000h to FFFF FFFFh • Products with capacity of 128 KB FFFE 0000h to FFFF FFFFh • Products with capacity of 96 KB FFFE 8000h to FFFF FFFFh • Products with capacity of 64 KB FFFF 0000h to FFFF FFFFh	• Products with capacity of 256 KB FFFC 0000h to FFFF FFFFh • Products with capacity of 128 KB FFFE 0000h to FFFF FFFFh • Products with capacity of 64 KB FFFF 0000h to FFFF FFFFh
FCU commands (RX210) Software commands (RX140)	• The following FCU commands are implemented P/E normal mode transition, status read mode transition, lock bit read mode transition (lock bit read 1), peripheral clock notification, programming, block erase, P/E suspend, P/E resume, status register clear, lock bit read 2/blank check	• The following software commands are implemented: Program, blank check, block erase, and all-block erase • The following commands are implemented for programming the extra area: Start-up area information program, access window protect, and access window information program
Value after erasure	• ROM: FFh • E2 DataFlash: undefined	• ROM: FFh • E2 DataFlash: FFh
Interrupt	An interrupt (FRDYI) is generated upon completion of FCU command execution.	An interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.

Item		RX210	RX140 (FLASH)
On-board programming		• Programming in boot mode — The clock synchronous serial interface (SCI1) is used. — The communication speed is adjusted automatically. — The user boot area is also programmable. • Programming in user boot mode — A user-specific boot program can be created. • Programming using a ROM programming routine in a user program — The ROM/E2 DataFlash can be programmed without resetting the system.	• Boot mode (SCI interface) — Channel 1 of the serial communications interface (SCI1) is used for asynchronous communication. — The user area and data area can be programmed. • Boot mode (FINE interface) — The FINE interface is used. — The user area and data area can be programmed. • Self-programming (single-chip mode) — The user area and data area can be programmed using a flash programming routine in a user program.
Off-board programming		A PROM programmer can be used to program the user area and user boot area.	The user area and data area can be programmed using a flash programmer compatible with the MCU.
ID codes protection		• Connection with a serial programmer can be controlled using ID codes in boot mode. • Connection with an on-chip debugging emulator can be controlled using ID codes.	• Connection with a serial programmer can be controlled using ID codes in boot mode. • Connection with an on-chip debugging emulator can be controlled using ID codes.
Protection functions	Software-controlled protection function	• The FENTRYR.FENTRYD bit, FWEPROR.FLWE[1:0] bits, lock bits, and DFLRE0 and DFLWE0 registers can be used to prevent unintentional programming. • Protection with the DFLRE0 and DFLWE0 registers is applied in 2 KB units.	The DFLCTL.DFLEN bit and FENTRYR.FENTRY0 bit can be used to prevent unintentional programming.
	Command-locked state	This function disables further programming or erasure when an abnormal operation is detected during programming or erasure.	—
	Boot program protection	Programming or erasure of the user boot area is only possible in boot mode.	—
	Start-up program protection function	—	This function is used to safely program blocks 0 to 7.
	Area protection	—	During self-programming, this function enables programming only of specified blocks in the user area and disables programming of the other blocks.

Item	RX210	RX140 (FLASH)
Background operation (BGO) function	• Programs in the ROM area can run while the E2 DataFlash is being programmed or erased. • The CPU can run programs in areas other than the ROM or E2 DataFlash while the ROM is being programmed or erased.	Programs in the ROM can run while the E2 DataFlash is being programmed.

Table 2.78 Comparison of Flash Memory Registers

Register	Bit	RX210	RX140 (FLASH)
DFLCTL	—	—	E2 DataFlash control register
MEMWAITR	—	—	Memory wait cycle setting register
FENTRYR	FENTRY1	ROM P/E mode entry 1 bit	—
DFLWAITR	—	—	Data flash wait cycle setting register
FPR	—	—	Protection unlock register
FPSR	—	—	Protection unlock status register
FPMCR	—	—	Flash P/E mode control register
FISR	—	—	Flash initial setting register
FRESETR	—	Flash reset register FRESETR is a 16-bit register.	Flash reset register FRESETR is an 8-bit register.
	FRKEY[7:0]	Key code bits	—
FASR	—	—	Flash area select register
FCR	—	—	Flash control register
FEXCR	—	—	Flash extra area control register
FSARH	—	—	Flash processing start address register H
FSARL	—	—	Flash processing start address register L
FEARH	—	—	Flash processing end address register H
FEARL	—	—	Flash processing end address register L
FWBn	—	—	Flash write buffer register n (n = 0 to 3)
FSTATR0	ERSERR (RX210) ERERR (140)	Erasure error bit (b5)	Erase error flag (b0)
	PRGERR	Programming error bit (b4)	Program error flag (b1)
	BCERR	—	Blank check error flag
	ILGLERR	Illegal command error bit (b6)	Illegal command error flag (b4)
	EILGLERR	—	Extra area illegal command error flag
	PRGSPD	Programming suspend status bit	—
	ERSSPD	Erasure suspend status bit	—
	SUSRDY	Suspend ready bit	—
	FRDY	Flash ready bit	—

Register	Bit	RX210	RX140 (FLASH)
FSTATR1	FRDY	—	Flash ready flag
	EXRDY	—	Extra area ready flag
	FLOCKST	Lock bit status bit	—
	FCUERR	FCU error bit	—
FEAMH	—	—	Flash error address monitor register H
FEAML	—	—	Flash error address monitor register L
FSCMR	—	—	Flash start-up setting monitor register
FAWSMR	—	—	Flash access window start address monitor register
FAWEMR	—	—	Flash access window end address monitor register
UIDRn	—	—	Unique ID register n (n = 0 to 3)
FWEPROR	—	Flash write erase protection register	—
FMODR	—	Flash mode register	—
FASTAT	—	Flash access status register	—
FAEINT	—	Flash access error interrupt enable register	—
FCURAME	—	FCU RAM enable register	—
FRDYIE	—	Flash ready interrupt enable register	—
FPROTR	—	Flash protection register	—
FCMDR	—	FCU command register	—
FCPSR	—	FCU processing switching register	—
FPESTAT	—	Flash P/E status register	—
PCKAR	—	Peripheral clock notification register	—
FMODR	—	Flash mode register	—
FASTAT	—	Flash access status register	—
FAEINT	—	Flash access error interrupt enable register	—
DFLRE0	—	E2 DataFlash read enable register 0	—
DFLWE0	—	E2 DataFlash programming/erasure enable register 0	—
DFLBCCNT	—	E2 DataFlash blank check control register	—
DFLBCSTAT	—	E2 DataFlash blank check status register	—

2.31 Packages

As indicated in Table 2.79, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage.

Table 2.79 Packages

Package Type	Renesas Code			
	RX210			RX140
	Chip Version A	Chip Version B	Chip Version C	—
145-pin TFLGA	✕	○	✕	✕
144-pin LQFP	✕	○	✕	✕
100-pin TFLGA	PTLG0100JA-A	PTLG0100JA-A PTLG0100KA-A	PTLG0100JA-A	✕
100-pin LQFP	PLQP0100KB-A	PLQP0100KB-A	PLQP0100KB-A	✕
80-pin LFQFP	✕	✕	✕	○
80-pin LQFP	PLQP0080KB-A	PLQP0080KB-A PLQP0080JA-A	PLQP0080KB-A PLQP0080JA-A	✕
69-pin WLBGA	✕	○	✕	✕
64-pin TFLGA	✕	○	✕	✕
64-pin LFQFP	✕	✕	✕	○
64-pin LQFP	PLQP0064KB-A	PLQP0064KB-A PLQP0064GA-A	PLQP0064KB-A PLQP0064GA-A	PLQP0064GA-A
48-pin LQFP	✕	○	✕	✕
48-pin LFQFP	✕	✕	✕	○
48-pin HWQFN	✕	✕	✕	○
32 -pin LQFP	✕	✕	✕	○
32-pin HWQFN	✕	✕	✕	○

○: Package available (Renesas code omitted); ✕: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by **blue text**. Items that exists on both groups with different specifications are indicated by **red text**. **Black text** indicates there is no differences in the item's specifications between groups.

3.1 80-Pin Package

Table 3.1 is a comparative listing of the pin functions of 80-pin package products.

Table 3.1 Comparative Listing of 80-Pin Package Pin Functions

80-Pin LFQFP/ LQFP	RX210	RX140
1	VREFH	P06*1
2	P03/DA0	P03*1/DA0
3	VREFL	P04*1
4	VCL	VCL
5	PJ1/MTIOC3A	PJ1/MTIOC3A
6	MD/FINED	MD/PG7/FINED
7	XCIN	XCIN/PH7
8	XCOUT	XCOUT/PH6
9	RES#	RES#
10	XTAL/P37	XTAL/P37/IRQ4
11	VSS	VSS
12	EXTAL/P36	EXTAL/P36/IRQ2
13	VCC	VCC
14	P35/NMI	P35/NMI
15	P34/MTIOC0A/TMCI3/POE2#/SCK6/IRQ4	P34/MTIOC0A/TMCI3/POE2#/SCK6/IRQ4
16	P32/MTIOC0C/TMO3/TXD6/SMOSI6/SSDA6/ IRQ2-DS/RTCOUT/RTCIC2	P32/MTIOC0C/TMO3/TXD6/SMOSI6/SSDA6/ TS0/IRQ2/RTCOUT
17	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/ IRQ1-DS/RTCIC1	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/ TS1/IRQ1
18	P30/MTIOC4B/TMRI3/POE8#/RXD1/ SMISO1/SSCL1/IRQ0-DS/RTCIC0	P30/MTIOC4B/TMRI3/POE8#/RXD1/ SMISO1/SSCL1/TS2/IRQ0
19	P27/MTIOC2B/TMCI3/SCK1	P27/MTIOC2B/TMCI3/SCK1/TS3
20	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1	P26/MTIOC2A/TMO1/LPTO/TXD1/SMOSI1/ SSDA1/TS4
21	P21/MTIOC1B/TMCI0/RXD0/SSCL0	P21/MTIOC1B/TMCI0
22	P20/MTIOC1A/TMRI0/TXD0/SSDA0	P20/MTIOC1A/TMRI0
23	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ SCK1/MISOA/SDA-DS/IRQ7	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ SCK1/MISOA/SDA0/IRQ7
24	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/ SMOSI1/SSDA1/MOSIA/SCL-DS/IRQ6/ RTCOUT/ADTRG0#	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/ SMOSI1/SSDA1/MOSIA/SCL0/IRQ6/ RTCOUT/ADTRG0#
25	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/IRQ5	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/CRXD0/TS5/IRQ5
26	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/IRQ4	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/CTXD0/TS6/IRQ4
27	P13/MTIOC0B/TMO3/SDA/IRQ3	P13/MTIOC0B/TMO3/SDA0/IRQ3
28	P12/TMCI1/SCL/IRQ2	P12/TMCI1/SCL0/IRQ2
29	PH3/TMCI0	PH3/MTIOC4D/TMCI0/TS7

80-Pin LFQFP/ LQFP	RX210	RX140
30	PH2/TMRI0/IRQ1	PH2/MTIOC4C/TMRI0/TS8/IRQ1
31	PH1/TMO0/IRQ0	PH1/MTIOC3D/TMO0/TS9/IRQ0
32	PH0/CACREF	PH0/MTIOC3B/TS10/CACREF
33	P55/MTIOC4D/TMO3	P55/MTIOC4A/MTIOC4D/TMO3/CRXD0/ TS11
34	P54/MTIOC4B/TMCI1	P54/MTIOC4B/TMCI1/CTXD0/TS12
35	PC7/MTIOC3A/TMO2/MTCLKB/TXD8/ SMOSI8/SSDA8/MISOA/CACREF	PC7/MTCLKB/MTIOC3A/TMO2/LPTO/ MISOA/TXD8/SMOSI8/SSDA8/TS13/ CACREF
36	PC6/MTIOC3C/MTCLKA/TMCI2/RXD8/ SMISO8/SSCL8/MOSIA	PC6/MTIOC3C/MTCLKA/TMCI2/MOSIA/ RXD8/SMISO8/SSCL8/TS14
37	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/ RSPCKA	PC5/MTIOC0C/MTIOC3B/MTCLKD/TMRI2/ RSPCKA/SCK8/TS15
38	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/ SCK5/CTS8#/RTS8#/SS8#/SSLA0	PC4/MTIOC0A/MTIOC3D/MTCLKC/TMCI1/ POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0/ TSCAP
39	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5/TS16
40	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/ SSLA3	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/ SSLA3/TS17
41	PB7/MTIOC3B/TXD9/SMOSI9/SSDA9	PB7/PC1*2/MTIOC3B/TXD9/SMOSI9/ SSDA9/TS18
42	PB6/MTIOC3D/RXD9/SMISO9/SSCL9	PB6/PC0*2/MTIOC3D/RXD9/SMISO9/ SSCL9/TS19
43	PB5/MTIOC2A/MTIOC1B/TMRI1/POE1#/ SCK9	PB5/MTIOC2A/MTIOC1B/TMRI1/POE1#/ SCK9/TS20
44	PB4/CTS9#/RTS9#/SS9#	PB4/CTS9#/RTS9#/SS9#/TS21
45	PB3/MTIOC0A/MTIOC4A/TMO0/POE3#/ SCK6	PB3/MTIOC0A/MTIOC4A/TMO0/POE3#/ LPTO/SCK6/TS22
46	PB2/CTS6#/RTS6#/SS6#	PB2/CTS6#/RTS6#/SS6#/TS23
47	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD6/ SMOSI6/SSDA6/IRQ4-DS	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD6/ SMOSI6/SSDA6/TS24/IRQ4/CMPOB1
48	VCC	VCC
49	PB0/MTIC5W/RXD6/SMISO6/SSCL6/ RSPCKA	PB0/MTIOC3D/MTIC5W/RXD6/SMISO6/ SSCL6/RSPCKA/TS25
50	VSS	VSS
51	PA6/MTIC5V/MTCLKB/TMCI3/POE2#/ CTS5#/RTS5#/SS5#/MOSIA	PA6/MTIOC3D/MTIC5V/MTCLKB/TMCI3/ POE2#/CTS5#/RTS5#/SS5#/MOSIA/TS26
52	PA5/RSPCKA	PA5/RSPCKA/TS27
53	PA4/MTIC5U/MTCLKA/TMRI0/TXD5/ SMOSI5/SSDA5/SSLA0/IRQ5-DS/CVREFB1	PA4/MTIOC4C/MTIC5U/MTCLKA/TMRI0/ TXD5/SMOSI5/SSDA5/SSLA0/TS28/IRQ5/ CVREFB1
54	PA3/MTIOC0D/MTCLKD/RXD5/SMISO5/ SSCL5/IRQ6-DS/CMPB1	PA3/MTIOC0D/MTIOC4D/MTIC5V/MTCLKD/ RXD5/SMISO5/SSCL5/TS29/IRQ6/CMPB1
55	PA2/RXD5/SMISO5/SSCL5/SSLA3	PA2/RXD5/SMISO5/SSCL5/SSLA3/TS30
56	PA1/MTIOC0B/MTCLKC/SCK5/SSLA2/ CVREFA	PA1/MTIOC0B/MTIOC3B/MTCLKC/SCK5/ SSLA2/TS31
57	PA0/MTIOC4A/SSLA1/CACREF	PA0/MTIOC4A/SSLA1/TS32/CACREF
58	PE5/MTIOC4C/MTIOC2B/IRQ5/AN013	PE5/MTIOC4C/MTIOC2B/IRQ5/AN021/ CMPOB0
59	PE4/MTIOC4D/MTIOC1A/AN012/CMPA2	PE4/MTIOC4D/MTIOC1A/MTIOC4A/TS33/ AN020/CMPA2/CLKOUT

80-Pin LFQFP/ LQFP	RX210	RX140
60	PE3/MTIOC4B/POE8#/CTS12#/RTS12#/ SS12#/AN011/CMPA1	PE3/MTIOC1B/MTIOC4B/POE8#/CTS12#/ RTS12#/SS12#/TS34/AN019/CLKOUT
61	PE2/MTIOC4A/RXD12/RXDX12/SMISO12/ SSCL12/IRQ7-DS/AN010/CVREFB0	PE2/MTIOC4A/RXD12/RXDX12/SMISO12/ SSCL12/TS35/IRQ7/AN018/CVREFB0
62	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12/AN009/CMPB0	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12/AN017/CMPB0
63	PE0/SCK12/AN008	PE0/SCK12/AN016
64	PD2/MTIOC4D/IRQ2	PD2/MTIOC4D/SCK6/IRQ2/AN026
65	PD1/MTIOC4B/IRQ1	PD1/MTIOC4B/RXD6/SMISO6/SSCL6/IRQ1/ AN025
66	PD0/IRQ0	PD0/TXD6/SMOSI6/SSDA6/IRQ0/AN024
67	P47/AN007	P47*1/AN007
68	P46/AN006	P46*1/AN006
69	P45/AN005	P45*1/AN005
70	P44/AN004	P44*1/AN004
71	P43/AN003	P43*1/AN003
72	P42/AN002	P42*1/AN002
73	P41/AN001	P41*1/AN001
74	VREFL0	VREFL0/PJ7*1
75	P40/AN000	P40*1/AN000
76	VREFH0	VREFH0/PJ6*1
77	AVCC0	AVCC0
78	P07/ADTRG0#	P07*1/ADTRG0#
79	AVSS0	AVSS0
80	P05/DA1	P05*1/DA1

Notes: 1. The power supply of the I/O buffer for these pins is AVCC0.
2. PC0 and PC1 are valid only when the port switching function is selected.

3.2 64-Pin Package

Table 3.2 is a comparative listing of the pin functions of 64-pin package products.

Table 3.2 Comparative Listing of 64-Pin Package Pin Functions

64-Pin LFQFP/ LQFP	RX210	RX140
1	P03/DA0	P03*1/DA0
2	VCL	VCL
3	MD/FINED	MD/PG7/FINED
4	XCIN	XCIN/PH7*3
5	XCOUT	XCOUT/PH6*3
6	RES#	RES#
7	XTAL/P37	XTAL/P37/IRQ4
8	VSS	VSS
9	EXTAL/P36	EXTAL/P36/IRQ2
10	VCC	VCC
11	P35/NMI	P35/NMI
12	P32/MTIOC0C/TMO3/TXD6/SMOSI6/SSDA6/ IRQ2-DS/RTCOUT/RTCIC2	P32/MTIOC0C/TMO3/TXD6*3/SMOSI6*3/ SSDA6*3/TS0*3/IRQ2/RTCOUT
13	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/ IRQ1-DS/RTCIC1	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/ TS1*3/IRQ1
14	P30/MTIOC4B/TMRI3/POE8#/RXD1/ SMISO1/SSCL1/IRQ0-DS/RTCIC0	P30/MTIOC4B/TMRI3/POE8#/RXD1/ SMISO1/SSCL1/TS2*3/IRQ0
15	P27/MTIOC2B/TMCI3/SCK1	P27/MTIOC2B/TMCI3/SCK1/TS3
16	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1	P26/MTIOC2A/TMO1/LPTO/TXD1/SMOSI1/ SSDA1/TS4
17	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ SCK1/MISOA/SDA-DS/IRQ7	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ SCK1/MISOA/SDA0/IRQ7
18	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/ SMOSI1/SSDA1/MOSIA/SCL-DS/IRQ6/ RTCOUT/ADTRG0#	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/ SMOSI1/SSDA1/MOSIA/SCL0/IRQ6/ RTCOUT/ADTRG0#
19	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/IRQ5	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/CRXD0/TS5*3/IRQ5
20	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/IRQ4	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/CTXD0/TS6*3/IRQ4
21	PH3/TMCI0	PH3/MTIOC4D/TMCI0/TS7*3
22	PH2/TMRI0/IRQ1	PH2/MTIOC4C/TMRI0/TS8*3/IRQ1
23	PH1/TMO0/IRQ0	PH1/MTIOC3D/TMO0/TS9*3/IRQ0
24	PH0/CACREF	PH0/MTIOC3B/TS10*3/CACREF
25	P55/MTIOC4D/TMO3	P55/MTIOC4A/MTIOC4D/TMO3/CRXD0/ TS11*3
26	P54/MTIOC4B/TMCI1	P54/MTIOC4B/TMCI1/CTXD0/TS12*3
27	PC7/MTIOC3A/TMO2/MTCLKB/TXD8/ SMOSI8/SSDA8/MISOA/CACREF	PC7/MTIOC3A/MTCLKB/TMO2/LPTO/ TXD8*3/SMOSI8*3/SSDA8*3/MISOA/TS13/ CACREF
28	PC6/MTIOC3C/MTCLKA/TMCI2/RXD8/ SMISO8/SSCL8/MOSIA	PC6/MTIOC3C/MTCLKA/TMCI2/RXD8*3/ SMISO8*3/SSCL8*3/MOSIA/TS14
29	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/ RSPCKA	PC5/MTIOC0C/MTIOC3B/MTCLKD/TMRI2/ SCK8*3/RSPCKA/TS15

64-Pin LFQFP/ LQFP	RX210	RX140
30	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/ SCK5/CTS8#/RTS8#/SS8#/SSLA0	PC4/MTIOC0A/MTIOC3D/MTCLKC/TMCI1/ POE0#/SCK5/CTS8#*3/RTS8#*3/SS8#*3/ SSLA0/TSCAP
31	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5/ TS16*3
32	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/ SSLA3	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/ SSLA3/TS17*3
33	PB7/MTIOC3B/TXD9/SMOSI9/SSDA9	PB7/PC1*2/MTIOC3B/TXD9*3/SMOSI9*3/ SSDA9*3/TS18*3
34	PB6/MTIOC3D/RXD9/SMISO9/SSCL9	PB6/PC0*2/MTIOC3D/RXD9*3/SMISO9*3/ SSCL9*3/TS19*3
35	PB5/MTIOC2A/MTIOC1B/TMRI1/POE1#/ SCK9	PB5/MTIOC2A/MTIOC1B/TMRI1/POE1#/ SCK9*3/TS20*3
36	PB3/MTIOC0A/MTIOC4A/TMO0/POE3#/ SCK6	PB3/MTIOC0A/MTIOC4A/TMO0/POE3#/ LPTO/SCK6*3/TS22*3
37	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD6/ SMOSI6/SSDA6/IRQ4-DS	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD6*3/ SMOSI6*3/SSDA6*3/TS24*3/IRQ4/CMPOB1
38	VCC	VCC
39	PB0/MTIC5W/RXD6/SMISO6/SSCL6/ RSPCKA	PB0/MTIOC3D/MTIC5W/RXD6*3/SMISO6*3/ SSCL6*3/RSPCKA/TS25
40	VSS	VSS
41	PA6/MTIC5V/MTCLKB/TMCI3/POE2#/ CTS5#/RTS5#/SS5#/MOSIA	PA6/MTIOC3D/MTIC5V/MTCLKB/TMCI3/ POE2#/CTS5#/RTS5#/SS5#/MOSIA/TS26*3
42	PA4/MTIC5U/MTCLKA/TMRI0/TXD5/ SMOSI5/SSDA5/SSLA0/IRQ5-DS/CVREFB1	PA4/MTIOC4C/MTIC5U/MTCLKA/TMRI0/ TXD5/SMOSI5/SSDA5/SSLA0/TS28/IRQ5/ CVREFB1
43	PA3/MTIOC0D/MTCLKD/RXD5/SMISO5/ SSCL5/IRQ6-DS/CMPB1	PA3/MTIOC0D/MTIOC4D/MTIC5V/MTCLKD/ RXD5/SMISO5/SSCL5/TS29/IRQ6/CMPB1
44	PA1/MTIOC0B/MTCLKC/SCK5/SSLA2/ CVREFA	PA1/MTIOC0B/MTIOC3B/MTCLKC/SCK5/ SSLA2/TS31
45	PA0/MTIOC4A/SSLA1/CACREF	PA0/MTIOC4A/SSLA1/TS32*3/CACREF
46	PE5/MTIOC4C/MTIOC2B/IRQ5/AN013	PE5/MTIOC4C/MTIOC2B/IRQ5/AN021/ CMPOB0
47	PE4/MTIOC4D/MTIOC1A/AN012/CMPA2	PE4/MTIOC4D/MTIOC1A/MTIOC4A/TS33/ AN020/CMPA2/CLKOUT
48	PE3/MTIOC4B/POE8#/CTS12#/RTS12#/ SS12#/AN011/CMPA1	PE3/MTIOC1B/MTIOC4B/POE8#/CTS12#/ RTS12#/SS12#/TS34/AN019/CLKOUT
49	PE2/MTIOC4A/RXD12/RXDX12/SMISO12/ SSCL12/IRQ7-DS/AN010/CVREFB0	PE2/MTIOC4A/RXD12/RXDX12/SMISO12/ SSCL12/TS35/IRQ7/AN018/CVREFB0
50	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12/AN009/CMPB0	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12/AN017/CMPB0
51	PE0/SCK12/AN008	PE0/SCK12/AN016
52	VREFL	P47*1/AN007
53	P46/AN006	P46*1AN006
54	VREFH	P45*1/AN005
55	P44/AN004	P44*1/AN004
56	P43/AN003	P43*1/AN003
57	P42/AN002	P42*1/AN002
58	P41/AN001	P41*1/AN001
59	VREFL0	VREFL0/PJ7*1
60	P40/AN000	P40*1/AN000

64-Pin LFQFP/ LQFP	RX210	RX140
61	VREFH0	VREFH0/PJ6*1
62	AVCC0	AVCC0
63	P05/DA1	P05*1/DA1
64	AVSS0	AVSS0

Notes: 1. The power supply of the I/O buffer for these pins is AVCC0.
2. PC0 and PC1 are valid only when the port switching function is selected.
3. Not implemented on products with a ROM capacity of 64 KB.

3.3 48-Pin Package

Table 3.3 is a comparative listing of the pin functions of 48-pin package products.

Table 3.3 Comparative Listing of 48-Pin Package Pin Functions

48-Pin LFQFP/ HWQFN	RX210	RX140
1	VCL	VCL
2	MD/FINED	MD/PG7/FINED
3	RES#	RES#
4	XTAL/P37	XTAL/P37/IRQ4
5	VSS	VSS
6	EXTAL/P36	EXTAL/P36/IRQ2
7	VCC	VCC
8	P35/NMI	P35/NMI
9	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/ IRQ1-DS	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/ TS1*3/IRQ1
10	P30/MTIOC4B/TMRI3/POE8#/RXD1/ SMISO1/SSCL1/IRQ0-DS	P30/MTIOC4B/TMRI3/POE8#/RXD1/ SMISO1/SSCL1/TS2*3/IRQ0
11	P27/MTIOC2B/TMCI3/SCK1	P27/MTIOC2B/TMCI3/SCK1/TS3
12	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1	P26/MTIOC2A/TMO1/LPTO/TXD1/SMOSI1/ SSDA1/TS4
13	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ SCK1/MISOA/SDA-DS/IRQ7	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ SCK1/MISOA/SDA0/IRQ7
14	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/ SMOSI1/SSDA1/MOSIA/SCL-DS/IRQ6/ ADTRG0#	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/ SMOSI1/SSDA1/MOSIA/SCL0/IRQ6/ ADTRG0#/RTCOUT
15	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/IRQ5	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/CRXD0/TS5*3/IRQ5
16	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/IRQ4	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/CTXD0/TS6*3/IRQ4
17	PH3/TMCI0	PH3/MTIOC4D/TMCI0/TS7*3
18	PH2/TMRI0/IRQ1	PH2/MTIOC4C/TMRI0/TS8*3/IRQ1
19	PH1/TMO0/IRQ0	PH1/MTIOC3D/TMO0/TS9*3/IRQ0
20	PH0/CACREF	PH0/MTIOC3B/TS10*3/CACREF
21	PC7/MTIOC3A/TMO2/MTCLKB/TXD8/ SMOSI8/SSDA8/MISOA/CACREF	PC7/MTIOC3A/TMO2/MTCLKB/LPTO/ TXD8*3/SMOSI8*3/SSDA8*3/MISOA/TS13/ CACREF
22	PC6/MTIOC3C/MTCLKA/TMCI2/RXD8/ SMISO8/SSCL8/MOSIA	PC6/MTIOC3C/MTCLKA/TMCI2/RXD8*3/ SMISO8*3/SSCL8*3/MOSIA/TS14
23	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/ RSPCKA	PC5/MTIOC0C/MTIOC3B/MTCLKD/TMRI2/ SCK8*3/RSPCKA/TS15
24	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/ SCK5/CTS8#/RTS8#/SS8#/SSLA0	PC4/MTIOC0A/MTIOC3D/MTCLKC/TMCI1/ POE0#/SCK5/CTS8#*3/RTS8#*3/SS8#*3/ SSLA0/TSCAP
25	PB5/MTIOC2A/MTIOC1B/TMRI1/POE1#	PB5/PC3*1/MTIOC2A/MTIOC1B/TMRI1/ POE1#/TS20*3
26	PB3/MTIOC0A/MTIOC4A/TMO0/POE3#/ SCK6	PB3/PC2*1/MTIOC0A/MTIOC4A/TMO0/ POE3#/LPTO/SCK6*3/TS22*3
27	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD6/ SMOSI6/SSDA6/IRQ4-DS	PB1/PC1*1/MTIOC0C/MTIOC4C/TMCI0/ TXD6*3/SMOSI6*3/SSDA6*3/TS24*3/IRQ4/ CMPOB1
28	VCC	VCC

48-Pin LFQFP/ HWQFN	RX210	RX140
29	PB0/MTIC5W/RXD6/SMISO6/SSCL6/ RSPCKA	PB0/PC0*1/MTIOC3D/MTIC5W/RXD6*3/ SMISO6*3/SSCL6*3/RSPCKA/TS25
30	VSS	VSS
31	PA6/MTIC5V/MTCLKB/TMCI3/POE2#/ CTS5#/RTS5#/SS5#/MOSIA	PA6/MTIOC3D/MTIC5V/MTCLKB/TMCI3/ POE2#/CTS5#/RTS5#/SS5#/MOSIA/TS26*3
32	PA4/MTIC5U/MTCLKA/TMRI0/TXD5/ SMOSI5/SSDA5/SSLA0/IRQ5-DS/CVREFB1	PA4/MTIOC4C/MTIC5U/MTCLKA/TMRI0/ TXD5/SMOSI5/SSDA5/SSLA0/TS28/IRQ5/ CVREFB1
33	PA3/MTIOC0D/MTCLKD/RXD5/SMISO5/ SSCL5/IRQ6-DS/CMPB1	PA3/MTIOC0D/MTIOC4D/MTIC5V/MTCLKD/ RXD5/SMISO5/SSCL5/TS29/IRQ6/CMPB1
34	PA1/MTIOC0B/MTCLKC/SCK5/SSLA2 CVREFA	PA1/MTIOC0B/MTIOC3B/MTCLKC/SCK5/ SSLA2/TS31
35	PE4/MTIOC4D/MTIOC1A/AN012/CMPA2	PE4/MTIOC4D/MTIOC1A/MTIOC4A/TS33/ AN020/CMPA2/CLKOUT
36	PE3/MTIOC4B/POE8#/CTS12#/RTS12#/ AN011/CMPA1	PE3/MTIOC1B/MTIOC4B/POE8#/CTS12#/ RTS12#/TS34/AN019/CLKOUT
37	PE2/MTIOC4A/RXD12/RXDX12/SSCL12/ IRQ7-DS/AN010/CVREFB0	PE2/MTIOC4A/RXD12/RXDX12/SSCL12/ TS35/IRQ7/AN018/CVREFB0
38	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/ SSDA12/AN009/CMPB0	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/ SSDA12/AN017/CMPB0
39	VREFL	P47*2/AN007
40	P46/AN006	P46*2/AN006
41	VREFH	P45*2/AN005
42	P42/AN002	P42*2/AN002
43	P41/AN001	P41*2/AN001
44	VREFL0	VREFL0/PJ7*2
45	P40/AN000	P40*2/AN000
46	VREFH0	VREFH0/PJ6*2
47	AVCC0	AVCC0
48	AVSS0	AVSS0

Notes: 1. PC0 to PC3 are valid only when the port switching function is selected.
2. The power supply of the I/O buffer for these pins is AVCC0.
3. Not implemented on products with a ROM capacity of 64 KB.

4. Important Information when Migrating Between MCUs

This section presents important information on differences between the RX140 Group and the RX210 Group. 4.1, Notes on Functional Design, presents information regarding the software.

4.1 Notes on Functional Design

Some software that runs on the RX210 Group is compatible with the RX140 Group. Nevertheless, appropriate caution must be exercised due to differences in aspects such as operation timing and electrical characteristics.

Software-related considerations regarding function settings that differ between the RX140 Group and RX210 Group are as follows:

For differences between modules and functions, refer to 2, Comparative Overview of Specifications. For further information, refer to the User's Manual: Hardware of each MCU group, listed in 5, Reference Documents.

4.1.1 VCL Pin (External Capacitor)

Connect a smoothing capacitor rated at 4.7 μF to the VCL pin of the RX140 Group for stabilization of the internal power supply.

4.1.2 Transition to Boot Mode (FINE Interface)

On the RX140 Group a transition to boot mode (FINE interface) occurs when the MD pin is low-level at the time of release from a reset and is then switched to high-level within 20 to 100 msec. For details on operating modes, refer to RX140 Group User's Manual: Hardware, listed in section 5, Reference Documents.

4.1.3 Mode Setting Pins

The mode setting pins after reset cancellation are the MD pin only on the RX140 Group and the MD pin and PC7 pin on the RX210 Group.

4.1.4 User Boot Mode

UB code A, UB code B, and user boot mode are implemented on the RX210 Group but not on the RX140 Group. When using the start-up program protection function on the RX140 Group, it is possible to use any interface to program and erase the user area in flash memory as an alternative to user boot mode. For details, refer to 41.5, Start-Up Program Protection, in RX140 Group User's Manual: Hardware, listed in section 5, Reference Documents.

4.1.5 Clock Frequency Settings

On the RX210 Group it is necessary to make frequency settings for the system clock (ICLK) and external bus clock (BCLK) such that ICLK ≥ BCLK. On the RX140 Group it is necessary to make frequency settings for the system clock (ICLK), peripheral module clocks B and D (PCLKB and PCLKD), and the FlashIF clock (FCLK) such that ICLK:FCLK and PCLKB and PCLKD = 1:N (where N is an integer value).

4.1.6 PLL Circuit

The frequency multiplication factor of the PLL circuit can be set to ×8 to ×25 on the RX210 Group and to ×4 or ×12 (in ×0.5 increments) on the RX140 Group. To use the PLL circuit, change the setting of the PLLCR.STC bits to an appropriate value.

4.1.7 All-Module Clock Stop Mode

The RX140 Group does not have an all-module clock stop mode.

4.1.8 Exception Vector Table

The address of the vector table is fixed on the RX210 Group, but on the RX140 Group the vector table is relocatable using the value set in the exception table register (EXTB) as the start address.

4.1.9 Endian Settings

On the RX210 Group the endian setting is configured in the MDES or MDEB register, according to the operating mode, but on the RX140 Group the endian settings is configured in the MDE register, regardless of the operating mode.

4.1.10 Restrictions on Compare Function

The compare function of the 12-bit A/D converter on the RX140 Group is subject to the following restrictions.

1. The compare function cannot be used together with the self-diagnosis function or double trigger mode. (The compare function is not available for the ADRD and ADDBLDR registers.)
2. It is necessary to specify single scan mode when using match or mismatch event outputs.
3. When the temperature sensor or internal reference voltage is selected for window A, window B operations are disabled.
4. When the temperature sensor or internal reference voltage is selected for window B, window A operations are disabled.
5. It is not possible to set the same channel for window A and window B.
6. It is necessary to specify single scan mode when using the buffer function. (Also, it is not possible to use double trigger mode together with the compare function.)
7. It is necessary to set the reference voltage values such that the high-side reference voltage value is equal to or larger than the low-side reference voltage value.

4.1.11 Eliminating I²C Bus Interface Noise

The RX210 Group has integrated analog noise filters on the SCL and SDA lines, but the RX140 Group has no integrated analog noise filters.

4.1.12 MOSCWTCR Register

On the RX210 Group this register counts cycles of the main clock, but on the RX140 Group it counts cycles of the LOCO clock.

4.1.13 Initialization of Port Direction Register (PDR)

The method of initializing the PDR register differs between the RX210 Group and RX140 Group, even on products with the same pin count.

4.1.14 Scan Conversion Time of 12-Bit A/D Converter

The scan conversion time differs between the RX210 Group and RX140 Group. The scan conversion time (t_{SCAN}) for each group of a single scan where the number of selected channels is n is expressed by the equations below. For details, refer to the description of the 12-bit A/D converter analog input sampling time and scan conversion time in the User's Manual: Hardware of the RX210 Group and RX140 Group, listed in section 5, Reference Documents.

RX210: $t_{SCAN} = t_D + t_{SH} + (t_{DIS} \times n) + t_{DIAG} + (t_{CONV} \times n) + t_{ED}$
RX140: $t_{SCAN} = t_D + (t_{DIS} \times n) + t_{DIAG} + (t_{CONV} \times n) + t_{ED}$

t_D	Start-of-scanning-delay time
t_{SH}	Channel-dedicated sample-and-hold circuit sampling time
t_{SPL}	Sampling time
t_{DIS}	Disconnection detection assist processing time
t_{DIAG}	Self-diagnosis A/D conversion processing time
t_{CONV}	A/D conversion processing time
t_{ED}	End-of-scanning-delay time

4.1.15 Note on Operating Frequency and Voltage Ranges in Operating Power Control Modes

The maximum operating frequencies during flash memory read operations in each of the operating power control modes differ between the RX210 Group and RX140 Group. Refer to the table below for details.

Operating Frequency and Voltage Ranges in Operating Power Control Modes

Operating Power Control Mode	Operating Voltage Range	Operating Frequency Range					
		Flash Memory Read					Flash Memory Programming/ Erasure
		ICLK	FCLK	PCLKD	PCLKB	BCLK	FCLK
High-speed operating mode (RX140)	1.8 to 5.5 V	Up to 48 MHz	Up to 48 MHz	Up to 48 MHz	Up to 32 MHz	—	1 MHz to 48 MHz
High-speed operating mode (RX210)	3.6 to 5.5 V	50 MHz max.	32 MHz max.	50 MHz max.	32 MHz max.	25 MHz max.	4 MHz to 32 MHz
	2.7 to 3.6 V						4 MHz to 32 MHz
	1.8 to 2.7 V	—	—	—	—	—	—
	1.62 to 1.8 V	—	—	—	—	—	—
Middle-speed operating mode (RX140)	1.8 to 5.5 V	Up to 24 MHz	Up to 24 MHz	Up to 24 MHz	Up to 24 MHz	—	1 MHz to 24 MHz
Middle-speed operating mode 1A (RX210)	3.6 to 5.5 V	32 MHz max.	32 MHz max.	32 MHz max.	32 MHz max.	25 MHz max.	4 MHz to 32 MHz
	2.7 to 3.6 V						4 MHz to 32 MHz
	1.8 to 2.7 V						—
	1.62 to 1.8 V	20 MHz max.	20 MHz max.	20 MHz max.	20 MHz max.	20 MHz max.	—
Middle-speed operating mode 1B (RX210)	3.6 to 5.5 V	32 MHz max.	32 MHz max.	32 MHz max.	32 MHz max.	25 MHz max.	—
	2.7 to 3.6 V						4 MHz to 32 MHz
	1.8 to 2.7 V						4 MHz to 32 MHz
	1.62 to 1.8 V	20 MHz max.	20 MHz max.	20 MHz max.	20 MHz max.	20 MHz max.	4 MHz to 32 MHz
Middle-speed operating mode 2 (RX140)	1.8 to 5.5 V	Up to 1 MHz	Up to 1 MHz	Up to 1 MHz	Up to 1 MHz	—	1 MHz
Low-speed operating mode 1 (RX210)	3.6 to 5.5 V	1 MHz max.	1 MHz max.	1 MHz max.	1 MHz max.	1 MHz max.	—
	2.7 to 3.6 V						—
	1.8 to 2.7 V						—
	1.62 to 1.8 V						—
Low-speed operating mode (RX140)	1.8 to 5.5 V	Up to 32.768 kHz	Up to 32.768 kHz	Up to 32.768 kHz	Up to 32.768 kHz	—	—
Low-speed operating mode 2 (RX210)	3.6 to 5.5 V	32.768 kHz max.	32.768 kHz max.	32.768 kHz max.	32.768 kHz max.	32.768 kHz max.	—
	2.7 to 3.6 V						—
	1.8 to 2.7 V						—
	1.62 to 1.8 V						—

4.1.16 Differences Among Chip Versions

There are differences in functionality among the different chip versions of RX210 Group MCUs. Refer to the table below for details.

Section		Specification Differences		
		Chip Version A	Chip Version C	Chip Version B
9. Clock Generation Circuit	9.2.2 System Clock Control Register 3 (SCKCR3)	The main clock oscillator cannot be selected as the clock source.	The main clock oscillator can be selected as the clock source.	← (Same as at left)
	9.2.17 PLL Power Control Register (PLLPCR)	There is no PLLPCR register. Therefore, there is no functionality for powering off the PLL to reduce power consumption.	← (Same as at left)	The PLLPCR register has been added. This provides functionality to power off the PLL to reduce power consumption when the PLL will not be used.
10. Clock Frequency Accuracy Measurement Circuit (CAC)	10.2.2 CAC Control Register 1 (CACR1)	The output clock of the main clock oscillator cannot be selected as the frequency measurement clock.	The output clock of the main clock oscillator can be selected as the frequency measurement clock.	← (Same as at left)
	10.2.3 CAC Control Register 2 (CACR2)	The output clock of the main clock oscillator cannot be selected as the reference signal generation clock.	The output clock of the main clock oscillator can be selected as the reference signal generation clock.	← (Same as at left)
11. Low Power Consumption	11.2.5 Operating Power Control Register (OPCCR)	Middle-speed operating modes 2A and 2B are not implemented.	← (Same as at left)	Middle-speed operating modes 2A and 2B have been added to reduce current consumption during operation.
	11.2.6 Sleep Mode Return Clock Source Switching Register (RSTCKCR)	The main clock oscillator cannot be selected as the sleep mode return clock source.	The main clock oscillator can be selected as the sleep mode return clock source.	← (Same as at left)
	11.2.18 Flash HOCO Software Standby Control Register (FHSSBYCR)	It is necessary to control the power supply for the flash memory in software standby mode.	← (Same as at left)	It is not necessary to control the power supply for the flash memory in software standby mode.
19. I/O Ports	Table 19.2 Port Functions	Port 17 is not 5 V tolerant.	Port 17 is 5 V tolerant.	← (Same as at left)

5. Reference Documents

User's Manual: Hardware

RX210 Group User's Manual: Hardware Rev.1.50 (R01UH0037EJ0150)
(The latest version can be downloaded from the Renesas Electronics website.)

RX140 Group User's Manual: Hardware Rev.1.10 (R01UH0905EJ0110)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This module reflects the content of the following technical updates:

TN-RX*-A035B/E
TN-RX*-A080A/E
TN-RX*-A087A/E
TN-RX*-A094A/E
TN-RX*-A096A/E
TN-RX*-A097A/E
TN-RX*-A099A/E
TN-RX*-A107A/E
TN-RX*-A118A/E
TN-RX*-A138A/E
TN-RX*-A141A/E
TN-RX*-A147A/E
TN-RX*-A151A/E
TN-RX*-A177A/E
TN-RX*-A188A/E
TN-RX*-A193A/E
TN-RX*-A0147B/E
TN-RX*-A0231A/E
TN-RX*-A0224B/E
TN-RX*-A0239B/E
TN-RX*-A0258A/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jan. 31, 2022	—	First edition issued
1.10	Mar. 28, 2022	21	*Corrected:* Table 2.10 Comparison of Clock Generation Circuit Registers
		45	*Revised:* Table 2.30 Comparative Overview of I/O Ports (80-Pin) *Revised:* Table 2.31 Comparative Overview of I/O Ports (64-Pin)
		106	*Revised:* Table 3.1 Comparative Listing of 80-Pin Package Pin Functions
		109	*Revised:* Table 3.2 Comparative Listing of 64-Pin Package Pin Functions

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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