RX140 Group, RX130 Group

Differences Between the RX140 Group and the RX130 Group

Introduction

This application note is intended as a reference to points of difference between the peripheral functions, I/O registers, and pin functions of the RX140 Group and RX130 Group, as well as a guide to key points to consider when migrating between the two groups.

Unless specifically otherwise noted, the information in this application note applies to the 80-pin package version of the RX140 Group and the 100-pin package version of the RX130 Group as the maximum specifications. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the User's Manual: Hardware of the products in question.

Target Devices

RX140 Group and RX130 Group

Contents

1. Comparison of Built-In Functions of RX140 Group and RX130 Group

A comparison of the built-in functions of the RX140 Group and RX130 Group is provided below. For details of the functions, see section 2, Comparative Overview of Specifications and section 5, Reference Documents.

Table 1.1 is a comparison of built-in functions of RX140 Group and RX130 Group.

Table 1.1 Comparison of Built-In Functions of RX140 Group and RX130 Group

Function	RX130	RX140
CPU	●	
Operating modes	○	
Address space	▲	
Resets	○	
Option-setting memory (OFSM)	▲	
Voltage detection circuit (LVDAb)	▲	
Clock generation circuit	●/■	
Clock frequency accuracy measurement circuit (CAC)	○	
Low power consumption	●	
Register write protection function	▲	
Exception handling	●	
Interrupt controller (ICUb)	○	
Buses	▲	
Data transfer controller (DTCa): RX130, (DTCb): RX140	●	
Event link controller (ELC)	●	
I/O ports	●/■	
Multi-function pin controller (MPC)	●/▲	
Multi-function timer pulse unit 2 (MTU2a)	○	
Port output enable 2 (POE2a)	○	
8-bit timer (TMR)	■	
Compare match timer (CMT)	○	
Realtime clock (RTCc)	■	
Low-power timer (LPT): RX130, (LPTa): RX140	●	
Independent watchdog timer (IWDTa)	○	
Serial communications interface (SCIg, SCIh): RX130, (SCIg*1, SCIk, SCIh): RX140	●	
Remote control signal receiver (REMC)	○	×
I²C bus interface (RIICa)	○	
CAN module (RSCAN)	×	○*1
Serial peripheral interface (RSPIa): RX130, (RSPIc): RX140	●/▲	
CRC calculator (CRC)	○	
Capacitive touch sensing unit (CTSUa): RX130, (CTSU2SL*1, CTSU2SL): RX140	●	
AESA	×	○
RNGA	×	○
12-bit A/D converter (S12ADE)	■	
D/A converter (DAa)	○	
Temperature sensor (TEMPSA)	▲	
Comparator B (CMPBa)	○	
Data operation circuit (DOC)	○	
RAM	●/■	
Flash memory (FLASH)	●/■	
Packages	●/■	

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

Note: 1. Not implemented on products with ROM capacity of 64 KB.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Differences in register specifications are not listed.

2.1 CPU

Table 2.1 is a comparative overview of CPU, and Table 2.2 is a comparison of CPU registers.

Table 2.1 Comparative Overview of CPU

Item	RX130	RX140
CPU	• Maximum operating frequency: 32 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Eight 32-bit registers — Accumulator: One 64-bit register • Basic instructions: 73, variable-length instruction format • DSP instructions: 9 • Addressing modes: 10 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits	• Maximum operating frequency: 48 MHz • 32-bit RX CPU (RXv2) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • Basic instructions: 75, variable-length instruction format • Floating point instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits
FPU	—	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard

Table 2.2 Comparison of CPU Registers

Register	Bit	RX130	RX140
EXTB	—	—	Exception table register
FPSW	—	—	Floating-point status word
ACC (RX130) ACC0, ACC1 (RX140)	—	Accumulator	Accumulator 0, accumulator 1

2.2 Address Space

Figure 2.1 is a comparative memory map of single-chip mode.

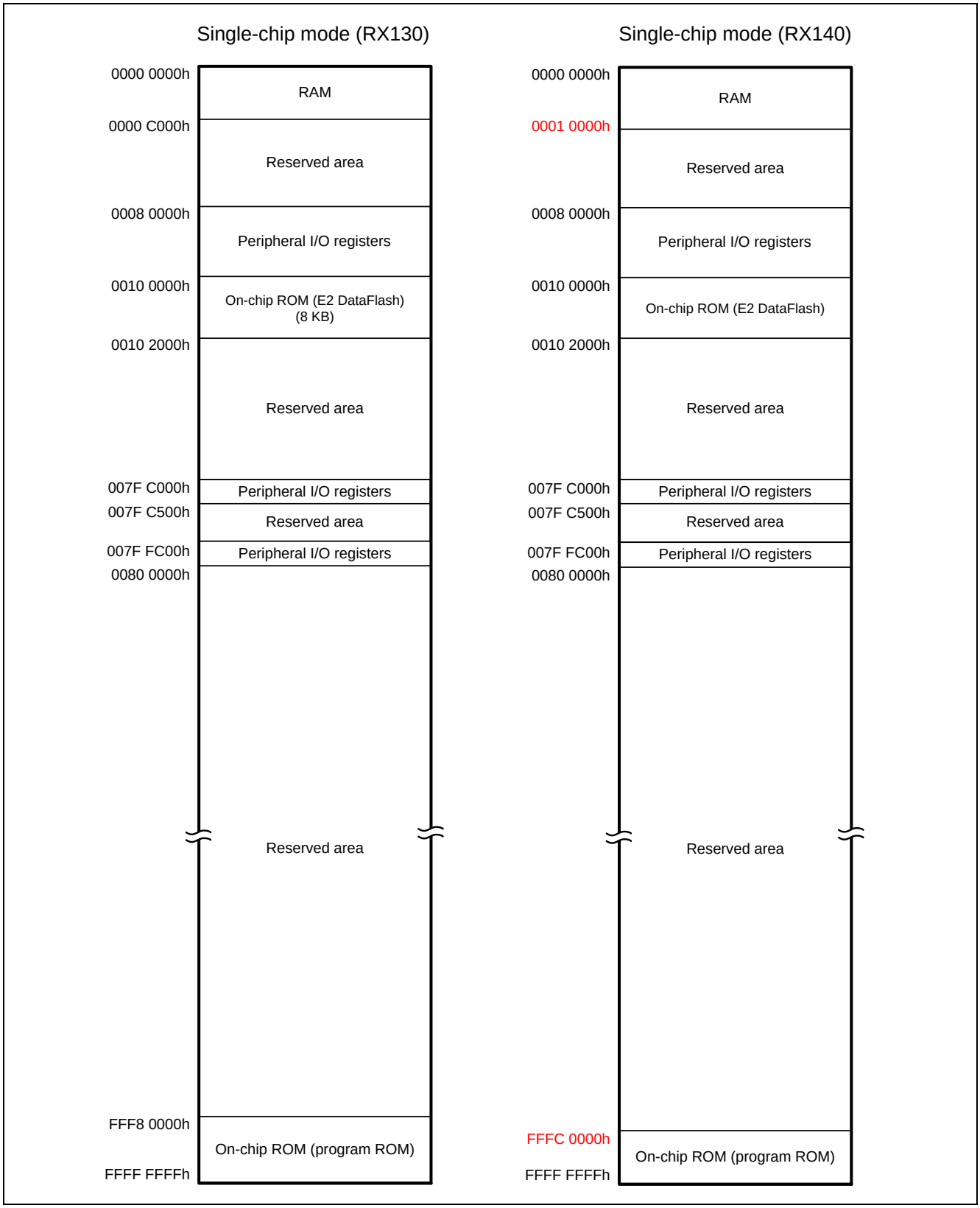

Figure 2.1 Comparative Memory Map of Single-Chip Mode

2.3 Option-Setting Memory

Table 2.3 is a comparison of option-setting memory registers.

Table 2.3 Comparison of Option-Setting Memory Registers

Register	Bit	RX130 (OFSM)	RX140 (OFSM)
OFS1	VDSEL[1:0]	Voltage detection 0 level select bits b1 b0 0 0: 3.84 V is selected 0 1: 2.82 V is selected 1 0: 2.51 V is selected 1 1: 1.90 V is selected	Voltage detection 0 level select bits b1 b0 0 0: 3.85 V is selected 0 1: 2.85 V is selected 1 0: 2.53 V is selected 1 1: 1.90 V is selected
	HOCOFQ[1:0]	—	HOCO frequency selection bits

2.4 Voltage Detection Circuit

Table 2.4 is a comparison of voltage detection circuit registers.

Table 2.4 Comparison of Voltage Detection Circuit Registers

Register	Bit	RX130 (LVDAb)	RX140 (LVDAb)
LVDLVLR	LVD1LVL[3:0]	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 0 0 0: 4.29 V 0 0 0 1: 4.14 V 0 0 1 0: 4.02 V 0 0 1 1: 3.84 V 0 1 0 0: 3.10 V 0 1 0 1: 3.00 V 0 1 1 0: 2.90 V 0 1 1 1: 2.79 V 1 0 0 0: 2.68 V 1 0 0 1: 2.58 V 1 0 1 0: 2.48 V 1 0 1 1: 2.20 V 1 1 0 0: 1.96 V 1 1 0 1: 1.86 V Settings other than the above are prohibited.	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 0 0 0: 4.29 V 0 0 0 1: 4.16 V 0 0 1 0: 4.03 V 0 0 1 1: 3.86 V 0 1 0 0: 3.10 V 0 1 0 1: 3.00 V 0 1 1 0: 2.90 V 0 1 1 1: 2.80 V 1 0 0 0: 2.68 V 1 0 0 1: 2.59 V 1 0 1 0: 2.48 V 1 0 1 1: 2.20 V 1 1 0 0: 1.96 V 1 1 0 1: 1.86 V Settings other than the above are prohibited.
	LVD2LVL[1:0]	Voltage detection 2 level select bits (Standard voltage during drop in voltage) b5 b4 0 0: 4.29 V 0 1: 4.14 V 1 0: 4.02 V 1 1: 3.84 V	Voltage detection 2 level select bits (Standard voltage during drop in voltage) b5 b4 0 0: 4.32 V 0 1: 4.17 V 1 0: 4.03 V 1 1: 3.84 V

2.5 Clock Generation Circuit

Table 2.5 is a comparative overview of the clock generation circuits, and Table 2.6 is a comparison of clock generation circuit registers.

Table 2.5 Comparative Overview of Clock Generation Circuits

Item	RX130	RX140
Use	• Generates the system clock (ICLK) to be supplied to the CPU, DTC, ROM, and RAM. • Of the peripheral module clocks (PCLKB and PCLKD) supplied to the peripheral modules, PCLKD is the operating clock for the S12AD, and PCLKB is the operating clock for modules other than S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the RTC-dedicated sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the LPT clock (LPTCLK) to be supplied to the LPT. • Generates the REMC clock (REMCLK) to be supplied to the REMC.	• Generates the system clock (ICLK) to be supplied to the CPU, DTC, ROM, and RAM. • Of the peripheral module clocks (PCLKB and PCLKD) supplied to the peripheral modules, PCLKD is the operating clock for the S12AD, and PCLKB is the operating clock for modules other than S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the RTC-dedicated sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT • Generates the LPT clock (LPTCLK) to be supplied to the LPT.
Operating frequency	• ICLK: 32 MHz (max.) • PCLKB: 32 MHz (max.) • PCLKD: 32 MHz (max.) • FCLK: — 1 MHz to 32 MHz (for programming and erasing the ROM and E2 DataFlash) — 32 MHz (max.) (for reading from the E2 DataFlash) • CACCLK: Same as clock from respective oscillators • RTCSCLK: 32.768 kHz • IWDTCLK: 15 kHz • LPTCLK: Same as clock from selected oscillator • REMCLK: Same as clock from respective oscillators	• ICLK: 48 MHz (max.) • PCLKB: 32 MHz (max.) • PCLKD: 48 MHz (max.) • FCLK: — 1 MHz to 48 MHz (for programming and erasing the ROM and E2 DataFlash) — 48 MHz (max.) (for reading from the E2 DataFlash) • CACCLK: Same as clock from respective oscillators • CANMCLK: 20 MHz (max.) • RTCSCLK: 32.768 kHz • IWDTCLK: 15 kHz • LPTCLK: Same as clock from selected oscillator

Item	RX130	RX140
Main clock oscillator	• Resonator frequency: 1 MHz to 20 MHz (VCC ≥ 2.4 V), 1 MHz to 8 MHz (VCC < 2.4 V) • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and MTU pin can be forcedly driven to high-impedance. • Drive capacity switching function	• Resonator frequency: 1 MHz to 20 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and MTU pin can be forcedly driven to high-impedance. • Drive capacity switching function
Sub-clock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal • Connection pins: XCIN and XCOUT • Drive capacity switching function	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal • Connection pins: XCIN and XCOUT • Drive capacity switching function
PLL circuit	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 8 MHz • Frequency multiplication ratio: Selectable from 4 to 8 (increments of 0.5) • Oscillation frequency: 24 MHz to 32 MHz (VCC ≥ 2.4 V)	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 12 MHz • Frequency multiplication ratio: Selectable from 4 to 12 (increments of 0.5) • Oscillation frequency: 24 MHz to 48 MHz
High-speed on-chip oscillator (HOCO)	Oscillation frequency: 32 MHz	Oscillation frequency: 24 MHz, 32 MHz, 48 MHz
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 4 MHz	Oscillation frequency: 4 MHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 15 kHz	Oscillation frequency: 15 kHz

Table 2.6 Comparison of Clock Generation Circuit Registers

Register	Bit	RX130	RX140
PLLCR	STC[5:0]	Frequency multiplication factor select bits b13 b8 0 0 0 1 1 1: ×4 0 0 1 0 0 0: ×4.5 0 0 1 0 0 1: ×5 0 0 1 0 1 0: ×5.5 0 0 1 0 1 1: ×6 0 0 1 1 0 0: ×6.5 0 0 1 1 0 1: ×7 0 0 1 1 1 0: ×7.5 0 0 1 1 1 1: ×8 Settings other than the above are prohibited.	Frequency multiplication factor select bits b13 b8 0 0 0 1 1 1: ×4 0 0 1 0 0 0: ×4.5 0 0 1 0 0 1: ×5 0 0 1 0 1 0: ×5.5 0 0 1 0 1 1: ×6 0 0 1 1 0 0: ×6.5 0 0 1 1 0 1: ×7 0 0 1 1 1 0: ×7.5 0 0 1 1 1 1: ×8 0 1 0 0 0 0: ×8.5 0 1 0 0 0 1: ×9 0 1 0 0 1 0: ×9.5 0 1 0 0 1 1: ×10 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12 Settings other than the above are prohibited.
SOSCCR	SOSTP	Sub-clock oscillator stop bit	Sub-clock oscillator stop bit This bit is not initialized by reset sources other than a power-on reset.
		Initial value after a reset differs.	
HOFCR	—	High-speed on-chip oscillator forced oscillation control register	—

Register	Bit	RX130	RX140
MOSCWTCR	MSTS[4:0]	Main clock oscillator wait time bits b4 b0 0 0 0 0 0: Wait time = 2 cycles (0.5 µs) 0 0 0 0 1: Wait time = 1,024 cycles (256 µs) 0 0 0 1 0: Wait time = 2,048 cycles (512 µs) 0 0 0 1 1: Wait time = 4,096 cycles (1.024 ms) 0 0 1 0 0: Wait time = 8,192 cycles (2.048 ms) 0 0 1 0 1: Wait time = 16,384 cycles (4.096 ms) 0 0 1 1 0: Wait time = 32,768 cycles (8.192 ms) 0 0 1 1 1: Wait time = 65,536 cycles (16.384 ms) Settings other than the above are prohibited. Wait time when LOCO = 4.0 MHz (0.25 µs, typ.)	Main clock oscillator wait time bits b4 b0 0 0 0 0 0: Wait time = 0 cycles (0 µs) 0 0 0 0 1: Wait time = 1,024 cycles (256 µs) 0 0 0 1 0: Wait time = 2,048 cycles (512 µs) 0 0 0 1 1: Wait time = 4,096 cycles (1.024 ms) 0 0 1 0 0: Wait time = 8,192 cycles (2.048 ms) 0 0 1 0 1: Wait time = 16,384 cycles (4.096 ms) 0 0 1 1 0: Wait time = 32,768 cycles (8.192 ms) 0 0 1 1 1: Wait time = 65,536 cycles (16.384 ms) 0 1 0 0 0: Wait time = 131,072 cycles (32.768 ms) Settings other than the above are prohibited. Wait time when LOCO = 4.0 MHz (0.25 µs, typ.)
LOFCR	—	—	Low-speed on-chip oscillator forced oscillation control register
CKOCR	CKOSEL[3:0]	CLKOUT output source select bit b11 b8 0 0 0 0: LOCO clock 0 0 0 1: HOCO clock 0 0 1 0: Main clock 0 0 1 1: Sub-clock 0 1 0 0: PLL Settings other than the above are prohibited.	CLKOUT output source select bit b11 b8 0 0 0 0: LOCO clock 0 0 0 1: HOCO clock 0 0 1 0: Main clock 0 0 1 1: Sub-clock 0 1 0 0: PLL 1 0 0 0: CTSU internal clock Settings other than the above are prohibited.
	CKODIV[2:0]	CLKOUT output division ratio select bits b14 b12 0 0 0: No division 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 Settings other than the above are prohibited.	CLKOUT output division ratio select bits b14 b12 0 0 0: No division 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 1 1 0: ×1/64 1 1 1: ×1/128

Register	Bit	RX130	RX140
MOFCR	MODRV21	Main clock oscillator drive capability switch bit VCC ≥ 2.4 V 0: 1 MHz to 10 MHz 1: 10 MHz to 20 MHz VCC < 2.4 V 0: 1 MHz to 8 MHz 1: Setting prohibited	Main clock oscillator drive capability switch bit 0: 1 MHz to less than 10 MHz 1: 10 MHz to 20 MHz
LOCOTRR (RX130) LOCOTRR2 (RX140)	LOCOTRD [4:0] (RX130) LOCOTRD2 [7:0] (RX140)	Low-speed on-chip oscillator frequency adjustment bits b4 b0 1 0 0 0 0: –16 (frequency: low) 1 0 0 0 1: –15 : : 0 1 1 1 0: 14 0 1 1 1 1: 15 (frequency: high)	Low-speed on-chip oscillator frequency adjustment bits 2 b7 b0 0 0 0 0 0 0 0 0: 0 (frequency: low) 0 0 0 0 0 0 0 1: 1 : : 0 1 1 1 1 1 1 0: 254 1 1 1 1 1 1 1 1: 255 (frequency: high)
SOMCR	—	—	Sub-clock oscillator mode control register

2.6 Low Power Consumption

Table 2.7 is a comparative overview of the low power consumption functions, Table 2.8 is a comparison of procedures for entering and exiting low power consumption modes and operating states in each mode, and Table 2.9 is a comparison of low power consumption registers.

Table 2.7 Comparative Overview of Low Power Consumption Functions

Item	RX130	RX140
Reducing power consumption by switching clock signals	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKB), S12AD clock (PCLKD), and FlashIF clock (FCLK).	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKB), S12AD clock (PCLKD), and FlashIF clock (FCLK).
Module stop function	Each peripheral module can be stopped independently by the module stop control register.	Each peripheral module can be stopped independently by the module stop control register.
Function for transition to low power consumption mode	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.
Low power consumption modes	• Sleep mode • Deep sleep mode • Software standby mode	• Sleep mode • Deep sleep mode • Software standby mode • Snooze mode
Function for lower operating power consumption	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Three operating power control modes are available — High-speed operating mode — Middle-speed operating mode — Low-speed operating mode	• Power consumption can be reduced in normal operation, sleep mode, deep sleep mode, and snooze mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Four operating power control modes are available — High-speed operating mode — Middle-speed operating mode — Middle-speed operating mode 2 — Low-speed operating mode

Table 2.8 Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX130	RX140
Sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM0 (0000 0000h to 0000 BFFFh: RX130, 0000 0000h to 0000 FFFFh: RX140)	Operation possible (retained)	Operation possible (retained)
	DTC	Operation possible	Operation possible
	Flash memory	Operation	Operation
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Remote control signal receiver (REMC)	Operation possible	—
	Realtime clock (RTC)	Operation possible	Operation possible
	Low-power timer (LPT)	Operation possible	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Operation possible	Operation possible
	I/O ports	Operation	Operation
	RTCOUT output	Operation possible	Operation possible
	CLKOUT output	Operation possible	Operation possible
	Comparator B	Operation possible	Operation possible
Deep sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM0 (0000 0000h to 0000 BFFFh: RX130, 0000 0000h to 0000 2FFFh: RX140)	Stopped (retained)	Stopped (retained)
	DTC	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX130	RX140
Deep sleep mode	Remote control signal receiver (REMC)	Operation possible	—
	Realtime clock (RTC)	Operation possible	Operation possible
	Low-power timer (LPT)	Operation possible	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Operation possible	Operation possible
	I/O ports	Operation	Operation
	RTCOUT output	Operation possible	Operation possible
	CLKOUT output	Operation possible	Operation possible
	Comparator B	Operation possible	Operation possible
Software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Stopped	Stopped
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Stopped	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Stopped	Stopped
	CPU	Stopped (retained)	Stopped (retained)
	RAM0 (0000 0000h to 0000 BFFFh: RX130, 0000 0000h to 0000 2FFFh: RX140)	Stopped (retained)	Stopped (retained)
	DTC	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Remote control signal receiver (REMC)	Operation possible	—
	Realtime clock (RTC)	Operation possible	Operation possible
	Low-power timer (LPT)	Operation possible	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained
	RTCOUT output	Operation possible	Operation possible
	CLKOUT output	Operation possible	Operation possible
	Comparator B	Operation possible	Operation possible
Snooze mode	Transition method	—	When snooze transition conditions are met while in software standby mode
	Method of cancellation other than reset	—	Interrupt or occurrence of snooze end condition

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX130	RX140
Snooze mode	State after cancellation	—	Program execution state (interrupt processing) or software standby mode
	Main clock oscillator	—	Operation possible
	Sub-clock oscillator	—	Operation possible
	High-speed on-chip oscillator	—	Operation possible
	Low-speed on-chip oscillator	—	Operation possible
	IWDT-dedicated on-chip oscillator	—	Operation possible
	PLL	—	Operation possible
	CPU	—	Stopped (retained)
	RAM0 (0000 0000h to 0000 BFFFh: RX130, 0000 0000h to 0000 FFFFh: RX140)	—	Operation possible (retained)
	DTC	—	Operation possible
	Flash memory	—	Stopped (retained)
	Independent watchdog timer (IWDT)	—	Operation possible
	Realtime clock (RTC)	—	Operation possible
	Low-power timer (LPT)	—	Operation possible
	Voltage detection circuit (LVD)	—	Operation possible
	Power-on reset circuit	—	Operation
	Peripheral modules	—	Operation possible
	I/O ports	—	Operation
	RTCOUT output	—	Operation possible
	CLKOUT output	—	Operation possible
	Comparator B	—	Operation possible

Note: “Operation possible” means that whether the state is operating or stopped is controlled by the control register setting.
“Stopped (retained)” means that internal register values are retained and internal operations are suspended.
“Stopped (undefined)” means that internal register values are undefined and power is not supplied to the internal circuit.

Table 2.9 Comparison of Low Power Consumption Registers

Register	Bit	RX130	RX140
MSTPCRB	MSTPB0	—	CAN module stop bit
	MSTPB31	Serial communication interface 0 module stop bit	—
MSTPCRC	MSTPC28	Remote control signal receiver 1 module stop bit	—
	MSTPC29	Remote control signal receiver 0 module stop bit	—
MSTPCRD	MSTPD29	—	True random number generator module stop bit
	MSTPD30	—	ASE hardware accelerator module stop bit
OPCCR	OPCM [2:0]	Operating power control mode select bits b2 b0 0 0 0: High-speed operating mode 0 1 0: Middle-speed operating mode Settings other than the above are prohibited.	Operating power control mode select bits b2 b0 0 0 0: High-speed operating mode 0 1 0: Middle-speed operating mode 1 0 0: Middle-speed operating mode 2 Settings other than the above are prohibited.
SNZCR	—	—	Snooze control register
SNZCR2	—	—	Snooze control register 2

2.7 Register Write Protection Function

Table 2.10 is a comparative overview of the register write protection functions.

Table 2.10 Comparative Overview of Register Write Protection Functions

Item	RX130	RX140
PRC0 bit	Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOFCR, OSTDCR, OSTDSR, CKOCR, LOCOTRR, ILOCOTRR, HOCOTRR0	Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, LOFCR, OSTDCR, OSTDSR, CKOCR, LOCOTRR2, ILOCOTRR, HOCOTRR0, SOMCR
PRC1 bit	• Register related to the operating modes: SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, SOPCCR • Registers related to the clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR	• Register related to the operating modes: SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, SOPCCR, SNZCR, SNZCR2 • Registers related to the clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR
PRC2 bit	Registers related to the low power timer: LPTCR1, LPTCR2, LPTCR3, LPTPRD, LPCMR0, LPWUCR	Registers related to the low power timer: LPTCR1, LPTCR2, LPTCR3, LPTPRD, LPCMR0, LPCMR1, LPWUCR
PRC3 bit	Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

2.8 Exception Handling

Table 2.11 is a comparative overview of exception handling, Table 2.12 is a comparative listing of vectors, and Table 2.13 is a comparative listing of instructions for returning from exception handling routines.

Table 2.11 Comparative Overview of Exception Handling

Item	RX130	RX140
Exception events	• Undefined instruction exception • Privileged instruction exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap	• Undefined instruction exception • Privileged instruction exception • Access exception • Floating-point exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap

Table 2.12 Comparative Listing of Vectors

Item		RX130	RX140
Undefined instruction exception		Fixed vector table	Exception vector table (EXTB)
Privileged instruction exception		Fixed vector table	Exception vector table (EXTB)
Access exception		—	Exception vector table (EXTB)
Floating-point exception		—	Exception vector table (EXTB)
Reset		Fixed vector table	Exception vector table (EXTB)
Non-maskable interrupt		Fixed vector table	Exception vector table (EXTB)
Interrupt	Fast interrupt	FINTV	FINTV
	Other than fast interrupt	Relocatable vector table (INTB)	Relocatable vector table (INTB)
Unconditional trap		Relocatable vector table (INTB)	Relocatable vector table (INTB)

Table 2.13 Comparative Listing of Instructions for Returning from Exception Handling Routines

Item		RX130	RX140
Undefined instruction exception		RTE	RTE
Privileged instruction exception		RTE	RTE
Access exception		—	RTE
Floating-point exception		—	RTE
Reset		Return not possible	Return not possible
Non-maskable interrupt		Return not possible	Prohibited
Interrupt	Fast interrupt	RTFI	RTFI
	Other than fast interrupt	RTE	RTE
Unconditional trap		RTE	RTE

2.9 Buses

Table 2.14 is a comparative overview of the buses.

Table 2.14 Comparative Overview of Buses

Bus Type		RX130	RX140
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	Connected to RAM	Connected to RAM
	Memory bus 2	Connected to ROM	Connected to ROM
Internal main buses	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules • Operates in synchronization with the peripheral-module clock (PCLKB, PCLKD)	• Connected to peripheral modules • Operates in synchronization with the peripheral-module clock (PCLKB, PCLKD)
	Internal peripheral bus 3	• Connected to peripheral modules (Touch) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (CTSU, RSCAN) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 6	• Connected to ROM (P/E) and E2 DataFlash • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to ROM (P/E) and E2 DataFlash • Operates in synchronization with the FlashIF clock (FCLK)

2.10 Data Transfer Controller

Table 2.15 is a comparative overview of the data transfer controllers, and Table 2.16 is a comparison of data transfer controller registers.

Table 2.15 Comparative Overview of Data Transfer Controllers

Item	RX130 (DTCa)	RX140 (DTCb)
Number of transfer channels	Equal to number of all interrupt sources that can start a DTC transfer.	Equal to number of all interrupt sources that can start a DTC transfer.
Transfer modes	• Normal transfer mode — A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address returns to the transfer start address when the number of data transfers equals the repeat size. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, or 1,024 bytes. • Block transfer mode — A single activation leads to the transfer of a single block of data. — The maximum block size is 256 × 32 bits = 1,024 bytes.	• Normal transfer mode — A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address returns to the transfer start address when the number of data transfers equals the repeat size. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, or 1,024 bytes. • Block transfer mode — A single activation leads to the transfer of a single block of data. — The maximum block size is 256 × 32 bits = 1,024 bytes.
Chain transfer function	• Multiple data transfer types can be executed sequentially in response to a single transfer request. • Either “performed only when the transfer counter reaches 0” or “every time” can be selected.	• Multiple data transfer types can be executed sequentially in response to a single transfer request. • Either “performed only when the transfer counter reaches 0” or “every time” can be selected.
Sequence transfer	—	A complex series of transfers can be registered as a sequence. Any sequence can be selected by the transfer data and executed. • Only one sequence transfer trigger source can be selected at a time. • Up to 256 sequences can correspond to a single trigger source. • The data that is initially transferred in response to a transfer request determines the sequence. • The entire sequence can be executed on a single request, or the sequence can be suspended in the middle and resumed on the next transfer request (sequence division).

Item	RX130 (DTCa)	RX140 (DTCb)
Transfer space	• 16 MB in short-address mode (within 0000 0000h to 007F FFFFh or FF80 0000h to FFFF FFFFh, excluding reserved areas) • 4 GB in full-address mode (within 0000 0000h to FFFF FFFFh, excluding reserved areas)	• 16 MB in short-address mode (within 0000 0000h to 007F FFFFh or FF80 0000h to FFFF FFFFh, excluding reserved areas) • 4 GB in full-address mode (within 0000 0000h to FFFF FFFFh, excluding reserved areas)
Data transfer units	• Single data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data units	• Single data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data units
CPU interrupt requests	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.
Event link function	An event link request is generated after one data transfer (for block transfers, after one block).	An event link request is generated after one data transfer (for block transfers, after one block).
Read skip	Reading of the transfer information can be skipped when the same transfer is repeated.	Reading of the transfer information can be skipped when the same transfer is repeated.
Write-back skip	Write-back of transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.	Write-back of transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.
Write-back disable	—	Ability to disable write-back of transfer information
Displacement addition	—	Ability to add displacement to the transfer source address (selectable by each transfer information)
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Table 2.16 Comparison of Data Transfer Controller Registers

Register	Bit	RX130 (DTCa)	RX140 (DTCb)
MRA	WBDIS	—	Write-back disable bit*1
MRB	SQEND	—	Sequence transfer end bit
	INDX	—	Index table reference bit
MRC	—	—	DTC mode register C
DTCIBR	—	—	DTC index table base register
DTCOR	—	—	DTC operation register
DTCSQE	—	—	DTC sequence transfer enable register
DTCDISP	—	—	DTC address displacement register

Note: 1. Transfer information is usually allocated to a RAM area, but it can be allocated to a ROM area by setting the MRA.WBDIS bit to 1 (no write-back).

2.11 Event Link Controller

Table 2.17 is a comparative overview of the event link controllers, and Table 2.18 shows correspondences between values set in ELSRn.ELS[7:0] and event signal names and numbers.

Table 2.17 Comparative Overview of Event Link Controllers

Item	RX130 (ELC)	RX140 (ELC)
Event link function	• 47 event signals can be directly connected to modules. • Operation of timer modules while inputting an event signal can be selected. • Event linkage operation is possible on port B. — Single port: Event link operation can be enabled on a single port corresponding to the specified bit. — Port group: Among the eight I/O ports, event link operation can be enabled for a group of ports corresponding to multiple specified bits.	• 48 event signals can be directly connected to modules. • Operation of timer modules while inputting an event signal can be selected. • Event linkage operation is possible on port B. — Single port: Event link operation can be specified on a single port corresponding to the specified bit. — Port group: Among the eight I/O ports, event link operation can be enabled for a group of ports corresponding to multiple specified bits.
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Table 2.18 Correspondence between Values Set in ELSRn.ELS[7:0] Bits and Event Signal Names and Numbers

Value of ELS[7:0] Bits	Peripheral Module	RX130 (ELC)	RX140 (ELC)
08h	Multi-function timer pulse unit 2	MTU1 compare match 1A	MTU1 compare match 1A
09h		MTU1 compare match 1B	MTU1 compare match 1B
0Ah		MTU1 overflow signal	MTU1 overflow signal
0Bh		MTU1 underflow signal	MTU1 underflow signal
0Ch		MTU2 compare match 2A	MTU2 compare match 2A
0Dh		MTU2 compare match 2B	MTU2 compare match 2B
0Eh		MTU2 overflow signal	MTU2 overflow signal
0Fh		MTU2 underflow signal	MTU2 underflow signal
10h		MTU3 compare match 3A	MTU3 compare match 3A
11h		MTU3 compare match 3B	MTU3 compare match 3B
12h		MTU3 compare match 3C	MTU3 compare match 3C
13h		MTU3 compare match 3D	MTU3 compare match 3D
14h		MTU3 overflow signal	MTU3 overflow signal
15h		MTU4 compare match 4A	MTU4 compare match 4A
16h		MTU4 compare match 4B	MTU4 compare match 4B
17h		MTU4 compare match 4C	MTU4 compare match 4C
18h		MTU4 compare match 4D	MTU4 compare match 4D
19h		MTU4 overflow signal	MTU4 overflow signal
1Ah		MTU4 underflow signal	MTU4 underflow signal

Value of ELS[7:0] Bits	Peripheral Module	RX130 (ELC)	RX140 (ELC)
1Fh	Compare match timer	CMT1 compare match 1	CMT1 compare match 1
22h	8-bit timer	TMR0 compare match A0	TMR0 compare match A0
23h		TMR0 compare match B0	TMR0 compare match B0
24h		TMR0 overflow signal	TMR0 overflow signal
28h		TMR2 compare match A2	TMR2 compare match A2
29h		TMR2 compare match B2	TMR2 compare match B2
2Ah		TMR2 overflow signal	TMR2 overflow signal
32h	Low-power timer	LPT compare match	LPT compare match 0
33h		—	LPT compare match 1
34h	12-bit A/D converter	S12AD compare condition satisfied	S12AD compare condition satisfied
35h		S12AD compare condition not satisfied	S12AD compare condition not satisfied
3Ah	Serial communications interface	SCI5 error (receive error or error signal detection)	SCI5 error (receive error or error signal detection)
3Bh		SCI5 receive data full signal	SCI5 receive data full signal
3Ch		SCI5 transmit data empty signal	SCI5 transmit data empty signal
3Dh		SCI5 transmit end signal	SCI5 transmit end signal
4Eh	I^2C bus interface	RIIC0 communication error or event generation signal	RIIC0 communication error or event generation signal
4Fh		RIIC0 receive data full signal	RIIC0 receive data full signal
50h		RIIC0 transmit data empty signal	RIIC0 transmit data empty signal
51h		RIIC0 transmit end signal	RIIC0 transmit end signal
58h	12-bit A/D converter	S12AD A/D conversion end	S12AD A/D conversion end
59h	Comparator B0	Comparator B0 comparison result change signal	Comparator B0 comparison result change signal
5Ah	Comparator B0 and B1	Comparator B0 and B1 common comparison result change signal	Comparator B0 and B1 common comparison result change signal
5Bh	Voltage detection circuit	LVD1 voltage detection signal	LVD1 voltage detection signal
61h	Data transfer controller	DTC transfer end	DTC transfer end
63h	I/O ports	Input edge detection signal of input port group 1	Input edge detection signal of input port group 1
65h		Input edge detection signal of single input port 0	Input edge detection signal of single input port 0
66h		Input edge detection signal of single input port 1	Input edge detection signal of single input port 1
69h	Event link controller	Software event signal	Software event signal
6Ah	Data operation circuit	DOC data operation condition met	DOC data operation condition met
Settings other than the above are prohibited.			

2.12 I/O Ports

Table 2.19 to Table 2.21 are comparative overviews of the I/O ports, Table 2.22 is a comparison of I/O port functions, and Table 2.23 is a comparison of I/O port registers.

Table 2.19 Comparative Overview of I/O Ports (80-Pin)

Port Symbol	RX130 (80-Pin)	RX140 (80-Pin)
PORT0	P03 to P07	P03 to P07
PORT1	P12 to P17	P12 to P17
PORT2	P20, P21, P26, P27	P20, P21, P26, P27
PORT3	P30 to P32, P34 to P37	P30 to P32, P34 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P54, P55	P54, P55
PORTA	PA0 to PA6	PA0 to PA6
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD2	PD0 to PD2
PORTE	PE0 to PE5	PE0 to PE5
PORTG	—	PG7
PORTH	PH0 to PH3	PH0 to PH3, PH6, PH7
PORTJ	PJ1, PJ6, PJ7	PJ1, PJ6, PJ7

Table 2.20 Comparative Overview of I/O Ports (64-Pin)

Port Symbol	RX130 (64-Pin)	RX140 (64-Pin)
PORT0	P03, P05	P03, P05
PORT1	P14 to P17	P14 to P17
PORT2	P26, P27	P26, P27
PORT3	P30 to P32, P35 to P37	P30 to P32, P35 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P54, P55	P54, P55
PORTA	PA0, PA1, PA3, PA4, PA6	PA0, PA1, PA3, PA4, PA6
PORTB	PB0, PB1, PB3, PB5 to PB7	PB0, PB1, PB3, PB5 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTE	PE0 to PE5	PE0 to PE5
PORTG	—	PG7
PORTH	PH0 to PH3	PH0 to PH3, PH6*1, PH7*1
PORTJ	PJ6, PJ7	PJ6, PJ7

Note: 1. A product with a ROM capacity of 64 KB is not equipped with this pin.

Table 2.21 Comparative Overview of I/O Ports (48-Pin)

Port Symbol	RX130 (48-Pin)	RX140 (48-Pin)
PORT1	P14 to P17	P14 to P17
PORT2	P26, P27	P26, P27
PORT3	P30, P31, P35 to P37	P30, P31, P35 to P37
PORT4	P40 to P42, P45 to P47	P40 to P42, P45 to P47
PORTA	PA1, PA3, PA4, PA6	PA1, PA3, PA4, PA6
PORTB	PB0, PB1, PB3, PB5	PB0, PB1, PB3, PB5
PORTC	PC0 to PC7	PC0 to PC7
PORTE	PE1 to PE4	PE1 to PE4
PORTG	—	PG7
PORTH	PH0 to PH3	PH0 to PH3
PORTJ	PJ6, PJ7	PJ6, PJ7

Table 2.22 Comparison of I/O Port Functions

Item	Port Symbol	RX130	RX140
Input pull-up function	PORT0	P03 to P07	P03 to P07
	PORT1	P12 to P17	P12 to P17
	PORT2	P20 to P27	P20, P21, P26, P27
	PORT3	P30 to P34, P36, P37	P30 to P32, P34, P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P55	P54, P55
	PORTA	PA0 to PA7	PA0 to PA6
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC2 to PC7
	PORTD	PD0 to PD7	PD0 to PD2
	PORTE	PE0 to PE7	PE0 to PE3, PE4, PE5
	PORTG	—	PG7
	PORTH	PH0 to PH3	PH0 to PH3
	PORTJ	PJ1, PJ3, PJ6, PJ7	PJ1, PJ6, PJ7
Open drain output function	PORT1	P12 to P17	P12 to P17
	PORT2	P20, P21 to P23, P26, P27	P20, P21, P26, P27
	PORT3	P30 to P34, P36, P37	P30 to P32, P34, P36, P37
	PORTA	PA0 to PA7	PA0 to PA6
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC2 to PC7
	PORTD	PD0 to PD2	PD0 to PD2
	PORTE	PE0 to PE3	PE0 to PE3
	PORTG	—	PG7
	PORTJ	PJ3	—

Item	Port Symbol	RX130	RX140
Drive capacity switching function	PORT0	P03 to P07	—
	PORT1	P12 to P17	—
	PORT2	P20 to P27	—
	PORT3	P30 to P34, P36, P37	—
	PORT4	P40 to P47	—
	PORT5	P50 to P55	—
	PORTA	PA0 to PA7	—
	PORTB	PB0 to PB7	—
	PORTC	PC0 to PC7	—
	PORTD	PD0 to PD7	—
	PORTE	PE0 to PE7	—
	PORTH	PH0 to PH3	—
	PORTJ	PJ1, PJ3, PJ6, PJ7	—
5 V tolerant	PORT1	P12, P13, P16, P17	P12, P13, P16, P17

Table 2.23 Comparison of I/O Port Registers

Register	Bit	RX130	RX140
PDR	B0 to B7	Pm0 to Pm7 I/O select bits (m = 0 to 5, A to E, H, J)	Pm0 to Pm7 I/O select bits (m = 0 to 5, A to E, G, H, J)
PODR	B0 to B7	Pm0 to Pm7 output data store bits (m = 0 to 5, A to E, H, J)	Pm0 to Pm7 output data store bits (m = 0 to 5, A to E, G, H, J)
PIDR	B0 to B7	Pm0 to Pm7 bits (m = 0 to 5, A to E, H, J)	Pm0 to Pm7 bits (m = 0 to 5, A to E, G, H, J)
PMR	B0 to B7	Pm0 pin mode control bits (m = 0 to 5, A to E, H, J) 0: Use pin as general I/O port. 1: Use pin as I/O port for peripheral function.	Pm0 to Pm7 pin mode control bits (m = 0 to 5, A to E, G, H, J) 0: Use pin as general I/O port. 1: Use pin as I/O port for peripheral function. PG7 only 0: Use pin as general I/O port. 1: Use pin as I/O port for MD function (initial value).
ODR1	B0, B2, B4, B6	Pm4, Pm5, Pm6, and Pm7 output type select bits (m = 1 to 3, A to C)	Pm4, Pm5, Pm6, and Pm7 output type select bits (m =1 to 3, A to C, G)
PCR	B0 to B7	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 5, A to E, H, J)	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 5, A to E, G, H, J)
DSCR	—	Drive capacity control register	—
PRWCNTR	—	—	Port read wait control register

2.13 Multi-Function Pin Controller

Table 2.24 is a comparison of the assignments of multiplexed pins, and Table 2.25 to Table 2.35 are comparisons of multi-function pin controller registers.

In the following comparison of the assignments of multiplexed pins, **blue text** designates pins that exist on the RX140 Group only. A circle (○) indicates that a function is assigned, a cross (×) that the pin does not exist or that no function is assigned, and grayed out items mean that the function is not implemented.

Table 2.24 Comparison of Multiplexed Pin Assignments

Module/ Function	Pin Function	Port Allocation	RX130			RX140		
			80 -Pin	64 -Pin	48 -Pin	80 -Pin	64 -Pin	48 -Pin
Interrupt	NMI (input)	P35	○	○	○	○	○	○
	IRQ0 (input)	P30	○	○	○	○	○	○
		PD0	○	×	×	○	×	×
		PH1	○	○	○	○	○	○
	IRQ1 (input)	P31	○	○	○	○	○	○
		PD1	○	×	×	○	×	×
		PH2	○	○	○	○	○	○
	IRQ2 (input)	P32	○	○	×	○	○	×
		P12	○	×	×	○	×	×
		PD2	○	×	×	○	×	×
		P36	×	×	×	○	○	○
	IRQ3 (input)	P13	○	×	×	○	×	×
	IRQ4 (input)	PB1	○	○	○	○	○	○
		P14	○	○	○	○	○	○
		P34	○	×	×	○	×	×
		P37	×	×	×	○	○	○
	IRQ5 (input)	PA4	○	○	○	○	○	○
		P15	○	○	○	○	○	○
		PE5	○	○	×	○	○	×
	IRQ6 (input)	PA3	○	○	○	○	○	○
		P16	○	○	○	○	○	○
	IRQ7 (input)	PE2	○	○	○	○	○	○
		P17	○	○	○	○	○	○
Clock generation circuit	CLKOUT (output)	PE3	○	○	○	○	○	○
		PE4	○	○	○	○	○	○
Multi-function timer unit 2	MTIOC0A (input/output)	P34	○	×	×	○	×	×
		PB3	○	○	○	○	○	○
		PC4	×	×	×	○	○	○
	MTIOC0B (input/output)	P13	○	×	×	○	×	×
		P15	○	○	○	○	○	○
		PA1	○	○	○	○	○	○
	MTIOC0C (input/output)	P32	○	○	×	○	○	×
		PB1	○	○	○	○	○	○
		PC5	×	×	×	○	○	○
	MTIOC0D (input/output)	PA3	○	○	○	○	○	○
	MTIOC1A (input/output)	P20	○	×	×	○	×	×
		PE4	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX130			RX140		
			80 -Pin	64 -Pin	48 -Pin	80 -Pin	64 -Pin	48 -Pin
Multi-function timer unit 2	MTIOC1B (input/output)	P21	○	×	×	○	×	×
		PB5	○	○	○	○	○	○
		PE3	×	×	×	○	○	○
	MTIOC2A (input/output)	P26	○	○	○	○	○	○
		PB5	○	○	○	○	○	○
	MTIOC2B (input/output)	P27	○	○	○	○	○	○
		PE5	○	○	×	○	○	×
	MTIOC3A (input/output)	P14	○	○	○	○	○	○
		P17	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
		PJ1	○	×	×	○	×	×
	MTIOC3B (input/output)	P17	○	○	○	○	○	○
		PB7	○	○	×	○	○	×
		PC5	○	○	○	○	○	○
		PA1	×	×	×	○	○	○
		PH0	×	×	×	○	○	○
	MTIOC3C (input/output)	P16	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	MTIOC3D (input/output)	P16	○	○	○	○	○	○
		PB6	○	○	×	○	○	×
		PC4	○	○	○	○	○	○
		PA6	×	×	×	○	○	○
		PB0	×	×	×	○	○	○
		PH1	×	×	×	○	○	○
	MTIOC4A (input/output)	PA0	○	○	×	○	○	×
		PB3	○	○	○	○	○	○
		PE2	○	○	○	○	○	○
		P55	×	×	×	○	○	×
		PE4	×	×	×	○	○	○
	MTIOC4B (input/output)	P30	○	○	○	○	○	○
		P54	○	○	×	○	○	×
		PC2	○	○	×	○	○	×
		PD1	○	×	×	○	×	×
		PE3	○	○	○	○	○	○
	MTIOC4C (input/output)	PB1	○	○	○	○	○	○
		PE1	○	○	○	○	○	○
		PE5	○	○	×	○	○	×
		PA4	×	×	×	○	○	○
		PH2	×	×	×	○	○	○
	MTIOC4D (input/output)	P31	○	○	○	○	○	○
		P55	○	○	×	○	○	×
		PC3	○	○	×	○	○	×
		PD2	○	×	×	○	×	×
		PE4	○	○	○	○	○	○
		PA3	×	×	×	○	○	○
		PH3	×	×	×	○	○	○
	MTIC5U (input)	PA4	○	○	○	○	○	○
	MTIC5V (input)	PA6	○	○	○	○	○	○
		PA3	×	×	×	○	○	○

Module/ Function	Pin Function	Port Allocation	RX130			RX140		
			80 -Pin	64 -Pin	48 -Pin	80 -Pin	64 -Pin	48 -Pin
Multi-function timer unit 2	MTIC5W (input)	PB0	○	○	○	○	○	○
	MTCLKA (input)	P14	○	○	○	○	○	○
		PA4	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	MTCLKB (input)	P15	○	○	○	○	○	○
		PA6	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	MTCLKC (input)	PA1	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	MTCLKD (input)	PA3	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
Port output enable 2	POE0# (input)	PC4	○	○	○	○	○	○
	POE1# (input)	PB5	○	○	○	○	○	○
	POE2# (input)	P34	○	×	×	○	×	×
		PA6	○	○	○	○	○	○
	POE3# (input)	PB3	○	○	○	○	○	○
	POE8# (input)	P17	○	○	○	○	○	○
		P30	○	○	○	○	○	○
		PE3	○	○	○	○	○	○
8-bit timer	TMO0 (output)	PB3	○	○	○	○	○	○
		PH1	○	○	○	○	○	○
	TMCI0 (input)	P21	○	×	×	○	×	×
		PB1	○	○	○	○	○	○
		PH3	○	○	○	○	○	○
	TMRI0 (input)	P20	○	×	×	○	×	×
		PA4	○	○	○	○	○	○
		PH2	○	○	○	○	○	○
	TMO1 (output)	P17	○	○	○	○	○	○
		P26	○	○	○	○	○	○
	TMCI1 (input)	P12	○	×	×	○	×	×
		P54	○	○	×	○	○	×
		PC4	○	○	○	○	○	○
	TMRI1 (input)	PB5	○	○	○	○	○	○
	TMO2 (output)	P16	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	TMCI2 (input)	P15	○	○	○	○	○	○
		P31	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	TMRI2 (input)	P14	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
	TMO3 (output)	P13	○	×	×	○	×	×
		P32	○	○	×	○	○	×
		P55	○	○	×	○	○	×
	TMCI3 (input)	P27	○	○	○	○	○	○
		P34	○	×	×	○	×	×
		PA6	○	○	○	○	○	○
	TMRI3 (input)	P30	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX130			RX140		
			80 -Pin	64 -Pin	48 -Pin	80 -Pin	64 -Pin	48 -Pin
Serial communications interface	RXD1 (input) / SMISO1 (input/output) / SSCL1 (input/output)	P15	○	○	○	○	○	○
		P30	○	○	○	○	○	○
	TXD1 (output) / SMOSI1 (input/output) / SSDA1 (input/output)	P16	○	○	○	○	○	○
		P26	○	○	○	○	○	○
	SCK1 (input/output)	P17	○	○	○	○	○	○
		P27	○	○	○	○	○	○
	CTS1# (input) / RTS1# (output) / SS1# (input)	P14	○	○	○	○	○	○
		P31	○	○	○	○	○	○
	RXD5 (input) / SMISO5 (input/output) / SSCL5 (input/output)	PA2	○	×	×	○	×	×
		PA3	○	○	○	○	○	○
		PC2	○	○	×	○	○	×
	TXD5 (output) / SMOSI5 (input/output) / SSDA5 (input/output)	PA4	○	○	○	○	○	○
		PC3	○	○	×	○	○	×
	SCK5 (input/output)	PA1	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	CTS5# (input) / RTS5# (output) / SS5# (input)	PA6	○	○	○	○	○	○
	RXD6 (input) / SMISO6 (input/output) / SSCL6 (input/output)	PB0	○	○	○	○	○*1	○*1
		PD1	○	×	×	○	×	×
	TXD6 (output) / SMOSI6 (input/output) / SSDA6 (input/output)	PB1	○	○	○	○	○*1	○*1
		PD0	○	×	×	○	×	×
		P32	○	○	×	○	○*1	×
	SCK6 (input/output)	P34	○	×	×	○	×	×
		PB3	○	○	○	○	○*1	○*1
		PD2	○	×	×	○	×	×
	CTS6# (input) / RTS6# (output) / SS6# (input)	PB2	○	×	×	○	×	×
	RXD8 (input) / SMISO8 (input/output) / SSCL8 (input/output)	PC6	×	×	×	○	○*1	○*1
	TXD8 (output) / SMOSI8 (input/output) / SSDA8 (input/output)	PC7	×	×	×	○	○*1	○*1
	SCK8 (input/output)	PC5	×	×	×	○	○*1	○*1
	CTS8# (input) / RTS8# (output) / SS8# (input)	PC4	×	×	×	○	○*1	○*1
	RXD9 (input) / SMISO9 (input/output) / SSCL9 (input/output)	PB6	×	×	×	○	○*1	×

Module/ Function	Pin Function	Port Allocation	RX130			RX140		
			80 -Pin	64 -Pin	48 -Pin	80 -Pin	64 -Pin	48 -Pin
Serial communications interface	TXD9 (output) / SMOSI9 (input/output) / SSDA9 (input/output)	PB7	×	×	×	○	○*1	×
	SCK9 (input/output)	PB5	×	×	×	○	○*1	×
	CTS9# (input) / RTS9# (output) / SS9# (input)	PB4	×	×	×	○	×	×
	RXD12 (input) / SMISO12 (input/output) / SSCL12 (input/output) / RXDX12 (input)	PE2	○	○	○*2	○	○	○*2
	TXD12 (output) / SMOSI12 (input/output) / SSDA12 (input/output) / TXDX12 (output) / SIOX12 (input/output)	PE1	○	○	○*2	○	○	○*2
	SCK12 (input/output)	PE0	○	○	×	○	○	×
	CTS12# (input) / RTS12# (output) / SS12# (input)	PE3	○	○	○*3	○	○	○*3
I^2C bus interface	SCL (input/output)	P16	○	○	○	○	○	○
		P12	○	×	×	○	×	×
	SDA (input/output)	P17	○	○	○	○	○	○
		P13	○	×	×	○	×	×
Serial peripheral interface	RSPCKA (input/output)	PA5	○	×	×	○	×	×
		PB0	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
	MOSIA (input/output)	P16	○	○	○	○	○	○
		PA6	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	MISOA (input/output)	P17	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	SSLA0 (input/output)	PA4	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	SSLA1 (output)	PA0	○	○	×	○	○	×
	SSLA2 (output)	PA1	○	○	○	○	○	○
	SSLA3 (output)	PA2	○	×	×	○	×	×
		PC2	○	○	×	○	○	×
Realtime clock	RTCOUT (output)	P16	○	○	×	○	○	○
		P32	○	○	×	○	○	×
12-bit A/D converter	AN000 (input)*4	P40	○	○	○	○	○	○
	AN001 (input)*4	P41	○	○	○	○	○	○
	AN002 (input)*4	P42	○	○	○	○	○	○
	AN003 (input)*4	P43	○	○	×	○	○	×
	AN004 (input)*4	P44	○	○	×	○	○	×
	AN005 (input)*4	P45	○	○	○	○	○	○
	AN006 (input)*4	P46	○	○	○	○	○	○
	AN007 (input)*4	P47	○	○	○	○	○	○
	AN016 (input)*4	PE0	○	○	×	○	○	×

Module/ Function	Pin Function	Port Allocation	RX130			RX140		
			80 -Pin	64 -Pin	48 -Pin	80 -Pin	64 -Pin	48 -Pin
12-bit A/D converter	AN017 (input)*4	PE1	○	○	○	○	○	○
	AN018 (input)*4	PE2	○	○	○	○	○	○
	AN019 (input)*4	PE3	○	○	○	○	○	○
	AN020 (input)*4	PE4	○	○	○	○	○	○
	AN021 (input)*4	PE5	○	○	×	○	○	×
	AN024 (input)*4	PD0	○	×	×	○	×	×
	AN025 (input)*4	PD1	○	×	×	○	×	×
	AN026 (input)*4	PD2	○	×	×	○	×	×
	ADTRG0# (input)	P07	○	×	×	○	×	×
		P16	○	○	○	○	○	○
D/A converter	DA0 (output)*4	P03	○	○	×	○	○	×
	DA1 (output)*4	P05	○	○	×	○	○	×
Clock frequency accuracy measurement circuit	CACREF (input)	PA0	○	○	×	○	○	×
		PC7	○	○	○	○	○	○
		PH0	○	○	○	○	○	○
LVD voltage detection input	CMPA2 (input)*4	PE4	○	○	○	○	○	○
Comparator B	CMPB0 (input)*4	PE1	○	○	○	○	○	○
	CVREFB0 (input)*4	PE2	○	○	○	○	○	○
	CMPOB0 (output)	PE5	○	○	×	○	○	×
	CMPB1 (input)*4	PA3	○	○	○	○	○	○
	CVREFB1 (input)*4	PA4	○	○	○	○	○	○
	CMPOB1 (output)	PB1	○	○	○	○	○	○
Capacitive Touch Sensing Unit (CTSU)	TSCAP (—)	PC4	○	○	○	○	○	○
	TS0 (input/output)	P32	○	○	×	○	○*1	×
	TS1 (input/output)	P31	○	○	○	○	○*1	○*1
	TS2 (input/output)	P30	○	○	○	○	○*1	○*1
	TS3 (input/output)	P27	○	○	○	○	○	○
	TS4 (input/output)	P26	○	○	○	○	○	○
	TS5 (input/output)	P15	○	○	○	○	○*1	○*1
	TS6 (input/output)	P14	○	○	○	○	○*1	○*1
	TS7 (input/output)	PH3	○	○	○	○	○*1	○*1
	TS8 (input/output)	PH2	○	○	○	○	○*1	○*1
	TS9 (input/output)	PH1	○	○	○	○	○*1	○*1
	TS10 (input/output)	PH0	○	○	○	○	○*1	○*1
	TS11 (input/output)	P55	○	○	×	○	○*1	×
	TS12 (input/output)	P54	○	○	×	○	○*1	×
	TS13 (input/output)	PC7	○	○	○	○	○	○
	TS14 (input/output)	PC6	○	○	○	○	○	○
	TS15 (input/output)	PC5	○	○	○	○	○	○
	TS16 (input/output)	PC3	○	○	×	○	○*1	×
	TS17 (input/output)	PC2	○	○	×	○	○*1	×
	TS18 (input/output)	PB7	○	○	×	○	○*1	×
	TS19 (input/output)	PB6	○	○	×	○	○*1	×
	TS20 (input/output)	PB5	○	○	○	○	○*1	○*1
	TS21 (input/output)	PB4	○	×	×	○	×	×
	TS22 (input/output)	PB3	○	○	○	○	○*1	○*1
	TS23 (input/output)	PB2	○	×	×	○	×	×

Module/ Function	Pin Function	Port Allocation	RX130			RX140		
			80 -Pin	64 -Pin	48 -Pin	80 -Pin	64 -Pin	48 -Pin
Capacitive Touch Sensing Unit (CTSU)	TS24 (input/output)	PB1	○	○	○	○	○ *1	○ *1
	TS25 (input/output)	PB0	○	○	○	○	○	○
	TS26 (input/output)	PA6	○	○	○	○	○ *1	○ *1
	TS27 (input/output)	PA5	○	×	×	○	×	×
	TS28 (input/output)	PA4	○	○	○	○	○	○
	TS29 (input/output)	PA3	○	○	○	○	○	○
	TS30 (input/output)	PA2	○	×	×	○	×	×
	TS31 (input/output)	PA1	○	○	○	○	○	○
	TS32 (input/output)	PA0	○	○	×	○	○ *1	×
	TS33 (input/output)	PE4	○	○	○	○	○	○
	TS34 (input/output)	PE3	○	○	○	○	○	○
	TS35 (input/output)	PE2	○	○	○	○	○	○
Low-power timer	LPTO (output)	P26				○	○	○
		PB3				○	○	○
		PC7				○	○	○
CAN module	CTXD0 (output)	P14				○	○ *1	○ *1
		P54				○	○ *1	×
	CRXD0 (input)	P15				○	○ *1	○ *1
		P55				○	○ *1	×

Notes: 1. This function is not implemented on RX140 Group products with ROM capacity of 64 KB.
2. The SMISO12 function is not implemented on 48-pin package products.
3. The SS12# function is not implemented on 48-pin package products.
4. To use these pin functions, set the relevant pins as general I/O ports (PORT.PDR.Bm and PORT.PMR.Bm bits both cleared to 0).

Table 2.25 Comparison of P1n Pin Function Control Register (P1nPFS)

Register	Bit	RX130 (n = 2 to 7)	RX140 (n = 2 to 7)
P14PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKA 00101b: TMRI2 01011b: CTS1#/RTS1#/SS1# 11001b: TS6	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKA 00101b: TMRI2 01011b: CTS1#/RTS1#/SS1# 11001b: TS6 11100b: CTXD0
P15PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKB 00101b: TMCI2 01010b: RXD1/SMISO1/SSCL1 11001b: TS5	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKB 00101b: TMCI2 01010b: RXD1/SMISO1/SSCL1 11001b: TS5 11100b: CRXD0

Table 2.26 Comparison of P2n Pin Function Control Register (P2nPFS)

Register	Bit	RX130 (n = 0 to 7)	RX140 (n = 0, 1, 6, 7)
P20PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC1A 00101b: TMRI0 01010b: TXD0/SMOSI0/SSDA0	Pin function select bits 00000b: Hi-Z 00001b: MTIOC1A 00101b: TMRI0
P21PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC1B 00101b: TMCI0 01010b: RXD0/SMISO0/SSCL0	Pin function select bits 00000b: Hi-Z 00001b: MTIOC1B 00101b: TMCI0
P22PFS	—	P22 pin function control register	—
P23PFS	—	P23 pin function control register	—
P24PFS	—	P24 pin function control register	—
P25PFS	—	P25 pin function control register	—
P26PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC2A 00101b: TMO1 01010b: TXD1/SMOSI1/SSDA1 11001b: TS4	Pin function select bits 00000b: Hi-Z 00001b: MTIOC2A 00101b: TMO1 01010b: TXD1/SMOSI1/SSDA 11001b: TS4 11011b: LPTO

Table 2.27 Comparison of P3n Pin Function Control Register (P3nPFS)

Register	Bit	RX130 (n = 0 to 4)	RX140 (n = 0 to 2, 4, 6, 7)
P33PFS	—	P33 pin function control register	—
P36PFS	—	—	P36 pin function control register
P37PFS	—	—	P37 pin function control register
P3nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0 (100/80/64/48-pin) P31: IRQ1 (100/80/64/48-pin) P32: IRQ2 (100/80/64-pin) P33: IRQ3 (100-pin) P34: IRQ4 (100/80-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0 (80/64/48/32-pin) P31: IRQ1 (80/64/48/32-pin) P32: IRQ2 (80/64-pin) P34: IRQ4 (80-pin) P36: IRQ2 (80/64/48/32-pin) P37: IRQ4 (80/64/48-pin)

Table 2.28 Comparison of P5n Pin Function Control Register (P5nPFS)

Register	Bit	RX130 (n = 1, 2, 4, 5)	RX140 (n = 4, 5)
P51PFS	—	P51 pin function control register	—
P52PFS	—	P52 pin function control register	—
P54PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 00101b: TMCI1 11001b: TS12	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 00101b: TMCI1 11001b: TS12 11100b: CTXD0
P55PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 00101b: TMO3 11001b: TS11	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 00101b: TMO3 11001b: TS11 11100b: CRXT0

Table 2.29 Comparison of PAn Pin Function Control Register (PAnPFS)

Register	Bit	RX130 (n = 0 to 7)	RX140 (n = 0 to 6)
PA1PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKC 01010b: SCK5 01101b: SSLA2 11001b: TS31	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKC 00011b: MTIOC3B 01010b: SCK5 01101b: SSLA2 11001b: TS31
PA3PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0D 00010b: MTCLKD 01010b: RXD5/SMISO5/SSCL5 11001b: TS29	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0D 00010b: MTCLKD 00011b: MTIOC4D 00100b: MTIC5V 01010b: RXD5/SMISO5/SSCL5 11001b: TS29
PA4PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIC5U 00010b: MTCLKA 00101b: TMRI0 01010b: TXD5/SMOSI5/SSDA5 01101b: SSLA0 11001b: TS28	Pin function select bits 00000b: Hi-Z 00001b: MTIC5U 00010b: MTCLKA 00011b: MTIOC4C 00101b: TMRI0 01010b: TXD5/SMOSI5/SSDA5 01101b: SSLA0 11001b: TS28
PA6PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIC5V 00010b: MTCLKB 00101b: TMCI3 00111b: POE2# 01011b: CTS5#/RTS5#/SS5# 01101b: MOSIA 11001b: TS26	Pin function select bits 00000b: Hi-Z 00001b: MTIC5V 00010b: MTCLKB 00011b: MTIOC3D 00101b: TMCI3 00111b: POE2# 01011b: CTS5#/RTS5#/SS5# 01101b: MOSIA 11001b: TS26
PA7PFS	—	PA7 pin function control register	—

Table 2.30 Comparison of PBn Pin Function Control Register (PBnPFS)

Register	Bit	RX130 (n = 0 to 7)	RX140 (n = 0 to 7)
PB0PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIC5W 01011b: RXD6/SMISO6/SSCL6 01101b: RSPCKA 11001b: TS25	Pin function select bits 00000b: Hi-Z 00001b: MTIC5W 00010b: MTIOC3D 01011b: RXD6/SMISO6/SSCL6 01101b: RSPCKA 11001b: TS25
PB3PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0A 00010b: MTIOC4A 00101b: TMO0 00111b: POE3# 01011b: SCK6 11001b: TS22	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0A 00010b: MTIOC4A 00101b: TMO0 00111b: POE3# 01011b: SCK6 11001b: TS22 11011b: LPTO

Table 2.31 Comparison of PCn Pin Function Control Register (PCnPFS)

Register	Bit	RX130 (n = 0 to 7)	RX140 (n = 2 to 7)
PC0PFS	—	PC0 pin function select register	—
PC1PFS	—	PC1 pin function select register	—
PC4PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3D 00010b: MTCLKC 00101b: TMCI1 00111b: POE0# 01010b: SCK5 01011b: CTS8#/RTS8#/SS8# 01101b: SSLA0 11001b: TSCAP	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3D 00010b: MTCLKC 00011b: MTIOC0A 00101b: TMCI1 00111b: POE0# 01010b: SCK5 01011b: CTS8#/RTS8#/SS8# 01101b: SSLA0 11001b: TSCAP
PC5PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3B 00010b: MTCLKD 00101b: TMRI2 01010b: SCK8 01101b: RSPCKA 11001b: TS15	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3B 00010b: MTCLKD 00011b: MTIOC0C 00101b: TMRI2 01010b: SCK8 01101b: RSPCKA 11001b: TS15

Register	Bit	RX130 (n = 0 to 7)	RX140 (n = 2 to 7)
PC7PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKB 00101b: TMO2 00111b: CACREF 01010b: TXD8/SMOSI8/SSDA8 01101b: MISOA 11001b: TS13	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKB 00101b: TMO2 00111b: CACREF 01010b: TXD8/SMOSI8/SSDA8 01101b: MISOA 11001b: TS13 11011b: LPTO

Table 2.32 Comparison of PDn Pin Function Control Register (PDnPFS)

Register	Bit	RX130 (n = 0 to 7)	RX140 (n = 0 to 2)
PD3PFS	—	PD3 pin function select register	—
PD4PFS	—	PD4 pin function select register	—
PD5PFS	—	PD5 pin function select register	—
PD6PFS	—	PD6 pin function select register	—
PD7PFS	—	PD7 pin function select register	—
PDnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PD0: IRQ0 (100/80-pin) PD1: IRQ1 (100/80-pin) PD2: IRQ2 (100/80-pin) PD3: IRQ3 (100-pin) PD4: IRQ4 (100-pin) PD5: IRQ5 (100-pin) PD6: IRQ6 (100-pin) PD7: IRQ7 (100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PD0: IRQ0 (80-pin) PD1: IRQ1 (80-pin) PD2: IRQ2 (80-pin)
	ASEL	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin PD0: AN024 (100/80-pin) PD1: AN025 (100/80-pin) PD2: AN026 (100/80-pin) PD3: AN027 (100-pin) PD4: AN028 (100-pin) PD5: AN029 (100-pin) PD6: AN030 (100-pin) PD7: AN031 (100-pin)	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin PD0: AN024 (80-pin) PD1: AN025 (80-pin) PD2: AN026 (80-pin)

Table 2.33 Comparison of PEn Pin Function Control Register (PEnPFS)

Register	Bit	RX130 (n = 0 to 7)	RX140 (n = 0 to 5)
PE3PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 00111b: POE8# 01001b: CLKOUT 01100b: CTS12#/RTS12#/SS12# 11001b: TS34	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 00010b: MTIOC1B 00111b: POE8# 01001b: CLKOUT 01100b: CTS12#/RTS12#/SS12# 11001b: TS34
PE4PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 00010b: MTIOC1A 01001b: CLKOUT 11001b: TS33	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 00010b: MTIOC1A 00011b: MTIOC4A 01001b: CLKOUT 11001b: TS33
PE6PFS	—	PE6 pin function control register	—
PE7PFS	—	PE7 pin function control register	—
PEnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE2: IRQ7 (100/80/64/48-pin) PE5: IRQ5 (100/80/64-pin) PE6: IRQ6 (100-pin) PE7: IRQ7 (100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE2: IRQ7 (80/64/48/32-pin) PE5: IRQ5 (80/64-pin)
	ASEL	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin PE0: AN016 (100/80/64-pin) PE1: AN017, CMPB0 (100/80/64/48-pin) PE2: AN018, CVREFB0 (100/80/64/48-pin) PE3: AN019 (100/80/64/48-pin) PE4: AN020, CMPA2 (100/80/64/48-pin) PE5: AN021 (100/80/64-pin) PE6: AN022 (100-pin) PE7: AN023 (100-pin)	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin PE0: AN016 (80/64-pin) PE1: AN017, CMPB0 (80/64/48/32-pin) PE2: AN018, CVREFB0 (80/64/48/32-pin) PE3: AN019 (80/64/48/32-pin) PE4: AN020, CMPA2 (80/64/48/32-pin) PE5: AN021 (80/64-pin)

Table 2.34 Comparison of PHn Pin Function Control Register (PHnPFS)

Register	Bit	RX130 (n = 0 to 3)	RX140 (n = 0 to 3)
PH0PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00111b: CACREF 11001b: TS10	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3B 00111b: CACREF 11001b: TS10
PH1PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00101b: TMO0 11001b: TS9	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3D 00101b: TMO0 11001b: TS9
PH2PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00101b: TMRI0 11001b: TS8	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4C 00101b: TMRI0 11001b: TS8
PH3PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00101b: TMCI0 11001b: TS7	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 00101b: TMCI0 11001b: TS7

Table 2.35 Comparison of PJn Pin Function Control Register (PJnPFS)

Register	Bit	RX130 (n = 1, 3, 6, 7)	RX140 (n = 1, 6, 7)
PJ3PFS	—	PJ3 pin function control register	—

2.14 8-Bit Timer

Table 2.36 is a comparative overview of 8-bit timers.

Table 2.36 Comparative Overview of 8-Bit Timers

Item	RX130 (TMR)	RX140 (TMRa)
Count clocks	• Frequency-divided clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock: external count clock	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock: external count clock
Number of channels	(8 bits × 2 channels) × 2 units	(8 bits × 2 channels) × 2 units
Compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selectable among compare match A, compare match B, and external reset signal.	Selectable among compare match A, compare match B, and external counter reset signal.
Timer output	Output pulses with a user-defined duty cycle or PWM output	Output pulses with a user-defined duty cycle or PWM output
Cascading of two channels	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
Event link function (output)	Compare match A, compare match B, and overflow (TMR0, TMR2)	Compare match A, compare match B, and overflow (TMR0, TMR2)
Event link function (input)	Ability to perform one of three actions according to accepted event (1) Counter start (TMR0, TMR2) (2) Event counter (TMR0, TMR2) (3) Counter restart (TMR0, TMR2)	Ability to perform one of three actions according to accepted event (1) Counter start (TMR0, TMR2) (2) Event counter (TMR0, TMR2) (3) Counter restart (TMR0, TMR2)
DTC activation	The DTC can be activated by compare match A interrupts or compare match B interrupts.	The DTC can be activated by compare match A interrupts or compare match B interrupts.
Generation of baud rate clock for SCI	Generation of baud rate clock for SCI	Generation of basic clock for SCI
Generation of REMC receive clock	Generation of operating clock for remote control signal reception function (REMC)	—
Low power consumption function	Each unit can be placed in a module stop state.	Each unit can be placed in a module stop state.

2.15 Realtime Clock

Table 2.37 is a comparison of realtime clock registers.

Table 2.37 Comparison of Realtime Clock Registers

Register	Bit	RX130 (RTCc)	RX140 (RTCc)
RCR3	—	RTC control register 3	—

2.16 Low-Power Timer

Table 2.38 is a comparative overview of the low-power timers, and Table 2.39 is a comparison of low-power timer registers.

Table 2.38 Comparative Overview of Low-Power Timers

Item	RX130 (LPT)	RX140 (LPTa)
Clock source	Sub-clock oscillator or IWDT-dedicated on-chip oscillator	Sub-clock, LOCO clock (divided by 4), or IWDT-dedicated clock
Clock division ratio	Divided by 2, 4, 8, 16, or 32	No division, or divided by 2, 4, 8, 16, or 32
Count operation	• Count up using the 16-bit up-counter • Count operation can be continued even in software standby mode	• Count up using the 16-bit up-counter. • Count operation can be continued even in software standby mode.
Compare match	• Compare match 0 (A compare match signal is generated only in software standby mode)	• Compare match 0 (A compare match signal is generated only in software standby mode.) • Compare match 1
PWM waveform generation	—	A PWM waveform can be output on the LPT0 pin.
Interrupt	—	Compare match 1
Event link function (output)	• Compare match 0 An event signal is output (a compare match signal is generated only in software standby mode).	• Compare match 0 (A compare match signal is generated only in software standby mode.) • Compare match 1

Table 2.39 Comparison of Low-Power Timer Registers

Register	Bit	RX130 (LPT)	RX140 (LPTa)
LPTCR1	LPCNTPSSEL [2:0]	Low-power timer clock division ratio select bits b2 b0 0 0 1: Source clock divided by 2 0 1 0: Source clock divided by 4 0 1 1: Source clock divided by 8 1 0 0: Source clock divided by 16 1 0 1: Source clock divided by 32 Settings other than the above are prohibited.	Clock division ratio select bits b2 b0 0 0 0: No division 0 0 1: Divided by 2 0 1 0: Divided by 4 0 1 1: Divided by 8 0 0 0: Divided by 16 1 0 1: Divided by 32 Settings other than the above are prohibited.
	LPCNTCKSEL (RX130) LPCNTCKSEL2, LPCNTCKSEL (RX140)	Low-power timer clock source select bit 0: Sub-clock oscillator is selected. 1: IWDT-dedicated on-chip oscillator is selected.	Clock source select bit 2 (b3), clock source select bit (b4) b4 b3 0 0: Sub-clock 0 1: LOCO clock divided by 4*1 1 0: IWDT-dedicated clock (IWDTCLK) 1 1: LOCO clock divided by 4*1 Make settings such that the frequency of the system clock (ICLK) and peripheral module clock (PCLKB) ≥ 4 × (the frequency of the clock source).
	LPCMRE1	—	Compare match 1 enable bit
LPTCR2	OPOL	—	Output polarity select bit
	OLVL	—	Output level select bit
	PWME	—	PWM mode enable bit
LPCMR1	—	—	Low-power timer compare register 1

Note: 1. The clock generated by the low-speed on-chip oscillator (LOCO), divided by 4, is supplied to the low-power timer. To ensure that operation of the LOCO clock continues in software standby mode when it being used as the clock source of the low-power timer, set the LFOCR.LOFXIN bit to 1.

2.17 Serial Communications Interface

Table 2.40 is a comparative overview of the serial communications interfaces, and Table 2.41 is a comparison of serial communications interface channel specifications, and Table 2.42 is a comparison of serial communications interface registers.

Table 2.40 Comparative Overview of Serial Communications Interfaces

Item		RX130 (SCIg, SCIh)	RX140 (SCIg, SCIk, SCIh)
Number of channels		• SCIg: 6 channels • SCIh: 1 channel	• SCIg: 3 channels • SCIk: 2 channels • SCIh: 1 channel
Serial communications modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I^2C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I^2C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable as LSB first or MSB first transfer.	Selectable as LSB first or MSB first transfer.
I/O signal level inversion		—	The levels of input and output signals can be inverted independently (SCI1 and SCI5).
Interrupt sources		Transmit end, transmit data empty, receive data full, and receive error, completion of generation of a start condition, restart condition, or stop condition (for simple I^2C mode)	Transmit end, transmit data empty, receive data full, receive error, and data match (SCI1 and SCI5), completion of generation of a start condition, restart condition, or stop condition (for simple I^2C mode)
Low power consumption function		Individual channels can be transitioned to the module stop state.	Individual channels can be transitioned to the module stop state.
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection function	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Data match detection	—	Compares receive data and comparison data, and generates interrupt when they are matched (SCI1 and SCI5)

Item		RX130 (SCIg, SCIh)	RX140 (SCIg, SCIk, SCIh)
Asynchronous mode	Start-bit detection	Low level or falling edge is selectable.	Low level or falling edge is selectable.
	Receive data sampling timing adjustment	—	The receive data sampling point can be shifted from the center of the data forward or backward to a base point (SCI1 and SCI5).
	Transmit signal change timing adjustment	—	Either the falling or rising edge of the transmit data can be delayed (SCI1 and SCI5).
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly or by reading the SPTR.RXDMON flag (SCI1 or SCI5).
	Clock source	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5, SCI6, and SCI12).	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5, SCI6, and SCI12).
	Double-speed mode	Baud rate generator double-speed mode is selectable.	Baud rate generator double-speed mode is selectable.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/ reception.	CTSn# and RTSn# pins can be used in controlling transmission/ reception.
Smart card interface mode	Error processing	• An error signal can be automatically transmitted when detecting a parity error during reception • Data can be automatically retransmitted when receiving an error signal during transmission	• An error signal can be automatically transmitted when detecting a parity error during reception • Data can be automatically retransmitted when receiving an error signal during transmission
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	I^2C bus format	I^2C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer rate	Fast mode is supported.	Fast mode is supported.
	Noise cancellation	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.

Item		RX130 (SCIg, SCIh)	RX140 (SCIg, SCIk, SCIh)
Simple SPI mode	Data length	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.
Extended serial mode (supported by SCI12 only)	Start frame transmission	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection
	Start frame reception	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two kinds of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two kinds of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates
	I/O control function	• Ability to select polarity or TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select receive data sampling timing of RXDX12 pin	• Ability to select polarity or TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select receive data sampling timing of RXDX12 pin
	Timer function	Usable as reloading timer	Usable as reloading timer
Bit rate modulation function		Correction of outputs from the on-chip baud rate generator can reduce errors.	Correction of outputs from the on-chip baud rate generator can reduce errors.

Item	RX130 (SCIg, SCIh)	RX140 (SCIg, SCIk, SCIh)
Event link function (supported by SCI5 only)	• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output	• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output

Table 2.41 Comparison of Serial Communications Interface Channel Specifications

Item	RX130 (SCIg, SCIh)	RX140 (SCIg, SCIk, SCIh)
Synchronous mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI1, SCI5, SCI6, SCI8, SCI9, SCI12
Clock synchronous mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI1, SCI5, SCI6, SCI8, SCI9, SCI12
Smart card interface mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI1, SCI5, SCI6, SCI8, SCI9, SCI12
Simple I^2C mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI1, SCI5, SCI6, SCI8, SCI9, SCI12
Simple SPI mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI1, SCI5, SCI6, SCI8, SCI9, SCI12
Data match detection	—	SCI1, SCI5
Extended serial mode	SCI12	SCI12
TMR clock input	SCI5, SCI6, SCI12	SCI5, SCI6, SCI12
Event link function	SCI5	SCI5
Peripheral module clock	PCLKB: SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	PCLKB: SCI1, SCI5, SCI6, SCI8, SCI9, SCI12

Table 2.42 Comparison of Serial Communications Interface Registers

Register	Bit	RX130 (SCIg, SCIh)	RX140 (SCIg, SCIk, SCIh)
SCR	MPIE	Multi-processor interrupt enable bit (Valid in asynchronous mode when SMR.MP bit = 1) 0: Normal receive operation 1: When data is received while the multi-processor bit is set to 0, the data is skipped, and setting of status flags ORER and FER in SSR is disabled. When data is received while the multi-processor bit is set to 1, the MPIE bit is automatically cleared to 0, and normal receive operation resumes.	Multi-processor interrupt enable bit (Valid in asynchronous mode when SMR.MP bit = 1) 0: Normal receive operation 1: When data is received while the multi-processor bit is set to 0, the data is skipped, and setting (to 1) of status flags RDRF, ORER, and FER in SSR is disabled. When data is received while the multi-processor bit is set to 1, the MPIE bit is automatically cleared to 0, and normal receive operation resumes.
SEMR	ITE	—	Immediate transmission enable bit
	ABCSE	—	Asynchronous basic clock select extended bit
CDR	—	—	Comparison data register
DCCR	—	—	Data comparison control register
SPTR	—	—	Serial port register
TMGR	—	—	Transmit/receive timing select register

2.18 Serial Peripheral Interface

Table 2.43 is a comparative overview of serial peripheral interfaces, and Table 2.44 is a comparison of serial peripheral interface registers.

Table 2.43 Comparative Overview of Serial Peripheral Interfaces

Item	RX130 (RSPIa)	RX140 (RSPIc)
Number of channels	1 channel	1 channel
RSPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK
Data format	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits).	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits). • Byte swapping of transmit and receive data is selectable
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 8 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 8). — Width at high level: 4 cycles of PCLK Width at low level: 4 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4). — Width at high level: 2 cycles of PCLK Width at low level: 2 cycles of PCLK
Buffer configuration	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection

Item	RX130 (RSPIa)	RX140 (RSPIc)
SSL control function	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) — Range:1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) — Range:1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity
Control in master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function
Interrupt sources	• Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, or parity error) • RSPI idle interrupt (RSPI idle)	• Receive buffer full interrupt • Transmit buffer empty interrupt • Error interrupt (mode fault, overrun, underrun, or parity error) • Idle interrupt
Other functions	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode	• Function for initializing the RSPI • Loopback mode
Low power consumption function	Ability to specify module stop state.	Ability to specify module stop state.

Table 2.44 Comparison of Serial Peripheral Interface Registers

Register	Bit	RX130 (RSPIa)	RX140 (RSPIc)
SPSR	MODF	Mode fault error flag 0: No mode fault error occurs 1: A mode fault error occurs	Mode fault error flag 0: Neither a mode fault error nor an underrun error occurs 1: A mode fault error or an underrun error occurs
	UDRF	—	Underrun error flag
SPDR	—	RSPI data register Accessible size • Longwords access (SPDCR.SPLW = 1) • Words access (SPDCR.SPLW = 0)	RSPI data register Accessible size • Longwords access (SPDCR.SPLW = 1, SPBYTE = 0) • Words access (SPDCR.SPLW = 0, SPBYTE = 0) • Bytes access (SPDCR.SPBYT = 1)
SPDCR	SPBYT	—	RSPI byte access specification bit
SPCR2	SPPE	Parity enable bit 0: A parity bit is not added to transmit data, and no parity checking of receive data is performed. 1: A parity bit is added to transmit data, and parity checking of receive data is performed (when SPCR.TXMD = 0). A parity bit is added to transmit data, but no parity checking of receive data is performed (when SPCR.TXMD = 1).	Parity enable bit 0: A parity bit is not added to transmit data, and no parity checking of receive data is performed. 1: A parity bit is added to transmit data, and parity checking of receive data is performed.
SPDCR2	—	—	RSPI data control register 2

2.19 Capacitive Touch Sensing Unit

Table 2.45 is a comparative overview of the capacitive touch sensing units, and Table 2.46 is a comparison of capacitive touch sensing unit registers.

Table 2.45 Comparative Overview of Capacitive Touch Sensing Units

Item		RX130 (CTSUa)	RX140 (CTSU2SL, CTSU2L)
Operating clock		PCLK, PCLK/2, or PCLK/4	Selectable among PCLKB (1 MHz and above), PCLKB/2, or PCLKB/4, and PCLKB/8
I/O pins	Electrostatic capacitance measurement pins	Electrostatic capacitance measurement pins (36 channels)	Electrostatic capacitance measurement pins (36*1/12 channels)
	Measurement power supply capacitor connection pin	TSCAP	TSCAP (0.01 µF)
Measurement modes	Self-capacitance method	A single touch key is assigned to a single touch pin, and the electrostatic capacitance when in proximity to the human body is measured.	The electrostatic capacitance of pins is determined by measuring the current flow to a switched capacitor.
	Mutual capacitance method	The electrostatic capacitance between two electrodes facing each other (transmission electrode and reception electrode) is measured. • The transmission power supply can be switched between the internal logic power supply and VCC (dedicated).	The mutual capacitance between two pins is determined by measuring the current flow to a switched capacitor. • The transmission power supply can be switched among the internal logic power supply, I/O power supply, and VCC (dedicated).
	Current measurement mode	—	Direct reading of current flowing to pin
Scan modes	Single-scan mode	Electrostatic capacitance is measured on a user-defined channel.	Electrostatic capacitance is measured on one channel.
	Multi-scan mode	Electrostatic capacitance is measured on multiple user-defined channels successively.	Electrostatic capacitance is measured on multiple channels successively.
Noise prevention		Synchronous noise prevention, high-range noise prevention	• Sensor drive pulse spectrum diffusion function • Sensor drive pulse random phase shift function • Noise hopping function using multiple-frequency sensor drive pulses
Individual pin adjustments		• Offset current adjustment function • Specification of sensor drive pulse frequency • Specification of measurement duration	• Offset current adjustment function • Specification of sensor drive pulse frequency • Specification of measurement duration

Item	RX130 (CTSUa)	RX140 (CTSU2SL, CTSU2L)
Measurement start conditions	• Software trigger • External trigger (event input from event link controller (ELC))	• Software trigger • External trigger (event input from event link controller (ELC))
Automatic processing functions	—	• Automatic correction function*1 • Automatic determination function*1
Low-power functions	—	Ability to perform measurement in snooze mode • Measurement start by external trigger input via ELC • Ability to end snooze mode by contactless determination using automatic determination function*1 • Ability to cancel snooze mode by measurement end interrupt
Interrupt sources	• Channel-specific setting register write request interrupt (CTSUWR) • Measurement data transfer request interrupt (CTSURD) • Measurement end interrupt (CTSUFN)	• Register setting request interrupt (CTSUWR) • Measurement result read request interrupt (CTSURD) • Measurement end interrupt (CTSUFN)
Event link function	—	Measurement start trigger input

Note: 1. These functions are implemented on products with ROM capacity of 128 KB or greater.

Table 2.46 Comparison of Capacitive Touch Sensing Unit Registers

Register	Bit	RX130 (CTSUa)	RX140 (CTSU2SL, CTSU2L)
CTSUCR0, CTSUCR1 (RX130) CTSUCRA (RX140)	—	CTSU control register 0, CTSU control register 1 CTSUCR0 and CTSUCR1 are 8-bit registers.	CTSU control register A CTSUCRA is a 32-bit register.
	CTSUCR0.CTSUSTRT (RX130) STRT (RX140)	CTSU measurement operation start bit	Measurement operation start bit
	CTSUCR0.CTSUCAP (RX130) CAP (RX140)	CTSU measurement operation start trigger select bit	Measurement start trigger select bit
	CTSUCR0.CTSUSNZ (RX130) SNZ (RX140)	CTSU wait state power-saving enable bit	Snooze function enable bit
	CTSUCR0.CTSUIOC	CTSU transmit pin control bit	— (The CTSUCALIB.IOC bit performs the same function.)
	CTSUCR0.CTSUINIT (RX130) INIT (RX140)	CTSU control block initialization bit	Control block initialization bit
	CTSUCR0.CTSUTXVSEL (RX130) TXVSEL[1:0] (RX140)	CTSU transmission power supply select bit (b7) 0: VCC selected. 1: Internal logic power supply selected.	Transmission power supply select bit (b7 and b6) b7 b6 0 0: I/O power supply 0 1: VCC 1 0: Internal logic power supply 1 1: VCC
	CTSUCR1.CTSUPON (RX130) PON (RX140)	CTSU power supply enable bit (b0)	Measurement power supply enable bit (b8)
	CTSUCR1.CTSUCSW (RX130) CSW (RX140)	CTSU LPF capacitance charging control bit (b1)	LPF capacitance charging control bit (b9)
	CTSUCR1.CTSUATUNE0 (RX130) ATUNE0 (RX140)	CTSU power supply operating mode setting bit (b2)	Power supply operating mode setting bit (b10) Set this bit to 1 when the VCC voltage is less than 2.4 V.

Register	Bit	RX130 (CTSUa)	RX140 (CTSU2SL, CTSU2L)
CTSUCR0, CTSUCR1 (RX130) CTSUCRA (RX140)	CTSUCR1.CTSUATUNE1 (RX130) ATUNE1, ATUNE2 (RX140)	CTSU power supply capacity adjustment bit (b3) 0: Normal output 1: High-current output	Current range setting bit 1 (b11) Current range setting bit 2 (b17) ATUNE2 ATUNE1 0 0: 80 µA 0 1: 40 µA 0 0: 20 µA 1 1: 160 µA
	CTSUCR1.CTSUCLK[1:0] (RX130) CLK[1:0] (RX140)	CTSU operating clock select bits (b5 and b4) b5 b4 0 0: PCLK 0 1: PCLK/2 (PCLK divided by 2) 1 0: PCLK/4 (PCLK divided by 4) 1 1: Setting prohibited.	Operating clock select bits (b13 and b12) b13 b12 0 0: PCLKB 0 1: PCLKB/2 (PCLKB divided by 2) 1 0: PCLKB/4 (PCLKB divided by 4) 1 1: PCLKB/8 (PCLKB divided by 4)
	CTSUCR1.CTSUMD[1:0] (RX130) MD0, MD1 (RX140)	CTSU measurement mode select bits (b7 and b6) b7 b6 0 0: Self-capacitance single-scan mode 0 1: Self-capacitance multi-scan mode 1 0: Setting prohibited. 1 1: Mutual capacitance full-scan mode	Measurement mode select bits 0 and 1 (b15 and b14) b15 b14 0 0: Self-capacitance single-scan mode 0 1: Self-capacitance multi-scan mode 1 0: Mutual capacitance single-scan mode 1 1: Mutual capacitance multi-scan mode
	PUMPON	—	Step-up circuit activation bit Set this bit to 1 when the VCC voltage is less than 4.5 V.
	LOAD[1:0]	—	Measurement load control bits
	POSEL[1:0]	—	Non-measurement channel output select bits
	SDPSEL	—	Sensor drive panel select bit
	PCSEL	—	Step-up circuit clock select bit
	STCLK[5:0]	—	State clock select bits
	DCMODE	—	Current measurement mode select bit
	DCBACK	—	Current measurement feedback select bit

Register	Bit	RX130 (CTSUa)	RX140 (CTSU2SL, CTSU2L)
CTSUSDPRS, CTSUSST (RX130) CTSUCRB (RX140)	—	CTSU synchronous noise reduction setting register, CTSU sensor stabilization wait control register CTSUSDPRS and CTSUSST are 8-bit registers.	CTSU control register B CTSUCRB is a 32-bit register.
	CTSUSDPRS.CTSUPRRATIO [3:0] (RX130) PRRATIO (RX140)	CTSU measurement time and pulse count adjustment bits Recommended setting value: 3 (0011b)	Pseudorandom number update period setting bit*1 Sets the shift period of the linear feedback shift register (LFSR) used to generate pseudorandom numbers.
	CTSUSDPRS.CTSUPRMODE [1:0] (RX130) PRMODE (RX140)	CTSU base period and pulse count setting bits b5 b4 0 0: 510 pulses 0 1: 126 pulses 1 0: 62 pulses (recommended setting value) 1 1: Setting prohibited.	Pseudorandom number generation cycle setting bit*1 b5 b4 0 0: 255 cycles 0 1: 63 cycles 1 0: 31 cycles 1 1: 3 cycles
	CTSUSDPRS.CTSUSOFF (RX130) SOFF (RX140)	CTSU high-pass noise reduction function off setting bit	Frequency diffusion function off bit
	PROFF	—	Pseudorandom number off bit
	CTSUSST.CTSUSST[7:0] (RX130) SST[7:0] (RX140)	CTSU sensor stabilization wait control bits (b7 to b0) The value of these bits should be fixed at 0001 0000b.	Sensor stabilization wait time setting bits (b15 to b8) • Random pulse mode If n is defined as the setting value when (CTSUCRA.SDPSEL = 0), the stabilization wait time is 2 (n + 1) cycles of the PCLKB-synchronous sensor drive pulse. • High-resolution pulse mode If n is defined as the setting value when (CTSUCRA.SDPSEL = 1), the stabilization wait time is n + 1 cycles of STCLK.

Register	Bit	RX130 (CTSUa)	RX140 (CTSU2SL, CTSU2L)
CTSUSDPRS, CTSUSST (RX130) CTSUCRB (RX140)	SSMOD[2:0]	—	SUCLK diffusion mode select bits
	SSCNT[1:0]	—	SUCLK diffusion control bits
CTSUMCH0, CTSUMCH1 (RX130) CTSUMCH (RX140)	—	CTSU measurement channel register 0, CTSU measurement channel register 1 CTSUMCH0 and CTSUMCH1 are 8-bit registers.	CTSU measurement channel register CTSUMCHCTSUCRB is a 32-bit register.
	CTSUMCH0.CTSUMCH0[5:0] (RX130) MCH0[5:0] (RX140)	CTSU measurement channel 0 bits (b5 to b0) • Self-capacitance single-scan mode b5 b0 0 0 0 0 0 0: TS0 : : 1 0 0 0 1 1: TS35 Other than above: Starting measurement operation (CTSUCR0.CTSUSTRT bit = 1) is prohibited after these bits are set. • Measurement modes other than self-capacitance single-scan mode b5 b0 0 0 0 0 0 0: TS0 : : 1 0 0 0 1 1: TS35 1 1 1 1 1 1: Measurement is stopped.	Measurement channel 0 bits (b5 to b0) • Single-scan mode Specifies the number of the receive channel to be measured. • Multi-scan mode Specifies the number of the receive channel currently being measured.
	CTSUMCH1.CTSUMCH1[5:0] (RX130) MCH1[5:0] (RX140)	CTSU measurement channel 1 bits (b5 to b0) b5 b0 0 0 0 0 0 0: TS0 : : 1 0 0 0 1 1: TS35 1 1 1 1 1 1: Measurement is stopped.	Measurement channel 1 bits (b13 to b8) • Single-scan mode Specifies the number of the transmit channel to be measured. • Multi-scan mode Specifies the number of the transmit channel currently being measured.

Register	Bit	RX130 (CTSUa)	RX140 (CTSU2SL, CTSU2L)
CTSUMCH0, CTSUMCH1 (RX130) CTSUMCH (RX140)	MCAn	—	Multi-clock n enable bit (n = 0 to 3)
CTSUCHACn (RX130) CTSUCHACx (RX140)	—	CTSU channel enable control register n (n = 0 to 4) CTSUCHACn is an 8-bit register.	CTSU channel enable control register x (x = A, B) CTSUCHACx is a 32-bit register.
	CTSUCHACnj (RX130) CHACm (RX140)	CTSU channel enable control nj bit (n = 0 to 4) (j = 0 to 7)	Channel m enable control bit (m = 0 to 35)
CTSUCHTRCn (RX130) CTSUCHTRCx (RX140)	—	CTSU channel transmit/receive control register n (n = 0 to 4) CTSUCHTRCn is an 8-bit register.	CTSU channel transmit/receive control register x (x = A, B) CTSUCHTRCA is a 32-bit register.
	CTSUCHTRCnj (RX130) CHTRCm (RX140)	CTSU channel transmit/ receive control nj bit (n = 0 to 4) (j = 0 to 7)	Channel m transmit/ receive control bit (m = 0 to 35)
CTSUDCLKC	CTSUSSMOD[1:0]	CTSU diffusion clock mode select bits	— (The CTSUCRB.SSMOD[2:0] bits perform the same function.)
	CTSUSSCNT[1:0]	CTSU diffusion clock control bits	— (The CTSUCRB.CTSUSSCNT [1:0] bits perform the same function.)
CTSUST (RX130) CTSUSR (RX140)	—	CTSU status register CTSUST is an 8-bit register.	CTSU status register CTSUSR is a 32-bit register.
	CTSUSTC[2:0] (RX130) STC[2:0] (RX140)	CTSU measurement status counter (b2 to b0)	Measurement status counter (b10 to b8)
	CTSUDTSR (RX130) DTSR (RX140)	CTSU data transfer status flag (b4)	Data transfer status flag (b12)
	CTSUSOVF (RX130) SOVF (RX140)	CTSU sensor counter overflow flag (b5)	Sensor counter overflow flag (b13)
	CTSUROVF (RX130) UCOVF (RX140)	CTSU reference counter overflow flag (b6)	Sensor unit clock counter overflow flag (b14)
	CTSUPS (RX130) PS (RX140)	CTSU mutual capacitance status flag (b7)	Mutual capacitance status flag (b15)
	MFC[1:0]	—	Multi-clock counter
	ICOMPRST	—	ICOMP0 and ICOMP1 flag reset bit

Register	Bit	RX130 (CTSUa)	RX140 (CTSU2SL, CTSU2L)
CTSUST (RX130) CTSUSR (RX140)	ICOMP1	—	Overcurrent detection flag
	ICOMP0	—	Overvoltage detection flag
CTSUSSC	—	CTSU high-pass noise reduction spectrum diffusion control register	—
CTSUSO0, CTSUSO1 (RX130) CTSUSO (RX140)	—	CTSU sensor offset registers 0 and 1 CTSUSO0 and CTSUSO1 are 16-bit registers.	CTSU sensor offset register CTSUSO is a 32-bit register.
	CTSUSO0.CTSUSO[9:0] (RX130) SO[9:0] (RX140)	CTSU sensor offset adjustment bits	Sensor offset adjustment bits
	CTSUSO0.CTSUSNUM[5:0] (RX130) SNUM[7:0] (RX140)	CTSU measurement count setting bits (b15 to b10) These bits specify the number of measurements by the CTSU.	Measurement period setting bits (b17 to b10) • Random pulse mode (CTSUCRA.SDPSEL = 0) The CTSU measurement period is specified as the number of times the basic measurement unit is repeated. The allowable setting range is 00h to 3Fh. If the setting value is n, the basic measurement unit is repeated n + 1 times. • High-resolution pulse mode (CTSUCRA.SDPSEL = 1) The CTSU measurement period is based on STCLK cycles. If the setting value is n, measurement takes place for a period equal to 8 (n + 1) cycles of STCLK.
	CTSUSO1.CTSURICOA[7:0]	CTSU reference ICO current adjustment bits	—

Register	Bit	RX130 (CTSUa)	RX140 (CTSU2SL, CTSU2L)
CTSUSO0, CTSUSO1 (RX130) CTSUSO (RX140)	CTSUSO1.CTSUSDPA[4:0] (RX130) SDPA[7:0] (RX140)	CTSU base clock setting bits (b12 to b8) b12 b8 0 0 0 0 0: Operating clock divided by 2 0 0 0 0 1: Operating clock divided by 4 : : 1 1 1 1 0: Operating clock divided by 62 1 1 1 1 1: Operating clock divided by 64	Base clock setting bits (b31 to b24) • Random pulse mode (CTSUCRA.SDPSEL = 0) If the setting value is n, the base clock frequency is the operating clock divided by 2 (n + 1). • High-resolution pulse mode (CTSUCRA.SDPSEL = 1) If the setting value is n, the base clock frequency is n + 1 SUCLK cycles.
	CTSUSO1.CTSUICOG[1:0]	CTSUICO gain adjustment bits	—
	SSDIV[3:0]	—	Spectrum diffusion sampling cycle control bits
CTSUSC	CTSUSC[15:0]	CTSU sensor counter bits	—
CTSURC	—	CTSU reference counter	—
CTSUERRS (RX130) CTSUCALIB (RX140)	—	CTSU error status register CTSUERRS is a 16-bit register.	CTSU calibration register CTSUCALIB is a 32-bit register.
	CTSUSPMD[1:0]	Calibration mode bits	—
	CTSUTSOD (RX130) TSOD (RX140)	TS pin fixed output bit	TS all-pin output control bit
	CTSUDRV (RX130) DRV (RX140)	Calibration setting bit 1	Calibration setting bit 1
	CTSUTSOC (RX130) TSOC (RX140)	Calibration setting bit 2	Calibration setting bit 2
	CTSUICOMP	TSCAP voltage error monitor bit	—
	CLKSEL[1:0]	—	Monitor clock select bits
	SUCLKEN	—	SUCLK enable bit
	IOC	—	Transmit pin control bit
	DCOFF	—	Down-convert off bit
	IOCSEL*2	—	TS pin IOC fixed select bit
	DACCARRY	—	DAC upper current source carry input
	SUCARRY	—	CCO carry input
	DACCLK	—	DAC modulation circuit clock select bit
	CCOCLK	—	CCO modulation circuit clock select bit

Register	Bit	RX130 (CTSUa)	RX140 (CTSU2SL, CTSU2L)
CTSUERRS (RX130) CTSUCALIB (RX140)	CCOCALIB	—	CCO calibration mode select bit
	TXREV	—	Transit pin inverted output bit
CTSUTRMR	—	CTSU reference current calibration register	—
CTSUSUCLKA	—	—	CTSU sensor unit clock control register A
CTSUSUCLKB	—	—	CTSU sensor unit clock control register B
CTSUTRIMA	—	—	CTSU trimming register A
CTSUTRIMB	—	—	CTSU trimming register B
CTSUOPT*2	—	—	CTSU option setting register
CTSUSCNTACT*2	—	—	CTSU sensor counter automatic correction table access register
CTSUAJCR*2	—	—	CTSU automatic judgment control register
CTSUAJTHR*2	—	—	CTSU threshold register
CTSUAJMMAR*2	—	—	CTSU moving average result register
CTSUAJBLACT*2	—	—	CTSU baseline average intermediate result register
CTSUAJBLAR*2	—	—	CTSU baseline average result register
CTSUAJRR*2	—	—	CTSU automatic judgment result register
CTSUADCC	—	—	CTSU A/D converter connection control register

Note: 1. Valid only when the value of the CTSUCRA.SDPSEL bit is 0 (random pulse mode).
Note: 2. These registers are implemented on products with ROM capacity of 128 KB or greater.

2.20 12-Bit A/D Converter

Table 2.47 is a comparative overview of the 12-bit A/D converters, and Table 2.48 is a comparison of 12-bit A/D converter registers.

Table 2.47 Comparative Overview of 12-Bit A/D Converters

Item	RX130 (S12ADE)	RX140 (S12ADE)
Number of units	1 unit	1 unit
Input channels	24 channels	18 channels
Extended analog function	Temperature sensor output, internal reference voltage	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	1.4 µs per channel (when A/D conversion clock ADCLK = 32 MHz)	Per channel 0.88 µs when value of conversion cycle bit is 0, 0.67 µs when value of conversion cycle bit is 1 (when A/D conversion clock (ADCLK) = 48 MHz)
A/D conversion clock	Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. PCLK to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.	Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. PCLK to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.
Data register	• 24 registers for analog input and one for A/D-converted data duplication in double trigger mode • One register for temperature sensor output • One register for internal reference • One register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • 12-bit accuracy output for the results of A/D conversion • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.	• 18 registers for analog input, one for A/D-converted data duplication in double trigger mode • One register for temperature sensor output • One register for internal reference • One register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • 12-bit accuracy output for the results of A/D conversion • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.

Item	RX130 (S12ADE)	RX140 (S12ADE)
Operating modes	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 24 channels arbitrarily selected. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of up to 24 channels arbitrarily selected. • Group scan mode: — Analog inputs of up to 24 arbitrarily selected channels are divided into group A and group B, and A/D conversion of the analog inputs selected on a group basis is performed only once. — Conversion start conditions (synchronous trigger) can be selected independently for group A and group B, allowing A/D conversion of the groups to start at different times. • Group scan mode (when group A is given priority): — If a group A trigger is input during A/D conversion on group B, A/D conversion on group B is stopped and A/D conversion is performed on group A. — Restart (rescan) of A/D conversion on group B after completion of A/D conversion on group A can be enabled.	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 18 channels arbitrarily selected. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of up to 18 channels arbitrarily selected. • Group scan mode: — Analog inputs of up to 18 arbitrarily selected channels are divided into group A and group B, and A/D conversion of the analog inputs selected on a group basis is performed only once. — Conversion start conditions (synchronous trigger) can be selected independently for group A and group B, allowing A/D conversion of the groups to start at different times. • Group scan mode (when group A is given priority): — If a group A trigger is input during A/D conversion on group B, A/D conversion on group B is stopped and A/D conversion is performed on group A. — Restart (rescan) of A/D conversion on group B after completion of A/D conversion on group A can be enabled.
Conditions for A/D conversion start	• Software trigger • Synchronous trigger Trigger by the multi-function timer pulse unit (MTU) or event link controller (ELC) • Asynchronous trigger A/D conversion can be triggered by the external trigger ADTRG0# pin.	• Software trigger • Synchronous trigger Trigger by the multi-function timer pulse unit (MTU) or event link controller (ELC) • Asynchronous trigger A/D conversion can be triggered by the external trigger ADTRG0# pin.

Item	RX130 (S12ADE)	RX140 (S12ADE)
Functions	• Variable sampling state count • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers • Compare function (window A and window B) • 16 ring buffers when the compare function is used	• Variable sampling state count • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers • Compare function (window A and window B) • 16 ring buffers when the compare function is used
Interrupt sources	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan. • In group scan mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of group A scan, whereas an A/D scan end interrupt request (GBADI) for group B can be generated on completion of group B scan. • When double trigger mode is selected in group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan of group A, whereas A/D scan end interrupt request (GBADI) specially for group B can be generated on completion of group B scan. • The S12ADI and GBADI interrupts can activate the data transfer controller (DTC).	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan. • In group scan mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of group A scan, whereas an A/D scan end interrupt request (GBADI) for group B can be generated on completion of group B scan. • When double trigger mode is selected in group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan of group A, whereas A/D scan end interrupt request (GBADI) specially for group B can be generated on completion of group B scan. • The S12ADI0 and GBADI interrupts can activate the data transfer controller (DTC).
Event link function	• An ELC event is generated on completion of scans other than group B scan in group scan mode. • An ELC event is generated on completion of group B scan in group scan mode. • An ELC event is generated on completion of all scans. • Scan can be started by a trigger output by the ELC. • An ELC event is generated according to the event conditions of the window compare function in single scan mode.	• An ELC event is generated on completion of scans other than group B scan in group scan mode. • An ELC event is generated on completion of group B scan in group scan mode. • An ELC event is generated on completion of all scans. • Scan can be started by a trigger output by the ELC. • An ELC event is generated according to the event conditions of the window compare function in single scan mode.

Item	RX130 (S12ADE)	RX140 (S12ADE)
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.48 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX130 (S12ADE)	RX140 (S12ADE)
ADANSA0	ANSA008	—	A/D conversion channel select bit
ADANSA1	ANSA106, ANSA107, ANSA111 to ANSA115	A/D conversion channel select bits	—
ADANSB0	ANSB008	—	A/D conversion channel select bit
ADANSB1	ANSB106, ANSB107, ANSB111 to ANSB115	A/D conversion channel select bits	—
ADADS0	ADS008	—	A/D-converted value addition/ average channel select bit
ADADS1	ADS106, ADS107, ADS111 to ADS115	A/D-converted value addition/ average channel select bits	—
ADSSTRn	—	A/D sampling state register n (n = 0 to 7, L, T, O)	A/D sampling state register n (n = 0 to 8, L, T, O)
ADCMPANSR0	CMPCHA008	—	Compare window A channel select bit
ADCMPANSR1	CMPCHA106, CMPCHA107, CMPCHA111 to CMPCHA115	Compare window A channel select bits	—
ADCMPLR0	CMPLCHA008	—	Compare window A comparison condition select bit
ADCMPLR1	CMPLCHA106, CMPLCHA107, CMPLCHA111 to CMPLCHA115	Compare window A comparison condition select bits	—
ADCMPSR0	CMPSTCHA008	—	Compare window A flag
ADCMPSR1	CMPSTCHA106, CMPSTCHA107, CMPSTCHA111 to CMPSTCHA115	Compare window A flag	—

Register	Bit	RX130 (S12ADE)	RX140 (S12ADE)
ADHVREFCNT	HVSEL[1:0]	High-potential reference voltage select bits b1 b0 0 0: AVCC0 is selected as the high-potential reference voltage. 0 1: VREFH0 is selected as the high-potential reference voltage. Settings other than the above are prohibited.	High-potential reference voltage select bits b1 b0 0 0: AVCC0 is selected as the high-potential reference voltage. 0 1: VREFH0 is selected as the high-potential reference voltage. Settings other than the above are prohibited. On 32-pin package products, set these bits to 01b.
ADCMPBNSR	CMPCHB[5:0]	Compare window B channel select bits These bits select channels to be compared with the compare window B conditions. b5 b0 0 0 0 0 0 0: AN000 0 0 0 0 0 1: AN001 0 0 0 0 1 0: AN002 : : 0 0 0 1 1 0: AN006 0 0 0 1 1 1: AN007 0 1 0 0 0 0: AN016 0 1 0 0 0 1: AN017 : 0 1 0 1 0 1: AN021 0 1 0 1 1 0: AN022 0 1 0 1 1 1: AN023 0 1 1 0 0 0: AN024 0 1 1 0 0 1: AN025 0 1 1 0 1 0: AN026 0 1 1 0 1 1: AN027 0 1 1 1 0 0: AN028 0 1 1 1 0 1: AN029 0 1 1 1 1 0: AN030 0 1 1 1 1 1: AN031 1 0 0 0 0 0: Temperature sensor 1 0 0 0 0 1: Internal reference voltage Settings other than the above are prohibited.	Compare window B channel select bits These bits select channels to be compared with the compare window B conditions. b5 b0 0 0 0 0 0 0: AN000 0 0 0 0 0 1: AN001 0 0 0 0 1 0: AN002 : : 0 0 0 1 1 0: AN006 0 0 0 1 1 1: AN007 0 0 1 0 0 0: AN008 0 1 0 0 0 0: AN016 0 1 0 0 0 1: AN017 : 0 1 0 1 0 1: AN021 0 1 1 0 0 0: AN024 0 1 1 0 0 1: AN025 0 1 1 0 1 0: AN026 1 0 0 0 0 0: Temperature sensor 1 0 0 0 0 1: Internal reference voltage Settings other than the above are prohibited.
ADCCR	—	—	A/D conversion cycle control register

2.21 Temperature Sensor

Table 2.49 is a comparison of temperature sensor registers.

Table 2.49 Comparison of Temperature Sensor Registers

Register	Bit	RX130 (TEMPSA)	RX140 (TEMPSA)
TSCDRH, TSCDRL (RX130) TSCDR (RX140)	—	Temperature sensor calibration data register	Temperature sensor calibration data register

2.22 RAM

Table 2.50 is a comparative overview of RAM.

Table 2.50 Comparative Overview of RAM

Item	RX130	RX140
RAM capacity	Max. 48 KB	Max. 64 KB
RAM address	• RAM capacity 48 KB RAM0: 0000 0000h to 0000 BFFFh • RAM capacity 32 KB RAM0: 0000 0000h to 0000 7FFFh • RAM capacity 16 KB RAM0: 0000 0000h to 0000 3FFFh • RAM capacity 10 KB RAM0: 0000 0000h to 0000 27FFh	• RAM capacity 64 KB RAM0: 0000 0000h to 0000 FFFFh • RAM capacity 32 KB RAM0: 0000 0000h to 0000 7FFFh • RAM capacity 16 KB RAM0: 0000 0000h to 0000 3FFFh
Access	• Single-cycle access is possible for both reading and writing. • On-chip RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. • On-chip RAM can be enabled or disabled.
Low power consumption function	Ability to specify module stop state.	Ability to specify module stop state.

2.23 Flash Memory

Table 2.51 is a comparative overview of flash memory, and Table 2.52 is a comparison of flash memory registers.

Table 2.51 Comparative Overview of Flash Memory

Item	RX130	RX140 (FLASH)
Memory capacity	• User area: Up to 512 KB • Data area: 8 KB • Extra area: Stores the start-up area information, access window information, and unique ID	• User area: Up to 256 KB • Data area: 8 KB • Extra area: Stores the start-up area information, access window information, and unique ID
Addresses	• Products with capacity of 512 KB FFF8 0000h to FFFF FFFFh • Products with capacity of 384 KB FFFA 0000h to FFFF FFFFh • Products with capacity of 256 KB FFFC 0000h to FFFF FFFFh • Products with capacity of 128 KB FFFE 0000h to FFFF FFFFh • Products with capacity of 64 KB FFFF 0000h to FFFF FFFFh	• Products with capacity of 256 KB FFFC 0000h to FFFF FFFFh • Products with capacity of 128 KB FFFE 0000h to FFFF FFFFh • Products with capacity of 64 KB FFFF 0000h to FFFF FFFFh
Software commands	• The following software commands are implemented: Program, blank check, block erase, and unique ID read • The following commands are implemented for programming the extra area: Start-up area information program and access window information program	• The following software commands are implemented: Program, blank check, block erase, and all-block erase • The following commands are implemented for programming the extra area: Start-up area information program, access window protect, and access window information program
Value after erasure	• ROM: FFh • E2 DataFlash: FFh	• ROM: FFh • E2 DataFlash: FFh
Interrupt	An interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.	An interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.
On-board programming	• Boot mode (SCI interface) — Channel 1 of the serial communications interface (SCI1) is used for asynchronous communication. — The user area and data area can be programmed. • Boot mode (FINE interface) — The FINE interface is used. — The user area and data area can be programmed. • Self-programming (single-chip mode) — The user area and data area can be programmed using a flash programming routine in a user program.	• Boot mode (SCI interface) — Channel 1 of the serial communications interface (SCI1) is used for asynchronous communication. — The user area and data area can be programmed. • Boot mode (FINE interface) — The FINE interface is used. — The user area and data area can be programmed. • Self-programming (single-chip mode) — The user area and data area can be programmed using a flash programming routine in a user program.

Item	RX130	RX140 (FLASH)
Off-board programming	The user area and data area can be programmed using a flash programmer compatible with the MCU.	The user area and data area can be programmed using a flash programmer compatible with the MCU.
ID codes protection	• Connection with a serial programmer can be controlled using ID codes in boot mode. • Connection with an on-chip debugging emulator can be controlled using ID codes.	• Connection with a serial programmer can be controlled using ID codes in boot mode. • Connection with an on-chip debugging emulator can be controlled using ID codes.
Start-up program protection function	This function is used to safely program blocks 0 to 15.	This function is used to safely program blocks 0 to 7.
Area protection	During self-programming, this function enables programming only of specified blocks in the user area and disables programming of the other blocks.	During self-programming, this function enables programming only of specified blocks in the user area and disables programming of the other blocks.
Background operation (BGO) function	Programs in the ROM can run while the E2 DataFlash is being programmed.	Programs in the ROM can run while the E2 DataFlash is being programmed.

Table 2.52 Comparison of Flash Memory Registers

Register	Bit	RX130	RX140 (FLASH)
MEMWAITR	—	—	Memory wait cycle setting register
DFLWAITR	—	—	Data flash wait cycle setting register
FPMCR	FMS0, FMS1, FSM2 (RX130) FMS0, FMS1 (RX140)	Flash operating mode select bits 0, 1, and 2 FMS2 FMS1 FMS0 0 0 0: ROM/E2 DataFlash read mode 0 1 0: E2 DataFlash P/E mode 0 1 1: Discharge mode 1 1 0 1: ROM P/E mode 1 1 1: Discharge mode 2 Settings other than the above are prohibited.	Flash operating mode select bits 0 and 1 FMS1 FMS0 0 0: ROM/E2 DataFlash read mode 0 1: ROMP/E mode 1 0: E2 DataFlash P/E mode 1 1: Setting prohibited.
	LVPE	Low-voltage P/E mode enable bit	—
FISR	PCKA[4:0] (RX130) PCKA[5:0] (RX140)	Peripheral clock notification bits	Peripheral clock notification bits

Register	Bit	RX130	RX140 (FLASH)
FCR	CMD[3:0]	Software command setting bits b3 b0 0 0 0 1: Program 0 0 1 1: Blank check 0 1 0 0: Block erase 0 1 0 1: Unique ID read Settings other than the above are prohibited.	Software command setting bits b3 b0 0 0 0 1: Program 0 0 1 1: Blank check 0 1 0 0: Block erase 0 1 1 0: All-block erase Settings other than the above are prohibited.
	DRC	Data read completion bit	—
FEXCR	CMD[2:0]	Software command setting bits b2 b0 0 0 1: Start-up area information program 0 1 0: Access window information program Settings other than the above are prohibited.	Software command setting bits b2 b0 0 0 1: Start-up area information program/access window protect 0 1 0: Access window information program Settings other than the above are prohibited.
FSARH	—	Flash processing start address register H FSARH is an 8-bit register.	Flash processing start address register H FSARH is a 16-bit register.
FEARH	—	Flash processing end address register H FEARH is an 8-bit register.	Flash processing end address register H FEARH is a 16-bit register.
FRBH	—	Flash read buffer register H	—
FRBL	—	Flash read buffer register L	—
FWBH, FWBL (RX130) FWBn (RX140)	—	Flash write buffer register H, Flash write buffer register L	Flash write buffer register n (n = 0 to 3)
FSTATR1	DRRDY	Data read ready flag	-
FEAMH	—	Flash error address monitor register H FEAMH is an 8-bit register.	Flash error address monitor register H FEAMH is a 16-bit register.
FSCMR	AWPR	—	Access window protect flag
FAWSMR	—	Flash access window start address monitor register	Flash access window start address monitor register
		Initial value after a reset differs.	
FAWEMR	—	Flash access window end address monitor register	Flash access window end address monitor register
		Initial value after a reset differs.	
UIDRn	—	Unique ID register n (n = 0 to 31) UIDRn is an 8-bit register.	Unique ID register n (n = 0 to 3) UIDRn is a 32-bit register.

2.24 Packages

As indicated in Table 2.53, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage.

Table 2.53 Packages

Package Type	Renesas Code	
	RX130	**RX140**
100-pin LFQFP	○	×
48-pin HWQFN	PWQN0048KB-A	PWQN0048KC-A
32-pin LQFP	×	○
32-pin HWQFN	×	○

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by **blue text**. Items that exists on both groups with different specifications are indicated by **red text**. **Black text** indicates there is no differences in the item's specifications between groups.

3.1 80-Pin Package

Table 3.1 is a comparative listing of the pin functions of 80-pin package products.

Table 3.1 Comparative Listing of 80-Pin Package Pin Functions

80-Pin LFQFP	RX130	RX140
1	P06*1	P06*1
2	P03*1/DA0	P03*1/DA0
3	P04*1	P04*1
4	VCL	VCL
5	PJ1/MTIOC3A	PJ1/MTIOC3A
6	MD/FINED	MD/PG7/FINED
7	XCIN	XCIN/PH7
8	XCOUT	XCOUT/PH6
9	RES#	RES#
10	XTAL/P37	XTAL/P37/IRQ4
11	VSS	VSS
12	EXTAL/P36	EXTAL/P36/IRQ2
13	VCC	VCC
14	P35/NMI	P35/NMI
15	P34/MTIOC0A/TMCI3/POE2#/SCK6/IRQ4	P34/MTIOC0A/TMCI3/POE2#/SCK6/IRQ4
16	P32/MTIOC0C/TMO3/TXD6/SMOSI6/ SSDA6/TS0/IRQ2/RTCOUT	P32/MTIOC0C/TMO3/TXD6/SMOSI6/ SSDA6/TS0/IRQ2/RTCOUT
17	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/ TS1/IRQ1	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/ TS1/IRQ1
18	P30/MTIOC4B/TMRI3/POE8#/RXD1/ SMISO1/SSCL1/TS2/IRQ0	P30/MTIOC4B/TMRI3/POE8#/RXD1/ SMISO1/SSCL1/TS2/IRQ0
19	P27/MTIOC2B/TMCI3/SCK1/TS3	P27/MTIOC2B/TMCI3/SCK1/TS3
20	P26/MTIOC2A/TMO1/TXD1/SMOSI1/ SSDA1/TS4	P26/MTIOC2A/TMO1/LPTO/TXD1/SMOSI1/ SSDA1/TS4
21	P21/MTIOC1B/TMCI0	P21/MTIOC1B/TMCI0
22	P20/MTIOC1A/TMRI0	P20/MTIOC1A/TMRI0
23	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ SCK1/MISOA/SDA0/IRQ7	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ SCK1/MISOA/SDA0/IRQ7
24	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/ SMOSI1/SSDA1/MOSIA/SCL0/IRQ6/ RTCOUT/ADTRG0#	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/ SMOSI1/SSDA1/MOSIA/SCL0/IRQ6/ RTCOUT/ADTRG0#
25	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/TS5/IRQ5	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/CRXD0/TS5/IRQ5
26	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/TS6/IRQ4	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/CTXD0/TS6/IRQ4
27	P13/MTIOC0B/TMO3/SDA0/IRQ3	P13/MTIOC0B/TMO3/SDA0/IRQ3
28	P12/TMCI1/SCL0/IRQ2	P12/TMCI1/SCL0/IRQ2
29	PH3/TMCI0/TS7	PH3/MTIOC4D/TMCI0/TS7
30	PH2/TMRI0/TS8/IRQ1	PH2/MTIOC4C/TMRI0/TS8/IRQ1

80-Pin LFQFP	RX130	RX140
31	PH1/TMO0/TS9/IRQ0	PH1/MTIOC3D/TMO0/TS9/IRQ0
32	PH0/TS10/CACREF	PH0/MTIOC3B/TS10/CACREF
33	P55/MTIOC4D/TMO3/TS11	P55/MTIOC4A/MTIOC4D/TMO3/CRXD0/ TS11
34	P54/MTIOC4B/TMCI1/TS12	P54/MTIOC4B/TMCI1/CTXD0/TS12
35	PC7/MTIOC3A/TMO2/MTCLKB/MISOA/ TS13/CACREF	PC7/MTCLKB/MTIOC3A/TMO2/LPTO/ MISOA/TXD8/SMOSI8/SSDA8/TS13/ CACREF
36	PC6/MTIOC3C/MTCLKA/TMCI2/MOSIA/ TS14	PC6/MTIOC3C/MTCLKA/TMCI2/MOSIA/ RXD8/SMISO8/SSCL8/TS14
37	PC5/MTIOC3B/MTCLKD/TMRI2/RSPCKA/ TS15	PC5/MTIOC0C/MTIOC3B/MTCLKD/TMRI2/ RSPCKA/SCK8/TS15
38	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/ SCK5/SSLA0/TSCAP	PC4/MTIOC0A/MTIOC3D/MTCLKC/TMCI1/ POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0/ TSCAP
39	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5/TS16	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5/TS16
40	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/ SSLA3/TS17	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/ SSLA3/TS17
41	PB7/PC1*[2]/MTIOC3B/TS18	PB7/PC1*[2]/MTIOC3B/TXD9/SMOSI9/ SSDA9/TS18
42	PB6/PC0*[2]/MTIOC3D/TS19	PB6/PC0*[2]/MTIOC3D/RXD9/SMISO9/ SSCL9/TS19
43	PB5/MTIOC2A/MTIOC1B/TMRI1/POE1#/ TS20	PB5/MTIOC2A/MTIOC1B/TMRI1/POE1#/ SCK9/TS20
44	PB4/TS21	PB4/CTS9#/RTS9#/SS9#/TS21
45	PB3/MTIOC0A/MTIOC4A/TMO0/POE3#/ SCK6/TS22	PB3/MTIOC0A/MTIOC4A/TMO0/POE3#/ LPTO/SCK6/TS22
46	PB2/CTS6#/RTS6#/SS6#/TS23	PB2/CTS6#/RTS6#/SS6#/TS23
47	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD6/ SMOSI6/SSDA6/TS24/IRQ4/CMPOB1	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD6/ SMOSI6/SSDA6/TS24/IRQ4/CMPOB1
48	VCC	VCC
49	PB0/MTIC5W/RXD6/SMISO6/SSCL6/ RSPCKA/TS25	PB0/MTIOC3D/MTIC5W/RXD6/SMISO6/ SSCL6/RSPCKA/TS25
50	VSS	VSS
51	PA6/MTIC5V/MTCLKB/TMCI3/POE2#/ CTS5#/RTS5#/SS5#/MOSIA/TS26	PA6/MTIOC3D/MTIC5V/MTCLKB/TMCI3/ POE2#/CTS5#/RTS5#/SS5#/MOSIA/TS26
52	PA5/RSPCKA/TS27	PA5/RSPCKA/TS27
53	PA4/MTIC5U/MTCLKA/TMRI0/TXD5/ SMOSI5/SSDA5/SSLA0/TS28/IRQ5/ CVREFB1	PA4/MTIOC4C/MTIC5U/MTCLKA/TMRI0/ TXD5/SMOSI5/SSDA5/SSLA0/TS28/IRQ5/ CVREFB1
54	PA3/MTIOC0D/MTCLKD/RXD5/SMISO5/ SSCL5/TS29/IRQ6/CMPB1	PA3/MTIOC0D/MTIOC4D/MTIC5V/MTCLKD/ RXD5/SMISO5/SSCL5/TS29/IRQ6/CMPB1
55	PA2/RXD5/SMISO5/SSCL5/SSLA3/TS30	PA2/RXD5/SMISO5/SSCL5/SSLA3/TS30
56	PA1/MTIOC0B/MTCLKC/SCK5/SSLA2/TS31	PA1/MTIOC0B/MTIOC3B/MTCLKC/SCK5/ SSLA2/TS31
57	PA0/MTIOC4A/SSLA1/TS32/CACREF	PA0/MTIOC4A/SSLA1/TS32/CACREF
58	PE5/MTIOC4C/MTIOC2B/IRQ5/AN021/ CMPOB0	PE5/MTIOC4C/MTIOC2B/IRQ5/AN021/ CMPOB0
59	PE4/MTIOC4D/MTIOC1A/TS33/AN020/ CMPA2/CLKOUT	PE4/MTIOC4D/MTIOC1A/MTIOC4A/TS33/ AN020/CMPA2/CLKOUT
60	PE3/MTIOC4B/POE8#/CTS12#/RTS12#/ SS12#/TS34/AN019/CLKOUT	PE3/MTIOC1B/MTIOC4B/POE8#/CTS12#/ RTS12#/SS12#/TS34/AN019/CLKOUT

80-Pin LFQFP	RX130	RX140
61	PE2/MTIOC4A/RXD12/RXDX12/SMISO12/ SSCL12/TS35/IRQ7/AN018/CVREFB0	PE2/MTIOC4A/RXD12/RXDX12/SMISO12/ SSCL12/TS35/IRQ7/AN018/CVREFB0
62	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12/AN017/CMPB0	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12/AN017/CMPB0
63	PE0/SCK12/AN016	PE0/SCK12/AN016
64	PD2/MTIOC4D/SCK6/IRQ2/AN026	PD2/MTIOC4D/SCK6/IRQ2/AN026
65	PD1/MTIOC4B/RXD6/SMISO6/SSCL6/IRQ1/ AN025	PD1/MTIOC4B/RXD6/SMISO6/SSCL6/IRQ1/ AN025
66	PD0/TXD6/SMOSI6/SSDA6/IRQ0/AN024	PD0/TXD6/SMOSI6/SSDA6/IRQ0/AN024
67	P47*1/AN007	P47*1/AN007
68	P46*1/AN006	P46*1/AN006
69	P45*1/AN005	P45*1/AN005
70	P44*1/AN004	P44*1/AN004
71	P43*1/AN003	P43*1/AN003
72	P42*1/AN002	P42*1/AN002
73	P41*1/AN001	P41*1/AN001
74	VREFL0/PJ7*1	VREFL0/PJ7*1
75	P40*1/AN000	P40*1/AN000
76	VREFH0/PJ6*1	VREFH0/PJ6*1
77	AVCC0	AVCC0
78	P07*1/ADTRG0#	P07*1/ADTRG0#
79	AVSS0	AVSS0
80	P05*1/DA1	P05*1/DA1

Notes: 1. The power supply of the I/O buffer for these pins is AVCC0.
2. PC0 and PC1 are valid only when the port switching function is selected.

3.2 64-Pin Package

Table 3.2 is a comparative listing of the pin functions of 64-pin package products.

Table 3.2 Comparative Listing of 64-Pin Package Pin Functions

64-Pin LFQFP/ LQFP	RX130	RX140
1	P03*1/DA0	P03*1/DA0
2	VCL	VCL
3	MD/FINED	MD/PG7/FINED
4	XCIN	XCIN/PH7*3
5	XCOUT	XCOUT/PH6*3
6	RES#	RES#
7	XTAL/P37	XTAL/P37/IRQ4
8	VSS	VSS
9	EXTAL/P36	EXTAL/P36/IRQ2
10	VCC	VCC
11	P35/NMI	P35/NMI
12	P32/MTIOC0C/TMO3/TXD6/SMOSI6/ SSDA6/TS0/IRQ2/RTCOUT	P32/MTIOC0C/TMO3/TXD6*3/SMOSI6*3/ SSDA6*3/TS0*3/IRQ2/RTCOUT
13	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/ TS1/IRQ1	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/ TS1*3/IRQ1
14	P30/MTIOC4B/TMRI3/POE8#/RXD1/ SMISO1/SSCL1/TS2/IRQ0	P30/MTIOC4B/TMRI3/POE8#/RXD1/ SMISO1/SSCL1/TS2*3/IRQ0
15	P27/MTIOC2B/TMCI3/SCK1/TS3	P27/MTIOC2B/TMCI3/SCK1/TS3
16	P26/MTIOC2A/TMO1/TXD1/SMOSI1/ SSDA1/TS4	P26/MTIOC2A/TMO1/LPTO/TXD1/SMOSI1/ SSDA1/TS4
17	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ SCK1/MISOA/SDA0/IRQ7	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ SCK1/MISOA/SDA0/IRQ7
18	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/ SMOSI1/SSDA1/MOSIA/SCL0/IRQ6/ RTCOUT/ADTRG0#	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/ SMOSI1/SSDA1/MOSIA/SCL0/IRQ6/ RTCOUT/ADTRG0#
19	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/TS5/IRQ5	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/CRXD0/TS5*3/IRQ5
20	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/TS6/IRQ4	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/CTXD0/TS6*3/IRQ4
21	PH3/TMCI0/TS7	PH3/MTIOC4D/TMCI0/TS7*3
22	PH2/TMRI0/TS8/IRQ1	PH2/MTIOC4C/TMRI0/TS8*3/IRQ1
23	PH1/TMO0/TS9/IRQ0	PH1/MTIOC3D/TMO0/TS9*3/IRQ0
24	PH0/TS10/CACREF	PH0/MTIOC3B/TS10*3/CACREF
25	P55/MTIOC4D/TMO3/TS11	P55/MTIOC4A/MTIOC4D/TMO3/CRXD0/ TS11*3
26	P54/MTIOC4B/TMCI1/TS12	P54/MTIOC4B/TMCI1/CTXD0/TS12*3
27	PC7/MTIOC3A/TMO2/MTCLKB/MISOA/ TS13/CACREF	PC7/MTIOC3A/MTCLKB/TMO2/LPTO/ TXD8*3/SMOSI8*3/SSDA8*3/MISOA/ TS13/ CACREF
28	PC6/MTIOC3C/MTCLKA/TMCI2/MOSIA/ TS14	PC6/MTIOC3C/MTCLKA/TMCI2/RXD8*3/ SMISO8*3/SSCL8*3/MOSIA/TS14
29	PC5/MTIOC3B/MTCLKD/TMRI2/RSPCKA/ TS15	PC5/MTIOC0C/MTIOC3B/MTCLKD/TMRI2/ SCK8*3/RSPCKA/TS15

64-Pin LFQFP/ LQFP	RX130	RX140
30	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/ SCK5/SSLA0/TSCAP	PC4/MTIOC0A/MTIOC3D/MTCLKC/TMCI1/ POE0#/SCK5/CTS8#*3/RTS8#*3/SS8#*3/ SSLA0/TSCAP
31	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5/TS16	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5/ TS16*3
32	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/ SSLA3/TS17	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/ SSLA3/TS17*3
33	PB7/PC1*2/MTIOC3B/TS18	PB7/PC1*2/MTIOC3B/TXD9*3/SMOSI9*3/ SSDA9*3/TS18*3
34	PB6/PC0*2/MTIOC3D/TS19	PB6/PC0*2/MTIOC3D/RXD9*3/SMISO9*3/ SSCL9*3/TS19*3
35	PB5/MTIOC2A/MTIOC1B/TMRI1/POE1#/ TS20	PB5/MTIOC2A/MTIOC1B/TMRI1/POE1#/ SCK9*3/TS20*3
36	PB3/MTIOC0A/MTIOC4A/TMO0/POE3#/ SCK6/TS22	PB3/MTIOC0A/MTIOC4A/TMO0/POE3#/ LPTO/SCK6*3/TS22*3
37	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD6/ SMOSI6/SSDA6/TS24/IRQ4/CMPOB1	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD6*3/ SMOSI6*3/SSDA6*3/TS24*3/IRQ4/CMPOB1
38	VCC	VCC
39	PB0/MTIC5W/RXD6/SMISO6/SSCL6/ RSPCKA/TS25	PB0/MTIOC3D/MTIC5W/RXD6*3/SMISO6*3/ SSCL6*3/RSPCKA/TS25
40	VSS	VSS
41	PA6/MTIC5V/MTCLKB/TMCI3/POE2#/ CTS5#/RTS5#/SS5#/MOSIA/TS26	PA6/MTIOC3D/MTIC5V/MTCLKB/TMCI3/ POE2#/CTS5#/RTS5#/SS5#/MOSIA/TS26*3
42	PA4/MTIC5U/MTCLKA/TMRI0/TXD5/ SMOSI5/SSDA5/SSLA0/TS28/IRQ5/ CVREFB1	PA4/MTIOC4C/MTIC5U/MTCLKA/TMRI0/ TXD5/SMOSI5/SSDA5/SSLA0/TS28/IRQ5/ CVREFB1
43	PA3/MTIOC0D/MTCLKD/RXD5/SMISO5/ SSCL5/TS29/IRQ6/CMPB1	PA3/MTIOC0D/MTIOC4D/MTIC5V/MTCLKD/ RXD5/SMISO5/SSCL5/TS29/IRQ6/CMPB1
44	PA1/MTIOC0B/MTCLKC/SCK5/SSLA2/TS31	PA1/MTIOC0B/MTIOC3B/MTCLKC/SCK5/ SSLA2/TS31
45	PA0/MTIOC4A/SSLA1/TS32/CACREF	PA0/MTIOC4A/SSLA1/TS32*3/CACREF
46	PE5/MTIOC4C/MTIOC2B/IRQ5/AN021/ CMPOB0	PE5/MTIOC4C/MTIOC2B/IRQ5/AN021/ CMPOB0
47	PE4/MTIOC4D/MTIOC1A/TS33/AN020/ CMPA2/CLKOUT	PE4/MTIOC4D/MTIOC1A/MTIOC4A/TS33/ AN020/CMPA2/CLKOUT
48	PE3/MTIOC4B/POE8#/CTS12#/RTS12#/ SS12#/TS34/AN019/CLKOUT	PE3/MTIOC1B/MTIOC4B/POE8#/CTS12#/ RTS12#/SS12#/TS34/AN019/CLKOUT
49	PE2/MTIOC4A/RXD12/RXDX12/SMISO12/ SSCL12/TS35/IRQ7/AN018/CVREFB0	PE2/MTIOC4A/RXD12/RXDX12/SMISO12/ SSCL12/TS35/IRQ7/AN018/CVREFB0
50	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12/AN017/CMPB0	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12/AN017/CMPB0
51	PE0/SCK12/AN016	PE0/SCK12/AN016
52	P47*1/AN007	P47*1/AN007
53	P46*1/AN006	P46*1/AN006
54	P45*1/AN005	P45*1/AN005
55	P44*1/AN004	P44*1/AN004
56	P43*1/AN003	P43*1/AN003
57	P42*1/AN002	P42*1/AN002
58	P41*1/AN001	P41*1/AN001
59	VREFL0/PJ7*1	VREFL0/PJ7*1
60	P40*1/AN000	P40*1/AN000

64-Pin LFQFP/ LQFP	RX130	RX140
61	VREFH0/PJ6*[1]	VREFH0/PJ6*[1]
62	AVCC0	AVCC0
63	P05*[1]/DA1	P05*[1]/DA1
64	AVSS0	AVSS0/

Notes: 1. The power supply of the I/O buffer for these pins is AVCC0.
2. PC0 and PC1 are valid only when the port switching function is selected.
3. Not implemented on products with ROM capacity of 64 KB.

3.3 48-Pin Package

Table 3.3 is a comparative listing of the pin functions of 48-pin package products.

Table 3.3 Comparative Listing of 48-Pin Package Pin Functions

48-Pin LFQFP/ HWQFN	RX130	RX140
1	VCL	VCL
2	MD/FINED	MD/PG7/FINED
3	RES#	RES#
4	XTAL/P37	XTAL/P37/IRQ4
5	VSS	VSS
6	EXTAL/P36	EXTAL/P36/IRQ2
7	VCC	VCC
8	P35/NMI	P35/NMI
9	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/ TS1/IRQ1	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/ TS1*3/IRQ1
10	P30/MTIOC4B/TMRI3/POE8#/RXD1/ SMISO1/SSCL1/TS2/IRQ0	P30/MTIOC4B/TMRI3/POE8#/RXD1/ SMISO1/SSCL1/TS2*3/IRQ0
11	P27/MTIOC2B/TMCI3/SCK1/TS3	P27/MTIOC2B/TMCI3/SCK1/TS3
12	P26/MTIOC2A/TMO1/TXD1/SMOSI1/ SSDA1/TS4	P26/MTIOC2A/TMO1/LPTO/TXD1/SMOSI1/ SSDA1/TS4
13	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ SCK1/MISOA/SDA0/IRQ7	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ SCK1/MISOA/SDA0/IRQ7
14	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/ SMOSI1/SSDA1/MOSIA/SCL0/IRQ6/ ADTRG0#	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/ SMOSI1/SSDA1/MOSIA/SCL0/IRQ6/ ADTRG0#/RTCOUT
15	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/TS5/IRQ5	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/CRXD0/TS5*3/IRQ5
16	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/TS6/IRQ4	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/CTXD0/TS6*3/IRQ4
17	PH3/TMCI0/TS7	PH3/MTIOC4D/TMCI0/TS7*3
18	PH2/TMRI0/TS8/IRQ1	PH2/MTIOC4C/TMRI0/TS8*3/IRQ1
19	PH1/TMO0/TS9/IRQ0	PH1/MTIOC3D/TMO0/TS9*3/IRQ0
20	PH0/TS10/CACREF	PH0/MTIOC3B/TS10*3/CACREF
21	PC7/MTIOC3A/TMO2/MTCLKB/MISOA/ TS13/CACREF	PC7/MTIOC3A/TMO2/MTCLKB/LPTO/ TXD8*3/SMOSI8*3/SSDA8*3/MISOA/TS13/ CACREF
22	PC6/MTIOC3C/MTCLKA/TMCI2/MOSIA/ TS14	PC6/MTIOC3C/MTCLKA/TMCI2/RXD8*3/ SMISO8*3/SSCL8*3/MOSIA/TS14
23	PC5/MTIOC3B/MTCLKD/TMRI2/RSPCKA/ TS15	PC5/MTIOC0C/MTIOC3B/MTCLKD/TMRI2/ SCK8*3/RSPCKA/TS15
24	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/ SCK5/SSLA0/TSCAP	PC4/MTIOC0A/MTIOC3D/MTCLKC/TMCI1/ POE0#/SCK5/CTS8#*3/RTS8#*3/SS8#*3/ SSLA0/TSCAP
25	PB5/PC3*1/MTIOC2A/MTIOC1B/TMRI1/ POE1#/TS20	PB5/PC3*1/MTIOC2A/MTIOC1B/TMRI1/ POE1#/TS20*3
26	PB3/PC2*1/MTIOC0A/MTIOC4A/TMO0/ POE3#/SCK6/TS22	PB3/PC2*1/MTIOC0A/MTIOC4A/TMO0/ POE3#/LPTO/SCK6*3/TS22*3
27	PB1/PC1*1/MTIOC0C/MTIOC4C/TMCI0/ TXD6/SMOSI6/SSDA6/TS24/IRQ4/CMPOB1	PB1/PC1*1/MTIOC0C/MTIOC4C/TMCI0/ TXD6*3/SMOSI6*3/SSDA6*3/TS24*3/ IRQ4/ CMPOB1
28	VCC	VCC

48-Pin LFQFP/ HWQFN	RX130	RX140
29	PB0/PC0*1/MTIC5W/RXD6/SMISO6/SSCL6/ RSPCKA/TS25	PB0/PC0*1/MTIOC3D/MTIC5W/RXD6*3/ SMISO6*3/SSCL6*3/RSPCKA/TS25
30	VSS	VSS
31	PA6/MTIC5V/MTCLKB/TMCI3/POE2#/ CTS5#/RTS5#/SS5#/MOSIA/TS26	PA6/MTIOC3D/MTIC5V/MTCLKB/TMCI3/ POE2#/CTS5#/RTS5#/SS5#/MOSIA/TS26*3
32	PA4/MTIC5U/MTCLKA/TMRI0/TXD5/ SMOSI5/SSDA5/SSLA0/TS28/IRQ5/ CVREFB1	PA4/MTIOC4C/MTIC5U/MTCLKA/TMRI0/ TXD5/SMOSI5/SSDA5/SSLA0/TS28/IRQ5/ CVREFB1
33	PA3/MTIOC0D/MTCLKD/RXD5/SMISO5/ SSCL5/TS29/IRQ6/CMPB1	PA3/MTIOC0D/MTIOC4D/MTIC5V/MTCLKD/ RXD5/SMISO5/SSCL5/TS29/IRQ6/CMPB1
34	PA1/MTIOC0B/MTCLKC/SCK5/SSLA2/TS31	PA1/MTIOC0B/MTIOC3B/MTCLKC/SCK5/ SSLA2/TS31
35	PE4/MTIOC4D/MTIOC1A/TS33/AN020/ CMPA2/CLKOUT	PE4/MTIOC4D/MTIOC1A/MTIOC4A/TS33/ AN020/CMPA2/CLKOUT
36	PE3/MTIOC4B/POE8#/CTS12#/RTS12#/ TS34/AN019/CLKOUT	PE3/MTIOC1B/MTIOC4B/POE8#/CTS12#/ RTS12#/TS34/AN019/CLKOUT
37	PE2/MTIOC4A/RXD12/RXDX12/SSCL12/ TS35/IRQ7/AN018/CVREFB0	PE2/MTIOC4A/RXD12/RXDX12/SSCL12/ TS35/IRQ7/AN018/CVREFB0
38	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/ SSDA12/AN017/CMPB0	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/ SSDA12/AN017/CMPB0
39	P47*2/AN007	P47*2/AN007
40	P46*2/AN006	P46*2/AN006
41	P45*2/AN005	P45*2/AN005
42	P42*2/AN002	P42*2/AN002
43	P41*2/AN001	P41*2/AN001
44	VREFL0/PJ7*2	VREFL0/PJ7*2
45	P40*2/AN000	P40*2/AN000
46	VREFH0/PJ6*2	VREFH0/PJ6*2
47	AVCC0	AVCC0
48	AVSS0	AVSS0

Notes: 1. PC0 to PC3 are valid only when the port switching function is selected.
2. The power supply of the I/O buffer for these pins is AVCC0.
3. Not implemented on products with ROM capacity of 64 KB.

4. Important Information when Migrating Between MCUs

This section presents important information on differences between the RX140 Group and the RX130 Group. 4.1, Notes on Functional Design, presents information regarding the software.

4.1 Notes on Functional Design

Some software that runs on the RX130 Group is compatible with the RX140 Group. Nevertheless, appropriate caution must be exercised due to differences in aspects such as operation timing and electrical characteristics.

Software-related considerations regarding function settings that differ between the RX140 Group and RX130 Group are as follows:

For differences between modules and functions, refer to 2, Comparative Overview of Specifications. For further information, refer to the User's Manual: Hardware of each MCU group, listed in 5, Reference Documents.

4.1.1 Exception Vector Table

On the RX130 Group the vector table is assigned to a fixed address space, but on the RX140 Group the vector table address can be changed by specifying a value for the start address in the exception table register (EXTB).

4.1.2 Port Direction Register (PDR) Initialization

PDR register initialization differs even between products with the same pin count.

4.1.3 Suppressing Noise on the I^2C Bus Interface

The RX130 Group has integrated analog noise filters for the SCL and SDA lines, but no such integrated analog noise filters are provided on the RX140 Group.

4.1.4 Sampling Interval Setting for Frequency Diffusion

When the frequency diffusion function is turned on (CTSUCRB.SOFF = 0) for the capacitive touch sensing unit of the RX140 Group, set the CTSUCRA.CLK[1:0] and CTSUSO.SDPA[7:0] bits such as that sensor drive pulse sampling interval is less than one-fourth (1/4) the sensor drive pulse interval.

4.1.5 Transmit Pins when Using Self-Capacitance Method

On the RX140 Group, the transmit pins of the capacitive touch sensing unit cannot be used for measurement when using the self-capacitance method. Pulses that are in-phase with the measurement pulses are output on the transmit pins. These should be used as a shield on the board. Also, do not select multiple transmit pins when using the self-capacitance method.

5. Reference Documents

User's Manual: Hardware

RX130 Group User's Manual: Hardware Rev.3.00 (R01UH0560EJ0300)
(The latest version can be downloaded from the Renesas Electronics website.)

RX140 Group User's Manual: Hardware Rev1.10 (R01UH0905EJ0110)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This module reflects the content of the following technical updates:

TN-RX*-A0217A/E

TN-RX*-A0224B/E

TN-RX*-A0227A/E

TN-RX*-A0238B/E

TN-RX*-A0258A/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Aug. 26, 2021	—	First edition issued
1.10	Feb. 21, 2022	13	*Revised:* Table 2.6 Comparison of Clock Generation Circuit Registers
		27	*Revised:* Table 2.19 Comparative Overview of I/O Ports (80-Pin) *Revised:* Table 2.20 Comparative Overview of I/O Ports (64-Pin)
		65	*Revised:* Table 2.46 Comparison of Capacitive Touch Sensing Unit Registers
		77	*Revised:* Table 3.1 Comparative Listing of 80-Pin Package Pin Functions
		80	*Revised:* Table 3.2 Comparative Listing of 64-Pin Package Pin Functions

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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