RX13T Group, RX24T Group

Differences Between the RX13T Group and the RX24T Group

Summary

This application note is intended as a reference to points of difference between the peripheral functions, I/O registers, and pin functions of the RX13T Group and RX24T Group, as well as a guide to key points to consider when migrating between the two groups.

Unless specifically otherwise noted, the information in this application note applies to the 48-pin package version of the RX13T Group and the 100-pin package version of the RX24T Group as the maximum specifications. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the User's Manual: Hardware of the products in question.

Target Devices

RX13T Group and RX24T Group

Contents

1. Comparison of Built-In Functions of RX13T Group and RX24T Group

A comparison of the built-in functions of the RX13T Group and RX24T Group is provided below. For details of the functions, see section 2, Comparative Overview of Specifications and section 4, Reference Documents.

Table 1.1 is a comparison of built-in functions of RX13T Group and RX24T Group.

Table 1.1 Comparison of Built-In Functions of RX13T Group and RX24T Group

Function	RX24T		RX13T
	Chip Version A	Chip Version B	
CPU	■		
Operating modes	○		
Address space	▲		
Resets	○		
Option-setting memory (OFSM)	○		
Voltage detection circuit (LVDAb)	○		
Clock generation circuit	■		
Clock frequency accuracy measurement circuit (CAC)	○		
Low power consumption	▲		
Register write protection function	▲/■		
Exception handling	■		
Interrupt controller (ICUb)	■		
Buses	▲/■		
Memory-protection unit (MPU)	○		×
Data transfer controller (DTCa): RX24T, (DTCb): RX13T	●		
I/O ports	▲		
Multi-function pin controller (MPC)	▲		
Multi-function timer pulse unit 3 (MTU3d): RX24T, (MTU3c): RX13T	■		
Port output enable 3 (POE3b, POE3A): RX24T, (POE3C): RX13T	■		
General PWM timer (GPTB)	×	○	×
8-bit timer (TMR)	○		×
Compare match timer (CMT)	■		
Independent watchdog timer (IWDTa)	○		
Serial communications interface (SCIg): RX24T, (SCIg, SCIh): RX13T	●		
I²C bus interface (RIICa)	×	○	
CAN module (RSCAN)	○		×
Serial peripheral interface (RSPIb)	○		×
CRC calculator (CRC)	○		
12-bit A/D converter (S12ADF): RX24T, (S12ADF): RX13T	■		
D/A converter (DA, DAa): RX24T, D/A converter for generating comparator C reference voltage (DA): RX13T	■		
Comparator C (CMPC)	▲		
Data operation circuit (DOC)	○		
RAM	▲		
Flash memory (FLASH)	▲/■		
Packages	●/■		

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

Notes: 1. On the RX24T Group, chip version A is provided with the POE3b and chip version B with the POE3A.
2. On the RX24T Group, chip version A is provided with the DA and chip version B with the DAa.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Differences in register specifications are not listed.

2.1 CPU

Table 2.1 is a comparative overview of CPU, and Table 2.2 is a comparison of CPU registers.

Table 2.1 Comparative Overview of CPU

Item	RX24T	RX13T
CPU	• Maximum operating frequency: 80 MHz • 32-bit RX CPU (RXv2) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit register • Basic instructions: 75, variable-length instruction format • Floating point instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • ROM cache: 2 KB (disabled by default)	• Maximum operating frequency: 32 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Nine 32-bit registers — Accumulator: One 64-bit registers • Basic instructions: 73, variable-length instruction format • Floating point instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits
FPU	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard

Table 2.2 Comparison of CPU Registers

Register	Bit	RX24T	RX13T
EXTB	—	Exception table register	—
ACC0, ACC1 (RX24T) ACC (RX13T)	—	Accumulator 0, accumulator 1	Accumulator

2.2 Address space

Figure 2.1 is a comparative memory map of single-chip mode.

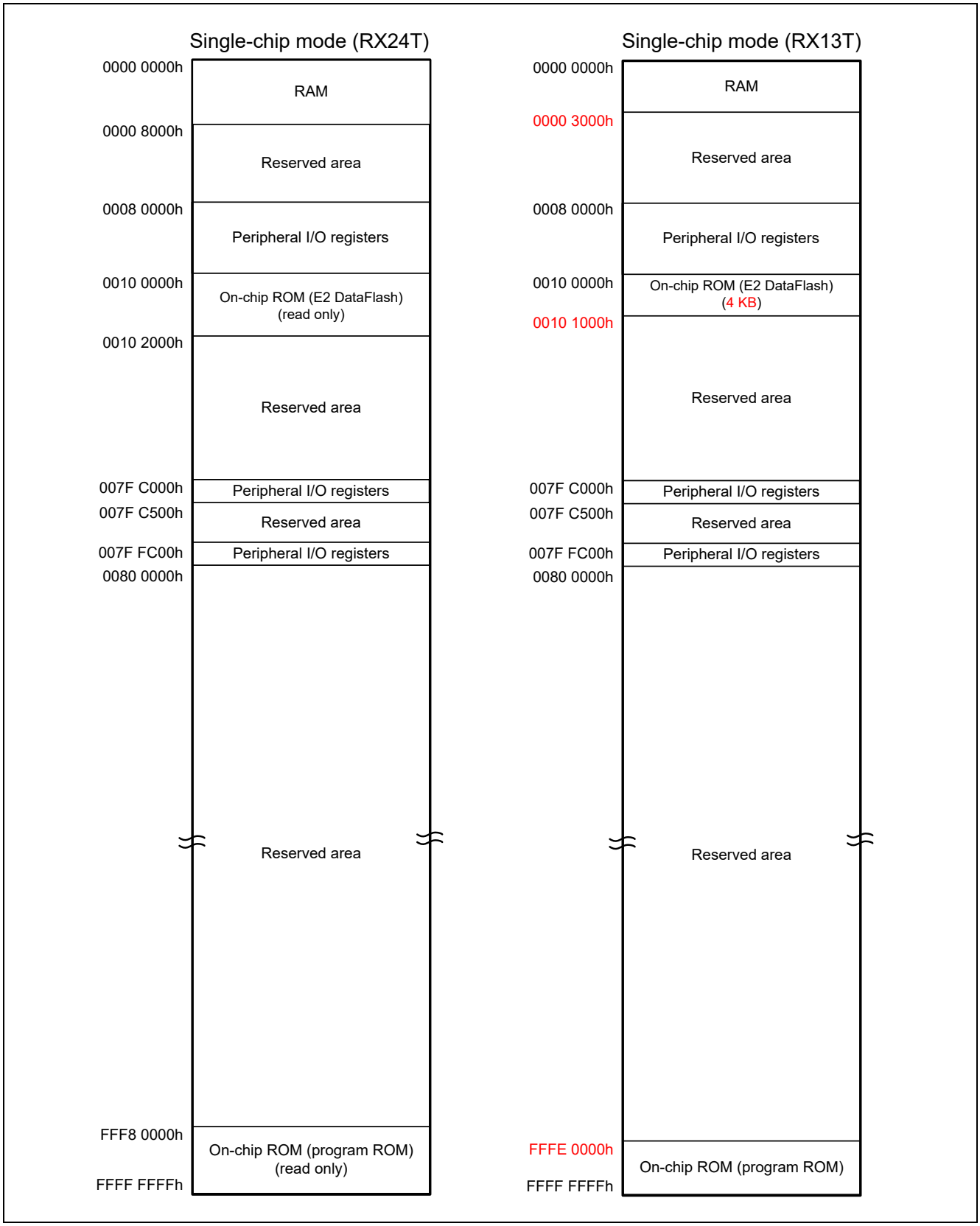

Figure 2.1 Comparative Memory Map of Single-Chip Mode

2.3 Clock Generation Circuit

Table 2.3 is a comparative overview of the clock generation circuits, and Table 2.4 is a comparison of clock generation circuit registers.

Table 2.3 Comparative Overview of Clock Generation Circuits

Item	RX24T	RX13T
Use	• Generates the system clock (ICLK) to be supplied to the CPU, DTC, ROM, and RAM. • Of the peripheral module clocks (PCLKA, PCLKB, and PCLKD) supplied to the peripheral modules, PCLKA is the operating clock for the MTU and GPT, PCLKD is the operating clock for the S12AD, and PCLKB is the operating clock for the other modules. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the CAN clock (CANMCLK) to be supplied to the RSCAN.	• Generates the system clock (ICLK) to be supplied to the CPU, DTC, ROM, and RAM. • Of the peripheral module clocks (PCLKB and PCLKD) supplied to the peripheral modules, PCLKD is the operating clock for the S12AD and PCLKB is the operating clock for the other modules. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.
Operating frequency	• ICLK: 80 MHz (max.) • PCLKA: 80 MHz (max.) • PCLKB: 40 MHz (max.) • PCLKD: 40 MHz (max.) • FCLK: 1 MHz to 32 MHz (ROM) • CACCLK: Same as clock from respective oscillators • IWDTCLK: 15 kHz • CANMCLK: 20 MHz (max.)	• ICLK: 32 MHz (max.)*1 • PCLKB: 32 MHz (max.) • PCLKD: 32 MHz (max.) • FCLK: — 1 MHz to 32 MHz (for programming and erasing the ROM and E2 DataFlash) — 32 MHz (max.) (for reading from the E2 DataFlash) • CACCLK: Same as clock from respective oscillators • IWDTCLK: 15 kHz
Main clock oscillator*2	• Resonator frequency: 1 MHz to 20 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO, and MTU and GPT pin output is stopped. • Drive capacity switching function	• Resonator frequency: 1 MHz to 20 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and MTU pin can be forcedly driven to high-impedance. • Drive capacity switching function

Item	RX24T	RX13T
PLL circuit	• Input clock source: Main clock, and HOCO (32 MHz) clock divided by 4 • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 12.5 MHz • Frequency multiplication ratio: Selectable from 4 to 5.5 (increments of 0.5) • Oscillation frequency: 40 MHz to 80 MHz	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 8 MHz • Frequency multiplication ratio: Selectable from 4 to 8 (increments of 0.5) • Oscillation frequency: 24 MHz to 32 MHz
High-speed on-chip oscillator (HOCO)	Oscillation frequency: 32 MHz, 64 MHz	Oscillation frequency: 32 MHz
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 4 MHz	Oscillation frequency: 4 MHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 15 kHz	Oscillation frequency: 15 kHz

Notes: 1. Make settings such that the division ratios for ICLK:FCLK, ICLK:PCLKB, and ICLK:PCLKD = 1:N (where N is an integer).
2. On the RX13T Group, set the main clock oscillator to 8 MHz or 16 MHz when the PLL is oscillating at 32 MHz.

Table 2.4 Comparison of Clock Generation Circuit Registers

Register	Bit	RX24T	RX13T
SCKCR	—	System clock control register	System clock control register
		The value after a reset differs.	
	PCKA[3:0]	Peripheral module clock A (PCLKA) select bits	—
	—	Reserved bits (b19 to b16) Set the same value as the set value of the PCKB[3:0] bits.	Reserved bits (b19 to b16) These bits are read as 0. The write value should be 0.
PLLCR	PLLSRCSEL	PLL clock source selection bit	—
	STC[5:0]	Frequency multiplication factor select bits b13 b8 0 0 0 1 1 1: ×4 0 0 1 0 0 0: ×4.5 0 0 1 0 0 1: ×5 0 0 1 0 1 0: ×5.5 0 0 1 0 1 1: ×6 0 0 1 1 0 0: ×6.5 0 0 1 1 0 1: ×7 0 0 1 1 1 0: ×7.5 0 0 1 1 1 1: ×8 0 1 0 0 0 0: ×8.5 0 1 0 0 0 1: ×9 0 1 0 0 1 0: ×9.5 0 1 0 0 1 1: ×10 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12 0 1 1 0 0 0: ×12.5 0 1 1 0 0 1: ×13 0 1 1 0 1 0: ×13.5 0 1 1 0 1 1: ×14 0 1 1 1 0 0: ×14.5 0 1 1 1 0 1: ×15 0 1 1 1 1 0: ×15.5 Settings other than the above are prohibited.	Frequency multiplication factor select bits b13 b8 0 0 0 1 1 1: ×4 0 0 1 0 0 0: ×4.5 0 0 1 0 0 1: ×5 0 0 1 0 1 0: ×5.5 0 0 1 0 1 1: ×6 0 0 1 1 0 0: ×6.5 0 0 1 1 0 1: ×7 0 0 1 1 1 0: ×7.5 0 0 1 1 1 1: ×8 Settings other than the above are prohibited.
HOCOCR2	—	High-speed on-chip oscillator control register 2	—
HOCOWTCR	—	High-speed on-chip oscillator wait control register	—
MEMWAIT	—	Main wait cycle setting register	—
LOCOTRR	—	—	Low-speed on-chip oscillator trimming register
ILOCOTRR	—	—	IWDT dedicated on-chip oscillator trimming register
HOCOTRRn	—	—	High-speed on-chip oscillator trimming register n (n = 0)

2.4 Low Power Consumption

Table 2.5 is a comparative overview of the low power consumption functions, and Table 2.6 is a comparison of low power consumption registers.

Table 2.5 Comparative Overview of Low Power Consumption Functions

Item	RX24T	RX13T
Reducing power consumption by switching clock signals	The frequency division ratio can be set independently for the system clock (ICLK), high speed peripheral module clock (PCLKA), peripheral module clock (PCLKB), S12AD clock (PCLKD), and FlashIF clock (FCLK).	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKB), S12AD clock (PCLKD), and FlashIF clock (FCLK).
Module stop function	Each peripheral module can be stopped independently by the module stop control register.	Each peripheral module can be stopped independently by the module stop control register.
Function for transition to low power consumption mode	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.
Low power consumption modes	• Sleep mode • Deep sleep mode • Software standby mode	• Sleep mode • Deep sleep mode • Software standby mode
Function for lower operating power consumption	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Two operating power control modes are available — High-speed operating mode — Middle-speed operating mode	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Two operating power control modes are available — High-speed operating mode — Middle-speed operating mode

Table 2.6 Comparison of Low Power Consumption Registers

Register	Bit	RX24T	RX13T
SBYCR	—	Standby control register	Standby control register
		The value after a reset differs.	
	—	Reserved bit (b14) This bit is read as 1. The write value should be 1.	Reserved bit (b14) This bit is read as 0. The write value should be 0.
MSTPCRA	MSTPA2	8-bit timer 7 and 6 (unit 3) module stop bit	—
	MSTPA3	8-bit timer 5 and 4 (unit 2) module stop bit	—
	MSTPA4	8-bit timer 3 and 2 (unit 1) module stop bit	—
	MSTPA5	8-bit timer 1 and 0 (unit 0) module stop bit	—
	MSTPA7	General PWM timer module stop bit	—
	MSTPA14	Compare match timer 1 (unit 1) module stop bit	—
	MSTPA16	12-bit A/D converter 1 module stop bit	—
	MSTPA23	12-bit A/D converter 2 module stop bit	—
MSTPCRB	MSTPB0	RCAN module stop bit	—
	MSTPB4	—	Serial communication interface SCIh module stop bit
	MSTPB17	Serial peripheral interface 0 module stop bit	—
	MSTPB25	Serial communication interface 6 module stop bit	—

2.5 Register Write Protection Function

Table 2.7 is a comparative overview of the register write protection functions, and Table 2.8 is a comparison of register write protection function registers.

Table 2.7 Comparative Overview of Register Write Protection Functions

Item	RX24T	RX13T
PRC0 bit	Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, OSTDCR, OSTDSR, MEMWAIT	Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, LOCOTRR, ILOCOTRR, HOCOTRR0
PRC1 bit	• Register related to the operating modes: SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR • Registers related to the clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR	• Register related to the operating modes: SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR • Registers related to clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR
PRC2 bit	Registers related to the clock generation circuit: HOCOWTCR	—
PRC3 bit	Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

Table 2.8 Comparison of Register Write Protection Function Registers

Register	Bit	RX24T	RX13T
PRCR	PRC2	Protect bit 2	—

2.6 Exception Handling

Table 2.9 is a comparative overview of exception handling, Table 2.10 is a comparative listing of vectors, and Table 2.11 is a comparative listing of instructions for returning from exception handling routines.

Table 2.9 Comparative Overview of Exception Handling

Item	RX24T	RX13T
Exception events	• Undefined instruction exception • Privileged instruction exception • Access exception • Floating-point exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap	• Undefined instruction exception • Privileged instruction exception • Floating-point exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap

Table 2.10 Comparative Listing of Vectors

Item		RX24T	RX13T
Undefined instruction exception		Exception vector table (EXTB)	Fixed vector table
Privileged instruction exception		Exception vector table (EXTB)	Fixed vector table
Access exception		Exception vector table (EXTB)	—
Floating-point exception		Exception vector table (EXTB)	Fixed vector table
Reset		Exception vector table (EXTB)	Fixed vector table
Non-maskable interrupt		Exception vector table (EXTB)	Fixed vector table
Interrupt	Fast interrupt	FINTV	FINTV
	Other than fast interrupt	Interrupt vector table (INTB)	Relocatable vector table (INTB)
Unconditional trap		Interrupt vector table (INTB)	Relocatable vector table (INTB)

Table 2.11 Comparative Listing of Instructions for Returning from Exception Handling Routines

Item		RX24T	RX13T
Undefined instruction exception		RTE	RTE
Privileged instruction exception		RTE	RTE
Access exception		RTE	—
Floating-point exception		RTE	RTE
Reset		Return not possible	Return not possible
Non-maskable interrupt		Prohibited	Return not possible
Interrupt	Fast interrupt	RTFI	RTFI
	Other than fast interrupt	RTE	RTE
Unconditional trap		RTE	RTE

2.7 Interrupt Controller

Table 2.12 is a comparative overview of interrupt controller, and Table 2.13 is a comparison of interrupt controller registers.

Table 2.12 Comparative Overview of Interrupt Controller

Item		RX24T (ICUb)	RX13T (ICUb)
Interrupt	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection Edge detection or level detection is fixed for each source of connected peripheral modules	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection Edge detection or level detection is fixed for each source of connected peripheral modules
	External pin interrupts	• Interrupts from pins IRQ0 to IRQ7 • Number of sources: 8 • Interrupt detection: Low level/falling edge/rising edge/rising and falling edges. One of these detection methods can be set for each source. • Digital filter function: Supported	• Interrupts from pins IRQ0 to IRQ5 • Number of sources: 6 • Interrupt detection: Low level/falling edge/rising edge/rising and falling edges. One of these detection methods can be set for each source. • Digital filter function: Supported
	Software interrupt	• Interrupt generated by writing to a register. • One interrupt source	• Interrupt generated by writing to a register. • One interrupt source
	Interrupt priority level	Specified by registers.	Specified by registers.
	Fast interrupt function	Faster interrupt processing of the CPU can be set only for a single interrupt source.	Faster interrupt processing of the CPU can be set only for a single interrupt source.
	DTC control	The DTC can be activated by interrupt sources.	The DTC can be activated by interrupt sources.
Non-maskable interrupts	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter function: Supported	• Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter function: Supported
	Oscillation stop detection interrupt	Interrupt on detection of oscillation having stopped	Interrupt on detection of oscillation having stopped
	IWDT underflow/ refresh error interrupt	Interrupt on an underflow of the down counter or occurrence of a refresh error	Interrupt on an underflow of the down counter or occurrence of a refresh error
	Voltage monitoring 1 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)

Item	RX24T (ICUb)	RX13T (ICUb)
Return from low power consumption modes	• Sleep mode, deep sleep mode: Return is initiated by non-maskable interrupts or any other interrupt source. • Software standby mode: Return is initiated by non-maskable interrupts and interrupts IRQ0 to IRQ7	• Sleep mode, deep sleep mode: Return is initiated by non-maskable interrupts or any other interrupt source. • Software standby mode: Return is initiated by non-maskable interrupts and interrupts IRQ0 to IRQ5.

Table 2.13 Comparison of Interrupt Controller Registers

Register	Bit	RX24T (ICUb)	RX13T (ICUb)
IRn*1	—	Interrupt request register n (n = 016 to 249)	Interrupt request register n (n = 016 to 255)
IPRn*1	—	Interrupt source priority register n (n = 000 to 249)	Interrupt source priority register n (n = 000 to 255)
DTCERn*1	—	DTC transfer request enable register n (n = 027 to 248)	DTC activation enable register n (n = 027 to 255)
IRQCRi	—	IRQ control register i (i = 0 to 7)	IRQ control register i (i = 0 to 5)
IRQFLTE0	FLTEN6	IRQ6 digital filter enable bit	—
	FLTEN7	IRQ7 digital filter enable bit	—
IRQFLTC0	FCLKSEL6 [1:0]	IRQ6 digital filter sampling clock setting bits	—
	FCLKSEL7 [1:0]	IRQ7 digital filter sampling clock setting bits	—

Note: 1. On both the RX24T Group and RX13T Group n = 250 to 255 are reserved areas.

2.8 Buses

Table 2.14 is a comparative overview of the buses, and Table 2.15 is a comparison of bus registers.

Table 2.14 Comparative Overview of Buses

Bus Type		RX24T	RX13T
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	Connected to RAM	Connected to RAM
	Memory bus 2	Connected to ROM	Connected to ROM
Internal main buses	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, and 4) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules • Operates in synchronization with the peripheral-module clock (PCLKB, PCLKD)
	Internal peripheral bus 3	• Connected to peripheral modules (RSCAN, CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 4	• Connected to peripheral modules (MTU, GPT) • Operates in synchronization with the peripheral-module clock (PCLKA)	—

Bus Type		RX24T	RX13T
Internal peripheral buses	Internal peripheral bus 6	• Connected to the flash control module and E2 DataFlash memory • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to ROM (P/E) and E2 DataFlash • Operates in synchronization with the FlashIF clock (FCLK)

Table 2.15 Comparison of Bus Registers

Register	Bit	RX24T	RX13T
BUSPRI	BPHB[1:0]	Internal peripheral bus 4 priority control bits	—

2.9 Data Transfer Controller

Table 2.16 is a comparative overview of the data transfer controllers, and Table 2.17 is a comparison of data transfer controller registers.

Table 2.16 Comparative Overview of Data Transfer Controllers

Item	RX24T (DTCa)	RX13T (DTCb)
Number of transfer channels	Equal to number of all interrupt sources that can start a DTC transfer.	Equal to number of all interrupt sources that can start a DTC transfer.
Transfer modes	• Normal transfer mode — A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address returns to the transfer start address when the number of data transfers equals the repeat size. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, or 1,024 bytes. • Block transfer mode — A single activation leads to the transfer of a single block of data. — The maximum block size is 256 × 32 bits = 1,024 bytes.	• Normal transfer mode — A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address returns to the transfer start address when the number of data transfers equals the repeat size. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, or 1,024 bytes. • Block transfer mode — A single activation leads to the transfer of a single block of data. — The maximum block size is 256 × 32 bits = 1,024 bytes.
Chain transfer function	• Multiple data transfer types can be executed sequentially in response to a single transfer request. • Either “performed only when the transfer counter reaches 0” or “every time” can be selected.	• Multiple data transfer types can be executed sequentially in response to a single transfer request. • Either “performed only when the transfer counter reaches 0” or “every time” can be selected.
Sequence transfer	—	A complex series of transfers can be registered as a sequence. Any sequence can be selected by the transfer data and executed. • Only one sequence transfer trigger source can be selected at a time. • Up to 256 sequences can correspond to a single trigger source. • The data that is initially transferred in response to a transfer request determines the sequence. • The entire sequence can be executed on a single request, or the sequence can be suspended in the middle and resumed on the next transfer request (sequence division).

Item	RX24T (DTCa)	RX13T (DTCb)
Transfer space	• 16 MB in short-address mode (within 0000 0000h to 007F FFFFh or FF80 0000h to FFFF FFFFh, excluding reserved areas) • 4 GB in full-address mode (within 0000 0000h to FFFF FFFFh, excluding reserved areas)	• 16 MB in short-address mode (within 0000 0000h to 007F FFFFh or FF80 0000h to FFFF FFFFh, excluding reserved areas) • 4 GB in full-address mode (within 0000 0000h to FFFF FFFFh, excluding reserved areas)
Data transfer units	• Single data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data units	• Single data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data units
CPU interrupt sources	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.
Read skip	Reading of the transfer information can be skipped when the same transfer is repeated.	Reading of the transfer information can be skipped when the same transfer is repeated.
Write-back skip	Write-back of transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.	Write-back of transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.
Write-back disable	—	Ability to disable write-back of transfer information
Displacement addition	—	Ability to add displacement to the transfer source address (selectable by each transfer information)
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Table 2.17 Comparison of Data Transfer Controller Registers

Register	Bit	RX24T (DTCa)	RX13T (DTCb)
MRA	WBDIS	—	Write-back disable bit
MRB	SQEND	—	Sequence transfer end bit
	INDX	—	Index table reference bit
MRC	—	—	DTC mode register C
DTCIBR	—	—	DTC index table base register
DTCOR	—	—	DTC operation register
DTCSQE	—	—	DTC sequence transfer enable register
DTCDISP	—	—	DTC address displacement register

2.10 I/O Ports

Table 2.18 is a comparative overview of the I/O ports (RX24T: 64-pin products, RX13T: 48-pin products), Table 2.19 is a comparative overview of the I/O ports (RX24T: 64-pin products, RX13T: 32-pin products), Table 2.20 is a comparison of I/O port functions, and Table 2.21 is a comparison of I/O port registers.

Table 2.18 Comparative Overview of I/O Ports (RX24T: 64-Pin Products, RX13T: 48-Pin Products)

Port Symbol	RX24T (64-Pin)	RX13T (48-Pin)
PORT0	P00 to P02	—
PORT1	P11	P10, P11
PORT2	P21 to P24	P22 to P24
PORT3	P30, P31, P36, P37	P36, P37
PORT4	P40 to P42, P44 to P46	P40 to P47
PORT5	P50 to P54	—
PORT7	P70 to P76	P70 to P76
PORT9	P90 to P96	P93, P94
PORTA	—	PA2, PA3
PORTB	PB1 to PB6	PB0 to PB7
PORTD	PD3 to PD7	PD3 to PD6
PORTE	PE2	PE2

Table 2.19 Comparative Overview of I/O Ports (RX24T: 64-Pin Products, RX13T: 32-Pin Products)

Port Symbol	RX24T (64-Pin)	RX13T (32-Pin)
PORT0	P00 to P02	—
PORT1	P11	P11
PORT2	P21 to P24	—
PORT3	P30, P31, P36, P37	P36, P37
PORT4	P40 to P42, P44 to P46	P40 to P44
PORT5	P50 to P54	—
PORT7	P70 to P76	P71 to P76
PORT9	P90 to P96	P93, P94
PORTB	PB1 to PB6	PB0 to PB3, PB6, PB7
PORTD	PD3 to PD7	—
PORTE	PE2	PE2

Table 2.20 Comparison of I/O Port Functions

Item	Port Symbol	RX24T	RX13T
Input pull-up function	PORT0	P00 to P02	—
	PORT1	P10, P11	P10, P11
	PORT2	P20 to P24	P22 to P24
	PORT3	P30 to P33, P36, P37	P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P55	—
	PORT6	P60 to P65	—
	PORT7	P70 to P76	P70 to P76
	PORT8	P80, P81, P82	—
	PORT9	P90 to P96	P93, P94
	PORTA	PA0 to PA5	PA2, PA3
	PORTB	PB0 to PB7	PB0 to PB7
	PORTD	PD0 to PD7	PD3 to PD6
	PORTE	PE0, PE1, PE3 to PE5	—
Open-drain output function	PORT0	P00 to P02	—
	PORT1	P10, P11	P10, P11
	PORT2	P20 to P24	P22 to P24
	PORT3	P30 to P33, P36, P37	P36, P37
	PORT7	P70 to P76	P70 to P76
	PORT8	P80, P81, P82	—
	PORT9	P90 to P96	P93, P94
	PORTA	PA0 to PA5	PA2, PA3
	PORTB	PB0 to PB7	PB0 to PB7
	PORTD	PD0 to PD7	PD3 to PD6
	PORTE	PE0, PE1, PE3 to PE5	—
Drive capacity switching function	PORT0	P00 to P02	—
	PORT1	P10, P11	P10, P11
	PORT2	P20 to P24	P22 to P24
	PORT3	P30 to P33, P36, P37	—
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P55	—
	PORT6	P60 to P65	—
	PORT7	P70 to P76	P70 to P76
	PORT8	P80 to P82	—
	PORT9	P90 to P96	P93, P94
	PORTA	PA0 to PA5	PA2, PA3
	PORTB	PB0 to PB7	PB0 to PB7
	PORTD	PD0 to PD7	PD3 to PD6
	PORTE	PE0, PE1, PE3 to PE5	—
5 V tolerant	PORTB	PB1, PB2	PB1, PB2

Table 2.21 Comparison of I/O Port Registers

Register	Bit	RX24T	RX13T
PDR	B0 to B7	Pm0 to Pm7 I/O select bits (m = 0 to 9, A, B, D, E)	Pm0 to Pm7 I/O select bits (m = 1 to 4, 7, 9, A, B, D)
PODR	B0 to B7	Pm0 to Pm7 output data store bits (m = 0 to 9, A, B, D, E)	Pm0 to Pm7 output data store bits (m = 1 to 4, 7, 9, A, B, D)
PIDR	B0 to B7	Pm0 to Pm7 bits (m = 0 to 9, A, B, D, E)	Pm0 to Pm7 bits (m = 1 to 4, 7, 9, A, B, D)
PMR	B0 to B7	Pm0 pin mode control bits (m = 0 to 3, 7, 9, A, B, D, E)	Pm0 to Pm7 pin mode control bits (m = 1 to 3, 7, 9, A, B, D, E)
ODR0	B0 (RX24T) B0, B1 (RX13T)	Pm0 output type select bit (m = 0 to 3, 7 to 9, A, B, D, E) 0: CMOS output 1: N-channel open-drain	Pm0 output type select bit (m = 1, 2, 7, 9, A, B, D) • P10, P70 b0 0: CMOS output 1: N-channel open-drain b1 This bit is read as 0. The write value should be 0. • PB0 b1 b0 0 0: CMOS output 0 1: N-channel open-drain 1 0: P-channel open-drain 1 1: Hi-Z
	B2, B4, B6	Pm1 to Pm3 output type select bits (m = 0 to 3, 7 to 9, A, B, D, E)	Pm1 to Pm3 output type select bits (m = 1, 2, 7, 9, A, B, D)
ODR1	B0, B2, B4, B6	Pm4 to Pm7 output type select bits (m = 2, 7, 9, A, B, D, E)	Pm4 to Pm7 output type select bits (m = 2, 3, 7, 9, B, D)
PCR	B0 to B7	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A, B, D, E)	Pm0 to Pm7 input pull-up resistor control bits (m = 1 to 4, 7, 9, A, B, D)
DSCR	B0 to B7	Pm0 to Pm7 drive capacity control bits (m = 0 to 3, 7 to 9, A, B, D, E)	Pm0 to Pm7 drive capacity control bits (m = 1, 2, 7, 9, A, B, D)

2.11 Multi-Function Pin Controller

Table 2.22 is a comparison of the assignments of multiplexed pins, and Table 2.23 to Table 2.36 are comparisons of multi-function pin controller registers.

In the following comparison of the assignments of multiplexed pins, **light blue text** designates pins that exist on the RX13T Group only and **orange text** pins that exist on the RX24T Group only. A circle (○) indicates that a function is assigned, a cross (×) that the pin does not exist or that no function is assigned, and grayed out items mean that the function is not implemented.

Table 2.22 Comparison of Multiplexed Pin Assignments

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)	RX13T (MPC)	
			64-Pin	48-Pin	32-Pin
Interrupt	NMI (input)	PE2	○	○	○
	IRQ0 (input)	P10	×	○	×
		P93	×	○	○
		PE2	×	○	○
		P52	○	×	×
	IRQ1 (input)	P11	○	○	○
		P94	×	○	○
		P53	○	×	×
	IRQ2 (input)	P22	×	○	×
		PB1	×	○	○
		PD4	○	○	×
		P00	○	×	×
		P54	○	×	×
	IRQ3 (input)	P24	×	○	×
		PB4	○	○	×
		PD5	○	○	×
	IRQ4 (input)	P23	×	○	×
		PA2	×	○	×
		P01	○	×	×
		P96	○	×	×
	IRQ5 (input)	P70	○	○	×
		PB7	×	○	○
		PD6	○	○	×
		P02	○	×	×
		PB6	○	×	×
	IRQ6 (input)	P21	○		
		P31	○		
	IRQ7 (input)	P30	○		
Multi-function timer unit 3	MTIOC0A (input/output)/ MTIOC0A# (input/output)	PB3	○	○	○
		PD3	×	○	×
		P31	○	×	×
	MTIOC0B (input/output)/ MTIOC0B# (input/output)	PB2	○	○	○
		PD4	×	○	×
		P30	○	×	×
	MTIOC0C (input/output)/ MTIOC0C# (input/output)	PB1	○	○	○
		PD5	×	○	×
	MTIOC0D (input/output)	PB0	×*1	○	○
		PD6	×*1	○	×

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)	RX13T (MPC)	
			64-Pin	48-Pin	32-Pin
Multi-function timer unit 3	MTIOC1A (input/output)	P93	×*1	○	○
		PA2	×*1	○	×
	MTIOC1B (input/output)	PA3	×*1	○	×
		PB6	×*1	○	○
	MTIOC2A (input/output)	PA3	×*1	○	×
		PB0	×*1	○	○
	MTIOC2B (input/output)	PA2	×*1	○	×
		P94	×*1	○	○
	MTIOC3A (input/output)/ MTIOC3A# (input/output)	P11	○	○	○
		PB6	×	○	○
	MTIOC3B (input/output)/ MTIOC3B# (input/output)	P71	○	○	○
	MTIOC3C (input/output)	PB7	×*1	○	○
	MTIOC3D (input/output)/ MTIOC3D# (input/output)	P74	○	○	○
	MTIOC4A (input/output)/ MTIOC4A# (input/output)	P72	○	○	○
	MTIOC4B (input/output)/ MTIOC4B# (input/output)	P73	○	○	○
	MTIOC4C (input/output)/ MTIOC4C# (input/output)	P75	○	○	○
	MTIOC4D (input/output)/ MTIOC4D# (input/output)	P76	○	○	○
	MTIC5U (input)/ MTIC5U# (input)	P24	○	○	×
		P94	×	○	○
	MTIC5V (input)/ MTIC5V# (input)	P23	○	○	×
		P93	×	○	○
	MTIC5W (input)/ MTIC5W# (input)	P22	○	○	×
		PB1	×	○	○
	MTIOC6B (input/output)/ MTIOC6B# (input/output)	P95	○		
	MTIOC6D (input/output)/ MTIOC6D# (input/output)	P92	○		
	MTIOC7A (input/output)/ MTIOC7A# (input/output)	P94	○		
	MTIOC7B (input/output)/ MTIOC7B# (input/output)	P93	○		
	MTIOC7C (input/output)/ MTIOC7C# (input/output)	P91	○		
	MTIOC7D (input/output)/ MTIOC7D# (input/output)	P90	○		
	MTIOC9A (input/output)/ MTIOC9A# (input/output)	P21	○		
		PD7	○		
		PD6	○		
	MTIOC9D (input/output)/ MTIOC9D# (input/output)	P02	○		
	MTCLKA (input)/ MTCLKA# (input)	P11	×	○	○
		P94	×	○	○
		PB1	×	○	○
		P21	○	×	×

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)	RX13T (MPC)	
			64-Pin	48-Pin	32-Pin
Multi-function timer unit 3	MTCLKB (input)	P10	×*1	○	×
		PB0	×*1	○	○
	MTCLKC (input)/ MTCLKC# (input)	PB2	×	○	○
		P11	○	×	×
		P31	○	×	×
	MTCLKD (input)/ MTCLKD# (input)	PB7	×	○	○
		P30	○	×	×
	ADSM0 (output)	PB2	○	○	○
	ADSM1 (output)	PB1	○		
8-bit timer	TMO0 (output)	PD3	○		
	TMCI0 (input)	PD4	○		
		PB1	○		
	TMRI0 (input)	PD5	○		
		PB2	○		
	TMO1 (output)	PD6	○		
	TMRI1 (input)	PD7	○		
	TMO2 (output)	P23	○		
	TMCI2 (input)	P24	○		
	TMRI2 (input)	P22	○		
	TMO3 (output)	P11	○		
	TMO4 (output)	P22	○		
	TMCI4 (input)	P21	○		
	TMRI5 (input)	PD7	○		
	TMO6 (output)	P24	○		
	TMCI6 (input)	P30	○		
		PD4	○		
	TMRI6 (input)	P31	○		
		PD5	○		
Port output enable 3	POE0# (input)	P70	○	○	×
	POE4# (input)	P96	○		
	POE8# (input)	PB4	○	○	×
		P11	×	○	○
	POE10# (input)	PE2	○	○	○
	POE12# (input)	P01	○		
Serial communications interface	RXD1 (input)/ SMISO1 (input/output)/ SSCL1 (input/output)	PD5	○	○	×
		PB7	×	○	○
	TXD1 (output)/ SMOSI1 (input/output)/ SSDA1 (input/output)	PD3	○	○	×
		PB6	×	○	○
	SCK1 (input/output)	PD4	○	○	×
	CTS1# (input)/ RTS1# (output)/ SS1# (input)	PD6	○	○	×
		P02	○	×	×
	RXD5 (input)/ SMISO5 (input/output)/ SSCL5 (input/output)	PB1	×	○	○
		PB7	×	○	○
		P24	×	○	×
		PB6	○	×	×

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)	RX13T (MPC)	
			64-Pin	48-Pin	32-Pin
Serial communications interface	TXD5 (output)/ SMOSI5 (input/output)/ SSDA5 (input/output)	PB2	×	○	○
		PB6	×	○	○
		P23	×	○	×
		PB5	○	×	×
	SCK5 (input/output)	P93	×*1	○	○
		PB3	×*1	○	○
	CTS5# (input)/ RTS5# (output)/ SS5# (input)	PA2	×	○	×
		PB4	○	×	×
	RXD6 (input)/ SMISO6 (input/output)	PB1	○		
	TXD6 (output)/ SMOSI6 (input/output)	PB2	○		
	SCK6 (input/output)	PB3	○		
	RXD12 (input)/ SMISO12 (input/output)/ SSCL12 (input/output)/ RXDX12 (input)	P94		○	○
	TXD12 (output)/ SMOSI12 (input/output)/ SSDA12 (input/output)/ TXDX12 (output)/ SIOX12 (input/output)	PB0		○	○
	SCK12 (input/output)	PB3		○	○
		P93		○	○
	CTS12# (input)/ RTS12# (output)/ SS12# (input)	PA3		○	×
I²C bus interface	SCL0 (input/output)	PB1	○	○	○
	SDA0 (input/output)	PB2	○	○	○
Serial peripheral interface	RSPCKA (input/output)	P24	○		
		PB3	○		
	MOSIA (input/output)	P23	○		
	MISOA (input/output)	P22	○		
	SSLA0 (input/output)	P30	○		
		PD6	○		
	SSLA1 (output)	P31	○		
		PD7	○		
12-bit A/D converter	AN000 (input)	P40	○	○	○
	AN001 (input)	P41	○	○	○
	AN002 (input)	P42	○	○	○
	AN003 (input)	P43	×*1	○	○
	AN004 (input)	P44		○	○
	AN005 (input)	P45	×	○	×
	AN006 (input)	P46	×	○	×
	AN007 (input)	P47	×	○	×
	AN100 (input)	P44	○		
	AN101 (input)	P45	○		
	AN102 (input)	P46	○		
	AN116 (input)	P21	○		

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)	RX13T (MPC)	
			64-Pin	48-Pin	32-Pin
12-bit A/D converter	AN206 (input)	P50	○		
	AN207 (input)	P51	○		
	AN208 (input)	P52	○		
	AN209 (input)	P53	○		
	AN210 (input)	P54	○		
	ADTRG0# (input)	P93	×*1	○	○
		PB5	×*1	○	×
	ADTRG1# (input)	P21	○		
	ADTRG2# (input)	P22	○		
	ADST0 (output)	PD6	○	○	×
		P02	○	×	×
	ADST1 (output)	P00	○		
	ADST2 (output)	P01	○		
Clock frequency accuracy measurement circuit	CACREF (input)	P23	○	○	×
		PB3	○	○	○
Comparator	CMPC00 (input)	P40	○	○	○
	CMPC01 (input)	P40	○		
	CMPC02 (input)	P43	×	○	○
		P45	○	×	×
	CMPC03 (input)	P46	×	○	×
		P45	○	×	×
	CMPC10 (input)	P41	×	○	○
		P44	○	×	×
	CMPC11 (input)	P44	○		
	CMPC12 (input)	P44	×	○	○
		P46	○	×	×
	CMPC13 (input)	P47	×	○	×
		P46	○	×	×
	CMPC20 (input)	P42	×	○	○
		P45	○	×	×
	CMPC21 (input)	P45	○		
	CMPC22 (input)	P45	×	○	×
		P40	○	×	×
	CMPC23 (input)	P40	○		
	CMPC30 (input)	P46	○		
	CMPC31 (input)	P46	○		
	CMPC32 (input)	P44	○		
	CMPC33 (input)	P44	○		
	COMP0 (output)	P24	○	○	×
	COMP1 (output)	P23	○	○	×
	COMP2 (output)	P22	○	○	×
	COMP3 (output)	P30	○		
	CVREFC0 (input)	P11	×*1	○	○
	CVREFC1 (input)	P21	○	×	×

Note: 1. This function is not available on 64-pin package products in the RX24T Group.

Table 2.23 Comparison of P0n Pin Function Control Register (P0nPFS)

Register	Bit	RX24T	RX13T
P0nPFS	—	P0n pin function control register (n = 0 to 2)	—

Table 2.24 Comparison of P1n Pin Function Control Register (P1nPFS)

Register	Bit	RX24T (n = 0, 1)		RX13T (n = 0, 1)
		Chip Version A	Chip Version B	
P10PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9B 00010b: MTCLKD 00101b: TMRI3 00111b: POE12# 01010b: CTS6#/RTS6#/SS6#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9B 00010b: MTCLKD 00011b: MTIOC9B# 00100b: MTCLKD# 00101b: TMRI3 00111b: POE12# 01010b: CTS6#/RTS6#/SS6#	Pin function select bits b4 b0 00000b: Hi-Z 00010b: MTCLKB
P11PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKC 00101b: TMO3	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKC 00011b: MTIOC3A# 00100b: MTCLKC# 00101b: TMO3	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKA 00111b: POE8#
P1nPFS	ASEL	—	—	Analog input function select bit

Table 2.25 Comparison of P2n Pin Function Control Register (P2nPFS)

Register	Bit	RX24T (n = 0 to 4)		RX13T (n = 2 to 4)
		Chip Version A	Chip Version B	
P20PFS	—	P20 pin function control register	P20 pin function control register	—
P21PFS	—	P21 pin function control register	P21 pin function control register	—
P22PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5W 00101b: TMRI2 00110b: TMO4 01001b: ADTRG2# 01101b: MISOA 11110b: COMP2	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5W 00011b: MTIC5W# 00101b: TMRI2 00110b: TMO4 01001b: ADTRG2# 01101b: MISOA 11110b: COMP2	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5W 11110b: COMP2

Register	Bit	RX24T (n = 0 to 4)		RX13T (n = 2 to 4)
		Chip Version A	Chip Version B	
P23PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5V 00101b: TMO2 00111b: CACREF 01101b: MOSIA 11110b: COMP1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5V 00011b: MTIC5V# 00101b: TMO2 00111b: CACREF 01101b: MOSIA 11110b: COMP1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5V 00111b: CACREF 01010b: TXD5/ SMOSI5/ SSDA5 11110b: COMP1
P24PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5U 00101b: TMCI2 00110b: TMO6 01101b: RSPCKA 11110b: COMP0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5U 00011b: MTIC5U# 00101b: TMCI2 00110b: TMO6 01101b: RSPCKA 11110b: COMP0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5U 01010b: RXD5/ SMISO5/ SSCL5 11110b: COMP0
P2nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P20: IRQ7 (100/80-pin) P21: IRQ6 (100/80/64-pin)		Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P22: IRQ2 (48-pin) P23: IRQ4 (48-pin) P24: IRQ3 (48-pin)
	ASEL	Analog pin function select bit	Analog pin function select bit	—

Table 2.26 Comparison of P3n Pin Function Control Register (P3nPFS)

Register	Bit	RX24T	RX13T
P3nPFS	—	P3 pin function control register 0 (n = 0 to 3)	—

Table 2.27 Comparison of P4n Pin Function Control Register (P4nPFS)

Register	Bit	RX24T (n = 0 to 7)	RX13T (n = 0 to 7)
P4nPFS	ASEL	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin P40: AN000, CMPC00, CMPC01, CMPC22, CMPC23 (100/80/64-pin) P41: AN001 (100/80/64-pin) P42: AN002 (100/80/64-pin) P43: AN003 (100/80-pin) P44: AN100, CMPC10, CMPC11, CMPC32, CMPC33 (100/80/64-pin) P45: AN101, CMPC02, CMPC03, CMPC20, CMPC21 (100/80/64-pin) P46: AN102, CMPC12, CMPC13, CMPC30, CMPC31 (100/80/64-pin) P47: AN103 (100/80-pin)	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin P40: AN000/CMPC00 (48/32-pin) P41: AN001/CMPC10 (48/32-pin) P42: AN002/CMPC20 (48/32-pin) P43: AN003/CMPC02 (48/32-pin) P44: AN004/CMPC12 (48/32-pin) P45: AN005/CMPC22 (48-pin) P46: AN006/CMPC03 (48-pin) P47: AN007/CMPC13 (48-pin)

Table 2.28 Comparison of P5n Pin Function Control Register (P5nPFS)

Register	Bit	RX24T	RX13T
P5nPFS	—	P5 pin function select register (n = 0 to 5)	—

Table 2.29 Comparison of P6n Pin Function Control Register (P6nPFS)

Register	Bit	RX24T	RX13T
P6nPFS	—	P6 pin function select register (n = 0 to 5)	—

Table 2.30 Comparison of P7n Pin Function Control Register (P7nPFS)

Register	Bit	RX24T (n = 0 to 6)		RX13T (n = 0 to 6)
		Chip Version A	Chip Version B	
P70PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00111b: POE0#	Pin function select bits b4 b0 00000b: Hi-Z 00111b: POE0#	Pin function select bits b4 b0 00000b: Hi-Z 00111b: POE0#
P71PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3B	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3B 00011b: MTIOC3B# 10100b: GTIOC0A 10110b: GTIOC0A#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3B

Register	Bit	RX24T (n = 0 to 6)		RX13T (n = 0 to 6)
		Chip Version A	Chip Version B	
P72PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4A	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4A 00011b: MTIOC4A# 10100b: GTIOC1A 10110b: GTIOC1A#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4A
P73PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4B	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4B 00011b: MTIOC4B# 10100b: GTIOC2A 10110b: GTIOC2A#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4B
P74PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3D	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3D 00011b: MTIOC3D# 10100b: GTIOC0B 10110b: GTIOC0B#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3D
P75PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4C	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4C 00011b: MTIOC4C# 10100b: GTIOC1B 10110b: GTIOC1B#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4C
P76PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4D	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4D 00011b: MTIOC4D# 10100b: GTIOC2B 10110b: GTIOC2B#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4D

Table 2.31 Comparison of P8n Pin Function Control Register (P8nPFS)

Register	Bit	RX24T	RX13T
P8nPFS	—	P8 pin function select register (n = 0 to 2)	—

Table 2.32 Comparison of P9n Pin Function Control Register (P9nPFS)

Register	Bit	RX24T (n = 0 to 6)		RX13T (n = 3, 4)
		Chip Version A	Chip Version B	
P90PFS	—	P90 pin function control register		—
P91PFS	—	P91 pin function control register		—
P92PFS	—	P92 pin function control register		—
P93PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC7B	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC7B 00011b: MTIOC7B#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC1A 00011b: MTIC5V 01001b: ADTRG0# 01010b: SCK5 01100b: SCK12
P94PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC7A	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC7A 00011b: MTIOC7A#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC2B 00010b: MTCLKA 00011b: MTIC5U 01100b: RXD12/ SMISO12/ SSCL12/ RXDX12
P95PFS	—	P95 pin function control register		—
P96PFS	—	P96 pin function control register		—
P9nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P96: IRQ4 (100/80/64-pin)		Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P93: IRQ0 (48/32-pin) P94: IRQ1 (48/32-pin)

Table 2.33 Comparison of PAn Pin Function Control Register (PAnPFS)

Register	Bit	RX24T (n = 0 to 5)		RX13T (n = 2, 3)
		Chip Version A	Chip Version B	
PA0PFS	—	PA0 pin function control register		—
PA1PFS	—	PA1 pin function control register		—
PA2PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC2B 00101b: TMO7 01010b: CTS6#/ RTS6#/SS6# 01101b: SSLA1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC2B 00010b: MTIOC2B# 00101b: TMO7 01010b: CTS6#/ RTS6#/SS6# 01101b: SSLA1 10100b: GTADSM1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC1A 00011b: MTIOC2B 01010b: CTS5#/ RTS5#/SS5#
PA3PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC2A 00101b: TMRI7 01101b: SSLA0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC2A 00010b: MTIOC2A# 00101b: TMRI7 01101b: SSLA0 10100b: GTADSM0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC1B 00011b: MTIOC2A 01100b: CTS12#/ RTS12#/ SS12#
PA4PFS	—	PA4 pin function control register		—
PA5PFS	—	PA5 pin function control register		—
PAnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA5: IRQ1 (100/80-pin)		Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA2: IRQ4 (48-pin)

Table 2.34 Comparison of PBn Pin Function Control Register (PBnPFS)

Register	Bit	RX24T (n = 0 to 7)		RX13T (n = 0 to 7)
		Chip Version A	Chip Version B	
PB0PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0D 00101b: TMO0 01001b: ADTRG2# 01010b: TXD6/ SMOSI6/ SSDA6 01101b: MOSIA	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0D 00011b: MTIOC0D# 00101b: TMO0 01001b: ADTRG2# 01010b: TXD6/ SMOSI6/ SSDA6 01101b: MOSIA	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0D 00010b: MTCLKB 00011b: MTIOC2A 01100b: TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12
PB1PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0C 00101b: TMCI0 01001b: ADSM1 01010b: RXD6/ SMISO6/ SSCL6 01111b: SCL0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0C 00011b: MTIOC0C# 00101b: TMCI0 01001b: ADSM1 01010b: RXD6/ SMISO6/ SSCL6 01111b: SCL0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0C 00010b: MTCLKA 00011b: MTIC5W 01010b: RXD5/ SMISO5/ SSCL5 01111b: SCL0
PB2PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0B 00101b: TMRI0 01001b: ADSM0 01010b: TXD6/ SMOSI6/ SSDA6 01111b: SDA0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0B 00011b: MTIOC0B# 00101b: TMRI0 01001b: ADSM0 01010b: TXD6/ SMOSI6/ SSDA6 01111b: SDA0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKC 01001b: ADSM0 01010b: TXD5/ SMOSI5/ SSDA5 01111b: SDA0

Register	Bit	RX24T (n = 0 to 7)		RX13T (n = 0 to 7)
		Chip Version A	Chip Version B	
PB3PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0A 00111b: CACREF 01010b: SCK6 01101b: RSPCKA	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0A 00011b: MTIOC0A# 00111b: CACREF 01010b: SCK6 01101b: RSPCKA	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0A 00111b: CACREF 01010b: SCK5 01100b: SCK12
PB4PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00111b: POE8# 01010b: CTS5#/ RTS5#/SS5#	Pin function select bits b4 b0 00000b: Hi-Z 00111b: POE8# 01010b: CTS5#/ RTS5#/SS5# 10100b: GTETRG 10101b: GTECLKD	Pin function select bits b4 b0 00000b: Hi-Z 00111b: POE8#
PB5PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 01010b: TXD5/ SMOSI5/ SSDA5	Pin function select bits b4 b0 00000b: Hi-Z 01010b: TXD5/ SMOSI5/ SSDA5 10100b: GTIOC2B 10110b: GTIOC2B#	Pin function select bits b4 b0 00000b: Hi-Z 01001b: ADTRG0#
PB6PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 01010b: RXD5/ SMISO5/ SSCL5	Pin function select bits b4 b0 00000b: Hi-Z 01010b: RXD5/ SMISO5/ SSCL5 10100b: GTIOC2A 10110b: GTIOC2A#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC1B 00011b: MTIOC3A 01010b: TXD5/ SMOSI5/ SSDA5 01011b: TXD1/ SMOSI1/ SSDA1

Register	Bit	RX24T (n = 0 to 7)		RX13T (n = 0 to 7)
		Chip Version A	Chip Version B	
PB7PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 01010b: SCK5	Pin function select bits b4 b0 00000b: Hi-Z 01010b: SCK5 10100b: GTIOC1B 10110b: GTIOC1B#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTCLKD 01010b: RXD5/ SMISO5/ SSCL5 01011b: RXD1/ SMISO1/ SSCL1
PBnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB4: IRQ3 (100/80/64-pin) PB6: IRQ5 (100/80/64-pin)		Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB1: IRQ2 (48/32-pin) PB4: IRQ3 (48-pin) PB7: IRQ5 (48/32-pin)

Table 2.35 Comparison of PDn Pin Function Control Register (PDnPFS)

Register	Bit	RX24T (n = 0 to 7)		RX13T (n = 3 to 6)
		Chip Version A	Chip Version B	
PD0PFS	—	PD0 pin function control register		—
PD1PFS	—	PD1 pin function control register		—
PD2PFS	—	PD2 pin function control register		—
PD3PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMO0 01010b: TXD1/ SMOSI1/ SSDA1	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMO0 01010b: TXD1/ SMOSI1/ SSDA1 10101b: GTECLKC	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0A 01010b: TXD1/ SMOSI1/ SSDA1
PD4PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMCI0 00110b: TMCI6 01010b: SCK1	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMCI0 00110b: TMCI6 01010b: SCK1 10101b: GTECLKB	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0B 01010b: SCK1

Register	Bit	RX24T (n = 0 to 7)		RX13T (n = 3 to 6)
		Chip Version A	Chip Version B	
PD5PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMRI0 00110b: TMRI6 01010b: RXD1/ SMISO1/ SSCL1	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMRI0 00110b: TMRI6 01010b: RXD1/ SMISO1/ SSCL1 10101b: GTECLKA	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0C 01010b: RXD1/ SMISO1/ SSCL1
PD6PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9C 00101b: TMO1 01001b: ADST0 01010b: CTS1#/ RTS1#/SS1# 01101b: SSLA0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9C 00011b: MTIOC9C# 00101b: TMO1 01001b: ADST0 01010b: CTS1#/ RTS1#/SS1# 01101b: SSLA0 10100b: GTIOC3B 10110b: GTIOC3B#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0D 01001b: ADST0 01010b: CTS1#/ RTS1#/SS1#
PD7PFS	—	PD7 pin function control register		—

Table 2.36 Comparison of PEn Pin Function Control Register (PEnPFS)

Register	Bit	RX24T (n = 0 to 5)		RX13T (n = 2)
		Chip Version A	Chip Version B	
PE0PFS	—	PE0 pin function control register		—
PE1PFS	—	PE1 pin function control register		—
PE3PFS	—	PE3 pin function control register		—
PE4PFS	—	PE4 pin function control register		—
PE5PFS	—	PE5 pin function control register		—
PEnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE3: IRQ2 (100/80-pin) PE4: IRQ1 (100/80-pin) PE5: IRQ0 (100-pin)		Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE2: IRQ0 (48/32-pin)

2.12 Multi-Function Timer Pulse Unit 3

Table 2.37 is a comparative overview of multi-function timer pulse unit 3, and Table 2.38 is a comparison of multi-function timer pulse unit 3 registers.

Table 2.37 Comparative Overview of Multi-Function Timer Pulse Unit 3

Item	RX24T (MTU3d)	RX13T (MTU3c)
Pulse input/output	Max. 28 lines	Max. 16 lines
Pulse input	3 lines	3 lines
Count clocks	11 clocks for each channel (14 clocks for MTU0 and MTU9, 12 clocks for MTU2, 10 clocks for MTU5, and four clocks for MTU1 and MTU2 (when LWA = 1))	11 clocks for each channel (14 clocks for MTU0, 12 clocks for MTU2, 10 clocks for MTU5, and four clocks for MTU1 and MTU2 (when LWA = 1))
Available operations	[MTU0 to MTU4, MTU6, MTU7, MTU9] • Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Simultaneous register input/output by synchronous counter operation • Up to 14-phase PWM output in combination with synchronous operation	[MTU0 to MTU4] • Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Simultaneous register input/output by synchronous counter operation • Up to 12-phase PWM output in combination with synchronous operation
	[MTU0, MTU3, MTU4, MTU6, MTU7, MTU9] • Ability to specify buffer operation	[MTU0, MTU3, MTU4] • Ability to specify buffer operation
	[MTU1, MTU2] • Independent specification of phase counting mode • Ability to specify 32-bit phase counting mode for interlocked operation of MTU1 and MTU2 (when TMDR3.LWA = 1) • Cascade connection operation available	[MTU1, MTU2] • Independent specification of phase counting mode • Ability to specify 32-bit phase counting mode for interlocked operation of MTU1 and MTU2 (when TMDR3.LWA = 1) • Cascade connection operation available
	[MTU3, MTU4, MTU6, MTU7] • Ability to output in complementary PWM and reset PWM operation positive and negative signals in six phases (12 phases in total) through interlocked operation of MTU3/MTU4 and MTU6/MTU7 • Ability to transfer values from buffer registers to temporary registers at peaks and troughs of the timer counter or at writes to the buffer registers (MTU4.TGRD and MTU7.TGRD) in complementary PWM mode • Ability to select double-buffering in complementary PWM mode	[MTU3, MTU4] • Ability to output in complementary PWM and reset PWM operation positive and negative signals in six phases through interlocked operation of MTU3 and MTU4 • Ability to transfer values from buffer registers to temporary registers at peaks and troughs of the timer counter or at writes to the buffer register (MTU4.TGRD) in complementary PWM mode • Ability to select double-buffering in complementary PWM mode

Item	RX24T (MTU3d)	RX13T (MTU3c)
Available operations	[MTU3, MTU4] • Ability to select between two types of waveform output (chopping or level) by specifying a mode for driving AC synchronous motors (brushless DC motors) that uses complementary PWM output or reset PWM output and interlocking with MTU0	[MTU3, MTU4] • Ability to select between two types of waveform output (chopping or level) by specifying a mode for driving AC synchronous motors (brushless DC motors) that uses complementary PWM output or reset PWM output and interlocking with MTU0
	[MTU5] • Ability to use the MTU5 as a dead-time compensation counter	[MTU5] • Ability to use the MTU5 as a dead-time compensation counter
	[MTU6, MTU7] • Ability to select between two types of waveform output (chopping or level) by specifying a mode for driving AC synchronous motors (brushless DC motors) that uses complementary PWM output or reset PWM output and interlocking with MTU9	—
Interrupt skipping function	Ability to skip interrupts at counter peaks and troughs and A/D conversion start triggers in complementary PWM mode	Ability to skip interrupts at counter peaks and troughs and A/D conversion start triggers in complementary PWM mode
Interrupt sources	45 sources	28 sources
Buffer operation	Automatic transfer of register data (transfer from buffer register to timer register)	Automatic transfer of register data (transfer from buffer register to timer register)
Trigger generation	• Ability to generate A/D converter start trigger • Ability to start A/D conversion at any desired timing and in synchronization with PWM output using A/D conversion start request delaying function	• Ability to generate A/D converter start trigger • Ability to start A/D conversion at any desired timing and in synchronization with PWM output using A/D conversion start request delaying function
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Table 2.38 Comparison of Multi-Function Timer Pulse Unit 3 Registers

Register	Bit	RX24T (MTU3d)	RX13T (MTU3c)
TMDR2B	—	Timer mode register 2	—
TSYCR	—	Timer synchronous clear register	—
TSTRA	CST9	Counter start 9 bit	—
TSTRB	—	Timer start register	—
TSYRA	SYNC9	Timer synchronous operation 9 bit	—
TSYRB	—	Timer synchronous register	—
TCSYSTR	SCH7	Synchronous start 7 bit	—
	SCH6	Synchronous start 6 bit	—
	SCH9	Synchronous start 9 bit	—
TRWERB	—	Timer read/write enable register	—
TOERB	—	Timer output master enable register	—
TOCR1B	—	Timer output control register 1	—
TOCR2B	—	Timer output control register 2	—
TGCRB	—	Timer gate control register	—

Register	Bit	RX24T (MTU3d)	RX13T (MTU3c)
TCNTSB	—	Timer subcounter	—
TCDRB	—	Timer period data register	—
TCBRB	—	Timer period buffer register	—
TDDRB	—	Timer dead time data register	—
TDERB	—	Timer dead time enable register	—
TBTERB	—	Timer buffer transfer set register	—
TWCRB	—	Timer waveform control register	—
NFCRn	—	Noise filter control register n (n = 0 to 4, 6, 7, 9, C)	Noise filter control register n (n = 0 to 4, C)
TITMRB	—	Timer interrupt skipping mode register	—
TITCR1B	—	Timer interrupt skipping set register 1	—
TITCNT1B	—	Timer interrupt skipping counter 1	—
TITCR2B	—	Timer interrupt skipping set register 2	—
TITCNT2B	—	Timer interrupt skipping counter 2	—
TADSTRGR0	TADSTRS0 [4:0]	A/D conversion start request select for ADSM0 pin output frame synchronization signal generation bits b4 b0 0 0 0 0 0: Source not selected. 0 0 0 0 1: TRGA0N 0 0 0 1 0: TRGA1N 0 0 0 1 1: TRGA2N 0 0 1 0 0: TRGA3N 0 0 1 0 1: TRGA4N 0 0 1 1 0: TRGA6N 0 0 1 1 1: TRGA7N 0 1 0 0 0: TRG0N 0 1 0 0 1: TRG4AN 0 1 0 1 0: TRG4BN 0 1 1 0 0: TRG4ABN 0 1 1 0 1: TRG7AN 0 1 1 1 0: TRG7BN 1 0 0 0 0: TRG7ABN 1 0 0 0 1: TRGA9N 1 0 0 1 0: TRG9N 1 0 0 1 1: TRG9AEN 1 0 1 0 0: TRG0AEN 1 0 1 0 1: TRGA09N 1 0 1 1 0: TRG09N	A/D conversion start request select for ADSM0 pin output frame synchronization signal generation bits b4 b0 0 0 0 0 0: Source not selected. 0 0 0 0 1: TRGA0N 0 0 0 1 0: TRGA1N 0 0 0 1 1: TRGA2N 0 0 1 0 0: TRGA3N 0 0 1 0 1: TRGA4N 0 1 0 0 0: TRG0N 0 1 0 0 1: TRG4AN 0 1 0 1 0: TRG4BN 0 1 1 0 0: TRG4ABN
TADSTRGR1	—	A/D conversion start request select register 1	—

2.13 Port Output Enable 3

Table 2.39 is a comparative overview of port output enable 3, and Table 2.40 is a comparison of port output enable 3 registers.

Table 2.39 Comparative Overview of Port Output Enable 3

Item	RX24T (POE3b, POE3A)	RX13T (POE3C)
Pin status while output is disabled	• High-impedance • General I/O port (chip version B only)	• High-impedance
High-impedance control target pins	• MTU output pins — MTU0 pin (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) — MTU3 pin (MTIOC3B, MTIOC3D) — MTU4 pin (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) — MTU6 pin (MTIOC6B, MTIOC6D) — MTU7 pin (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D) — MTU9 pin (MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D) • GPT output pins (chip version B only) — GPT0 pin (GTIOC0A, GTIOC0B) — GPT1 pin (GTIOC1A, GTIOC1B) — GPT2 pin (GTIOC2A, GTIOC2B) — GPT3 pin (GTIOC3A, GTIOC3B)	• MTU output pins — MTU0 pin (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) — MTU3 pin (MTIOC3B, MTIOC3D) — MTU4 pin (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D)
Conditions for generating high-impedance request	• Input pin change: Detection of signal input on POE0#, POE4#, POE8#, POE10#, POE11#, or POE12# • Register setting • Detection of oscillation stop by main clock oscillator • Detection of output from comparator C (CMPC) • Short circuit between output pins: A match (short circuit) between the output signal levels (active level) over one or more cycles on any of the following combinations of pins [MTU complementary PWM output pins] MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D — MTIOC6B and MTIOC6D — MTIOC7A and MTIOC7C — MTIOC7B and MTIOC7D	• Input pin change: Detection of signal input on POE0#, POE8#, or POE10# • SPOER register setting • Detection of oscillation stop by main clock oscillator • Detection of output from comparator C (CMPC) • Short circuit between output pins: A match (short circuit) between the output signal levels (active level) over one or more cycles on any of the following combinations of pins [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D

Item	RX24T (POE3b, POE3A)	RX13T (POE3C)
Conditions for generating high-impedance request	[GPT output pins] — GTIOC0A and GTIOC0B — GTIOC1A and GTIOC1B — GTIOC2A and GTIOC2B	
Functions	• The POE0#, POE4#, POE8#, POE10#, POE11#, and POE12# input pins can each be set for falling edge, PCLK/8 × 16, PCLK/16 × 16, or PCLK/128 × 16 low-level sampling. • Output on all the target pins can be disabled by falling-edge or low-level sampling of the POE0#, POE4#, POE8#, POE10#, POE11#, or POE12# pin. • Output on all the target pins can be disabled when oscillation stop is detected by the oscillation stop detection function of the clock generator. • Output on the MTU complementary PWM output pins can be disabled when output levels of MTU complementary PWM output pins are compared and simultaneous active-level output continues for one cycle or more. • Output on the GPT output pins can be disabled when output levels of GPT output pins (GPT0, GPT1, and GPT2) are compared and simultaneous active-level output continues for one cycle or more. • Output on all the target pins can be disabled at comparator detection by comparator C (CMPC). • Output on all the target pins can be disabled by modifying the settings of the POE registers. • Interrupts can be generated by input-level sampling or output-level comparison results.	• The POE0#, POE8#, and POE10# input pins can each be set for falling edge, PCLK/8 × 16, PCLK/16 × 16, or PCLK/128 × 16 low-level sampling. • MTU complementary PWM output pins and MTU0 pins can be placed in the high-impedance state at falling-edge or low-level sampling of the POE0#, POE8#, or POE10# pins. • Output on all the target pins can be disabled when oscillation stop is detected by the oscillation stop detection function of the clock generator. • MTU complementary PWM output pins can be placed in the high-impedance state when output levels of MTU complementary PWM output pins are compared and simultaneous active-level output continues for one cycle or more. • MTU complementary PWM output pins and MTU0 pins can be placed in the high-impedance state at comparator detection by the comparator (CMPC). • Output on all the target pins can be disabled by modifying the settings of the POE registers. • Interrupts can be generated by input-level sampling or output-level comparison results.

Table 2.40 Comparison of Port Output Enable 3 Registers

Register	Bit	RX24T (POE3b, POE3A)	RX13T (POE3C)
ICSR2	—	Input level control/status register 2	—
ICSR5	—	Input level control/status register 5	—
ICSR7	—	Input level control/status register 7	—
OCSR2	—	Output level control/status register 2	—
ALR1	OLSG0A	MTIOC3B/GTIOC0A (P71) pin active level setting bit	MTIOC3B active level setting bit
	OLSG0B	MTIOC3D/GTIOC0B(P74) pin active level setting bit	MTIOC3D active level setting bit
	OLSG1A	MTIOC4A/GTIOC1A (P72) pin active level setting bit	MTIOC4A active level setting bit
	OLSG1B	MTIOC4C/GTIOC1B(P75) pin active level setting bit	MTIOC4C active level setting bit
	OLSG2A	MTIOC4B/GTIOC2A (P73) pin active level setting bit	MTIOC4B active level setting bit
	OLSG2B	MTIOC4D/GTIOC2B(P76) pin active level setting bit	MTIOC4D active level setting bit
ALR2	—	Active level register 2	—
SPOER	MTUCH34HIZ	MTU3 and MTU4 or GPT0 to GPT2 pin output disable bit	MTU3 and MTU4 output high-impedance enable bit
	MTUCH67HIZ	MTU6 and MTU7 pin output disable bit	—
	GPT03HIZ	GPT0 to GPT3 pin output disable bit*1	—
	MTUCH9HIZ	MTU9 pin output disable bit	—
POECR1	MTU0C1ZE	—	MTIOC0C (PD5) pin high-impedance enable bit
	MTU0D1ZE	—	MTIOC0D (PD6) pin high-impedance enable bit
POECR2	MTU7BDZE	MTIOC7B/MTIOC7D pin high-impedance enable bit	—
	MTU7ACZE	MTIOC7A/MTIOC7C pin high-impedance enable bit	—
	MTU6BDZE	MTIOC6B/MTIOC6D pin high-impedance enable bit	—
POECR3	—	Port output enable control register 3	—
POECR4	IC2ADDMT34ZE	MTU3 and MTU4 output disabling condition POE4F add bit	—
	IC5ADDMT34ZE	MTU3 and MTU4 output disabling condition POE11F add bit	—
	IC6ADDMT34ZE	MTU3 and MTU4 output disabling condition POE12F add bit	—
	CMADDMT67ZE	MTU6 and MTU7 output disabling condition CFLAG add bit	—
	IC1ADDMT67ZE	MTU6 and MTU7 output disabling condition POE0F add bit	—
	IC3ADDMT67ZE	MTU6 and MTU7 output disabling condition POE8F add bit	—

Register	Bit	RX24T (POE3b, POE3A)	RX13T (POE3C)
POECR4	IC4ADDMT67ZE	MTU6 and MTU7 output disabling condition POE10F add bit	—
	IC5ADDMT67ZE	MTU6 and MTU7 output disabling condition POE11F add bit	—
	IC6ADDMT67ZE	MTU6 and MTU7 output disabling condition POE12F add bit	—
POECR5	IC2ADDMT0ZE	MTU0 output disabling condition POE4F add bit	—
	IC5ADDMT0ZE	MTU0 output disabling condition POE11F add bit	—
	IC6ADDMT0ZE	MTU0 output disabling condition POE12F add bit	—
POECR6	—	Port output enable control register 6	—
POECR7	—	Port output enable control register 7	—
POECR8	—	Port output enable control register 8	—
PMMCR0	—	Port mode mask control register 0*2	—
PMMCR1	—	Port mode mask control register 1*2	—
PMMCR2	—	Port mode mask control register 2*2	—
PMMCR3	—	Port mode mask control register 3*2	—
POECMPFR	C3FLAG	Comparator channel 3 output detection flag	—
POECMPSEL	POEREQ3	Comparator channel 3 output disabling request enable bit	—
POECMPEXm	—	Port output enable comparator request extended selection register m (m = 0 to 2, 4, or 5)	—

Notes: 1. This bit is reserved on chip version A. The read value is 0 and the write value should be 0.
2. Only implemented on chip version B.

2.14 Compare Match Timer

Table 2.41 is a comparative overview of compare match timer, and Table 2.42 is a comparison of compare match timer registers.

Table 2.41 Comparative Overview of Compare Match Timer

Item	RX24T (CMT)	RX13T (CMT)
Number of channels	2 channels × 2 units	2 channels × 1 unit
Count clocks	Four frequency dividing clocks: One clock among PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.	Four frequency dividing clocks: One clock among PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.
Interrupts	A compare match interrupt can be requested for each channel.	A compare match interrupt can be requested for each channel.
Low power consumption function	Each unit can be placed in a module stop state.	Ability to specify to module stop state

Table 2.42 Comparison of Compare Match Timer Registers

Register	Bit	RX24T (CMT)	RX13T (CMT)
CMSTR1	—	Compare match timer start register 1	—

2.15 Serial Communications Interface

Table 2.43 is a comparative overview of the serial communications interfaces, and Table 2.44 is a comparison of serial communications interface channel specifications, and Table 2.45 is a comparison of serial communications interface registers.

Table 2.43 Comparative Overview of Serial Communications Interfaces

Item		RX24T (SCIg)	RX13T (SCIg, SCIh)
Number of channels		• SCIg: 3 channels	• SCIg: 2 channels • SCIh: 1 channel
Serial communications modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable as LSB first or MSB first transfer.	Selectable as LSB first or MSB first transfer.
Interrupt sources		Transmit end, transmit data empty, receive data full, and receive error, completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)	Transmit end, transmit data empty, receive data full, and receive error, completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)
Low power consumption function		Module stop state can be set for each channel.	Module stop state can be set for each channel.
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection function	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Start-bit detection	Low level or falling edge is selectable.	Low level or falling edge is selectable.
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.
	Clock source	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5 and SCI6).	• An internal or external clock can be selected. • Transfer rate clock input from the MTU can be used (SCI1 and SCI5).

Item		RX24T (SCIg)	RX13T (SCIg, SCIh)
Asynchronous mode	Double-speed mode	Baud rate generator double-speed mode is selectable.	Baud rate generator double-speed mode is selectable.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/ reception.	CTSn# and RTSn# pins can be used in controlling transmission/ reception.
Smart card interface mode	Error processing	An error signal can be automatically transmitted when detecting a parity error during reception	An error signal can be automatically transmitted when detecting a parity error during reception
		Data can be automatically retransmitted when receiving an error signal during transmission	Data can be automatically retransmitted when receiving an error signal during transmission
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	I^2C bus format	I^2C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer rate	Fast mode is supported.	Fast mode is supported.
	Noise cancellation	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.

Item		RX24T (SCIg)	RX13T (SCIg, SCIh)
Extended serial mode (supported by SCI12 only)	Start frame transmission	—	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection
	Start frame reception	—	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two kinds of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates
	I/O control function	—	• Ability to select polarity or TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select receive data sampling timing of RXDX12 pin
	Timer function	—	Usable as reloading timer
Bit rate modulation function		Correction of outputs from the on-chip baud rate generator can reduce errors.	Correction of outputs from the on-chip baud rate generator can reduce errors.

Table 2.44 Comparison of Serial Communications Interface Channel Specifications

Item	RX24T (SCIg)	RX13T (SCIg, SCIh)
Synchronous mode	SCI1, SCI5, SCI6	SCI1, SCI5, SCI12
Clock synchronous mode	SCI1, SCI5, SCI6	SCI1, SCI5, SCI12
Smart card interface mode	SCI1, SCI5, SCI6	SCI1, SCI5, SCI12
Simple I^2C mode	SCI1, SCI5, SCI6	SCI1, SCI5, SCI12
Simple SPI mode	SCI1, SCI5, SCI6	SCI1, SCI5, SCI12
Extended serial mode	—	SCI12
TMR clock input (RX24T)/ MTU clock input (RX13T)	SCI5, SCI6	SCI1, SCI5, SCI12

Table 2.45 Comparison of Serial Communications Interface Registers

Register	Bit	RX24T (SCIg)	RX13T (SCIg, SCIh)
SEMR	ACS0	Asynchronous mode clock source select bit (Valid only in asynchronous mode) 0: External clock input 1: Logical AND of two compare matches output from TMR (valid for SCI5 and SCI6 only) Available compare match output varies among SCI channels.	Asynchronous mode clock source select bit (Valid only in asynchronous mode) 0: External clock input 1: Logical AND of two compare matches output from MTU
ESMER	—	—	Extended serial mode enable register
CR0	—	—	Control register 0
CR1	—	—	Control register 1
CR2	—	—	Control register 2
CR3	—	—	Control register 3
PCR	—	—	Port control register
ICR	—	—	Interrupt control register
STR	—	—	Status register
STCR	—	—	Status clear register
CF0DR	—	—	Control field 0 data register
CF0CR	—	—	Control field 0 compare enable register
CF0RR	—	—	Control field 0 receive data register
PCF1DR	—	—	Primary control field 1 data register
SCF1DR	—	—	Secondary control field 1 data register
CF1CR	—	—	Control field 1 compare enable register
CF1RR	—	—	Control field 1 receive data register
TCR	—	—	Timer control register
TMR	—	—	Timer mode register
TPRE	—	—	Timer prescaler register
TCNT	—	—	Timer count register

2.16 12-Bit A/D Converter

Table 2.46 is a comparative overview of the 12-bit A/D converters, Table 2.47 is a comparison of 12-bit A/D converter registers, Table 2.48 is a comparison of A/D conversion start trigger settings in the ADSTRGR register, and Table 2.49 is a comparison of A/D conversion start trigger settings in the ADGCTRGR register.

Table 2.46 Comparative Overview of 12-Bit A/D Converters

Item	RX24T (S12ADF)	RX13T (S12ADF)
Number of units	3 unit (S12AD, S12AD1, S12AD2)	1 unit (S12AD)
Input channels	S12AD: 5 channels S12AD1: 5 channels S12AD2: 12 channels	S12AD: 8 channels
Extended analog function	Internal reference voltage (S12AD2 only)	Internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	1.0 µs per channel (when A/D conversion clock ADCLK = 40 MHz)	1.4 µs per channel (when A/D conversion clock ADCLK = 32 MHz)
A/D conversion clock	Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. PCLK to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.	Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. PCLK to ADCLK frequency ratio = 1:1, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.
Data register	• 22 registers (five for S12AD, five for S12AD1, and 12 for S12AD2) for analog input, one for A/D-converted data duplication in double trigger mode, and two for A/D-converted data duplication during extended operation in double trigger mode unit • One register for internal reference (S12AD2) • One register for self-diagnosis per unit • The results of A/D conversion are stored in 12-bit A/D data registers. • 12-bit accuracy output for the results of A/D conversion • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode.	• 8 registers for analog input, one for A/D-converted data duplication in double trigger mode, and two for A/D-converted data duplication during extended operation in double trigger mode • One register for internal reference • One register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • 12-bit accuracy output for the results of A/D conversion • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode.

Item	RX24T (S12ADF)	RX13T (S12ADF)
Data register	• Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): A/D-converted analog input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.	• Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): A/D-converted analog input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.
Operating modes	The operating mode can be set independently for each of three units. • Single scan mode: — A/D conversion is performed only once on the analog inputs of the arbitrarily selected channels. — A/D conversion is performed only once on the internal reference voltage (S12AD2). • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of up to 10 channels arbitrarily selected. • Group scan mode: — The number of groups used is selectable between two (groups A and B) and three (groups A, B, and C). (When two is selected as the number of groups, only group A and group B may be used in combination.) — Analog inputs of arbitrarily selected channels are divided into group A and group B, or group A, group B, and group C, and A/D conversion of the analog inputs selected on a group basis is performed only once. — Conversion start conditions (synchronous trigger) can be selected independently for group A, group B, and group C, allowing A/D conversion of the groups to start at different times.	• Single scan mode: — A/D conversion is performed only once on the analog inputs of the arbitrarily selected channels. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of the arbitrarily selected. • Group scan mode: — The number of groups used is selectable between two (groups A and B) and three (groups A, B, and C). (When two is selected as the number of groups, only group A and group B may be used in combination.) — Analog inputs of arbitrarily selected channels are divided into group A and group B, or group A, group B, and group C, and A/D conversion of the analog inputs selected on a group basis is performed only once. — Conversion start conditions (synchronous trigger) can be selected independently for group A, group B, and group C, allowing A/D conversion of the groups to start at different times.

Item	RX24T (S12ADF)	RX13T (S12ADF)
Operating modes	• Group scan mode (when a group is given priority): — If a trigger is input for a higher-priority group during A/D conversion on a lower-priority group, A/D conversion on the lower-priority group is stopped and A/D conversion is performed on the higher-priority group. — The order of priority is group A (highest) > group B > group C (lowest). — Restart (rescan) of A/D conversion on the lower-priority group after completion of A/D conversion on the higher-priority group can be enabled. In addition, rescan can be set to start from the first of the selected channels or from the channels on which A/D conversion has not yet finished.	• Group scan mode (when a group is given priority): — If a trigger is input for a higher-priority group during A/D conversion on a lower-priority group, A/D conversion on the lower-priority group is stopped and A/D conversion is performed on the higher-priority group. — The order of priority is group A (highest) > group B > group C (lowest). — Restart (rescan) of A/D conversion on the lower-priority group after completion of A/D conversion on the higher-priority group can be enabled. In addition, rescan can be set to start from the first of the selected channels or from the channels on which A/D conversion has not yet finished.
Conditions for A/D conversion start	• Software trigger • Synchronous trigger Trigger by the multi-function timer pulse unit (MTU), general PWM timer (GPT), or 8-bit timer (TMR) • Asynchronous trigger A/D conversion can be triggered by the external trigger ADTRG0# (S12AD), ADTRG1# (S12AD1), or ADTRG2# (S12AD2) pin (independently for each of three units).	• Software trigger • Synchronous trigger Trigger by the multi-function timer pulse unit (MTU) • Asynchronous trigger A/D conversion can be triggered by the external trigger ADTRG0# pin.
Functions	• Channel-dedicated sample-and-hold function (three channels for S12AD1 only) • Input signal amplification function using programmable gain amplifier (1 channel for S12AD and three channels for S12AD1) • Variable sampling state count (independently settable for each channel) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers	• Channel-dedicated sample-and-hold function (three channels) • Input signal amplification function using programmable gain amplifier (three channels) • Variable sampling state count (independently settable for each channel) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers

Item	RX24T (S12ADF)	RX13T (S12ADF)
Interrupt sources	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of single scan (independently for each of three units). • In double trigger mode, A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of double scan (independently for each of three units). • In group scan mode, an A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of group A scan, whereas an A/D scan end interrupt request (GBADI, GBADI1, or GBADI2) for group B can be generated on completion of group B scan. A dedicated group C scan end interrupt request (GCADI, GBADI1, or GBADI2) can be generated on completion of group C scan. • When double trigger mode is selected in group scan mode, A/D scan end interrupt request (S12ADI, S12ADI1, S12ADI2) can be generated on completion of double scan of group A. A dedicated group B or dedicated group C scan end interrupt request (GBADI/GCADI, GBADI1/GCADI1, or GBADI2/GCADI2) can be generated on completion of group B or group C scan, respectively. • The S12ADI/S12ADI1/S12ADI2, GBADI/GBADI1/GBADI2, and GCADI/GCADI1/GCADI2 interrupts can activate the data transfer controller (DTC).	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI) can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt request (S12ADI) can be generated on completion of double scan. • In group scan mode, an A/D scan end interrupt request (S12ADI) can be generated on completion of group A scan, whereas an A/D scan end interrupt request (GBADI) for group B can be generated on completion of group B scan. A dedicated group C scan end interrupt request (GCADI) can be generated on completion of group C scan. • When double trigger mode is selected in group scan mode, A/D scan end interrupt request (S12ADI) can be generated on completion of double scan of group A. A dedicated group B or dedicated group C scan end interrupt request (GBADI or GCADI) can be generated on completion of group B or group C scan, respectively. • The S12ADI, GBADI, and GCADI interrupts can activate the data transfer controller (DTC).
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.47 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX24T (S12ADF)	RX13T (S12ADF)
ADDRy	—	A/D data register y (y = 0 to 3, 16: S12AD and S12AD1, y = 0 to 11: S12AD2)	A/D data register y (y = 0 to 7)
S12AD. ADANSA0	ANSA0n	A/D conversion channel select bit (n = 00 to 03)	A/D conversion channel select bit (n = 00 to 07)
S12AD1. ADANSA0	—	A/D channel select register A0	—
S12AD2. ADANSA0	—	A/D channel select register A0	—
ADANSA1	—	A/D channel select register A1	—
S12AD. ADANSB0	ANSB0n	A/D conversion channel select bit (n = 00 to 03)	A/D conversion channel select bit (n = 00 to 07)
S12AD1. ADANSB0	—	A/D channel select register B0	—
S12AD2. ADANSB0	—	A/D channel select register B0	—
ADANSB1	—	A/D channel select register B1	—
S12AD. ADANSC0	ANSC0n	A/D conversion channel select bit (n = 00 to 03)	A/D conversion channel select bit (n = 00 to 07)
S12AD1. ADANSC0	—	A/D channel select register C0	—
S12AD2. ADANSC0	—	A/D channel select register C0	—
ADANSC1	—	A/D channel select register C1	—
S12AD. ADADS0	ADS0n	A/D-converted value addition/ average channel select bit (n = 00 to 03)	A/D-converted value addition/ average channel select bit (n = 00 to 07)
S12AD1. ADADS0	—	A/D-converted value addition/ average function channel select register 0	—
S12AD2. ADADS0	—	A/D-converted value addition/ average function channel select register 0	—
ADADS1	—	A/D-converted value addition/ average function channel select register 1	—
ADSSTRn	—	A/D sampling state register n (n = 0 to 11, L, O)	A/D sampling state register n (n = 0 to 7, O)
ADPGACR	P001SEL1	—	PGA P001 amplifier pass-through enable bit
	P001ENAMP	—	PGA P001 amplifier enable bit
	P002SEL1	—	PGA P002 amplifier pass-through enable bit
	P002ENAMP	—	PGA P002 amplifier enable bit
S12AD1. ADPGACR	—	A/D programmable gain amplifier control register	—

Register	Bit	RX24T (S12ADF)	RX13T (S12ADF)
S12AD. ADPGAGS0	P000GAIN [3:0]	PGA P000 gain setting bits The relationship between each setting and the gain is as follows: b3 b0 0 0 0 0: ×2.000 0 0 0 1: ×2.500 0 1 0 0: ×3.077 0 1 1 0: ×3.636 0 1 1 1: ×4.000 1 0 0 0: ×4.444 Settings other than the above are prohibited.	PGA P000 gain setting bits The relationship between each setting and the gain is as follows: b3 b0 0 0 0 0: ×2.000 0 0 0 1: ×2.500 0 1 0 0: ×3.077 1 0 0 1: ×5.000 1 1 0 0: ×8.000 1 1 0 1: ×10.000 Settings other than the above are prohibited.
	P001GAIN [3:0]	—	PGA P001 gain setting bits
	P002GAIN [3:0]	—	PGA P002 gain setting bits
S12AD1. ADPGAGS0	—	—	A/D programmable gain amplifier gain setting register 0

Table 2.48 Comparison of A/D Start Triggers and Corresponding ADSTRGR Register Settings

Bit	RX24T (S12ADF)	RX13T (S12ADF)
TRSB[5:0]	A/D conversion start trigger select bits for group B b5 b0 1 1 1 1 1 1: No trigger source selected. 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN	A/D conversion start trigger select bits for group B b5 b0 1 1 1 1 1 1: No trigger source selected. 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 0 1 1 0: TRGA6N 0 0 0 1 1 1: TRGA7N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 0 1 1 0 1: TRG7AN 0 0 1 1 1 0: TRG7BN 0 0 1 1 1 1: TRG7AN or TRG7BN 0 1 0 0 0 0: TRG7ABN 0 1 0 0 1 1: TRGA9N 0 1 0 1 0 0: TRG9N 0 1 1 0 0 1: TRGA0N or TRG0N 0 1 1 0 1 0: TRGA9N or TRG9N 0 1 1 0 1 1: TRGA0N or TRGA9N 0 1 1 1 0 0: TRG0N or TRG9N 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1 0 1 1 1 1 1: TMTRG0AN_2 1 0 0 0 0 0: TMTRG0AN_3 1 0 0 0 0 1: TRG9AEN 1 0 0 0 1 0: TRG0AEN 1 0 0 0 1 1: TRGA09N 1 0 0 1 0 0: TRG09N 1 1 0 0 1 0: GTADTRA0N 1 1 0 0 1 1: GTADTRB0N 1 1 0 1 0 0: GTADTRA1N 1 1 0 1 0 1: GTADTRB1N 1 1 0 1 1 0: GTADTRA2N 1 1 0 1 1 1: GTADTRB2N 1 1 1 0 0 0: GTADTRA3N 1 1 1 0 0 1: GTADTRB3N 1 1 1 0 1 0: GTADTRA0N or GTADTRB0N 1 1 1 0 1 1: GTADTRA1N or GTADTRB1N 1 1 1 1 0 0: GTADTRA2N or GTADTRB2N 1 1 1 1 0 1: GTADTRA3N or GTADTRB3N

Bit	RX24T (S12ADF)	RX13T (S12ADF)
TRSA[5:0]	A/D conversion start trigger select bits b13 b8 1 1 1 1 1 1: No trigger source selected. 0 0 0 0 0 0: ADTRG0# 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN	A/D conversion start trigger select bits b13 b8 1 1 1 1 1 1: No trigger source selected. 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 0 1 1 0: TRGA6N 0 0 0 1 1 1: TRGA7N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 0 1 1 0 1: TRG7AN 0 0 1 1 1 0: TRG7BN 0 0 1 1 1 1: TRG7AN or TRG7BN 0 1 0 0 0 0: TRG7ABN 0 1 0 0 1 1: TRGA9N 0 1 0 1 0 0: TRG9N 0 1 1 0 0 1: TRGA0N or TRG0N 0 1 1 0 1 0: TRGA9N or TRG9N 0 1 1 0 1 1: TRGA0N or TRGA9N 0 1 1 1 0 0: TRG0N or TRG9N 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1 0 1 1 1 1 1: TMTRG0AN_2 1 0 0 0 0 0: TMTRG0AN_3 1 0 0 0 0 1: TRG9AEN 1 0 0 0 1 0: TRG0AEN 1 0 0 0 1 1: TRGA09N 1 0 0 1 0 0: TRG09N 1 1 0 0 1 0: GTADTRA0N 1 1 0 0 1 1: GTADTRB0N 1 1 0 1 0 0: GTADTRA1N 1 1 0 1 0 1: GTADTRB1N 1 1 0 1 1 0: GTADTRA2N 1 1 0 1 1 1: GTADTRB2N 1 1 1 0 0 0: GTADTRA3N 1 1 1 0 0 1: GTADTRB3N 1 1 1 0 1 0: GTADTRA0N or GTADTRB0N 1 1 1 0 1 1: GTADTRA1N or GTADTRB1N 1 1 1 1 0 0: GTADTRA2N or GTADTRB2N 1 1 1 1 0 1: GTADTRA3N or GTADTRB3N

Table 2.49 Comparison of A/D Start Triggers and Corresponding ADGCTRGR Register Settings

Bit	RX24T (S12ADF)	RX13T (S12ADF)
TRSC[5:0]	A/D conversion start trigger select bits for group C b5 b0 1 1 1 1 1 1: No trigger source selected. 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN	A/D conversion start trigger select bits for group C b5 b0 1 1 1 1 1 1: No trigger source selected. 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 0 1 1 0: TRGA6N 0 0 0 1 1 1: TRGA7N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 0 1 1 0 1: TRG7AN 0 0 1 1 1 0: TRG7BN 0 0 1 1 1 1: TRG7AN or TRG7BN 0 1 0 0 0 0: TRG7ABN 0 1 0 0 1 1: TRGA9N 0 1 0 1 0 0: TRG9N 0 1 1 0 0 1: TRGA0N or TRG0N 0 1 1 0 1 0: TRGA9N or TRG9N 0 1 1 0 1 1: TRGA0N or TRGA9N 0 1 1 1 0 0: TRG0N or TRG9N 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1 0 1 1 1 1 1: TMTRG0AN_2 1 0 0 0 0 0: TMTRG0AN_3 1 0 0 0 0 1: TRG9AEN 1 0 0 0 1 0: TRG0AEN 1 0 0 0 1 1: TRGA09N 1 0 0 1 0 0: TRG09N 1 1 0 0 1 0: GTADTRA0N 1 1 0 0 1 1: GTADTRB0N 1 1 0 1 0 0: GTADTRA1N 1 1 0 1 0 1: GTADTRB1N 1 1 0 1 1 0: GTADTRA2N 1 1 0 1 1 1: GTADTRB2N 1 1 1 0 0 0: GTADTRA3N 1 1 1 0 0 1: GTADTRB3N 1 1 1 0 1 0: GTADTRA0N or GTADTRB0N 1 1 1 0 1 1: GTADTRA1N or GTADTRB1N 1 1 1 1 0 0: GTADTRA2N or GTADTRB2N 1 1 1 1 0 1: GTADTRA3N or GTADTRB3N

2.17 D/A Converter / D/A Converter for Generating Comparator C Reference Voltage

Table 2.50 is a comparative overview of the D/A converters, and Table 2.51 is a comparison of D/A converter registers.

Table 2.50 Comparative Overview of D/A Converters

Item	RX24T (DA, DAa)	RX13T (DA)
Resolution	8 bits	8 bits
Output channels	[Chip version A] One channel [Chip version B] Two channels	 Two channels
Measure against mutual interference between analog modules	Measure against interference between D/A and A/D converters • D/A-converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable input signal from the 12-bit A/D converter (unit 2). This reduces degradation of A/D conversion accuracy due to interference by controlling, by means of an enable signal, the timing at which the 8-bit D/A converter inrush current occurs. (chip version B only)	—
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Table 2.51 Comparison of D/A Converter Registers

Register	Bit	RX24T (DA, DAa)	RX13T (DA)
DADRm	—	D/A data register m (m = 0, 1)	D/A data register m (m = 0)
DACR	DAOE1	D/A output enable 1 bit This bit is reserved on chip version A. The read value is 0 and the write value should be 0.	—
DADPR	—	DADRm format select register (m = 0 or 1)	Data register format select register
DAADSCR	—	D/A A/D synchronous start control register Implemented in chip version B only.	—

2.18 Comparator C

Table 2.52 is a comparative overview of the comparator C modules, and Table 2.53 is a comparison of comparator C registers.

Table 2.52 Comparative Overview of Comparator C Modules

Item	RX24T (CMPC)	RX13T (CMPC)
Number of channels	4 channels (comparator C0 to comparator C3)	3 channels (comparator C0 to comparator C2)
Analog input voltage	Input voltage to CMPCnm pin (n = channel number; m = 0 to 3)	Input voltage to CMPCnm pin (n = channel number; m = 0 to 3)
Reference input voltage	[Chip version A] Input voltage to CVREFC0 or CVREFC1 pin or on-chip D/A converter 0 output voltage [Chip version B] Output voltage from on-chip D/A converter 0 or on-chip D/A converter 1	Input voltage to CVREFC0 pin or on-chip D/A converter 0 output voltage
Comparison result	The comparison result can be output externally.	The comparison result can be output externally.
Digital filter function	• One of three sampling periods can be selected. • The filter function can also be disabled. • A noise-filtered signal can be used to generate interrupt request output and POE source output, and GPT internal trigger source output, and comparison results can be read from registers.	• One of three sampling periods can be selected. • The filter function can also be disabled. • A noise-filtered signal can be used to generate interrupt request output and POE source output, and comparison results can be read from registers.
Interrupt request	• An interrupt request is generated upon detection of a valid edge of the comparison result. • The rising edge, falling edge, or both edges of the comparison result can be selected.	• An interrupt request is generated upon detection of a valid edge of the comparison result. • The rising edge, falling edge, or both edges of the comparison result can be selected as valid edges.
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Table 2.53 Comparison of Comparator C Registers

Register	Bit	RX24T (CMPC)	RX13T (CMPC)
CMPSEL0	CMPSEL [3:0]	Comparator input select bits • Comparator C0 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC00 selected 0 0 1 0: CMPC01 selected 0 1 0 0: CMPC02 selected 1 0 0 0: CMPC03 selected Settings other than the above are prohibited. • Comparator C1 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC10 selected 0 0 1 0: CMPC11 selected 0 1 0 0: CMPC12 selected 1 0 0 0: CMPC13 selected Settings other than the above are prohibited. • Comparator C2 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC20 selected 0 0 1 0: CMPC21 selected 0 1 0 0: CMPC22 selected 1 0 0 0: CMPC23 selected Settings other than the above are prohibited. • Comparator C3 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC30 selected 0 0 1 0: CMPC31 selected 0 1 0 0: CMPC32 selected 1 0 0 0: CMPC33 selected Settings other than the above are prohibited.	Comparator input select bits • Comparator C0 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC00 selected 0 0 1 0: CMPC01 selected 0 1 0 0: CMPC02 selected 1 0 0 0: CMPC03 selected Settings other than the above are prohibited. • Comparator C1 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC10 selected 0 0 1 0: CMPC11 selected 0 1 0 0: CMPC12 selected 1 0 0 0: CMPC13 selected Settings other than the above are prohibited. • Comparator C2 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC20 selected 0 0 1 0: CMPC21 selected 0 1 0 0: CMPC22 selected Settings other than the above are prohibited.

Register	Bit	RX24T (CMPC)	RX13T (CMPC)
CMPSEL1	CVRS [1:0]	Reference input voltage select bits [Chip version A] • Comparator C0 b1 b0 0 0: No input 0 1: Input to CVREFC0 pin selected as reference input voltage 1 0: On-chip D/A converter 0 output selected as reference input voltage Settings other than the above are prohibited. • Comparator C1 to comparator C3 b1 b0 0 0: No input 0 1: Input to CVREFC1 pin selected as reference input voltage 1 0: On-chip D/A converter 0 output selected as reference input voltage Settings other than the above are prohibited. [Chip version B] b1 b0 0 0: No input 0 1: On-chip D/A converter 1 output selected as reference input voltage 1 0: On-chip D/A converter 0 output selected as reference input voltage Settings other than the above are prohibited.	Reference input voltage select bits b1 b0 0 0: No input 0 1: Input to CVREFC0 pin selected as reference input voltage 1 0: On-chip D/A converter 0 output selected as reference input voltage Settings other than the above are prohibited.

2.19 RAM

Table 2.54 is a comparative overview of RAM.

Table 2.54 Comparative Overview of RAM

Item	RX24T	RX13T
RAM capacity	Max. 32 KB (RAM0: 32 KB)	12 KB
RAM address	• When the RAM capacity is 32 KB RAM0: 0000 0000h to 0000 7FFFh • When the RAM capacity is 16 KB RAM0: 0000 0000h to 0000 3FFFh	• When the RAM capacity is 12 KB RAM0: 0000 0000h to 0000 2FFFh
Access	• Single-cycle access is possible for both reading and writing. • On-chip RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. • On-chip RAM can be enabled or disabled.
Low power consumption function	Ability to set module stop state for RAM0	Ability to set module stop state for RAM0

2.20 Flash Memory

Table 2.55 is a comparative overview of flash memory, and Table 2.56 is a comparison of flash memory registers.

Table 2.55 Comparative Overview of Flash Memory

Item	RX24T	RX13T (FLASH)
Memory capacity	• User area: Up to 512 KB • Data area: 8 KB • Extra area: Stores the start-up area information, access window information, and unique ID	• User area: Up to 128 KB • Data area: 4 KB • Extra area: Stores the start-up area information, access window information, and unique ID
Addresses	• Products with capacity of 512 KB FFF8 0000h to FFFF FFFFh • Products with capacity of 384 KB FFFA 0000h to FFFF FFFFh • Products with capacity of 256 KB FFFC 0000h to FFFF FFFFh • Products with capacity of 128 KB FFFE 0000h to FFFF FFFFh	• Products with capacity of 128 KB FFFE 0000h to FFFF FFFFh • Products with capacity of 64 KB FFFF 0000h to FFFF FFFFh
ROM cache	Capacity: 2 KB	—
Software commands	• The following software commands are implemented: Program, blank check, block erase, and all-block erase • The following commands are implemented for programming the extra area: Start-up area information program and access window information program	• The following software commands are implemented: Program, blank check, block erase, and unique ID read • The following commands are implemented for programming the extra area: Start-up area information program and access window information program
Value after erasure	• ROM: FFh • E2 DataFlash: FFh	• ROM: FFh • E2 DataFlash: FFh
Interrupt	An interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.	An interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.
On-board programming	• Boot mode (SCI interface) — Channel 1 of the serial communications interface (SCI1) is used for asynchronous communication. — The user area and data area can be programmed. • Boot mode (FINE interface) — The FINE interface is used. — The user area and data area can be programmed. • Self-programming (single-chip mode) — The user area and data area can be programmed using a flash programming routine in a user program.	• Boot mode (SCI interface) — Channel 1 of the serial communications interface (SCI1) is used for asynchronous communication. — The user area and data area can be programmed. • Boot mode (FINE interface) — The FINE interface is used. — The user area and data area can be programmed. • Self-programming (single-chip mode) — The user area and data area can be programmed using a flash programming routine in a user program.

Item	RX24T	RX13T (FLASH)
Off-board programming	The user area and data area can be programmed using a flash programmer (serial programmer or parallel programmer) compatible with the MCU.	The user area and data area can be programmed using a flash programmer compatible with the MCU.
ID codes protection	• Connection with a serial programmer can be controlled using ID codes in boot mode. • Connection with an on-chip debugging emulator can be controlled using ID codes. • ROM codes can be used for control when connecting to a parallel programmer.	• Connection with a serial programmer can be controlled using ID codes in boot mode. • Connection with an on-chip debugging emulator can be controlled using ID codes.
Start-up program protection function	This function is used to safely program blocks 0 to 7.	This function is used to safely program blocks 0 to 15.
Area protection	During self-programming, this function enables programming only of specified blocks in the user area and disables programming of the other blocks.	During self-programming, this function enables programming only of specified blocks in the user area and disables programming of the other blocks.
Background operation (BGO) function	Programs in the ROM can run while the E2 DataFlash is being programmed.	Programs in the ROM can run while the E2 DataFlash is being programmed.

Table 2.56 Comparison of Flash Memory Registers

Register	Bit	RX24T	RX13T
FCR	DRC	—	Data read complete bit
FSARH	—	Flash processing start address register H FSARH is a 16-bit register. The flash memory address for programming or erasure is set in bits b31 to b25 and b20 to b16 in this register.	Flash processing start address register H FSARH is an 8-bit register. The flash memory address for programming or erasure is set in bits b19 to b16 in this register.
FSARL	—	Flash processing start address register L The flash memory address for programming or erasure is set in bits b15 to b0 in this register. When the target is the ROM, set bits b2 to b0 to 000b.	Flash processing start address register L The flash memory address for programming or erasure is set in bits b15 to b0 in this register. When the target is the ROM, set bits b1 and b0 to 00b.
FEARH	—	Flash processing end address register H FEARH is a 16-bit register. The flash memory address for programming or erasure is set in bits b31 to b25 and b20 to b16 in this register.	Flash processing end address register H FEARH is an 8-bit register. The flash memory address for programming or erasure is set in bits b19 to b16 in this register.

Register	Bit	RX24T	RX13T
FEARL	—	Flash processing end address register L The flash memory address for programming or erasure is set in bits b15 to b0 in this register. When the target is the ROM, set bits b2 to b0 to 000b.	Flash processing end address register L The flash memory address for programming or erasure is set in bits b15 to b0 in this register. When the target is the ROM, set bits b1 and b0 to 00b.
FWBn (RX24T) FWBH, FWBL (RX13T)	—	Flash write buffer n register (n = 0 to 3)	Flash write buffer registers H and L
FRBH	—	—	Flash read buffer register H
FRBL	—	—	Flash read buffer register L
FSTATR1	DRRDY	—	Data read ready flag
FEAMH	—	Flash error address monitor register H FEAMH is a 16-bit register. This register stores bits b31 to b25 and b20 to b16 of the address where an error has occurred for the program command or blank check command, or it stores bits b31 to b25 and b20 to b16 of the start address of the area where an error has occurred for the block erase command or all-block erase command.	Flash error address monitor register H FEAMH is an 8-bit register. This register stores bits b19 to b16 of the address where an error has occurred for the program command or blank check command, or it stores bits b19 to b16 of the start address of the area where an error has occurred for the block erase command.
FSCMR	—	Flash start-up setting monitor register	Flash start-up setting monitor register
		The value after a reset differs.	
FAWSMR	—	Flash access window start address monitor register In a blank product the value after a reset of bits b11 to b0 is 1. After the access window information program command is executed these bits are set to the same value as that set in bits b11 to b0 in the FWB0 register.	Flash access window start address monitor register In a blank product the value after a reset of bits b9 to b0 is 1. After the access window information program command is executed these bits are set to the same value as that set in bits b9 to b0 in the FWBL register.
FAWEMR	—	Flash access window end address monitor register In a blank product the value after a reset of bits b11 to b0 is 1. After the access window information program command is executed these bits are set to the same value as that set in bits b11 to b0 in the FWB1 register.	Flash access window end address monitor register In a blank product the value after a reset of bits b9 to b0 is 1. After the access window information program command is executed these bits are set to the same value as that set in bits b9 to b0 in the FWBH register.
UIDRn	—	Unique ID register n (n = 0 to 3) UIDRn is a 32-bit register.	Unique ID register n (n = 0 to 31) UIDRn is an 8-bit register.
ROMCE	—	ROM cache enable register	—
ROMCIV	—	ROM cache invalidate register	—

2.21 Packages

As indicated in Table 2.57, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage.

Table 2.57 Packages

Package Type	Renesas Code	
	RX24T	RX13T
100-pin LFQFP	○	×
80-pin LQFP	○	×
80-pin LFQFP	○	×
64-pin LFQFP	○	×
48-pin LFQFP	×	○
48-pin HWQFN	×	○
32-pin LQFP	×	○
32-pin HWQFN	×	○

○: Package available (Renesas code omitted); ×: Package not available

3. Important Information when Migrating Between MCUs

This section presents important information on differences between the RX13T Group and the RX24T Group. 3.1, Notes on Functional Design, presents information regarding the software.

3.1 Notes on Functional Design

Some software that runs on the RX24T Group is compatible with the RX13T Group. Nevertheless, appropriate caution must be exercised due to differences in aspects such as operation timing and electrical characteristics.

Software-related considerations regarding function settings that differ between the RX13T Group and RX24T Group are as follows:

For differences between modules and functions, refer to 2, Comparative Overview of Specifications. For further information, refer to the User's Manual: Hardware of each MCU group, listed in 4, Reference Documents.

3.1.1 Exception Vector Table

On the RX24T Group the vector addresses are relocatable using the value set in the exception table register (EXTB) as the start address, but addresses allocated in the vector table are fixed on the RX13T Group.

3.1.2 Note on High-Speed Mode

The maximum operating frequencies when reading the flash memory in high-speed mode differ on the RX13T Group and RX24T Group. For details, refer to Table 3.1, Comparison of Maximum Operating Frequencies when Reading Flash Memory in High-Speed Mode.

Table 3.1 Comparison of Maximum Operating Frequencies when Reading Flash Memory in High-Speed Mode

Item	RX24T	RX13T
ICLK	80 MHz	32 MHz
PCLKA	80 MHz	—
PCLKB, PCLKD	40 MHz	32 MHz
FCLK	32 MHz	32 MHz

3.1.3 PB1 Pin Input Level

On the RX13T Group the input level of the PB1 pin is specified as TTL when SCL is selected by the PB1PFS.PSEL bit and SMBus is selected by the ICMR3.SMBS bit in the RIIC. At this time, the PB1 port read and IRQ2 input level is also TTL.

4. Reference Documents

User's Manual: Hardware

RX24T Group User's Manual: Hardware Rev.2.00 (R01UH0576EJ0200)
(The latest version can be downloaded from the Renesas Electronics website.)

RX13T Group User's Manual: Hardware Rev.1.00 (R01UH0822EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This module reflects the content of the following technical updates:

TN-RX*-A173A/E

TN-RX*-A194A/E

TN-RX*-A193A/E

TN-RX*-A200A/E

TN-RX*-A0206A/E

TN-RX*-A0213A/E

TN-RX*-A0216A/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Apr. 28, 2020	—	First edition issued
1.10	Nov. 5, 2021	67	2.21 Table 2.57 Packages revised and errors corrected

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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