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M32C/84 Group, M32C/8B Group

Differences between M32C/84 and M32C/8B

1. Abstract

This document describes differences between the M32C/84 144-pin package and the M32C/8B 144-pin package. Refer to each device's hardware manual or software manual for details.

2. Introduction

The document described in this document applies to the following MCUs:

- MCUs: M32C/84 144-pin package
  M32C/8B 144-pin package

Refer to the latest hardware manuals and technical updates when using this application note.

3. Differences

3.1 Differences in Functions

Table 3.1 lists differences in functions.

Table 3.1 Differences in Functions

Item		M32C/84	M32C/8B
Minimum Instruction Execution Time		•31.3 ns (f(BCLK) = 32 MHz, VCC1 = 4.2 V to 5.5 V) •41.7 ns (f(BCLK) = 24 MHz, VCC1=3.0 V to 5.5 V)	•31.3 ns (f(CPU) = 32 MHz , VCC1 = 3.0 to 5.5 V)
Supply Voltage		•VCC1 = 4.2 V to 5.5 V, VCC2 = 3.0 V to VCC1 (f(BCLK) = 32 MHz) •VCC1 = 3.0 V to 5.5 V, VCC2 = 3.0 V to VCC1 (f(BCLK) = 24 MHz)	•VCC1 = 3.0 V to 5.5 V, VCC2 = 3.0 V to VCC1
Current Consumption		•28 mA (VCC1 = VCC2 = 5 V, f(BCLK) = 32 MHz) •22 mA (VCC1 = VCC2 = 3.3 V, f(BCLK) = 24 MHz) •10 μA (VCC1 = VCC2 = 5 V, f(BCLK) = 32 kHz, in wait mode)	•26 mA (32 MHz, VCC1 = VCC2 = 5 V) •23 mA (32 MHz, VCC1 = VCC2 = 3.3 V) •110 μA (approx. 1 MHz, VCC1 = VCC2 = 3.3 V, on-chip oscillator low-power consumption mode → wait mode) •8 μA (approx. 32 kHz, VCC1 = VCC2 = 3.3 V, low-power consumption mode → wait mode) •4 μA (VCC1 = VCC2 = 3.3 V, stop mode)
Clock Generation Circuit	Maximum Frequency of the Main Clock	32 MHz	16 MHz
Power Supply Voltage Detection Circuit		Available	Not available
Power Supply Voltage Monitor Function		Not available	Available
DMAC	Trigger Sources	40	31
Intelligent I/O		Available	Not available
Timer for Three-Phase Motor Control	Count Source	f1, f8, f2n, fC32 (n = 0 to 15, no division only where n = 0)	f1
CAN Module		Available	Not available
Flash Memory	Program Method	•Per word (2-byte) •Per byte(1)	•Per 4-byte
	Erase Method	•All block erase •Block erase	•Block erase
	Number of Software Commands	8 commands	9 commands
	Data Flash	4-Kbyte × 1 (block A)	4-Kbyte × 2 (block A, block B)
	User ROM	•64-Kbyte × 7 •32-Kbyte × 1 •8-Kbyte × 3 •4-Kbyte × 2	•64-Kbyte × 4
	Boot ROM	4-Kbyte	8-Kbyte

Note:
1. Programming per byte is available in parallel I/O mode only.

3.2 Pin Characteristics

Table 3.2 lists differences in pin characteristics.

Table 3.2 Differences in Pin Characteristics

M32C/84	M32C/8B	Differences from M32C/84
P14_3/INPC1_7/OUTC1_7	P14_3	Deleted: INPC1_7/OUTC1_7
P14_2/INPC1_6/OUTC1_6	P14_2	Deleted: INPC1_6/OUTC1_6
P14_1/INPC1_5/OUTC1_5	P14_1	Deleted: INPC1_5/OUTC1_5
P14_0/INPC1_4/OUTC1_4	P14_0	Deleted: INPC1_4/OUTC1_4
P8_3/$\overline{\text{INT1}}$/CAN0IN	P8_3/$\overline{\text{INT1}}$	Deleted: CAN0IN
P8_2/$\overline{\text{INT0}}$/CAN0OUT	P8_2/$\overline{\text{INT0}}$	Deleted: CAN0OUT
P8_1/TA4IN/$\overline{\text{U}}$/INPC1_5/OUTC1_5	P8_1/TA4IN/$\overline{\text{U}}$	Deleted: INPC1_5/OUTC1_5
P8_0/TA4OUT/U/ISRXD0	P8_0/TA4OUT/U	Deleted: ISRXD0
P7_7/TA3IN/CAN0IN/INPC1_4/ OUTC1_4/ISCLK0	P7_7/TA3IN	Deleted: CAN0IN/INPC1_4/ OUTC1_4/ISCLK0
P7_6/TA3OUT/CAN0OUT/INPC1_3/ OUTC1_3/ISTXD0	P7_6/TA3OUT	Deleted: CAN0OUT/INPC1_3/ OUTC1_3/ISTXD0
P7_5/TA2IN/$\overline{\text{W}}$/INPC1_2/OUTC1_2/ ISRXD1/BE1IN	P7_5/TA2IN/$\overline{\text{W}}$	Deleted: INPC1_2/OUTC1_2/ ISRXD1/BE1IN
P7_4/TA2OUT/W/INPC1_1/ OUTC1_1/ISCLK1	P7_4/TA2OUT/W	Deleted: INPC1_1/OUTC1_1/ISCLK1
P7_3/TA1IN/$\overline{\text{V}}$/$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/$\overline{\text{SS2}}$/ INPC1_0/OUTC1_0/ISTXD1/ BE1OUT	P7_3/TA1IN/$\overline{\text{V}}$/$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/$\overline{\text{SS2}}$	Deleted: INPC1_0/OUTC1_0/ ISTXD1/BE1OUT
P7_1/TB5IN/TA0IN/RXD2/SCL2/ STXD2/INPC1_7/OUTC1_7	P7_1/TB5IN/TA0IN/RXD2/SCL2/STXD2	Deleted: INPC1_7/OUTC1_7
P7_0/TA0OUT/TXD2/SDA2/SRXD2/ INPC1_6/OUTC1_6	P7_0/TA0OUT/TXD2/SDA2/SRXD2	Deleted: INPC1_6/OUTC1_6
P11_3/INPC1_3/OUTC1_3	P11_3	Deleted: INPC1_3/OUTC1_3
P11_2/INPC1_2/OUTC1_2/ISRXD1/ BE1IN	P11_2	Deleted: INPC1_2/OUTC1_2/ ISRXD1/BE1IN
P11_1/INPC1_1/OUTC1_1/ISCLK1	P11_1	Deleted: INPC1_1/OUTC1_1/ISCLK1
P11_0/INPC1_0/OUTC1_0/ISTXD1/ BE1OUT	P11_0	Deleted: INPC1_0/OUTC1_0/ ISTXD1/BE1OUT
P15_2/ISRXD0/AN15_2	P15_2/AN15_2	Deleted: ISRXD0
P15_1/ISCLK0/AN15_1	P15_1/AN15_1	Deleted: ISCLK0
P15_0/ISTXD0/AN15_0	P15_0/AN15_0	Deleted: ISTXD0

4. Detailed Comparison

4.1 Differences in Clock

Table 4.1 lists the differences in clock and Table 4.2 lists the differences in clock associated SFR.

Table 4.1 Differences in Clock

Item	M32C/84	M32C/8B
Maximum Frequency of the Main Clock	32 MHz	16 MHz
Peripheral Function Clock	f1, f8, f32, f2n, fAD, fC32, fCAN (n = 0 to 15, no division only where n = 0)	f1, f8, f32, f2n, fAD, fC32 (n = 0 to 15, no division only where n = 0)
Flash Memory Low-speed Access	Not available	Available
PLL Clock Multiplication	Multiply-by-6 Multiply-by-8	Multiply-by-4 Multiply-by-8

Table 4.2 Differences in Clock Associated SFR

Symbol	Address		Bit	Differences	
	M32C/84	M32C/8B		M32C/84	M32C/8B
PLC0	0026h		2 to 0	Programmable counter select bits 0 1 1: Multiply-by-6 1 0 0: Multiply-by-8 Do not set to values other than the above	PLL clock multiplication factor select bits 0 1 0: Multiply-by-4 1 0 0: Multiply-by-8 Do not set to values other than the above
			4	Reserved bit Set to 1	Reference clock division rate select bits 0 0: No division 0 1: Divide-by-2 1 0: Divide-by-4 Do not set to values other than the above
			5	Reserved bit Set to 0	
			6	Reserved bit Set to 1	Reserved bit Set to 0
PM2	0013h		4	CPU clock select bit 3 0: Clock selected by the CM07 bit 1: Main clock	Reserved bits
			5	CAN clock select bit 0: f1 1: Main clock	
PLC1	0027h	–	–	Only M32C/84	–
FMR4	–	0059h	–	–	Only M32C/8B
VRCR	–	001Fh	–	–	Only M32C/8B

4.2 Differences in Protection

Table 4.3 lists the differences in protection associated SFR.

Table 4.3 Differences in Protection Associated SFR

Symbol	Address		Bit	Differences	
	M32C/84	M32C/8B		M32C/84	M32C/8B
PRCR	000Ah		0	Writing to registers CM0, CM1, CM2, MCD, PLC0 and PLC1 is enabled	Writing to registers CM0, CM1, CM2, MCD, and PLC0 is enabled
			3	Writing to registers VCR2 and D4INT is enabled	Writing to registers DVCR, LVDC, and VRCR is enabled

4.3 Differences in Interrupt

Table 4.4 lists the differences in interrupt vector and Table 4.5 lists the differences in interrupt associated SFR.

Table 4.4 Differences in Interrupt Vector

Software Interrupt Number	Vector Table Address	M32C/84	M32C/8B
44	+176 to +179 (00B0h to 00B3h)	Intelligent I/O interrupt 0	Reserved area
45	+180 to +183 (00B4h to 00B7h)	Intelligent I/O interrupt 1	
46	+184 to +187 (00B8h to 00BBh)	Intelligent I/O interrupt 2	
47	+188 to +191 (00BCh to 00BFh)	Intelligent I/O interrupt 3	
48	+192 to +195 (00C0h to 00C3h)	Intelligent I/O interrupt 4	
52	+208 to +211 (00D0h to 00D3h)	Intelligent I/O interrupt 8	
53	+212 to +215 (00D4h to 00D7h)	Intelligent I/O interrupt 9, CAN 0	
54	+216 to +219 (00D8h to 00DBh)	Intelligent I/O interrupt 10, CAN 1	
57	+228 to +231 (00E4h to 00E7h)	CAN 2	

Table 4.5 Differences in Interrupt Associated SFR

Symbol	Address		Bit	Differences	
	M32C/84	M32C/8B		M32C/84	M32C/8B
IIO0IC	0075h	–	–	Only M32C/84	–
IIO1IC	0095h	–	–	Only M32C/84	–
IIO2IC	0077h	–	–	Only M32C/84	–
IIO3IC	0097h	–	–	Only M32C/84	–
IIO4IC	0079h	–	–	Only M32C/84	–
IIO8IC	007Dh	–	–	Only M32C/84	–
IIO9IC	009Dh	–	–	Only M32C/84	–
IIO10IC	007Fh	–	–	Only M32C/84	–
CAN0IC	009Dh	–	–	Only M32C/84	–
CAN1IC	007Fh	–	–	Only M32C/84	–
CAN2IC	0081h	–	–	Only M32C/84	–
IIO0IR to IIO4IR	00A0h to 00A4h	–	–	Only M32C/84	–
IIO8IR to IIO11IR	00A8h to 00ABh	–	–	Only M32C/84	–
IIO0IE to IIO4IE	00B0h to 00B4	–	–	Only M32C/84	–
IIO8IE to IIO11IE	00B8h to 00BBh	–	–	Only M32C/84	–

4.4 Differences in DMAC

Table 4.6 lists the differences in DMAC and Table 4.7 lists the differences in DMAi request sources (i = 0 to 3).

Table 4.6 Differences in DMAC

Item	M32C/84	M32C/8B
Trigger Sources	40	31

Table 4.7 Differences in DMAi Request Sources (i = 0 to 3)

DSEL4 to DSEL0	M32C/84				M32C/8B
	DMA0	DMA1	DMA2	DMA3	DMA0 to DMA3
11001b	Intelligent I/O interrupt 0 request	–	Intelligent I/O interrupt 2 request	Intelligent I/O interrupt 9 request, CAN interrupt 0 request	Do not set to values
11010b	Intelligent I/O interrupt 1 request	Intelligent I/O interrupt 8 request	Intelligent I/O interrupt 3 request	Intelligent I/O interrupt 10 request, CAN interrupt 1 request	
11011b	Intelligent I/O interrupt 2 request	Intelligent I/O interrupt 9 request, CAN interrupt 0 request	Intelligent I/O interrupt 4 request	CAN interrupt 2 request	
11100b	Intelligent I/O interrupt 3 request	Intelligent I/O interrupt 10 request, CAN interrupt 1 request	–	Intelligent I/O interrupt 0 request	
11101b	Intelligent I/O interrupt 4 request	CAN interrupt 2 request	–	Intelligent I/O interrupt 1 request	
11110b	–	Intelligent I/O interrupt 0 request	–	Intelligent I/O interrupt 2 request	
11111b	–	Intelligent I/O interrupt 1 request	Intelligent I/O interrupt 8 request	Intelligent I/O interrupt 3 request	

4.5 Differences in Three-Phase Motor Control Timer Function

Table 4.8 lists the differences in three-phase motor control timer function and Table 4.9 lists the differences in three-phase motor control timer function associated SFR.

Table 4.8 Differences in Three-Phase Motor Control Timer Function

Item	M32C/84	M32C/8B
Count Source	f1, f8, f2n, fC32 (n = 0 to 15, no division only where n = 0)	f1

Table 4.9 Differences in Three-Phase Motor Control Timer Function Associated SFR

Symbol	Address		Bit	Differences	
	M32C/84	M32C/8B		M32C/84	M32C/8B
TA1MR TA2MR TA4MR	0357h 0358h 035Ah		7 to 6	Count source select bits 0 0: f1 0 1: f8 1 0: f2n(1) 1 1: fC32	Count source select bits Set to 00b (f1) to use the three-phase motor control timer function
TB2MR	035Dh		7 to 6	Count source select bits 0 0: f1 0 1: f8 1 0: f2n(1) 1 1: fC32	Count source select bits Set to 00b (f1) to use the three-phase motor control timer function

Note:
1. The CNT3 to CNT0 bits in the TCSPR register select no division (n = 0) or divide-by-2n (n = 1 to 15).

4.6 Differences in Serial Interface

Table 4.10 lists the differences in serial interface associated SFR.

Table 4.10 Differences in Serial Interface Associated SFR

Symbol	Address		Bit	Differences	
	M32C/84	M32C/8B		M32C/84	M32C/8B
U0SMR U1SMR U2SMR U3SMR U4SMR	0367h 02E7h 0337h 0327h 02F7h		3	SCLL sync output enable bit 0: Disabled 1: Enabled	Reserved bit
U0C0 U1C0 U2C0 U3C0 U4C0	036Ch 02ECh 033Ch 032Ch 02FCh		2	CST/RTS function select bit 0: CTS function selected 1: RTS function selected	CTS function select bit 0: CTS function selected 1: CTS function not selected
			4	CTS/RTS disable bit 0: CTS/RTS function enabled 1: CTS/RTS function disabled	CTS function disable bit 0: CTS function enabled 1: CTS function disabled

4.7 Differences in Programmable I/O Ports

Table 4.11 to Table 4.13 list the differences in programmable I/O ports associated SFR.

Table 4.11 Differences in Programmable I/O Ports Associated SFR (1/3)

Symbol	Address		Bit	Differences	
	M32C/84	M32C/8B		M32C/84	M32C/8B
PS0	03B0h		0	Port P6_0 output function select bit 0: I/O port 1: RTS0	Port P6_0 output function select bit 0: I/O port/peripheral function input 1: Select by the PSL0_0 bit
			1	Port P6_1 output function select bit 0: I/O port 1: CLK0 output	Port P6_1 output function select bit 0: I/O port/peripheral function input 1: Select by the PSL0_1 bit
			3	Port P6_3 output function select bit 0: I/O port 1: TXD0/SDA0 output	Port P6_3 output function select bit 0: I/O port/peripheral function input 1: Select by the PSL0_3 bit
			5	Port P6_5 output function select bit 0: I/O port 1: CLK1 output	Port P6_5 output function select bit 0: I/O port/peripheral function input 1: Select by the PSL0_5 bit
			7	Port P6_7 output function select bit 0: I/O port 1: TXD1/SDA1 output	Port P6_7 output function select bit 0: I/O port/peripheral function input 1: Select by the PSL0_7 bit
PS1	03B1h		7	Port P7_7 output function select bit 0: I/O port 1: Selected by the PSL1_7 bit	Port P7_7 output function select bit 0: I/O port/peripheral function input 1: Do not set to this value
PS2	03B4h		2	Port P8_2 output function select bit 0: I/O port 1: Selected by the PSL2_2 bit	Reserved bit
PS3	03B5h		0	Port P9_0 output function select bit 0: I/O port 1: CLK3 output	Port P9_0 output function select bit 0: I/O port/peripheral function input 1: Select by the PSL3_0 bit
			6	Port P9_6 output function select bit 0: I/O port 1: Selected by the PSC3_6 bit	Port P9_6 output function select bit 0: I/O port/peripheral function input 1: TXD4/SDA4 output
PSL0	03B2h		0	Reserved bits	Port P6_0 peripheral function output select bit 0: RTS0 1: Do not set to this value
			1		Port P6_1 peripheral function output select bit 0: CLK0 output 1: Do not set to this value
			3		Port P6_3 peripheral function output select bit 0: TXD0/SDA0 output 1: Do not set to this value
			5		Port P6_5 peripheral function output select bit 0: CLK1 output 1: Do not set to this value
			7		Port P6_7 peripheral function output select bit 0: TXD1/SDA1 output 1: Do not set to this value

Table 4.12 Differences in Programmable I/O Ports Associated SFR (2/3)

Symbol	Address		Bit	Differences	
	M32C/84	M32C/8B		M32C/84	M32C/8B
PSL1	03B3h		5	Port P7_5 peripheral function output select bit 0: $\overline{W}$ 1: OUTC1_2	Port P7_5 peripheral function output select bit 0: $\overline{W}$ 1: Do not set to this value
			6	Port P7_6 peripheral function output select bit 0: Selected by the PSC_6 bit 1: TA3OUT output(1)	Port P7_6 peripheral function output select bit 0: Do not set to this value 1: TA3OUT output
			7	Port P7_7 peripheral function output select bit 0: ISCLK0 output 1: OUTC1_4	Reserved bit
PSL2	03B6h		1	Port P8_1 peripheral function output select bit 0: $\overline{U}$ 1: Selected by the PSC2_1 bit	Port P8_1 peripheral function output select bit 0: $\overline{U}$ 1: Do not set to this value
			2	Port P8_2 peripheral function output select bit 0: Do not set to this value 1: Selected by the PSC2_2 bit	Reserved bit
PSL3	03B7h		0	Reserved bit	Port P9_0 peripheral function output select bit 0: CLK3 output 1: Do not set to this value
PSC	03AFh		0	Port P7_0 peripheral function output select bit 0: TXD2/SDA2 output 1: Selected by the PSD1_0 bit	Port P7_0 peripheral function output select bit 0: TXD2/SDA2 output 1: Do not set to this value
			1	Port P7_1 peripheral function output select bit 0: SCL2 output 1: Selected by the PSD1_1 bit	Port P7_1 peripheral function output select bit 0: SCL2 output 1: Do not set to this value
			3	Port P7_3 peripheral function output select bit 0: $\overline{RTS2}$ 1: OUTC1_0/ISTXD1/BE1OUT	Port P7_3 peripheral function output select bit 0: $\overline{RTS2}$ 1: Do not set to this value
			4	Port P7_4 peripheral function output select bit 0: TA2OUT output 1: OUTC1_1/ISCLK1	Port P7_4 peripheral function output select bit 0: TA2OUT output 1: Do not set to this value
			6	Port P7_6 peripheral function output select bit 0: Selected by the PSD1_6 bit 1: CAN0OUT	Reserved bit

Note:
1. When setting the PSL1_i (i=0 to 4, 6) bit to 1, set the corresponding PSC_i bit in the PSC register to 0.

Table 4.13 Differences in Programmable I/O Ports Associated SFR (3/3)

Symbol	Address		Bit	Differences	
	M32C/84	M32C/8B		M32C/84	M32C/8B
PS5	03B9h	–	–	Only M32C/84	–
PS8	03A0h	–	–	Only M32C/84	–
PS9	03A1h	–	–	Only M32C/84	–
PSC2	03ACh	–	–	Only M32C/84	–
PSC3	03ADh	–	–	Only M32C/84	–
PSD1	03A7h	–	–	Only M32C/84	–
IPS	0178h	–	–	Only M32C/84	–
IPSA	0179h	–	–	Only M32C/84	–

4.8 Differences in Flash Memory (Flash Memory Version)

4.8.1 Differences in Flash Memory

Table 4.14 lists the differences in flash memory, Table 4.15 lists the differences in flash memory associated SFR and Table 4.16 lists the differences in software commands.

Table 4.14 Differences in Flash Memory

Item	M32C/84	M32C/8B
Program Method	•Per word (2-byte) •Per byte(1)	•Per 4-byte
Erase Method	•All block erase •Block erase	•Block erase
Number of Software Commands	8 commands	9 commands
Data Flash	4-Kbyte × 1 (block A)	4-Kbyte × 2 (block A, block B)
User ROM	•64-Kbyte × 7 •32-Kbyte × 1 •8-Kbyte × 3 •4-Kbyte × 2	•64-Kbyte × 4
Boot ROM	4-Kbyte	8-Kbyte

Note:
1. Programming per byte is available in parallel I/O mode only.

Table 4.15 Differences in Flash Memory Associated SFR

Symbol	Address		Bit	Differences	
	M32C/84	M32C/8B		M32C/84	M32C/8B
FMR1	0055h		1	EW mode select bit 0: EW mode 0 1: EW mode 1	Reserved bit
FMR2	–	0052h	–	–	Only M32C/8B
FMR3	–	0050h	–	–	Only M32C/8B

Table 4.16 Differences in Software Commands

Software Command	MCUs	First Bus Cycle		Second Bus Cycle		Third Bus Cycle	
		Address	Data	Address	Data	Address	Data
Program	M32C/84	WA	xx40h	WA	WD		
	M32C/8B	WA0	xx41h	WA0	WD0	WA1	WD1
Erase all unlock block	M32C/84	FA	xxA7h	FA	xxD0h		
	M32C/8B	–					
Lock bit program	M32C/84	BA	xx77h	BA	xxD0h		
	M32C/8B	BA0	xx77h	BA0	xxD0h		
Read lock bit status	M32C/84	FA	xx71h	BA	xxD0h		
	M32C/8B(1)	FA	xx71h	BA0	xxD0h		
	M32C/8B(2)	FA	xx71h	BA1	RD0		
Protect bit program	M32C/84	–					
	M32C/8B	PBA	xx67h	PBA	xxD0h		
Read protect bit status	M32C/84	–					
	M32C/8B	FA	xx61h	PBA	RD1		

Notes:
1. When the FMR31 bit in the FMR3 register is set to 1 (read by the FMR16 bit in the FMR1 register).
2. When the FMR31 bit in the FMR3 register is set to 0 (read via the data bus).

FA: Any even address in the user ROM area
xx: 8 high-order bits of command code (ignored)

WA: Write address
WD: Write data
Set sequentially WA and WD from 00h to FEh (where the write address is byte address and even address). The page size is 256-byte.
BA: Block Address (Enter the maximum address of each block that is an even address.)

WA0: 16 low-order bits of write address
- Set the lowest 2-bit of the address to 00b.
- The address specified in the first bus cycle is the same even address as the write address specified in the second bus cycle.

WA1: 16 high-order bits of write address
- Set the lowest 2-bit of the address to 10b.
- Specify WA0 and WA1 in the consecutive even addresses.

WD0: 16 low-order bit of write data
WD1: 16 high-order bit of write data
BA0: Highest-order even address of a block
BA1: Any even address of a block
PBA: The protect bit address
RD0: Read data (bit 6 is the lock bit data)
RD1: Read data (bit 6 is the protect bit data)

4.8.2 Differences in Flash Memory Blocks

Figure 4.1 shows the differences in specifications of flash memory block.

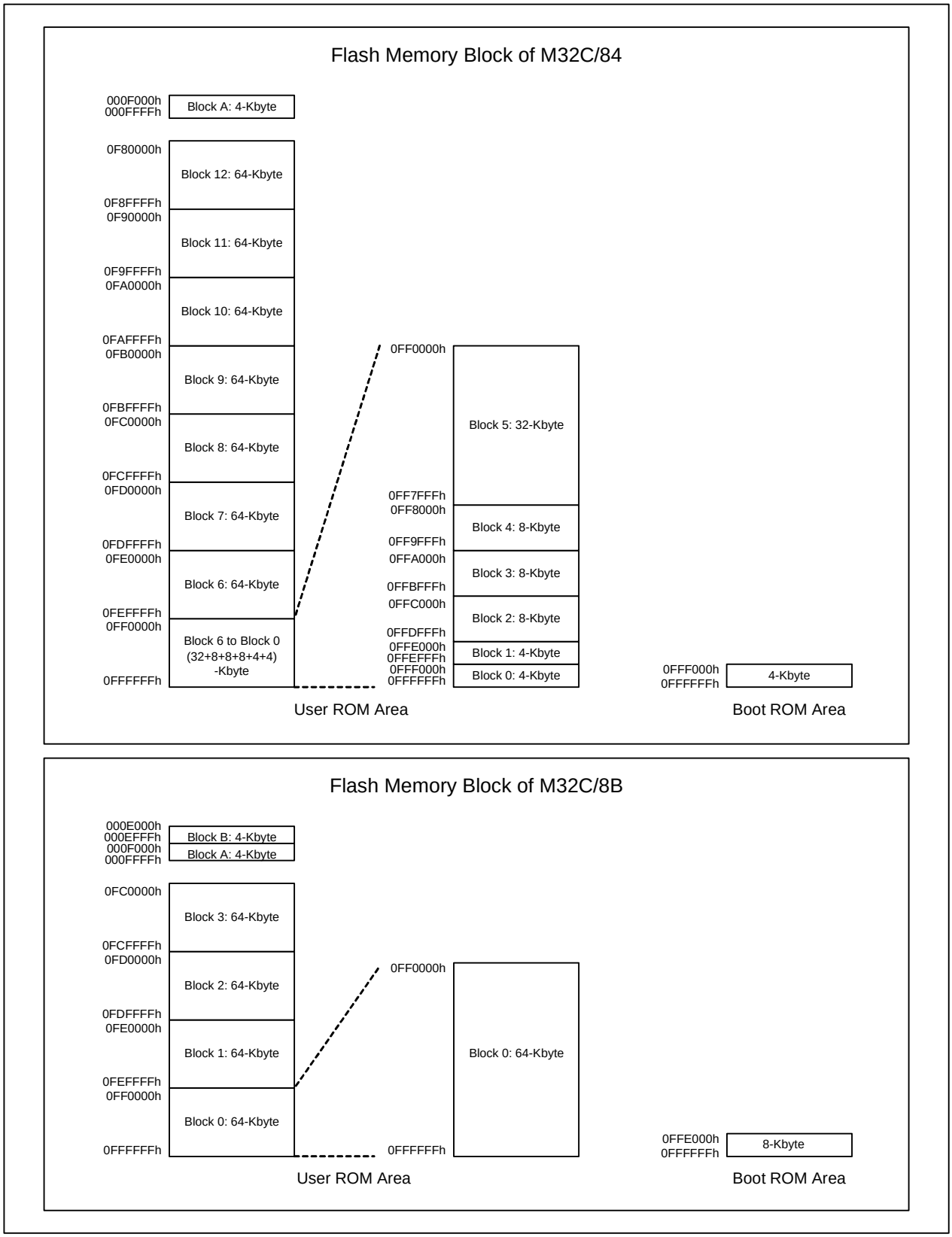

Figure 4.1 Specifications of Flash Memory Block

4.8.3 Differences in ROM Code Protection

Table 4.17 lists the differences in ROM code protection associated SFR.

Table 4.17 Differences in ROM Code Protection Associated SFR

Symbol	Address		Bit	Differences	
	M32C/84	M32C/8B		M32C/84	M32C/8B
ROMCP	0FFFFFFh	–	–	Only M32C/84	–

Each block has two protect bits in the M32C/8B flash memory. Table 4.18 lists addresses of the protect bits. If any of these protect bits is set to 0 (protected), all blocks becomes protected. To set the protect bit to 0, execute the protect bit program command. To enhance security, set all the protect bits shown in Table 4.18 to 0 when using the ROM code protect function.

Table 4.18 ROM Code Protect Function of M32C/8B

Block	Protect Bit 1	Protect Bit 0
Block B	00E300h	00E100h
Block A	00F300h	00F100h
Block 3	FC0300h	FC0100h
Block 2	FD0300h	FD0100h
Block 1	FE0300h	FE0100h
Block 0	FF0300h	FF0100h

4.9 Differences in Development Tools

Table 4.19 lists the differences in development tools.

Table 4.19 Differences in Development Tools

Tool	M32C/84	M32C/8B
Emulation Probe Emulation Pod	M30850T-EPB	R0E3308B0EPB00
Compact Emulator	M30850T2-CPE	–

5. Reference Documents

Hardware Manual
M32C/84 Group Hardware Manual Rev.1.01
M32C/8B Group Hardware Manual Rev.1.00
The latest version of these documents can be downloaded from the Renesas Technology website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Technology website.

Website and Support

Renesas Technology Website
http://www.renesas.com/

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http://www.renesas.com/inquiry
csc@renesas.com

REVISION HISTORY	M32C/84 Group, M32C/8B Group Differences between M32C/84 and M32C/8B

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