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April 1st, 2010
Renesas Electronics Corporation

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M16C/80 Group, M32C/8B Group

Differences between M16C/80 and M32C/8B

1. Abstract

This document describes differences between the M16C/80 144-pin package and the M32C/8B 144-pin package. Refer to each device's hardware manual or software manual for details.

2. Introduction

The document described in this document applies to the following MCUs:

- MCUs: M16C/80 144-pin package
  M32C/8B 144-pin package

Refer to the latest hardware manuals and technical updates when using this application note.

3. Differences

3.1 Differences in Functions

Table 3.1 and Table 3.2 list differences in functions.

Table 3.1 Differences in Functions (1/2)

Item		M16C/80	M32C/8B
Basic Instructions		106 instructions	108 instructions
Minimum Instruction Execution Time		50 ns (f(XIN) = 20 MHz)	31.3 ns (f(CPU) = 32 MHz, VCC = 3.0 to 5.5 V)
Power Supply Channels		1 channel (VCC)	2 channels (VCC1, VCC2)
Supply Voltage		•4.2 V to 5.5 V (f(XIN) = 20 MHz) •2.7 V to 5.5 V (f(XIN) = 10 MHz)	•VCC1 = 3.0 V to 5.5 V •VCC2 = 3.0 V to VCC1
Current Consumption		•45 mA (VCC = 5 V, f(XIN) = 20 MHz) •14 mA (VCC = 3.0 V, f(XIN) = 10 MHz) •1.5 μA (VCC = 3.0 V, f(XCIN) = 32 kHz, oscillation capability = Low)	•26 mA (32 MHz, VCC1 = VCC2 = 5 V) •23 mA (32 MHz , VCC1 = VCC2 = 3.3 V) •110 μA (approx. 1 MHz, VCC1 = VCC2 = 3.3 V, on-chip oscillator low-power consumption mode → wait mode) •8 μA (approx. 32 kHz, VCC1 = VCC2 = 3.3 V, low-power consumption mode → wait mode) •4 μA (VCC1 = VCC2 = 3.3 V, stop mode)
Clock Generation Circuits	Number of Circuits	2 circuits: •Main clock •Sub clock	4 circuits: •Main clock •Sub clock •On-chip oscillator •PLL frequency synthesizer
	Maximum Frequency of the Main Clock	20 MHz	16 MHz
	Oscillation Stop Detection	Not available	Main clock oscillation stop detect function
	System Clock Protect Function	Not available	Available
Power Consumption Control	Flash Memory Low-speed Access	Not available	Available (flash memory version)
	Main Voltage Regulator Stop Function	Not available	Available
Power Supply Voltage Detection		Not available	Voltage monitor interrupt (optional)(1)
Bus	Bus Wait States	No wait state to 3 wait states	1 wait state to 7 wait states
	Recovery Cycle	Not available	Insertable
	Page Mode Control Function	Not available	Available (ROMless version)
Watchdog Timer	Count Source	•BCLK (main clock, sub clock)	•CPU clock (main clock, sub clock, PLL frequency synthesizer) •On-chip oscillator clock

Note:
1. Please contact a Renesas sales office for optional features.

Table 3.2 Differences in Functions (2/2)

Item		M16C/80	M32C/8B
DMACII		Not available	Available
Timer	Count Source	f1, f8, f32, fC32	f1, f8, f2n, fC32 (n = 0 to 15, no division only where n = 0)
Timer for Three-Phase Motor Control	Count Source	f1, f8, f32, fC32	f1
	Dead Time	Enabled	Selectable from enabled and disabled
	Dead Time Trigger	Fixed	Selectable
Serial Interface	Operating Modes	•(Clock synchronous mode, clock asynchronous mode) × 2 channels •(Clock synchronous mode, clock asynchronous mode, I^2C-bus, IEBus(1) (optional(2)), SIM interface) × 3 channels	•(Clock synchronous mode, clock asynchronous mode, I^2C-bus, special mode 2, GCI mode, SIM mode, IEBus(1) (optional(2))) × 5 channels
	Count Source	f1, f8, f32	f1, f8, f2n (n = 0 to 15, no division only where n = 0)
A/D Converter	Operating Clock ϕAD	•fAD, fAD/2, fAD/4, fAD = f(XIN) (VCC = 5 V) •fAD/2, fAD/4, fAD = f(XIN) (VCC = 3 V)	•fAD, fAD/2, fAD/3, fAD/4, fAD/6, fAD/8
	Operating Modes	5 modes	7 modes
	Analog Input Pins	10 pins: •8 pins of AN_0 to AN_7 •2 extended input pins (ANEX0 and ANEX1)	34 pins: •8 pins of AN_0 to AN_7 •8 pins of AN0_0 to AN0_7 •8 pins of AN2_0 to AN2_7 •8 pins of AN15_0 to AN15_7 •2 extended input pins (ANEX0 and ANEX1)
DRAM Controller		Available	Not available
Flash Memory(3)	Rewrite Mode	•CPU rewrite mode (EW0 mode)	•EW0 mode •EW1 mode
	Program Method	In units of pages (in units of 256-byte)	In units of 4-byte
	Erase Method	•Collective erase •Block erase	•Block erase
	Number of Software Commands	8 commands	9 commands
	Data Flash	Not available	4-Kbyte × 2 (block A, block B)
	User ROM	•64-Kbyte × 3 •32-Kbyte × 1 •16-Kbyte × 1 •8-Kbyte × 2	•64-Kbyte × 4

Notes:
1. IEBus is a registered trademark of NEC Electronics Corporation.
2. Please contact a Renesas sales office for optional features.
3. Only flash memory version

3.2 Pin Characteristics

Table 3.1 lists differences in pin characteristics.

Table 3.3 Differences in Pin Characteristics

M16C/80	M32C/8B	Changes from M16C/80
VCC	VCC1, VCC2	Deleted: VCC Added: VCC1/VCC2
P7_3/$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/TA1IN/$\overline{\text{V}}$	P7_3/TA1IN/ $\overline{\text{V}}$/$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/$\overline{\text{SS2}}$	Added: $\overline{\text{SS2}}$
P7_1/RXD2/SCL2/TA0IN/TB5IN	P7_1/TA0IN/TB5IN/RXD2/SCL2/STXD2	Added: STXD2
P7_0/TXD2/SDA2/TA0OUT	P7_0/TA0OUT/TXD2/SDA2/SRXD2	Added: SRXD2
P6_7/TXD1	P6_7/TXD1/SDA1/SRXD1	Added: SDA1/SRXD1
P6_6/RXD1	P6_6/RXD1/SCL1/STXD1	Added: SCL1/STXD1
P6_4/$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{CTS0}}$/CLKS1	P6_4/$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{SS1}}$	Deleted: $\overline{\text{CTS0}}$/CLKS1 Added: $\overline{\text{SS1}}$
P6_3/TXD0	P6_3/TXD0/SDA0/SRXD0	Added: SDA0/SRXD0
P6_2/RXD0	P6_2/RXD0/SCL0/STXD0	Added: SCL0/STXD0
P6_0/$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$	P6_0/$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$/$\overline{\text{SS0}}$	Added: $\overline{\text{SS0}}$
P5_6/ALE/$\overline{\text{RAS}}$	P5_6/ALE	Deleted: $\overline{\text{RAS}}$
P5_2/$\overline{\text{RD}}$/$\overline{\text{DW}}$	P5_2/$\overline{\text{RD}}$	Deleted: $\overline{\text{DW}}$
P5_1/$\overline{\text{WRH}}$/$\overline{\text{BHE}}$/$\overline{\text{CASH}}$	P5_1/$\overline{\text{WRH}}$/$\overline{\text{BHE}}$	Deleted: $\overline{\text{CASH}}$
P5_0/$\overline{\text{WRL}}$/$\overline{\text{WR}}$/$\overline{\text{CASL}}$	P5_0/$\overline{\text{WRL}}$/$\overline{\text{WR}}$	Deleted: $\overline{\text{CASL}}$
P4_4/$\overline{\text{CS3}}$/A20 (MA12)	P4_4/$\overline{\text{CS3}}$/A20	Deleted: MA12
P4_3/A19 (MA11)	P4_3/A19	Deleted: MA11
P4_2/A18 (MA10)	P4_2/A18	Deleted: MA10
P4_1/A17 (MA9)	P4_1/A17	Deleted: MA9
P4_0/A16 (MA8)	P4_0/A16	Deleted: MA8
P3_7/A15 (MA7) (/ D15)	P3_7/A15, [A15/D15]	Deleted: MA7
P3_6/A14 (MA6) (/ D14)	P3_6/A14, [A14/D14]	Deleted: MA6
P3_5/A13 (MA5) (/ D13)	P3_5/A13, [A13/D13]	Deleted: MA5
P3_4/A12 (MA4) (/ D12)	P3_4/A12, [A12/D12]	Deleted: MA4
P3_3/A11 (MA3) (/ D11)	P3_3/A11, [A11/D11]	Deleted: MA3
P3_2/A10 (MA2) (/ D10)	P3_2/A10, [A10/D10]	Deleted: MA2
P3_1/A9 (MA1) (/ D9)	P3_1/A9, [A9/D9]	Deleted: MA1
P3_0/A8 (MA0) (/ D8)	P3_0/A8, [A8/D8]	Deleted: MA0
P0_7/D7	P0_7/AN0_7/D7	Added: AN0_7
P0_6/D6	P0_6/AN0_6/D6	Added: AN0_6
P0_5/D5	P0_5/AN0_5/D5	Added: AN0_5
P0_4/D4	P0_4/AN0_4/D4	Added: AN0_4
P0_3/D3	P0_3/AN0_3/D3	Added: AN0_3
P0_2/D2	P0_2/AN0_2/D2	Added: AN0_2
P0_1/D1	P0_1/AN0_1/D1	Added: AN0_1
P0_0/D0	P0_0/AN0_0/D0	Added: AN0_0
P15_7	P15_7/AN15_7	Added: AN15_7
P15_6	P15_6/AN15_6	Added: AN15_6
P15_5	P15_5/AN15_5	Added: AN15_5
P15_4	P15_4/AN15_4	Added: AN15_4
P15_3	P15_3/AN15_3	Added: AN15_3
P15_2	P15_2/AN15_2	Added: AN15_2
P15_1	P15_1/AN15_1	Added: AN15_1
P15_0	P15_0/AN15_0	Added: AN15_0

4. Detailed Comparison

4.1 Differences in Processor Mode

Table 4.1 lists the differences in processor mode associated SFR.

Table 4.1 Differences in Processor Mode Associated SFR

Symbol	Address		Bit	Differences	
	M16C/80	M32C/8B		M16C/80	M32C/8B
PM1	0005h		3	Reserved bit	SFR area wait bit 0: 1 wait state 1: 2 wait states
			7 to 6	Reserved bits Set to 1 (flash memory version)	Reserved bits Set to 0

4.2 Differences in Bus

Table 4.2 lists the differences in bus and Table 4.3 lists the differences in bus associated SFR.

Table 4.2 Differences in Bus

Item	M16C/80	M32C/8B
Bus Wait Status	No wait state to 3 wait states	1 wait state to 7 wait states
Recovery Cycle	Not available	Insertable
Page Mode Control Function	Not available	Available (ROMless version)

Table 4.3 Differences in Bus Associated SFR

Symbol	Address		Bit	Differences	
	M16C/80	M32C/8B		M16C/80	M32C/8B
WCR	0008h	–	–	Only M16C/80	–
EWCR0 EWCR1 EWCR2 EWCR3	–	0048h 0049h 004Ah 004Bh	–	–	Only M32C/8B
PWCR0	–	004Ch	–	–	Only M32C/8B (ROMless version)
PWCR1	–	004Dh	–	–	Only M32C/8B (ROMless version)

4.3 Differences in Clock

Table 4.4 lists the differences in clock and Table 4.5 lists the differences in clock associated SFR.

Table 4.4 Differences in Clock

Item	M16C/80	M32C/8B
Clock Generation Circuits	2 circuits: •Main clock •Sub clock	4 circuits: •Main clock •Sub clock •On-chip oscillator •PLL frequency synthesizer
Maximum Frequency of the Main Clock	20 MHz	16 MHz
Oscillation Stop Detection	Not available	Available
XCIN-XCOUT Drive Capability Select Bit	Selectable	Not available
System Clock Protect Function	Not available	Available
Flash Memory Low-speed Access	Not available	Available (flash memory version)
Main Voltage Regulator Stop Function	Not available	Available

Table 4.5 Differences in Clock Associated SFR

Symbol	Address		Bit	Differences	
	M16C/80	M32C/8B		M16C/80	M32C/8B
CM0	0006h		7	System clock select bit 0: XIN, XOUT 1: XCIN, XOUT	CPU clock select bit 0 0: Clock selected by the CM21 bit divided by the MCD register 1: Sub clock
CM1	0007h		5	XCIN-XCOUT drive capacity select bit 0: LOW 1: HIGH	Reserved bit Set to 1
			7	Reserved bit	CPU clock select bit 1 0: Main clock 1: PLL clock
CM2	–	000Dh	–	–	Only M32C/8B
PLC0	–	0026h	–	–	Only M32C/8B
PM2	–	0013h	–	–	Only M32C/8B
TCSPR	–	035Fh	–	–	Only M32C/8B
FMR4	–	0059h	–	–	Only M32C/8B (flash memory version)
VRCR	–	001Fh	–	–	Only M32C/8B

4.4 Differences in Protection

Table 4.6 lists the differences in protection associated SFR.

Table 4.6 Differences in Protection Associated SFR

Symbol	Address		Bit	Differences	
	M16C/80	M32C/8B		M16C/80	M32C/8B
PRCR	000Ah		0	Writing to registers CM0, CM1 and MCD is enabled.	Writing to registers CM0, CM1, CM2, MCD, and PLC0 is enabled.
			1	Writing to registers PM0 and PM1 is enabled.	Writing to registers PM0, PM1, PM2, INVC0, and INVC1 is enabled.
			3	No register bit	Writing to registers DVCR, LVDC, and VRCR is enabled.

4.5 Differences in Interrupt

Table 4.7 lists the differences in interrupt, Table 4.8 lists the differences in interrupt vector and Table 4.9 lists the differences in interrupt associated SFR.

Table 4.7 Differences in Interrupt

Item	M16C/80	M32C/8B
Special Interrupt	Reset NMI Watchdog timer Single step(1) Address match	Reset NMI Watchdog timer Single step(1) Address match Oscillation stop detection Voltage monitor DMACII transfer complete
Address Match Interrupt	4 addresses	8 addresses

Note:
1. Do not use these interrupts. They are for use with development tool only.

Table 4.8 Differences in Interrupt Vector

Software Interrupt Number	Vector Table Address	M16C/80	M32C/8B
17	+68 to +71 (0044h to 0047h)	UART0 transmission	UART0 transmission, NACK(1)
18	+72 to +75 (0048h to 004Bh)	UART0 reception	UART0 reception, ACK(1)
19	+76 to +79 (004Ch to 004Fh)	UART1 transmission	UART1 transmission, NACK(1)
20	+80 to +83 (0050h to 0053h)	UART1 reception	UART1 reception, ACK(1)

Note:
1. In I^2C mode, NACK, ACK or start/stop condition detection can be the interrupt sources.

Table 4.9 Differences in Interrupt Associated SFR

Symbol	Address		Bit	Differences	
	M16C/80	M32C/8B		M16C/80	M32C/8B
BCN0IC	–	0071h	–	–	Only M32C/8B
BCN1IC	–	0091h	–	–	Only M32C/8B
ADIC (AD0IC)	0073h		–	Symbol is changed from ADIC (M16C/80) to AD0IC (M32C/8B).	
RLVL	009Fh		5	No register bit	DMACII select bit 0: Interrupt priority level 7 is used for interrupt 1: Interrupt priority level 7 is used for DMACII transfer
IFSR	031Fh		6	No register bits	UART0, UART3 interrupt source select bit 0: UART3 bus conflict, start condition detection, stop condition detection 1: UART0 bus conflict, start condition detection, stop condition detection
			7		UART1, UART4 interrupt source select bit 0: UART4 bus conflict, start condition detection, stop condition detection 1: UART1 bus conflict, start condition detection, stop condition detection
RMAD4	–	0028h to 002Ah	–	–	Only M32C/8B
RMAD5	–	002Ch to 002Eh	–	–	Only M32C/8B
RMAD6	–	0038h to 003Ah	–	–	Only M32C/8B
RMAD7	–	003Ch to 003Eh	–	–	Only M32C/8B
AIER	0009h		4	No register bits	Address match interrupt 4 enable bit 0: Interrupt disabled 1: Interrupt enabled
			5		Address match interrupt 5 enable bit 0: Interrupt disabled 1: Interrupt enabled
			6		Address match interrupt 6 enable bit 0: Interrupt disabled 1: Interrupt enabled
			7		Address match interrupt 7 enable bit 0: Interrupt disabled 1: Interrupt enabled

4.6 Differences in Watchdog Timer

Table 4.10 lists the differences in watchdog timer and Table 4.11 lists the differences in watchdog timer associated SFR.

Table 4.10 Differences in Watchdog Timer

Item	M16C/80	M32C/8B
Count Source	•BCLK (main clock, sub clock)	•CPU clock (main clock, sub clock, PLL frequency synthesizer) •On-chip oscillator clock

Table 4.11 Differences in Watchdog Timer Associated SFR

Symbol	Address		Bit	Differences	
	M16C/80	M32C/8B		M16C/80	M32C/8B
PM2	–	0013h	2	–	WDT count source protect bit 0: CPU clock as count source for the watchdog timer 1: On-chip oscillator clock as count source for the watchdog timer

4.7 Differences in DMAC

Table 4.12 lists the differences in DMAC associated SFR.

Table 4.12 Differences in DMAC Associated SFR

Symbol	Address		Bit	Differences	
	M16C/80	M32C/8B		M16C/80	M32C/8B
DM0SL to DM3SL	0378h to 037Bh		4 to 0	DMA request source select bits(1) 01111: UART0 receive 10001: UART1 receive	DMA request source select bits 01111: UART0 receive interrupt or ACK interrupt request 10001: UART1 receive interrupt or ACK interrupt request

Note:
1. “DMA request cause select bit” is used in M16C/80, and this word is changed to “DMA request source select bit” in M32C/8B.

4.8 Differences in Timer A

Table 4.13 lists the differences in timer A and Table 4.14 lists the differences in timer A associated SFR.

Table 4.13 Differences in Timer A

Item	M16C/80	M32C/8B
Count Source	f1, f8, f32, fC32	f1, f8, f2n(1), fC32

Note:
1. Bits CNT3 to CNT0 in the TCSPR register select no division (n = 0) or divide-by-2n (n = 1 to 15).

Table 4.14 Differences in Timer A Associated SFR

Symbol	Address		Bit	Differences	
	M16C/80	M32C/8B		M16C/80	M32C/8B
TAiMR (i = 0 to 4)	0356h to 035Ah		7 to 6	Count source select bits 0 0: f1 0 1: f8 1 0: f32 1 1: fC32	Count source select bits 0 0: f1 0 1: f8 1 0: f2n(1) 1 1: fC32
TCSPR	–	035Fh	–	–	Only M32C/8B

Note:
1. Bits CNT3 to CNT0 in the TCSPR register select no division (n = 0) or divide-by-2n (n = 1 to 15). To select f2n, set the CST bit in the TCSPR register to 1 before setting bits TCK1 and TCK0 to 10b.

4.9 Differences in Timer B

Table 4.15 lists the differences in timer B and Table 4.16 lists the differences in timer B associated SFR.

Table 4.15 Differences in Timer B

Item	M16C/80	M32C/8B
Count Source	f1, f8, f32, fC32	f1, f8, f2n(1), fC32

Note:
1. Bits CNT3 to CNT0 in the TCSPR register select no division (n = 0) or divide-by-2n (n = 1 to 15).

Table 4.16 Differences in Timer B Associated SFR

Symbol	Address		Bit	Differences	
	M16C/80	M32C/8B		M16C/80	M32C/8B
TBiMR (i = 0 to 5)	035Bh to 035Dh, 031Bh to 031Dh		7 to 6	Count source select bits 0 0: f1 0 1: f8 1 0: f32 1 1: fC32	Count source select bits 0 0: f1 0 1: f8 1 0: f2n(1) 1 1: fC32
TCSPR	–	035Fh	–	–	Only M32C/8B

Notes:
1. Bits CNT3 to CNT0 in the TCSPR register select no division (n = 0) or divide-by-2n (n = 1 to 15). To select f2n, set the CST bit in the TCSPR register to 1 before setting bits TCK1 and TCK0 to 10b.

4.10 Differences in Three-Phase Motor Control Timer Function

Table 4.17 lists the differences in three-phase motor control timer function and Table 4.18 lists the differences in three-phase motor control timer function associated SFR.

Table 4.17 Differences in Three-Phase Motor Control Timer Function

Item	M16C/80	M32C/8B
Count Source	f1, f8, f32, fC32	f1
Dead Time	Available	Selectable
Dead Time Trigger	Fixed	Selectable

Table 4.18 Differences in Three-Phase Motor Control Timer Function Associated SFR

Symbol	Address		Bit	Differences	
	M16C/80	M32C/8B		M16C/80	M32C/8B
INVC1	0309h		5	No register bits	Dead time disable bit 0: Dead time enabled 1: Dead time disabled
			6		Dead time timer trigger select bit 0: Falling edge of one-shot pulse of timer (A4, A1 and A2) 1: Rising edge of the three-phase output shift register (U-, V-, W-phase)
			7		Reserved bit
TA1MR TA2MR TA4MR	0357h 0358h 035Ah		7 to 6	Count source select bits 0 0: f1 0 1: f8 1 0: f32 1 1: fC32	Count source select bits Set to 00b (f1) to use the three-phase motor control timer function
TB2MR	035Dh		7 to 6	Count source select bits 0 0: f1 0 1: f8 1 0: f32 1 1: fC32	Count source select bits Set to 00b (f1) to use the three-phase motor control timer function

4.11 Differences in Serial Interface

Table 4.19 lists the differences in serial interface and Table 4.20 to Table 4.24 list the differences in serial interface associated SFR.

Table 4.19 Differences in Serial Interface

Item	M16C/80	M32C/8B
Operating Modes	UART0, UART1 •Clock synchronous mode •Clock asynchronous mode (UART mode) UART2 to UART4 •Clock synchronous mode •Clock asynchronous mode •I²C-bus •IEBus(1) (optional(2)) •SIM interface	UART0 to UART4 •Clock synchronous mode •Clock asynchronous mode (UART mode) •I²C-bus •Special mode 2 •GCI mode •SIM mode •IEBus(1) (optional(2))
Count Source	f1, f8, f32	f1, f8, f2n (n = 0 to 15, no division only where n = 0)
LSB First or MSB First	•UART0, UART1 Selectable in clock synchronous mode •UART2 to UART4 Selectable in clock synchronous mode or UART mode	•UART0 to UART4 Selectable in clock synchronous mode or UART mode
Transfer Clock Output from Multiple Pins Selection	1 channel (UART1)	Not available
Separate CTS/RTS Pins	1 channel (UART0)	Not available
Serial Data Logic Inverse	3 channels (UART2 to UART4)	5 channels (UART0 to UART4)
Sleep Mode Selection	2 channels (UART0, UART1)	Not available
TXD and RXD I/O Polarity Inverse	3 channels (UART2 to UART4)	5 channels (UART0 to UART4)
Bus Conflict Detection	3 channels (UART2 to UART4)	5 channels (UART0 to UART4)
Occurrence Timing of Overrun Error	•Clock synchronous/UART mode The overrun error occurs when the next data is ready before reading the UiRB register (i = 0 to 4).	•Clock synchronous mode The overrun error occurs when the 7th bit of the next data is received before reading the UiRB register. •UART mode Overrun error occurs when the preceding bit of the final stop bit of the next data (the first stop bit when selecting 2 stop bits) is received before reading the UiRB register.
Timing of “L” Signal Output from RTSi Pin in UART Mode	At the completion of reception operation	At the completion of reading receive buffer
Automatic Generation of Start Condition or Stop Condition in I²C Mode	Not available	Available
Count Source of SDAi Delay	1/f(XIN)	UiBRG register count source

Notes:
1. IEBus is a registered trademark of NEC Electronics Corporation.
2. Please contact a Renesas sales office for optional features.

Table 4.20 Differences in Serial Interface Associated SFR (1/5)

Symbol	Address		Bit	Differences	
	M16C/80	M32C/8B		M16C/80	M32C/8B
UCON	0370h	–	–	Only M16C/80	–
U0TB	0362h to 0363h	036Ah to 036Bh	–	Different address	
U1TB	036Ah to 036Bh	02EAh to 02EBh	–	Different address	
U0RB	0366h to 0367h	036Eh to 036Fh	–	Different address	
			11	No register bit	Arbitration lost detect flag 0: Not detected (won) 1: Detected (lost)
U1RB	036Eh to 036Fh	02EEh to 02EFh	–	Different address	
			11	No register bit	Arbitration lost detect flag 0: Not detected (won) 1: Detected (lost)
U0MR U1MR	0360h 0368h	0368h 02E8h	–	Different address	
			2 to 0	Serial I/O mode select bits 0 1 0: Do not set this value.	Serial interface mode select bits 0 1 0: I^2C mode
			7	Sleep select bit •(In clock synchronous serial I/O mode) Set to 0 •(In UART mode) 0: Sleep mode deselected 1: Sleep mode selected	TXD, RXD input/output polarity switch bit 0: Not inverted 1: Inverted
U0SMR	–	0367h	–	–	Only M32C/8B
U1SMR	–	02E7h	–	–	Only M32C/8B
U2SMR U3SMR U4SMR	0337h 0327h 02F7h		3	SCLL sync output enable bit 0: Disabled 1: Enabled	Reserved bit
			7	No register bit	Clock division synchronous bit 0: External clock not divided 1: External clock divided by 2
U0SMR2	–	0366h	–	–	Only M32C/8B
U1SMR2	–	02E6h	–	–	Only M32C/8B
U2SMR2 U3SMR2 U4SMR2	0336h 0326h 02F6h		7	Start/stop condition control bit Set to 1 in selecting I^2C mode.	External clock synchronous bit 0: Not synchronized with external clock 1: Synchronized with external clock
U0SMR3	–	0365h	–	–	Only M32C/8B
U1SMR3	–	02E5h	–	–	Only M32C/8B

Table 4.21 Differences in Serial Interface Associated SFR (2/5)

Symbol	Address		Bit	Differences	
	M16C/80	M32C/8B		M16C/80	M32C/8B
U2SMR3	0335h		0	No register bits	SS function enable bit 0: SS function disabled 1: SS function enabled
			1		Clock phase set bit 0: No Clock delay 1: Clock delay
			2		Serial I/O pin set bit 0: Pins TXD2 and RXD2 selected (master mode) 1: Pins STXD2 and SRXD2 selected (slave mode)
			3		Clock output select bit 0: CLK2 is CMOS output 1: CLK2 is N-channel open drain output
			4		•Special mode 2 Mode error flag 0: No mode error 1: Mode error occurred
			7 to 5	SDA2 (TXD2) digital delay time set bits 000: No delay 0 0 1: 1-to-2 cycles of 1/f(XIN) 0 1 0: 2-to-3 cycles of 1/f(XIN) ~ 1 1 1: 7-to-8 cycles of 1/f(XIN)	SDA2 digital delay set bits SDA2 output is delayed by the following cycles. 0 0 0: No delay 0 0 1: 1-to-2 cycles of BRG count source ~ 1 1 1: 7-to-8 cycles of BRG count source
U3SMR3	0325h		7 to 5	SDA3 (TXD3) digital delay time set bits 000: No delay 0 0 1: 1-to-2 cycles of 1/f(XIN) 0 1 0: 2-to-3 cycles of 1/f(XIN) ~ 1 1 1: 7-to-8 cycles of 1/f(XIN)	SDA3 digital delay set bits SDA3 output is delayed by the following cycles. 0 0 0: No delay 0 0 1: 1-to-2 cycles of BRG count source ~ 1 1 1: 7-to-8 cycles of BRG count source
U4SMR3	02F5h		7 to 5	SDA4 (TXD4) digital delay time set bits 000: No delay 0 0 1: 1-to-2 cycles of 1/f(XIN) 0 1 0: 2-to-3 cycles of 1/f(XIN) ~ 1 1 1: 7-to-8 cycles of 1/f(XIN)	SDA4 digital delay set bits SDA4 output is delayed by the following cycles. 0 0 0: No delay 0 0 1: 1-to-2 cycles of BRG count source ~ 1 1 1: 7-to-8 cycles of BRG count source
U0SMR4	–	0364h	–	–	Only M32C/8B
U1SMR4	–	02E4h	–	–	Only M32C/8B
U2SMR4	–	0334h	–	–	Only M32C/8B
U3SMR4	–	0324h	–	–	Only M32C/8B
U4SMR4	–	02F4h	–	–	Only M32C/8B

Table 4.22 Differences in Serial Interface Associated SFR (3/5)

Symbol	Address		Bit	Differences	
	M16C/80	M32C/8B		M16C/80	M32C/8B
U0C0	0364h	036Ch	–	Different address	
			1 to 0	BRG count source select bits 1 0: f32 selected	U0BRG count source select bits 1 0: f2n selected
			2	CTS/RTS function select bit 0: CTS function selected 1: RTS function selected	CTS function select bit 0: CTS function selected 1: CTS function not selected
			4	CTS/RTS disable bit 0: CTS/RTS function enabled 1: CTS/RTS function disabled	CTS function disable bit 0: CTS function enabled 1: CTS function disabled
			7	(In UART mode) Set to 0.	(Where data length is 8-bit long in UART mode) Bit order select bit 0: LSB first 1: MSB first
U1C0	036Ch	02ECh	–	Different address	
			1 to 0	BRG count source select bits 1 0: f32 selected	U1BRG count source select bits 1 0: f2n selected
			2	CTS/RTS function select bit 0: CTS function selected 1: RTS function selected	CTS function select bit 0: CTS function selected 1: CTS function not selected
			4	CTS/RTS disable bit 0: CTS/RTS function enabled 1: CTS/RTS function disabled	CTS function disable bit 0: CTS function enabled 1: CTS function disabled
			7	Transfer format select bit (In UART mode) Set to 0.	Bit order select bit (Where data length is 8-bit long in UART mode) 0: LSB first 1: MSB first
U2C0	033Ch		1 to 0	BRG count source select bits 1 0: f32 selected	U2BRG count source select bits 1 0: f2n selected
			2	CTS/RTS function select bit 0: CTS function selected 1: RTS function selected	CTS function select bit 0: CTS function selected 1: CTS function not selected
			4	CTS/RTS disable bit 0: CTS/RTS function enabled 1: CTS/RTS function disabled	CTS function disable bit 0: CTS function enabled 1: CTS function disabled
			5	No register bit	Data output select bit 0: TXD2, SDA2 and SCL2 are CMOS output ports 1: TXD2, SDA2 and SCL2 are N-channel open drain output ports
U3C0	032Ch		1 to 0	BRG count source select bits 1 0: f32 selected	U3BRG count source select bits 1 0: f2n selected
			2	CTS/RTS function select bit 0: CTS function selected 1: RTS function selected	CTS function select bit 0: CTS function selected 1: CTS function not selected
			4	CTS/RTS disable bit 0: CTS/RTS function enabled 1: CTS/RTS function disabled	CTS function disable bit 0: CTS function enabled 1: CTS function disabled

Table 4.23 Differences in Serial Interface Associated SFR (4/5)

Symbol	Address		Bit	Differences	
	M16C/80	M32C/8B		M16C/80	M32C/8B
U4C0	02FCh		1 to 0	BRG count source select bits 1 0: f32 selected	U4BRG count source select bits 1 0: f2n selected
			2	CTS/RTS function select bit 0: CTS function selected 1: RTS function selected	CTS function select bit 0: CTS function selected 1: CTS function not selected
			4	CTS/RTS disable bit 0: CTS/RTS function enabled 1: CTS/RTS function disabled	CTS function disable bit 0: CTS function enabled 1: CTS function disabled
U0BRG	0361h	0369h	–	Different address	
U1BRG	0369h	02E9h	–	Different address	
U0C1	0365h	036Dh	–	Different address	
			4	No register bits	Transmit interrupt source select bit 0: No data in the U0TB register (TI = 1) 1: Transmit operation is completed (TXEPT = 1)
			5		Continuous receive mode enable bit 0: Continuous receive mode disabled 1: Continuous receive mode enabled
			6		Data logic select bit 0: Not inverted 1: Inverted
			7		•Special mode 3 Clock-divided synchronous stop bit 0: Synchronization stopped 1: Synchronization started •Special mode 4 Error signal output enable bit 0: Not output 1: Output
U1C1	036Dh	02EDh	–	Different address	
			4	No register bits	Transmit interrupt source select bit 0: No data in the U1TB register (TI = 1) 1: Transmit operation is completed (TXEPT = 1)
			5		Continuous receive mode enable bit 0: Continuous receive mode disabled 1: Continuous receive mode enabled
			6		Data logic select bit 0: Not inverted 1: Inverted
			7		•Special mode 3 Clock-divided synchronous stop bit 0: Synchronization stopped 1: Synchronization started •Special mode 4 Error signal output enable bit 0: Not output 1: Output

Table 4.24 Differences in Serial Interface Associated SFR (5/5)

Symbol	Address		Bit	Differences	
	M16C/80	M32C/8B		M16C/80	M32C/8B
U2C1	033Dh		5	UART2 continuous receive mode enable bit •(In UART mode) Set to 0.	Continuous receive mode enable bit 0: Continuous receive mode disabled 1: Continuous receive mode enabled
			7	Error signal output enable bit •(In clock synchronous serial I/O mode) Set to 0. •(In the UART mode) 0: Output disabled 1: Output enabled	•Special mode 3 Clock-divided synchronous stop bit 0: Synchronization stopped 1: Synchronization started •Special mode 4 Error signal output enable bit 0: Not output 1: Output
U3C1	032Dh		5	UART3 continuous receive mode enable bit •(In UART mode) Set to 0.	Continuous receive mode enable bit 0: Continuous receive mode disabled 1: Continuous receive mode enabled
			7	Error signal output enable bit •(In clock synchronous serial I/O mode) Set to 0. •(In UART mode) 0: Output disabled 1: Output enabled	•Special mode 3 Clock-divided synchronous stop bit 0: Synchronization stopped 1: Synchronization started •Special mode 4 Error signal output enable bit 0: Not output 1: Output
U4C1	02FDh		5	UART4 continuous receive mode enable bit •(In UART mode) Set to 0.	Continuous receive mode enable bit 0: Continuous receive mode disabled 1: Continuous receive mode enabled
			7	Error signal output enable bit •(In clock synchronous serial I/O mode) Set to 0. •(In UART mode) 0: Output disabled 1: Output enabled	•Special mode 3 Clock-divided synchronous stop bit 0: Synchronization stopped 1: Synchronization started •Special mode 4 Error signal output enable bit 0: Not output 1: Output
IFSR	031Fh		6	No register bits	UART0, UART3 interrupt source select bit 0: UART3 bus conflict, start condition detection, stop condition detection 1: UART0 bus conflict, start condition detection, stop condition detection
			7		UART1, UART4 interrupt source select bit 0: UART4 bus conflict, start condition detection, stop condition detection 1: UART1 bus conflict, start condition detection, stop condition detection

4.12 Differences in A/D Converter

Table 4.25 lists the differences in A/D converter and Table 4.26 and Table 4.27 list the differences in A/D converter associated SFR.

Table 4.25 Differences in A/D Converter

Item	M16C/80	M32C/8B
Maximum Operating Frequency	10 MHz	16 MHz (VCC1 = VCC2 = 5.0V)
Operating Clock ϕAD	•fAD, fAD/2, fAD/4, fAD = f(XIN) (VCC = 5 V) •fAD/2, fAD/4, fAD = f(XIN) (VCC = 3 V)	•fAD, fAD/2, fAD/3, fAD/4, fAD/6, fAD/8
Operating Modes	5 modes: •One-shot mode •Repeat mode •Single sweep mode •Repeat sweep mode 0 •Repeat sweep mode 1	7 modes: •One-shot mode •Repeat mode •Single sweep mode •Repeat sweep mode 0 •Repeat sweep mode 1 •Multi-port single sweep mode •Multi-port repeat sweep mode 0
Analog Input Pins	10 pins: •8 pins of AN_0 to AN_7 •2 extended input pins (ANEX0 and ANEX1)	34 pins: •8 pins of AN_0 to AN_7 •8 pins of AN0_0 to AN0_7 •8 pins of AN2_0 to AN2_7 •8 pins of AN15_0 to AN15_7 •2 extended input pins (ANEX0 and ANEX1)
A/D Conversion Start Condition	•Software trigger •External trigger (retrigger is enabled)	•Software trigger •External trigger (retrigger is enabled) •Hardware trigger (retrigger is enabled)
DMAC Operating Mode	Not available	Available

Table 4.26 Differences in A/D Converter Associated SFR (1/2)

Symbol	Address		Bit	Differences	
	M16C/80	M32C/8B		M16C/80	M32C/8B
ADCON0 (AD0CON0)	0396h		–	Symbol is changed from ADCON0 (M16C/80) to AD0CON0 (M32C/8B).	
			0 1 2	Analog input pin select bits 0 0 0: AN_0 is selected ~ 1 1 1: AN_7 is selected	Analog input pin select bits 0 0 0: ANi_0 is selected ~ 1 1 1: ANi_7 is selected (i = None, 0, 2 or 15)
			3 4	A/D operation mode select bits 0 0 0: One-shot mode 0 1: Repeat mode 1 0: Single sweep mode 1 1: Repeat sweep mode 0 Repeat sweep mode 1	A/D operating mode select bits 0 the MSS bit in the AD0CON3 register = 1 0 0: Do not set to this value 0 1: Do not set to this value 1 0: Multi-port single sweep mode 1 1: Multi-port repeat sweep mode 0
			5	Trigger select bit 0: Software trigger 1: ADTRG trigger	Trigger select bit 0: Software trigger 1: External trigger, hardware trigger
			7	Frequency select bit 0 0: fAD/4 is selected 1: fAD/2 is selected	Frequency select bit 0(1)

Note:

1. ϕAD is selected by the combination of the frequency select bit 0 in the AD0CON0 resister, the frequency select bit 1 in the AD0CON1 register, and the frequency select bit 2 in the AD0CON3 register. Refer to the hardware manual for details.

Table 4.27 Differences in A/D Converter Associated SFR (2/2)

Symbol	Address		Bit	Differences	
	M16C/80	M32C/8B		M16C/80	M32C/8B
ADCON1 (AD0CON1)	0397h		–	Symbol is changed from ADCON1 (M16C/80) to AD0CON1 (M32C/8B).	
			0	A/D sweep pin select bits	A/D sweep pin select bits
			1	•Single sweep mode and repeat sweep mode 0 0 0: AN0, AN1 (2 pins) ~ 1 1: AN0 to AN7 (8 pins) •Repeat sweep mode 1 0 0: AN0 (1 pin) ~ 1 1: AN0 to AN3 (4 pins)	•Single sweep mode and repeat sweep mode 0 0 0: ANi_0, ANi_1 ~ 1 1: ANi_0 to ANi_7 (i = none, 0, 2, 15) •Repeat sweep mode 1 0 0: ANi_0 ~ 1 1: ANi_0 to ANi_3 •Multi-port single sweep mode and multi-port repeat sweep mode 0 Set to 11b.
			4	Frequency select bit 1 0: fAD/2 or fAD/4 is selected. 1: fAD is selected.	Frequency select bit 1(1)
ADCON2 (AD0CON2)	0394h		–	Symbol is changed from ADCON2 (M16C/80) to AD0CON2 (M32C/8B).	
			1	Reserved bits	Analog input port select bits When the MSS bit in the AD0CON3 register = 0 0 0: AN_0 to AN_7, ANEX0, ANEX1 0 1: AN15_0 to AN15_7(2) 1 0: AN0_0 to AN0_7 1 1: AN2_0 to AN2_7 When the MSS bit in the AD0CON3 register = 1 Set to 01b.
			2		
			5	No register bit	External trigger source select bit 0: $\overline{\text{ADTRG}}$ selected 1: Timer B2 interrupt request of the three-phase motor control timer function (after the ICTB2 register completes counting) selected
AD0CON3	–	0395h	–	–	Only M32C/8B
AD0CON4	–	0392h	–	–	Only M32C/8B

Note:
1. ϕAD is selected by the combination of the frequency select bit 0 in the AD0CON0 resister, the frequency select bit 1 in the AD0CON1 register, and the frequency select bit 2 in the AD0CON3 register. Refer to the hardware manual for details.

4.13 Differences in Programmable I/O Ports

Table 4.28 to Table 4.32 list the differences in programmable I/O ports associated SFR.

Table 4.28 Differences in Programmable I/O Ports Associated SFR (1/5)

Symbol	Address		Bit	Differences	
	M16C/80	M32C/8B		M16C/80	M32C/8B
PS0	03B0h		0	Port P6_0 output function select bit 0: I/O port 1: RTS0 output	Port P6_0 output function select bit 0: I/O port/peripheral function input 1: Select by the PSL0_0 bit
			1	Port P6_1 output function select bit 0: I/O port 1: CLK0 output	Port P6_1 output function select bit 0: I/O port/peripheral function input 1: Select by the PSL0_1 bit
			2	No register bit	Port P6_2 output function select bit 0: I/O port/peripheral function input 1: Select by the PSL0_2 bit
			3	Port P6_3 output function select bit 0: I/O port 1: TXD0 output	Port P6_3 output function select bit 0: I/O port/peripheral function input 1: Select by the PSL0_3 bit
			4	Port P6_4 output function select bit 0: I/O port 1: Peripheral function output (PSL0_4 enabled)	Port P6_4 output function select bit 0: I/O port/peripheral function input 1: Select by the PSL0_4 bit
			5	Port P6_5 output function select bit 0: I/O port 1: CLK1 output	Port P6_5 output function select bit 0: I/O port/peripheral function input 1: Select by the PSL0_5 bit
			6	No register bit	Port P6_6 output function select bit 0: I/O port/peripheral function input 1: Select by the PSL0_6 bit
			7	Port P6_6 output function select bit 0: I/O port 1: TXD1 output	Port P6_7 output function select bit 0: I/O port/peripheral function input 1: Select by the PSL0_7 bit

Table 4.29 Differences in Programmable I/O Ports Associated SFR (2/5)

Symbol	Address		Bit	Differences	
	M16C/80	M32C/8B		M16C/80	M32C/8B
PS1	03B1h		0	Port P7_0 output function select bit 0: I/O port 1: Peripheral function output (PSL1_0 enabled)	Port P7_0 output function select bit 0: I/O port/peripheral function input 1: Select by the PSL1_0 bit
			1	Port P7_1 output function select bit 0: I/O port 1: SCL2 output	Port P7_1 output function select bit 0: I/O port/peripheral function input 1: Select by the PSL1_1 bit
			2	Port P7_2 output function select bit 0: I/O port 1: Peripheral function output (PSL1_2, PSC_0 enabled)	Port P7_2 output function select bit 0: I/O port/peripheral function input 1: Select by the PSL1_2 bit
			3	Port P7_3 output function select bit 0: I/O port 1: Peripheral function output (PSL1_3 enabled)	Port P7_3 output function select bit 0: I/O port/peripheral function input 1: Select by the PSL1_3 bit
			4	Port P7_4 output function select bit 0: I/O port 1: Peripheral function output (PSL1_4 enabled)	Port P7_4 output function select bit 0: I/O port/peripheral function input 1: Select by the PSL1_4 bit
			5	Port P7_5 output function select bit 0: I/O port 1: $\overline{W}$ phase output	Port P7_5 output function select bit 0: I/O port/peripheral function input 1: Select by the PSL1_5 bit
			6	Port P7_6 output function select bit 0: I/O port 1: TA3OUT output	Port P7_6 output function select bit 0: I/O port/peripheral function input 1: Select by the PSL1_6 bit
			7	No register bit	Port P7_7 output function select bit 0: I/O port/peripheral function input 1: Do not set to this value

Table 4.30 Differences in Programmable I/O Ports Associated SFR (3/5)

Symbol	Address		Bit	Differences	
	M16C/80	M32C/8B		M16C/80	M32C/8B
PS2	03B4h		1	Port P8_1 output function select bit 0: I/O port 1: $\overline{U}$ phase output	Port P8_1 output function select bit 0: I/O port/peripheral function input 1: Select by the PSL2_1 bit
PS3	03B5h		0	Port P9_0 output function select bit 0: I/O port 1: CLK3 output	Port P9_0 output function select bit 0: I/O port/peripheral function input 1: Select by the PSL3_0 bit
			2	Port P9_2 output function select bit 0: I/O port 1: TXD3 (SDA3) output	Port P9_2 output function select bit 0: I/O port/peripheral function input 1: Select by the PSL3_2 bit
PSL0	03B2h		0	No register bits	Port P6_0 peripheral function output select bit 0: $\overline{RTS0}$ 1: Do not set to this value
			1		Port P6_1 peripheral function output select bit 0: CLK0 output 1: Do not set to this value
			2		Port P6_2 peripheral function output select bit 0: SCL0 output 1: STXD0
			3		Port P6_3 peripheral function output select bit 0: TXD0/SDA0 output 1: Do not set to this value
			4	Port P6_4 peripheral function output select bit 0: $\overline{RTS1}$ output 1: CLKS1 output	Port P6_4 peripheral function output select bit 0: $\overline{RTS1}$ 1: Do not set to this value
			5	No register bits	Port P6_5 peripheral function output select bit 0: CLK1 output 1: Do not set to this value
			6		Port P6_6 peripheral function output select bit 0: SCL1 output 1: STXD
			7		Port P6_7 peripheral function output select bit 0: TXD1/SDA1 output 1: Do not set to this value

Table 4.31 Differences in Programmable I/O Ports Associated SFR (4/5)

Symbol	Address		Bit	Differences	
	M16C/80	M32C/8B		M16C/80	M32C/8B
PSL1	03B3h		0	Port P7_0 peripheral function output select bit 0: TxD2 (SDA2) port 1: TA0OUT output	Port P7_0 peripheral function output select bit 0: Select by the PSC_0 bit 1: TA0OUT output
			1	No register bit	Port P7_1 peripheral function output select bit 0: Select by the PSC_1 bit 1: STXD2
			2	Port P7_2 peripheral function output select bit 0: Port P72 peripheral subfunction select bit (PSC_0) is enabled 1: TA1OUT output	Port P7_2 peripheral function output select bit 0: Select by the PSC_2 bit 1: TA1OUT output
			3	Port P7_3 peripheral function output select bit 0 : RTS2 port 1 : V phase output	Port P7_3 peripheral function output select bit 0: Select by the PSC_3 bit 1: V
			4	Port P7_4 peripheral function output select bit 0: TA2OUT port 1: W phase output	Port P7_4 peripheral function output select bit 0: Select by the PSC_4 bit 1: W
			5	No register bits	Port P7_5 peripheral function output select bit 0: W 1: Do not set to this value
			6		Port P7_6 peripheral function output select bit 0: Do not set to this value 1: TA3OUT output
PSL2	03B6h		1	No register bit	Port P8_1 peripheral function output select bit 0: U 1: Do not set to this value
PSL3	03B7h		0	No register bit	Port P9_0 peripheral function output select bit 0: CLK3 output 1: Do not set to this value
			2	No register bit	Port P9_2 peripheral function output select bit 0: TXD3/SDA3 output 1: Do not set to this value

Table 4.32 Differences in Programmable I/O Ports Associated SFR (5/5)

Symbol	Address		Bit	Differences	
	M16C/80	M32C/8B		M16C/80	M32C/8B
PSC	03AFh		0	Port P7_2 peripheral subfunction select bit (Enabled when PS1_2 = 1 and PSL1_2 = 0) 0: CLK2 output 1: V phase output	Port P7_0 peripheral function output select bit 0: TXD2/SDA2 output 1: Do not set to this value
			1	No register bits	Port P7_1 peripheral function output select bit 0: SCL2 output 1: Do not set to this value
			2		Port P7_2 peripheral function output select bit 0: CLK2 output 1: V
			3		Port P7_3 peripheral function output select bit 0: $\overline{\text{RTS2}}$ 1: Do not set to this value
			4		Port P7_4 peripheral function output select bit 0: TA2OUT output 1: Do not set to this value
			7	Key input interrupt disable bit 0: Enabled 1: Disabled	Port P10_4 to P10_7 peripheral function input select bit 0: P10_4 to P10_7 or $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ 1: AN_4 to AN_7

Table 4.33 lists the differences in unassigned pin handling.

Table 4.33 Unassigned Pin Handling

Operation Modes	Pin Name	M16C/80	M32C/8B
Single-Chip Mode	$\overline{\text{NMI}}$	Connect the pin to VCC via a resistor	Connect the pin to VCC1 via a resistor
	AVCC	Connect the pin to VCC	Connect the pin to VCC1
Memory Expansion Mode Microprocessor Mode	$\overline{\text{HOLD}}$	Connect the pin to VCC via a resistor	Connect the pin to VCC2 via a resistor
	$\overline{\text{RDY}}$		
	$\overline{\text{NMI}}$		Connect the pin to VCC1 via a resistor
	AVCC	Connect the pin to VCC	Connect the pin to VCC1

4.14 Differences in Flash Memory (Flash Memory Version)

4.14.1 Differences in Flash Memory

Table 4.34 lists the differences in flash memory, Table 4.35 lists the differences in flash memory associated SFR and Table 4.36 lists the differences in software commands.

Table 4.34 Differences in Flash Memory

Item	M16C/80	M32C/8B
Rewrite Mode	•CPU rewrite mode (EW0 mode)	•EW0 mode •EW1 mode
Program Method	In units of pages (in units of 256-byte)	In units of 4-byte
Erase Method	•Collective erase •Block erase	•Block erase
Number of Software Commands	8 commands	9 commands
Data Flash	Not available	4-Kbyte × 2 (block A, block B)
User ROM	•64-Kbyte × 3 •32-Kbyte × 1 •16-Kbyte × 1 •8-Kbyte × 2	•64-Kbyte × 4
Status Register	Bit 3: Block status after program	Bit 3: Reserved bit

Table 4.35 Differences in Flash Memory Associated SFR

Symbol	Address		Bit	Differences	
	M16C/80	M32C/8B		M16C/80	M32C/8B
FMR0	0377h	0057h	–	Different address	
			3	Flash memory reset bit 0: Normal operation 1: Reset	Flash memory stop bit 0: Flash memory started 1: Flash memory stopped (enters low-power consumption state and flash memory is initialized)
			6	No register bits	Program status flag 0: Successfully completed 1: Terminated by error
			7		Erase status flag 0: Successfully completed 1: Terminated by error
FMR1	0376h	0055h	–	Different address	
			3	Flash memory power supply-OFF bit 0: Flash memory power supply is connected 1: Flash memory power supply-off	Reserved bit
			6	Reserved bit	Lock bit status flag 0: Locked 1: Unlocked
FMR2	–	0052h	–	–	Only M32C/8B
FMR3	–	0050h	–	–	Only M32C/8B

Table 4.36 Differences in Software Commands

Software Command	MCUs	First Bus Cycle		Second Bus Cycle		Third Bus Cycle	
		Address	Data	Address	Data	Address	Data
Page program	M16C/80	FA	xx41h	WA0	WD0	WD1	WD1
	M32C/8B	–					
Program	M16C/80	–					
	M32C/8B	WA0	xx41h	WA0	WD0	WA1	WD1
Erase all unlock block	M16C/80	FA	xxA7h	FA	xxD0h		
	M32C/8B	–					
Lock bit program	M16C/80	FA	xx77h	BA	xxD0h		
	M32C/8B	BA0	xx77h	BA0	xxD0h		
Read lock bit status	M16C/80	FA	xx71h	BA	D6		
	M32C/8B(1)	FA	xx71h	BA0	xxD0h		
	M32C/8B(2)	FA	xx71h	BA1	RD0		
Protect bit program	M16C/80	–					
	M32C/8B	PBA	xx67h	PBA	xxD0h		
Read protect bit status	M16C/80	–					
	M32C/8B	FA	xx61h	PBA	RD1		

Notes:
1. When the FMR31 bit in the FMR3 register is set to 1 (read by the FMR16 bit in the FMR1 register).
2. When the FMR31 bit in the FMR3 register is set to 0 (read via the data bus).

FA: Any even address in the user ROM area
xx: 8 high-order bits of command code (ignored)

WA: Write address
WD: Write data
Set sequentially WA and WD from 00h to FEh (where the write address is byte address and even address). The page size is 256-byte.
BA: Block Address (Enter the maximum address of each block that is an even address.)
D6: Corresponds to the block lock status. D6 = 1: Block not locked. D6 = 0: Block locked.

WA0: 16 low-order bits of write address
- Set the lowest 2-bit of the address to 00b.
- The address specified in the first bus cycle is the same even address as the write address specified in the second bus cycle.

WA1: 16 high-order bits of write address
- Set the lowest 2-bit of the address to 10b.
- Specify WA0 and WA1 in the consecutive even addresses.

WD0: 16 low-order bit of write data
WD1: 16 high-order bit of write data
BA0: Highest-order even address of a block
BA1: Any even address of a block
PBA: The protect bit address
RD0: Read data (bit 6 is the lock bit data)
RD1: Read data (bit 6 is the protect bit data)

4.14.2 Differences in Flash Memory Blocks

Figure 4.1 shows the differences in specifications of flash memory block.

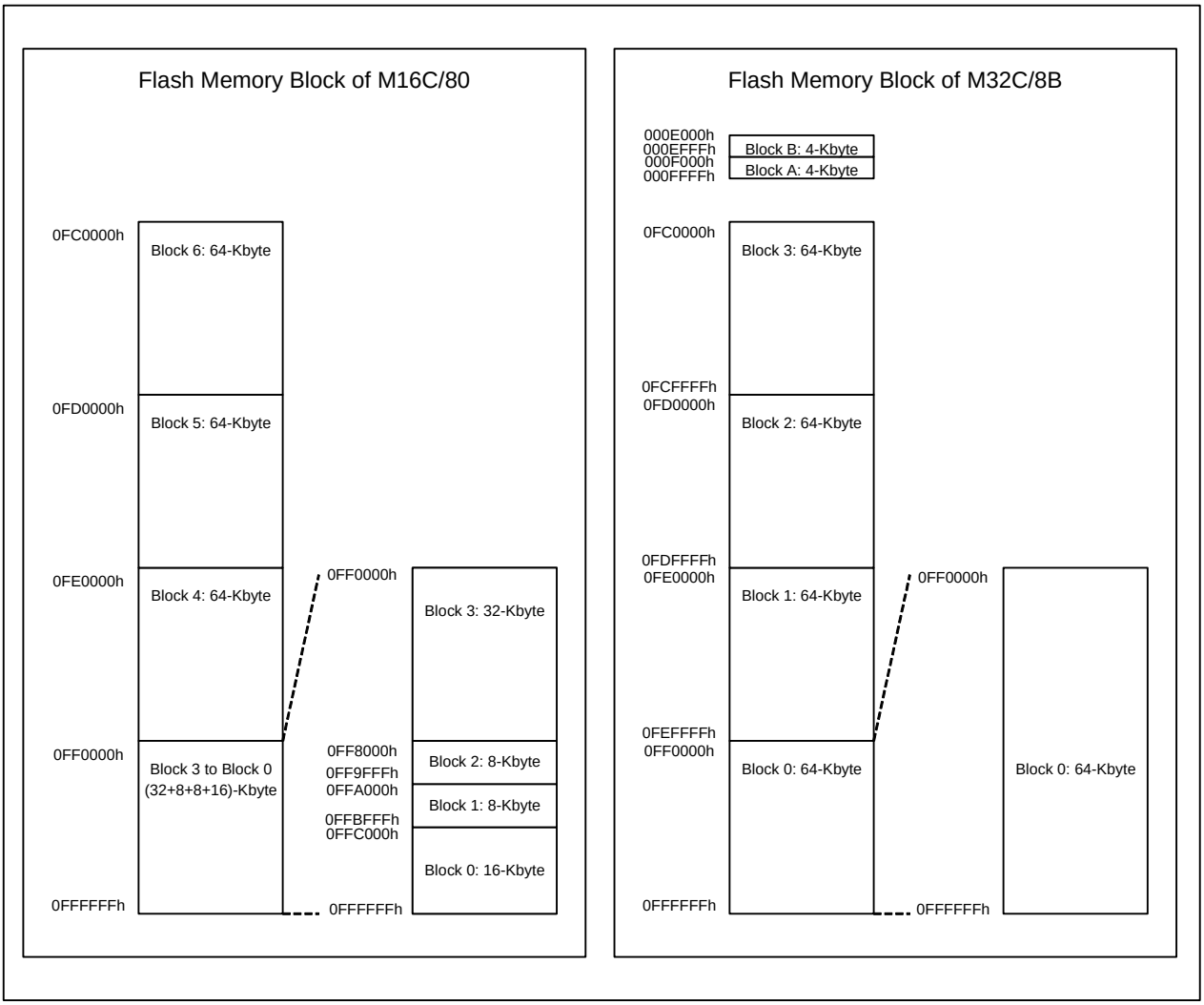

Figure 4.1 Specifications of Flash Memory Block

4.14.3 Differences in ROM Code Protection

Table 4.37 lists the differences in ROM code protection associated SFR.

Table 4.37 Differences in ROM Code Protection Associated SFR

Symbol	Address		Bit	Differences	
	M16C/80	M32C/8B		M16C/80	M32C/8B
ROMCP	0FFFFFFh	–	–	Only M16C/80	–

Each block has two protect bits in M32C/8B flash memory. Table 4.38 lists addresses of the protect bits. If any of these protect bits is set to 0 (protected), all blocks becomes protected. To set the protect bit to 0, execute the protect bit program command. To enhance security, set all the protect bits shown in Table 4.38 to 0 when using the ROM code protect function.

Table 4.38 ROM Code Protect Function of M32C/8B

Block	Protect Bit 1	Protect Bit 0
Block B	00E300h	00E100h
Block A	00F300h	00F100h
Block 3	FC0300h	FC0100h
Block 2	FD0300h	FD0100h
Block 1	FE0300h	FE0100h
Block 0	FF0300h	FF0100h

4.15 Functions Added in M32C/8B

Peripheral functions added in M32C/8B are shown as follows.

- Power supply voltage monitor function
- DMACII

4.16 Differences in Development Tools

Table 4.39 lists the differences in development tools.

Table 4.39 Differences in Development Tools

Tool	M16C/80	M32C/8B
Simulator Debugger	M3T-PD308SIM	Included C compiler package for M32C Series (M3T-NC308WA)
Emulator Debugger	M3T-PD308	PC7501 emulator debugger
Emulator	PC4701U	PC7501
Emulation Pod and Emulation Probe	M30803T-RPD-E	R0E3308B0EPB00
Compact Emulator	M30800T-CPE	–
On-Chip Debugging Emulator	M3A-0665 FoUSB	E8a

5. Reference Documents

Hardware Manual
M16C/80 Group Hardware Manual Rev.1.00
M32C/8B Group Hardware Manual Rev.1.00
The latest version of these documents can be downloaded from the Renesas Technology website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Technology website.

Website and Support

Renesas Technology Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
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REVISION HISTORY	M16C/80 Group, M32C/8B Group Differences between M16C/80 and M32C/8B

Rev.	Date	Description	
		Page	Summary
1.00	Feb. 26, 2010	–	First edition issued

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