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M16C/62P, M16C/30P Group

Differences between M16C/62P and M16C/30P

Abstract

This is the reference document to verify the differences between M16C/62P and M16C/30P.

2. Introduction

The explanation of this issue is applied to the following condition:

Applicable MCU: M16C/62P, M16C/30P

3. Contents

3.1 Function Differences

Table 3.1.1 and table 3.1.2 show the Function Differences.

Table 3.1.1 Function Differences (1) (Note1)

Item	M16C/62P	M16C/30P
Shortest instruction Execution Time	41.7ns(f(BCLK)=24MHz, VCC1=3.0 to 5.5V) 100ns(f(BCLK)=10MHz, VCC1=2.7 to 5.5V)	62.5ns(f(XIN)=16MHz, VCC=3.0 to 5.5V) 100ns(f(XIN)=10MHz, VCC=2.7 to 5.5V)
Supply Voltage	VCC1=3.0 to 5.5V, VCC2=3.0V to VCC1 (f(BCLK)=24MHz) VCC1=VCC2=2.7 to 5.5V (f(BCLK)=10MHz)	VCC1=VCC2=3.0 to 5.5V(f(XIN)=16MHz) VCC1=VCC2=2.7 to 5.5V(f(XIN)=10MHz)
I/O Power Supply	Double (VCC1, VCC2)	Single (VCC1=VCC2)
Package	80-pin, 100-pin, 128-pinplastic mold QFP	100-pinplastic mold QFP
Memory	Mask ROM Flash Memory ROMless	Mask ROM Flash Memory One time Flash Memory ROMless
Voltage Detection Circuit	Built-in Vdet3, Vdet4 detect Voltage down detect interrupt Voltage down detect reset (hardware reset 2)	None
Clock Generating Circuit	PLL, XIN, XCIN, On-chip oscillator	XIN, XCIN
System Clock Protective Function	Built-in	None (protected by protect register)
Oscillation Stop, Re-oscillation Detection Function	Built-in	None
Power Consumption	18mA(VCC1=VCC2=5V, f(BCLK)=24MHz) 8mA(VCC1=VCC2=3V, f(BCLK)=10MHz) 1.8μA(VCC1=VCC2=3V, f(XCIN)=32kHz, wait mode)	10mA(VCC=5V, f(XIN)=16MHz) 8mA(VCC=3V, f(XIN)=10MHz) 1.8μA(VCC=3V, f(XCIN)=32kHz, wait mode)
Memory Area	Memory area expandable (4M bytes)	1 M bytes fixed

Note 1: About the details and the characteristics, refer to hardware manual.



Table 3.1.2 Function Differences (2) (Note1)

Item	M16C/62P	M16C/30P
External Device Connect Area	04000h to 07FFFh (PM13=0) 08000h to 0FFFFh(PM10=0) 10000h to 26FFFh 28000h to 7FFFFh 80000h to CFFFFh (PM13=0) D0000h to FFFFh (Microprocessor mode) 04000h to 07FFFh 08000h to 0FFFFh 28000h to 7FFFFh 80000h to 7FFFFh 80000h to FFFFFh (PM13=0 or without the PM13 bit) D0000h to FFFFFh (Microprocessor mode)	
Bus Mode	Separate bus Multiplexed bus	Separate bus
Upper Address Memory Expansion Mode and Microprocessor mode	P4_0 to P4_3(A16 to A19), P3_4 to P3_7(A12 to A15) Switchable between address bus and I/O port P4_0 to P4_3(A16 to A19) Switchable between address bus and I/O port P3_4 to P3_7(A12 to A15) Can not be switched	
Access to SFR	Variable (1 to 2 waits)	1 wait fixed
Software Wait to External Area	Variable (0 to 3 waits)	Variable (0 to 1 wait)
Protect	Can be set for PM0, PM1, PM2, CM0, CM1, CM2, PLC0, INVC0, INVC1, PD9, S3C, S4C, TB2SC, PCLKR, VCR2, D4INT registers	Can be set for PM0, PM1, CM0, CM1, PD9, PCLKR registers
Watchdog Timer	Watchdog timer interrupt or watchdog timer reset is selected Count source protective mode is available	Watchdog timer interrupt No count source protective mode
INT Interrupt	6 (INTO to INT5)	5 (INTO to INT4)
Address Match Interrupt	4	2
Multifunction Timer	11 channels Timer A x 5 channels, Timer B x 6 channels	6 channels Timer A x 3 channels, Timer B x 3 channels
Timer A two-phase pulse signal processing	Function Z-phase (counter reset) input	No function Z-phase (counter reset) input
Timer Functions for Three-phase Motor Control	Built-in	None
Serial Interface (UART0 to UART2)	(UART, Clock synchronous, I ² C bus (Note 2), IEBus (Note 3)) x 3	(UART, Clock synchronous, I ² C bus (Note 2)) x 2 (UART, Clock synchronous, I ² C bus (Note 2), IEBus (Note 3)) x 1
Clock Synchronous Serial I/O (SI/O3, SI/O4)	2 channels	None
A/D Converter	10 bits x 8 channels Expandable up to 26 channels	10 bits x 8 channels Expandable up to 18 channels
A/D Converter Operation Mode	One-shot mode, Repeat mode, Single sweep mode, Repeat sweep mode 0, Repeat sweep mode 1 With External Op-amp mode	One-shot mode, Repeat mode Without External Op-amp mode
A/D Converter Input Pin	Select from ports P0, P2, P10	Select from ports P0, P10
D/A Converter	8 bits x 2 channels	None

Note 1: About the details and the characteristics, refer to hardware manual.

Note 2: I²C bus is a registered trademark of Koninklijke Philips Electronics N. V.

Note 3: IEBus is a registered trademark of NEC Electronics Corporation.



3.2 Pin function Differences

Table 3.2.1 shows the Pin Function Differences.

Table 3.2.1 Pin Function Differences

M16C/62P	M16C/30P	Remarks
P9_7/ ADTRG /SIN4	P9_7/ ADTRG	
P9_6/ANEX1/SOUT4	P9_6/ANEX1	
P9_5/ANEX0/CLK4	P9_5/ANEX0	
P9_4/DA1/TB4IN	P9_4	
P9_3/DA0/TB3IN	P9_3	
P9_2/TB2IN/SOUT3	P9_2/TB2IN	
P9_1/TB1IN/SIN3	P9_1/TB1IN	
P9_0/TB0IN/CLK3	P9_0/TB0IN	
P8_4/ INT2 /ZP	P8_4/ INT2	
P8_1/TA4IN/ U	P8_1	
P8_0/TA4OUT/U	P8_0	
P7_7/TA3IN	P7_7	
P7_6/TA3OUT	P7_6	
P7_5/TA2IN/ W	P7_5/TA2IN	
P7_4/TA2OUT/W	P7_4/TA2OUT	
P7_3/ CTS2 / RTS2 /TA1IN/ V	P7_3/ CTS2 / RTS2 /TA1IN	
P7_2/CLK2/TA1OUT/V	P7_2/CLK2/TA1OUT	
P7_1/RXD2/SCL2/TA0IN/TB5IN	P7_1/RXD2/SCL2/TA0IN	
P3_0/A8(/-/D7)	P3_0/A8	
P2_7/AN2_7/A7(/D7/D6)	P2_7/A7	
P2_6/AN2_6/A6(/D6/D5)	P2_6/A6	
P2_5/AN2_5/A5(/D5/D4)	P2_5/A5	
P2_4/AN2_4/A4(/D4/D3)	P2_4/A4	
P2_3/AN2_3/A3(/D3/D2)	P2_3/A3	
P2_2/AN2_2/A2 (/D2/D1)	P2_2/A2	
P2_1/AN2_1/A1(/D1/D0)	P2_1/A1	
P2_0/AN2_0/A0(/D0/-)	P2_0/A0	
P1_7/D15/ INT5	P1_7/D15	



3.3 SFR Differences

Table 3.3.1 and table 3.2.2 show the SFR Differences.

Table 3.3.1 SFR Differences (1)

PM0	M16C/62P	M16C/30P	Remarks
CM0	PM0	PM0	
CM1	PM1	PM1	
PRCR PRCR DBR - CM2 - VCR1 - VCR2 - CSE - PLCO - PM2 - D4INT - TBSIC - TBSIC - TBJIC, U1BCNIC U1BCNIC TBJIC, U1BCNIC U0BCNIC S3IC, INTAIC INTAIC TAJIC - TAJIC - TAJIC - FIDR - FMR1 - FMR2 - FMR3 - FMR4 - FMR0 - AIER2 - RMAD3 - PCLKR PCLKR TBSR - TA11 - TA21 - TA41 - INVC0 - INVC1 - IDB0 - <	CM0	CM0	
DBR	CM1	CM1	
CM2	PRCR	PRCR	
VCR1 - VCR2 - CSE - PLC0 - PM2 - D4INT - TB5IC - TB4IC, UBCNIC U1BCNIC TB3IC, U0BCNIC U0BCNIC S4IC, INTSIC - S3IC, INTSIC - TA3IC - TA4IC - FIDR - FMR1 - FMR0 - RMAD2 - AIER2 - RMAD3 - PCLKR PCLKR TBSR - TA41 - TA21 - TA41 - INVC0 - IDB0 - DTT -	DBR	-	
VCR2 - CSE - PLCO - PM2 - DAINT - TA3IC - SIGNAD2 - FIDR - FMR0 -	CM2	-	
CSE	VCR1	-	
PLCO - PM2 - D4INT - TB5IC - D7 D4INT - D7 D7 D4INT - D7 D7 D4INT - D7 D7 D4INT - D7	VCR2	-	
PM2	CSE	-	
D4INT -	PLC0	-	
TBSIC - TB4IC, U1BCNIC U1BCNIC U0BCNIC SAIC, INTSIC - S3IC, INT4IC INTAIC - TA4IC - FIDR - FMR1 - FMR0 - FMR0 - FMRD3 - FMRMD3 - FMLKR FEBR - TA4IC - TMB - TA4IC - TMB - TM	PM2	-	
TB4IC, U1BCNIC U1BCNIC TB3IC, U0BCNIC U0BCNIC S4IC, INT5IC - S3IC, INT4IC INT4IC TA3IC - TA4IC - FIDR - FMR1 - FMR0 - RMAD2 - AIER2 - RMAD3 - PCLKR PCLKR TBSR - TA11 - TA21 - TA41 - INVC0 - INVC1 - IDB0 - IDB1 - DTT -	D4INT	-	
TB3IC, U0BCNIC U0BCNIC S4IC, INT5IC - S3IC, INT4IC INT4IC TA3IC - TA4IC - FIDR - FMR1 - FMR0 - RMAD2 - AIER2 - RMAD3 - PCLKR PCLKR TBSR - TA11 - TA21 - TA41 - INVC0 - INVC1 - IDB0 - IDB1 - DTT -	TB5IC	-	
S4IC, INT5IC - S3IC, INT4IC INT4IC TA3IC - TA4IC - FIDR - FMR1 - FMR0 - RMAD2 - AIER2 - RMAD3 - PCLKR PCLKR TBSR - TA11 - TA21 - TA41 - INVC0 - INVC1 - IDB0 - IDB1 - DTT -	TB4IC, U1BCNIC	U1BCNIC	
S3IC, INT4IC	TB3IC, U0BCNIC	U0BCNIC	
TA3IC - TA4IC - FIDR - FMR1 - FMR0 - FMR0 - FMRD2 - FMRD2 - FMRD3 - FCLKR FCLK	S4IC, INT5IC	-	
TA4IC - FIDR - FMR1 - FMR0 - FMR0 - FMR0 - FMRD2 - FMRD2 - FMRD2 - FMRD3 - FCLKR FCL	S3IC, INT4IC	INT4IC	
FIDR - FMR1 - FMR0 - FMR0 - FMR0 - FMRD2 - FMRD2 - FMRD3 - FMR	TA3IC	-	
FMR1 - FMR0 - RMAD2 - AIER2 - RMAD3 - PCLKR PCLKR PCLKR TBSR - TA11 - TA21 - TA41 - INVCO - INVCO - IDBO - IDB1 - DTT - TA11 - T	TA4IC	-	
FMR0 - RMAD2 - AIER2 - RMAD3 - PCLKR PCLKR TBSR - TA11 - TA21 - TA41 - INVC0 - INVC1 - IDB0 - IDB1 - DTT -	FIDR	-	
RMAD2 - AIER2 - RMAD3 - PCLKR PCLKR PCLKR TBSR - TA11 - TA21 - TA41 - INVCO - INVCO - IDB0 - IDB1 - DTT -	FMR1	-	
AIER2 - RMAD3 - PCLKR PCLKR TBSR - TA11 - TA21 - TA41 - INVC0 - INVC1 - IDB0 - IDB1 -	FMR0	-	
RMAD3 - PCLKR PCLKR TBSR - TA11 - TA21 - TA41 - INVC0 - INVC1 - IDB0 - IDB1 - DTT -	RMAD2	-	
PCLKR PCLKR TBSR - TA11 - TA21 - TA41 - INVC0 - INVC1 - IDB0 - IDB1 - DTT -	AIER2	-	
TBSR - TA11 - TA21 - TA41 - INVC0 - INVC1 - IDB0 - IDB1 - DTT -	RMAD3	-	
TA11 - TA21 - TA41 - INVC0 - INVC1 - IDB0 - IDB1 - DTT -	PCLKR	PCLKR	
TA21 - TA41 - INVC0 - INVC1 - IDB0 - IDB1 - DTT -	TBSR	-	
TA41 - INVC0 - INVC1 - IDB0 - IDB1 - DTT -	TA11	-	
INVC0 - INVC1 - IDB0 - IDB1 - DTT -	TA21	-	
INVC1 - IDB0 - IDB1 - DTT -	TA41	-	
IDB0 - IDB1 - DTT -	INVC0	-	
IDB1 - DTT -	INVC1	-	
DTT -	IDB0	-	
	IDB1	-	
ICTR2	DTT	-	
10102	ICTB2	-	
TB3 -	TB3	-	
TB4 -	TB4	-	
TB5 -	TB5	-	



Table 3.3.2 SFR Differences (2)

M16C/62P	M16C/30P	Remarks
TB3MR	-	
TB4MR	-	
TM5MR	-	
IFSR2A	IFSR2A	
IFSR	IFSR	
S3TRR	-	
S3C	-	
S3BRG	-	
S4TRR	-	
S4C	-	
S4BRG	-	
TABSR	TABSR	
ONSF	ONSF	
TRGSR	TRGSR	
UDF	UDF	
TA3	-	
TA4	-	
TA3MR	-	
TA4MR	-	
TB2SC	-	
DM0SL	DM0SL	
DM1SL	DM1SL	
ADCON2	ADCON2	
ADCON0	ADCON0	
ADCON1	ADCON1	
DA0	-	
DA1	-	
DACON	-	
PUR3	-	



3.4 Interrupt Vector Differences

Table 3.4.1 shows the Fixed Vector Table Differences. Table 3.4.2 shows the Relocatable Vector Table Differences.

Table 3.4.1 Fixed Vector Table Differences

M16C/62P Interrupt Factor	M16C/30P Interrupt Factor
Watchdog timer	Watchdog timer
Oscillation stop and re-oscillation detection	
Voltage down detection	

Table 3.4.2 Relocatable Vector Table Differences

M16C/62P Interrupt Factor	M16C/30P Interrupt Factor	Software Interrupt Number
Timer B5	-	5
Timer B4, UART1 bus collision detect	UART1 bus collision detect	6
Timer B3, UART0 bus collision detect	UART0 bus collision detect	7
SI/O4, INT5	-	8
SI/O3, INT4	ĪNT4	9
Timer A3	-	24
Timer A4	-	25



4. Reference

HARDWARE MANUAL

M16C/62P Group Hardware manual Rev.2.41 M16C/30P Group Hardware manual Rev.1.21

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REVISION HISTORY

Rev.	Date	Description	
		Page Summary	
1.00	Sep 01, 2004	-	First Edition issued.
1.01	Mar 25, 2005	1	Table 3.1.1 Function Differences is revised.
1.10	Nov 01, 2005	1	Table 3.1.1 Function Differences is revised, and Processor Mode deleted.
		2	Table 3.1.2 Function Differences is revised, and Bus Mode added.
		3	Table 3.2.1 Pin Function Differences is partly revised and deleted
		4	Table 3.3.1 SFR Differences is partly deleted.
1.11	Jan 16, 2007	1	Add Flash Memory, One time Flash Memory (M16C/30P)



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