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7548/7549 Group, 7546/7547 Group

Differences between 7548/49 Group and 7546/47 Group

1. Differences between 7548/49 Group and 7546/47 Group

	7546/47 0	Group	7548/49 Group	
	7546	7547	7548	7549
Applicable Product	M37546G2-XXXGP/HP/SP M37546G2GP/HP/SP M37546G4-XXXGP/HP/SP M37546G4GP/HP/SP	M37547G2-XXXFP M37547G2FP M37547G4-XXXFP M37547G4FP	M37548G3-XXXFP M37548G3FP M37548G2-XXXFP M37548G2FP M37548G1-XXXFP M37548G1FP	M37549G3-XXXFP M37549G3FP M37549G2-XXXFP M37549G2FP M37549G1-XXXFP M37549G1FP
Package	PLQP0032GB-A(32P6U-A) PWQN0036KA-A(36PJW-A) PRDP0032BA-A(32P4B)	PRSP0036GA-A (36P2R-A)	PLSP0020JB-A (20P2F-A)	PRSP0024GA-A (24P2Q-A)
ROM Type: ROM/RAM Size (Bytes)	QzROM: 8K/384 (for G2) QzROM: 16K/512 (for G4)		QzROM: 2K/192 (for G1) QzROM: 4K/256 (for G2) QzROM: 6K/256 (for G3)	
Programmable I/O	25	29	15	19
LED Ports	16 (Total electrical current: 80 mA)		8	•
Interrupts	18 sources, 16 vectors (six external sources)		12 sources, 12 vectors (four external sources)	
Timer	8-bit x 2 (Timer 1, X)		8-bit x 2 (Timer 1, 2)	
	16-bit x 2 (Timer A, B)		16-bit x 1 (Timer A)	
Output Compare	4-channels		3-channels	
Input Capture	2-channels		1-channel	
Serial Interface	8-bit x 2 (UART or Clock-synchronized)		8-bit x 1 (UART or Clos	ck-synchronized)
A/D Converter	10-bit x 6-channels 10-bit x 8-channels		10-bit x 6-channels	10-bit x 8-channels
On-Chip Oscillator	2MHz(Typ.)		High-speed: 4MHz(Typ Low-speed: 250kHz(Typ	



2. Pin configuration of 7548/49 Group and 7546/47 Group

The 7548/49 Group and 7546/47 Group are NOT pin compatible. The differences of the pin configuration and package type are indicated below.

7546/47 Group Pin Configuration & Package Type



Package type: PLQP0032GB-A (32P6U-A)









Package type: PWQN0036KA-A (36PJW-A)



Package type: PRSP0036GA-A (36P2R-A)





7548/49 Group Pin Configuration & Package Type

Package type: PRSP0024GA-A (24P2Q-A)



Package type: PLSP0020JB-A (20P2F-A)

3. SFR of 7548/49 Group and 7546/47 Group

The differences of the SFRs between the 7548/49 Group and 7546/47 Group are indicated below.



7548/7549 Group, 7546/7547 Group Differences between 7548/49 and 7546/47 Group

7546/47 Group

7548/49 Group

		1040/40 Oloup
0000 ₁₆	Port P0 (P0)	Port P0 (P0)
0001 ₁₆	Port P0 direction register (P0D)	Port P0 direction register (P0D)
0002 ₁₆	Port P1 (P1)	Port P1 (P1)
0003 ₁₆	Port P1 direction register (P1D)	Port P1 direction register (P1D)
0004 ₁₆	Port P2 (P2)	Port P2 (P2)
0005_{16}^{10}	Port P2 direction register (P2D)	Port P2 direction register (P2D)
0006 ₁₆	Port P3 (P3)	Port P3 (P3) *only 7549
0007 ₁₆	Port P3 direction register (P3D)	Port P3 direction register (P3D) *only 7549
0008 ₁₆	Reserved	Reserved
0009 ₁₆	Reserved	Reserved
000A ₁₆	Interrupt source set register (INTSET)	Reserved
$000B_{16}$	Interrupt source discrimination register (INTDIS)	
$000C_{16}$	Capture register 0 (low-order) (CAP0L)	Port P0 drive capacity control register (DCCR)
$000D_{16}$	Capture register 0 (high-order) (CAP0H)	Port P0 Pull-up control register (PULL0)
$000E_{16}$	Capture register 1 (low-order) (CAP1L)	Port P1 Pull-up control register (PULL1)
$000F_{16}$	Capture register 1 (high-order) (CAP1H)	Key-on wake-up input select register(KEYS)
0010 ₁₆	Compare register (low-order) (CMPL)	Capture/Compare register (low-order) (CRAL)
0011_{16}^{10}	Compare register (high-order) (CMPH)	Capture/Compare register (high-order) (CRAH)
0012 ₁₆	Capture/compare register R/W pointer (CCRP)	Capture/Compare register R/W pointer (CCRP)
0013 ₁₆	Capture software trigger register (CSTR)	Compare output mode register (CMOM)
0014 ₁₆	Compare register re-load register (CMPR)	Timer A (low-order) (TAL)
0015 ₁₆	Port P0P3 drive capacity control register (DCCR)	Timer A (high-order) (TAH)
0016 ₁₆	Pull-up control register (PULL)	Reserved
0017 ₁₆	Port P1P3 control register (P1P3C)	Reserved
0018 ₁₆	Transmit 1 /Receive 1 buffer register (TB1/RB1)	Transmit/Receive buffer register (TB/RB)
0019 ₁₆	Serial I/O1 status register (SIO1STS)	Serial I/O status register (SIOSTS)
001A ₁₆	Serial I/O1 control register (SIO1CON)	Serial I/O control register (SIOCON)
001B ₁₆	UART1 control register (UART1CON)	UART control register (UARTCON)
001C ₁₆	Baud rate generator 1 (BRG1)	Baud rate generator (BRG)
001D ₁₆	Timer A, B mode register (TABM)	Reserved
001E ₁₆	Capture/compare port register (CCPR)	Reserved
$001F_{16}$	Timer source selection register (TMSR)	Reserved
002016	Capture mode register (CAPM)	Reserved
0021 ₁₆	Compare output mode register (CMOM)	Reserved
002216	Capture/compare status register (CCSR)	Reserved
0023 ₁₆	Compare interrupt source set register (CISR)	Reserved
002416	Timer A (low-order) (TAL)	Reserved
0025 ₁₆	Timer A (high-order) (TAH)	Reserved
0026 ₁₆	Timer B (low-order) (TBL)	Reserved
0027_{16}	Timer B (high-order) (TBH)	Reserved
002816	Prescaler 1 (PRE1)	Prescaler 12 (PRE12)
0029 ₁₆	Timer 1 (T1)	Timer 1 (T1)
$002A_{16}$	Timer count source set register (TCSS)	Timer 2 (T2)
$002B_{16}$	Timer X mode register (TXM)	Timer mode register (TM)
$002C_{16}$	Prescaler X (PREX)	Timer count source set register (TCSS)
$002D_{16}$	Timer X (TX)	Compare register re-load register (CMPR)
-		



7548/7549 Group, 7546/7547 Group Differences between 7548/49 and 7546/47 Group

	7546/47 Group	7548/49 Group				
002E ₁₆	Transmit 2 / Receive 2 buffer register (TB2/RB2)	Capture/compare port register (CCPR)				
$002F_{16}$	Serial I/O2 status register (SIO2STS)	Capture/compare status register (CCSR)				
0030 ₁₆	Serial I/O2 control register (SIO2CON)	Compare interrupt source set register (CISR)				
0031 ₁₆	UART2 control register (UART2CON)	Capture software trigger register (CSTR)				
003216	Baud rate generator 2 (BRG2)	Capture mode register (CAPM)				
0033 ₁₆	Reserved	Reserved				
0034 ₁₆	A/D control register (ADCON)	A/D control register (ADCON)				
0035_{16}	A/D conversion register (low-order) (ADL)	A/D conversion register (low-order) (ADL)				
0036 ₁₆	A/D conversion register (high-order) (ADH)	A/D conversion register (high-order) (ADH)				
0037_{16}	OSC division ratio selection register (RODR)	Clock mode register (CLKM)				
0038_{16}	MISRG	Oscillation stop detection register (CLKSTP)				
0039 ₁₆	Watchdog timer control register (WDTCON)	Watchdog timer control register (WDTCON)				
$003A_{16}$	Interrupt edge selection register (INTEDGE)	Interrupt edge selection register (INTEDGE)				
$003B_{16}$	CPU mode register (CPUM)	CPU mode register (CPUM)				
$003C_{16}$	Interrupt request register 1 (IREQ1)	Interrupt request register 1 (IREQ1)				
$003D_{16}$	Interrupt request register 2 (IREQ2)	Interrupt request register 2 (IREQ2)				
$003E_{16}$	Interrupt control register 1 (ICON1)	Interrupt control register 1 (ICON1)				
$003F_{16}$	Interrupt control register 2 (ICON2)	Interrupt control register 2 (ICON2)				

Note : Do not access to the SFR reserved area.

: New SFR in 7548/49 : Changed in 7548/49

: Only in 7546/47

4. Interrupt vector of 7548/49 Group and 7546/47 Group

Interrupt sources and interrupt vector addresses are changed to the 7548/49 Group with additional registers as indicated below. The bits in interrupt request registers and interrupt control registers are also changed. (Please refer to their datasheet for the detail information)

Vector address		Duiquity	7546/47 Choun Interment Source	7549/40 Choun Interment Source
High-order	Low-order	Priority	7546/47 Group Interrupt Source	7548/49 Group Interrupt Source
FFFD ₁₆	FFFC ₁₆	1	Reset	Reset
FFFB ₁₆	FFFA ₁₆	2	Serial I/O1 receive	Serial I/O receive
FFF9 ₁₆	FFF8 ₁₆	3	Serial I/O1 transmit	Serial I/O transmit
FFF7 ₁₆	FFF6 ₁₆	4	Serial I/O2 receive	INT ₀
FFF5 ₁₆	FFF4 ₁₆	5	Serial I/O2 transmit	INT ₁
FFF3 ₁₆	FFF2 ₁₆	6	INT ₀	Key-on wake-up
FFF1 ₁₆	FFF0 ₁₆	7	INT ₁	Capture
FFEF ₁₆	FFEE ₁₆	8	Key-on wake-up / UART1 bus collision detection	Compare
FFED ₁₆	FFEC ₁₆	9	CNTR ₀	Timer A
FFEB ₁₆	FFEA ₁₆	10	Capture 0	Timer 2
FFE9 ₁₆	FFE8 ₁₆	11	Capture 1	A/D conversion
FFE7 ₁₆	FFE6 ₁₆	12	Compare	Timer 1
FFE5 ₁₆	FFE4 ₁₆	13	Timer X	Reserved area
FFE3 ₁₆	FFE2 ₁₆	14	Timer A	Reserved area
FFE1 ₁₆	FFE0 ₁₆	15	Timer B	Reserved area
FFDF ₁₆	FFDE ₁₆	16	A/D conversion / Timer 1	Reserved area
FFDD ₁₆	FFDC ₁₆	17	BRK instruction	BRK instruction

7546/47 Group and 7548/49 Group Difference =



5. Clock generating circuit of 7548/49 Group and 7546/47 Group

The differences of clock generating circuit between the 7548/49 Group and 7546/47 Group are indicated below.



Figure 1 7546/47 Group Clock Generating Circuit Block Diagram



Figure 2 7548/49 Group Clock Generating Circuit Block Diagram



6. Timer of 7548/49 Group and 7546/47 Group

The differences of Timers between the 7548/49 Group and 7546/47 Group are indicated below. Compared with the 7546/47 Group, some functions of the timer 2 are reduced in the 7548/49 Group, and the compare modulation output function is also reduced in Timer A of the 7548/49 Group.

Timer 1 (Prescaler 1)	Count source: f(XIN)/16 or f(RING)/16 (set using the CPUM register)	Timer 1 (Prescaler 12)	Count source: $f(\phi \text{SOURCE})/16$, or $f(X_{CIN}):32$ kHz quartz crystal oscillation (set using the CLKM and TCSS register)	
Timor V	Count source: f(XIN)/16, f(XIN)/2, f(XIN) (set using the TCSS register)		Count source: $f(\phi SOURCE)/16$, $f(\phi SOURCE)/256$, Prescaler 12 output, Timer A underflow (set using the CLKM and TCSS register)	
Timer X (Prescaler X)	 Timer X has four operating modes: (set using the TXM register) (1) Timer mode (2) Pulse output mode (3) Event counter mode (4) Pulse width measurement mode 	Timer 2 (Prescaler 12)	 Timer 2 has two operating modes: (set using the TM register) (1) Timer mode (2) Pulse output mode 	
Timer A/B (16-bit)	Count source: f(XIN)/16, f(XIN)/2, f(XIN)/32,f(XIN)/64,f(XIN)/128, f(XIN)/256, or on-chip oscillator output(only timerA), timer A underflow(only timer B) (set using the TCSS register)	Timer A (16-bit)	Count source: $f(_{\phi}SOURCE)/16$, $f(_{\phi}SOURCE)/2$, $f(_{\phi}SOURCE)/32$, $f(_{\phi}SOURCE)/64$, $f(_{\phi}SOURCE)/128$, $f(_{\phi}SOURCE)/256$, $f(LSOCO)$, $f(X_{CIN})$ (set using the CLKM and TCSS register)	
	Timers A/B have three operating modes: (set using the TABM register)		Timer A has three operating modes:	
	 (1) Timer mode (2) Output compare mode (Normal or Modulation output) (3) Input capture mode 		 (1) Timer mode (2) Output compare mode (only Normal output) (3) Input capture mode 	

7546/47 Group Timer

7548/49 Group Timer

7. Notes

Each product has different oscillation circuit constants of $X_{IN}-X_{OUT}$ and $X_{CIN}-X_{COUT}$. Consult with an oscillator manufacturer when deciding on an oscillator and oscillation circuit constants. For products used in mass production, make sure a stable operation clock is obtained from the user system and usage (especially when being used in wide voltage and temperature ranges). When designing a circuit, we recommend the user refer to the feedback resistor, dumping resistor, and load capacity trace routing. In addition, although compatibility in characteristics is fully considered when designing each device, actual values such as operating margin, A/D conversion accuracy, noise immunity, and noise radiation may be different within the range of electrical characteristics due to different manufacturing processes. Therefore, perform thorough system evaluations for each product before starting mass production.



8. Reference Document

Hardware manual 7546 Group datasheet (Rev.1.21) 7547 Group datasheet (Rev.1.21) 7548 Group datasheet (Rev.2.01) 7549 Group datasheet (Rev.2.01) (Download the latest version from the Renesas Technology website.)

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Revision Record

Rev.	Date		Description	
Nev.	Dale	Page	Summary	
1.00	Aug.21.06	-	First edition issued	
	1	The content of "Function Set ROM Data" column in table deleted.		
			The number of interrupts of 7548/49 group in table revised.	
2.00 Oct.30.	Oct.30.07	7	The figure 2 updated.	
2.00	2.00 001.30.07	8	The table content of 7548/49 group updated.	
			The part of "Notes" supplemented.	
		9	The revision of the datasheets updated.	



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