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7546/47 Group, 7544 Group (QzROM version)

Differences Between 7546/47 Group and 7544 Group (QzROM version)

1. Differences Between 7546/47 Group and 7544 Group (QzROM version)

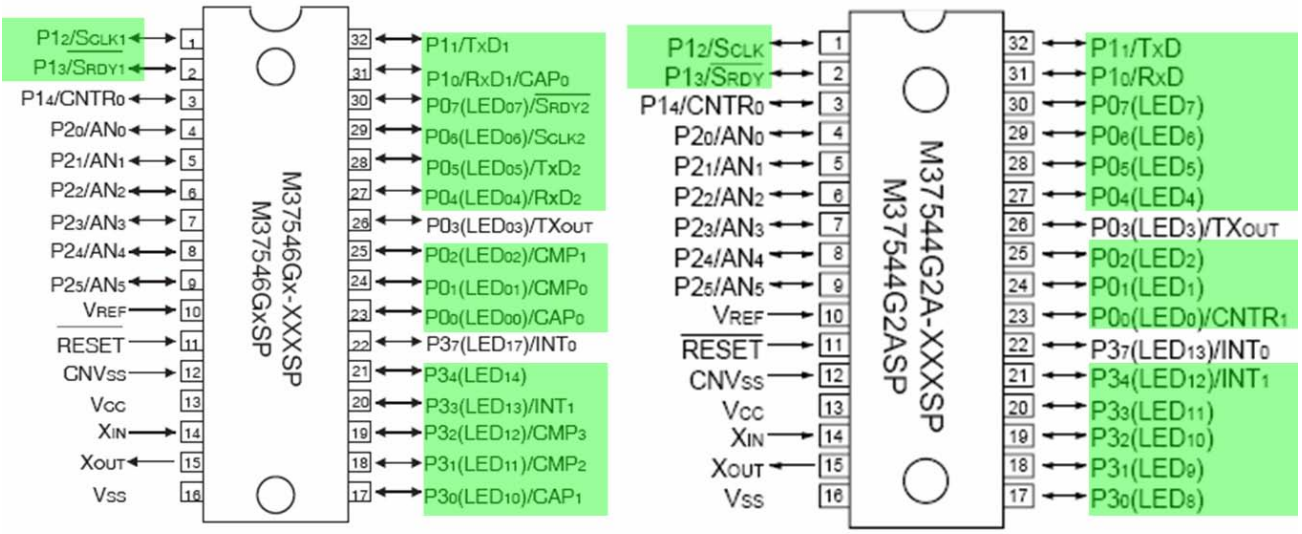
Table 1 Differences Between 7546/47 Group and 7544 Group (QzROM version)

		7546 Group	7547 Group	7544 Group (QzROM version)
Applicable Product		M37546GxGP/SP/HP M37546Gx-XXXGP/SP/HP	M37547GxFP M37547Gx-XXXFP	M37544G2A-XXXGP/SP M37544G2ASP/GP
Package		PRDP0032BA-A (Previous name 32P4B): 32-pin SDIP PLQP0032GB-A (Previous name 32P6U-A): 32-pin LQFP PWQN0036KA-A (Previous name 36PJW-A): 36-pin WQFN	PRSP0036GA-B (Previous name 36P2R-D): 36-pin SSOP	PRDP0032BA-A (Previous name 32P4B): 32-pin SDIP PLQP0032GB-A (Previous name 32P6U-A): 32-pin LQFP
ROM Type: ROM/RAM Size (bytes)		QzROM: 8K/384 bytes, 16K/512 bytes	QzROM: 8K/384 bytes, 16K/512 bytes	QzROM: 8K/256 bytes
Programmable I/O Port		25	29	25
Interrupts		18 sources, 16 vectors	18 sources, 16 vectors	12 sources, 12 vectors
Timer		8-bit × 2 16-bit × 2	8-bit × 2 16-bit × 2	8-bit × 2 16-bit × 1
Clock Generating Circuit		Built-in	Built-in	Built-in
Watchdog Timer		16-bit × 1	16-bit × 1	16-bit × 1
Output Compare		4-channels	4-channels	Not built-in
Input Capture		2-channels	2-channels	Not built-in
Serial Interface		8-bit × 2	8-bit × 2	8-bit × 1
A/D Converter		10-bit × 6ch	10-bit × 8ch	8-bit × 6ch
Power-on Reset		Built-in	Built-in	Not built-in
Low Voltage Detection Circuit		Built-in	Built-in	Not built-in
Function Set ROM Area		Addresses $FFD4_{16}$ to $FFDB_{16}$	Addresses $FFD4_{16}$ to $FFDB_{16}$	Address $FFD4_{16}$
Function Set ROM Data		Built-in	Built-in	Not built-in
	Oscillation Mode Selection	Selected by ROM data or program	Selected by ROM data or program	Selected by program
	Stop of On-chip Oscillator Disabled	Available	Available	Not available
	Selection of STP Instruction Function	Selected by ROM data or program	Selected by ROM data or program	Selected by program
	Watchdog Timer H Count Source	Selected by ROM data or program	Selected by ROM data or program	Selected by program
	Watchdog Timer Source Clock	Can be selected	Can be selected	Source clock is fixed
	Start of Watchdog Timer	Can start automatically after reset	Can start automatically after reset	Starts by program

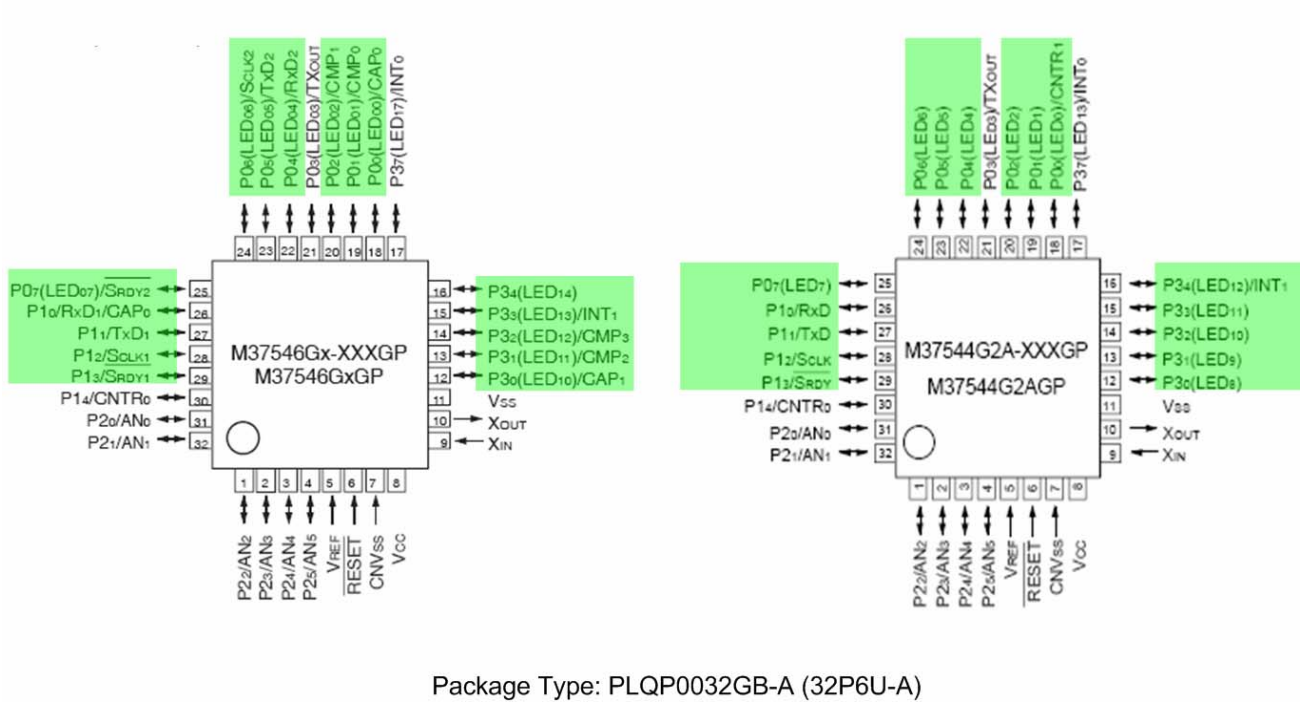
※ Please refer to each MCUs datasheet for detailed information.

2. Pin Configuration

7546 Group/7544 Group (QzROM version) difference =

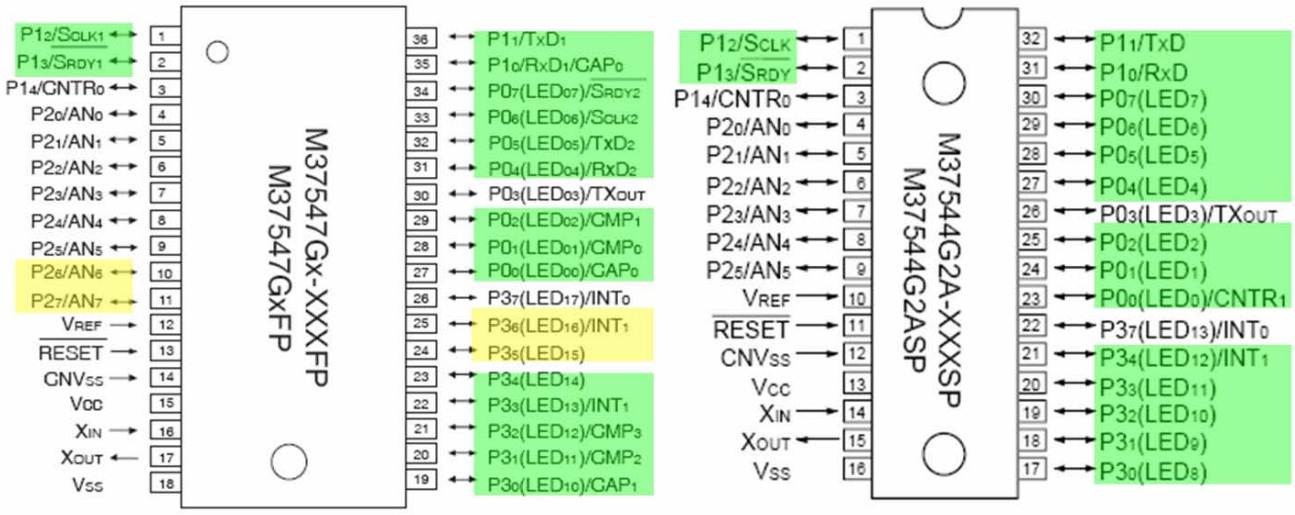


Package Type: PRDP0032BA-A (32P4B)



Package Type: PLQP0032GB-A (32P6U-A)

36-pin SSOP package is not available in the 7544 Group (QzROM version).
32-pin SDIP is compared for reference only. The pin numbers do not match.
7546/47 Group, 7544 Group (QzROM version) difference =
Reduced I/O ports in the 7544 Group (QzROM version) =



Package Type: PRSP0036GA-B (36P2R-D)

Package Type: PRDP0032BA-A (32P4B)

3. Memory Map of 7546/47 Group and 7544 Group (QzROM version)

Both 7546/47 Group and 7544 Group (QzROM version) have the function set ROM area, but the contents of these two Groups are different.

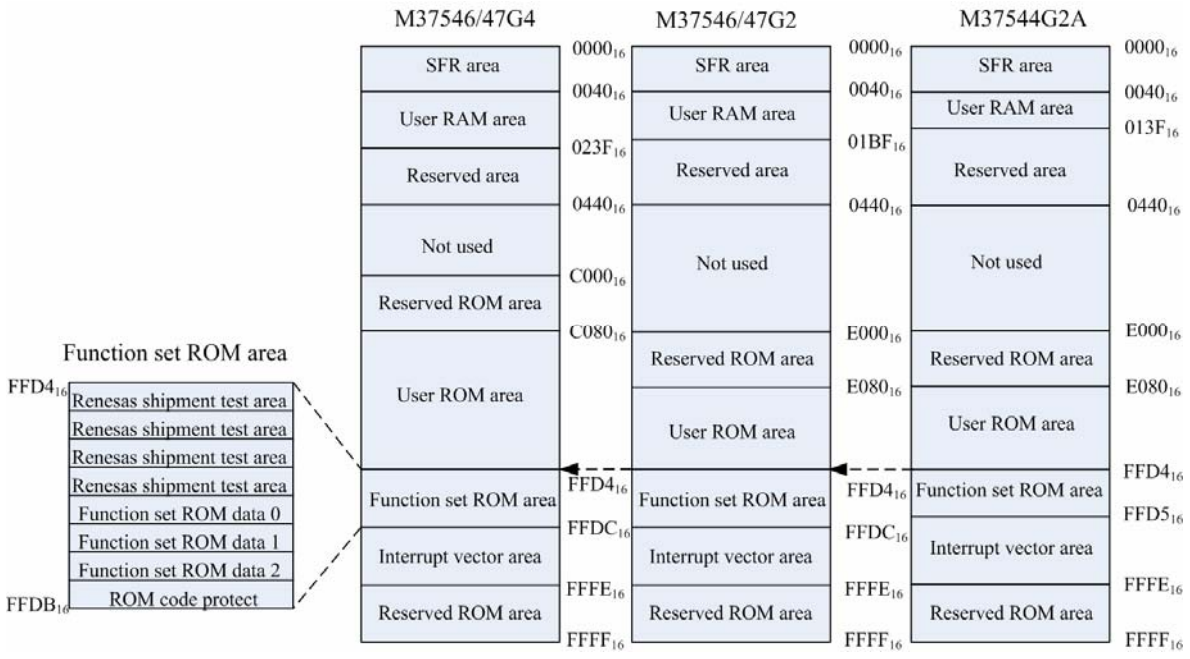
In 7546/47 Group, $FFD4_{16}$ to $FFDB_{16}$ are allocated as the function set ROM area and this area is divided into the following three areas.

— Renesas shipment test area is the area which random data are written in when shipment test is performed by Renesas.

— Function set ROM area is to start watchdog timer, disable STP instruction, or select clock to be active immediately after releasing reset.

— ROM code protect area is to disable the reading of the built-in QzROM area by serial programmer.

For 7544 Group (QzROM version), the function set ROM area which is only located in $FFD4_{16}$ is functioned as ROM code protect area.



4. Interrupt Vector of 7546/47 Group and 7544 Group (QzROM version)

Table 2 Differences of Interrupt Vector Between 7546/47 Group and 7544 Group (QzROM version)

Difference between 7546/47 Group and 7544 Group (QzROM version) =

Vector Addresses (Note 1)		7546/47 Group		7544 Group (QzROM version)	
High-order	Low-order	Priority	Interrupt Source	Priority	Interrupt Source
$FFFD_{16}$	$FFFC_{16}$	1	Reset (Note 2)	1	Reset (Note 2)
$FFFB_{16}$	$FFFA_{16}$	2	Serial I/O1 receive	2	Serial I/O receive
$FFF9_{16}$	$FFF8_{16}$	3	Serial I/O1 transmit	3	Serial I/O transmit
$FFF7_{16}$	$FFF6_{16}$	4	Serial I/O2 receive	4	INT0
$FFF5_{16}$	$FFF4_{16}$	5	Serial I/O2 transmit	5	INT1
$FFF3_{16}$	$FFF2_{16}$	6	INT0	6	Key-on wake-up
$FFF1_{16}$	$FFF0_{16}$	7	INT1	7	CNTR0
$FFEF_{16}$	$FFEE_{16}$	8	Key-on wake-up/UART1 bus collision detection (Note 3)	8	CNTR1
$FFED_{16}$	$FFEC_{16}$	9	CNTR0	9	Timer X
$FFEB_{16}$	$FFEA_{16}$	10	Capture0	—	Reserved area
$FFE9_{16}$	$FFE8_{16}$	11	Capture1	—	Reserved area
$FFE7_{16}$	$FFE6_{16}$	12	Compare	10	Timer A
$FFE5_{16}$	$FFE4_{16}$	13	Timer X	—	Reserved area
$FFE3_{16}$	$FFE2_{16}$	14	Timer A	11	A/D conversion
$FFE1_{16}$	$FFE0_{16}$	15	Timer B	12	Timer 1
$FFDF_{16}$	$FFDE_{16}$	16	A/D conversion/Timer 1 (Note 4)	—	Reserved area
$FFDD_{16}$	$FFDC_{16}$	17	BRK instruction	13	BRK instruction

Notes:
1. Vector addresses contain internal jump destination addresses.
2. Reset function is same way as an interrupt with the highest priority.
3. Key-on wake-up interrupt and UART1 bus collision detection interrupt can be enabled by setting interrupt source set register. The occurrence of these interrupts is discriminated by interrupt source discrimination register.
4. A/D conversion interrupt and Timer 1 interrupt can be enabled by setting interrupt source set register. The occurrence of these interrupt are discriminated by interrupt source discrimination register.

5. SFR of 7546/47 Group and 7544 Group (QzROM version)

Table 3 Differences of SFR Between 7546/47 Group and 7544 Group (QzROM version)

Changed function =
New function =
Same function different address =
Same function different register name =

	7546/47 Group	7544 Group (QzROM version)
0000_{16}	Port P0 (P0)	Port P0 (P0)
0001_{16}	Port P0 direction register (P0D)	Port P0 direction register (P0D)
0002_{16}	Port P1 (P1)	Port P1 (P1)
0003_{16}	Port P1 direction register (P1D)	Port P1 direction register (P1D)
0004_{16}	Port P2 (P2)	Port P2 (P2)
0005_{16}	Port P2 direction register (P2D)	Port P2 direction register (P2D)
0006_{16}	Port P3 (P3)	Port P3 (P3)
0007_{16}	Port P3 direction register (P3D)	Port P3 direction register (P3D)
0008_{16}	Reserved	Reserved
0009_{16}	Reserved	Reserved
$000A_{16}$	Interrupt source set register (INTSET)	Reserved
$000B_{16}$	Interrupt source discrimination register (INTDIS)	Reserved
$000C_{16}$	Capture register 0 (low-order)(CAP0L)	Reserved
$000D_{16}$	Capture register 0 (high-order)(CAP0H)	Reserved
$000E_{16}$	Capture register 1 (low-order)(CAP1L)	Reserved
$000F_{16}$	Capture register 1 (high-order)(CAP1H)	Reserved
0010_{16}	Compare register (low-order)(CMPL)	Reserved
0011_{16}	Compare register (high-order)(CMPH)	Reserved
0012_{16}	Capture/compare register R/W pointer (CCRP)	Reserved
0013_{16}	Capture software trigger register (CSTR)	Reserved
0014_{16}	Compare register re-load register (CMPR)	Reserved
0015_{16}	Port P0P3 drive capacity conrol register (DCCR)	Reserved
0016_{16}	Pull-up control register (PULL)	Pull-up control register (PULL)
0017_{16}	Port P1P3 control register (P1P3C)	Port P1P3 control register (P1P3C)
0018_{16}	Transmit 1/Receive 1 buffer register (TB1/RB1)	Transmit/Receive buffer register (TB/RB)
0019_{16}	Serial I/O1 status register (SIO1STS)	Serial I/O status register (SIOSTS)
$001A_{16}$	Serial I/O1 control register (SIO1CON)	Serial I/O control register (SIOCON)
$001B_{16}$	UART1 control register (UART1CON)	UART control register (UARTCON)
$001C_{16}$	Baud rate generator 1 (BRG1)	Baud rate generator (BRG)
$001D_{16}$	Timer A, B mode register (TABM)	Timer A mode register (TAM)
$001E_{16}$	Capture/compare port register (CCPR)	Timer A register (low-order)(TAL)

	7546/47 Group	7544 Group (QzROM version)
$001F_{16}$	Timer source selection register (TMSR)	Timer A register (high-order)(TAH)
0020_{16}	Capture mode register (CAPM)	Reserved
0021_{16}	Compare output mode register (CMOM)	Reserved
0022_{16}	Capture/compare status set register (CCSR)	Reserved
0023_{16}	Compare interrupt source set register (CISR)	Reserved
0024_{16}	Timer A register (low-order)(TAL)	Reserved
0025_{16}	Timer A register (high-order)(TAH)	Reserved
0026_{16}	Timer B register (low-order)(TBL)	Reserved
0027_{16}	Timer B register (high-order)(TBH)	Reserved
0028_{16}	Prescaler 1 (PRE1)	Prescaler 1 (PRE1)
0029_{16}	Timer 1 (T1)	Timer 1 (T1)
$002A_{16}$	Timer counter source set register (TCSS)	Reserved
$002B_{16}$	Timer X mode register (TXM)	Timer X mode register (TXM)
$002C_{16}$	Prescaler X (PREX)	Prescaler X (PREX)
$002D_{16}$	Timer X (TX)	Timer X (TX)
$002E_{16}$	Transmit 2/Receive 2 buffer register (TB2/RB2)	Timer counter source set register 1 (TCSS1)
$002F_{16}$	Serial I/O2 status register (SIO2STS)	Timer counter source set register 2 (TCSS2)
0030_{16}	Serial I/O2 control register (SIO2CON)	Reserved
0031_{16}	UART2 control register (UART2CON)	Reserved
0032_{16}	Baud rate generator 2 (BRG2)	Reserved
0033_{16}	Reserved	Reserved
0034_{16}	A/D control register (ADCON)(Note)	A/D control register (ADCON)(Note)
0035_{16}	AD conversion register (low-order)(ADL)	A/D register (AD)
0036_{16}	AD conversion register (high-order)(ADH)	Reserved
0037_{16}	On-chip oscillation division ratio selection register (RODR)	Reserved
0038_{16}	MISRG	MISRG
0039_{16}	Watchdog timer control register (WDTCON)	Watchdog timer control register (WDTCON)
$003A_{16}$	Interrupt edge selection register (INTEDGE)	Interrupt edge selection register (INTEDGE)
$003B_{16}$	CPU mode register (CPUM)	CPU mode register (CPUM)
$003C_{16}$	Interrupt request register 1 (IREQ1)	Interrupt request register 1 (IREQ1)
$003D_{16}$	Interrupt request register 2 (IREQ2)	Interrupt request register 2 (IREQ2)
$003E_{16}$	Interrupt control register 1 (ICON1)	Interrupt control register 1 (ICON1)
$003F_{16}$	Interrupt control register 2 (ICON2)	Interrupt control register 2 (ICON2)

Note: 8 channels A/D converter is available in 7547 Group, only 6 channels A/D converter is available in 7544 Group (QzROM version) and 7546 Group.

6. Notes on Replacing 7544 Group (QzROM version) with 7546/47 Group

1. Pin configuration

— When replacing 7544 Group (QzROM version) with 7546/47 Group, the number of CNTR pins of 7546/47 Group is different from 7544 Group (QzROM version).

— INT1 is assigned to different port.

2. Timer function

Three timers (Timer1, Timer X, Timer A) are available in 7544 Group (QzROM version). Four timers (Timer 1, Timer X, Timer A, Timer B) are available in 7546/47 Group. The differences in timers are as follows:

Table 4 Differences of Timers Between 7546/47 Group and 7544 Group (QzROM version)

Timer	7546/47 Group			7544 Group (QzROM version)		
	Count Source	Function	Related Register	Count Source	Function	Related Register
Timer 1	Oscillation frequency divided by 16	Timer mode	PRE1 T1	f(XIN)/16 f(XIN)/2 On chip oscillation (Note1)	Timer mode	PRE1 T1 TCSS2
Timer X	f(XIN)/16 f(XIN)/2 f(XIN) (Note2)	Timer mode Pulse output mode Event counter mode Pulse width measurement mode	PREX TX TXM TCSS	f(XIN)/16 f(XIN)/2 f(XIN) (Note2)	Timer mode Pulse output mode Event counter mode Pulse width measurement mode	PREX TX TXM TCSS1
Timer A	f(XIN)/16 f(XIN)/2 f(XIN)/32 f(XIN)/64 f(XIN)/128 f(XIN)/256	Timer mode	TAH TAL TABM TCSS	f(XIN)/16 f(XIN)/2 On chip oscillation (Note1)	Timer mode Pulse output mode Event counter mode Pulse width HL countinously measurement mode	TAH TAL TAM TCSS2
Timer B	f(XIN)/16 f(XIN)/2 f(XIN)/32 f(XIN)/64 f(XIN)/128 f(XIN)/256	Timer mode	TBH TBL TABM TCSS	Not available	Not available	Not available

Notes: – System operates using an on-chip oscillator as a count source by setting the on-chip oscillator to oscillation enabled by bit 3 of CPUM.
– f(XIN) can be used as Timer X count source when using a ceramic resonator or on-chip oscillator. Do not use it at RC oscillation.

3. Except for the interrupt vectors of RESET, Serial I/O and BRK, other interrupt vectors of 7544 Group (QzROM version) are all different from 7546/47 Group (Refer to Table 2 for details).
4. The bit definitions of the following (Refer to Page 8) registers are different. Setting measure for corresponding function should be noticed when replacing 7544 Group (QzROM version) with 7546/47 Group.
5. Contact an oscillator manufacturer. Select an oscillator and oscillation circuit constants to obtain the stabilized operation clock on the user system and its condition for mass-production since oscillation circuit constants of XIN-XOUT are different every product.

Address (Register Name)	Bit	7544 Group (QzROM version)	7546/47 Group
PULL (0016_{16}) (Pull-up control register)	Bit 1	P01 pull-up control bit	P01, P02 pull-up control bit
	Bit 2	P02, P03 pull-up control bit	P03, P07 pull-up control bit
	Bit 3	P04-P07 pull-up control bit	P30 pull-up control bit
	Bit 4	P30-P33 pull-up control bit	P31, P32 pull-up control bit
	Bit 5	P34 pull-up control bit	P33 pull-up control bit
	Bit 6	Reserved bit	P34 pull-up control bit *only 7546 P34, P35 pull-up control bit *only 7547
	Bit 7	Reserved bit	Reserved bit *only 7546 P36, P37 pull-up control bit *only 7547
P1P3C (0017_{16}) (Port P1P3 control register)	Bit 1	P34/INT1 input level selection bit	Set "0" to this bit certainly *only 7546 P36/INT1 input level selection bit *only 7547
	Bit 2	P10, P12 input level selection bit	P10, P12, P13 input level selection bit
MISRG (0038_{16})	Bit 2	Reserved bit	Oscillation stop reset bit
	Bit 3	Reserved bit	Oscillation stop detection status bit
	Bit 7	Oscillation stop detection status bit	Reserved bit
WDTCON (0039_{16}) (Watchdog timer control register)	Bit 7	Watchdog timer H count source selection bit 0: Wachdog timer L underflow 1: f(XIN)/16	Watchdog timer H count source selection bit 0: Wachdog timer L underflow 1: On-chip oscillator/16 or f(XIN)/16
INTEDGE ($003A_{16}$) (Interrupt edge selection register)	Bit 2	Reserved bit	Set "1" to this bit certainly
	Bit 5	Reserved bit	P00 key-on wakeup enable bit
	Bit 6	Reserved bit	P04 key-on wakeup enable bit
	Bit 7	P00 key-on wakeup enable bit	P06 key-on wakeup enable bit
IREQ1 ($003C_{16}$) (Interrupt request register 1)	Bit 0	Serial I/O receive interrupt request bit	Serial I/O1 receive interrupt request bit
	Bit 1	Serial I/O transmit interrupt request bit	Serial I/O1 transmit interrupt request bit
	Bit 2	INT0 interrupt request bit	Serial I/O2 receive interrupt request bit
	Bit 3	INT1 interrupt request bit	Serial I/O2 transmit interrupt request bit
	Bit 4	Key-on wake up interrupt request bit	INT0 interrupt request bit
	Bit 5	CNTR0 interrupt request bit	INT1 interrupt request bit
	Bit 6	CNTR1 interrupt request bit	Key-on wake up/UART1 bus collision detection interrupt request bit
	Bit 7	Timer X interrupt request bit	CNTR0 interrupt request bit
IREQ2 ($003D_{16}$) (Interrupt request register 1)	Bit 0	Reserved bit	Capture 0 interrupt request bit
	Bit 1	Reserved bit	Capture 1 interrupt request bit
	Bit 2	Timer A interrupt request bit	Compare interrupt request bit
	Bit 3	Reserved bit	Timer X interrupt request bit
	Bit 4	A/D conversion interrupt request bit	Timer A interrupt request bit
	Bit 5	Timer 1 interrupt request bit	Timer B interrupt request bit
	Bit 6	Reserved bit	A/D conversion/Timer 1 interrupt request bit
ICON1 ($003E_{16}$) (Interrupt control register 1)	Bit 0	Serial I/O receive interrupt enable bit	Serial I/O1 receive interrupt enable bit
	Bit 1	Serial I/O transmit interrupt enable bit	Serial I/O1 transmit interrupt enable bit
	Bit 2	INT0 interrupt enable bit	Serial I/O2 receive interrupt enable bit
	Bit 3	INT1 interrupt enable bit	Serial I/O2 transmit interrupt enable bit
	Bit 4	Key-on wake up interrupt enable bit	INT0 interrupt enable bit
	Bit 5	CNTR0 interrupt enable bit	INT1 interrupt enable bit
	Bit 6	CNTR1 interrupt enable bit	Key-on wake up/UART1 bus collision detection interrupt enable bit
	Bit 7	Timer X interrupt enable bit	CNTR0 interrupt enable bit
ICON2 ($003F_{16}$) (Interrupt control register 2)	Bit 0	Reserved bit	Capture 0 interrupt enable bit
	Bit 1	Reserved bit	Capture 1 interrupt enable bit
	Bit 2	Timer A interrupt enable bit	Compare interrupt enable bit
	Bit 3	Reserved bit	Timer X interrupt enable bit
	Bit 4	A/D conversion interrupt enable bit	Timer A interrupt enable bit
	Bit 5	Timer 1 interrupt enable bit	Timer B interrupt enable bit
	Bit 6	Reserved bit	A/D conversion/Timer 1 interrupt enable bit

7. Reference Documents

Datasheets
7544 Group (QzROM version) Datasheet
7546 Group Datasheet
7547 Group Datasheet
The latest version can be downloaded from the Renesas Technology website.

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Apr.13.07	—	First edition issued
1.01	Mar.21.08	All pages	7544 Group→7544 Group (QzROM version)
		1	In Table 1, modified the applicable product name and ROM type of 7544 Group (QzROM version)
		3	Deleted the note for INT1
		7	Revised note 1 and added note 5

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