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April 1st, 2010
Renesas Electronics Corporation

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455A Group, 4559 Group

Differences between 455A Group and 4559 Group

1. The Performance Overview Differences

Parameter		Function	
		455A Group	4559 Group
Number of basic instructions		138 (SBK*, RBK*, TW5A, TA5W instructions added, CRCK instruction deleted)	135
ROM type		QzROM	← The same as 455A Group
ROM size		8192 words × 10 bit (M3455AG8FP / M3455AG8-XXXFP) 12288 words × 10 bit (M3455AGCFP / M3455AGC-XXXFP)	6144 words × 10 bit (M34559G6FP / M34559G6-XXXFP)
RAM size		512 words × 4 bit (Including LCD display RAM 32 words × 4 bit)	288 words × 4 bit (Including LCD display RAM 32 words × 4 bit)
Input/Output ports	D_0 ~ D_5	Key-on wakeup function and Pull-up function Both functions can be switched by software	No such function
		The output structure can be switched by software. Port D_5 is also used as INT pin	← The same as 455A Group
	D_6, D_7	Key-on wakeup function and Pull-up function Both functions can be switched by software	No such function
		Port D_6, D_7 are input/output ports, and are used as X_{CIN} and X_{COUT}	Port D_6, D_7 are only output ports, and are also used as X_{CIN} and X_{COUT}
	$P0_0$ ~ $P0_3$	The pull-up, key-on wakeup function, and structure can be switched by software. Port $P0_0$ ~ $P0_3$ are also used as SEG_{16} ~ SEG_{19} pins	← The same as 455A Group
		$PU0_0$, $PU0_1$ are pull-up control register of $P0_0$ ~ $P0_1$ and $P0_2$ ~ $P0_3$, respectively	$PU0_0$ ~ $PU0_3$ are pull-up control register of $P0_0$ ~ $P0_3$, respectively
	$P1_0$ ~ $P1_3$	The pull-up, key-on wakeup function, and structure can be switched by software. Port $P1_0$ ~ $P1_3$ are also used as SEG_{20} ~ SEG_{23} pins	← The same as 455A Group
		$PU0_2$, $PU0_3$ are pull-up control register of $P1_0$ ~ $P1_1$ and $P1_2$ ~ $P1_3$, respectively	$PU1_0$ ~ $PU1_3$ are pull-up control register of $P1_0$ ~ $P1_3$, respectively
	$P2_0$ ~ $P2_3$	The pull-up, key-on wakeup function, and structure can be switched by software. Port $P2_0$ ~ $P2_3$ are also used as SEG_{24} ~ SEG_{27} pins	← The same as 455A Group
		$PU1_0$ ~ $PU1_3$ are pull-up control register of $P2_0$ ~ $P2_3$, respectively	$PU2_0$ ~ $PU2_3$ are pull-up control register of $P2_0$ ~ $P2_3$, respectively
	$P3_0$ ~ $P3_3$	The pull-up, key-on wakeup function, and structure can be switched by software. Port $P3_0$ ~ $P3_3$ are also used as SEG_{28} ~ SEG_{31} pins	← The same as 455A Group
		$PU2_0$ ~ $PU2_3$ are pull-up control register of $P3_0$ ~ $P3_3$, respectively	$PU3_0$ ~ $PU3_3$ are pull-up control register of $P3_0$ ~ $P3_3$, respectively
		Key-on wakeup return only by edge	Key-on wakeup return by edge/level
	C	Port C is also used as CNTR	← The same as 455A Group
Timer	Timer 1	8-bit programmable timer with 1 reload register	← The same as 455A Group
	Timer 2	8-bit programmable timer with 2 reload registers	
	Timer 3	16-bit fixed dividing timer (for clock)	← The same as 455A Group
		4 counter sources: X_{CIN} input, ORCLK input, Low-speed/High-speed on-chip oscillator Counter source selection register: $W5_1$, $W5_0$	2 counter sources: X_{CIN} input, ORCLK input Counter source selection register: $W3_3$
		8 kinds of optional count value Count value selection register: $W3_0$ ~ $W3_2$	4 kinds of optional count value Count value selection register: $W3_0$ ~ $W3_1$
	Timer LC	4-bit timer with 1 reload register (for LCD)	← The same as 455A Group
	WDT	16-bit fixed dividing timer (for watching)	

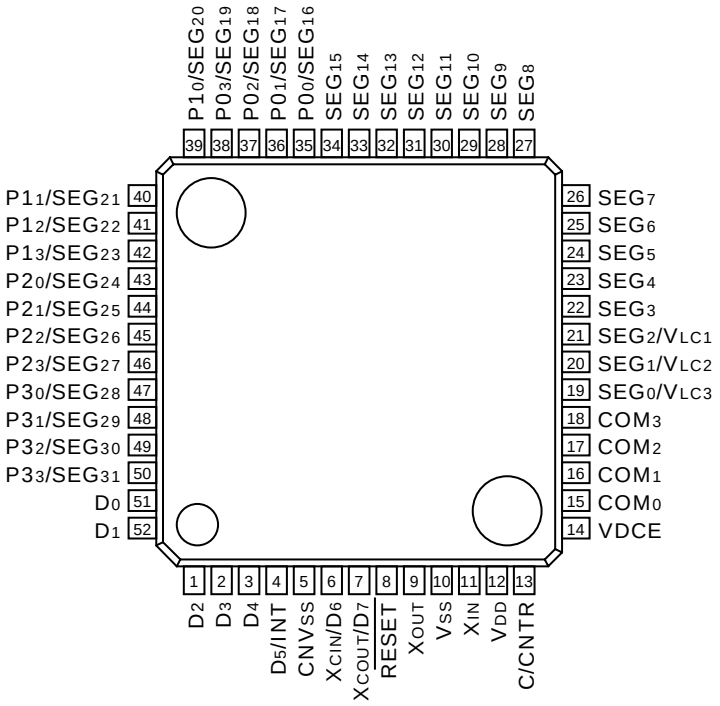
* (SBK, RBK) cannot be used in the M3455AG8.

(Continued)

LCD control circuit	Bias	1/2, 1/3	← The same as 455A Group
	Duty	1/2, 1/3, 1/4	
	Common out	4	
	Segment output	32	
	Internal resistor	2r×3, 2r×2, r×3, r×2 (r=100kΩ typical)	
On-chip oscillator	High speed	f(HSOCO): 500KHz Typ. (Ta=25℃、VDD=3V)	f(RING): 250KHz Typ. (Ta=25℃、VDD=3V)
	Low speed	f(LSOCO): 50KHz Typ. (Ta=25℃、VDD=3V)	← No such function
Interrupts	Sources	4 (one for external, three for timer)	← The same as 455A Group
	Nesting	1 level	
Sub-routing nesting		8 level	← The same as 455A Group
Clock generating circuit		Main clock (Ceramic oscillator) Sub-clock (Quartz-crystal oscillator) Internal clock (High-speed/Low-speed on chip oscillator)	Main clock (Ceramic/RC oscillation) Sub-clock (Quartz-crystal oscillator) Internal clock (on chip oscillator)

2. Pin Configuration Differences

455A Group Pin Configuration (Top View)



PLQP0052JA-A (52P6A-A)

4559 Group pin configuration is the same as 455A Group

3. Control Register Differences

Interrupt control register V1			455A Group			4559 Group
			at RESET: 0000_2	at power down: 0000_2	R/W	
$V1_3$	Timer 2 interrupt enable bit	0	Interrupt disabled (SNZT2 instruction is valid)			← (The same as 455A Group)
		1	Interrupt enabled (SNZT2 instruction is invalid)			
$V1_2$	Timer 1 interrupt enable bit	0	Interrupt disabled (SNZT1 instruction is valid)			
		1	Interrupt enabled (SNZT1 instruction is invalid)			
$V1_1$	Not used	0	The bit has no function, but Read/Write is enabled.			
		1				
$V1_0$	External 0 interrupt enable bit	0	Interrupt disabled (SNZ0 instruction is valid)			
		1	Interrupt enabled (SNZ0 instruction is invalid)			

Interrupt control register V2			455A Group			4559 Group
			at RESET: 0000_2	at power down: 0000_2	R/W	
$V2_3$	Not used	0	The bit has no function, but Read/Write is enabled.			← (The same as 455A Group)
		1				
$V2_2$	Not used	0	The bit has no function, but Read/Write is enabled.			
		1				
$V2_1$	Not used	0	The bit has no function, but Read/Write is enabled.			
		1				
$V2_0$	Timer 3 interrupt enable bit	0	Interrupt disabled (SNZT3 instruction is valid)			
		1	Interrupt enabled (SNZT3 instruction is invalid)			

Interrupt control register I1			455A Group			4559 Group
			at RESET: 0000_2	at power down: state retained	R/W	
$I1_3$	INT pin input control bit	0	INT pin input disabled			← (The same as 455A Group)
		1	INT pin input enabled			
$I1_2$	INT pin interrupt valid waveform /return level selection bit	0	Falling waveform/"L" level			
		1	Rising waveform/"H" level			
$I1_1$	INT pin edge detection circuit control bit	0	One-side edge detection			
		1	Both edges detection			
$I1_0$	INT pin timer 1 count start synchronous circuit control bit	0	Not selected			
		1	Selected			

Clock control register MR			455A Group			4559 Group
			at RESET: 1100_2	at power down: state retained	R/W	
MR_3	Operation mode selection bits	MR_3 MR_2	Operation mode			← (The same as 455A Group)
MR_2		0 0	Through mode			
		0 1	Frequency divided by 2 mode			
		1 0	Frequency divided by 4 mode			
		1 1	Frequency divided by 8 mode			
MR_1	System clock selection bits	MR_1 MR_0	System clock			
		0 0	f(HSOCO)			f(RING)
MR_0		0 1	f(X_{IN})			← (The same as 455A Group)
		1 0	f(X_{CIN})			
		1 1	f(LSOCO)			Not available

Clock control register RG			455A Group			4559 Group		
			at RESET: 1000_2	at power down: state retained	W	at RESET: 000_2	at power down: state retained	W
RG_3	Low-speed on-chip oscillator (f(LSOCO)) control bit	0	Low-speed on-chip oscillator (f(LSOCO)) oscillation available			No such bit		
		1	Low-speed on-chip oscillator (f(LSOCO)) oscillation stop					
RG_2	Sub-clock (f(X_{CIN})) control bit	0	Sub-clock (f(X_{CIN})) oscillation available, Ports D_6 and D_7 not selected			← (The same as 455A Group)		
		1	Sub-clock (f(X_{CIN})) oscillation stop, Ports D_6 and D_7 selected					
RG_1	Main-clock (f(X_{IN})) control bit	0	Main clock (f(X_{IN})) available					
		1	Main clock (f(X_{IN})) stop					
RG_0	On-chip oscillator control bit	0	High-speed on-chip oscillator (f(HSOCO)) oscillation available			On-chip oscillator (f(RING)) oscillation available		
		1	High-speed on-chip oscillator (f(HSOCO)) oscillation stop			On-chip oscillator (f(RING)) oscillation stop		

Timer control register W1			455A Group			4559 Group
			at RESET: 0000_2	at power down: state retained	R/W	
$W1_3$	Timer 1 count auto-stop circuit selection bit	0	Timer 1 count auto-stop circuit not selected			← (The same as 455A Group)
		1	Timer 1 count auto-stop circuit selected			
$W1_2$	Timer 1 control bit	0	Stop (retained)			
		1	Operating			
$W1_1$ $W1_0$	Timer 1 count source selection bit	$W1_1$ $W1_0$	Count source			
		0 0	PWM signal (PWMOUT)			
		0 1	Prescaler output (ORCLK)			
		1 0	Timer 3 underflow signal (T3UDF)			
		1 1	CNTR input			

Timer control register W2			455A Group			4559 Group
			at RESET: 0000_2	at power down: state retained	R/W	
$W2_3$	CNTR pin output control bit	0	CNTR pin output invalid			← (The same as 455A Group)
		1	CNTR pin output valid			
$W2_2$	PWM signal “H” interval expansion function control bit	0	PWM signal “H” interval expansion function invalid			
		1	PWM signal “H” interval expansion function valid			
$W2_1$	Timer 2 control bit	0	Stop (status retained)			
		1	Operating			
$W2_0$	Timer 2 count source selection bit	0	X_{IN} input			
		1	Prescaler output (ORCLK)/2			

Timer control register W3			455A Group		
			at RESET: 0000_2	at power down: state retained	R/W
$W3_3$	Timer 3 control bit	0	Stop (initial state)		
		1	Operating		
$W3_2$ $W3_1$ $W3_0$	Timer 3 count value selection bit	$W3_2$ $W3_1$ $W3_0$	Count value		
		0 0 0	Underflow every 512 count		
		0 0 1	Underflow every 1024 count		
		0 1 0	Underflow every 2048 count		
		0 1 1	Underflow every 4096 count		
		1 0 0	Underflow every 8192 count		
		1 0 1	Underflow every 16384 count		
		1 1 0	Underflow every 32768 count		
		1 1 1	Underflow every 65536 count		

Timer control register W3			4559 Group		
			at RESET: 0000_2	at power down: state retained	R/W
$W3_3$	Timer 3 count source selection bit	0	X_{CIN} input		
		1	Prescaler output (ORCLK)		
$W3_2$	Timer 3 control bit	0	Stop (initial state)		
		1	Operating		
$W3_1$	Timer 3 count value selection bit	$W3_1$ $W3_0$	Count value		
		0 0	Underflow every 8192 count		
		0 1	Underflow every 16384 count		
$W3_0$		1 0	Underflow every 32768 count		
		1 1	Underflow every 65536 count		

Timer control register W4			455A Group			4559 Group
			at RESET: 0000_2	at power down: state retained	R/W	
$W4_3$	Timer LC control bit	0	Stop (state retained)			← (The same as 455A Group)
		1	Operating			
$W4_2$	Timer LC count source selection bit	0	Bit 4 of Timer 3 ($T3_4$)			
		1	System clock (STCK)			
$W4_1$	CNTR pin output auto-control circuit selection bit	0	CNTR output auto-control circuit not selected			
		1	CNTR output auto-control circuit selected			
$W4_0$	CNTR pin input count edge selection bit	0	Falling edge			
		1	Rising edge			

Timer control register W5			455A Group			4559 Group
			at RESET: 0000_2	at power down: state retained	R/W	
$W5_3$	Not used	0	The bit has no function, but Read/Write is enable.			No such register
		1	The bit has no function, but Read/Write is enable.			
$W5_2$	Not used	0	The bit has no function, but Read/Write is enable.			
		1	The bit has no function, but Read/Write is enable.			
$W5_1$	Timer 3 count source selection bit	$W5_1$ $W5_0$	Count source			
		0 0	X_{CIN} input			
		0 1	ORCLK input			
$W5_0$		1 0	Low-speed on chip oscillator			
		1 1	High-speed on chip oscillator			

LCD control register L1			455A Group			4559 Group
			at RESET: 0000_2	at power down: state retained	R/W	
$L1_3$	Internal dividing resistor for LCD power supply selection bit	0	2r×3, 2r×2			← (The same as 455A Group)
		1	r×3, r×2			
$L1_2$	LCD control bit	0	Stop			
		1	Operating			
$L1_1$	LCD duty and bias selection bit	$L1_1$ $L1_0$	Duty	Bias		
		0 0	Not available	Not available		
		0 1	1/2	1/2		
$L1_0$		1 0	1/3	1/3		
		1 1	1/4	1/3		

Timer control register PA			455A Group			4559 Group
			at RESET: 0_2	at power down: 0_2	W	
PA_0	Prescaler control bit	0	Stop (state retained)			← (The same as 455A Group)
		1	Operating			

LCD control register L2			455A Group			4559 Group
			at RESET: 0000_2	at power down: state retained	W	
$L2_3$	SEG_0/V_{LC3} pin function switch bit	0	SEG_0			← (The same as 455A Group)
		1	V_{LC3}			
$L2_2$	SEG_1/V_{LC2} pin function switch bit	0	SEG_1			
		1	V_{LC2}			
$L2_1$	SEG_2/V_{LC1} pin function switch bit	0	SEG_2			
		1	V_{LC1}			
$L2_0$	Internal dividing resistor for LCD power supply control bit	0	Internal dividing resistor valid			
		1	Internal dividing resistor invalid			

LCD control register L3			455A Group			4559 Group
			at RESET: 1111_2	at power down: state retained	W	
$L3_3$	$P2_3/SEG_{27}$ pin function switch bit	0	SEG_{27}			← (The same as 455A Group)
		1	$P2_3$			
$L3_2$	$P2_2/SEG_{26}$ pin function switch bit	0	SEG_{26}			
		1	$P2_2$			
$L3_1$	$P2_1/SEG_{25}$ pin function switch bit	0	SEG_{25}			
		1	$P2_1$			
$L3_0$	$P2_0/SEG_{24}$ pin function switch bit	0	SEG_{24}			
		1	$P2_0$			

LCD control register C1			455A Group			4559 Group
			at RESET: 1111_2	at power down: state retained	W	
$C1_3$	$P0_3/SEG_{19}$ pin function switch bit	0	SEG_{19}			← (The same as 455A Group)
		1	$P0_3$			
$C1_2$	$P0_2/SEG_{18}$ pin function switch bit	0	SEG_{18}			
		1	$P0_2$			
$C1_1$	$P0_1/SEG_{17}$ pin function switch bit	0	SEG_{17}			
		1	$P0_1$			
$C1_0$	$P0_0/SEG_{16}$ pin function switch bit	0	SEG_{16}			
		1	$P0_0$			

LCD control register C2			455A Group			4559 Group
			at RESET: 1111_2	at power down: state retained	W	
$C2_3$	$P1_3/SEG_{23}$ pin function switch bit	0	SEG_{23}			← (The same as 455A Group)
		1	$P1_3$			
$C2_2$	$P1_2/SEG_{22}$ pin function switch bit	0	SEG_{22}			
		1	$P1_2$			
$C2_1$	$P1_1/SEG_{21}$ pin function switch bit	0	SEG_{21}			
		1	$P1_1$			
$C2_0$	$P1_0/SEG_{20}$ pin function switch bit	0	SEG_{20}			
		1	$P1_0$			

LCD control register C3			455A Group			4559 Group
			at RESET: 1111_2	at power down: state retained	W	
$C3_3$	$P3_3/SEG_{31}$ pin function switch bit	0	SEG_{31}			← (The same as 455A Group)
		1	$P3_3$			
$C3_2$	$P3_2/SEG_{30}$ pin function switch bit	0	SEG_{30}			
		1	$P3_2$			
$C3_1$	$P3_1/SEG_{29}$ pin function switch bit	0	SEG_{29}			
		1	$P3_1$			
$C3_0$	$P3_0/SEG_{28}$ pin function switch bit	0	SEG_{28}			
		1	$P3_0$			

Pull-up control register PU0			455A Group			4559 Group
			at RESET: 0000_2	at power down: state retained	R/W	← (The same as 455A Group)
$PU0_3$	Pull-up transistor control bit	0	$P1_2$, $P1_3$ pull-up transistor OFF			$P0_3$ pull-up transistor OFF
		1	$P1_2$, $P1_3$ pull-up transistor ON			$P0_3$ pull-up transistor ON
$PU0_2$	Pull-up transistor control bit	0	$P1_0$, $P1_1$ pull-up transistor OFF			$P0_2$ pull-up transistor OFF
		1	$P1_0$, $P1_1$ pull-up transistor ON			$P0_2$ pull-up transistor ON
$PU0_1$	Pull-up transistor control bit	0	$P0_2$, $P0_3$ pull-up transistor OFF			$P0_1$ pull-up transistor OFF
		1	$P0_2$, $P0_3$ pull-up transistor ON			$P0_1$ pull-up transistor ON
$PU0_0$	Pull-up transistor control bit	0	$P0_0$, $P0_1$ pull-up transistor OFF			$P0_0$ pull-up transistor OFF
		1	$P0_0$, $P0_1$ pull-up transistor ON			$P0_0$ pull-up transistor ON

Pull-up control register PU1			455A Group			4559 Group
			at RESET: 0000_2	at power down: state retained	R/W	← (The same as 455A Group)
$PU1_3$	Pull-up transistor control bit	0	$P2_3$ pull-up transistor OFF			$P1_3$ pull-up transistor OFF
		1	$P2_3$ pull-up transistor ON			$P1_3$ pull-up transistor ON
$PU1_2$	Pull-up transistor control bit	0	$P2_2$ pull-up transistor OFF			$P1_2$ pull-up transistor OFF
		1	$P2_2$ pull-up transistor ON			$P1_2$ pull-up transistor ON
$PU1_1$	Pull-up transistor control bit	0	$P2_1$ pull-up transistor OFF			$P1_1$ pull-up transistor OFF
		1	$P2_1$ pull-up transistor ON			$P1_1$ pull-up transistor ON
$PU1_0$	Pull-up transistor control bit	0	$P2_0$ pull-up transistor OFF			$P1_0$ pull-up transistor OFF
		1	$P2_0$ pull-up transistor ON			$P1_0$ pull-up transistor ON

Pull-up control register PU2			455A Group			4559 Group
			at RESET: 0000_2	at power down: state retained	R/W	← (The same as 455A Group)
$PU2_3$	Pull-up transistor control bit	0	$P3_3$ pull-up transistor OFF			$P2_3$ pull-up transistor OFF
		1	$P3_3$ pull-up transistor ON			$P2_3$ pull-up transistor ON
$PU2_2$	Pull-up transistor control bit	0	$P3_2$ pull-up transistor OFF			$P2_2$ pull-up transistor OFF
		1	$P3_2$ pull-up transistor ON			$P2_2$ pull-up transistor ON
$PU2_1$	Pull-up transistor control bit	0	$P3_1$ pull-up transistor OFF			$P2_1$ pull-up transistor OFF
		1	$P3_1$ pull-up transistor ON			$P2_1$ pull-up transistor ON
$PU2_0$	Pull-up transistor control bit	0	$P3_0$ pull-up transistor OFF			$P2_0$ pull-up transistor OFF
		1	$P3_0$ pull-up transistor ON			$P2_0$ pull-up transistor ON

Pull-up control register PU3			455A Group			4559 Group
			at RESET: 0000_2	at power down: state retained	R/W	← (The same as 455A Group)
$PU3_3$	Pull-up transistor control bit	0	D_6, D_7 pull-up transistor OFF			$P3_3$ pull-up transistor OFF
		1	D_6, D_7 pull-up transistor ON			$P3_3$ pull-up transistor ON
$PU3_2$	Pull-up transistor control bit	0	D_4, D_5 pull-up transistor OFF			$P3_2$ pull-up transistor OFF
		1	D_4, D_5 pull-up transistor ON			$P3_2$ pull-up transistor ON
$PU3_1$	Pull-up transistor control bit	0	D_2, D_3 pull-up transistor OFF			$P3_1$ pull-up transistor OFF
		1	D_2, D_3 pull-up transistor ON			$P3_1$ pull-up transistor ON
$PU3_0$	Pull-up transistor control bit	0	D_0, D_1 pull-up transistor OFF			$P3_0$ pull-up transistor OFF
		1	D_0, D_1 pull-up transistor ON			$P3_0$ pull-up transistor ON

Output structure control register FR0			455A Group			4559 Group
			at RESET: 0000_2	at power down: state retained	W	
$FR0_3$	Ports $P1_2$ and $P1_3$ output structure selection bit	0	N-channel open-drain output			← (The same as 455A Group)
		1	CMOS output			
$FR0_2$	Ports $P1_0$ and $P1_1$ output structure selection bit	0	N-channel open-drain output			
		1	CMOS output			
$FR0_1$	Ports $P0_2$ and $P0_3$ output structure selection bit	0	N-channel open-drain output			
		1	CMOS output			
$FR0_0$	Ports $P0_0$ and $P0_1$ output structure selection bit	0	N-channel open-drain output			
		1	CMOS output			

Output structure control register FR1			455A Group			4559 Group
			at RESET: 0000_2	at power down: state retained	W	
$FR1_3$	Ports D_3 output structure selection bit	0	N-channel open-drain output			← (The same as 455A Group)
		1	CMOS output			
$FR1_2$	Ports D_2 output structure selection bit	0	N-channel open-drain output			
		1	CMOS output			
$FR1_1$	Ports D_1 output structure selection bit	0	N-channel open-drain output			
		1	CMOS output			
$FR1_0$	Ports D_0 output structure selection bit	0	N-channel open-drain output			
		1	CMOS output			

Output structure control register FR2			455A Group			4559 Group
			at RESET: 0000_2	at power down: state retained	W	
$FR2_3$	Ports $P3_2$, $P3_3$ output structure selection bit	0	N-channel open-drain output			← (The same as 455A Group)
		1	CMOS output			
$FR2_2$	Ports $P3_0$, $P3_1$ output structure selection bit	0	N-channel open-drain output			
		1	$P3_0$, $P3_1$ CMOS output			
$FR2_1$	Ports D_5 output structure selection bit	0	N-channel open-drain output			
		1	CMOS output			
$FR2_0$	Ports D_4 output structure selection bit	0	N-channel open-drain output			
		1	CMOS output			

Output structure control register FR3			455A Group			4559 Group
			at RESET: 0000_2	at power down: state retained	W	
$FR3_3$	Ports $P2_3$ output structure selection bit	0	N-channel open-drain output			← (The same as 455A Group)
		1	CMOS output			
$FR3_2$	Ports $P2_2$ output structure selection bit	0	N-channel open-drain output			
		1	CMOS output			
$FR3_1$	Ports $P2_1$ output structure selection bit	0	N-channel open-drain output			
		1	CMOS output			
$FR3_0$	Ports $P2_0$ output structure selection bit	0	N-channel open-drain output			
		1	CMOS output			

Key-on wakeup control register K0			455A Group			4559 Group
			at RESET: 0000_2	at power down: state retained	R/W	
$K0_3$	Ports $P1_2$, $P1_3$ key-on wakeup control bit	0	Key-on wakeup invalid			← (The same as 455A Group)
		1	Key-on wakeup valid			
$K0_2$	Ports $P1_0$, $P1_1$ key-on wakeup control bit	0	Key-on wakeup invalid			
		1	Key-on wakeup valid			
$K0_1$	Ports $P0_2$, $P0_3$ key-on wakeup control bit	0	Key-on wakeup invalid			
		1	Key-on wakeup valid			
$K0_0$	Ports $P0_0$, $P0_1$ key-on wakeup control bit	0	Key-on wakeup invalid			
		1	Key-on wakeup valid			

Key-on wakeup control register K1			455A Group			4559 Group
			at RESET: 0000_2	at power down: state retained	R/W	
$K1_3$	Ports $P2_3$ key-on wakeup control bit	0	Key-on wakeup invalid			← (The same as 455A Group)
		1	Key-on wakeup valid			
$K1_2$	Ports $P2_2$ key-on wakeup control bit	0	Key-on wakeup invalid			
		1	Key-on wakeup valid			
$K1_1$	Ports $P2_1$ key-on wakeup control bit	0	Key-on wakeup invalid			
		1	Key-on wakeup valid			
$K1_0$	Ports $P2_0$ key-on wakeup control bit	0	Key-on wakeup invalid			
		1	Key-on wakeup valid			

Key-on wakeup control register K2			455A Group			4559 Group
			at RESET: 0000_2	at power down: state retained	R/W	
$K2_3$	Ports $P3_2$, $P3_3$ Key-on wakeup control bit	0	Key-on wakeup not used			← (The same as 455A Group)
		1	Key-on wakeup used			
$K2_2$	Ports $P3_0$, $P3_1$ Key-on wakeup control bit	0	Key-on wakeup not used			
		1	Key-on wakeup used			
$K2_1$	INT pin return condition selection bit	0	Returned by level			
		1	Returned by edge			
$K2_0$	INT pin key-on condition selection bit	0	Key-on wakeup invalid			
		1	Key-on wakeup valid			

Key-on wakeup control register K3			455A Group		
			at RESET: 0000_2	at power down: state retained	R/W
$K3_3$	Ports D_6 and D_7 Key-on wakeup control bit	0	Key-on wakeup not used		
		1	Key-on wakeup used		
$K3_2$	Ports D_4 and D_5 Key-on wakeup control bit	0	Key-on wakeup not used		
		1	Key-on wakeup used		
$K3_1$	Ports D_2 and D_3 Key-on wakeup control bit	0	Key-on wakeup not used		
		1	Key-on wakeup used		
$K3_0$	Ports D_0 and D_1 Key-on wakeup control bit	0	Key-on wakeup not used		
		1	Key-on wakeup used		

Key-on wakeup control register K3			4559 Group		
			at RESET: 0000_2	at power down: state retained	R/W
$K3_3$	Ports $P3_2$, $P3_3$ return condition selection bit	0	Return by level		
		1	Return by edge		
$K3_2$	Ports $P3_2$, $P3_3$ valid waveform/level selection bit	0	Falling waveform/“L” level		
		1	Rising waveform/“H” level		
$K3_1$	Ports $P3_0$, $P3_1$ return condition selection bit	0	Return by level		
		1	Return by edge		
$K3_0$	Ports $P3_0$, $P3_1$ valid waveform/level selection bit	0	Falling waveform/“L” level		
		1	Rising waveform/“H” level		

4. RAM Map Differences

455A Group RAM Map

512 words × 4 bit (2048 bits)

Register Y	Register Z	0									1								
	Register X	0	1	2	3	…	12	13	14	15	0	1	2	3	…	12	13	14	15
0																			
1																			
2																			
3																			
4																			
5																			
6																			
7																			
8																0	8	16	24
9																1	9	17	25
10																2	10	18	26
11																3	11	19	27
12																4	12	20	28
13																5	13	21	29
14																6	14	22	30
15																7	15	23	31

Note: The numbers in the shaded area indicate the corresponding segment output pin numbers.

4559 Group RAM Map

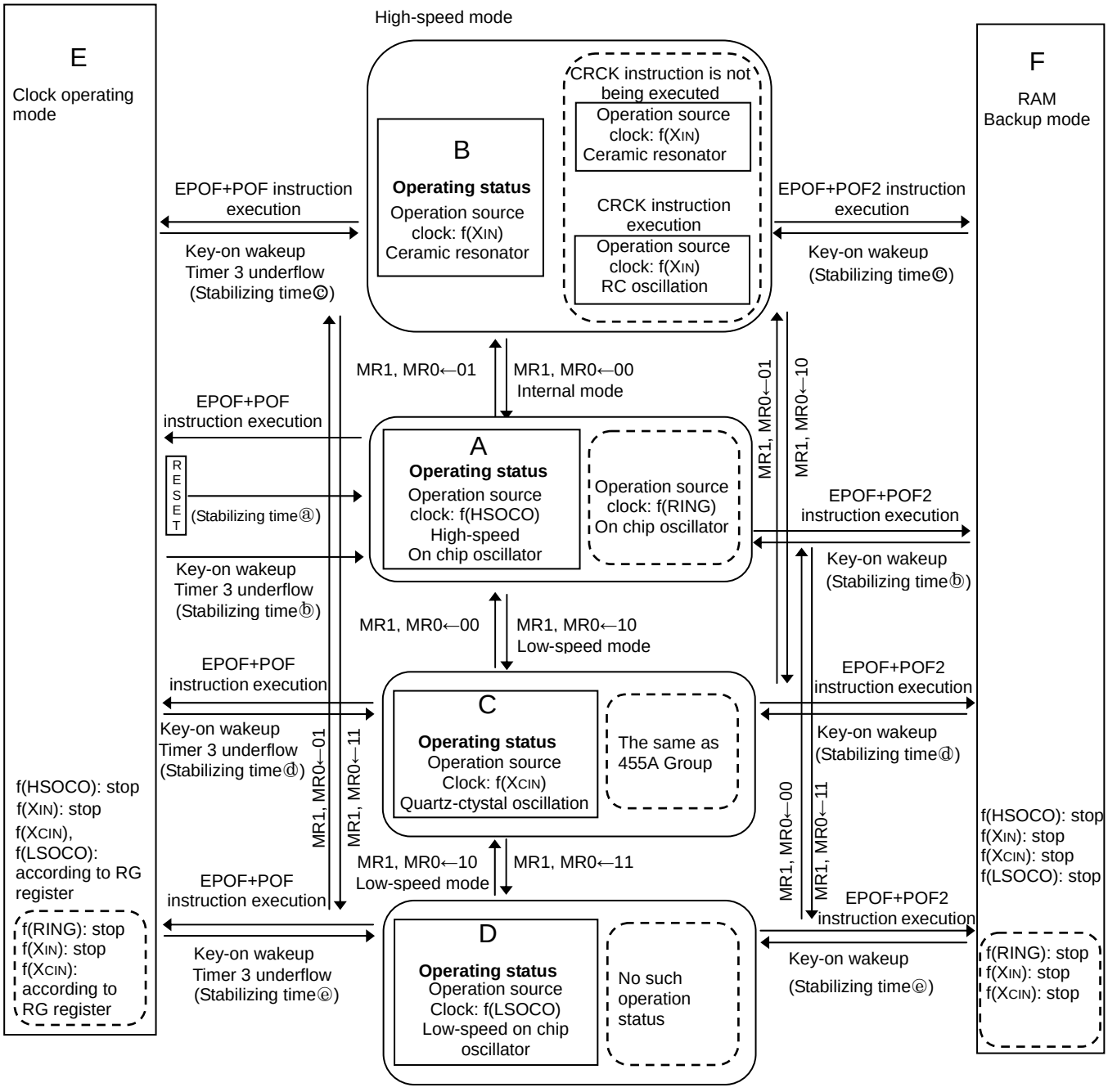
288 words × 4 bit (1152 bits)

Register Y	Register Z	0									1			
	Register X	0	1	2	3	…	12	13	14	15	0	1	2	3
0														
1														
2														
3														
4														
5														
6														
7														
8											0	8	16	24
9											1	9	17	25
10											2	10	18	26
11											3	11	19	27
12											4	12	20	28
13											5	13	21	29
14											6	14	22	30
15											7	15	23	31

Note: The numbers in the shaded area indicate the corresponding segment output pin numbers.

5. State Transition Graph of M3455AG8FP/ M3455AGCFP and M34559G6FP

Inside is the state of M34559G6FP



Stabilizing time:

ⓐ:Microcomputer starts its operation after counting the f(HSOCO)/ f(RING) to 1376 times.

ⓑ:Microcomputer starts its operation after counting the f(HSOCO) to (system clock division ratio × 15) times.
Microcomputer starts its operation after counting the f(RING) to (system clock division ratio × 171) times.

ⓒ:Microcomputer starts its operation after counting the f(XIN) to (system clock division ratio × 171) times. The same as 455A Group

ⓓ:Microcomputer starts its operation after counting the f(XCIN) to (system clock division ratio × 171) times. The same as 455A Group

ⓔ:Microcomputer starts its operation after counting the f(LSOCO) to (system clock division ratio × 15) times.

6. The Added and Deleted Instructions of 455A Group

Mnemonic	Added /Deleted	Instruction Code(HEX)	Function	Detailed Description
TW5A	added	2 1 2	(W5) ← (A)	Transfers the contents of register A to timer control register W5.
TAW5	added	2 4 F	(A) ← (W5)	Transfers the contents of timer control register W5 to register A.
RBK	added	0 4 0	TABP p instruction execution: p6←0	Sets referring data area to pages 0 to 63 when the TABP p instruction is executed. This instruction is valid only for the TABP p instruction.
SBK	added	0 4 1	TABP p instruction execution: p6←1	Sets referring data area to pages 64 to 127 when the TABP p instruction is executed. This instruction is valid only for the TABP p instruction.
CRCK	deleted	2 9 B	RC oscillation circuit selected	Selects the RC oscillation circuit for main clock f(X_{IN}).

7. Reference Document

Datasheet
455A Group Datasheet
4559 Group Datasheet
(Use the most recent version of the document on the Renesas Technology Website.)

Technical News/Technical Update
(Use the most recent version of the document on the Renesas Technology Website.)

Website and Support

Renesas Technology Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
csc@renesas.com

REVISION HISTORY	455A Group, 4559 Group Differences between 455A Group and 4559 Group

Rev.	Date	Description	
		Page	Summary
1.00	Mar 07, 2008	—	First edition issued
2.00	Aug 27, 2008	1	The content of “The Performance Overview Differences” revised
		2	The content of “Pin Configuration Differences” revised
		12	The content of “State Transition Graph” revised

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