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Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

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Renesas Electronics Corporation

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4553 Group, 4559 Group

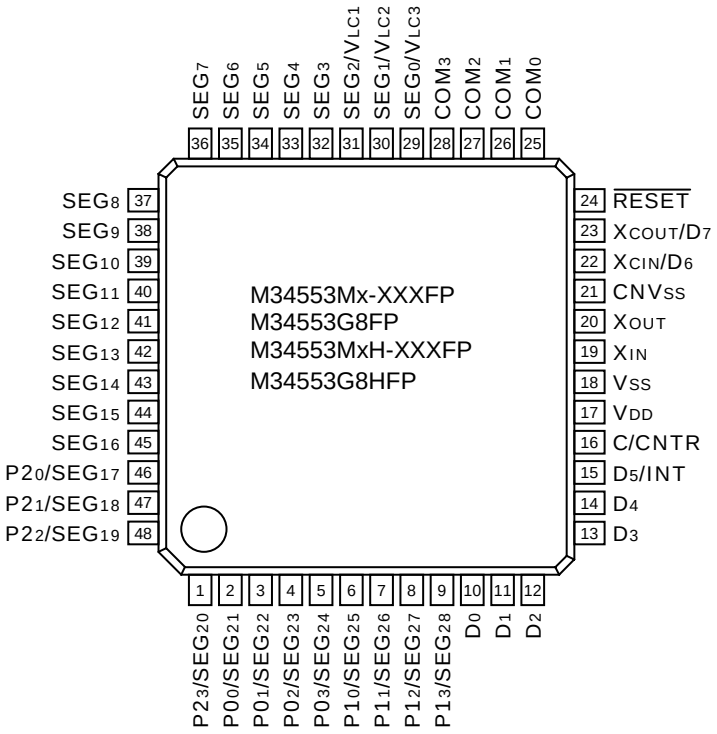
Differences between 4553 Group and 4559 Group

1. The Performance Overview Differences

Parameter		Function	
		4553group	4559 group
Number of basic instructions		123(4553 Group) 124(4553H Group)	135
ROM type		Mask ROM/One Time PROM	QzROM
ROM size		4096/8912 words × 10 bit	6144 words × 10 bit
RAM size		288 words × 4 bit (Including LCD display RAM 29 words × 4bit)	288 words × 4 bit (Including LCD display RAM 32 words × 4bit)
Input/output ports	D_0 ~ D_5	The output structure can be switched through software. Port D_5 is also used as INT pin	← The same as 4553 group
	D_6, D_7	Port D_6, D_7 are also used as X_{CIN} and X_{COUT}	← The same as 4553 group
	$P0_0$ ~ $P0_3$	The pull-up, key-on wakeup function, and structure can be switched through software.	← The same as 4553 group
		Port $P0_0$ ~ $P0_3$ are also used as SEG_{21} ~ SEG_{24} pins	Port $P0_0$ ~ $P0_3$ are also used as SEG_{16} ~ SEG_{19} pins
	$P1_0$ ~ $P1_3$	The pull-up, key-on wakeup function, and structure can be switched through software.	← The same as 4553 group
		Port $P1_0$ ~ $P1_3$ are also used as SEG_{25} ~ SEG_{28} pins	Port $P1_0$ ~ $P1_3$ are also used as SEG_{20} ~ SEG_{23} pins
	$P2_0$ ~ $P2_3$	The output structure can be switched through software.	The pull-up,key-on wakeup function,and structure can be switched through software.
		Port $P2_0$ ~ $P2_3$ are also used as SEG_{17} ~ SEG_{20} pins	Port $P2_0$ ~ $P2_3$ are also used as SEG_{24} ~ SEG_{27} pins
	$P3_0$ ~ $P3_3$	No such pins	The pull-up, key-on wakeup function, and structure can be switched through software. Port $P3_0$ ~ $P3_3$ are also used as SEG_{28} ~ SEG_{31} pins
	C	Port C is also used as CNTR	← The same as 4553 group
Timer	Timer 1	8-bit programmable timer with 1 reload register	← The same as 4553 group
	Timer 2	8-bit programmable timer with 2 reload registers	
	Timer 3	16-bit fixed dividing timer(for clock)	
	Timer LC	4-bit timer with one reload register(for LCD)	
	WDT	16-bit fixed dividing timer(for watching)	
LCD control circuit	Bias	1/2, 1/3	← The same as 4553 group
	Duty	1/2, 1/3, 1/4	
	Common out	4	
	Segment output	29	32
	Internal resistor	2r × 3, 2r × 2, r × 3, r × 2 (r=80kΩ typical)	2r × 3, 2r × 2, r × 3, r × 2 (r=100kΩ typical)
Interrupts	Sources	4(one for external, three for timer)	← The same as 4553 group
	Nesting	1 level	
Sub-routing nesting		8 level	← The same as 4553 group

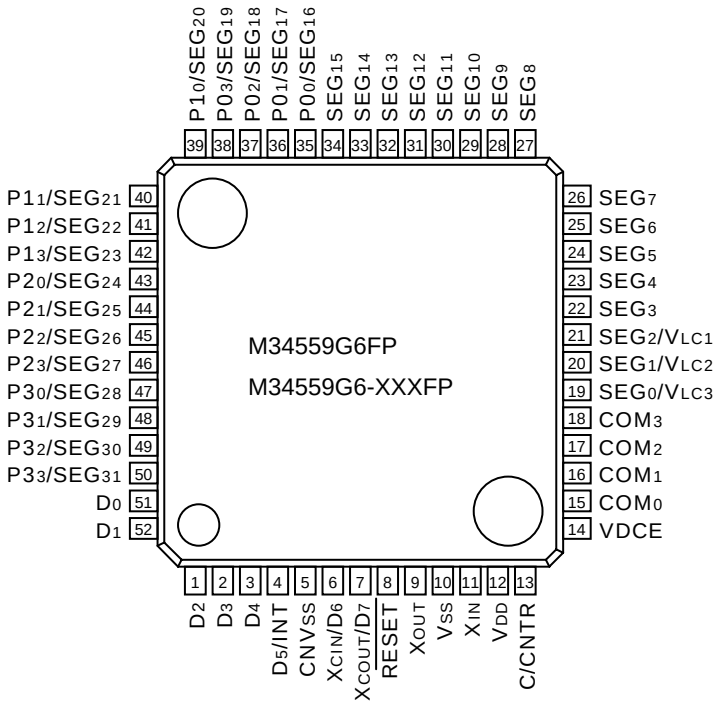
2. Pin Configuration Differences

4553 group pin configuration(top view)



PLQP0048KB-A(48P6Q-A)

4559 group pin configuration(top view)



PLQP0052JA-A (52P6A-A)

3. Control Register Differences

Interrupt control register V1			4553 group			4559 group
			At RESET : 0000_2	At POF : 0000_2	R/W	
$V1_3$	Timer 2 interrupt enable bit	0	Interrupt disabled (SNZT2 instruction is valid)			← (The same as 4553 group)
		1	Interrupt enabled (SNZT2 instruction is invalid)			
$V1_2$	Timer 1 interrupt enable bit	0	Interrupt disabled (SNZT1 instruction is valid)			
		1	Interrupt enabled (SNZT1 instruction is invalid)			
$V1_1$	Not used	0	The bit has no function,			
		1	Read/Write is enabled.			
$V1_0$	External 0 interrupt enable bit	0	Interrupt disabled (SNZ0 instruction is valid)			
		1	Interrupt enabled (SNZ0 instruction is invalid)			

Interrupt control register V2			4553 group			4559 group
			At RESET : 0000_2	At POF : 0000_2	R/W	
$V2_3$	Not used	0	The bit has no function,			← (The same as 4553 group)
		1	Read/Write is enabled.			
$V2_2$	Not used	0	The bit has no function,			
		1	Read/Write is enabled.			
$V2_1$	Not used	0	The bit has no function,			
		1	Read/Write is enabled.			
$V2_0$	Timer 3 interrupt enable bit	0	Interrupt disabled (SNZT3 instruction is valid)			
		1	Interrupt enabled (SNZT3 instruction is invalid)			

Interrupt control register I1			4553 group			4559 group
			At RESET : 0000_2	At POF : retained	R/W	
$I1_3$	INT pin input control bit	0	INT pin input disabled			← (The same as 4553 group)
		1	INT pin input enabled			
$I1_2$	INT pin interrupt valid waveform /return level selection bit	0	Falling waveform/"L" level			
		1	Rising waveform/"H" level			
$I1_1$	INT pin Edge detection circuit control bit	0	One-side edge detection			
		1	Both edges detection			
$I1_0$	INT pin timer 1 count start synchronous circuit control bit	0	Not selected			
		1	Selected			

Clock control register MR			4553 group			4559 group
			At RESET : 1100_2	At POF : retained	R/W	
MR_3	Operation mode Selection bits	MR_3 MR_2	Operation mode			← (The same as 4553 group)
MR_2		0 0	Through mode (no dividing)			
		0 1	Frequency divided by 2 mode			
		1 0	Frequency divided by 4 mode			
		1 1	Frequency divided by 8 mode			
MR_1	System clock Selection bits	MR_1 MR_0	System clock			
MR_0		0 0	f (RING)			
		0 1	f (X_{IN})			
		1 0	f (X_{CIN})			
		1 1	Not used			

Clock control register RG			4553 group			4559 group
			At RESET : 000_2	At POF : retained	W	
RG_2	f(X_{CIN}) control bit	0	f(X_{CIN}) available, Port D6,D7 not selected			← (The same as 4553 group)
		1	f(X_{CIN}) stop, Port D6,D7 selected			
RG_1	f(X_{IN}) control bit	0	f(X_{IN}) available			
		1	f(X_{IN}) stop			
RG_0	f(RING) control bit	0	f(RING) available			
		1	f(RING) stop			

Timer control register PA			4553 group			4559 group
			At RESET : 0_2	At POF : 0_2	W	
PA0	Prescaler control bit	0	Stop(status retained)			← (The same as 4553 group)
		1	Operating			

Timer control register W1				4553 group			4559 group
				At RESET : 0000_2	At POF : retained	R/W	
$W1_3$	Timer 1 count auto-stop circuit selection bit	0		Not selected			← (The same as 4553 group)
		1		selected			
$W1_2$	Timer 1 control bit	0		Stop(retained)			
		1		Operating			
$W1_1$	Timer 1 Count source selection	$W1_1$	$W1_0$	Timer 1 count source selection			
		0	0	PWM signal(PWMOUT)			
		0	1	Prescaler output (ORCLK)			
$W1_0$		1	0	Timer 3 underflow signal (T3UDF)			
		1	1	CNTR input			

Timer control register W2			4553 group			4559 group
			At RESET : 0000_2	At POF : 0000_2	R/W	
$W2_3$	CNTR pin output control bit	0	CNTR pin output invalid			← (The same as 4553 group)
		1	CNTR pin output valid			
$W2_2$	PWM signal "H" interval Expansion function control bit	0	"H" interval expansion function invalid			
		1	"H" interval expansion function valid			
$W2_1$	Timer 2 control bit	0	Stop(status retained)			
		1	Operating			
$W2_0$	Timer 2 count source selection bit	0	X_{IN} input			
		1	Prescaler output divided by 2(ORCLK)			

Timer control register W3				4553 group			4559 group
				At RESET : 00002	At POF : retained	R/W	
$W3_3$	Timer 3 Count source selection bit	0		X_{CIN} input			← (The same as 4553 group)
		1		Prescaler output (ORCLK)			
$W3_2$	Timer 3 control bit	0		Stop(status retained)			
		1		Operating			
$W3_1$	Timer 3 Count value selection bit	$W3_1$	$W3_0$	Timer 3 count value			
		0	0	Underflow every 8192 count			
		0	1	Underflow every 16384 count			
$W3_0$		1	0	Underflow every 32768 count			
		1	1	Underflow every 65536 count			

Timer control register W4			4553 group			4559 group
			At RESET : 0000_2	At POF : retained	R/W	
$W4_3$	Timer LC control bit	0	Stop(status retained)			← (The same as 4553 group)
		1	operating			
$W4_2$	Timer LC Count source selection bit	0	Bit 4 of Timer 3($T3_4$)			
		1	System clock(STCK)			
$W4_1$	CNTR pin output auto-control circuit selection bit	0	Not selected			
		1	Selected			
$W4_0$	CNTR pin input count edge selection bit	0	Falling edge			
		1	Rising edge			

LCD control register L1			4553 group			4559 group
			At RESET : 0000_2	At POF : retained	R/W	
$L1_3$	LCD internal dividing resistor selection bit	0	$2r \times 3$, $2r \times 2$			← (The same as 4553 group)
		1	$r \times 3$, $r \times 2$			
$L1_2$	LCD control bit	0	Stop			
		1	Operating			
$L1_1$	LCD duty and bias selection bit	$L1_1$ $L1_0$	Duty	Bias		
$L1_0$		0 0	Not available	Not available		
		0 1	1/2	1/2		
		1 0	1/3	1/3		
		1 1	1/4	1/3		

LCD control register L2			4553 group			4559 group
			At RESET : 0000_2	At POF : retained	W	
$L2_3$	SEG_0/V_{LC3} pin function switch bit	0	SEG_0			← (The same as 4553 group)
		1	V_{LC3}			
$L2_2$	SEG_1/V_{LC2} pin function switch bit	0	SEG_1			
		1	V_{LC2}			
$L2_1$	SEG_2/V_{LC1} pin function switch bit	0	SEG_2			
		1	V_{LC1}			
$L2_0$	LCD internal dividing resistor control bit	0	Valid			
		1	Invalid			

LCD control register L3			4553 group			4559 group
			At RESET : 1111_2	At POF : retained	W	←
$L3_3$	Port $P2_3$ function switch bit	0	SEG_{20}			SEG_{27}
		1	$P2_3$			←
$L3_2$	Port $P2_2$ function switch bit	0	SEG_{19}			SEG_{26}
		1	$P2_2$			←
$L3_1$	Port $P2_1$ function switch bit	0	SEG_{18}			SEG_{25}
		1	$P2_1$			←
$L3_0$	Port $P2_0$ function switch bit	0	SEG_{17}			SEG_{24}
		1	$P2_0$			←

LCD control register C1			4553 group			4559 group
			At RESET : 1111_2	At POF : retained	W	←
$C1_3$	Port $P0_3$ function switch bit	0	SEG_{24}			SEG_{19}
		1	$P0_3$			←
$C1_2$	Port $P0_2$ function switch bit	0	SEG_{23}			SEG_{18}
		1	$P0_2$			←
$C1_1$	Port $P0_1$ function switch bit	0	SEG_{22}			SEG_{17}
		1	$P0_1$			←
$C1_0$	Port $P0_0$ function switch bit	0	SEG_{21}			SEG_{16}
		1	$P0_0$			←

LCD control register C2			4553 group			4559 group
			At RESET : 1111_2	At POF : retained	W	
$C2_3$	Port $P1_3$ function switch bit	0	SEG_{28}			SEG_{23}
		1	$P1_3$			←
$C2_2$	Port $P1_2$ function switch bit	0	SEG_{27}			SEG_{22}
		1	$P1_2$			←
$C2_1$	Port $P1_1$ function switch bit	0	SEG_{26}			SEG_{21}
		1	$P1_1$			←
$C2_0$	Port $P1_0$ function switch bit	0	SEG_{25}			SEG_{20}
		1	$P1_0$			←

LCD control register C3			4553 group	4559 group		
				At RESET : 1111_2	At POF : retained	W
$C3_3$	Port $P3_3$ function switch bit	0	No such register	SEG_{31}		
		1		$P3_3$		
$C3_2$	Port $P3_2$ function switch bit	0		SEG_{30}		
		1		$P3_2$		
$C3_1$	Port $P3_1$ function switch bit	0		SEG_{29}		
		1		$P3_1$		
$C3_0$	Port $P3_0$ function switch bit	0		SEG_{28}		
		1		$P3_0$		

Pull-up control register PU0			4553 group			4559 group
			At RESET : 0000_2	At POF : retained	R/W	
$PU0_3$	Pull-up transistor control bit	0	$P0_3$ pull-up transistor OFF			← (The same as 4553 group)
		1	$P0_3$ pull-up transistor ON			
$PU0_2$	Pull-up transistor control bit	0	$P0_2$ pull-up transistor OFF			
		1	$P0_2$ pull-up transistor ON			
$PU0_1$	Pull-up transistor control bit	0	$P0_1$ pull-up transistor OFF			
		1	$P0_1$ pull-up transistor ON			
$PU0_0$	Pull-up transistor control bit	0	$P0_0$ pull-up transistor OFF			
		1	$P0_0$ pull-up transistor ON			

Pull-up control register PU1			4553 group			4559 group
			At RESET : 0000_2	At POF : retained	R/W	
$PU1_3$	Pull-up transistor control bit	0	$P1_3$ pull-up transistor OFF			← (The same as 4553 group)
		1	$P1_3$ pull-up transistor ON			
$PU1_2$	Pull-up transistor control bit	0	$P1_2$ pull-up transistor OFF			
		1	$P1_2$ pull-up transistor ON			
$PU1_1$	Pull-up transistor control bit	0	$P1_1$ pull-up transistor OFF			
		1	$P1_1$ pull-up transistor ON			
$PU1_0$	Pull-up transistor control bit	0	$P1_0$ pull-up transistor OFF			
		1	$P1_0$ pull-up transistor ON			

LCD control register PU2			4553 group	4559 group		
				At RESET : 0000_2	At POF : retained	R/W
$PU2_3$	Port $P2_3$ function switch bit	0	No such register	$P2_3$ pull-up transistor OFF		
		1		$P2_3$ pull-up transistor ON		
$PU2_2$	Port $P2_2$ function switch bit	0		$P2_2$ pull-up transistor OFF		
		1		$P2_2$ pull-up transistor ON		
$PU2_1$	Port $P2_1$ function switch bit	0		$P2_1$ pull-up transistor OFF		
		1		$P2_1$ pull-up transistor ON		
$PU2_0$	Port $P2_0$ function switch bit	0		$P2_0$ pull-up transistor OFF		
		1		$P2_0$ pull-up transistor ON		

LCD control register PU3			4553 group	4559 group		
				At RESET : 0000_2	At POF : retained	R/W
$PU3_3$	Port $P3_3$ function switch bit	0	No such register	$P3_3$ pull-up transistor OFF		
		1		$P3_3$ pull-up transistor ON		
$PU3_2$	Port $P3_2$ function switch bit	0		$P3_2$ pull-up transistor OFF		
		1		$P3_2$ pull-up transistor ON		
$PU3_1$	Port $P3_1$ function switch bit	0		$P3_1$ pull-up transistor OFF		
		1		$P3_1$ pull-up transistor ON		
$PU3_0$	Port $P3_0$ function switch bit	0		$P3_0$ pull-up transistor OFF		
		1		$P3_0$ pull-up transistor ON		

Output structure control register FR0			4553 group			4559 group
			At RESET : 0000_2	At POF : retained	W	
$FR0_3$	Output structure selection bit	0	$P1_2$, $P1_3$ N-channel open-drain output			← (The same as 4553 group)
		1	$P1_2$, $P1_3$ CMOS output			
$FR0_2$	Output structure selection bit	0	$P1_0$, $P1_1$ N-channel open-drain output			
		1	$P1_0$, $P1_1$ CMOS output			
$FR0_1$	Output structure selection bit	0	$P0_2$, $P0_3$ N-channel open-drain output			
		1	$P0_2$, $P0_3$ CMOS output			
$FR0_0$	Output structure selection bit	0	$P0_0$, $P0_1$ N-channel open-drain output			
		1	$P0_0$, $P0_1$ CMOS output			

Output structure control register FR1			4553 group			4559 group
			At RESET : 0000_2	At POF : retained	W	
$FR1_3$	Output structure selection bit	0	D3 N-channel open-drain output			← (The same as 4553 group)
		1	D3 CMOS output			
$FR1_2$	Output structure selection bit	0	D2 N-channel open-drain output			
		1	D2 CMOS output			
$FR1_1$	Output structure selection bit	0	D1 N-channel open-drain output			
		1	D1 CMOS output			
$FR1_0$	Output structure selection bit	0	D0 N-channel open-drain output			
		1	D0 CMOS output			

Output structure control register FR2			4553 group			4559 group
			At RESET : 0000_2	At POF : retained	W	←
$FR2_3$	Output structure selection bit	0	$P2_2$, $P2_3$ N-channel open-drain output			$P3_2$, $P3_3$ N-channel open-drain output
		1	$P2_2$, $P2_3$ CMOS output			$P3_2$, $P3_3$ CMOS output
$FR2_2$	Output structure selection bit	0	$P2_0$, $P2_1$ N-channel open-drain output			$P3_0$, $P3_1$ N-channel open-drain output
		1	$P2_0$, $P2_1$ CMOS output			$P3_0$, $P3_1$ CMOS output
$FR2_1$	Output structure selection bit	0	D5 N-channel open-drain output			←
		1	D5 CMOS output			←
$FR2_0$	Output structure selection bit	0	D4 N-channel open-drain output			←
		1	D4 CMOS output			←

Output structure control register FR3			4553 group			4559 group		
			At RESET : 0000_2	At POF : retained	W	At RESET : 0000_2	At POF : retained	W
$FR3_3$	Output structure selection bit	0	No such register			$P2_3$ N-channel open-drain output		
		1				$P2_3$ CMOS output		
$FR3_2$	Output structure selection bit	0				$P2_2$ N-channel open-drain output		
		1				$P2_2$ CMOS output		
$FR3_1$	Output structure selection bit	0				$P2_1$ N-channel open-drain output		
		1				$P2_1$ CMOS output		
$FR3_0$	Output structure selection bit	0				$P2_0$ N-channel open-drain output		
		1				$P2_0$ CMOS output		

Key-on wakeup control register K0			4553 group			4559 group
			At RESET : 0000_2	At POF : retained	R/W	
$K0_3$	Key-on wakeup control bit	0	$P1_2$, $P1_3$ key-on wakeup invalid			← (The same as 455A group)
		1	$P1_2$, $P1_3$ key-on wakeup valid			
$K0_2$	Key-on wakeup control bit	0	$P1_0$, $P1_1$ key-on wakeup invalid			
		1	$P1_0$, $P1_1$ key-on wakeup valid			
$K0_1$	Key-on wakeup control bit	0	$P0_2$, $P0_3$ key-on wakeup invalid			
		1	$P0_2$, $P0_3$ key-on wakeup valid			
$K0_0$	Key-on wakeup control bit	0	$P0_0$, $P0_1$ key-on wakeup invalid			
		1	$P0_0$, $P0_1$ key-on wakeup valid			

Key-on wakeup control register K1			4553 group			4559 group
			At RESET : 0000_2	At POF : retained	R/W	←
$K1_3$	Key-on wakeup control bit	0	$P1_2$, $P1_3$ returned by edge			$P2_3$ key-on wakeup invalid
		1	$P1_2$, $P1_3$ returned by level			$P2_3$ key-on wakeup valid
$K1_2$	Key-on wakeup control bit	0	$P1_2$, $P1_3$ falling waveform/returned by “L” level			$P2_2$ key-on wakeup invalid
		1	$P1_2$, $P1_3$ rising waveform/returned by “H” level			$P2_2$ key-on wakeup valid
$K1_1$	Key-on wakeup control bit	0	$P1_0$, $P1_1$ returned by edge			$P2_1$ key-on wakeup invalid
		1	$P1_0$, $P1_1$ returned by level			$P2_1$ key-on wakeup valid
$K1_0$	Key-on wakeup control bit	0	$P1_0$, $P1_1$ falling waveform/returned by “L” level			$P2_0$ key-on wakeup invalid
		1	$P1_0$, $P1_1$ rising waveform/returned by “H” level			$P2_0$ key-on wakeup valid

Key-on wakeup control register K2			4553 group			4559 group
			At RESET : 0000_2	At POF : retained	R/W	←
$K2_3$	Key-on wakeup control bit	0	Not used			$P3_2$, $P3_3$ key-on wakeup invalid
		1	Read/Write enable			$P3_2$, $P3_3$ key-on wakeup valid
$K2_2$	Key-on wakeup control bit	0	Not used			$P3_0$, $P3_1$ key-on wakeup invalid
		1	Read/Write enable			$P3_0$, $P3_1$ key-on wakeup valid
$K2_1$	Return condition selection bit	0	INT returned by level			←
		1	INT returned by edge			←
$K2_0$	Key-on wakeup control bit	0	INT key-on wakeup invalid			←
		1	INT key-on wakeup valid			←

Output structure control register K3			4553 group			4559 group		
			At RESET : 0000_2	At POF : retained	R/W	At RESET : 0000_2	At POF : retained	W
$K3_3$	Return condition selection bit	0	No such register			$P3_2$, $P3_3$ returned by level		
		1				$P3_2$, $P3_3$ returned by edge		
$K3_2$	Valid waveform/level selection bit	0				$P3_2$, $P3_3$ falling waveform/returned by “L” level		
		1				$P3_2$, $P3_3$ rising waveform/returned by “H” level		
$K3_1$	Return condition selection bit	0				$P3_0$, $P3_1$ returned by level		
		1				$P3_0$, $P3_1$ returned by edge		
$K3_0$	Valid waveform/level selection bit	0				$P3_0$, $P3_1$ falling waveform/returned by “L” level		
		1				$P3_0$, $P3_1$ rising waveform/returned by “H” level		

4. The Added Instructions of 4559 Group

Mnemonic	Instruction Code HEX	Function	Detailed description
IAP3	2 6 3	(A) ← (P3)	Transfers the input of port P3 to the register A.
OP3A	2 2 3	(P3) ← (A)	Outputs the contents of the register A to port P3.
TAK3	2 5 B	(A) ← (K3)	Transfers the contents of key-on wakeup control register K3 to register A.
TK3A	2 2 C	(K3) ← (A)	Transfers the contents of register A to key-on wakeup control register K3.
TAPU2	2 5 F	(A) ← (PU2)	Transfers the contents of pull-up control register PU2 to register A.
TPU2A	2 2 F	(PU2) ← (A)	Transfers the contents of register A to pull-up control register PU2.
TAPU3	2 5 D	(A) ← (PU3)	Transfers the contents of pull-up control register PU3 to register A.
TPU3A	2 0 8	(PU3) ← (A)	Transfers the contents of register A to pull-up control register PU3.
TFR3A	2 2 B	(FR3) ← (A)	Transfers the contents of register A to port output structure control register FR3.
TC3A	2 2 6	(C3) ← (A)	Transfers the contents of register A to the LCD control register C3.
SNZVD	2 8 A	(VDF) = 1?	Skips the next instruction when voltage drop detection circuit flag VDF is “1”. Execute instruction when VDF is “0”.After skipping, the contents of VDF remains unchanged.

5. The Added/Changed Functions of 4559 Group

5.1 Ports

- Added Port P3 (added the pull-up, key-on wakeup function, and structure can be switched through software).
- Added segment output Ports SEG_{29} ~ SEG_{31} (LCD display RAM map as shown in the following table).

	Z	1			
	X	0	1	2	3
Y	8	SEG_0	SEG_8	SEG_{16}	SEG_{24}
	9	SEG_1	SEG_9	SEG_{17}	SEG_{25}
	10	SEG_2	SEG_{10}	SEG_{18}	SEG_{26}
	11	SEG_3	SEG_{11}	SEG_{19}	SEG_{27}
	12	SEG_4	SEG_{12}	SEG_{20}	SEG_{28}
	13	SEG_5	SEG_{13}	SEG_{21}	SEG_{29}
	14	SEG_6	SEG_{14}	SEG_{22}	SEG_{30}
	15	SEG_7	SEG_{15}	SEG_{23}	SEG_{31}

Added SEG_{29} ~ SEG_{31}

- Changed Port/Segment pins definition (as shown in the following table).

4553Group	4559Group	4553Group	4559Group	4553Group	4559Group	4553Group	4559Group
$P0_0/SEG_{21}$	$P0_0/SEG_{16}$	$P1_0/SEG_{25}$	$P1_0/SEG_{20}$	$P2_0/SEG_{17}$	$P2_0/SEG_{24}$	—	$P3_0/SEG_{28}$
$P0_1/SEG_{22}$	$P0_1/SEG_{17}$	$P1_1/SEG_{26}$	$P1_1/SEG_{21}$	$P2_1/SEG_{18}$	$P2_1/SEG_{25}$	—	$P3_1/SEG_{29}$
$P0_2/SEG_{23}$	$P0_2/SEG_{18}$	$P1_2/SEG_{27}$	$P1_2/SEG_{22}$	$P2_2/SEG_{19}$	$P2_2/SEG_{26}$	—	$P3_2/SEG_{30}$
$P0_3/SEG_{24}$	$P0_3/SEG_{19}$	$P1_3/SEG_{28}$	$P1_3/SEG_{23}$	$P2_3/SEG_{20}$	$P2_3/SEG_{27}$	—	$P3_3/SEG_{31}$

- Deleted Ports P1 key-on wakeup return condition selection and valid waveform selection functions, added the functions to Ports P3.
- Added Ports P2 Pull-up transistor control and key-on wakeup selection functions.
- Changed Ports P2 output structure selection bits from 2 bits to 1 bit.

5.2 Voltage Drop Detection Circuit

- Added skip judgment function by the SNZVD instruction (Typ. 2.0V(Ta=25℃)).
- Changed reset occurrence/release voltage.

	4553 Group	4559 Group	Condition
Reset occurrence	Typ. 1.8V	Typ. 1.7V	Ta = 25 ℃
Reset release	Typ. 1.9V	Typ. 1.8V	Ta = 25 ℃

6. Reference Document

Datasheet
4553 Group Datasheet
4559 Group Datasheet
(Use the most recent version of the document on the Renesas Technology Web site.)

Technical News/Technical Update
(Use the most recent version of the document on the Renesas Technology Web site.)

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