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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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3803 Group, 3802 Group

Differences between 3803 Group and 3802 Group

1. Differences between 3803 Group and 3802 Group

		3802 Group	3803 Group	Additional Register in 3803 Group
Minimum Instruction Execution Time		0.5 μs (at max. 8 MHz oscillation frequency)	0.24 μs (at max. 16.8 MHz oscillation frequency)	—
Sub-clock Oscillating Circuit		—	Composed of P40/XCOUT and P41/XCIN	CPU mode register (bits 4, 6, 7 at address 003B16)
Internal System Clock ϕ		f(XIN) / 2, only	f(XIN) / 2 in high-speed mode, f(XIN) / 8 in middle-speed mode, f(XCIN) / 2 in low-speed mode	CPU mode register (bits 4 to 7 at address 003B16); ***MCU starts in middle-speed mode after releasing Reset.**
Interrupt		16 sources, 16 vectors (external 7, internal 8, software 1)	21 sources, 16 vectors (external 8, internal 12, software 1)	Interrupt source selection register (address 003916)
Watchdog Timer		—	16-bit × 1	Watchdog timer control register (address 001E16)
LED Direct Drive Port		—	8 pins, P20 to P27; IOL(peak) = 20 mA, ΣIOL(peak) = 80 mA, IOL(avg) = 15 mA, ΣIOL(avg) = 40 mA	—
Software Pull-up Resistors		—	Included in all ports P0 to P6, Programmable for each bit	Port pull-up control registers (addresses 0FF016 to 0FF616)
A-D Converter	Resolution	8-bit	10-bit	A-D conversion register 2 (address 003816); ***10-bit A-D mode after releasing Reset.**
	Channel	8 channels, P60 to P67	16 channels; P60 to P67, P00 to P07	AD/DA control register (bits 0 to 2, 4 at address 003416)
Timer	Structure	Prescaler 12 (8-bit) →Timer 1 (8-bit) →Timer 2 (8-bit) Prescaler X (8-bit) →Timer X (8-bit) Prescaler Y (8-bit) →Timer Y (8-bit)	Prescaler 12 (8-bit) →Timer 1 (8-bit) →Timer 2 (8-bit) Prescaler X (8-bit) →Timer X (8-bit) Prescaler Y (8-bit) →Timer Y (8-bit) Timer Z (16-bit)	Timer Z low-order (address 002816) Timer Z high-order (address 002916) Timer Z mode register (address 002A16)
	Count source	f(XIN) / 16, only	Built-in count source divider, Selectable for each Timer; f(XIN) or f(XCIN) divided by 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024; f(XCIN) (not divided)	Timer 12, X count source selection register (address 000E16) Timer Y, Z count source selection register (address 000F16)
Serial I/O1 (UART/Clock synchronous)		8-bit × 1 channel, P44 to P47 used	8-bit × 1 channel, P44 to P47 used	—
Serial I/O2 (Clock synchronous)		8-bit × 1 channel, P50 to P53 used	8-bit × 1 channel, P50 to P53 used	—
Serial I/O3 (UART/Clock synchronous)		—	8-bit × 1 channel, P34 to P37 used	Baud rate generator 3 (address 002F16) Transmit/Receive buffer register 3 (address 003016) Serial I/O3 status register (address 003116) Serial I/O3 control register (address 003216) UART3 control register (address 003316)
PWM		8-bit × 1 channel, with 8-bit Prescaler	8-bit × 1 channel, with 8-bit Prescaler	—
D-A Converter		8-bit × 2 channels	8-bit × 2 channels	

- Every additional register of 3803 Group has the same state after releasing Reset as that of 3802 Group. However, the above mentioned (*) shows that it differs from 3802 Group.
- The following 3803 group's registers have additional functions from 3802 Group: AD/DA control register (bit 4 at address 003416), Interrupt edge selection register (bit 6 at address 003A16), CPU mode register (address 003B16).
  Note when programming to bits which have not been used in 3802 Group.

	3802 Group	3803 Group	Additional Register in 3803 Group
N-channel Open-drain Pin	—	$P3_2$, $P3_3$	—
INT_0, INT_4 Interrupt Switch	Not switched	INT_{00}, INT_{40} or INT_{01}, INT_{41}	Interrupt edge selection register (bit 6 at address $003A_{16}$)
Processor mode	Single-chip, Memory expansion, or Microprocessor mode	Single-chip mode	CPU mode register (bits 0, 1 at address $003B_{16}$)

- Every additional register of 3803 Group has the same state after releasing Reset as that of 3802 Group.
- The following 3803 group's registers have additional functions from 3802 Group: AD/DA control register (bit 4 at address 0034_{16}), Interrupt edge selection register (bit 6 at address $003A_{16}$), CPU mode register (address $003B_{16}$).
  Note when programming to bits which have not been used in 3802 Group.

2. Reference

Data Sheet

3803 Group (Spec. H) Datasheet

3802 Group Datasheet

User's Manual

3803 Group (Spec. H) USER'S MANUAL

3802 Group USER'S MANUAL

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Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Nov.10.00	—	Issue as reference selection.
1.01	Mar.18.05	—	Change to application note format and issue

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