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Old Company Name in Catalogs and Other Documents

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Renesas Electronics Corporation

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38C5 Group, 38D5 Group

Difference between 38C5 Group and 38D5 Group

1. Difference between 38C5 Group and 38D5 Group

Table 1. Difference between 38C5 Group and 38D5 Group

	38C5 Group		38D5 Group
	Mask ROM	One Time PROM	QzROM
Related Products	M38C58M8-XXXFP/HP M38C59MC-XXXFP/HP M38C59MF-XXXFP/HP	M38C59GFFP/HP	M38D58G8FP/HP M38D58G8-XXXFP/HP M38D59GCFP/HP M38D59GC-XXXFP/HP M38D59GFFP/HP M38D59GF-XXXFP/HP
Package	PLQP0080KB-A(Previous Code 80P6Q-A) : 80-pin LQFP(0.5mm pin-pitch) PLQP0080GA-A(Previous Code 80P6U-A) : 80-pin LQFP(0.8mm pin-pitch)		PLQP0080KB-A(Previous Code 80P6Q-A) : 80-pin LQFP(0.5mm pin-pitch) PRQP0080GB-A(Previous Code 80P6N-A) : 80-pin QFP(0.8mm pin-pitch)
ROM Type : ROM/RAM Size	MASK:32K/1536,48K/2048,60K/2048	60K/2048	QzROM:32K/1536, 48K/2048, 60K/2048
ROM Correction Function	N/A		Included (Refer to 38D5 Group datasheet)
Watchdog Timer	Included (8 Bits x 1)		Included (8 Bits x 1) (On-Chip Oscillator selectable)
CPU Mode Register	On-chip oscillator mode		OSCSEL(*1) = H: f(XIN)/8 mode OSCSEL= L: On-Chip Oscillator mode

	38C5 Group		38D5 Group
	Mask ROM	One Time PROM	QzROM
Operating mode at reset, or when the stop mode returns	Refer to P5 for details		
Maximum oscillation frequency	12.5MHz	6MHz	16.0MHz(*2)
Supply Voltage	1.8～5.5 V	1.8～3.6 V	1.8～5.5 V
ID-code area	–	$FFD4_{16}$～$FFDA_{16}$	–
Reserved ROM area	–	–	$FFD0_{16}$～$FFDB_{16}$

*1 In the 38D5 group, Pin name of the 9th pin has been altered to OSCSEL from CNV_{SS}.

*2 In the 38D5 group, f(XIN)/2 cannot be used at 12.5MHz< f(XIN)≤16MHz.

2. SFR Comparison between 38C5 Group and 38D5 Group

	38C5 Group	38D5 Group
000016	Port P0(P0)	Port P0(P0)
000116	Port P0 direction register (P0D)	Port P0 direction register (P0D)
000216	Port P1(P1)	Port P1(P1)
000316	Port P1 direction register (P1D)	Port P1 direction register (P1D)
000416	Port P2(P2)	Port P2(P2)
000516	Port P2 direction register (P2D)	Port P2 direction register (P2D)
000616	Port P3(P3)	Port P3(P3)
000716	Port P3 direction register (P3D)	Port P3 direction register (P3D)
000816	Port P4(P4)	Port P4(P4)
000916	Port P4 direction register (P4D)	Port P4 direction register (P4D)
000A16	Port P5(P5)	Port P5(P5)
000B16	Port P5 direction register (P5D)	Port P5 direction register (P5D)
000C16	Port P6(P6)	Port P6(P6)
000D16	Port P6 direction register (P6D)	Port P6 direction register (P6D)
000E16	Port P7(P7)	Port P7(P7)
000F16	Port P7 direction register (P7D)	Port P7 direction register (P7D)
001016		
001116		CPU mode register2 (CPUM2)
001216	RRF register (RRFR)	RRF register (RRFR)
001316	LCD mode register 1 (LM1)	LCD mode register 1 (LM1)
001416	LCD mode register 2 (LM2)	LCD mode register 2 (LM2)
001516	A/D control register (ADCON)	A/D control register (ADCON)
001616	A/D conversion register (low-order) (ADL)	A/D conversion register (low-order) (ADL)
001716	A/D conversion register (high-order) (ADH)	A/D conversion register (high-order) (ADH)
001816	Transmit/receive buffer register1(TB1RB1)	Transmit/receive buffer register1(TB1RB1)
001916	Serial I/O1status register (SIO1STS)	Serial I/O1status register (SIO1STS)
001A16	Serial I/O1 control register (SIO1CON)	Serial I/O1 control register (SIO1CON)
001B16	UART control register (UARTCON)	UART control register (UARTCON)
001C16	Baudrate generator (BRG)	Baudrate generator (BRG)
001D16	Serial I/O2 control register (SIO2CON)	Serial I/O2 control register (SIO2CON)
001E16	Reserved area (access disabled)	Reserved area (access disabled)
001F16	Serial I/O2 register (SIO2)	Serial I/O2 register (SIO2)

NOTES:
Do not access memory in free space of SFR.

: Additional function register

	38C5 Group	38D5 Group
0020₁₆	Timer 1 (T1)	Timer 1 (T1)
0021₁₆	Timer 2 (T2)	Timer 2 (T2)
0022₁₆	Timer 3 (T3)	Timer 3 (T3)
0023₁₆	Timer 4 (T4)	Timer 4 (T4)
0024₁₆	PWM01register (PWM01)	PWM01register (PWM01)
0025₁₆	Timer 12 mode register (T12M)	Timer 12 mode register (T12M)
0026₁₆	Timer 34 mode register (T34M)	Timer 34 mode register (T34M)
0027₁₆	Timer 1234 mode register (T1234M)	Timer 1234 mode register (T1234M)
0028₁₆	Timer 1234 frequency division selection register (PRE1234)	Timer 1234 frequency division selection register (PRE1234)
0029₁₆	Watchdog timer control register (WDTCON)	Watchdog timer control register (WDTCON)
002A₁₆	Timer X (low-order) (TXL)	Timer X (low-order) (TXL)
002B₁₆	Timer X (high-order) (TXH)	Timer X (high-order) (TXH)
002C₁₆	Timer X (extension) (TXEX)	Timer X (extension) (TXEX)
002D₁₆	Timer X mode register (TXM)	Timer X mode register (TXM)
002E₁₆	Timer X control register1 (TXCON1)	Timer X control register1 (TXCON1)
002F₁₆	Timer X control register2 (TXCON2)	Timer X control register2 (TXCON2)

0030₁₆	Compare register 1 (low-order) (COMP1L)	Compare register 1 (low-order) (COMP1L)
0031₁₆	Compare register 1 (high-order)(COMP1H)	Compare register 1 (high-order)(COMP1H)
0032₁₆	Compare register 2 (low-order) (COMP2L)	Compare register 2 (low-order) (COMP2L)
0033₁₆	Compare register 2 (high-order)(COMP2H)	Compare register 2 (high-order)(COMP2H)
0034₁₆	Compare register 3 (low-order) (COMP3L)	Compare register 3 (low-order) (COMP3L)
0035₁₆	Compare register 3 (high-order)(COMP3H)	Compare register 3 (high-order)(COMP3H)
0036₁₆	Timer Y (low-order) (TYL)	Timer Y (low-order) (TYL)
0037₁₆	Timer Y (high-order) (TYH)	Timer Y (high-order) (TYH)
0038₁₆	Timer Y mode register (TYM)	Timer Y mode register (TYM)
0039₁₆	Timer Y control register (TYCON)	Timer Y control register (TYCON)
003A₁₆	Interrupt edge selection register (INTEDGE)	Interrupt edge selection register (INTEDGE)
003B₁₆	CPU mode register (CPUM)	CPU mode register (CPUM)
003C₁₆	Interrupt request register1 (IREQ1)	Interrupt request register1 (IREQ1)
003D₁₆	Interrupt request register2 (IREQ2)	Interrupt request register2 (IREQ2)
003E₁₆	Interrupt control register1 (ICON1)	Interrupt control register1 (ICON1)
003F₁₆	Interrupt control register2 (ICON2)	Interrupt control register2 (ICON2)

NOTES:
Do not access memory in free space of SFR.

: Additional function register

	38C5 Group	38D5 Group
0FF0₁₆	PULL register1 (PULL1)	PULL register1 (PULL1)
0FF1₁₆	PULL register2 (PULL2)	PULL register2 (PULL2)
0FF2₁₆	PULL register3 (PULL3)	PULL register3 (PULL3)
0FF3₁₆	Clock output control register (CKOUT)	Clock output control register (CKOUT)
0FF4₁₆	Segment output disable 0 (SEG0)	Segment output disable 0 (SEG0)
0FF5₁₆	Segment output disable 1 (SEG1)	Segment output disable 1 (SEG1)
0FF6₁₆	Segment output disable 2(SEG2)	Segment output disable 2(SEG2)
0FF7₁₆	Key input control register (KIC)	Key input control register (KIC)
0FF8₁₆		ROM correction address 1 (high-order)
0FF9₁₆		ROM correction address 1 (low-order)
0FFA₁₆		ROM correction address 2 (high-order)
0FFB₁₆		ROM correction address 2 (low-order)
0FFC₁₆		ROM correction enable register
0FFD₁₆		Reserved area (access disabled)
0FFE₁₆		
0FFF₁₆		

NOTES:
Do not access memory in free space of SFR.

: Additional function register

3. CPUM Mode Register

In the 38D5 Group, f(XIN)/4 (frequency/4 mode) has been added. In addition the on-chip oscillator can be selected not used / used by setting the ROSC stop bit in the CPU mode register 2.

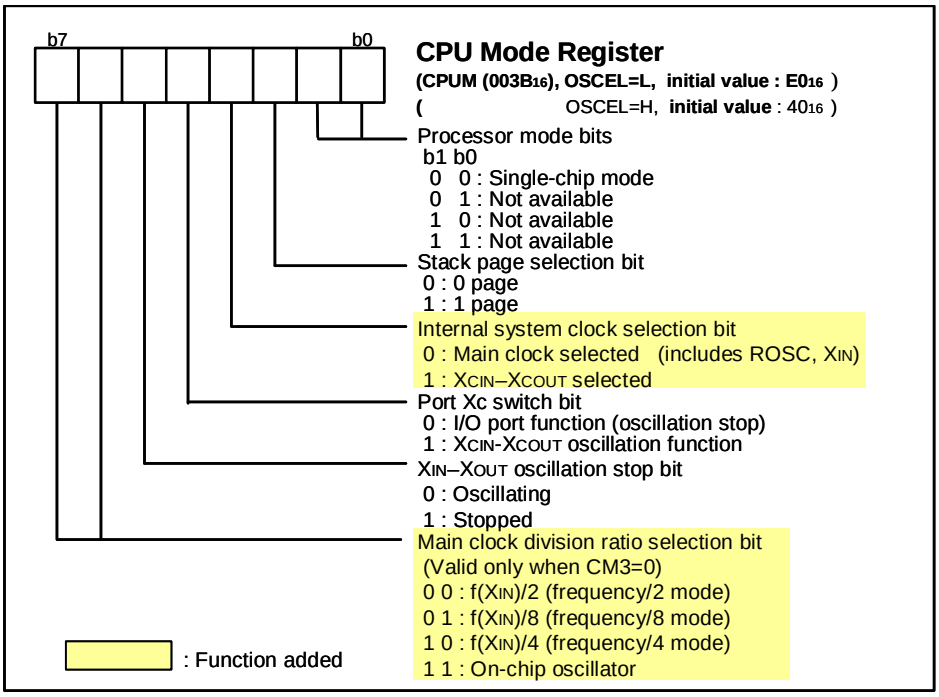

Figure 1. Structure of CPU Mode Register

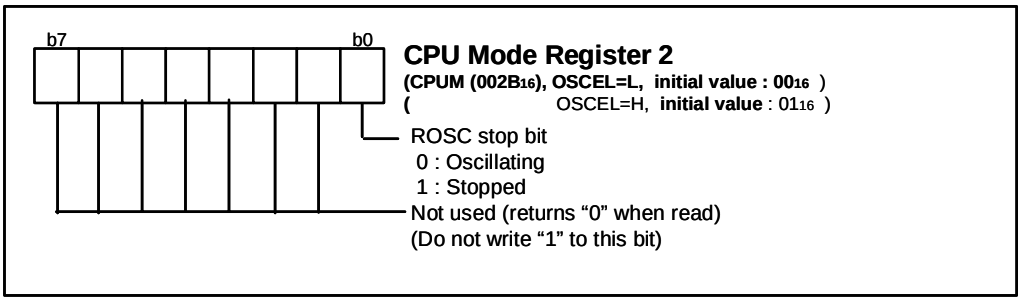

Figure 2. Structure of CPU Mode Extension Register

In the 38D5 group, the operating mode can be selected by setting the OSCSEL pin at reset, or when the stop mode returns.

OSCSEL= H, frequency / 8 mode
OSCSEL= L, On-chip oscillator mode

4. Watchdog timer function

In the 38D5 Group, the on-chip oscillator can be selected by setting the Watchdog timer count source selection bit 2.

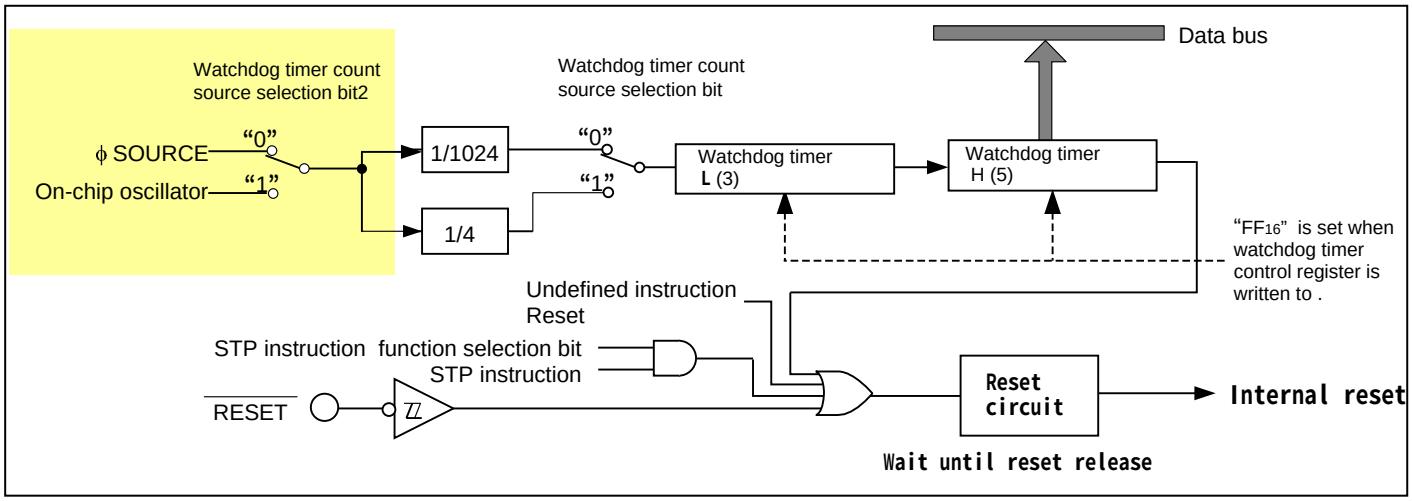

Figure 3. Block diagram of Watchdog timer

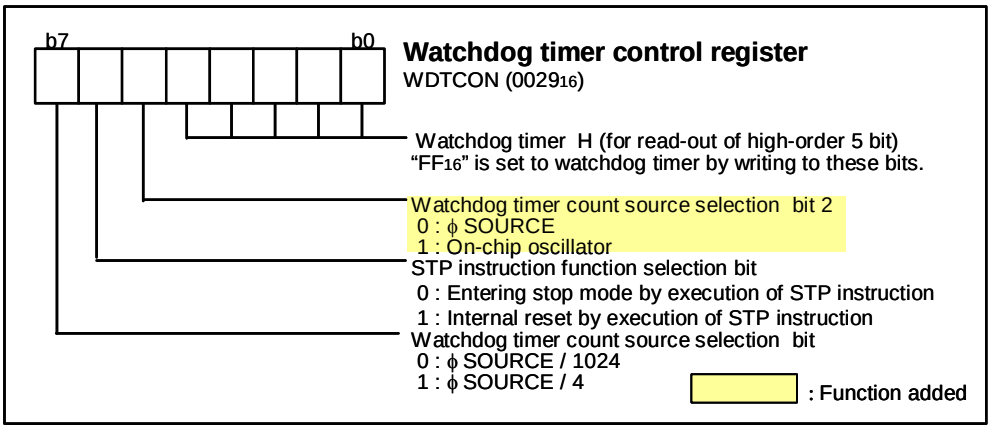

Figure 4. Structure of Watchdog timer control register

1: ϕSOURCE represents the supply source of internal clock ϕ.
XIN input: in the middle- or high-speed mode.
Internal on-chip oscillator divided by 4 in the on-chip oscillator mode, and Sub clock in the low-speed mode.
2: When the on-chip oscillator is selected by the watchdog timer count source selection bit 2 , set the STP instruction function selection bit to "1".
3: Bits 7 to 5 can be rewritten only once after releasing reset.
After rewriting it is disable to write any data to this bit.

5. Writing for the OSCSEL pin

The OSCSEL pin is the power source input pin for the built-in QzROM.
When programming in the QzROM, the impedance of the OSCSEL pin is low to allow the electric current for writing to flow into the built-in QzROM. Because of this, noise can enter easily. If noise enters the OSCSEL pin, abnormal instruction codes or data are read from the QzROM, which may cause a program runaway.

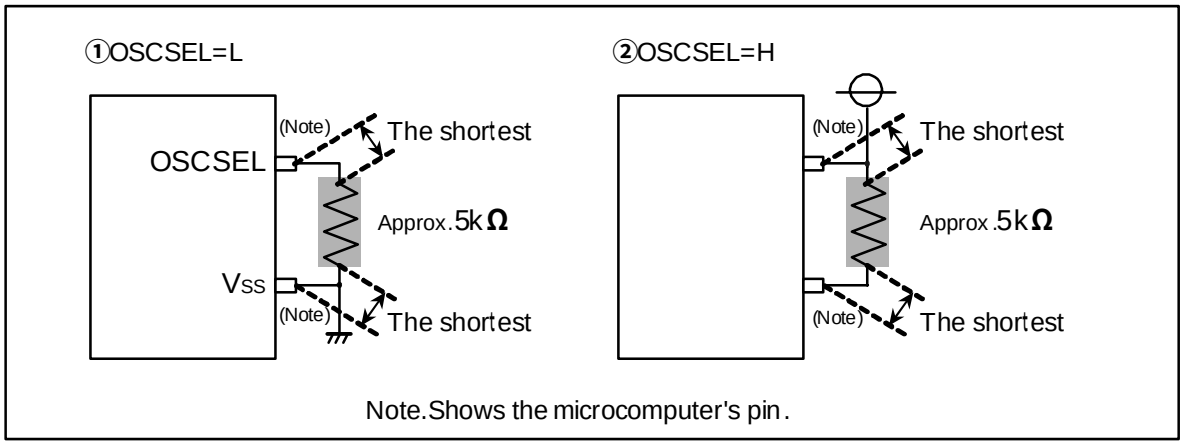

Figure 5. Wiring for the OSCSEL pin

(1) OSCSEL=L
Connect the OSCSEL pin the shortest possible to the GND pattern which is supplied to the VSS pin of the microcomputer.
In addition connecting an approximately 5 kΩ resistor in series to the GND could improve noise immunity.
In this case as well as the above mention, connect the pin the shortest possible to the GND pattern which is supplied to the Vss pin of the microcomputer.

(2) OSCSEL=H
Connect the OSCSEL pin the shortest possible to the VCC pattern which is supplied to the VCC pin of the microcomputer.
In addition connecting an approximately 5 kΩ resistor in series to the VCC could improve noise immunity. In this case as well as the above mention, connect the pin the shortest possible to the VCC pattern which is supplied to the Vcc pin of the microcomputer.

6. Notes on Replacement

Although the 38D5 Group is pin-compatible with the 38C5 Group, in the 38D5 Group, pin name of the 9th pin has been altered to OSCSEL from CNVss by the added function of the CPU mode register. When the OSCSEL pin is “L” level, the 38D5 Group operating mode is the same as the 38C5 Group. (Refer to P6 for details.)

Registers have been added with functions of ROM correction, watchdog timer and on-chip oscillator added. (Refer to P5 for details.) Check ROM correction in the 38D5 data sheet.

When these added functions are not used, process the added registers (bits) as follows (1) or (2) :

(1) Do not write anything to the added registers (bits) (hold an initial value after reset).
(2) Write the initial value to the added registers (bits) after reset.

While handling (1) or (2) is progress, the program of the 38C5 Group specification can be operated in the 38D5 Group specifications without modifying the program, except for the setting the CPU mode register in a program. Refer to P6 for the CPU mode register.

Addresses $FFD0_{16}$ to $FFDB_{16}$ in the 38D5 Group are reserved ROM areas. These areas overlap with ID code areas of one-time PROM version in the 38C5 Group (addresses $FFD4_{16}$ to $FFDA_{16}$). These areas are also user ROM areas for the mask ROM version.

Contact an oscillator manufacturer. Select an oscillator and oscillation circuit constants to obtain the stabilized operation clock on the user system and its condition for mass-production since the oscillation circuits are different between the 38C5 Group and 38D5 Group, and oscillation circuit constants of XIN-XOUT, XCIN-XCOUT are different every product.

Be careful especially when range of voltage and temperature is wide.

We recommend to design the circuit in consideration of the wiring pattern of the feed-back resistor, the dumping resistor and the load capacity in advance.

The 38D5 Group has been considered compatibility and designed for characteristics, actual values such as operation margin, A/D conversion accuracy, noise immunity, and noise radiation in electrical characteristics depending on the differences in the manufacturing processes may be different.

In the 38D5 Group, noise radiation is decreased compared with the 38C5 Group. Perform sufficient evaluations every individual product.

7. Reference

Data Sheet

38C5 Group Datasheet

38C5 Group Datasheet (One time PROM version)

38D5 Group Datasheet

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REVISION HISTORY	Difference between 38C5 Group and 38D5 Group

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		Page	Summary
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