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Renesas Electronics Corporation

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38C1 Group, 38D2 Group

Difference between 38C1 Group and 38D2 Group

1. Difference between 38C1 Group and 38D2 Group

Table 1.1 Difference Between 38C1 Group and 38D2 Group (1)

	38C1 Group		38D2 Group
	Mask ROM	One-time PROM	QzROM
Part number	M38C12M4-XXXFP/HP M38C13M6-XXXFP/HP	M38C13E6FP/HP	M38D24G4FP/HP,M38D24G4-XXXFP/HP M38D24G6FP/HP,M38D24G6-XXXFP/HP M38D28G8FP/HP,M38D28G8-XXXFP/HP M38D29GCFP/HP,M38D29GC-XXXFP/HP M38D29GFFP/HP,M38D29GF-XXXFP/HP
Package	PLQP0064KB-A (Old part no. 64P6Q-A): 64-pin LQFP (0.5 mm pin-pitch) PLQP0064GA-A (Old part no. 64P6U-A): 64-pin LQFP (0.8 mm pin-pitch) (Refer to P4 for pin configurations comparison)		
ROM type: ROM/RAM size	MASK: 16K/384, 24K/512	OTP: 24K/512	QzROM: 16K/640, 24K/640, 32K/1.5K, 48K/2K, 60K/2K
On-chip oscillator mode	Available		
Watchdog timer	N/A		Available (8 bits x 1) (Refer to P10 for details) (On-chip oscillator selectable)
CPU mode register	Refer to P9 for details		
Operation mode at reset and exiting from stop mode	On-chip oscillator mode		Depends on OSCSEL pin (Note 1) status When OSCSEL=H: f(X_{IN})/8 mode When OSCSEL=L: On-chip oscillator mode
Maximum oscillation frequency	8.0 MHz		16.0 MHz (Note 2)
Clock output function	Available (Refer to P11 for output control)		
ROM correction function	N/A		Available (Refer to datasheet)
Reserved ROM area (ROM code protect address)	—	—	$FFDB_{16}$

Notes: 1. The pin name of the 7th pin is changed from CNVSS to OSCSEL in 38D2 Group.

2. 12.5MHz< f(XIN)≤16MHz is not available in frequency/2 mode in 38D2 Group.

Refer to each group's datasheet for absolute maximum ratings, electric characteristics, and recommended operating conditions.

Table 1.2 Difference Between 38C1 Group and 38D2 Group (2)

	38C1 Group		38D2 Group
	Mask ROM	One-time PROM	QzROM
Programmable I/O port	30		51
Shared SEG port	16		24 (Note 3)
Internal pull-up resistor	Available		
Internal pull-down resistor	Available		N/A
Interrupt source	13 sources, 13 vectors		18 sources, 16 vectors (Refer to P8 for interrupt vector comparison)
Serial interface	8 bits x 1 (Clock synchronous)		8 bits x 2 (UART or clock synchronous)
Synchronous clock count source	1/8, 1/16, 1/32, 1/64,1/128,1/256 x ϕSOURCE (Note 4)		1/4, 1/16 x ϕSOURCE (Note 5) or external clock
Serial interface: Transfer direction	LSB first or MSB first		LSB first
PWM	N/A		10 bits x 2, 16 bits x 1 (shared with IGBT output)
LED direct drive port	5		8
LCD drive control circuit: Maximum number of pixels	100 pixels (4 com x 5 seg)		96 pixels (4 com x 24 seg)
LCD drive control circuit: Bias	1/1,1/2,1/3		1/2, 1/3
LCD drive control circuit: Duty ratio	1(Static), 2, 3, 4		2, 3, 4
LCD driving timing selection bit	N/A		Available
LCD power dividing resistor	N/A		Available

Notes: 3. Each pull-up bit of the shared segment ports is controlled by setting direction registers and segment output disable registers (Refer to 38D2 Group datasheet).

4. and 5. → See notes 4 and 5 on P3.

Refer to each group's datasheet for absolute maximum ratings, electric characteristics, and recommended operating conditions.

Table 1.3 Difference Between 38C1 Group and 38D2 Group (3)

	38C1 Group		38D2 Group
	Mask ROM	One-time PROM	QzROM
8-bit timer	3		4
8-bit timer: Operation mode	Timer mode		Timer mode, PWM mode (Timer 3, Timer 4)
8-bit timer: Count source	1/1 x f(XCIN), 1/16 x ϕSOURCE (Note 4), 1/16 x f(XIN) (Refer to datasheet)		1/1, 1/2, 1/16, 1/256 x ϕSOURCE (Note 5)
16-bit timer: Count source	1/1(only in pulse output mode), 1/16 x ϕSOURCE (Note 4)		1/1, 1/2, 1/16, 1/256 x ϕSOURCE (Note 5)
Timer X: Operation mode	Timer mode, pulse output mode, event counter mode, pulse width measurement mode		Timer mode, pulse output mode, event counter mode, pulse width measurement mode, IGBT mode, PWM mode
Timer X: IGBT output mode /PWM mode	N/A		Compare register x 3
Timer X output port	1 (*Output from CNTR0 pin in pulse output mode)		2 (TXOUT2 pin added)
Timer Y: Operation mode	Timer mode, period measurement mode, event counter mode, pulse width continuous measurement mode		
Timer Y: Real time port control	N/A		Available
A/D converter	8 bits x 8 (Available in low-speed mode)		10 bits x 8 (Available in low-speed mode)
ADKEY function	Available (Refer to datasheet)		
RRF register	Available		
Temporary data register	Available		N/A

Notes: 4. ϕSOURCE = XIN input in frequency/2, 8 mode, on-chip oscillator in on-chip oscillator mode, oscillation frequency of sub-clock in low-speed mode (Refer to 38C1 group datasheet)
5. ϕSOURCE = XIN input in frequency/2, 4, 8 mode, on-chip oscillator/4 in on-chip oscillator mode, oscillation frequency of sub-clock in low-speed mode (Refer to 38D2 group datasheet)

Refer to each group's datasheet for absolute maximum ratings, electric characteristics, and recommended operating conditions.

2. Pin configurations of 38C1 Group and 38D2 Group (Top View)

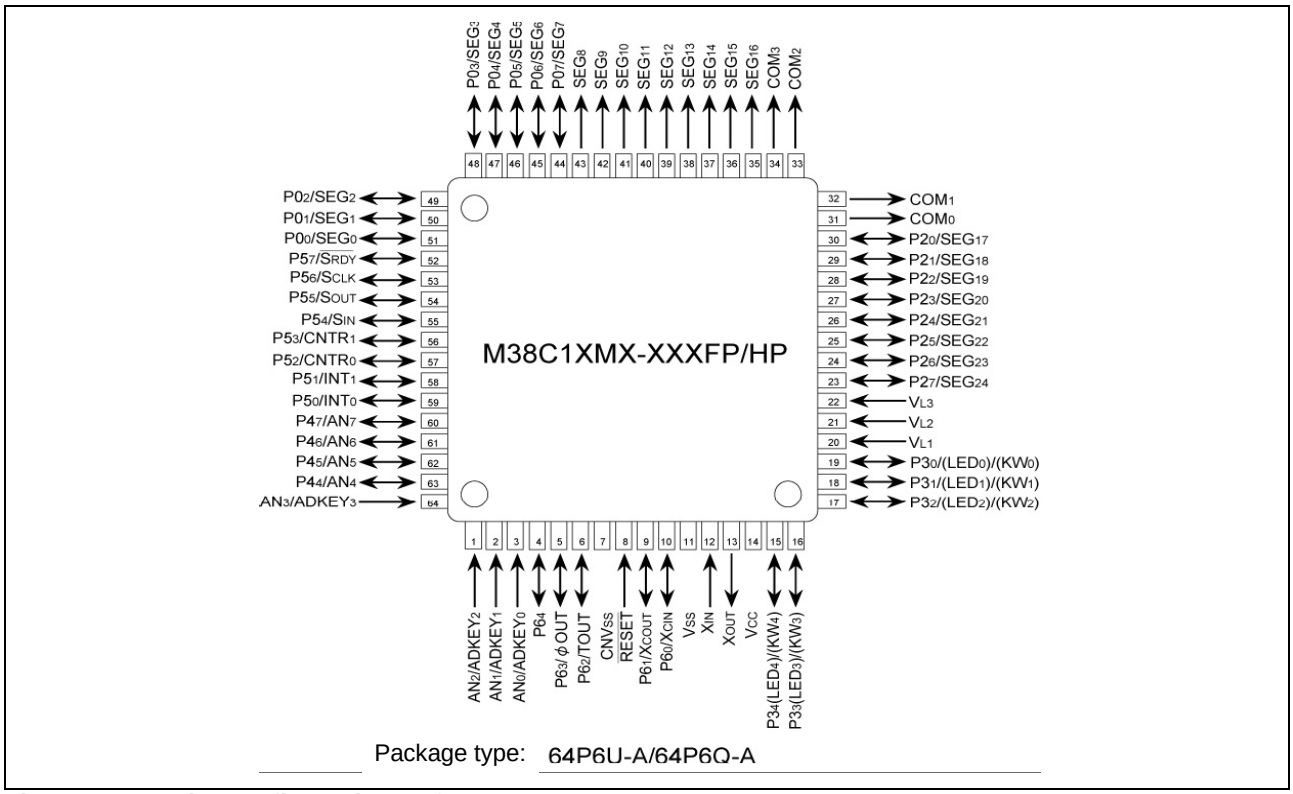


Figure 2.1 Pin Configurations of 38C1 Group

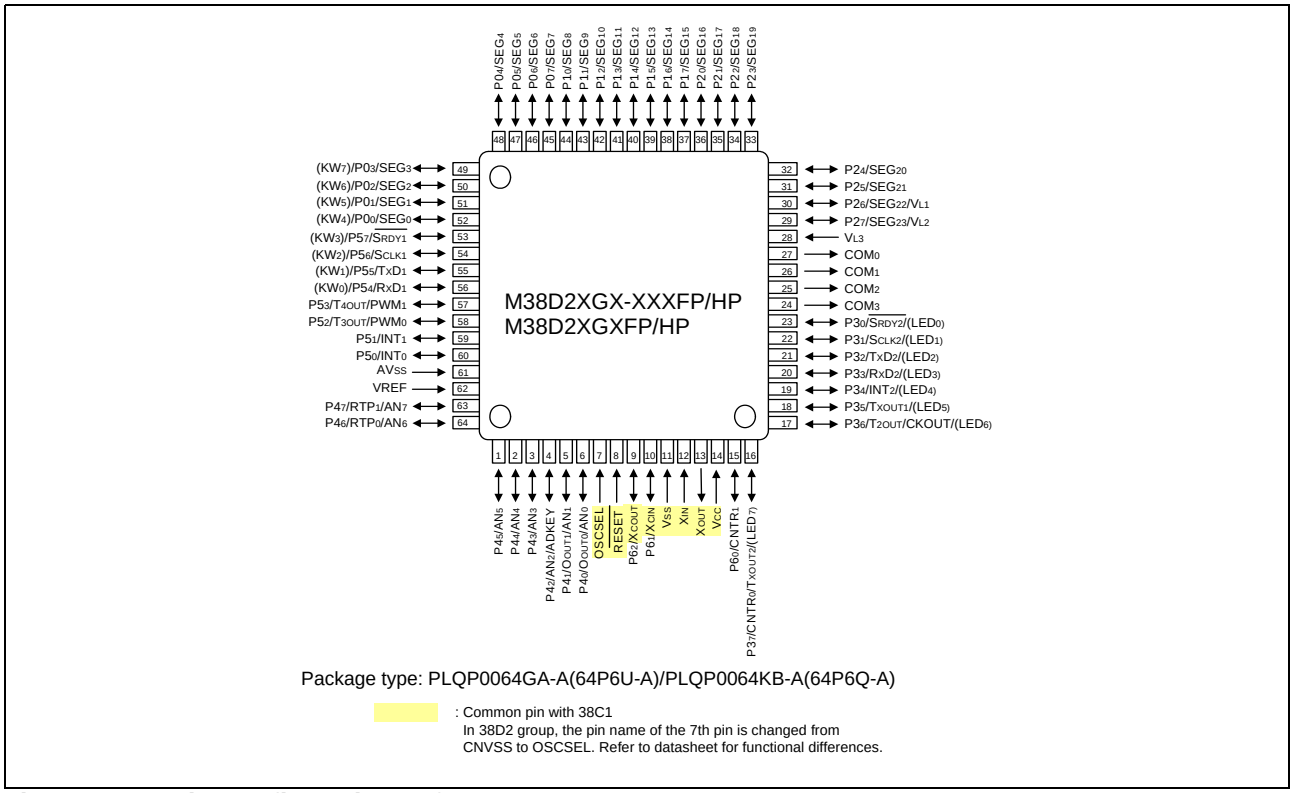


Figure 2.2 Pin Configurations of 38D2 Group

3. SFR comparison between 38C1 Group and 38D2 Group

Table 3.1 SFR Comparison Between 38C1 Group and 38D2 Group (1)

	38C1 Group	38D2 Group
0000_{16}	Port P0 (P0)	Port P0 (P0)
0001_{16}		Port P0 direction register (P0D)
0002_{16}		Port P1 (P1)
0003_{16}		Port P1 direction register (P1D)
0004_{16}	Port P2 (P2)	Port P2 (P2)
0005_{16}	Port P2 direction register (P2D)	Port P2 direction register (P2D)
0006_{16}	Port P3 (P3)	Port P3 (P3)
0007_{16}	Port P3 direction register (P3D)	Port P3 direction register (P3D)
0008_{16}	Port P4 (P4)	Port P4 (P4)
0009_{16}	Port P4 direction register (P4D)	Port P4 direction register (P4D)
$000A_{16}$	Port P5 (P5)	Port P5 (P5)
$000B_{16}$	Port P5 direction register (P5D)	Port P5 direction register (P5D)
$000C_{16}$	Port P6 (P6)	Port P6 (P6)
$000D_{16}$	Port P6 direction register (P6D)	Port P6 direction register (P6D)
$000E_{16}$		
$000F_{16}$		
0010_{16}	LCD display register 0 (LCD_0)	Oscillation output control register (OSCOUT)
0011_{16}	LCD display register 1 (LCD_1)	CPU mode register 2 (CPUM2)
0012_{16}	LCD display register 2 (LCD_2)	RRF register (RRFR)
0013_{16}	LCD display register 3 (LCD_3)	LCD mode register (LM)
0014_{16}	LCD display register 4 (LCD_4)	LCD power control register (VLCON)
0015_{16}	LCD display register 5 (LCD_5)	AD control register (ADCON)
0016_{16}	LCD display register 6 (LCD_6)	AD conversion register (low-order) (ADL)
0017_{16}	LCD display register 7 (LCD_7)	AD conversion register (high-order) (ADH)
0018_{16}	LCD display register 8 (LCD_8)	Transmit/Receive buffer register 1 (TB1/RB1)
0019_{16}	LCD display register 9 (LCD_9)	Serial I/O1 status register (SIO1STS)
$001A_{16}$	LCD display register 10 (LCD_{10})	Serial I/O1 control register (SIO1CON)
$001B_{16}$	LCD display register 11 (LCD_{11})	UART1 control register (UART1CON)
$001C_{16}$	LCD display register 12 (LCD_{12})	Baud rate generator 1 (BRG1)
$001D_{16}$	Serial I/O control register (SIOCON)	Transmit/Receive buffer register 2 (TB2/RB2)
$001E_{16}$		Serial I/O2 register (SIO2STS)
$001F_{16}$	Serial I/O register (SIO)	Serial I/O2 control register (SIO2CON)

Note: Do not access memory in free space of SFR.

: New SFR in 38D2

: Register contents changed (same register name and address)

: Address changed (same register name and contents)

:Register contents and address changed (same register name)

Table 3.2 SFR Comparison Between 38C1 Group and 38D2 Group (2)

	38C1 Group	38D2 Group
0020₁₆	Timer X (low-order) (TXL)	Timer 1 (T1)
0021₁₆	Timer X (high-order) (TXH)	Timer 2 (T2)
0022₁₆	Timer Y (low-order) (TYL)	Timer 3 (T3)
0023₁₆	Timer Y (high-order) (TYH)	Timer 4 (T4)
0024₁₆	Timer 1 (T1)	PWM01 register (PWM01)
0025₁₆	Timer 2 (T2)	Timer 12 mode register (T12M)
0026₁₆	Timer 3 (T3)	Timer 34 mode register (T34M)
0027₁₆	Timer X mode register (TXM)	Timer 1234 mode register (T1234M)
0028₁₆	Timer Y mode register (TYM)	Timer 1234 frequency division selection register (PRE1234)
0029₁₆	Timer 123 mode register (T123M)	Watchdog timer control register (WDTCON)
002A₁₆	Φ output control register	Timer X (low-order) (TXL)
002B₁₆		Timer X (high-order) (TXH)
002C₁₆	Temporary data register 1 (TD0)	Timer X (Expansion) (TXEX)
002D₁₆	Temporary data register 2 (TD1)	Timer X mode register (TXM)
002E₁₆	Temporary data register 3 (TD2)	Timer X control register 1 (TXCON1)
002F₁₆	RRF register (RRFR)	Timer X control register 2 (TXCON2)
0030₁₆		Compare register 1 (low-order) (COMP1L)
0031₁₆		Compare register 1 (high-order) (COMP1H)
0032₁₆		Compare register 2 (low-order) (COMP2L)
0033₁₆	PULL register (PULL)	Compare register 2 (high-order) (COMP2H)
0034₁₆	AD control register (ADCON)	Compare register 3 (low-order) (COMP3L)
0035₁₆	AD conversion register (AD)	Compare register 3 (high-order) (COMP3H)
0036₁₆		Timer Y (low-order) (TYL)
0037₁₆		Timer Y (high-order) (TYH)
0038₁₆	Segment output enable register (SEG)	Timer Y mode register (TYM)
0039₁₆	LCD mode register (LM)	Timer Y control register (TYCON)
003A₁₆	Interrupt edge selection register (INTEDGE)	Interrupt edge selection register (INTEDGE)
003B₁₆	CPU mode register (CPUM)	CPU mode register (CPUM)
003C₁₆	Interrupt request register 1(IREQ1)	Interrupt request register 1 (IREQ1)
003D₁₆	Interrupt request register 2(IREQ2)	Interrupt request register 2 (IREQ2)
003E₁₆	Interrupt control register 1(ICON1)	Interrupt control register 1 (ICON1)
003F₁₆	Interrupt control register 2(ICON2)	Interrupt control register 2 (ICON2)

Note: Do not access memory in free space of SFR.

: New SFR in 38D2

: Register contents changed (same register name and address)

: Address changed (same register name and contents)

:Register contents and address changed (same register name)

Table 3.3 SFR Comparison Between 38C1 Group and 38D2 Group (3)

	38C1 Group	38D2 Group
0FF0$_{16}$		PULL register (PULL)
0FF1$_{16}$		UART2 control register (UART2CON)
0FF2$_{16}$		Baud rate generator 2 (BRG2)
0FF3$_{16}$		Clock output control register (CKOUT)
0FF4$_{16}$		Segment output disable register 0 (SEG0)
0FF5$_{16}$		Segment output disable register 1 (SEG1)
0FF6$_{16}$		Segment output disable register 2 (SEG2)
0FF7$_{16}$		Key input control register (KIC)
0FF8$_{16}$		ROM correction address 1 (high-order) (RCA1H)
0FF9$_{16}$		ROM correction address 1 (low-order) (RCA1L)
0FFA$_{16}$		ROM correction address 2 (high-order) (RCA2H)
0FFB$_{16}$		ROM correction address 2 (low-order) (RCA2L)
0FFC$_{16}$		ROM correction enable register (RCR)
0FFD$_{16}$		Reserved area (Do not access)
0FFE$_{16}$		Reserved area (Do not access)
0FFF$_{16}$		Reserved area (Do not access)

Note: Do not access memory in free space of SFR.

: New SFR in 38D2

:Register contents and address changed (same register name)

*** Do not access free space and reserved area on SFR memory map.**

4. Interrupt vector comparison between 38C1 group and 38D2 group

Table 4.1 Interrupt Vector Comparison Between 38C1 Group and 38D2 Group

: Difference between 38D5 Group and 38D2 Group

Vector address		Priority	38D5 Group Interrupt Source	38D2 Group Interrupt Source
high-order	low-order			
FFFD16	FFFC16	1	Reset	Reset
FFFB16	FFFA16	2	INT0 (INT00 or INT01)	INT0
FFF916	FFF816	3	INT1 (INT10 or INT11)	INT1
FFF716	FFF616	4	INT2	INT2 / Key input (Key-on wake up)
FFF516	FFF416	5	Key input (Key-on wake up)	CNTR0
FFF316	FFF216	6	Timer X	Timer X
FFF116	FFF016	7	Timer 1	Timer 1
FFEF16	FFEE16	8	Timer 2	Timer 2
FFED16	FFEC16	9	Timer 3	Timer 3
FFEB16	FFEA16	10	Timer 4	Timer 4
FFE916	FFE816	11	Serial I/O1 reception	Serial I/O1 reception
FFE716	FFE616	12	Serial I/O1 transmission	Serial I/O1 transmission
FFE516	FFE416	13	Serial I/O2	Serial I/O2 reception
FFE316	FFE216	14	CNTR0	Serial I/O2 transmission
FFE116	FFE016	15	Timer Y / CNTR1	Timer Y / CNTR1
FFDF16	FFDE16	16	A/D conversion	A/D conversion
FFDD16	FFDC16	17	BRK instruction	BRK instruction

5. CPU mode register

An oscillation operation (oscillating/stop oscillating) of internal on-chip oscillator can be selected by setting the on-chip oscillator stop bit at the CPU mode register 2 in 38D2 Group.

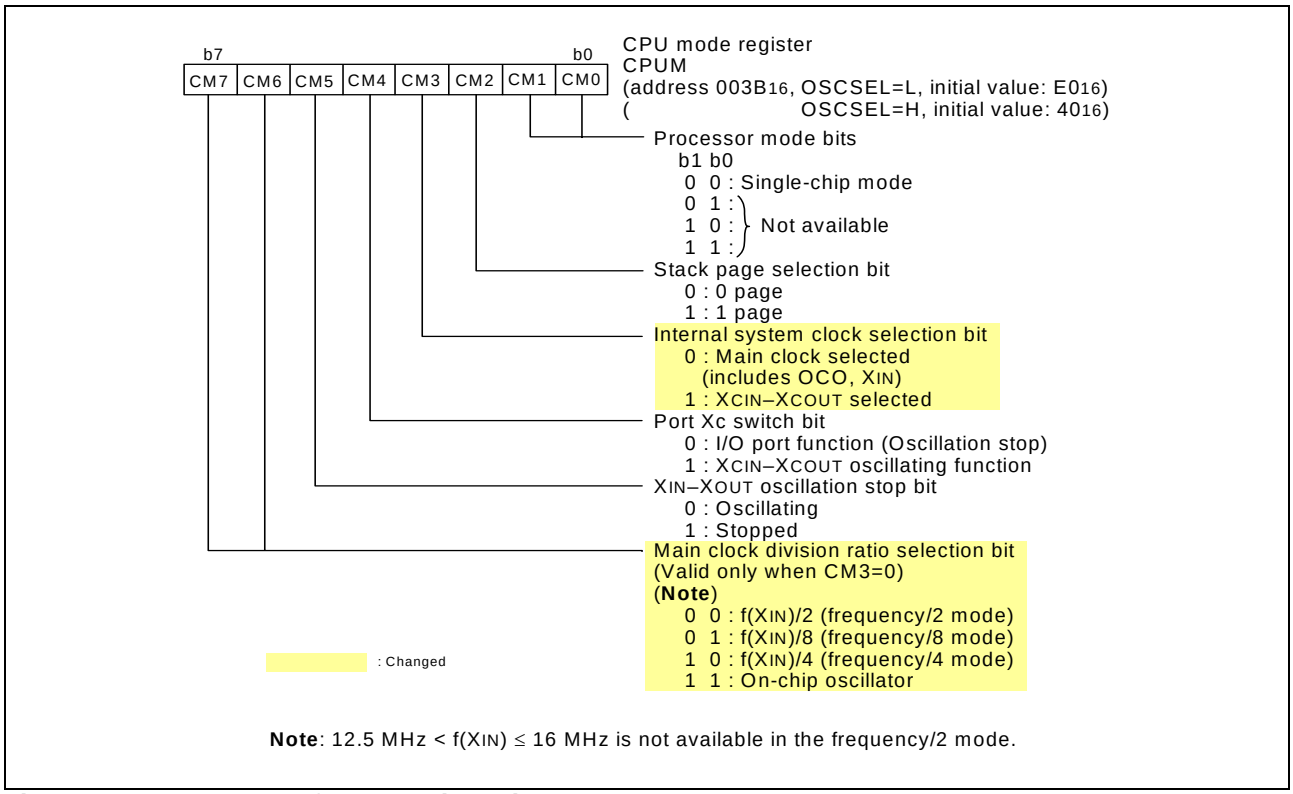


Figure 5.1 Structure of CPU mode register

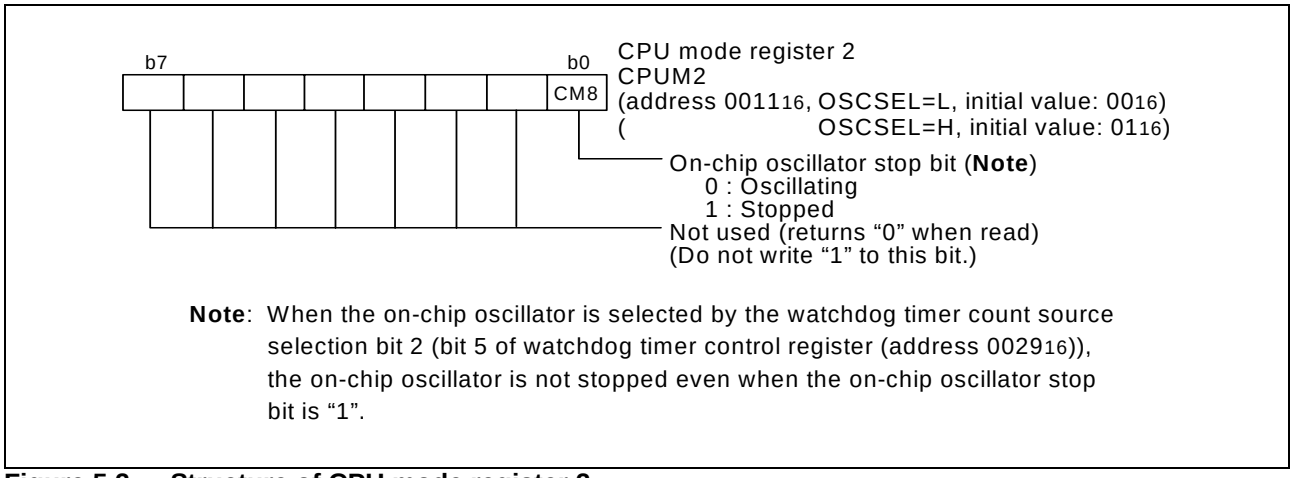
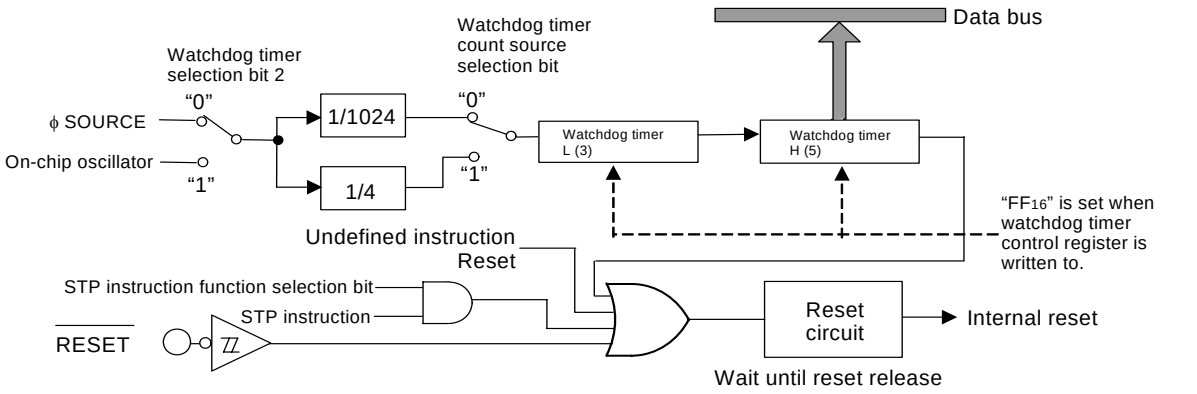


Figure 5.2 Structure of CPU mode register 2

An operation mode after exiting from stop mode or at reset can be selected by voltage applied to the OSCSEL pin in 38D2 Group.
OSCSEL pin = H: f(XIN)/8 mode
OSCSEL pin = L: ON-chip oscillator mode

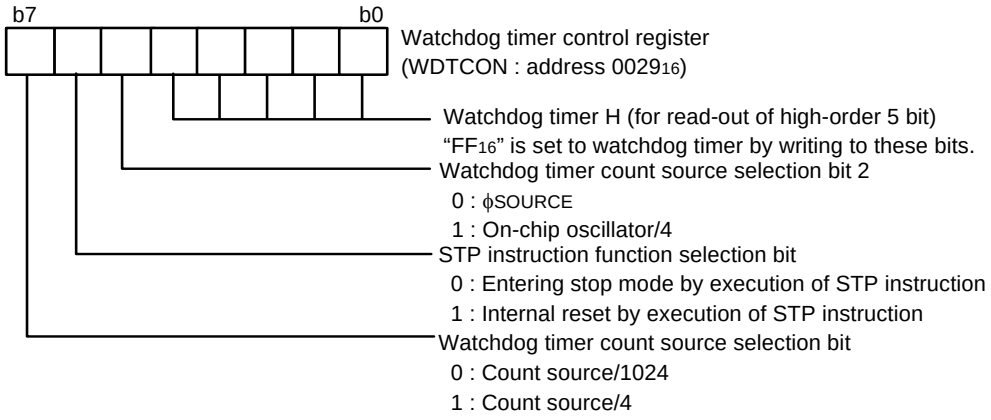
6. Watchdog Timer

The 38D2 group devices have the watchdog timer function. The watchdog timer consists of 8-bit counter and the count source can select on-chip oscillator by setting the watchdog timer count source selection bit 2. At this time, set the STP instruction function selection bit to 1.



Note: In frequency/2, frequency/4, or frequency/8 mode, ϕSOURCE is the XIN input. In on-chip oscillator mode, ϕSOURCE is the on-chip oscillator frequency divided by 4. In low-speed mode, ϕSOURCE is the sub-clock frequency.

Figure 6.1 Block diagram of watchdog timer function



Notes 1: ϕ SOURCE represents the supply source of internal clock ϕ.
XIN input: in the frequency/2, 4 or 8 mode,
Internal on-cihp oscillator divided by 4 in the on-chip oscillator mode, and Sub clock in the low-speed mode.
2: When the on-chip oscillator is selected by the watchdog timer count source selection bit 2 , set the STP instruction function selection bit to "1".
3: Bits 7 to 5 can be rewritten only once after releasing reset. After rewriting it is disable to write any data to this bit.

Figure 6.2 Structure of watchdog timer control register

7. Clock output function

The system clock f can be output from Port P63 in 38C1 Group and from P36 in 38D2 Group. In 38D2 Group, a clock output of the timer 2 is also possible in addition to the system clock f by the timer 2 output selection bit at the timer 12 mode register (address 0025$_{16}$).

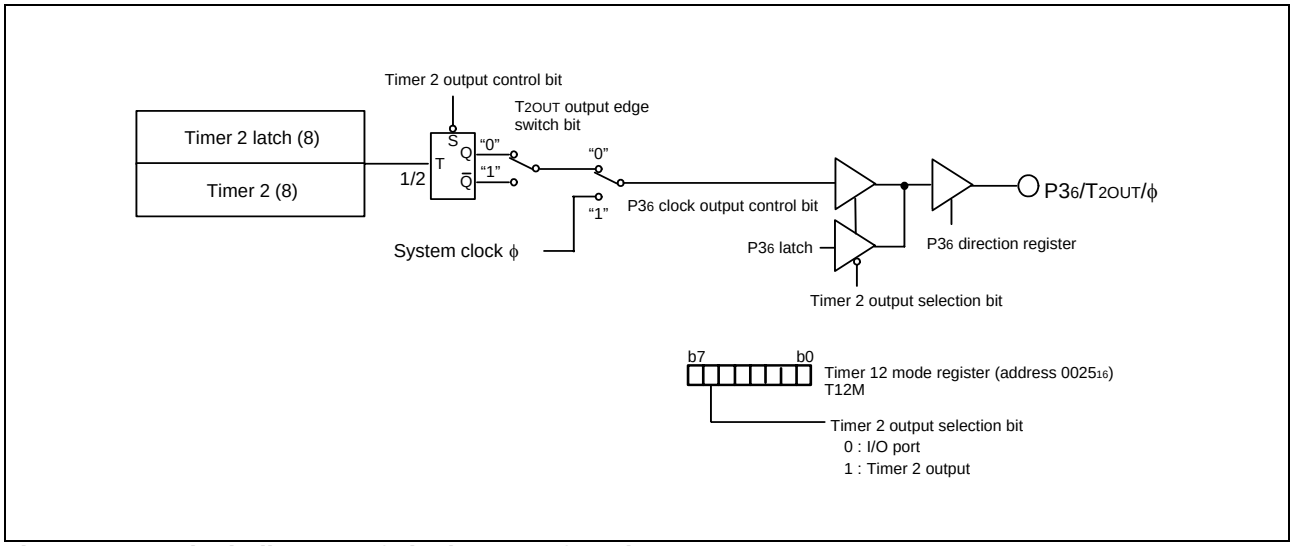


Figure 7.1 Block diagram of clock output function

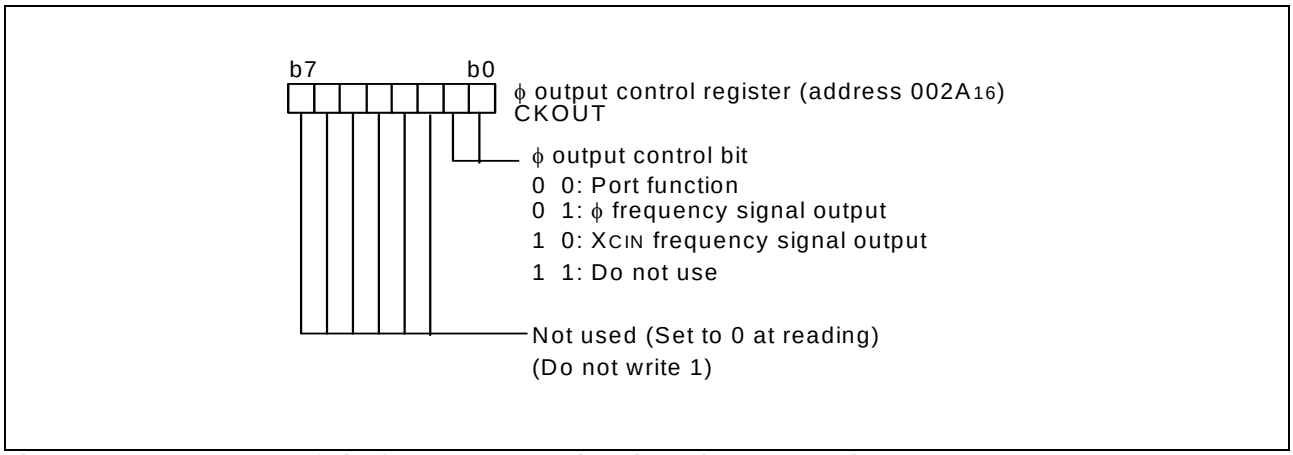


Figure 7.2 Structure of clock output control register (38C1 group)

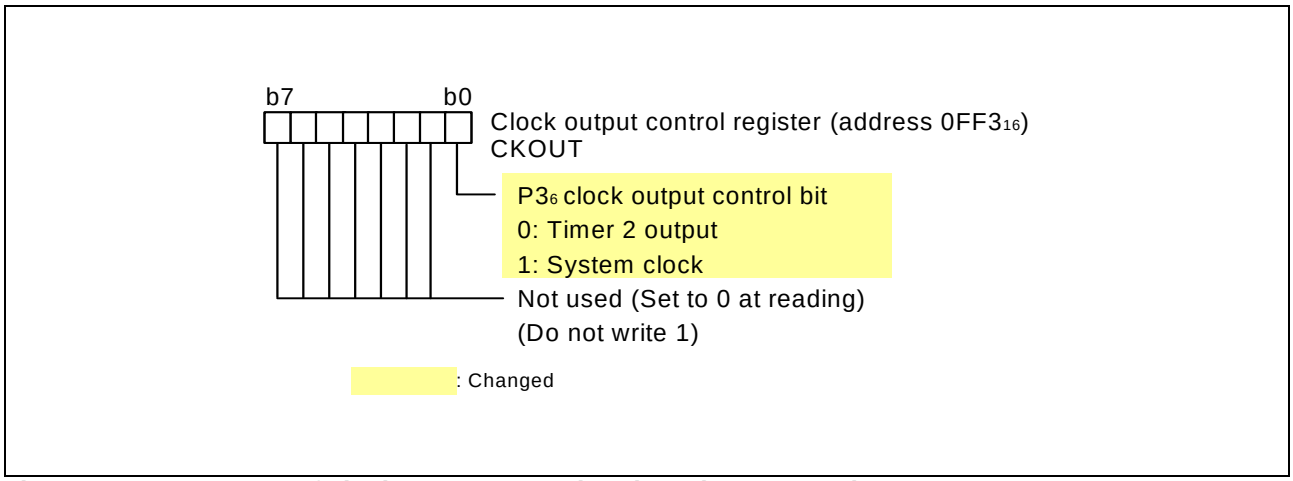


Figure 7.3 Structure of clock output control register (38D2 group)

8. Range of operating power source voltage in 38C1 Group and 38D2 Group (Excluding A/D operation)

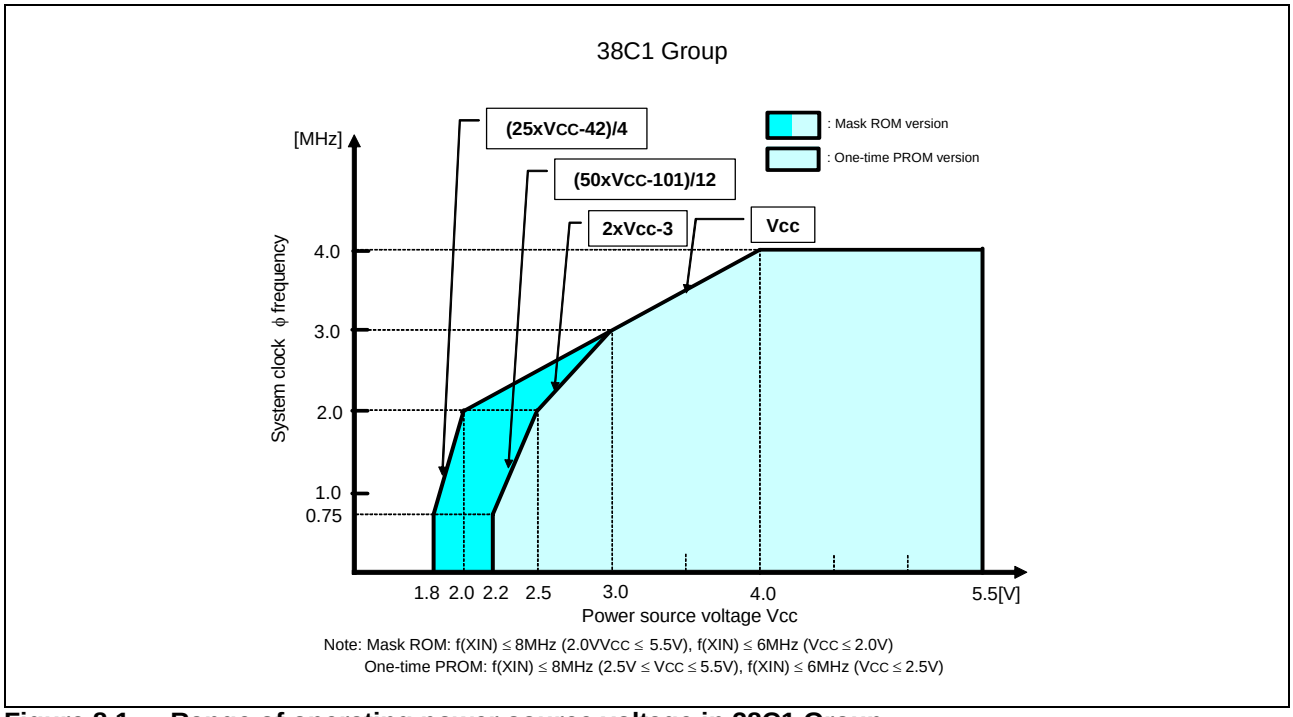


Figure 8.1 Range of operating power source voltage in 38C1 Group

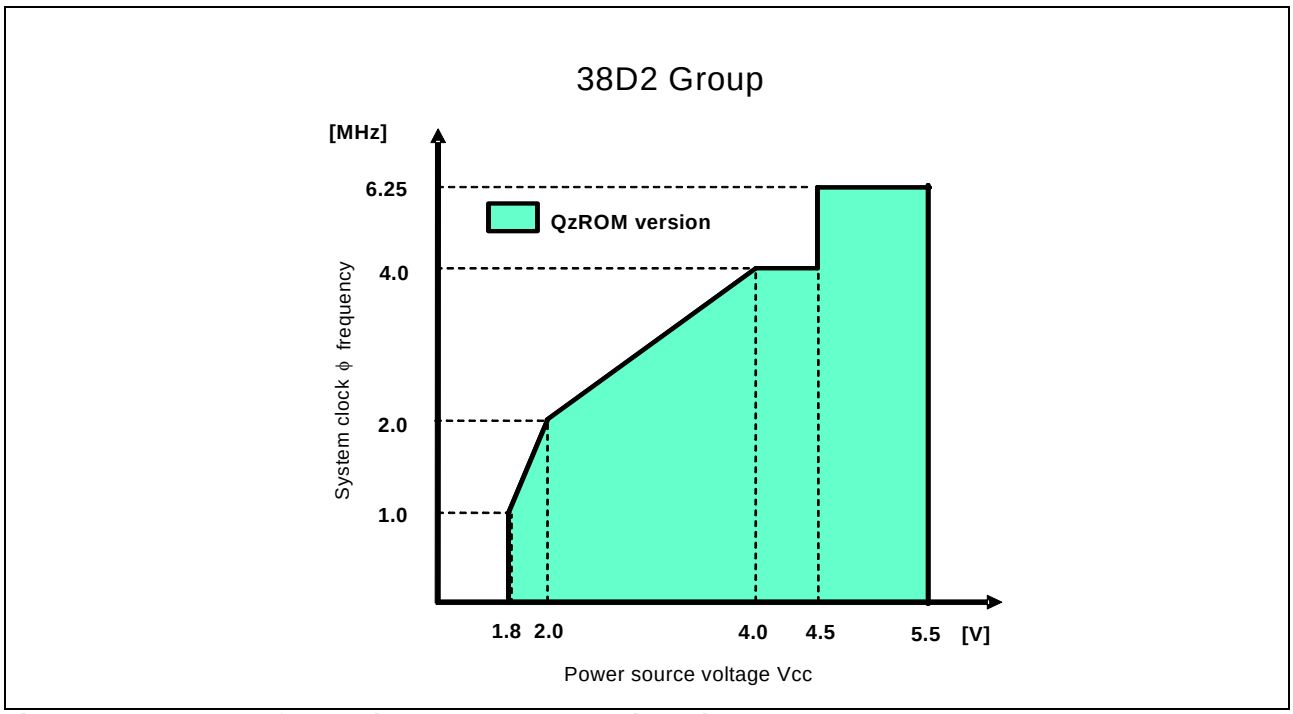


Figure 8.2 Range of operating power source voltage in 38D2 Group

9. Range of operating power source voltage in 38C1 Group and 38D2

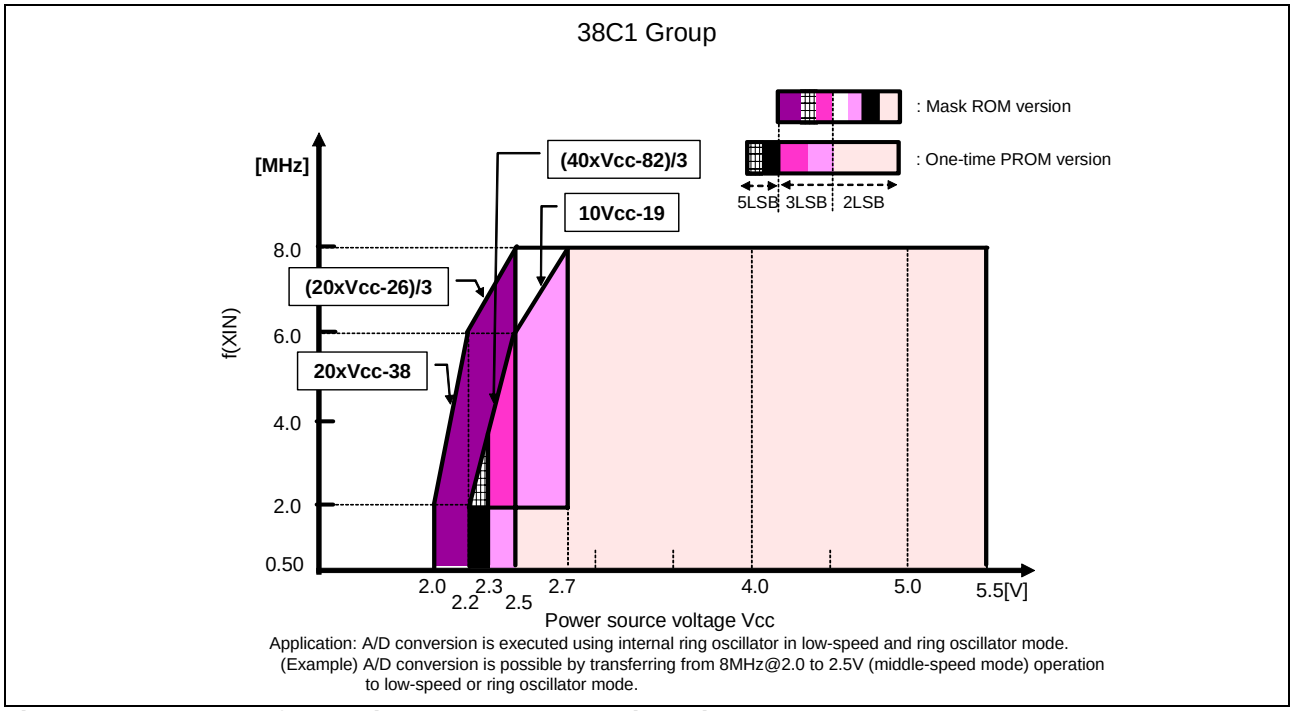


Figure 9.1 Range of operating power source voltage in 38C1 Group

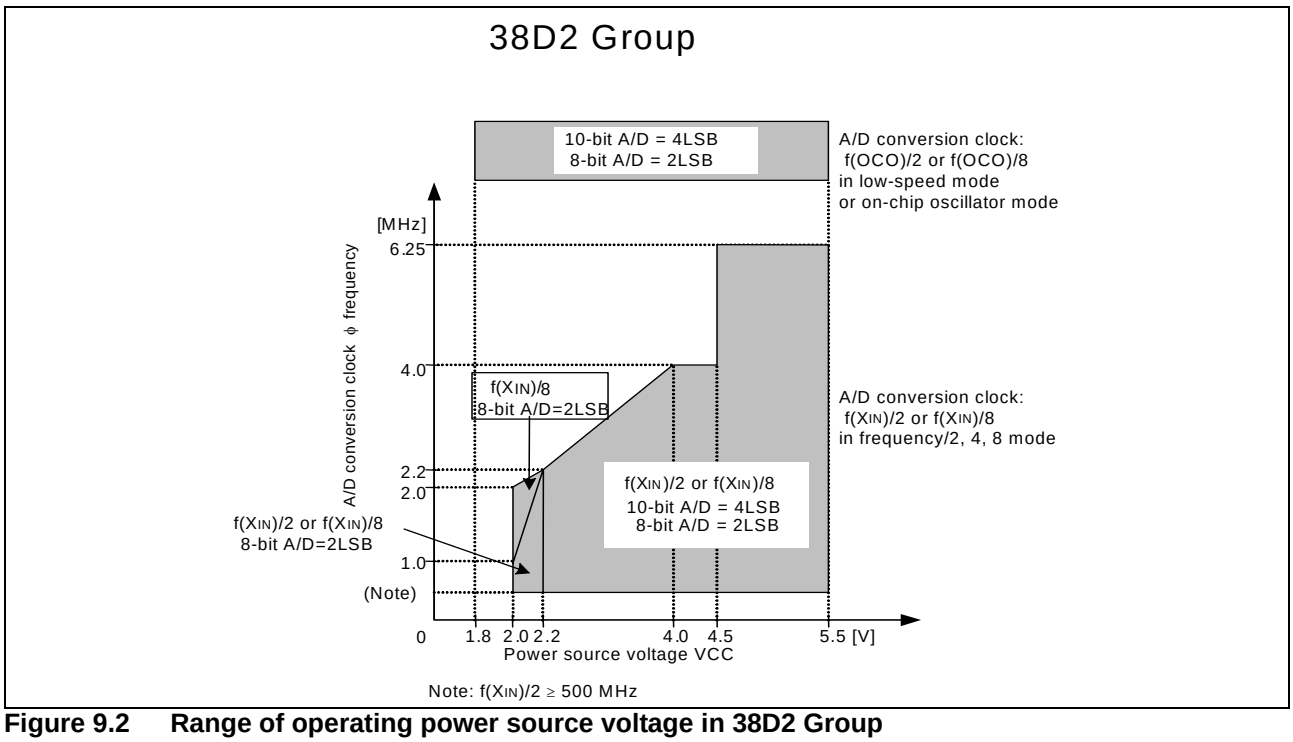


Figure 9.2 Range of operating power source voltage in 38D2 Group

10. OSCSEL pin wiring

The OSCSEL pin functions as the power source input pin for the built-in QzROM in 38D2 Group. The impedance of the OSCSEL pin is set to low to allow the electric current for writing to flow into the QzROM when writing a program in the QzROM. Because of this, noise comes in from the OSCSEL pin easier. When noise comes in from the OSCSEL pin, the MCU may go out of control because reading operation of instruction codes or data is not performed normally.

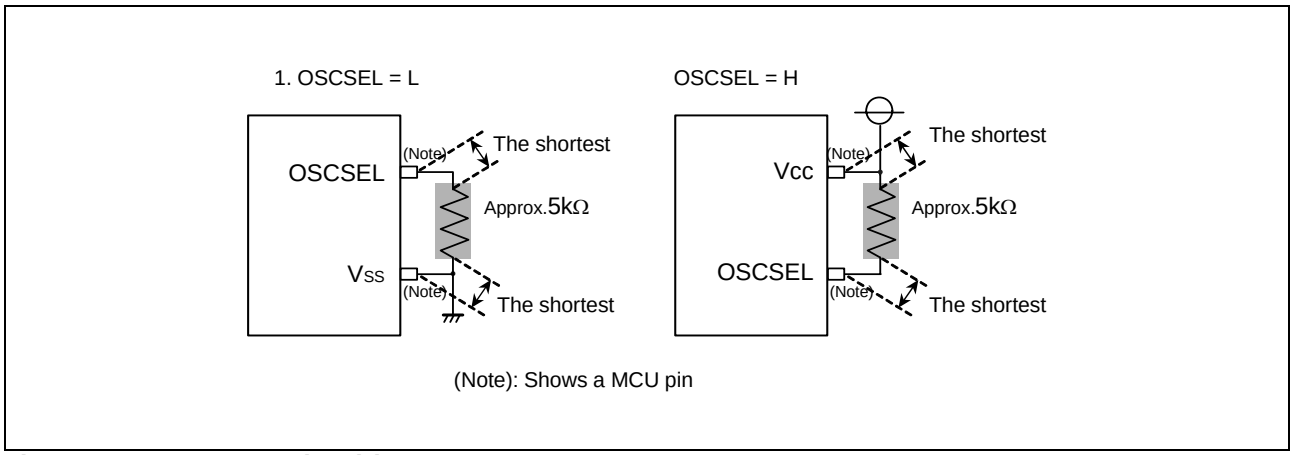


Figure 10.1 OSCSEL pin wiring

1. When OSCSEL = L:
Connect the OSCSEL pin by the shortest wiring to the GND pattern which is the closest to the GND supplying power to the Vss pin of the MCU. In addition, the noise immunity may be improved by connecting a resistor of approximately 5 kΩ to the GND in series. At this time, connect the OSCSEL pin by the shortest wiring to the GND pattern which is as close as possible to the GND supplying to the Vcc pin of the MCU as written above.

2. When OSCSEL = H:
Connect the OSCSEL pin by the shortest wiring to the Vcc pattern which is the closest to the Vcc supplying power to the Vcc pin of the MCU. In addition, the noise immunity may be improved by connecting a resistor of approximately 5 kΩ to the Vcc in series. At this time, connect the OSCSEL pin by the shortest wiring to the Vcc pattern which is the closest to the Vcc supplying power to the Vcc pin of the MCU as written above.

11. Notes on Replacement

The 38C1 group devices and the 38D2 group devices have different oscillation circuit structures. In addition, oscillation circuit constants of XIN-XOUT, XCIN-XCOUT vary in each product. Therefore, contact an oscillator manufacture when selecting an oscillator and oscillation circuit constants so that a stable operation clock can be obtained on the user system and conditions for mass-production. Be careful especially when the range of voltage and temperature is wide. Considering the wiring pattern of the feed-back resistor, the dumping resistor, and the load capacity in advance is recommended when designing a circuit.

In addition, although compatibility in characteristics is fully considered in designing each device, actual values such as operating margin, A/D conversion accuracy, noise immunity, noise radiation may be different within the range of electrical characteristics due to different manufacturing processes. Therefore, perform sufficient system evaluations for every individual product before starting mass-production.

12. Datasheet

38C1 Group Datasheet
38D2 Group Datasheet
Download the latest version from the Renesas Technology website.

Technical News/Technical Update
Download the latest information from the Renesas Technology website.

Website and Support

Renesas Technology website
http://www.renesas.com

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http://www.renesas.com/inquiry
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REVISION HISTORY	38C1 Group, 38D2 Group Difference between 38C1 Group and 38D2 Group

Rev.	Date	Description	
		Page	Summary
1.00	Feb 16, 2007	–	First Edition issued
1.01	Jan 15, 2008	1,5,6, 7,8	Clerical error revised

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