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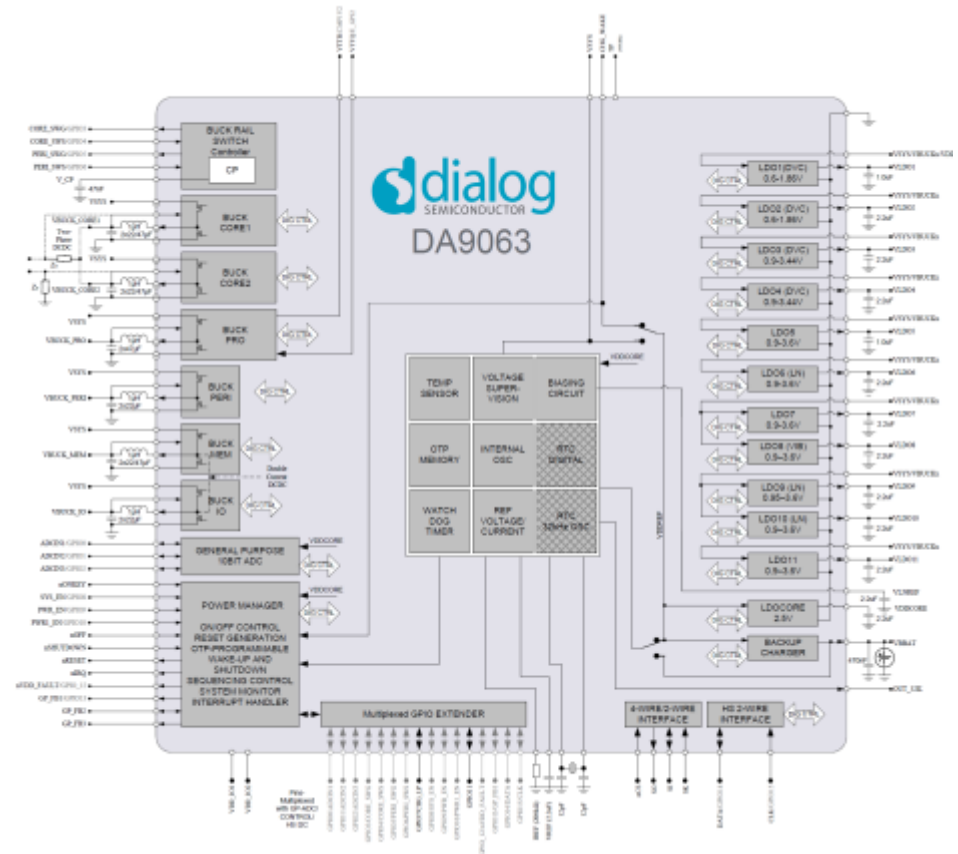
# Dialog Power Tree solutions for Xilinx Zynq Ultrascale+ MPSoC

Jan 2017

# Dialog Power Solutions

Dialog specializes in a range of flexible, OTP programmable PMIC products.

- At the heart of the Dialog PMIC family is the DA9063 System PMIC



# DA9063

## Key blocks and features

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- 6x 3 MHz buck converters with programmable current limits.
  - 11x LDO linear regulators.
  - 2x slew rate programmable rail switch controllers (with charge pump for drive voltage generation).
  - Programmable power sequencer.
  - Low quiescent current 32 kHz crystal oscillator and RTC clock with alarm.
  - Backup battery or super-cap charger with programmable voltage and current limit.
  - 16x GPIO, some with dedicated alternative functionality.
  - Can be controlled via 2-wire I<sup>2</sup>C or 4-wire SPI.
  - 10bit multi-channel ADC.
  - Voltage supervisory function able to monitor input and output voltages.
    - Provides for a controlled shutdown in the event of brown-outs on input or output.
  - Watchdog supervisor for automatic recovery from a system software crash.
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- AEC-Q100 Grade3

# DA9063

## Buck power supplies

### 6x high current bucks

- BuckCore1 and 2 are identical and can optionally be combined to provide a dual phase double current output (5 A total).
  - BuckMem and BuckIO can optionally be combined to provide single phase double current output (3 A total).
  - BuckPeri is designed to power higher voltage peripherals.
  - BuckPro is similar but has the option to sink and source current in memory termination (VTT) mode.
  - Each buck has a pull-down resistor that can be configured to automatically turn on when the buck is disabled.
- All bucks can perform DVC ramping during output voltage changes.
  - All bucks can be operated in:
    - PWM mode for fixed frequency operation
    - PFM mode for best efficiency at low load currents
    - Auto mode for best efficiency across all load currents

DA9063	Vout (V)	Iout Single (A)	Iout Merged (A)	DVC	Bypass	Low Noise	Notes
BuckCore1	0.30 - 1.57	2.50	5.00	Y			
BuckCore2	0.30 - 1.57	2.50					
BuckMem	0.80 - 3.34	1.50	3.00	Y			
BuckIO	0.80 - 3.34	1.50					
BuckPeri	0.80 - 3.34	1.50	-	Y			
BuckPro	0.53 - 1.80	2.50	-	Y			VTT mode
LDO1	0.60 - 1.86	0.10	-	Y			Always on
LDO2	0.60 - 1.86	0.20	-	Y			
LDO3	0.90 - 3.34	0.20	-	Y	Y		
LDO4	0.90 - 3.34	0.20	-	Y	Y		
LDO5	0.90 - 3.60	0.10	-				
LDO6	0.90 - 3.60	0.20	-			Y	
LDO7	0.90 - 3.60	0.20	-		Y		
LDO8	0.90 - 3.60	0.20	-		Y		
LDO9	0.95 - 3.60	0.20	-			Y	
LDO10	0.90 - 3.60	0.30	-			Y	
LDO11	0.90 - 3.60	0.30	-		Y		
CORE_SW							Rail Switch
PERI_SW							Rail Switch

# DA9063

## LDO power supplies & GPIO

### 11x LDOs

- LDO1 – 4 can perform DVC ramping during output voltage changes.
  - LDO1 can optionally be set as “always on”.
- LDO3, 4, 7, 8 & 11 can be operated in an unregulated bypass mode.
  - Allowing them to be used as sequenced rail switches.
- LDO6, 9 & 10 are designed to be very low noise output.
- 2x LDOs have 100mA load current capability
- 7x LDOs have 200mA load current capability
- 2x LDOs have 300mA load current capability

DA9063	Vout (V)	Iout Single (A)	Iout Merged (A)	DVC	Bypass	Low Noise	Notes
BuckCore1	0.30 - 1.57	2.50	5.00	Y			
BuckCore2	0.30 - 1.57	2.50					
BuckMem	0.80 - 3.34	1.50	3.00	Y			
BuckIO	0.80 - 3.34	1.50					
BuckPeri	0.80 - 3.34	1.50	-	Y			
BuckPro	0.53 - 1.80	2.50	-	Y			VTT mode
LDO1	0.60 - 1.86	0.10	-	Y			Always on
LDO2	0.60 - 1.86	0.20	-	Y			
LDO3	0.90 - 3.34	0.20	-	Y	Y		
LDO4	0.90 - 3.34	0.20	-	Y	Y		
LDO5	0.90 - 3.60	0.10	-				
LDO6	0.90 - 3.60	0.20	-			Y	
LDO7	0.90 - 3.60	0.20	-		Y		
LDO8	0.90 - 3.60	0.20	-		Y		
LDO9	0.95 - 3.60	0.20	-			Y	
LDO10	0.90 - 3.60	0.30	-			Y	
LDO11	0.90 - 3.60	0.30	-		Y		
CORE_SW							Rail Switch
PERI_SW							Rail Switch

### GPIO

- 16 flexible GPIO
- 5 controllable via the sequencer for the control of sub PMICs

# DA921x Sub PMICs

Powering the high current rails of SOC

The DA921x family of sub PMIC's are designed to work alongside a System PMIC such as the DA9063

The Sub-PMIC family consists of 6 members:

Device	Current	Phase
DA9210	12A	4
DA9211	12A	4
DA9212	6A+6A	2,2
DA9213	20A	4
DA9214	15A +5A	3,1
DA9215	10A+10A	2,2

Combining these building blocks it is possible to address the power tree requirements for a wide range of systems such as the Xilinx Zynq Ultrascale+ MPSoc range.

# Automotive Solutions

Many of the Dialog PMIC products are already automotive qualified to AECQ-100 grade 3 with further qualification to grade 2 in progress during DA2017.

DA9062-A AECQ 100 grade 3

DA9063-A AECQ 100 grade 3, grade 2 qualification ongoing.

DA9210-A AECQ 100 grade 3

DA9213-A AECQ 100 grade 2, 1H 2017

DA9214-A AECQ 100 grade 2, 1H 2017

This means that a common design can be ported between Automotive and Consumer/industrial applications with a fairly simple exchange of the passive components  
And by specifying the –A PMIC part.

# Dialog Solutions for Xilinx ZUXX Family

Power Scheme	ZU19EG	ZU9EG	ZU9CG	ZU7EG	ZU5EG	ZU3EG(1)	ZU3EG(2)
Always On: Cost optimized		2xDA9210, DA9063	2xDA9210, DA9063	DA9213, DA9063	DA9210, DA9063	DA9210, DA9063	DA9210, DA9062
Always On: Power/Efficiency optimized		DA9213, DA9063 *	DA9213, DA9063 *	DA9214, DA9063	DA9214, DA9063	DA9063	
Always On: PL performance optimized		2xDA9210, DA9063	2xDA9210, DA9063	DA9213, DA9063	DA9210, DA9063	DA9210, DA9063	DA9210, DA9062
Full power management flexibility	DA9215, DA9063 *	DA9213, DA9063 *	DA9213, DA9063	DA9214, DA9063	DA9214, DA9063	DA9063	
* Additional single external regulator required							



# ZU3CG Example

Always On: Power/Efficiency optimized

Based on the ZU3CG Requirements we can map all of the required rails for the Always On: Power/Efficiency optimized solution on to a single DA9063.

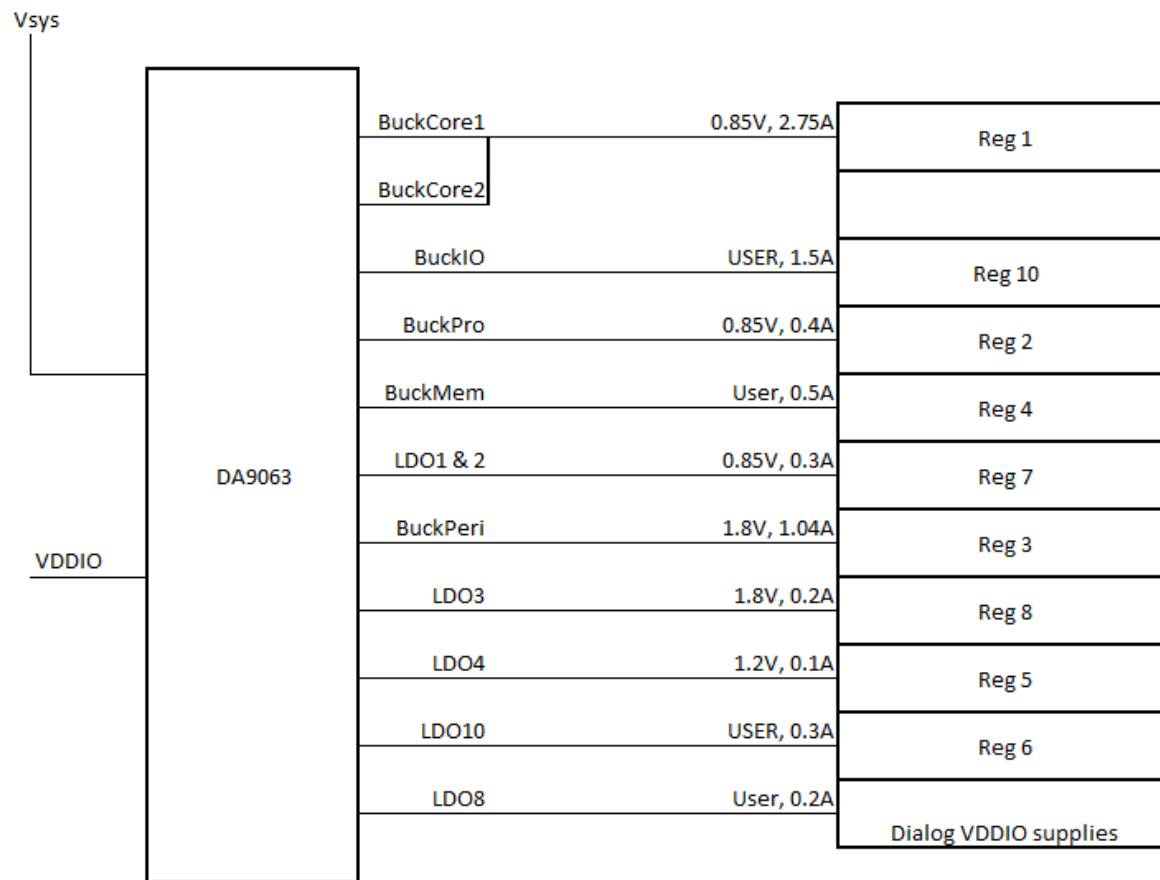
This mapping still leaves 6 LDO's available for additional system requirements.

The DA9063-EVAL8 evaluation kit is available to evaluate this configuration.

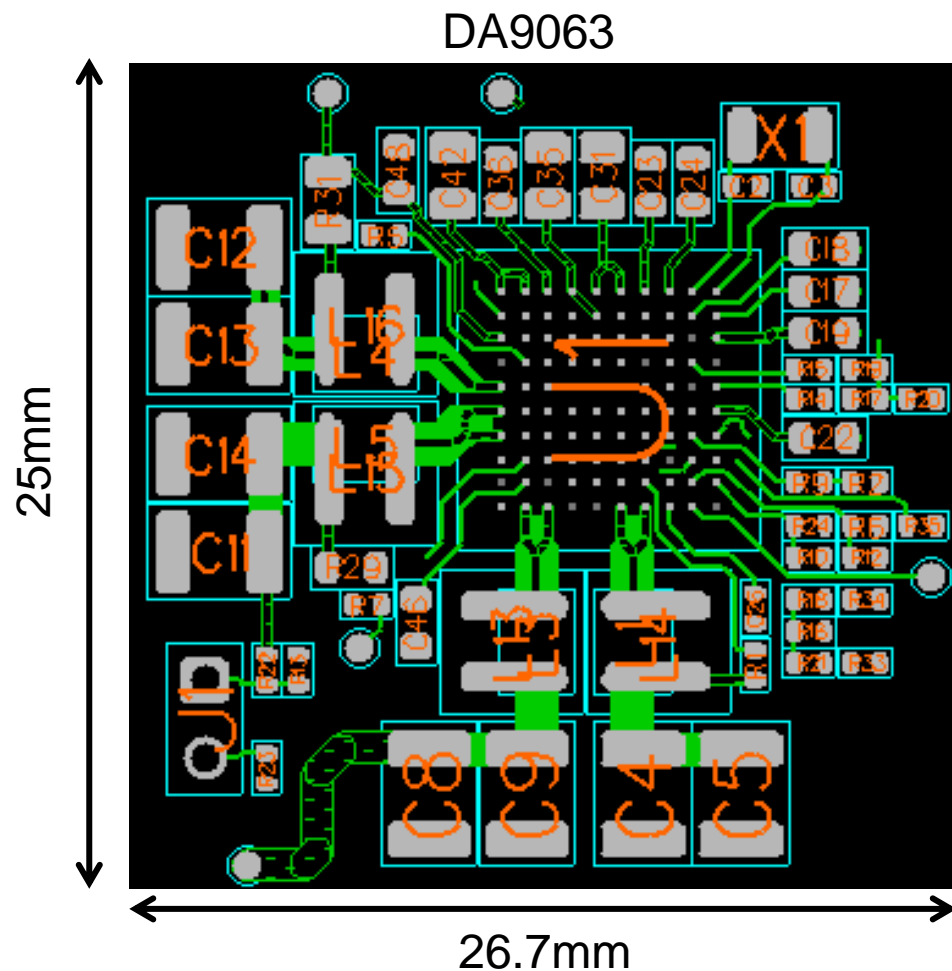
Always On: Power/Efficiency optimized					Dialog Mapping	
	Power Regulator	Possible Power Rail Consolidation	Voltage	Current	Resource	Current
Required	1	VCCINT,VCCINT_IO, VCCBRAM	0.85	4.6	Core1&2	5
	2	VCC_PSINTFP, VCC_PSINTLP, VCC_PSINTFP_DDR, , and VCCINT_VCU	0.85	2.55	Pro	2.5
	3	VCC_PSAUX, VCC_PSADC(1), VCC_PSDDR_PLL(2),VCC AUX, VCCAUX_IO, and VCCADC(1)	1.8	1.04	Peri	1.5
	4	VCCO_PSDDR	USER	0.5	Mem	1.5
	5	VCC_PSPLL, VMGTAVTT (GTH), and VMGTAVTT (GTY)	1.2	0.1	LDO4	0.2
	6	VCCO_PSIO[0:3] assuming all PS I/Os run from same voltage	USER	0.3	LDO10	0.3
User-Defined	7	VPS_MGTRAVCC	0.85	0.3	LDO1&2	0.1+0.2
	8	VPS_MGTRAVTT, VMGTVCCAUX (GTH), and VMGTVCCAUX (GTY)	1.8	0.1	LDO3	0.2
	9	VMGTAVCC (GTH) and VMGTAVCC (GTY)	0.9	0		
	10	Optional PL and PS I/O voltages	USER	1	IO	1.5

# ZU3CG Example

Always On: Power/Efficiency optimized



# ZU3CG: PCB area



Note: in this layout the DA9063 has input decoupling in the reverse side of the board.

# ZU3CG Example

The DA9063-EVAL8 evaluation kit is available to evaluate this configuration.  
See the Dialog Website for further details of the DA9063 and the evaluation boards.

DA9063 Performance Board Merged Buck Core 1&2

ZIP



# ZU9EG

## Full power management flexibility

To Support the Fully Flexible solution for the ZU9EG requires the use of a DA9213 to supply the high current VCCINT rail, along with the DA9063. In addition a single external regulator will be required for Reg 13. This can be scaled dependant on the end system requirements and utilisation of the Gigabit interfaces

Full power management flexibility					Dialog Mapping	
	Power Regulator	Possible Power Rail Consolidation	Voltage	Current	Resource	Current
Required	1	VCC_PSINTLP	0.85	0.4	Pro	2.5
	2	VCC_PSAUX, VCC_PSADC(1)	1.8	0.12	LDO3	0.2
	3	VCC_PSPLL,	1.2	0.1	LDO4	0.2
	4	VCCO_PSIO[0:3] assuming all PS I/Os run from same voltage	USER	0.3	LDO10	0.3
	5	VCC_PSINTFP, VCC_PSINTFP_DDR,	0.85	2.75	Core1	2.5
	6	VCC_PSDDR_PLL(2)	1.8	0.1	LDO5	0.1
	7	VCCO_PSDDR	USER	0.5	Mem	1.5
	8	VCCINT, VCCINT_IO, VCCBRAM	0.85	20.8	DA9213	20
	9	VCCAUX, VCCAUX_IO, and VCCADC(1)	1.8	1.12	Peri	1.5
User-Defined	10	VPS_MGTRAVCC	0.85	0.3	LDO1&2	0.1+0.2
	11	VPS_MGTRAVTT	1.8	0.1	LDO6	0.2
	12	VMGTAVTT (GTH), VMGTAVTT (GTY), and VCC_VCU_PLL	1.2	2	Core2	2.5
	13	VMGTAVCC (GTH) and VMGTAVCC (GTY)	0.9	2	External	
	14	VMGTVCCAUX (GTH), and VMGTVCCAUX (GTY)	1.8	0.1	LDO7	0.2
	15	Optional PL and PS I/O voltages	USER	1.5	IO	1.5
Spare					LDO8,9,11	

# ZU9EG

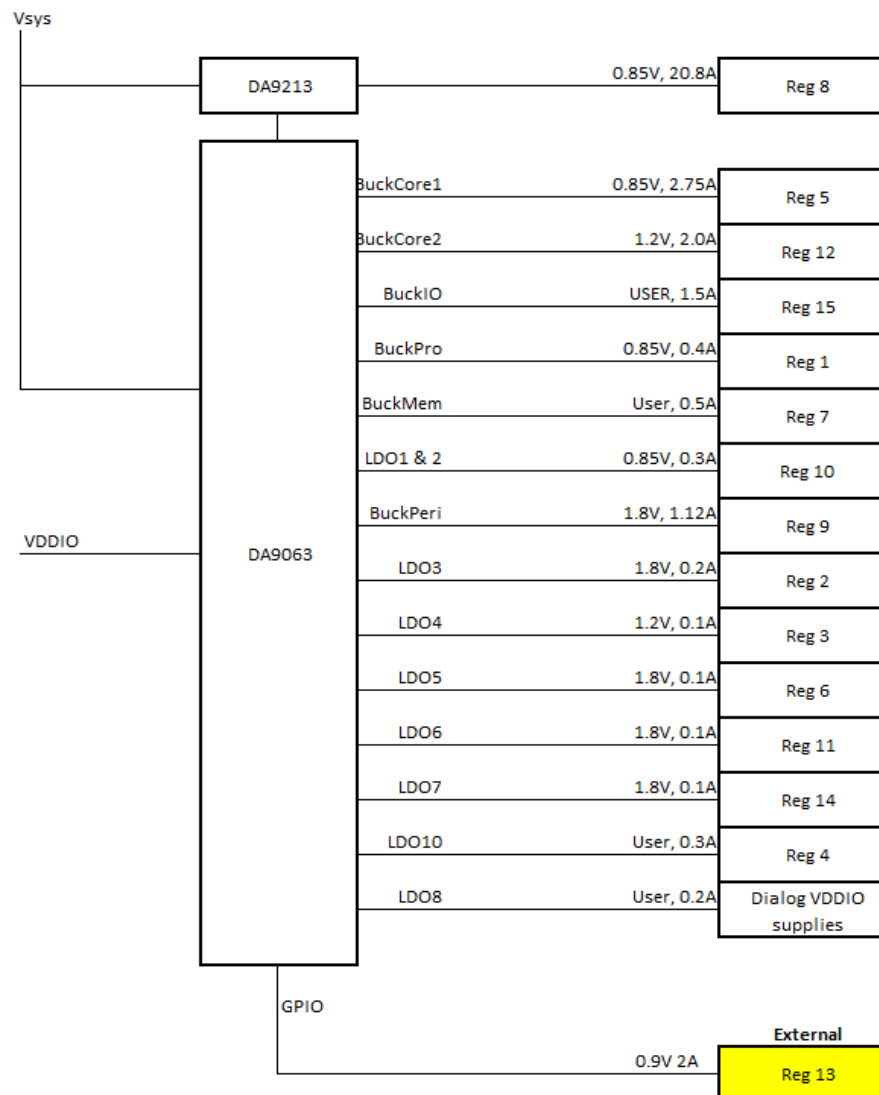
## Full power management flexibility

The DA9063 provides control of both the DA9213 and the external regulator via its sequence-able GPIO.

Currently in development is a Power Board for this solution.

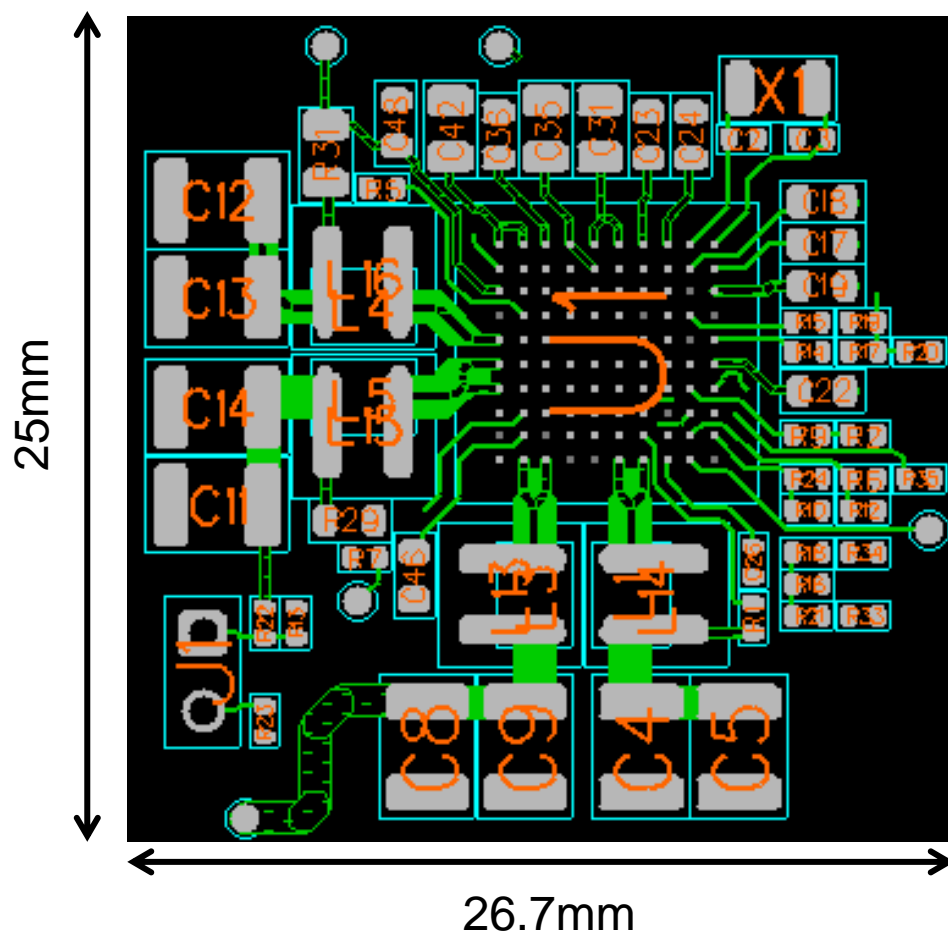
Schematics and BOM will be available during early Feb. 2017

Layout will be available by the end of Feb and actual boards will be available during March.

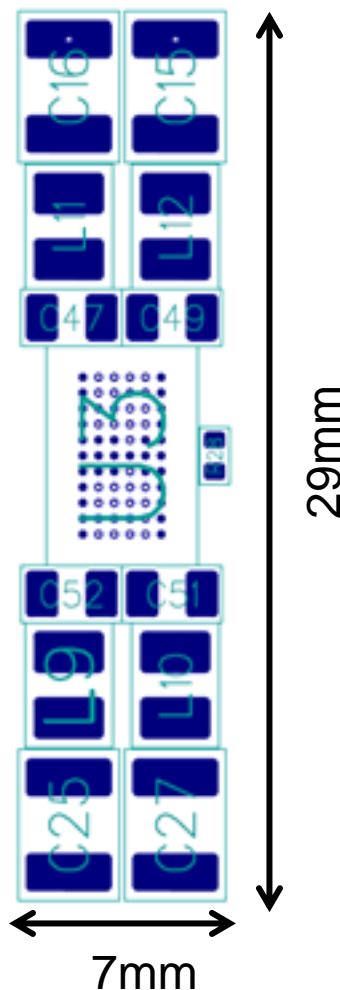


# ZU9EG

ZU9EG solution : Automotive components  
DA9063



DA9213



This layout example provides an indication of the area required for the ZU9 solution including the DA9063 and the DA9213. This example uses Automotive qualified components, the overall area could be further optimised if consumer grade parts were used.

Note: in this layout the DA9063 has input decoupling in the reverse side of the board.

# ZU19EG

## Full power management flexibility

The final example demonstrates how we can extend this flexible solution with the addition of a single external High current regulator to address the requirements of the ZU19.

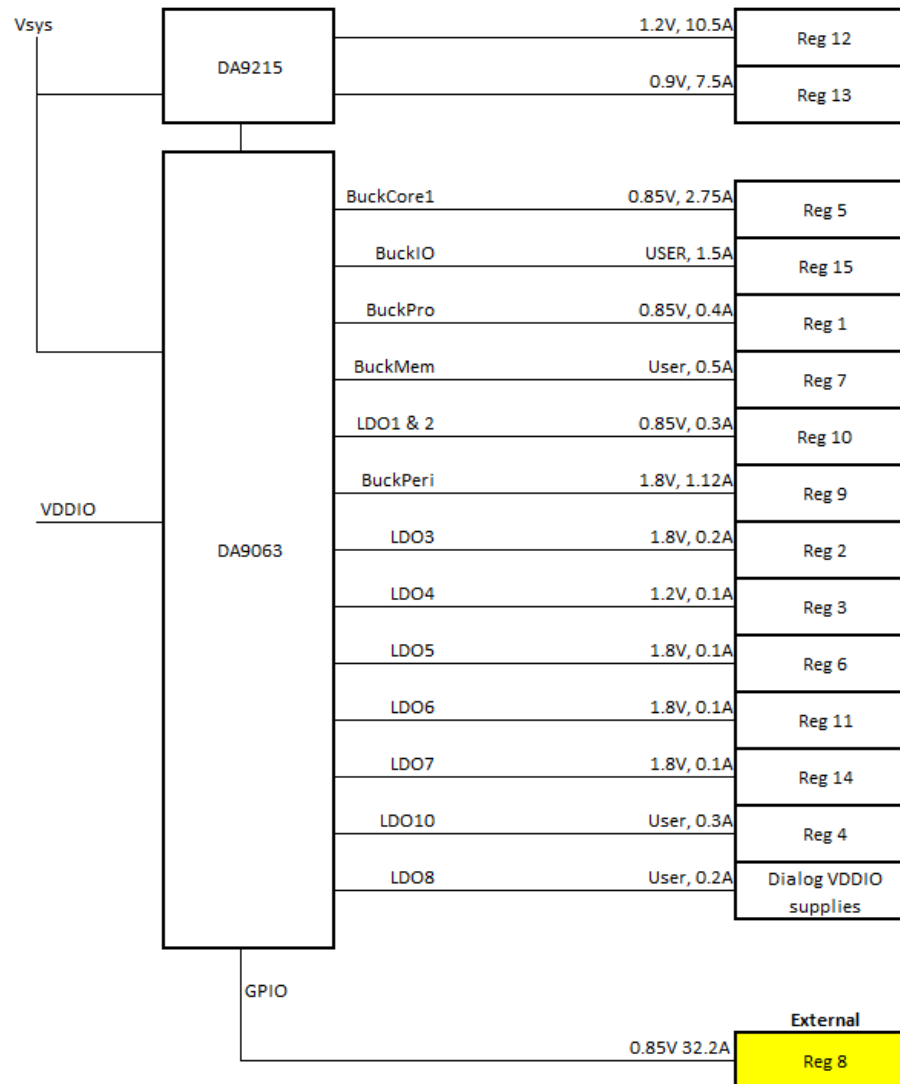
This solution uses a DA9215 to provide two 10A rails for regulators 12 & 13 along with a DA9063 as the main system PMIC and the previously mentioned high current single regulator.

Full power management flexibility					Dialog Mapping	
	Power Regulator	Possible Power Rail Consolidation	Voltage	Current	Resource	Current
Required	1	VCC_PSINTLP	0.85	0.4	Pro	2.5
	2	VCC_PSAUX, VCC_PSADC(1)	1.8	0.12	LDO3	0.2
	3	VCC_PSPLL,	1.2	0.1	LDO4	0.2
	4	VCCO_PSIO[0:3] assuming all PS I/Os run from same voltage	USER	0.3	LDO10	0.3
	5	VCC_PSINTFP, VCC_PSINTFP_DDR,	0.85	2.75	Core1	2.5
	6	VCC_PSDDR_PLL(2)	1.8	0.1	LDO5	0.1
	7	VCCO_PSDDR	USER	0.5	Mem	1.5
	8	VCCINT, VCCINT_IO, VCCBRAM	0.85	32.2	External	
	9	VCCAUX, VCCAUX_IO, and VCCADC(1)	1.8	1.82	Peri	1.5
User-Defined	10	VPS_MGTRAVCC	0.85	0.3	LDO1&2	0.1+0.2
	11	VPS_MGTRAVTT	1.8	0.1	LDO6	0.2
	12	VMGTAVTT (GTH), VMGTYAVTT (GTY), and VCC_VCU_PLL	1.2	10.5	DA9215	10
	13	VMGTAVCC (GTH) and VMGTYAVCC (GTY)	0.9	7.5	DA9215	10
	14	VMGTVCCAUX (GTH), and VMGTYVCCAUX (GTY)	1.8	0.3	LDO7	0.2
	15	Optional PL and PS I/O voltages	USER	1.5	IO	1.5
Spare					LDO8,9,11	



# ZU19EG

## Full power management flexibility



## More Information

For more information about the range of Dialog Semiconductor PMICs and Sub-PMICs

See the Dialog Website <http://www.dialog-semiconductor.com/>

Or Contact your local Dialog Field Applications team for direct support.

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