To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

RENESAS

H8/36077 Group

Determining the Reset Sources

Introduction

There are four types of reset sources for the H8/36077: the power-on reset, the LVD (low voltage detection) reset, the external signal reset, and the WDT reset. By reading the Reset Source Determination Register (LVDRF) after a reset is cleared, the source of the reset can be determined.

Target Device

H8/36077Group MCU

Contents

1. Specifications

1. The connection diagram of the microcomputer for this sample task is shown in figure 1.
2. The H8/36077 uses the internal power-on reset circuit to perform a power-on reset.
   - By connecting an external capacitor, an internal reset signal is generated when the power is turned on.
   - To determine the source of the reset after it is cleared, the value of the LVDRF (H'02) register is serially output to the PC.
3. The H8/36077 incorporates the internal low-voltage detection circuit (LVDR) to generate a reset when the voltage decreases (3.6 V (typical) is set as the voltage to be detected as the low voltage).
   - When the power supply voltage becomes 3.6 V or lower, an internal reset signal is generated.
   - When the voltage becomes greater than 3.6 V during the low-voltage reset state, prescaler S (PSS) starts counting up. When 131,072 states elapse, the internal reset signal is canceled.
   - To determine the source of the reset, the value of the LVDRF register (H'02) is serially output to the PC.
4. The H8/36077 has the watchdog timer (WDT) for watchdog operation.
   - After the power-on reset is cleared, timer counter WD (TCWD) starts counting up.
   - When the count value of TCWD overflows, an internal reset signal is generated.
   - After the reset state is released, the value of the LVDRF register (H'01) is serially output to the PC.
5. When a reset signal $\overline{\text{RES}}$ is input to the external reset pin the H8/36077 conducts an external reset operation.
   - When the $\overline{\text{RES}}$ signal is driven low, the reset state is entered.
   - When the $\overline{\text{RES}}$ signal remains at a low level for a specified length of time and then goes to a high level, the reset is cleared.
   - To determine the source of the reset, the value of the LVDRF register (H'00) is serially output to the PC.

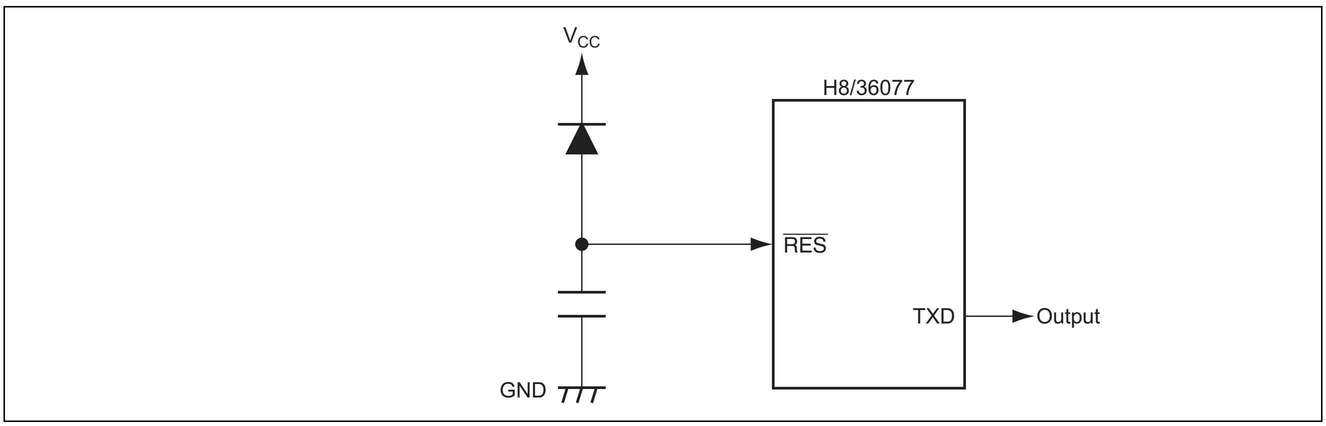


Figure 1 Connection Diagram of the H8/36077

6. The flow of performing different types of reset in this sample task is as follows. Table 1 shows how the source of a reset is determined.
   - First, a power-on reset is performed. Secondly, the program checks that the value of LVDRF is H'02. Continue execution of the program to perform a watchdog operation. After the WDT reset is cleared, the program checks that the value of LVDRF is H'01.
   - Next, an external reset signal is input and an external reset is performed. The program then checks that the value of LVDRF is H'00.
   - Finally, a low-voltage detection reset is conducted. The power supply voltage is lowered to 3.6 V. Then the power supply voltage is again returned to 5.0 V. The program then checks that the value of LVDRF is H'02.

Table 1 Determining the Source of a Reset

LVDRF Register		
PRST (Bit 1)	**WRST (Bit 0)**	**Source of Reset**
1	0	Power-on or LVDR (low voltage detection)
0	0	Reset signal $\overline{\text{RES}}$ input to the external reset pin
0	1	WDT (watchdog timer)

Note: Bits 7 to 2 are reserved.

2. Description of Functions Used

2.1 Functions Used

1. In this sample task, the internal power-on reset circuit and the low-voltage detection circuit (LVDR) of the H8/36077 are used to perform a power-on reset and a low-voltage reset. Figure 2 shows the block diagram of the internal power-on reset circuit and the low-voltage detection circuit. This section describes the details on the internal power-on reset circuit and the low-voltage detection circuit.
   - System clock (ϕ)
     The basic clock for operating the CPU and peripheral modules.
   - Prescaler S (PSS)
     A 13-bit counter that uses the system clock (ϕ) as the source. Prescaler S is incremented for each cycle.
   - Low-Voltage Detection Control Register (LVDCR)
     This register is for controlling the low-voltage detection circuit. In this sample task, the low-voltage detection circuit is used to set 3.6 V as the reset detection voltage.

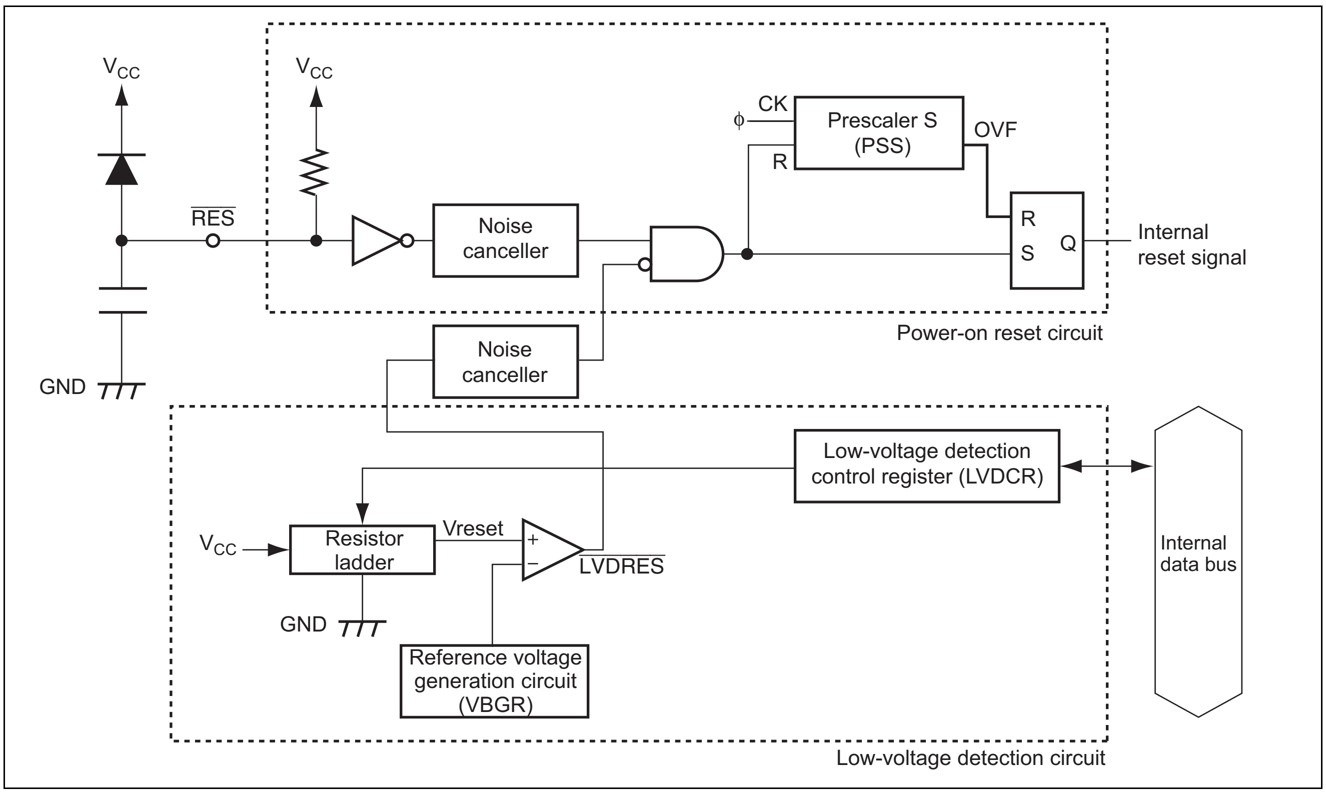


Figure 2 Block Diagrams of the Power-On Reset Circuit and the Low-Voltage Detection Circuit

2. In this sample task, the watchdog timer (WDT) function is used to perform a watchdog operation. Figure 3 shows the block diagram of the watchdog timer. The following describes the details on the watchdog timer.
   - System clock (ϕ)
     A 10-MHz clock used as the basis for operating the CPU and peripheral modules.
   - Prescaler S (PSS)
     A 13-bit counter that uses the system clock (ϕ) as the source. Prescaler S is incremented for each cycle.
   - Timer Control/Status Register WD (TCSRWD)
     An 8-bit readable/writable register. This register controls the writes to TCSRWD itself and TCWD (timer counter for the watchdog timer). TCSRWD also controls the watchdog timer operation and indicates the operating state of the watchdog timer. The watchdog timer is enabled from the initial state and starts when a reset is cleared.
   - Timer Counter WD (TCWD)
     An 8-bit readable/writable up-counter. The counter is incremented based on the clock input of ϕ/8192.
   - Timer Mode Register WD (TMWD)
     Selects an input clock. In this sample task, the input clock is ϕ/8192.

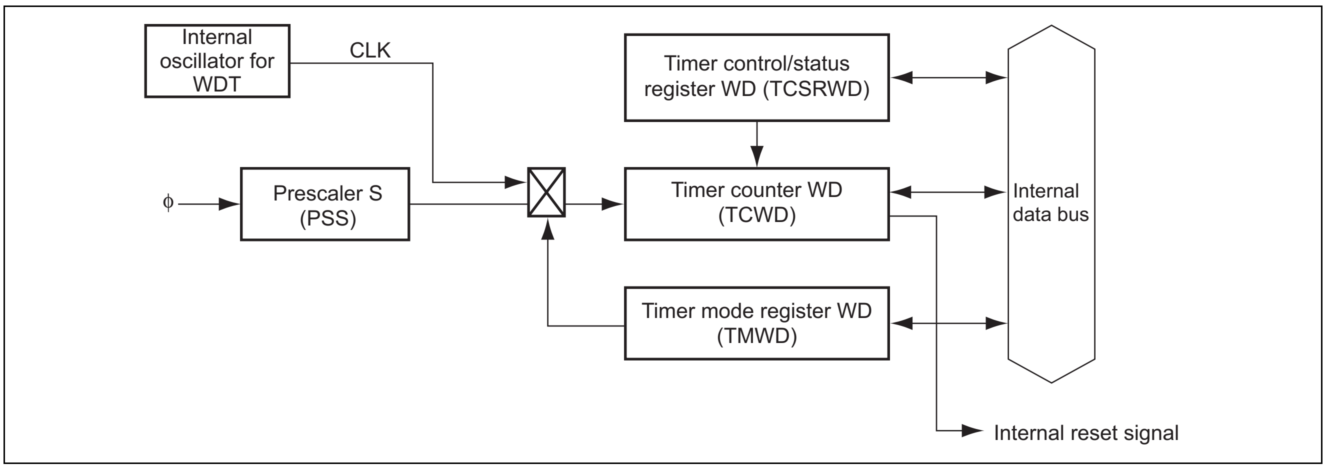


Figure 3 Block Diagram of the Watchdog Timer

2.2 Function Assignment

Table 2 shows the assignment of functions in this sample task. Functions are assigned as shown in table 2 to perform each type of reset operation.

Table 2 Assignment of Functions

Elements	Description
TCSRWD	Stops the watchdog timer.
LVDRF	LVDRF is read after a reset is cleared to determine the source of the reset.
LVDCR	Setting of the low-voltage detection circuit.
SSR	Status flag that indicates the operating state of the SCI3 (serial communication interface 3)
SMR	Sets the asynchronous mode as the communication mode and selects the clock source for the SCI3.
BRR	Sets the communication bit rate to 9600 bps.
SCR3	Enables data transmission.
PMR1	TXD output pin setting.

3. Principles of Operation

1. The operation of the power-on reset circuit is shown in figure 4. When a power-on reset is generated, the LVDRF register is read after the reset is cleared and the source of the reset is determined through the hardware and software processing described in figure 4.

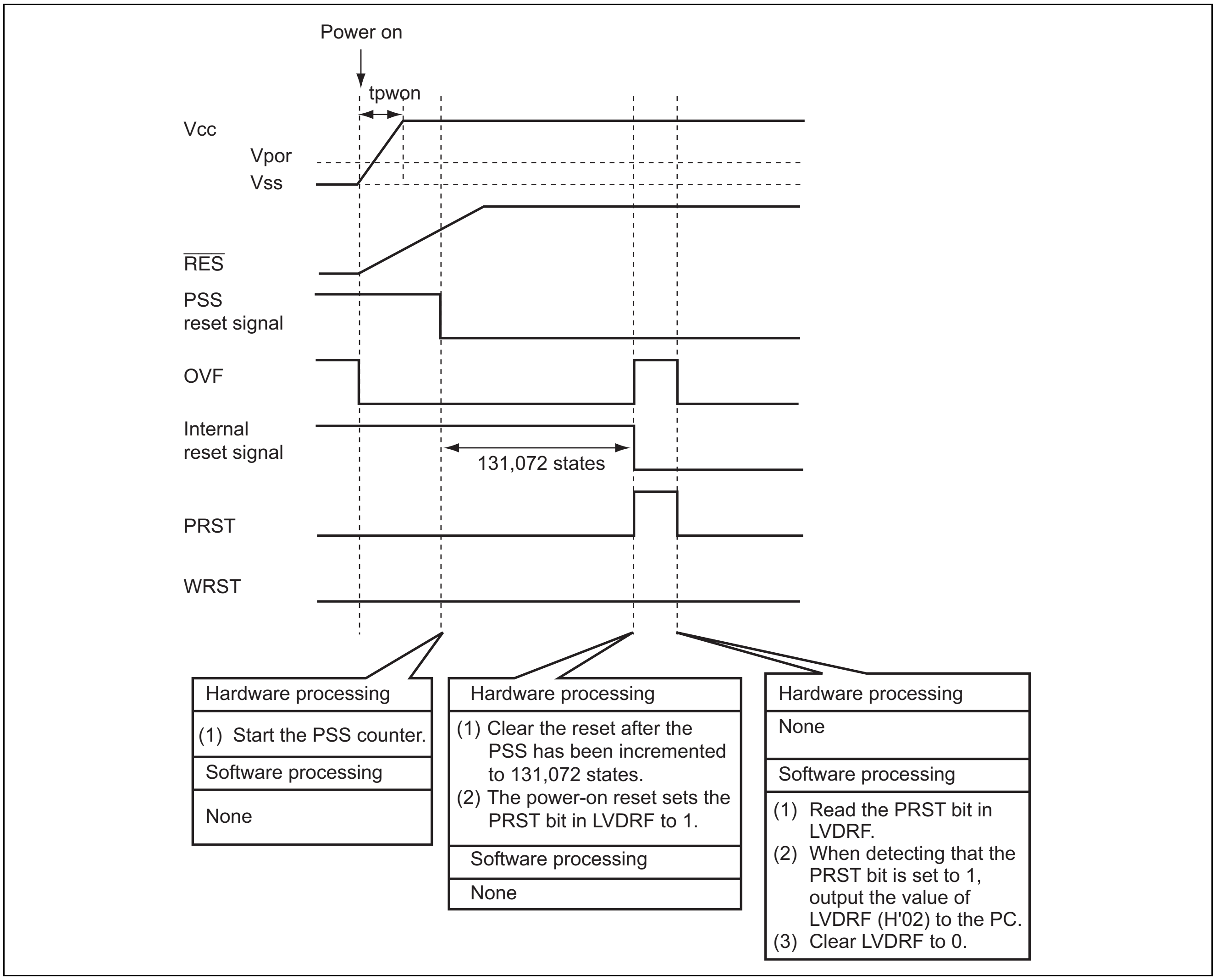


Figure 4 Operation of the Power-On Reset Circuit

2. The operation of the low-voltage detection reset (LVDR) circuit is shown in figure 5. When an LVDR is generated, the LVDRF register is read after the LVDR is cleared and the source of the reset is determined through the hardware and software processing described in figure 5.

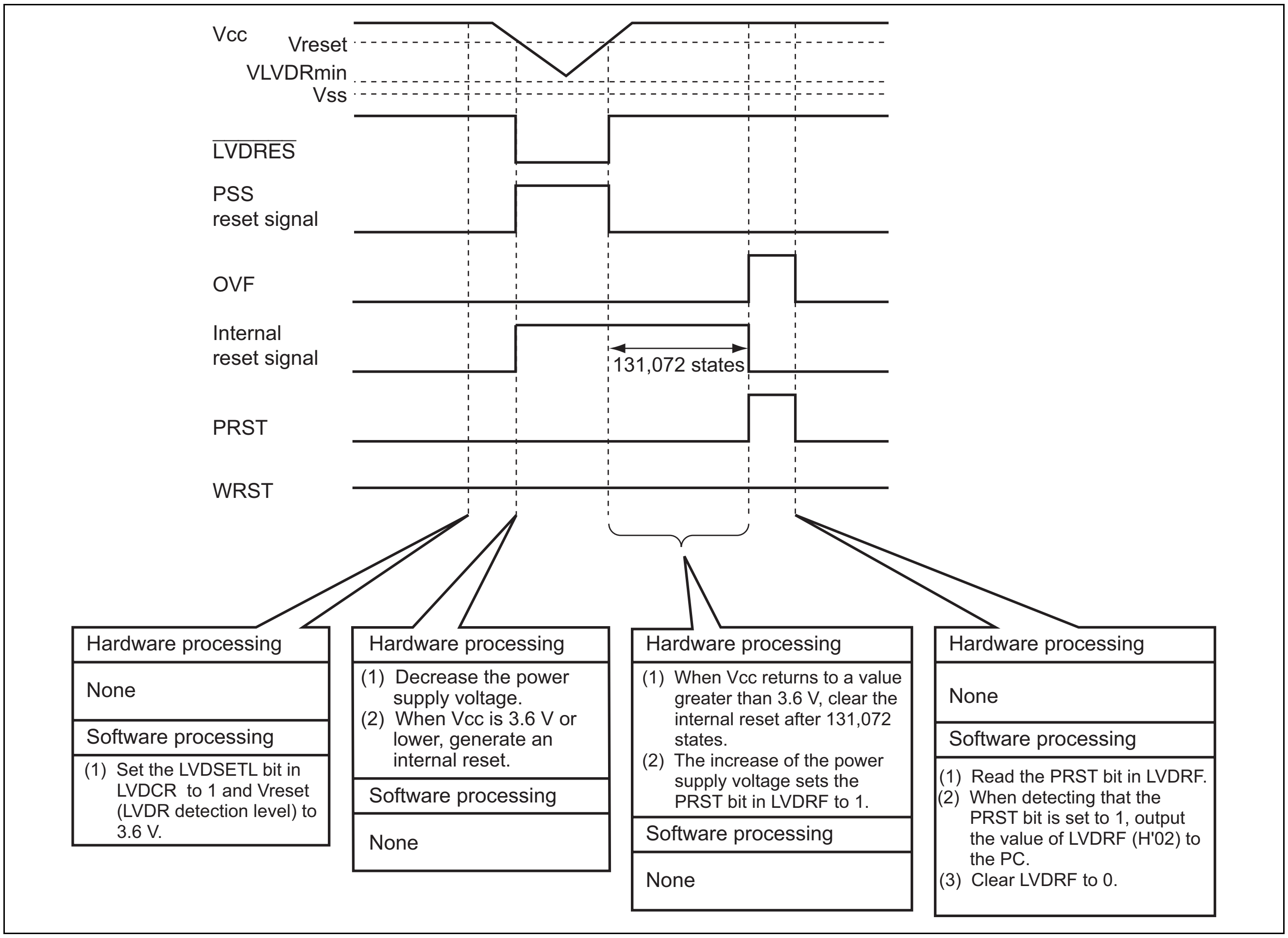


Figure 5 Operation of the Low-Voltage Detection Reset Circuit

3. The operation of the watchdog timer (WDT) reset is shown in figure 6. The CPU enables the watchdog timer from the initial state. In this sample task, the watchdog timer is enabled to generate a WDT reset. As shown in figure 6, when a WDT reset is generated, the LVDRF register is read after the reset is cleared and the source of the reset is determined.

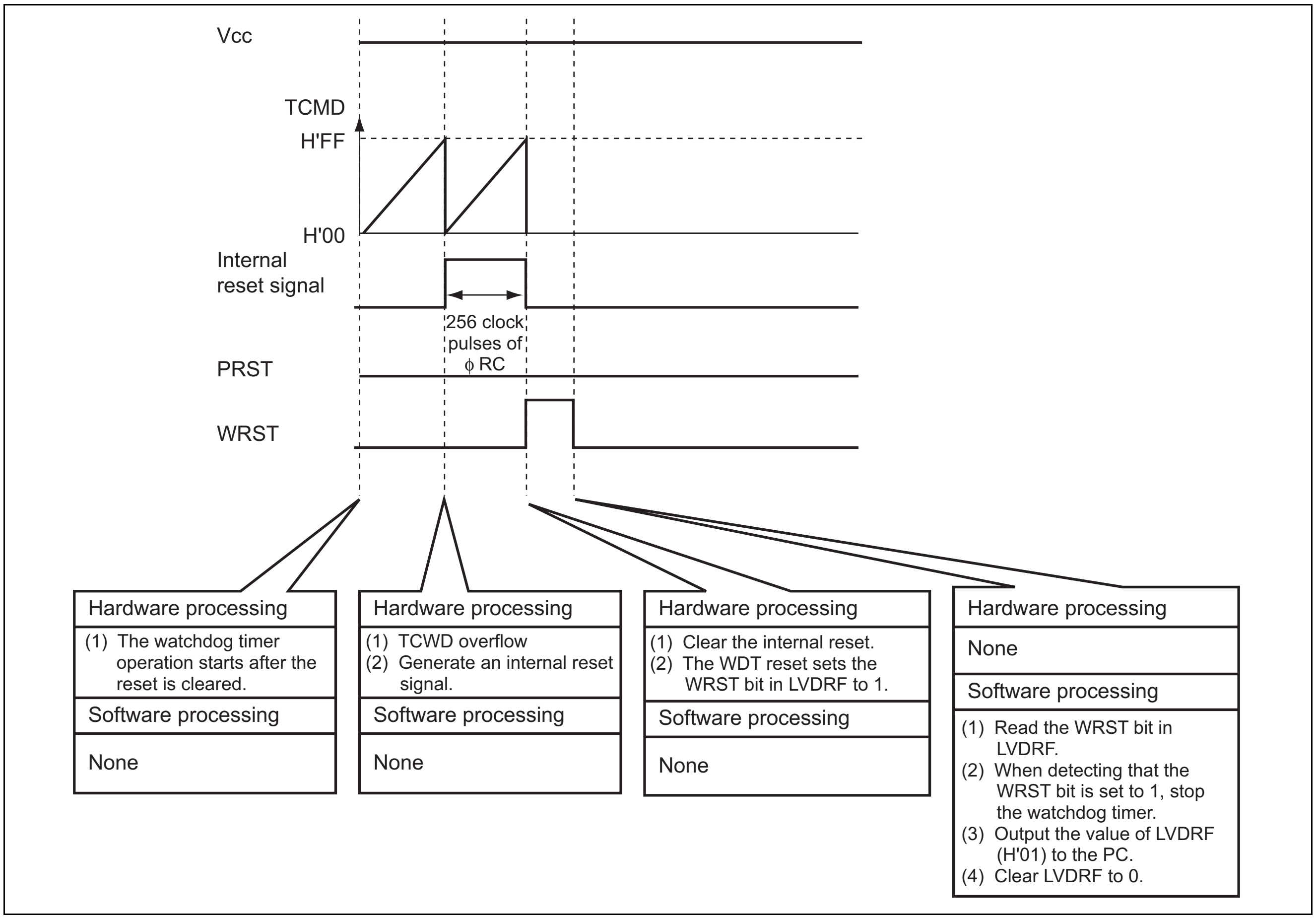


Figure 6 Operation of a Watchdog Timer Reset

4. The operation of an external reset is shown in figure 7. When a reset signal is input to the external reset pin $\overline{RES}$, the LVDRF register is read after the reset is cleared and the source of the reset is determined through the hardware and software processing described in figure 7.

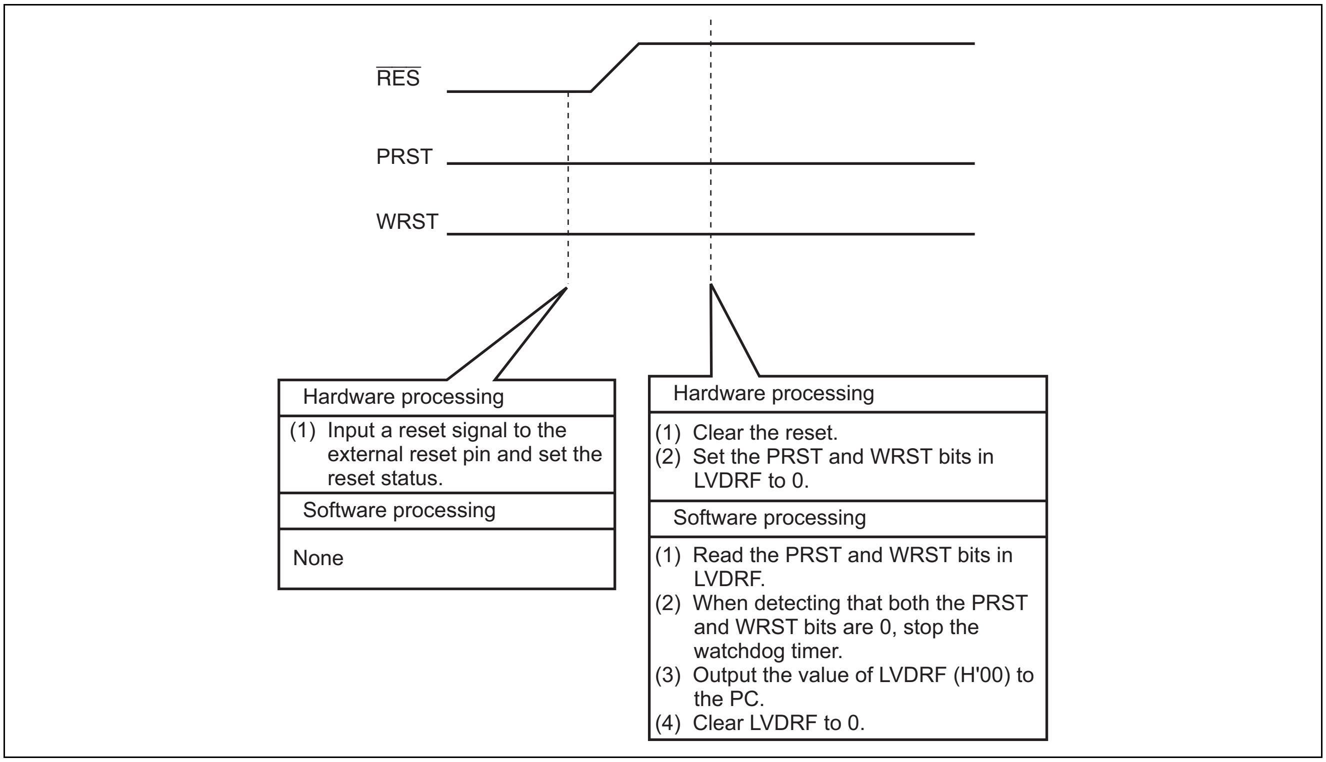


Figure 7 Operation of a Reset by the External Reset Pin $\overline{RES}$

4. Description of Software

4.1 Description of Modules

Table 3 shows the modules used in this sample task.

Table 3 Description of Modules

Function Name	Description
main	Initializes the SCI3, sets the low-voltage detection circuit, reads the LVDRF register, determines the source of the generated reset, and outputs the result to the PC.
sci_init	Initializes the SCI3.
sci_print_hex_byte	Converts the acquired data to one-byte hexadecimal data and outputs it to the PC.
sci_write	Sends data via the SCI3.

4.2 Description of Arguments

Table 4 describes the arguments used in this sample task.

Table 4 Description of Arguments Used

Label Name	Description	Data Length	Used In	Input/Output
d	Transmit data	1 byte	sci_write	Input
data	Hexadecimal data to be output to the PC	1 byte	sci_print_hex_byte	Input

4.3 Description of Internal Registers Used

The following tables describe the internal registers used in this sample task.

- Low-Voltage Detection Control Register (LVDCR) Address: H'F730

Bit	Bit Name	Setting Value	R/W	Function
5	VDDII	1	R/W	LVDI External Comparison Voltage Input Disable 0: Uses the external voltage as the LVDI comparison voltage. 1: Uses the internal voltage as the LVDI comparison voltage.
3	LVDSEL	1	R/W	LVDR Detection Level Select 0: 2.3 V (typical) as the reset detection voltage 1: 3.6 V (typical) as the reset detection voltage For reset detection, use 3.6 V (typical).
1	LVDDE	0	R	Voltage Decrease Interrupt Enable 0: Disables an interrupt request when the voltage decreases. 1: Enables an interrupt request when the voltage decreases.
0	LVDUE	0	R	Voltage Increase Interrupt Enable 0: Disables an interrupt request when the voltage increases. 1: Enables an interrupt request when the voltage increases.

- Reset Source Determination Register (LVDRF) Address: H'F732

Bit	Bit Name	Setting Value	R/W	Function
1	PRST	*	R/W	POR/LVDR Detect [Setting condition] • When a power-on reset or an LVDR reset is generated [Clearing condition] • When 0 is written
0	WRST	*	R/W	WDT Reset Detect [Setting condition] • When a reset is generated by the WDT [Clearing condition] • When a power-on reset, an LVDR reset, or a reset by the external reset signal is generated, or 0 is written

- Timer Control/Status Rregister WD (TCSRWD) Address: H'FFC0

Bit	Bit Name	Setting Value	R/W	Function
7	B6WI	1	R/W	Bit 6 Write Disable The TCWE bit can be written to only when 0 is written to the B6WI bit. This bit is always read as 1.
6	TCWE	0	R/W	Timer Counter WD Write Enable TCWD (timer counter WD) can be written when the TCWE bit is set to 1. To write a value to this bit, the value of bit 7 (B6WI) must be 0.
5	B4WI	0 or 1	R/W	Bit 4 Write Disable The TCSRWE bit can be written to only when the 0 is written to the B4WI bit. This bit is always read as 1.
4	TCSRWE	1	R/W	Timer Control/Status Register WD Write Enable The WDON and WRST bits can be written to when this TCSRWE bit is set to 1. When writing to this bit, 0 must be written to bit 5 (B4WI).
3	B2WI	1 or 0	R/W	Bit 2 Write Disable The WDON bit can be written to only when 0 is written to this B2WI bit. This bit is always read as 1.
2	WDON	1 or 0	R/W	Watchdog Timer On TCWD (timer counter WD) starts counting up when WDON is set to 1 and halts when WDON is cleared to 0. In the initial state, the watchdog timer is enabled. If you do not use the watchdog timer, clear this bit to 0. [Clearing condition] • When 0 is written to B2WI and WDON while TCSRWE = 1 [Setting conditions] • Reset • When 0 is written to B2WI and 1 is written to WDON while TCSRWE = 1
1	B0WI	1	R/W	Bit 0 Write Disable The WRST bit can be written to only when 0 is written to this B0WI bit. This bit is always read as 1.
0	WRST	0	R/W	Watchdog Timer Reset [Clearing conditions] • Reset by the external reset signal $\overline{RES}$ input • When 0 is written to B2WI and WDON while TCSRWE = 1 [Setting condition] • When TCWD (timer counter WD) overflows and an internal reset signal is generated

- Timer Counter WD (TCWD) Address: H'FFC1

Function: An 8-bit readable/writable up-counter. When TCWD overflows from H'FF to H'00, an internal reset signal is generated and the WRST bit of TCSRWD is set to 1. The initial value of TCWD is H'00.

Setting value: H'00

- Timer Mode Register WD (TMWD) Address: H'FFC2

Bit	Bit Name	Setting Value	R/W	Function
3	CKS3	1	R/W	Clock Select 3 to 0
2	CKS2	1	R/W	Select the clock to be input to TCWD (timer counter WD).
1	CKS1	1	R/W	1111: Internal clock: counts on Φ/8192
0	CKS0	1	R/W	

- Transmit Shift Register (TSR)

Function: A shift register for sending serial data. To perform serial data transmission, the SCI3 first transfers transmit data from the TDR register to the TSR register automatically, then sends the data starting from the LSB to the TXD pin. The CPU cannot directly access this register.

- Transmit Data Register (TDR) Address: H'FFAB

Function: An 8-bit register for storing transmit data. When the SCI3 detects that the TSR register is empty, it transfers the transmit data written in the TDR register to the TSR register and starts transmission. The double-buffered structure of TDR and TSR enables continuous serial transmission. If the next portion of transmit data is already written to TDR during transmission of one-frame data, the SCI3 transfers the written data to TSR to continue transmission. To achieve reliable serial transmission, write transmit data to TDR only once after confirming that the TDRE bit of SSR is set to 1. The initial value of TDR is H'FF.

Setting value: H'xx

- Serial Mode Register (SMR) Address: H'FFA8

Bit	Bit Name	Setting Value	R/W	Function
7	COM	0	R/W	Communication Mode 0: Asynchronous mode 1: Clock synchronous mode
6	CHR	0	R/W	Character Length (available in the asynchronous mode only) 0: Data is sent and received in units of 8 bits. 1: Data is sent and received in units of 7 bits.
5	PE	0	R/W	Parity Enable (available in the asynchronous mode only) When this bit is set to 1, a parity bit is added for transmission and a parity check is performed for reception.
4	PM	0	R/W	Parity Mode (available in the asynchronous mode only when PE = 1) 0: Data is sent and received using even parity. 1: Data is sent and received using odd parity.
3	STOP	0	R/W	Stop Bit Length (available in the asynchronous mode only) Selects the length of the stop bit for transmission. 0: One stop bit 1: Two stop bits For reception, only the first bit of the stop bits is checked regardless of the setting of this bit. When the second bit is 0, it is assumed to be the start bit of the next character is sent.
2	MP	0	R/W	Multiprocessor Mode When this bit is set to 1, the multiprocessor communication functions is enabled. The settings of the PE and PM bits are invalid. Set this bit to 0 in the clock synchronous mode.
1 0	CKS1 CKS0	All 0	R/W	Clock Select 1 and 0 Select the clock source of the internal baud rate generator. 00: ϕ clock (n = 0)

- Serial Control Register 3 (SCR3) Address: H'FFAA

Bit	Bit Name	Setting Value	R/W	Function
7	TIE	0	R/W	Transmit Interrupt Enable Setting this bit to 1 enables TXI interrupt requests.
6	RIE	0	R/W	Receive Interrupt Enable Setting this bit to 1 enables RXI and ERI interrupt requests.
5	TE	1	R/W	Transmit Enable Setting this bit to 1 enables transmission.
4	RE	1	R/W	Receive Enable Setting this bit to 1 enables reception.
3	MPIE	0	R/W	Multiprocessor Interrupt Enable (available in the asynchronous mode when the MP bit of SRM is 1)
2	TEIE	0	R/W	Transmit End Interrupt Enable Setting this bit to 1 enables TEI interrupt requests.
1 0	CKE1 CKE0	All 0	R/W	Clock Enable 1 and 0 Select the clock source. 00: Internal baud rate generator

- Serial Status Register (SSR) Address: H'FFAC

Bit	Bit Name	Setting Value	R/W	Function
7	TDRE	x	R/W	Transmit Data Register Empty Indicates whether TDR contains transmit data. [Setting conditions] • When the TE bit in SCR3 is 0 • When data is transferred from TDR to TSR [Clearing conditions] • When 1 is read from TDRE then 0 is written to it • When transmit data is written to TDR
6	RDRF	0	R/W	Receive Data Register Full Indicates whether received data is stored in RDR. [Setting condition] • When reception ends normally and the received data is transferred from RSR to RDR [Clearing conditions] • When 1 is read from RDRF then 0 is written to it • When data is read from RDR
5	OER	0	R/W	Overrun Error [Setting condition] • If an overrun error occurs during reception [Clearing condition] • When 1 is read from OER then 0 is written to it
4	FER	0	R/W	Framing Error [Setting condition] • If a framing error occurs during reception [Clearing condition] • When 1 is read from FER then 0 is written to it
3	PER	0	R/W	Parity Error [Setting condition] • If a parity error occurs during reception [Clearing condition] • When 1 is read from PER then 0 is written to it
2	TEND	x	R	Transmit End [Setting conditions] • When the TE bit in SCR3 is 0 • When the TDRE bit is 1 when the last bit in the transmit character data is sent [Clearing conditions] • When 1 is read from the TDRE flag then 0 is written to it • When transmit data is written to TDR
1	MPBR	0	R	Multiprocessor Bit Receive Stores the multiprocessor bit in the received character data. The state of this bit is retained when the RE bit of SCR3 is 0.
0	MPBT	0	R/W	Multiprocessor Bit Transfer Stores the multiprocessor bit to be added to the transmit character.

- Bit Rate Register (BRR) Address: H'FFA9

  Function: An 8-bit register that sets the bit rate. The initial value of BRR is H'FF.
  Setting value: H'1F

- Port Mode Register 1 (PMR1) Address: H'FFE0

Bit	Bit Name	Setting Value	R/W	Function
7	IRQ3	0	R/W	Selects the function of the P17/$\overline{\text{IRQ3}}$/TRGV pin. 0: General I/O port 1: $\overline{\text{IRQ3}}$/TRGV input pin
6	IRQ2	0	R/W	Selects the function of the P16/$\overline{\text{IRQ2}}$ pin. 0: General I/O port 1: $\overline{\text{IRQ2}}$ input pin
5	IRQ1	0	R/W	Selects the function of the P15/$\overline{\text{IRQ1}}$/TMIB1 pin. 0: General I/O port 1: $\overline{\text{IRQ1}}$/TMIB1 input pin
4	IRQ0	0	R/W	Selects the function of the P14/$\overline{\text{IRQ0}}$ pin. 0: General I/O port 1: $\overline{\text{IRQ0}}$ input pin
3	TXD2	1	R/W	Selects the function of the P72/TXD_2 pin. 0: General I/O port 1: TXD_2 output pin
2	PWM	1	R/W	Selects the function of the P11/PWM pin. 0: General I/O port 1: PWM output pin
1	TXD	1	R/W	Selects the function of the P22/TXD pin. 0: General I/O port 1: TXD output pin
0	TMOW	0	R/W	Selects the function of the P10/TMOW pin. 0: General I/O port 1: TMOW output pin

4.4 RAM Usage

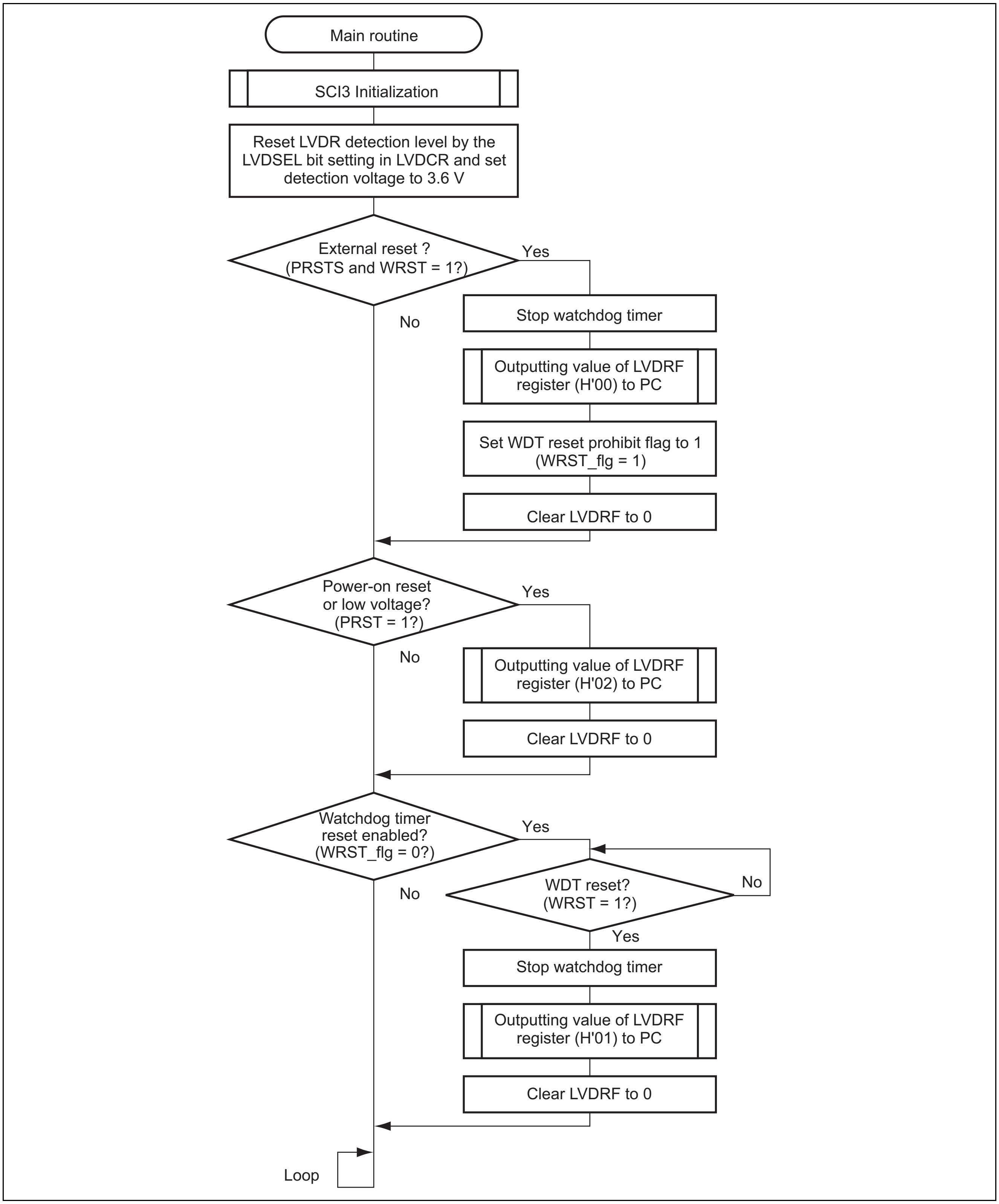
Table 5 shows the description of the RAM used in this sample task.

Table 5 RAM Usage

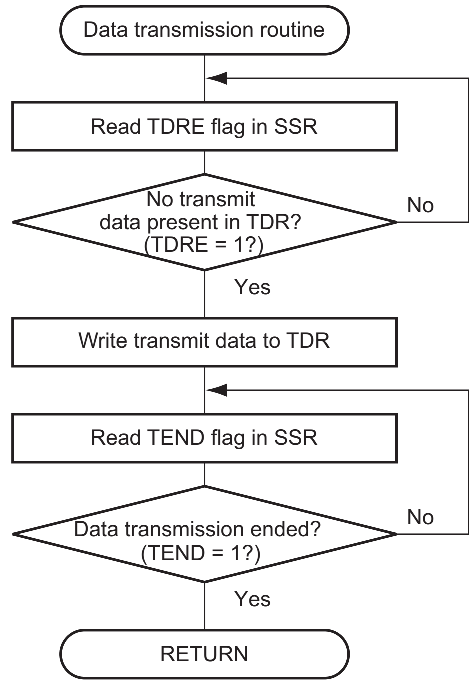
Label Name	Description	Address	Used In
disp_table	Array for storing a hexadecimal character (from "1" to "F")	H'FB80	sci_print_hex_byte

5. Flowcharts

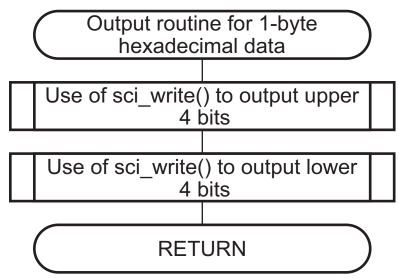
5.1 Main Routine



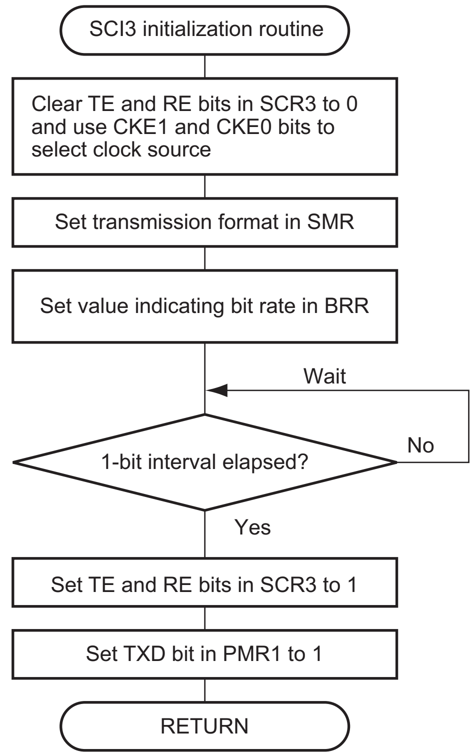
5.2 Data Transmission Routine



5.3 Output Routine for One-Byte Hexadecimal Data



5.4 SCI3 Initialization Routine



6. Program Listing

```
/**********************************************************************************/
/*                                                                                */
/*  H8/300H Series -H8/36077-                                                     */
/*  Application Note                                                              */
/*                                                                                */
/*  Function                                                                      */
/*  : How to Use Reset Factor Flag                                                */
/*                                                                                */
/*  External Clock : 10MHz                                                        */
/*  Internal Clock : 10MHz                                                        */
/*                                                                                */
/*  Sub Clock      : 32.768kHz                                                    */
/*                                                                                */
/**********************************************************************************/

#include    <machine.h>

/**********************************************************************************/
/*  Symbol Definition                                                             */
/**********************************************************************************/
struct BIT {
    unsigned char   b7:1;                           /* bit7                       */
    unsigned char   b6:1;                           /* bit6                       */
    unsigned char   b5:1;                           /* bit5                       */
    unsigned char   b4:1;                           /* bit4                       */
    unsigned char   b3:1;                           /* bit3                       */
    unsigned char   b2:1;                           /* bit2                       */
    unsigned char   b1:1;                           /* bit1                       */
    unsigned char   b0:1;                           /* bit0                       */
};
#define TDR      *(volatile unsigned char*)0xFFAB       /* Transmit Data Register         */
#define SSR      *(volatile unsigned char*)0xFFAC       /* Serial Status Register         */
#define SCR3  *(volatile unsigned char*)0xFFAA          /* Serial Control Register 3      */
#define SMR      *(volatile unsigned char*)0xFFA8       /* Serial Mode Register           */
#define BRR      *(volatile unsigned char*)0xFFA9       /* Bit Rate Register              */
#define PMR1  *(volatile unsigned char*)0xFFE0          /* Port Mode Register 1           */
#define TCSRWD    *(volatile unsigned char*)0xFFC0    /* Timer Control Status Register WD */
#define TCSRWD_BIT (*(volatile struct BIT *)0xFFC0)   /* Timer Control Status Register WD */
#define B6WI    TCSRWD_BIT.b7              /* Timer Control Status Register WD Bit 7   */
#define TCWE    TCSRWD_BIT.b6              /* Timer Control Status Register WD Bit 6   */
#define B4WI    TCSRWD_BIT.b5              /* Timer Control Status Register WD Bit 5   */
#define TCSRWE  TCSRWD_BIT.b4              /* Timer Control Status Register WD Bit 4   */
#define B2WI    TCSRWD_BIT.b3              /* Timer Control Status Register WD Bit 3   */
#define WDON    TCSRWD_BIT.b2              /* Timer Control Status Register WD Bit 2   */
#define B0WI    TCSRWD_BIT.b1              /* Timer Control Status Register WD Bit 1   */
#define WRST    TCSRWD_BIT.b0              /* Timer Control Status Register WD Bit 0   */
#define TCWD  *(volatile unsigned char*)0xFFC1          /* Timer Count WD                 */
#define TMWD  *(volatile unsigned char*)0xFFC2          /* Timer Mode Register WD         */
#define LVDCR *(volatile unsigned char*)0xF730 /* Low Voltage Detect Control Register      */
#define LVDSR *(volatile unsigned char*)0xF731 /* Low Voltage Detect Status Register       */
#define LVDRF  *(volatile unsigned char *)0xF732 /* Reset Factor Distinguish Register      */
#define LVDRF_BIT (*(volatile struct BIT *)0xF732) /* Reset Factor Distinguish Register    */
```

```
#define LVDRF_PRST    LVDRF_BIT.b1           /* Reset Factor Distinguish Register Bit 1 */
#define LVDRF_WRST    LVDRF_BIT.b0           /* Reset Factor Distinguish Register Bit 0 */

/*********************************************************************************************/
/*  Function Define                                                                          */
/*********************************************************************************************/
extern void INIT (void);                               /* SP Set                         */
void main ( void );                                    /* Main Function                  */
void sci_write ( unsigned char d);                     /* Serial Transmit Routine        */
void sci_init ( void );                                /* SCI3 Serial Initial Setting    */
void sci_print_hex_byte ( unsigned char data );        /* 16Hex Byte Output              */

/*********************************************************************************************/
/*  RAM Define                                                                               */
/*********************************************************************************************/
unsigned char disp_table[16];                          /* 16Hex Display Table            */

/*********************************************************************************************/
/*  Vector Address                                                                           */
/*********************************************************************************************/
#pragma section     V1                                 /* Vector Section Setting         */
void (*const VEC_TBL1[])(void) = {                     /* 0x00 Reset                     */
    INIT
};

#pragma section                                        /* P                              */

/*********************************************************************************************/
/*  Main Program                                                                             */
/*********************************************************************************************/
void main ( void )
{
    unsigned char WRST_flg = 0;                        /* WDT Reset Flag                 */

    disp_table[0] = 0x30;                              /* Define "0"                     */
    disp_table[1] = 0x31;                              /* Define "1"                     */
    disp_table[2] = 0x32;                              /* Define "2"                     */
    disp_table[3] = 0x33;                              /* Define "3"                     */
    disp_table[4] = 0x34;                              /* Define "4"                     */
    disp_table[5] = 0x35;                              /* Define "5"                     */
    disp_table[6] = 0x36;                              /* Define "6"                     */
    disp_table[7] = 0x37;                              /* Define "7"                     */
    disp_table[8] = 0x38;                              /* Define "8"                     */
    disp_table[9] = 0x39;                              /* Define "9"                     */
    disp_table[10] = 0x41;                             /* Define "A"                     */
    disp_table[11] = 0x42;                             /* Define "B"                     */
    disp_table[12] = 0x43;                             /* Define "C"                     */
    disp_table[13] = 0x44;                             /* Define "D"                     */
    disp_table[14] = 0x45;                             /* Define "E"                     */
    disp_table[15] = 0x46;                             /* Define "F"                     */

    sci_init();                                        /* Serial Initial Setting         */

    LVDCR = 0xFC;                                      /* Set LVDR Detect Voltage 3.6V   */
```

```
    if ((LVDRF_PRST == 0) && (LVDRF_WRST == 0))          /* External Reset?              */
    {
       TCSRWD = 0x9E;                                    /* Watch Dog Timer Stop         */
       TCSRWD = 0xB2;                                    /* Watch Dog Timer Stop         */
       sci_print_hex_byte(LVDRF);                        /* Output LVDRF With 16Hex      */
       WRST_flg = 1;                                     /* Set WDT Reset Flag           */

       LVDRF = 0x00;                                     /* Clear LVDRF For Next Detection */
    }

    if (LVDRF_PRST == 1)                   /* Power On Reset Or Low Voltage Detect Reset?  */
    {
       sci_print_hex_byte(LVDRF);                        /* Output LVDRF With 16Hex      */
       LVDRF = 0x00;                                     /* Clear LVDRF For Next Detection */
    }

    if (WRST_flg ==0)                                    /* WDT Reset Flag Clear?        */
    {
       while(LVDRF_WRST != 1);                           /* Wait Until WRST=1            */

       TCSRWD = 0x9E;                                    /* Watch Dog Timer Stop         */
       TCSRWD = 0xB2;                                    /* Watch Dog Timer Stop         */

       sci_print_hex_byte(LVDRF);                        /* Output LVDRF With 16Hex      */
       LVDRF = 0x00;                                     /* Clear LVDRF For Next Detection */
    }
    while(1);
}

/******************************************************************************************/
/* Serial Transmit Routine                                                                */
/******************************************************************************************/
void sci_write ( unsigned char d)
{
    while(!(SSR & 0x80)){                                /* Wait Until TDRE=1            */
    }
    TDR = d;                                             /* Write Data To TDR            */
    while(!(SSR & 0x04)){                                /* Wait Until TEND=1            */
    }
}

/******************************************************************************************/
/* Output 16Hex Byte
                                                                                          */
/******************************************************************************************/
void sci_print_hex_byte( unsigned char data )
{

    sci_write( disp_table[ ( data & 0xf0 ) >> 4 ] );     /* Output High 4 bits           */

    sci_write( disp_table[ ( data & 0xf ) ] );           /* Output Low 4 bits            */

}
```

```
/*********************************************************************************************/
/* Serial Initial Setting
                                                                                             */
/*********************************************************************************************/
void sci_init( void )
{
    unsigned long i = 0;

    SCR3 = 0x00;                                              /* Clear TE And RE             */
    SMR = 0x00;                                       /* Set Transmit Formart And Clock Source  */
    BRR = 0x1f;                                               /* Set 9.8304MHz 9600bps       */


    for( i=0; i<10; i++ );                                    /* Wait 1 bit                  */

    SCR3 = 0x30;                                              /* Set TE And RE               */
    PMR1 = 0x0e;                                              /* Set TXD Output Terminal     */

}
```

Link Addressing

Section Name	Address
CV1	H'0000
P	H'0100
C$BSEC	
C$DSEC	
D	
R	H'FB80
B	

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Sep.07.05	—	First edition issued

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
   The information described here may contain technical inaccuracies or typographical errors. Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
   Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (http://www.renesas.com).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
   Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.