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H8SX Family

ΔΣ Analog–Digital Conversion in Single Mode

Introduction

The H8SX/1622F has an on-chip 16-bit ΔΣ A/D converter, i.e. a converter in which the ΔΣ-modulation technique is applied. In comparison with successive-approximation A/D converters, this technique is suitable when high resolution is required. This application note describes an example of the ΔΣ A/D converter in single-mode operation.

Target Device

H8SX/1622F

Preface

Descriptions in this application note are in line with those in the hardware manual for the H8SX/1622 group, and the program is usable on the above device for which operation has been confirmed.

For other devices, however, since some functions and the set of included functions will vary from device to device, only apply the program after full evaluation with confirmation against the relevant hardware manual.

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2. Applicable Conditions 3
3. Description of Operation 4
4. Description of Software 6
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6. Point for Caution 18

1. Specifications

In this example, the ΔΣ A/D converter is operated in single-mode to A/D-convert, with a gain of eight, input voltages in the range from 1.45 to 1.85 V*. The results of conversion are stored in internal RAM.

Note: * When AVrefT = 3.3 V, input to a maximum range from 1.375 to 1.925 V is possible.

1. Figure 1 shows an example of the connections for ΔΣ A/D conversion in single mode.
2. In single mode, A/D conversion proceeds once on one channel.
3. Input voltages on the ANDS0 pin vary within the range from 1.45 to 1.85 V. The gain for ΔΣ A/D conversion is set to eight times, and offset cancellation of the DC component sets the central value of input voltage to 1.65 V.
4. A/D conversion is initiated by an external trigger.
5. When a rising edge is input on the $\overline{\text{ANDSTRG}}$ pin the result of A/D conversion is stored in the DSADDR0 register. The value in that register is then transferred to on-chip RAM. In more detail, the result stored in register DSADDR0 is the A/D-converted input voltage on the ANDS0 pin (for channel 0), in the form of a signed two's complement number relative to the offset-canceling voltage.

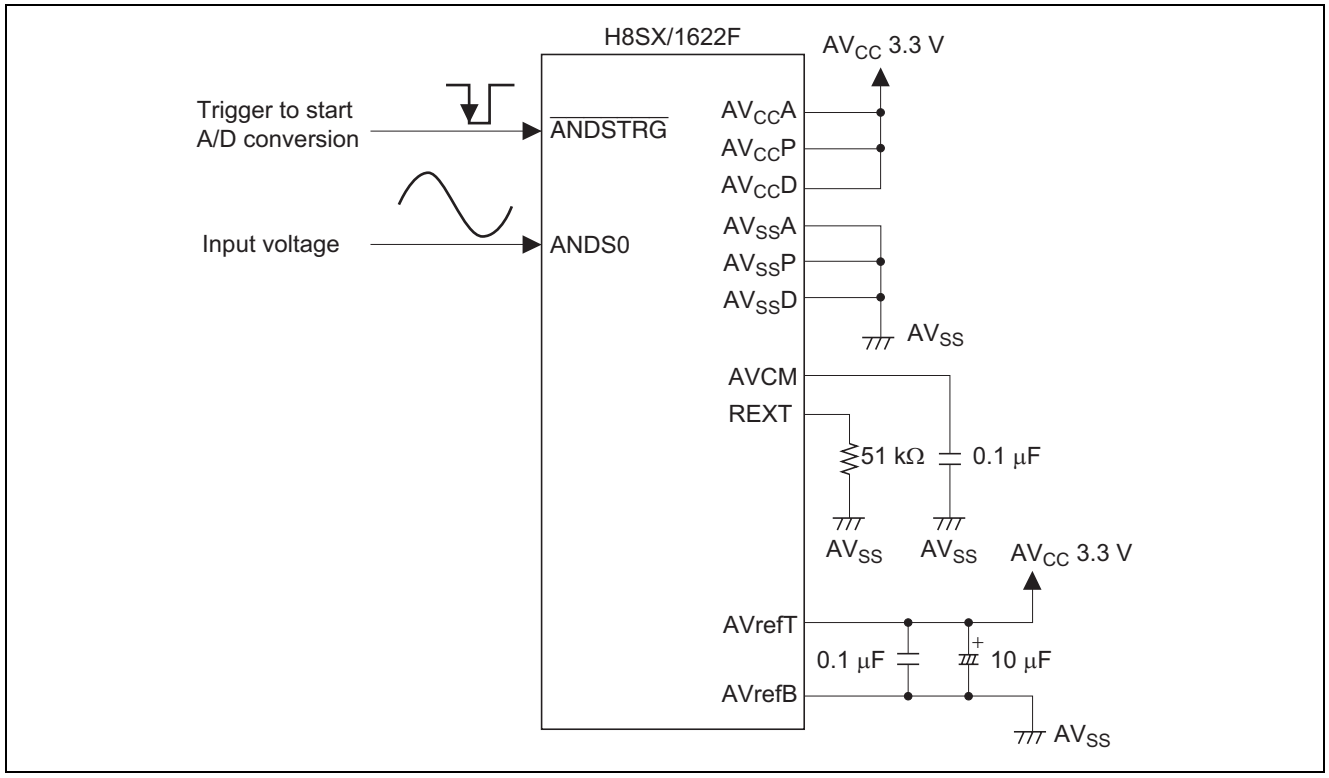


Figure 1 Example of Connection for ΔΣA/D Conversion in Single Mode

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Details
Operating frequency	EXTAL input clock: 16 MHz System clock (Iϕ): 32 MHz (input clock frequency-multiplied by 2) Peripheral-module clock (Pϕ): 32 MHz (input clock frequency-multiplied by 2) External-bus clock (Bϕ): 32 MHz (input clock frequency-multiplied by 2) ΔΣ-dedicated clock (Aϕ): 25.6 MHz (input clock frequency-multiplied by 8/5)
Operating mode	Mode 7 (single-chip mode) Mode-pin setting: MD2 = 1, MD1 = 1, MD0 = 1

3. Description of Operation

Figure 2 gives a schematic view of the operation of ΔΣ A/D conversion in single mode. Table 2 gives detailed descriptions of the operations at points 1 to 4 in figure 2. Please refer to both table 2 and figure 2.

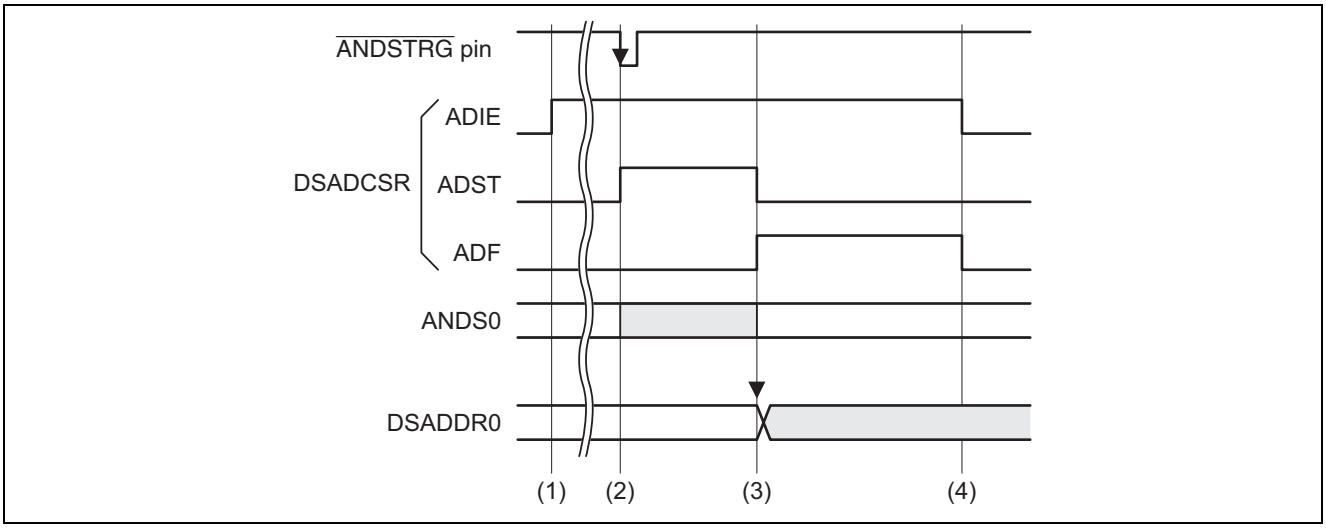


Figure 2 Operation of ΔΣA/D Conversion in Single Mode

Table 2 Details of Processing

	Hardware Processing	Software Processing
(1)	Power-on reset	Initial settings (a) Enable starting of ΔΣ A/D conversion by a trigger signal on the $\overline{\text{ANDSTRG}}$ pin. (b) Set the gain for ΔΣ A/D conversion to eight. (c) Other settings: See "3. Description of Software" for these.
(2)	Start of A/D conversion (a) Generation of trigger input for the $\overline{\text{ANDSTRG}}$ pin (b) ADST bit in DSADCSR = 1 Start A/D conversion on channel 0 (ANDS0 pin).	No processing
(3)	End of A/D conversion (a) Transfer of data produced by A/D conversion to DSADDR0 (b) ADF bit in DSADCSR is set to 1 (setting of the A/D end flag).	No processing
(4)	No processing	DSADI interrupt request (a) ADF in DSADCSR = 0 Clear the A/D end flag. (b) Store the value from DSADDR0 in on-chip RAM. (c) By setting bits TRGS0, 1 in DSADCSR to b'00, disable starting of A/D conversion by an external trigger. (d) Clear (to 0) the ADIE bit in DSADCSR.

[Legend]
DSADCSR: ΔΣ A/D conversion control/status register
DSADDR0: ΔΣ A/D data register 0

4. Description of Software

4.1 Operating Environment

Table 3 Operating Environment

Item	Details
Development tool	High-performance Embedded Workshop Ver. 4.03.00
C/C++ compiler	H8, H8/300 Series C/C++ Compiler Ver. 6.02.00 from Renesas Technology
	Option settings -cpu=h8sxa:24:md, -code = machinecode, -optimize=1, -regparam=3 -speed=(register, shift, struct, expression)
Optimizing linkage editor	Optimizing Linkage Editor Ver. 9.03.00 from Renesas Technology
	Option settings: None

Table 4 Section Settings

Address	Section Name	Description
H'001000	P	Program area
H'FF2000	ADCbuf	Non-initialized data area (on-chip RAM area)

Table 5 Interrupt/exception-processing vector tables

Requesting Source		Vector Number	Vector Table Address	Destination Interrupt Function
Reset		0	H'000000	init
ΔΣA/D	DSADI	224	H'000380	dsadi_int

4.2 List of Functions

The functions of this sample application are listed in table 6. The hierarchy of function calls for the application is shown in figure 3.

Table 6 List of Functions

Function Name	Description
init	Initialization routine Releases required modules from the module-stop state, makes clock settings, and calls function main
main	Main routine Enables ΔΣ A/D conversion on channel 0 and makes the setting for the trigger signal on the $\overline{\text{ANDSTRG}}$ pin to start A/D conversion.
dsadi_int	ΔΣ A/D interrupt processing Processing for the DSADI (end of ΔΣ A/D conversion) interrupt. Handles processing to store the result of A/D conversion in on-chip RAM, clear the end-of-A/D-conversion flag, and disable A/D conversion interrupts.

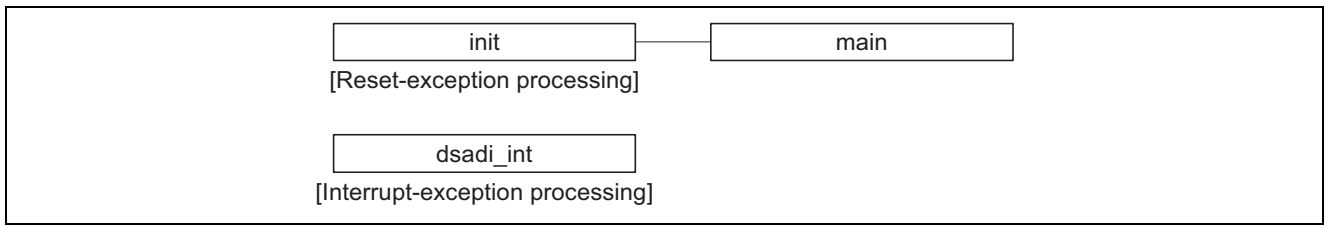


Figure 3 Hierarchical Structure of Function Calls

4.3 RAM Usage

Table 7 RAM Usage

Type	Variable Name	Description	Used in (Functions)
unsigned short	ADCbuf	Area of on-chip RAM (two bytes) for storage of the result of A/D conversion (DSADDR) (two bytes)	main, dsadi_int

4.4 Description of Functions

4.4.1 Function init

1. Functionality in outline
   Initialization routine. Releases the required modules from module-stop mode, makes clock settings, and calls the main function.
2. Arguments
   None
3. Return value
   None
4. Description of internal registers used
   The internal registers used in the sample application are listed below. Note that the settings below are for this sample task and are not the initial values.

- Mode control register (MDCR) Number of bits: 16 Address: H'FFFDC0

Bit	Bit Name	Setting	R/W	Description
11	MDS3	—*	R	Mode Select 3 to 0
10	MDS2	—*	R	These bits indicate the operating mode selected by the mode
9	MDS1	—*	R	pins (MD2 to MD0) (see table 8).
8	MDS0	—*	R	When MDCR is read, the signal levels input on pins MD2 to MD0 are latched into these bits. These latches are released by a reset.

Note: * Determined by pins MD3 to MD0.

Table 8 Setting of Bits MDS3 to MDS0

MCU	Pins			MDCR			
Operating Mode	MD2	MD1	MD0	MDS3	MDS2	MDS1	MDS0
1	0	0	1	1	1	0	1
2	0	1	0	1	1	0	0
4	1	0	0	0	0	1	0
5	1	0	1	0	0	0	1
6	1	1	0	0	1	0	1
7	1	1	1	0	1	0	0

- System clock control register (SCKCR) Number of bits: 16 Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Description
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock provided to
8	ICK0	1	R/W	the CPU, DMAC, and DTC. 001: Input clock × 2
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module clock.
4	PCK0	1	R/W	001: Input clock × 2
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	1	R/W	001: Input clock × 2

- MSTPCRA, MSTPCRB, and MSTPCRC set the module stop function. Setting a bit to 1 makes the corresponding module enter the module stop state, while clearing the bit to 0 clears the module stop state.

- Module stop control register A (MSTPCRA) Number of bits: 16 Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Target Module
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable Enables/disables all-module-clock-stop mode for reducing current consumption by stopping the bus controller and I/O ports operations when the CPU executes the SLEEP instruction after the module stop state has been set for all the on-chip peripheral modules controlled by MSTPCR. 0: All-module-clock-stop mode disabled. 1: All-module-clock-stop mode enabled.
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
11	MSTPA11	1	R/W	8-bit timers (TMR_7 and TMR_6)
10	MSTPA10	1	R/W	8-bit timers (TMR_5 and TMR_4)
9	MSTPA9	1	R/W	8-bit timers (TMR_3 and TMR_2)
8	MSTPA8	1	R/W	8-bit timers (TMR_1 and TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
0	MSTPA0	1	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

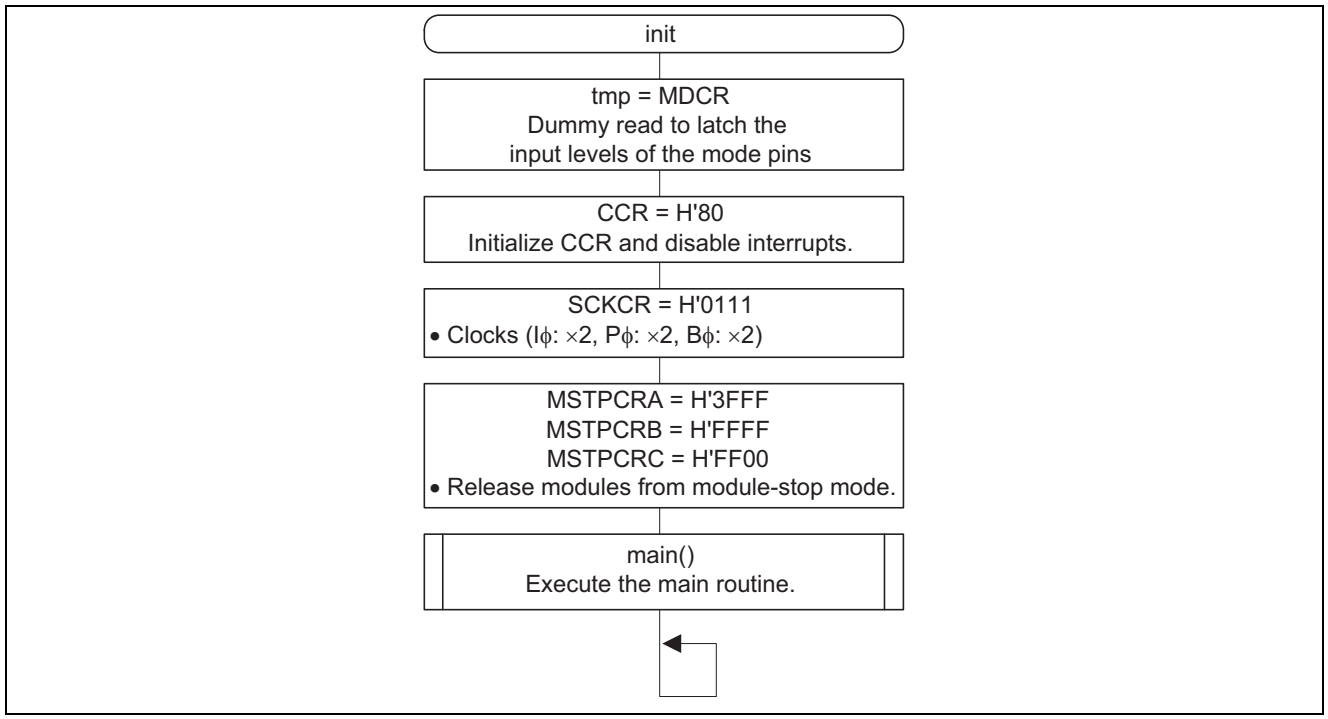
- Module stop control register B (MSTPCRB) Number of bits: 16 Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Target Module
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communications interface_4 (SCI_4)
11	MSTPB11	1	R/W	Serial communications interface_3 (SCI_3)
10	MSTPB10	1	R/W	Serial communications interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communications interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial communications interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus interface 1 (IIC_1)
6	MSTPB6	1	R/W	I^2C bus interface 0 (IIC_0)
5	MSTPB5	1	R/W	User break controller (USB)

- Module stop control register C (MSTPCRC) Number of bits: 16 Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Target Module
14	MSTPC14	1	R/W	ΔΣ A/D converter
13	MSTPC13	1	R/W	A/D conterter
5	MSTPC5	0	R/W	On-chip RAM Always set the MSTPC2 and MSTPC5 bits to the same value.
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF) Always set the MSTPC2 and MSTPC5 bits to the same value.
1	MSTPC1	0	R/W	On-chip RAM_1, 0 (H'FF8000 to H'FFBFFF)
0	MSTPC0	0	R/W	Always set the MSTPC1 and MSTPC0 bits to the same value.

5. Flowchart



4.4.2 main Function

1. Functional overview
   Main routine. Enables ΔΣ A/D conversion on channel 0 and sets starting of A/D conversion by the trigger signal on the $\overline{\text{ANDSTRG}}$ pin.
2. Arguments
   None
3. Return value
   None

4. Description of internal registers used
   The internal registers used in the sample application are listed below. Note that the settings below are for this sample task and are not the initial values.

- ΔΣ A/D control/status register (DSADCSR) Number of bits: 16 Address: H'FFFC18

Bit	Bit Name	Setting	R/W	Description
15	ADF	0	R/(W)*	A/D Conversion End Flag Indicates whether A/D conversion has ended. [Setting condition] • A/D conversion on all of the selected channels has ended. [Clearing conditions] • Writing 0 to ADF after reading it as 1 (When cleared to 0 by interrupts from CPU, be sure to read the flag after writing 0). • Activation of the DMAC by the DSADI interrupt and transfer of data in DSADDRn.
14	ADIE	1	R/W	A/D Conversion Interrupt Enable Setting this bit to 1 enables generation of DSADI interrupt requests in accord with the ADF bit.
13	ADST	0	R/W	A/D Conversion Start Controls starting and stopping of A/D conversion. Clearing this bit to 0 stops A/D conversion, placing the converter in the wait sate. Setting this bit to 1 starts A/D conversion. In single mode, ADST is automatically cleared at the end of A/D conversion on the selected channels. In scan mode, ADST must be cleared by software because it is not cleared automatically. [Setting conditions] • Writing 1 to ADST by software • Input of the corresponding A/D conversion trigger signal while starting of A/D conversion by a trigger is enabled (TRGS1, TRGS0 ≠ B'00) [Clearing conditions] • Writing 0 to ADST by software • End of A/D conversion on all selected channels while SCANE = 0
11	SCANE	0	R/W	Scan Mode Enable Selects the mode of A/D conversion. 0: Single mode 1: Scan mode

Bit	Bit Name	Setting	R/W	Description
9	TRGS1	1	R/W	Timer Trigger Select 1, 0
8	TRGS0	1	R/W	These bits enable starting of A/D conversion by a trigger signal. 00: Disables starting by trigger signals. 01: Enables starting by a trigger from the TPU. 10: Enables starting by a trigger from the TMR. 11: Enables starting by the $\overline{\text{ANDSTRG}}$ pin input. *2
5	CH5	0	R/W	A/D Conversion Channel Select
4	CH4	0	R/W	These bits select the analog input channels for A/D conversion.
3	CH3	0	R/W	They are independent of each other and can be set as desired.
2	CH2	0	R/W	0: Channel n is not selected.
1	CH1	0	R/W	1: Channel n is selected.
0	CH0	1	R/W	(n = 0 to 5)

Notes: 1. Only 0 can be written to clear the flag.
2. When selecting starting of A/D conversion by the $\overline{\text{ANDSTRG}}$ signal, clear the DDR bit for the corresponding pin to 0 and set the ICR bit to 1.

- ΔΣ A/D control register (DSADCR) Number of bits: 16 Address: H'FFFC1A

Bit	Bit Name	Setting	R/W	Description
15	CKS	0	R/W	Clock Select Sets the A/D conversion time. 0: 286-state conversion 1: Setting prohibited
13	GAIN1	1	R/W	Gain Select
12	GAIN2	1	R/W	These bits set the gain for amplifying the analog input signals. 00: ×1 01: ×2 10: ×4 11: ×8
7	DSE	1	R/W	ΔΣ Modulator Control Controls whether the ΔΣ modulator is stopped or run. 0: ΔΣ modulator is stopped (Aϕ/8 clock is stopped). 1: ΔΣ modulator runs (Aϕ/8 clock runs).

- ΔΣ A/D mode register (DSADMR) Number of bits: 8 Address: H'FFFC24

When overwriting the value in this register, do so after setting the module-stop bit for the ΔΣ A/D converter to 1 and ensuring that the ΔΣ A/D converter has stopped.

Bit	Bit Name	Setting	R/W	Description
7	BIASE	1	R/W	Bias Circuit Control Sets whether the bias circuit is to be operated or stopped. 0: Stops the bias circuit. 1: Operates the bias circuit.
2	ACK2	0	R/W	ΔΣ A/D Converter Frequency Division Clock Select These bits select the frequency of the ΔΣ A/D clock (Aϕ). The ratio to the input clock is as follows. In setting, the value of Aϕ should be in the neighborhood of 25 MHz. 000: · 1/6 001: · 1/5 010: · 1/4 011: · 1/3 1xx: Setting prohibited
1	ACK1	0	R/W	
0	ACK0	1	R/W	

[Legend] x: Don't care

- ΔΣ A/D offset cancel DAC input 0 (DSADOF0) Number of bits: 16 Address: H'FFFC10

DSADOF0 specifies the values to be input to the DAC for canceling the offset of analog input channel 0. Offset cancellation here means cancellation of the DC components of signals input to analog input channels 0, not cancellation of the offset of the internal amplifier.

Settings of the DSADOF registers can only be changed while the ADST bit is clear.

Setting: H'0200

- Port 1 Data Direction Register (P1DDR) Number of bits: 8 Address: H'FFFB80

Bit	Bit Name	Setting	R/W	Description
7	P17DDR	0	R/W	0: Sets pin P17 as an input pin 1: Sets pin P17 as an output pin

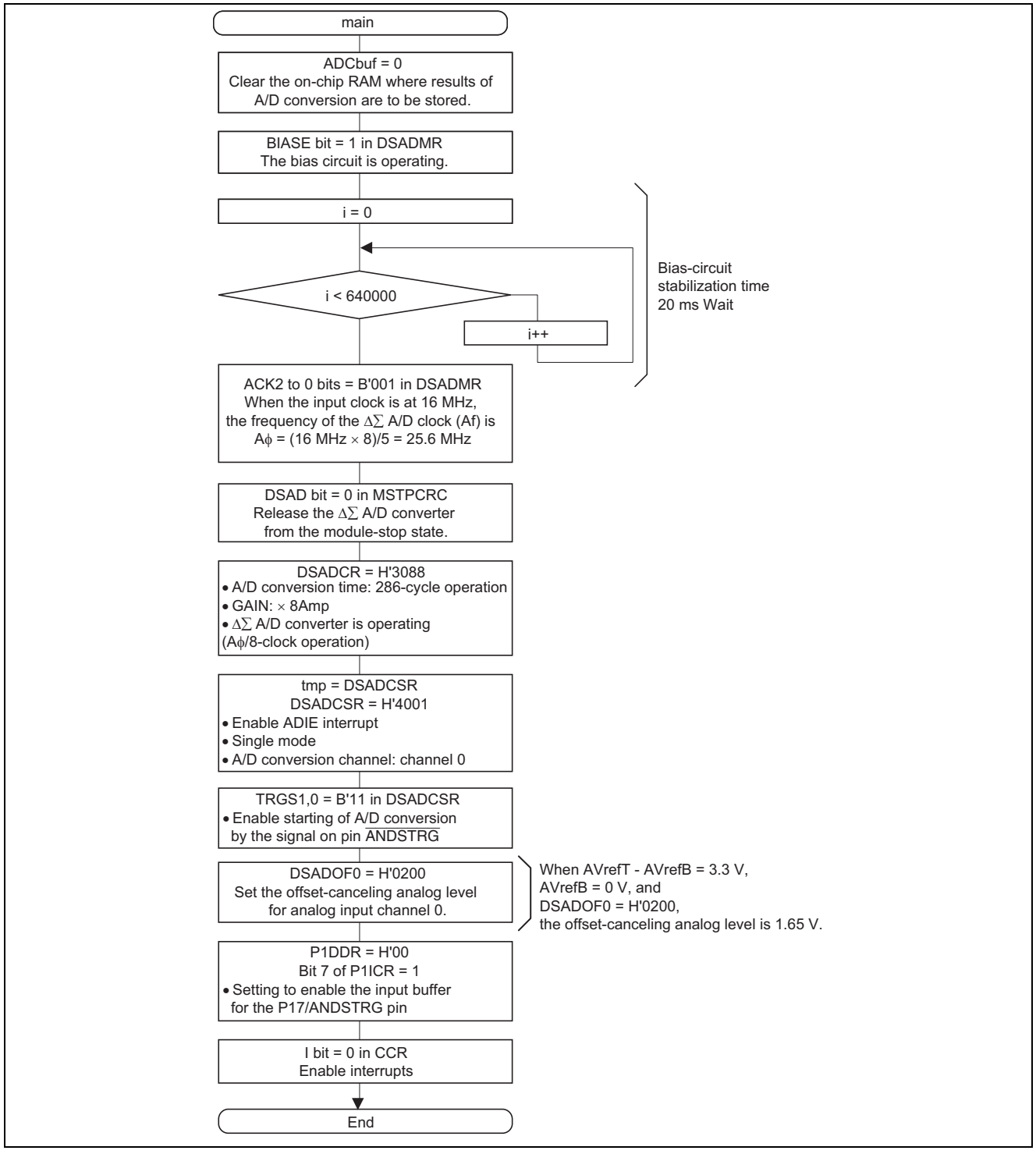
- Port 1 Input Buffer Control Register (P1CR) Number of bits: 8 Address: H'FFFB90

Bit	Bit Name	Setting	R/W	Description
7	P17ICR	1	R/W	0: Disables the input buffer on pin P17. The input signal from the pin is fixed to the high level. 1: Enables the input buffer on pin P17. The input signal reflects the pin state on the peripheral module side.

- Module Stop Mode Control Register C (MSTPCRC) Number of bits: 16 Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Description
14	MSTPC14	0	R/W	0: Releases the ΔΣ A/D converter from module-stop mode 1: Places the ΔΣ A/D converter in module-stop mode

5. Flowchart


main
ADCbuf = 0
Clear the on-chip RAM where results of A/D conversion are to be stored.
BIASE bit = 1 in DSADMR
The bias circuit is operating.
i = 0
i < 640000
i++
Bias-circuit stabilization time 20 ms Wait
ACK2 to 0 bits = B'001 in DSADMR
When the input clock is at 16 MHz, the frequency of the ΔΣ A/D clock (Af) is Aϕ = (16 MHz × 8)/5 = 25.6 MHz
DSAD bit = 0 in MSTPCRC
Release the ΔΣ A/D converter from the module-stop state.
DSADCR = H'3088
• A/D conversion time: 286-cycle operation
• GAIN: × 8Amp
• ΔΣ A/D converter is operating (Aϕ/8-clock operation)
tmp = DSADCSR
DSADCSR = H'4001
• Enable ADIE interrupt
• Single mode
• A/D conversion channel: channel 0
TRGS1,0 = B'11 in DSADCSR
• Enable starting of A/D conversion by the signal on pin ANDSTRG
DSADOF0 = H'0200
Set the offset-canceling analog level for analog input channel 0.
When AVrefT - AVrefB = 3.3 V, AVrefB = 0 V, and DSADOF0 = H'0200, the offset-canceling analog level is 1.65 V.
P1DDR = H'00
Bit 7 of P1ICR = 1
• Setting to enable the input buffer for the P17/ANDSTRG pin
I bit = 0 in CCR
Enable interrupts
End

4.4.3 Function dsadi_int

1. Functional overview
   Processing routine for the DSADI interrupt (ΔΣ A/D conversion end interrupt). Handles processing to store the result of A/D conversion in on-chip RAM, clear the A/D conversion end flag, and disable A/D conversion interrupts.
2. Arguments
   None
3. Return value
   None
4. Description of internal registers used
   The internal registers used in the sample application are listed below. Note that the settings below are for this sample task and are not the initial values.

- ΔΣ A/D control/status register (DSADCSR) Number of bits: 8 Address: H'FFFC18

Bit	Bit Name	Setting	R/W	Description
15	ADF	0	R/(W)*[1]	A/D Conversion End Flag Indicates whether A/D conversion has ended. [Setting condition] • A/D conversion on all of the selected channels has ended. [Clearing conditions] • Writing 0 to ADF after reading it as 1 • Activation of the DMAC by the DSADI interrupt and transfer of data in DSADDRn.
9	TRGS1	0	R/W	Timer Trigger Select 1, 0
8	TRGS0	0	R/W	These bits enable starting of A/D conversion by a trigger signal. 00: Disables starting by trigger signals. 01: Enables starting by a trigger from the TPU. 10: Enables starting by a trigger from the TMR. 11: Enables starting by the $\overline{\text{ANDSTRG}}$ pin input. *[2]

Notes: 1. Only 0 can be written here, to clear the flag.
2. When selecting starting of A/D conversion by the $\overline{\text{ANDSTRG}}$ signal, clear the DDR bit for the corresponding pin to 0 and set the ICR bit to 1.

- ΔΣ A/D data register 0 (DSADDR0) Number of bits: 16 Address: H'FFFC00

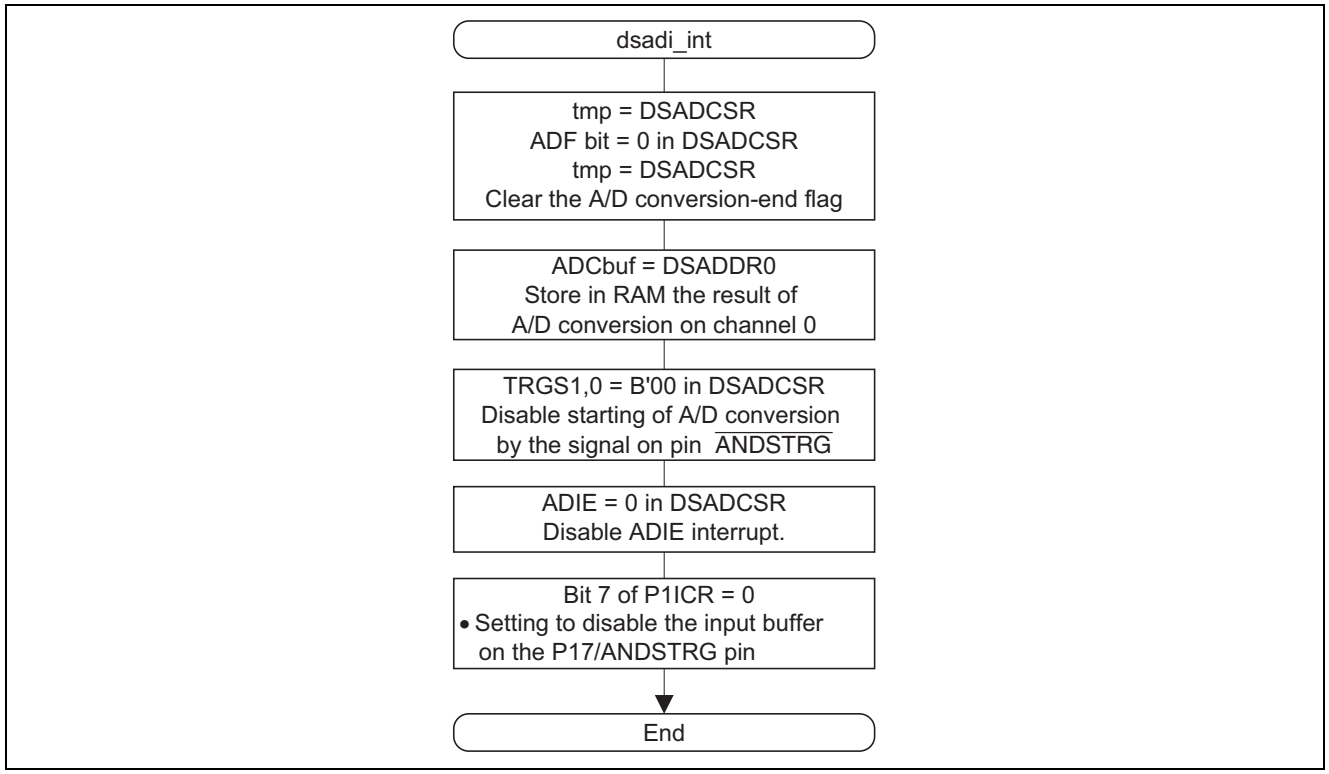
Function: DSADDR0 is 16-bit read-only registers for storing the results of A/D conversion.
One register is provided for each analog input channel, and when A/D conversion on a channel is completed, the result of conversion is stored in the corresponding register. Data stored in each register are retained until the next round of A/D conversion on that channel ends and the new result is stored.
DSADDR registers can be read by the CPU at any time, but cannot be written to.
This register is initialized with the initial value of H'0000 by a reset or in the following modes: hardware standby, deep software standby, software standby, module stop.
The A/D-converted data is stored in bit 15 to bit 0 as a signed binary number (two's complement).
Bit 15 holds the MSB and bit 0 the LSB.

Setting:

- Port 1 Input Buffer Control Register (P11CR) Number of bits: 8 Address: H'FFFB90

Bit	Bit Name	Setting	R/W	Description
7	P17ICR	0	R/W	0: Disables the input buffer on pin P17. The input signal from the pin is fixed to the high level. 1: Enables the input buffer on pin P17. The input signal reflects the pin state on the peripheral module side.

5. Flowchart



5. Documents for Reference

- Hardware Manual
  H8SX/1622 Group Hardware Manual
  The most up-to-date versions of these documents are available on the Renesas Technology Website.
- Technical News/Technical Update
  The most up-to-date information is available on the Renesas Technology Website.

6. Point for Caution

When a pin of the device is used as an input pin for a peripheral module, be sure to set the corresponding bit of the input buffer control register (PnICR) to 1.

See the hardware manual for details.

Website and Support

Renesas Technology Website
http://www.renesas.com/

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Revision Record

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