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H8SX Family

Deep Software Standby Mode

Introduction

The H8SX/1638F microcomputer has a deep software standby mode as one of its low-power states.

This application note gives an example of employment of the deep software standby mode.

Target Device

H8SX/1638F

Preface

Although the writing of this application note is in accord with the hardware manual for the H8SX/1638 Group, the program covered in this application note can be run on the target device indicated above. However, since some functional modules may be changed for the addition of functionality etc., be sure to perform a thorough evaluation by confirming the details with the hardware manual for the target device

Contents

1. Specification

The H8SX/1638F microcomputer has a deep software standby mode as one of its low power states. In deep software standby mode, the CPU, on-chip peripheral functions, on-chip RAM areas 6 to 4, and oscillator functionality are all halted. In addition, the internal power supply to these modules stops, resulting in a significant reduction in power consumption. At this time, the contents of all the registers of the CPU, on-chip peripheral functions, and on-chip RAM areas 6 to 4 become undefined.

Contents of the on-chip RAM areas 3 to 0 can be retained when all the bits RAMCUT2 to RAMCUT0 in DPSBYCR have been cleared to 0. If these bits are set to all 1, the internal power supply to the on-chip RAM areas 3 to 0 stops and the power consumption is further reduced. At this time, the contents of the on-chip RAM areas 3 to 0 become undefined.

The deep standby backup register is a 16-byte readable/writable register. The contents of this register are retained in deep software standby mode.

This application note shows an example of using the deep software standby mode which involves the deep standby backup register.

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Setting	
Operating frequency	Input clock:	12 MHz
	System clock (Iϕ):	24 MHz (input clock frequency × 2)
	Peripheral module clock (Pϕ):	24 MHz (input clock frequency × 2)
	External bus clock (Bϕ):	24 MHz (input clock frequency × 2)
Operating mode	Mode 7 (single-chip mode, MD2 = 1, MD1 = 1, MD0 = 1)	

3. Description of Modules Used

3.1 Power-down Mode

Table 2 shows conditions to shift to a power-down mode, states of the CPU and peripheral modules, and clearing method for each mode. After the reset state, since this LSI operates in normal program execution state, the modules, other than the DMAC and DTC, are stopped.

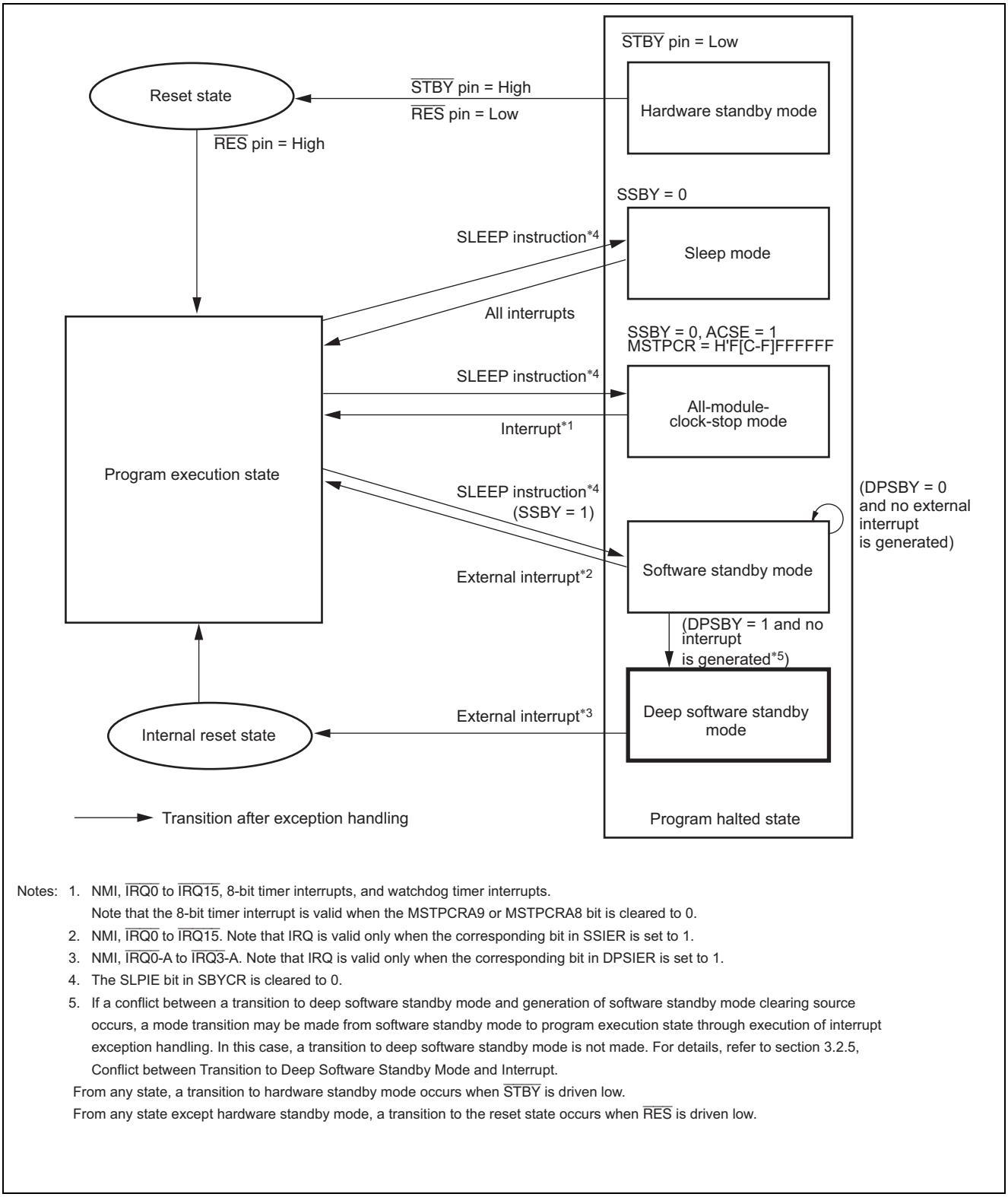
Table 2 States of Operation

State of Operation	Sleep Mode	All-Module-Clock-Stop Mode	Software Standby Mode	Deep Software Standby Mode	Hardware Standby Mode
Transition condition	Control register + instruction	Control register + instruction	Control register + instruction	Control register + instruction	Pin input
Cancellation method	Interrupt	Interrupt*2	External interrupt	External interrupt	
Oscillator	Operating	Operating	Halted	Halted	Halted
CPU	Halted (retained)	Halted (retained)	Halted (retained)	Halted (undefined)	Halted (undefined)
On-chip RAM areas 6 to 4 (H'FEE000 to H'FF3FFF)	Operating (retained)	Halted (retained)	Halted (retained)	Halted (undefined)	Halted (undefined)
On-chip RAM areas 3 to 0 (H'FF4000 to H'FFBFFF)	Operating (retained)	Halted (retained)	Halted (retained)	Halted (retained/ undefined)*5	Halted (undefined)
Watchdog timer	Operating	Operating	Halted (retained)	Halted (undefined)	Halted (undefined)
8-bit timer (unit 0/1)	Operating	Operating*4	Halted (retained)	Halted (undefined)	Halted (undefined)
Other peripheral modules	Operating	Halted*1	Halted*1	Halted*7 (undefined)	Halted*3 (undefined)
I/O ports	Operating	Retained	Retained*6	Halted*6 (undefined)	Hi-Z

Notes: "Halted (retained)" in the table means that the internal values are retained and internal operations are suspended.
"Halted (undefined)" in the table means that the internal values are undefined and the power supply for internal operations is turned off.

1. SCI enters the reset state, and other peripheral modules retain their states.
2. External interrupt and some internal interrupts (8-bit timer and watchdog timer).
3. All peripheral modules enter the reset state.
4. "Functioning" or "Halted" is selectable through the setting of bits MSTPA9 and MSTPA8 in MSTPCRA.
5. "Retained" or "undefined" of the contents of RAM is selected by the setting of the bits RAMCUT2 to RAMCUT0 in DPSBYCR.
6. Retention or high-impedance for the address bus and bus-control signals ($\overline{CS0}$ to $\overline{CS7}$, $\overline{AS}$, $\overline{RD}$, $\overline{HWR}$, and $\overline{LWR}$) is selected by the setting of the OPE bit in SBYCR.
7. Some peripheral modules enter a state where the register values are retained.

The mode transitions are shown below.



Notes: 1. NMI, IRQ0 to IRQ15, 8-bit timer interrupts, and watchdog timer interrupts.
Note that the 8-bit timer interrupt is valid when the MSTPCRA9 or MSTPCRA8 bit is cleared to 0.
2. NMI, IRQ0 to IRQ15. Note that IRQ is valid only when the corresponding bit in SSIER is set to 1.
3. NMI, IRQ0-A to IRQ3-A. Note that IRQ is valid only when the corresponding bit in DPSIER is set to 1.
4. The SLPIE bit in SBYCR is cleared to 0.
5. If a conflict between a transition to deep software standby mode and generation of software standby mode clearing source occurs, a mode transition may be made from software standby mode to program execution state through execution of interrupt exception handling. In this case, a transition to deep software standby mode is not made. For details, refer to section 3.2.5, Conflict between Transition to Deep Software Standby Mode and Interrupt.

From any state, a transition to hardware standby mode occurs when STBY is driven low.
From any state except hardware standby mode, a transition to the reset state occurs when RES is driven low.

Figure 1 Mode Transitions

3.2 Deep Software Standby Mode

3.2.1 Entry to Deep Software Standby Mode

If a SLEEP instruction is executed when the SSBY bit in SBYCR has been set to 1, a transition to software standby mode is made. In this state, if the DPSBY bit in DPSBYCR is set to 1, a transition to deep software standby mode is made.

If a software standby mode clearing source (the NMI, or IRQ0 to IRQ15) occurs when a transition to software standby mode is made, software standby mode will be cleared regardless of the DPSBY bit setting, and the interrupt exception handling starts after the oscillation settling time for software standby mode specified by the bits STS4 to STS0 in SBYCR has elapsed.

When both of the SSBY bit in SBYCR and the DPSBY bit in DPSBYCR are set to 1 and no software standby mode clearing source occurs, a transition to deep software standby mode will be made immediately after software standby mode is entered.

In deep software standby mode, the CPU, on-chip peripheral functions, on-chip RAM areas 6 to 4, and oscillator functionality are all halted. In addition, the internal power supply to these modules stops, resulting in a significant reduction in power consumption. At this time, the contents of all the registers of the CPU, on-chip peripheral functions, and on-chip RAM areas 6 to 4 become undefined.

Contents of the on-chip RAM areas 3 to 0 can be retained when all the bits RAMCUT2 to RAMCUT0 in DPSBYCR have been cleared to 0. If these bits are set to all 1, the internal power supply to the on-chip RAM areas 3 to 0 stops and the power consumption is further reduced. At this time, the contents of the on-chip RAM areas 3 to 0 become undefined.

The I/O ports can be retained in the same state as in software standby mode.

3.2.2 Exit from Deep Software Standby Mode

Exit from deep software standby mode is initiated by signals on the external interrupt pins (the NMI and $\overline{\text{IRQ0}}$-A to $\overline{\text{IRQ3}}$-A), $\overline{\text{RES}}$ pin, or $\overline{\text{STBY}}$ pin.

1. Exit from deep software standby mode by external interrupt pins
   Deep software standby mode is released when any of the DNMIF and DIRQnF (n = 3 to 0) bits in DPSIFR is set to 1. The DNMIF or DIRQnF (n = 3 to 0) bit is set to 1 when a specified edge is generated in the NMI or $\overline{\text{IRQ0}}$-A to $\overline{\text{IRQ3}}$-A pins, that has been enabled by the DIRQnE (n = 3 to 0) bit in DPSIER. The rising or falling edge of the signals can be specified with DPSIEGR for each pin.
   When deep software standby mode clearing source is generated, internal power supply starts simultaneously with the start of clock oscillation, and internal reset signal is generated for the entire LSI. Once the time specified by the WTSTS5 to WTSTS0 bits in DPSWCR has elapsed, a stable clock signal is being supplied throughout the LSI and the internal reset is cleared. Deep software standby mode is released on clearing of the internal reset, and then the reset exception handling starts.
   When deep software standby mode is released by an external interrupt pin, the DPSRSTF bit in RSTSR is set to 1.
2. Exit from deep software standby mode by the signal on the $\overline{\text{RES}}$ pin
   Clock oscillation and internal power supply start as soon as the signal on the $\overline{\text{RES}}$ pin is driven low. At the same time, clock signals are supplied to the LSI. In this case, the $\overline{\text{RES}}$ pin has to be held low until the clock oscillation has become stable. Once the signal on the $\overline{\text{RES}}$ pin is driven high, the CPU starts reset exception handling.
3. Exit from deep software standby mode by the signal on the $\overline{\text{STBY}}$ pin
   When the $\overline{\text{STBY}}$ pin is driven low, a transition is made to hardware standby mode.

3.2.3 Pin State on Exit from Deep Software Standby Mode

In deep software standby mode, the ports retain the states that were held during software standby mode. The internal of the LSI is initialized by an internal reset caused by deep software standby mode, and the reset exception handling starts as soon as deep software standby mode is released. The following shows the port states at this time.

(1) **Pins for address bus, bus control and data bus**

Pins for the address bus, bus control signals ($\overline{CS0}$, $\overline{AS}$, $\overline{RD}$, $\overline{HWR}$ and $\overline{LWR}$), and data bus operate depending on the CPU.

(2) **Pins other than address bus, bus control and data bus pins**

Whether the ports are initialized or retain the states that were held during software standby mode can be selected by the IOKEEP bit.

- When IOKEEP = 0
  Ports are initialized by an internal reset caused by deep software standby mode.
- When IOKEEP = 1
  The port states that were held in deep software standby mode are retained regardless of the LSI internal state though the internal of the LSI is initialized by an internal reset caused by deep software standby mode. At this time, the port states that were held in software standby mode are retained even if settings of I/O ports or peripheral modules are set. Subsequently, the retained port states are released when the IOKEEP bit is cleared to 0 and operation is performed according to the internal settings.

The IOKEEP bit is not initialized by internal reset caused by release of the deep software standby mode.

3.2.4 Setting Oscillation Settling Time after Exit from Deep Software Standby Mode

The WTSTS5 to WTSTS0 bits in DPSWCR should be set as follows:

1. Using a crystal resonator
   Specify the WTSTS5 to WTSTS0 bits so that the standby time is at least equal to the oscillation settling time. Table 3 shows EXTAL input clock frequencies and the standby time according to WTSTS5 to WTSTS0 settings.
2. Using an external clock
   The PLL circuit settling time should be considered. See table 3 to set the standby time.

Table 3 Oscillation Settling Time Settings

WTSTS5	WTSTS4	WTSTS3	WTSTS2	WTSTS1	WTSTS0	Standby Time	EXTAL Input Clock Frequency* (MHz) 18	16	14	12	10	0	Unit
0	0	0	0	0	0	Reserved	—	—	—	—	—	—	µs
					1	Reserved	—	—	—	—	—	—	
				1	0	Reserved	—	—	—	—	—	—	
					1	Reserved	—	—	—	—	—	—	
			1	0	0	Reserved	—	—	—	—	—	—	
					1	64	3.8	4.0	4.6	5.3	6.4	8.0	
				1	0	512	28.4	32.0	36.6	42.7	51.2	64.0	
					1	1024	56.9	64.0	73.1	85.3	102.4	128.0	
		1	0	0	0	2048	113.8	128.0	146.3	170.7	204.8	256.0	
					1	4096	0.23	0.26	0.29	0.34	0.41	0.51	ms
				1	0	16384	0.91	1.02	1.17	1.37	1.64	2.05	
					1	32768	1.82	2.05	2.34	2.73	3.28	4.10	
			1	0	0	65536	3.64	4.10	4.68	5.46	6.55	8.19	
					1	131072	7.28	8.19	9.36	10.92	13.11	16.38	
				1	0	262144	14.56	16.38	18.72	21.85	26.21	32.77	
					1	524288	29.13	32.77	37.45	43.69	52.43	65.54	
	1	0	0	0	0	Reserved	—	—	—	—	—	—	

[Legend]

: Recommended setting when external clock is in use

: Recommended setting when crystal oscillator is in use

Note * The oscillation settling time, which includes a period where the oscillation by an oscillator is not stable, depends on the resonator characteristics. The above figures are for reference.

3.2.5 Conflict between Transition to Deep Software Standby Mode and Interrupts

If a conflict between a transition to deep software standby mode and generation of software standby mode clearing source occurs, a transition to deep software standby mode is not made but the software standby mode clearing sequence is executed. In this case, an interrupt exception handling for the input interrupt starts after the oscillation settling time for software standby mode (set by the STS4 to STS0 bits in SBYCR) has elapsed.

Note that if a conflict between a deep software standby mode transition and the NMI occurs, the NMI exception handling routine is required. If this routine is not in place and the NMI is generated while the system is not in deep software standby mode, the program might crash. Thus, be sure to provide this routine.

If a conflict between a deep software standby mode transition and IRQ0 to IRQ15 interrupts occurs, a transition to deep software standby mode can be made without executing the interrupt execution handling by clearing the SSIn bits in SSIER to 0 beforehand.

4. Principles of Operation

The flow of processing of this sample task is given in figure 2. The timing of operation of this sample task is shown in figure 3. This flow of processing is described in chronological order below. Operations (1) to (5) in figure 2 and figure 3 correspond to steps (1) to (5) below.

The DPSRSTF bit in RSTSR is set to 1 when an external interrupt source releases the system from deep software standby mode, thereby generating an internal reset. This bit is set to its initial value of 0 when the $\overline{\text{RES}}$ pin is used for a pin-generated reset. In this example, the value of the DPSRSTF bit is judged at the start of the program.

Operation in the cases of a pin-generated reset or internal reset proceeds with reference to the same entry in the vector table.

(1) When the DPSRSTF bit in RSTSR is 0, the following initial settings for deep software standby mode are made and the user program is executed.
   - The deep software standby mode is entered when a SLEEP instruction is executed (SSBY in SBYCR = 1, DPSBY in DPSBYCR = 1).
   - Retained port states are released on exit from the deep software standby mode (IOKEEP in DPSBYCR = 0).
   - Power is not supplied to the on-chip RAM in deep software standby mode (bits RAMCUT2 to RAMCUT0 in DPSBYCR = B'111).
   - A falling-edge signal on the NMI pin generates the NMI which releases the system from the deep software standby mode (DNMIEG in DPSIEGR = 0).
   - The MCU's waiting time on release from the deep software standby mode is 131072 clock pulses (bits WTSTS5 to WTSTS0 in DPSBYCR = B'001101).

(2) User data in the on-chip RAM is saved in a deep standby backup register (DPSBKR0) immediately before execution of the SLEEP instruction.

(3) The SLEEP instruction causes the system to exit the program execution status and enter the deep software standby mode.

(4) The NMI releases the system from the deep software standby mode and generates an internal reset.

(5) When DPSRSTF in RSTSR is 1, the deep software standby mode setting is remade (SSBY in SBYCR = 1), user data saved to DPSBKR0 is restored, and then the user program is executed.

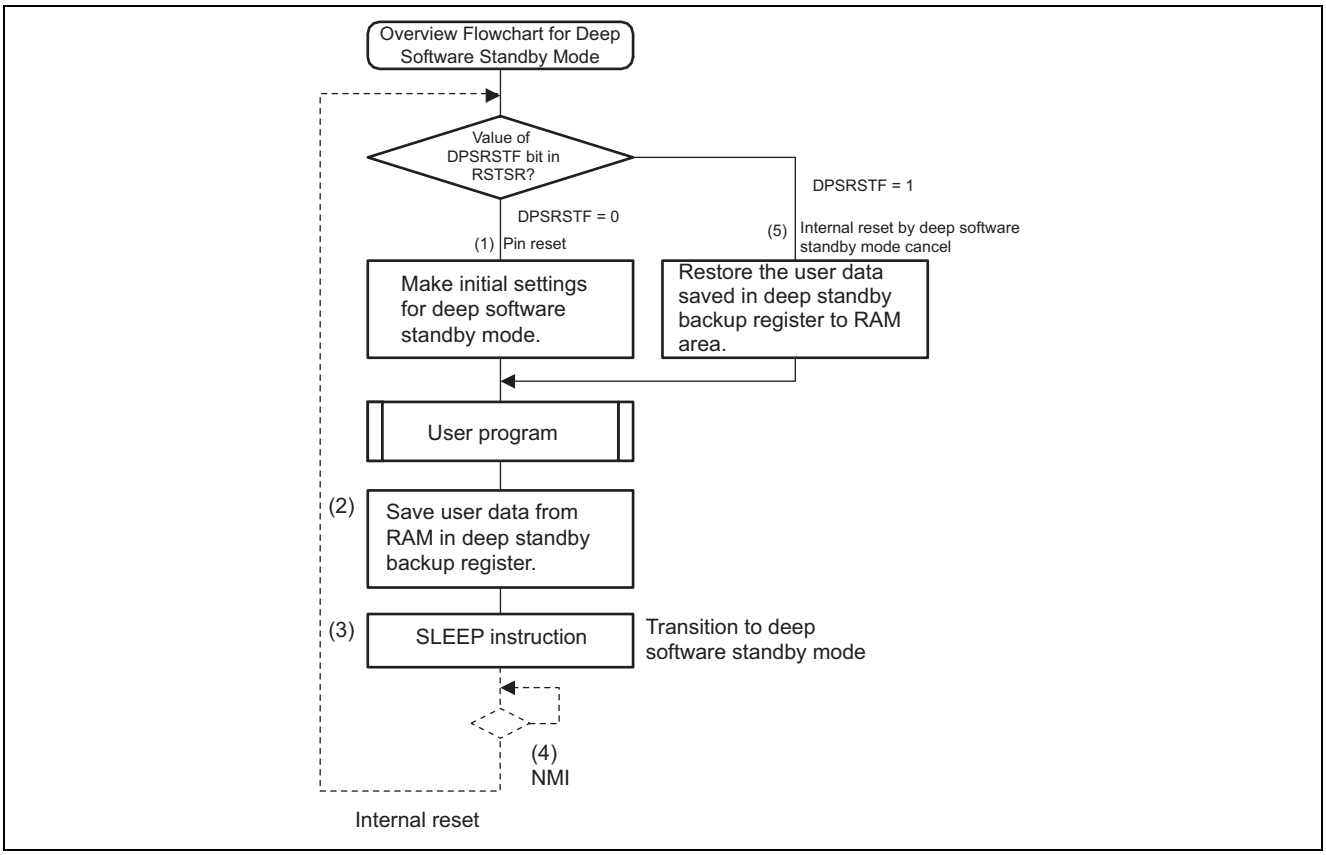


Figure 2 Overview Flowchart

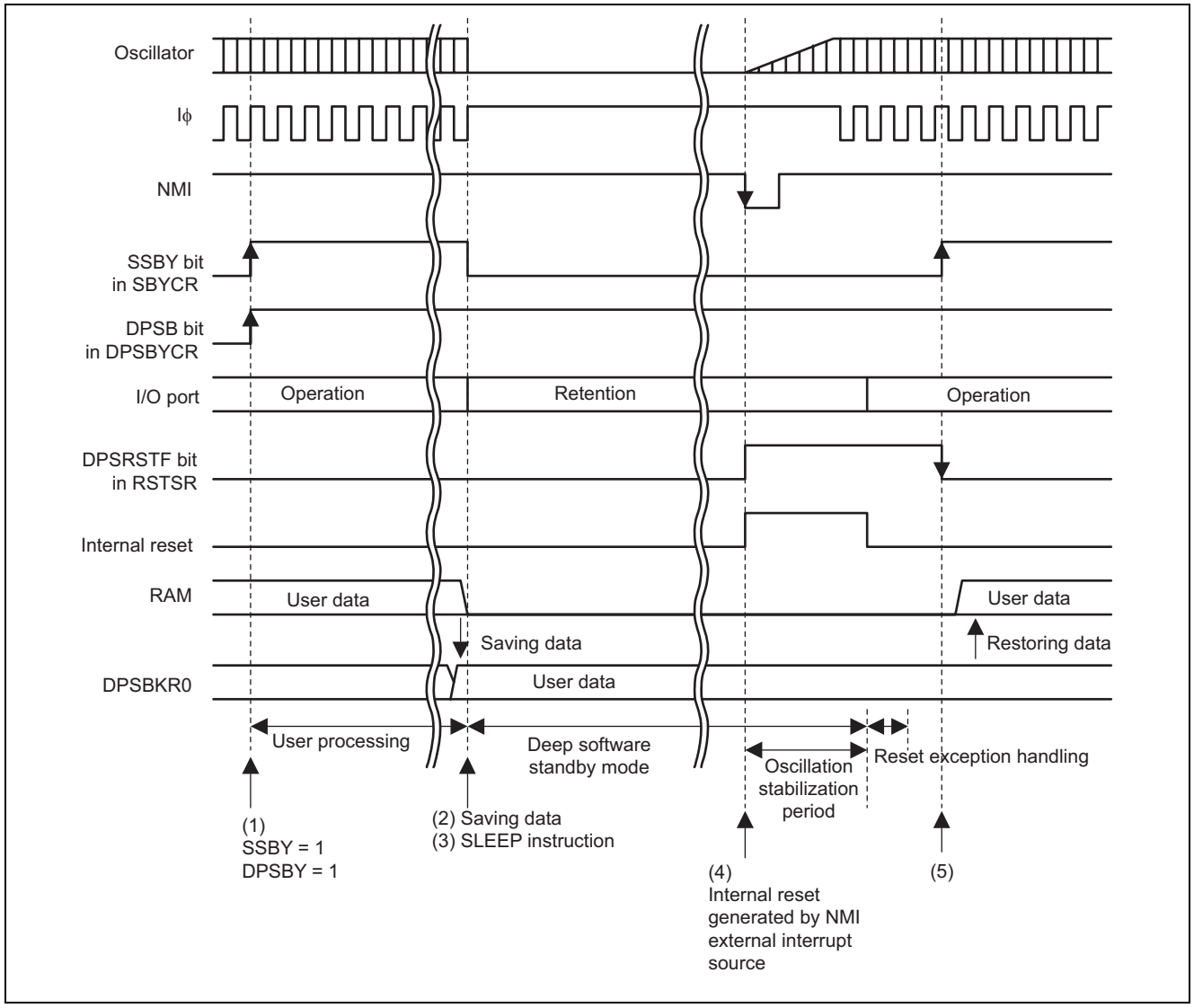


Figure 3 Operation Timing

5. Description of Software

5.1 Operating Environment

Table 4 Operating Environment

Item	Description
Development tool	High-performance Embedded Workshop Ver.4.03.00
C/C++ compiler	H8S, H8/300 SERIES C/C++ Compiler Ver.6.02.00 (manufactured by Renesas Technology)
Compiler options	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3 -speed = (register,shift,struct,expression)
Optimizing linkage editor	Optimizing Linkage Editor Ver.9.03.00 (manufactured by Renesas Technology)
Linkage editor options	None

Table 5 Section Settings

Address	Section Name	Description
H'001000	P	Program area
H'FF6000	BRAM2	Non-initialized data area (RAM area)

Table 6 Interrupt Exception Handling Vector Table

Exception Handling Source	Vector No.	Address in Vector Table	Function to Interrupt Destination
Reset	0	H'000000	init
NMI	7	H'00001C	nmi_int

5.2 List of Functions

The functions in this sample task are shown in table 7. The hierarchy of calls in the user program is shown in figure 4.

Table 7 List of Functions

Function Name	Description
init	Initialization routine Cancels the module stop, sets the clocks and calls the main function.
main	Main routine Makes initial settings of deep software standby mode, saves user data in a deep standby backup register immediately before execution of the SLEEP instruction, and then executes the SLEEP instruction.
nmi_int	NMI exception handling Routine for resolving a conflict between a transition to deep software standby mode and the NMI. For details, see section 3.2.5, Conflict between Transition to Deep Software Standby Mode and Interrupts.

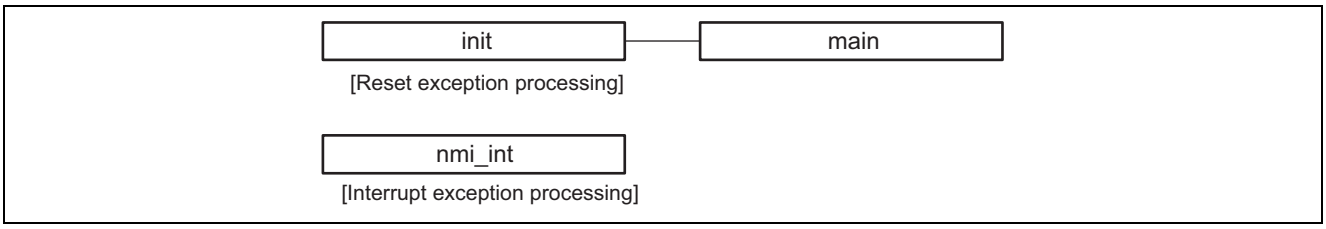


Figure 4 Hierarchy of Calls in the User Program

5.3 RAM Usage

Table 8 RAM Usage

Type	Variable Name	Description	Used in
unsigned char	userdata	User data (1 byte)	main

5.4 Description of Functions

5.4.1 init Function

1. Functional overview
   Initializes routine which releases the required modules from module stop mode, makes clock settings, and calls the main function.
2. Arguments
   None
3. Return value
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- Mode control register (MDCR) Number of bits: 16 Address:H'FFFDC0

Bit	Bit Name	Setting	R/W	Description
11	MDS3	—*	R	Mode Select 3 to 0
10	MDS2	—*	R	Indicate the operating mode selected by the mode pins (MD2 to MD0) (see table 9). When MDCR is read, the signal levels input on pins MD2 to MD0 are latched into these bits. These latches are released by a reset.
9	MDS1	—*	R	
8	MDS0	—*	R	

Note: *These values depend on the settings for pins MD3 to MD0.

Table 9 Settings of Bits MDS3 to MDS0

MCU Operating Mode	Pin			MDCR			
	MD2	MD1	MD0	MDS3	MDS2	MDS1	MDS0
1	0	0	1	1	1	0	1
2	0	1	0	1	1	0	0
3	0	1	1	0	1	0	0
4	1	0	0	0	0	1	0
5	1	0	1	0	0	0	1
6	1	1	0	0	1	0	1
7	1	1	1	0	1	0	0

- System clock control register (SCKCR) Number of bits: 16 Address:H'FFFDC4

Bit	Bit Name	Setting	R/W	Description
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	Select the frequency of the system clock provided to the CPU,
8	ICK0	1	R/W	EXDMAC, DMAC, and DTC. 001: Input clock × 2
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	Select the frequency of the peripheral module clock.
4	PCK0	1	R/W	001: Input clock × 2
2	BCK2	0	R/W	External-bus Clock (Bϕ) Select
1	BCK1	0	R/W	Select the frequency of the external bus clock.
0	BCK0	1	R/W	001: Input clock × 2

- MSTPCRA, MSTPCRB and MSTPCRC control the module stop mode. Setting a bit to 1 places the corresponding module in module stop mode, while clearing the bit to 0 releases the module from module stop mode.

- Module stop control register A (MSTPCRA) Number of bits: 16 Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Description
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable Enables/disables all-module-clock-stop state for reducing current consumption by stopping the bus controller and I/O ports operations when the CPU executes the SLEEP instruction after module stop state has been set for all the on-chip peripheral modules controlled by MSTPCR. 0: All-module-clock-stop mode disabled 1: All-module-clock-stop mode enabled
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timer unit (TMR_3, TMR_2)
8	MSTPA8	1	R/W	8-bit timer unit (TMR_1, TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
1	MSTPA1	1	R/W	16-bit timer pulse unit (TPU channels 11 to 6)
0	MSTPA0	1	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

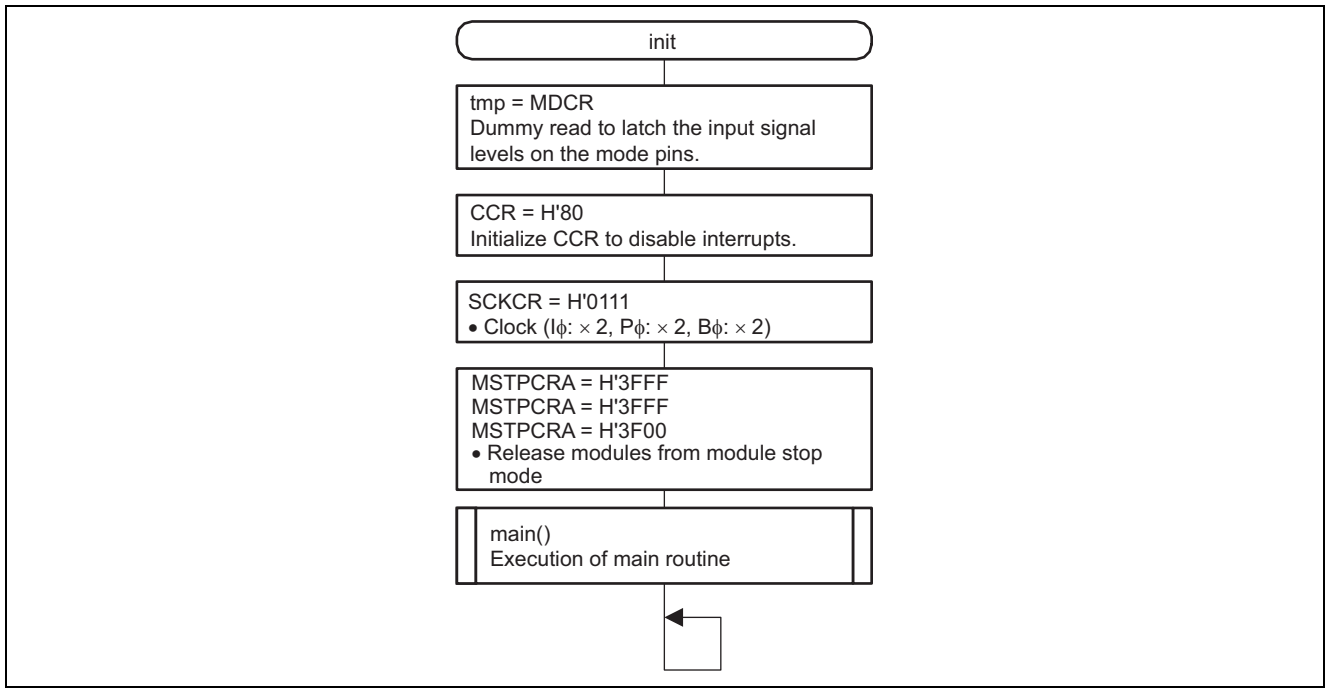
- Module stop control register B (MSTPCRB) Number of bits: 16 Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Description
15	MSTPB15	1	R/W	Programmable pulse generator (PPG_0: PO15 to PO0)
12	MSTPB12	1	R/W	Serial communications interface_4 (SCI_4)
11	MSTPB11	1	R/W	Serial communications interface_3 (SCI_3)
10	MSTPB10	1	R/W	Serial communications interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communications interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial communications interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus interface 2_1 (IIC2_1)
6	MSTPB6	1	R/W	I^2C bus interface 2_0 (IIC1_0)
5	MSTPB5	1	R/W	User break controller (USC)

- Module stop control register C (MSTPCRC) Number of bits: 16 Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Description
15	MSTPC15	1	R/W	Serial communications interface_5 (SCI_5), (IrDA)
14	MSTPC14	1	R/W	Serial communications interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timer unit (TMR_4, TMR_5)
12	MSTPC12	1	R/W	8-bit timer unit (TMR_6, TMR_7)
10	MSTPC10	1	R/W	Cyclic redundancy check module
9	MSTPC9	1	R/W	A/D converter (unit 1)
8	MSTPC8	1	R/W	Programmable pulse generator (PPG_1: PO31 to PO16)
7	MSTPC7	0	R/W	On-chip RAM_6 (H'FEE000 to H'FEFFFF)
6	MSTPC6	0	R/W	Always set the MSTPC7 and MSTPC6 to the same value.
5	MSTPC5	0	R/W	On-chip RAM_5 and RAM_4 (H'FF0000 to H'FF3FFF)
4	MSTPC4	0	R/W	Always set the MSTPC5 and MSTPC4 to the same value.
3	MSTPC3	0	R/W	On-chip RAM_3 and RAM_2 (H'FF4000 to H'FF7FFF)
2	MSTPC2	0	R/W	Always set the MSTPC3 and MSTPC2 to the same value.
1	MSTPC1	0	R/W	On-chip RAM_1 and RAM_0 (H'FF8000 to H'FFBFFF)
0	MSTPC0	0	R/W	Always set the MSTPC1 and MSTPC0 to the same value.

5. Flowchart



5.4.2 main Function

1. Functional overview
   Main routine which makes initial settings for the deep software standby mode and saves user data in a deep standby backup register immediately before execution of the SLEEP instruction. It then executes the SLEEP instruction.
2. Arguments
   None
3. Return value
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- Deep standby backup register 0 (DPSBKR0) Number of bits: 8 Address: H'FFFBF0

  DPSBKRn (n = 15 to 0) is initialized by a reset signal on the $\overline{\text{RES}}$ pin but is not initialized by the internal reset signal upon exit from the deep software standby mode.

  Function: DPSBKRn (n = 15 to 0) is a 16-byte readable/writable register to store data during deep software standby mode. DPSBKR0 (1 byte) is used in this sample task.

  Set value: userdata

- Standby control register (SBYCR) Number of bits: 16 Address: H'FFFDC6

Bit	Bit Name	Setting	R/W	Description
15	SSBY	0	R/W	Software Standby Specifies the transition mode after executing the SLEEP instruction. 0: Enters sleep mode after execution of the SLEEP instruction. 1: Enters software standby mode after execution of the SLEEP instruction. This bit does not change to 0 when clearing the software standby mode by using interrupts and shifting to normal operation. For clearing, write 0 to this bit. When the WDT is used in watchdog timer mode, the setting of this bit is disabled. In this case, a transition is always made to sleep mode or all-module-clock-stop mode after the SLEEP instruction is executed. When the SLPIE bit is set to 1, this bit should be cleared to 0.

- Deep standby control register (DPSBYCR) Number of bits: 8 Address: H'FFFE70
  DPSBYCR is initialized by a reset signal on the $\overline{\text{RES}}$ pin but is not initialized by the internal reset signal upon exit from the deep software standby mode.

Bit	Bit Name	Setting	R/W	Description
7	DPSBY	1	R/W	Deep Software Standby When the SSBY bit in SBYCR has been set to 1, executing the SLEEP instruction causes a transition to software standby mode. At this time, if there is no source to clear software standby mode and this bit is set to 1, a transition to deep software standby mode is made. 0x: Enters sleep mode after execution of a SLEEP instruction. 10: Enters software standby mode after execution of a SLEEP instruction. 11: Enters deep software standby mode after execution of a SLEEP instruction. When deep software standby mode is released due to an external interrupt, this bit remains at 1. Write a 0 here to clear it. Setting of this bit has no effect when the WDT is used in watchdog timer mode. In this case, executing the SLEEP instruction always initiates entry to sleep mode or all-module-clock-stop mode. Be sure to clear this bit to 0 when setting the SLPIE bit to 1.
6	IOKEEP	0	R/W	I/O Port Retention In deep software standby mode, the ports retain the states that were held in software standby mode. This bit specifies whether or not the state that has been held in deep software standby mode is retained after exit from deep software standby mode. 0: The retained port states are released simultaneously with exit from deep software standby mode. 1: The retained port states are released when a 0 is written to this bit following exit from deep software standby mode. In operation in external extended mode, however, the address bus, bus control signals ($\overline{\text{CS0}}$, $\overline{\text{AS}}$, $\overline{\text{RD}}$, $\overline{\text{HWR}}$, and $\overline{\text{LWR}}$), and data bus are set to the initial state upon exit from deep software standby mode.
5	RAMCUT2	1	R/W	On-chip RAM Power Off 2
4	RAMCUT1	1	R/W	On-chip RAM Power Off 1
0	RAMCUT0	1	R/W	On-chip RAM Power Off 0 Controls the internal power supply to the on-chip RAM areas 3 to 0 in deep software standby mode in combination with RAMCUT2 and RAMCUT1. 000: Power is supplied to the on-chip RAM areas 3 to 0 (H'FF4000 to H'FFBFFF). 111: Power is not supplied to the on-chip RAM areas 3 to 0 (H'FF4000 to H'FFBFFF).

- Deep standby wait control register (DPSWCR) Number of bits: 8 Address: H'FFFE71

  DPSWCR is initialized by a reset signal on the $\overline{\text{RES}}$ pin but is not initialized by the internal reset signal upon exit from deep software standby mode.

Bit	Bit Name	Setting	R/W	Description
5 to 0	WTSTS5 to WTSTS0	001101	R/W	Deep Software Standby Wait Time Setting Select the time for which the MCU waits until the clock settles when deep software standby mode is released by an external interrupt. During the oscillation settling period, counting is performed with the clock frequency input to the EXTAL. 001101: Wait time = 131072 states (CPU cycles)

- Deep standby interrupt flag register (DPSIFR) Number of bits: 8 Address: H'FFFE73

  DPSIFR is initialized by input of the reset signal on the $\overline{\text{RES}}$ pin but is not initialized by the internal reset signal upon exit from deep software standby mode.

Bit	Bit Name	Setting	R/W	Description
7	DNMIF	0	R/W	NMI Flag [Setting condition] Generation of NMI input specified in DPSIEGR [Clearing condition] Writing a 0 to this bit after reading it as 1

- Deep standby interrupt edge register (DPSIEGR) Number of bits: 8 Address: H'FFFE74

  DPSIEGR is initialized by a reset signal on the $\overline{\text{RES}}$ pin but is not initialized by the internal reset signal upon exit from deep software standby mode

Bit	Bit Name	Setting	R/W	Description
7	DNMIEG	0	R/W	NMI Edge Select Selects the active edge for NMI pin input. 0: The interrupt request is generated by a falling edge. 1: The interrupt request is generated by a rising edge.

- Reset status register (RSTSR) Number of bits: 8 Address: H'FFFE75

  RSTSR is initialized by a reset signal on the $\overline{\text{RES}}$ pin but is not initialized by the internal reset signal upon exit from deep software standby mode

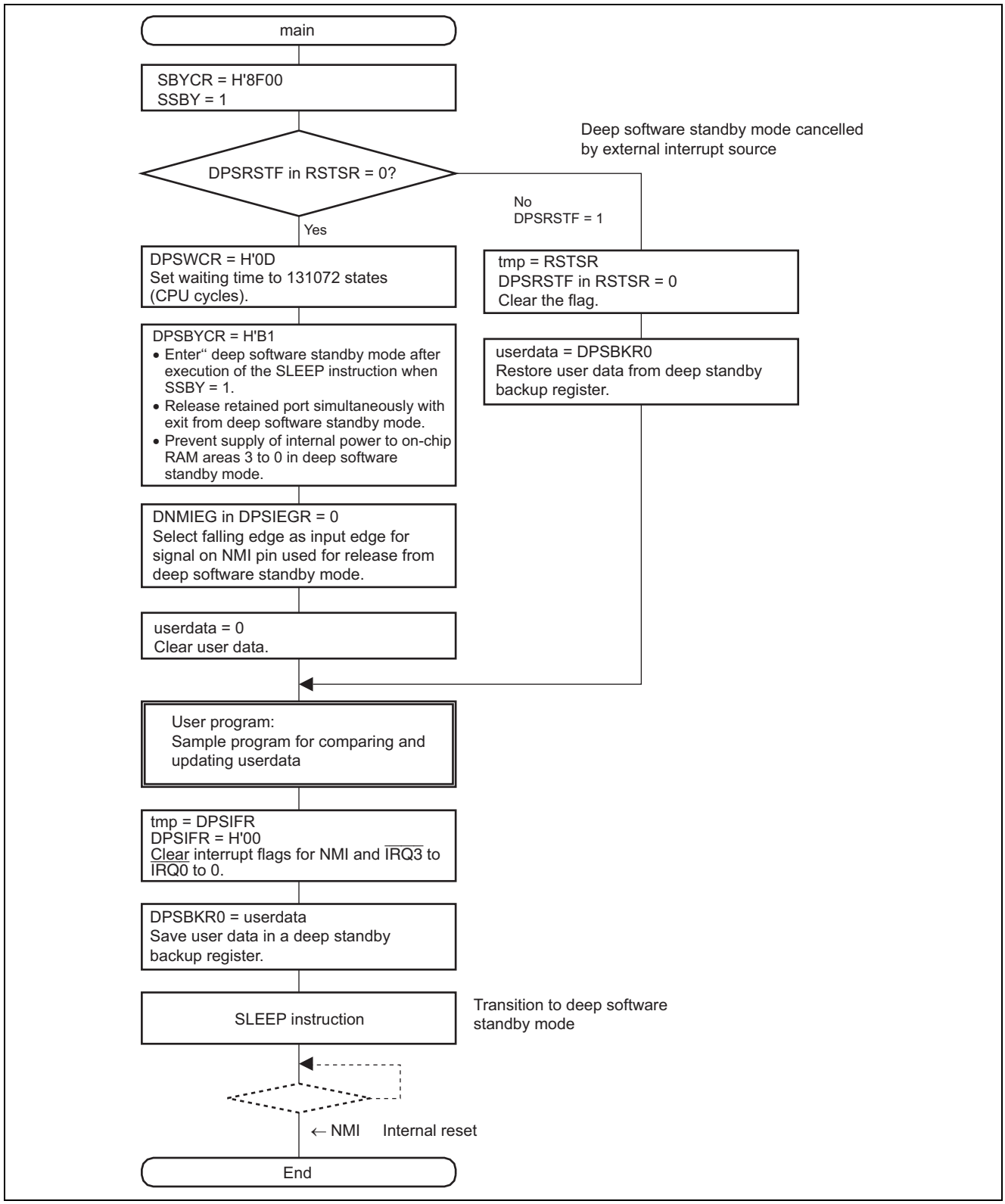
Bit	Bit Name	Setting	R/W	Description
7	DPSRSTF	0	R/(W)*	Deep Software Standby Reset Flag Indicates that deep software standby mode has been released by an external interrupt source specified in DPSIER or DPSIEGR and an internal reset is generated. [Setting condition] Release of deep software standby mode by an external interrupt source. [Clearing condition] Writing a 0 to this bit after reading it as 1

Note: Only 0 can be written to clear the flag.

- Port 3 data register (P3DR) Number of bits: 8 Address: H'FFFF52

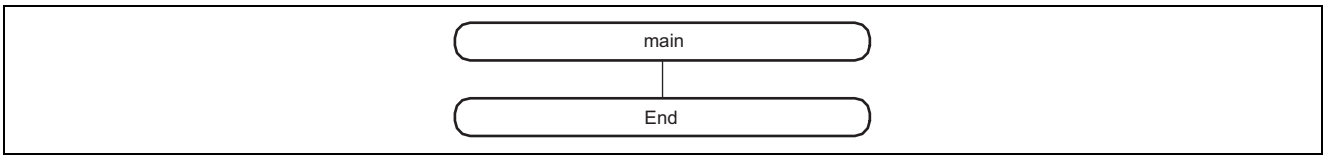
Bit	Bit Name	Setting	R/W	Description
2	P32DR	0	R/W	0: The P32 pin is set to a low level. 1: The P32 pin is set to a high level.
1	P31DR	0	R/W	0: The P31 pin is set to a low level. 1: The P31 pin is set to a high level.
0	P30DR	0	R/W	0: The P30 pin is set to a low level. 1: The P30 pin is set to a high level.

5. Flowchart


main
SBYCR = H'8F00
SSBY = 1
DPSRSTF in RSTSR = 0?
Deep software standby mode cancelled by external interrupt source
No
DPSRSTF = 1
Yes
DPSWCR = H'0D
Set waiting time to 131072 states (CPU cycles).
tmp = RSTSR
DPSRSTF in RSTSR = 0
Clear the flag.
DPSBYCR = H'B1
• Enter" deep software standby mode after execution of the SLEEP instruction when SSBY = 1.
• Release retained port simultaneously with exit from deep software standby mode.
• Prevent supply of internal power to on-chip RAM areas 3 to 0 in deep software standby mode.
userdata = DPSBKR0
Restore user data from deep standby backup register.
DNMIEG in DPSIEGR = 0
Select falling edge as input edge for signal on NMI pin used for release from deep software standby mode.
userdata = 0
Clear user data.
User program:
Sample program for comparing and updating userdata
tmp = DPSIFR
DPSIFR = H'00
Clear interrupt flags for NMI and IRQ3 to IRQ0 to 0.
DPSBKR0 = userdata
Save user data in a deep standby backup register.
SLEEP instruction
Transition to deep software standby mode
← NMI
Internal reset
End

5.4.3 nmi_int Function

1. Functional overview
   Handles NMI exceptions. It is required as a measure in case of conflict between a transition to deep software standby mode and the NMI. For details, see section 3.2.5, Conflict between Transition to Deep Software Standby Mode and Interrupts.
2. Arguments
   None
3. Return value
   None
4. Description of internal registers used
   None
5. Flowchart



6. Documents for Reference

- Hardware Manual
  H8SX/1638 Group Hardware Manual
  (The most up-to-date version of this document is available on the Renesas Technology Website.)
- Technical News/Technical Update
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