Application Note

DA9062 / Atlas7 Power Connections

AN-PM-083

Abstract

This document outlines the connectivity between the Dialog DA9062 Power Management Integrated Circuit (PMIC) and Qualcomm® Atlas7™ system processor.

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1 Terms and Definitions

GUI	Graphical User Interface
Atlas7	Qualcomm CSRatlas7™ SoC, formerly known as SiRFatlas7™
SoC	System on a Chip
PMIC	Power Management Integrated Circuit
PWRC	Power Controller

2 References

[1] DA9062, Datasheet, Dialog Semiconductor

[2] SiRFatlas7, http://www.csr.com/tw/node/6376i [Accessed 01-Nov-2016]

[3] The Linux Kernel Archives, https://kernel.org/ [Accessed 13-Sep-2016]

3 Introduction

This document provides details of integrating the DA9062 with the CSRatlas7 (‘Atlas7’) SoC [2], suitable for highly-integrated display audio solutions.

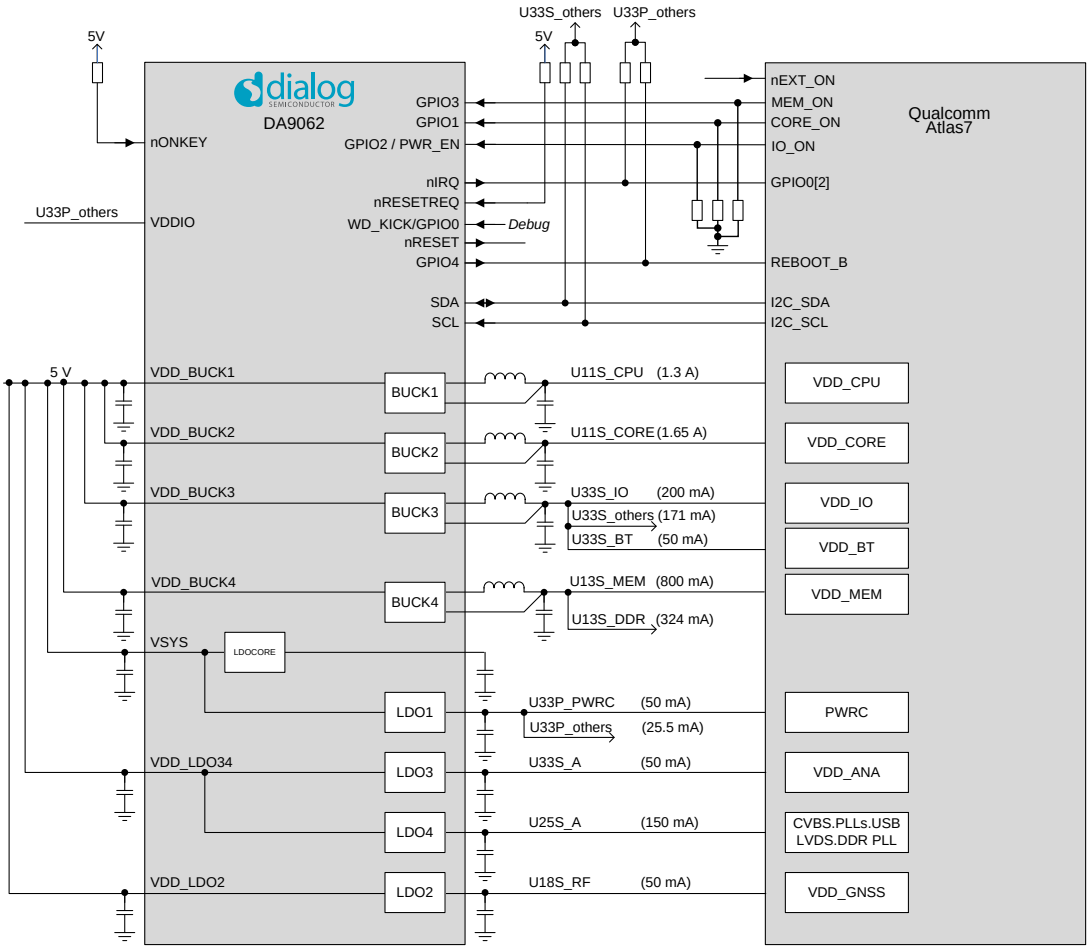

Figure 1: Qualcomm Atlas7 Platform

Note 1 The WD_KICK/GPIO0 input requires a pulse every 2 s (as set by register control TWDSCALE). Alternatively, by setting register control WDG_MODE=’1’, the input can be permanently asserted using a pull-up to U33S_others. This may be useful during application debugging.

Note 2 DA9062 nONKEY is not used. System start-up is initiated by nEXT_ON.

Note 3 nRESET is not used.

DA9062 / Atlas7 Power Connections

Table 1: GPIO Mapping for Atlas7

GPIO	Function	Description
GPIO0	WD_KICK	Watchdog kick – for debug
GPIO1	CORE_ON	Active-high GPI enables Buck1 and Buck2
GPIO3	MEM_ON	Active-high GPI enables Buck4
GPIO4	REBOOT_B	Reboots processor, including the PWRC block. Active-low. GPIO4 is configured as an open-drain output. (External pull-up used to avoid reliance on 'soft' configuration of PMIC internal pull-up.) On power-up, the signal is driven a steady high. This allows the PWRC to start up. The signal remains high unless there is a watchdog timeout. On a watchdog timeout, the PMIC powers down through the sequence. The sequence is modified by the PMIC itself at the beginning of the power-down so that a high-low-high pulse is created on GPIO4. (The pulse is defined by controls GP_RISE5_STEP and GP_FALL5_STEP).
GPIO2 / PWR_EN	IO_ON	Enables the LDOs and Buck3 via the sequencer. GPIO2 is configured as an active-high input.

The GPIOs configured as outputs can be supplied internally from VDDIO and driven with a push-pull stage, or with an open-drain stage with an optional internal pull-up to VDDIO. Similarly, nIRQ and nRESET can be driven with a push-pull or with an open-drain stage but an external pull-up is required (as shown in Figure 1). The PMIC nRESET line is not used in this application.

4 Timing Diagrams

4.1 Cold Boot

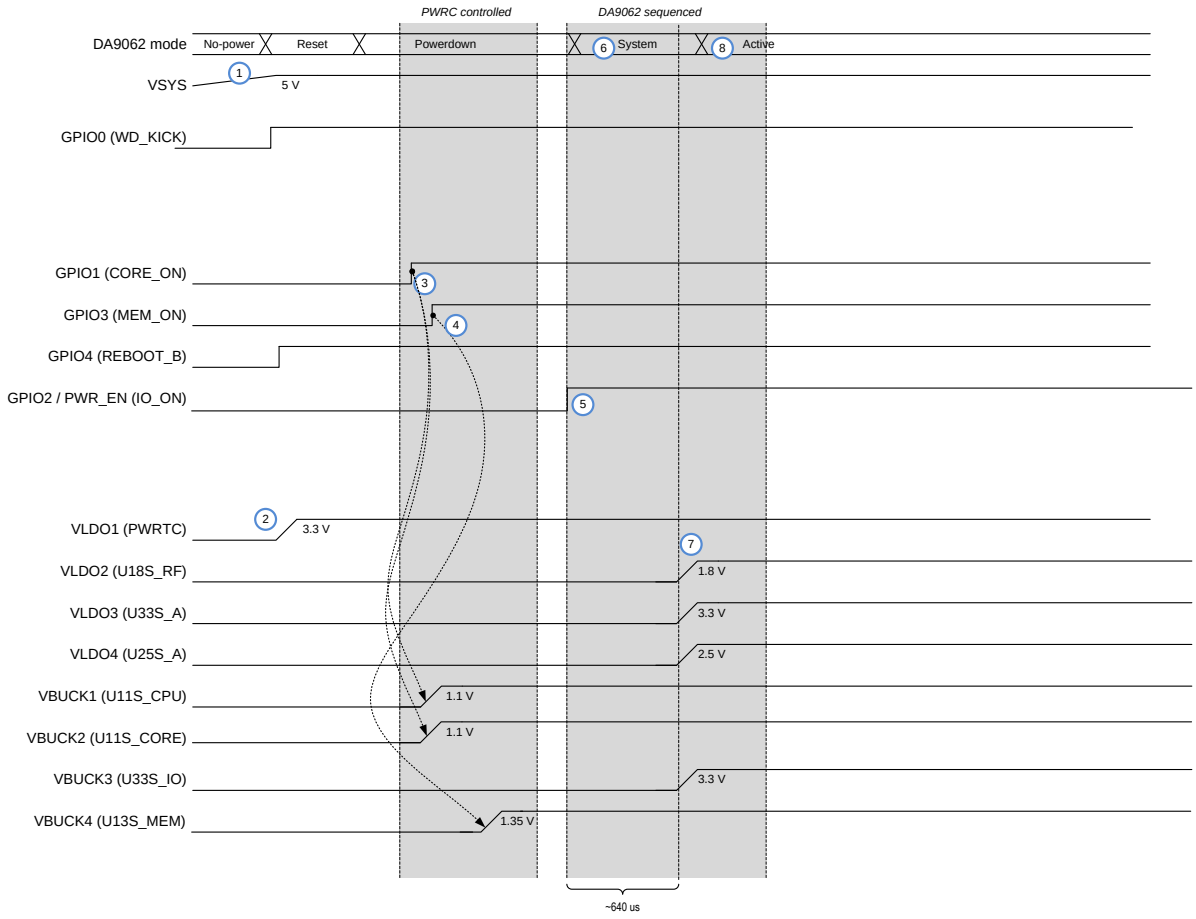

Figure 2: Timing Diagram for Cold Boot

1. The system supply rises above a threshold value after which the internal digital core supply of DA9062 is enabled and the device enters RESET mode. It then automatically proceeds to POWERDOWN mode.
2. The always-on supply LDO1 (U33P_PWRC) is enabled while the device is in RESET mode.
3. With U33P_PWRC powered up, the Atlas7 PWRC asserts GPIO1 (CORE_ON). CORE_ON directly enables Buck1 (U11S_CPU) and Buck2 (U11S_CORE). This is therefore asynchronous to the DA9062 start-up sequence.
4. The Atlas7 PWRC asserts GPIO3 (MEM_ON) which directly enables Buck4 (U13S_MEM). This is also asynchronous to the DA9062 start-up sequence.
5. The Atlas7 PWRC asserts IO_ON which drives GPIO2 configured as PWR_EN. The assertion of this signal causes the DA9062 to wake up from POWERDOWN mode.
6. The DA9062 executes the power-up sequence. It firstly passes through the SYSTEM state without any changes to the supplies.
7. The power-up sequencer continues. The DA9062 turns on LDO2 (U18S_RF), LDO3 (U33S_A), LDO4 (U25S_A) and VBUCK3 (U33S_IO).
8. The sequencer continues and the PMIC reaches ACTIVE mode. The watchdog kick on GPIO0 (WD_KICK) must be asserted for the PMIC to reach ACTIVE mode.

4.2 Power-Down / Suspend by Atlas7

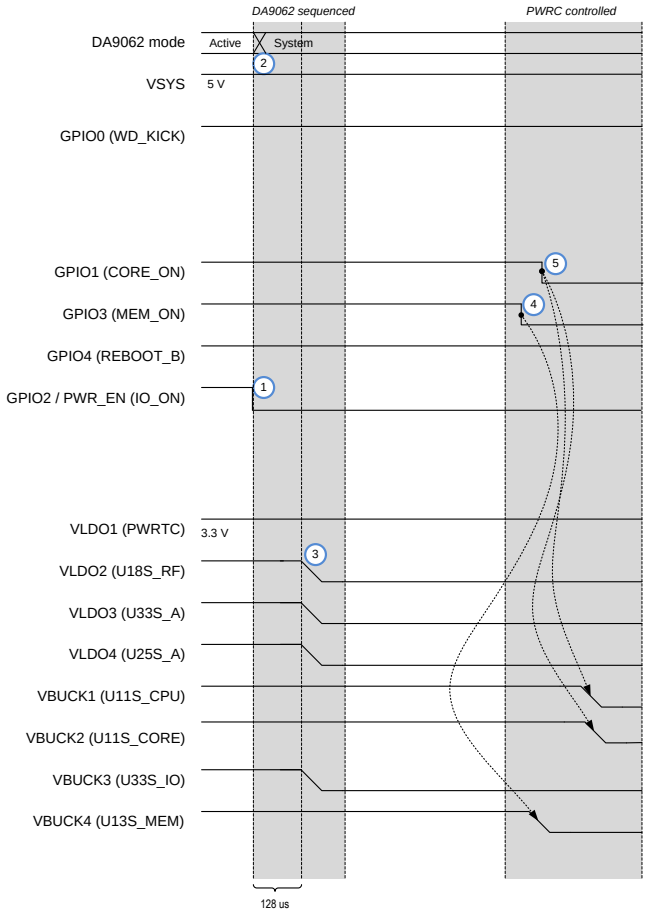

Figure 3: Timing Diagram for Power Down by Atlas7

This sequence shows a system power-down controlled by the Atlas7 processor. It is similar to the cold boot sequence reversed, except that it leaves the PMIC in the SYSTEM state.

1. Atlas7 initiates the power-down by de-asserting IO_ON.
2. The de-assertion of IO_ON (PWR_EN) causes the DA9062 to begin the power-down sequence from the ACTIVE state to the SYSTEM state.
3. The sequencer includes the power-down of LDO2 (U18S_RF), LDO3 (U33S_A), LDO4 (U25S_A) and VBUCK3 (U33S_IO).
4. The Atlas7, some time later, may continue to power itself down by de-asserting MEM_ON.
5. The Atlas7, some time later, may continue to power itself down by also de-asserting CORE_ON.

4.3 Warm Boot

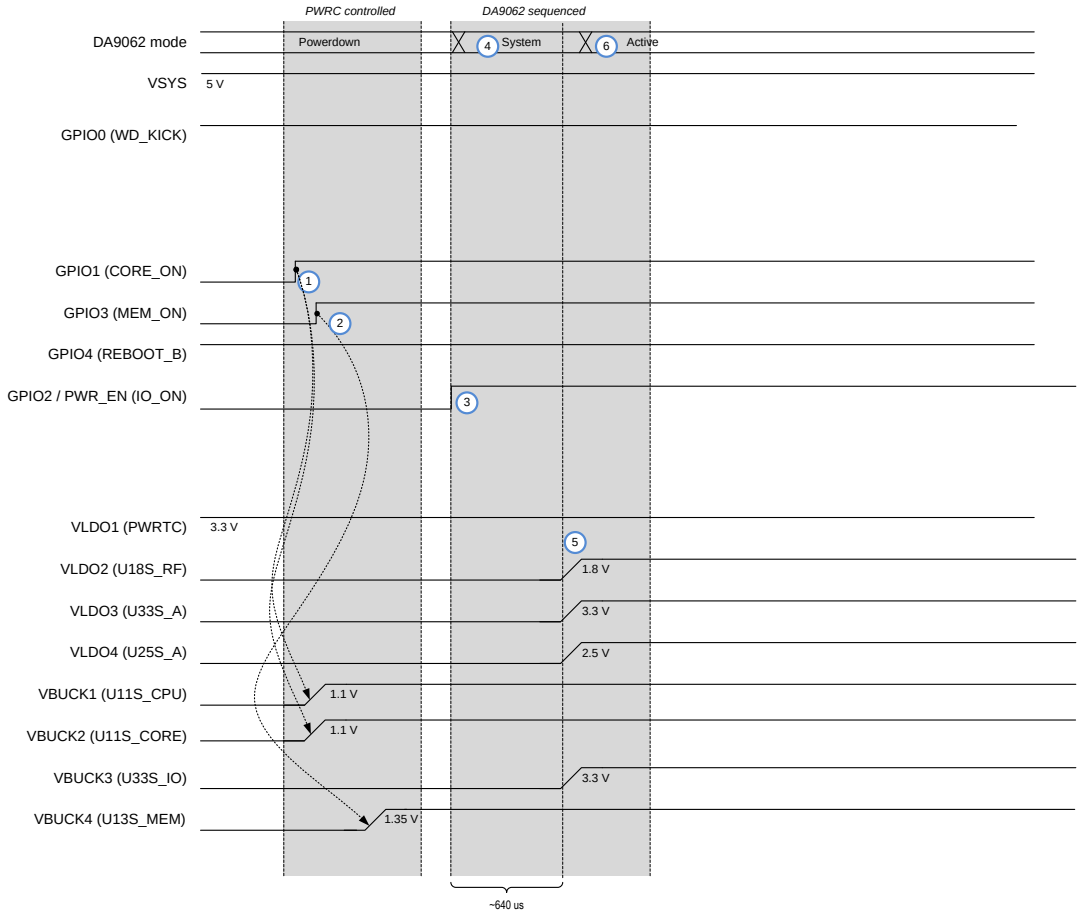

Figure 4: Timing Diagram for Warm Boot

When the DA9062 is in POWERDOWN mode, the PWRC is on but the Atlas7 core, memory and IOs are powered down. The system therefore requires a warm boot to power up again. The sequence is identical to the later portion of the cold boot sequence.

1. With the PMIC in POWERDOWN and the Atlas7 PWRC powered, the PWRC asserts GPIO1 (CORE_ON). CORE_ON directly enables Buck1 (U11S_CPU) and Buck2 (U11S_CORE). This is therefore asynchronous to the DA9062 start-up sequence.
2. The Atlas7 PWRC then asserts GPIO3 (MEM_ON) which directly enables Buck4 (U13S_MEM). This is also asynchronous to the DA9062 start-up sequence.
3. The Atlas7 PWRC then asserts IO_ON which drives GPIO2 configured as PWR_EN. The assertion of this signal causes the DA9062 to wake up from POWERDOWN mode.
4. The DA9062 executes the power-up sequence. It firstly passes through its SYSTEM state without any changes to the supplies.
5. The power-up sequencer continues. The DA9062 turns on LDO2 (U18S_RF), LDO3 (U33S_A), LDO4 (U25S_A) and VBUCK3 (U33S_IO).
6. The sequencer continues and the PMIC reaches ACTIVE mode. The watchdog kick on GPIO0 (WD_KICK) must be asserted for the PMIC to reach ACTIVE mode.

4.4 Watchdog Timeout

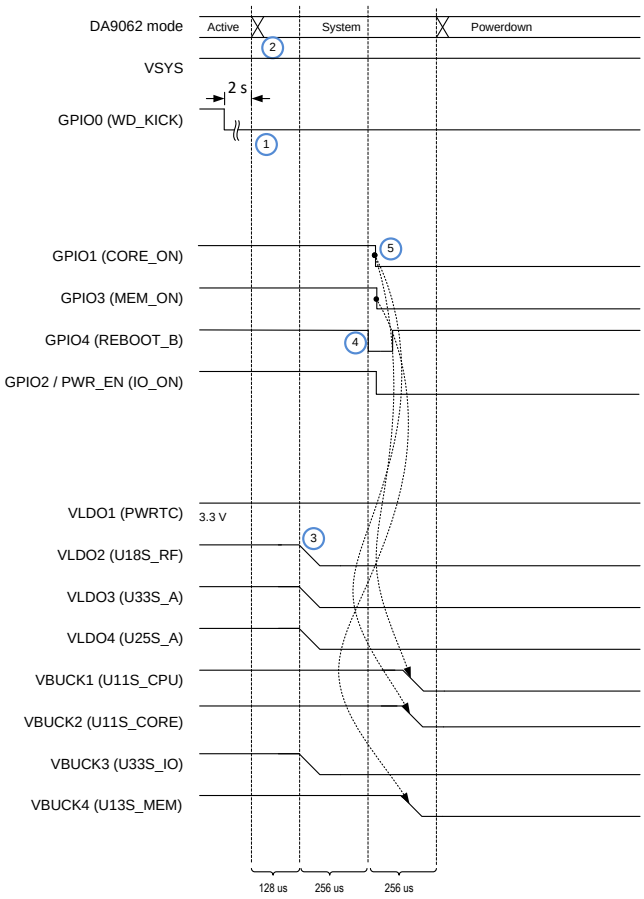

Figure 5: Timing Diagram for a Watchdog Timeout

The watchdog feature is enabled in OTP. The DA9062 requires GPIO0 (WD_KICK) to be asserted or pulsed in order to enter and maintain ACTIVE mode. If the input is not asserted within 2 s (set by control TWDSCALE), then a timeout has occurred and the system powers down by the following sequence:

1. The GPIO0 (WD_KICK) input remains de-asserted for >2 s. This initiates the watchdog timeout.
2. The DA9062 powers down through its sequence, transitioning from the ACTIVE state to the SYSTEM state.
3. The DA9062 sequence turns off LDO2 (U18S_RF), LDO3 (U33S_A), LDO4 (U25S_A) and VBUCK3 (U33S_IO).
4. The sequencer leaves the SYSTEM state and continues towards the POWERDOWN state. This part of the power-down sequence includes a low-going pulse on REBOOT_B. The pulse duration is 128 µs.
5. The REBOOT_B assertion immediately causes the Atlas7 PWRC to shut down the remaining rails by de-asserting IO_ON, MEM_ON and CORE_ON. The DA9062 therefore turns off these remaining rails.

The system passes through a reset state controlled by the Atlas7 processor. After completing its reset procedure, the system restarts.

4.5 Temperature Warning and Temperature Error

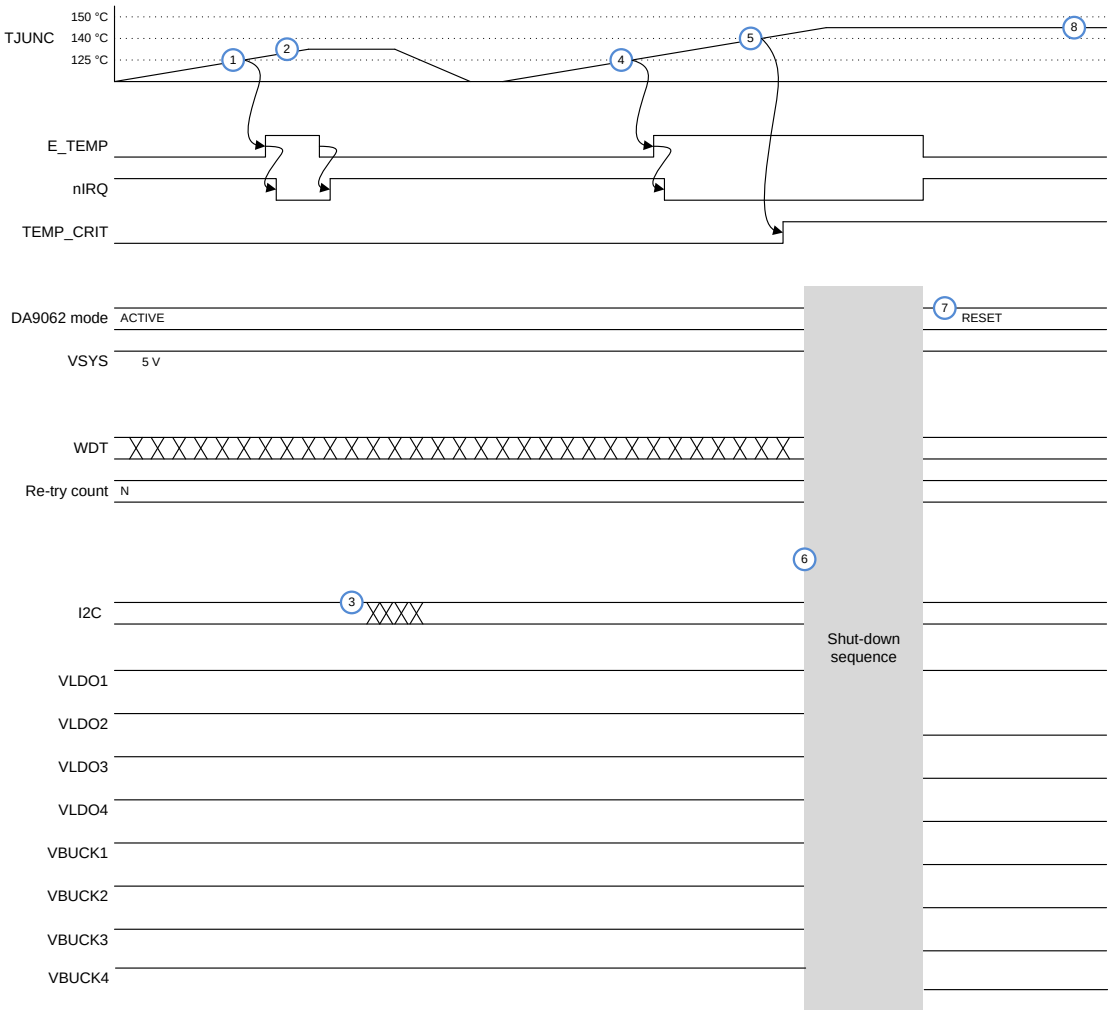

Figure 6: Timing Diagram for Temperature Warning and Temperature Error

1. The die temperature exceeds TEMP_WARN which causes the event E_TEMP to be asserted. The event, if not masked, asserts nIRQ.
2. Atlas7 software sees the temperature warning and reduces the activity of the platform.
3. Atlas7 software clears the event E_TEMP. If no other events are active, this de-asserts nIRQ.
4. The die temperature exceeds TEMP_WARN again which causes the event E_TEMP to be asserted. The event, if not masked, asserts nIRQ.
5. The die temperature exceeds TEMP_CRIT which causes the temperature error flag TEMP_CRIT to be asserted, and a shutdown sequence is triggered.
6. The DA9062 executes the shutdown sequence which is the same as the power-down sequence described in Section 4.2, although a shutdown sequence triggered by a temperature error proceeds directly to the RESET mode.
7. The DA9062 completes the shutdown sequence and enters the RESET mode. The retry count is reset, but the temperature error flag is not reset.
8. The DA9062 remains in RESET mode as long as the die temperature stays above TEMP_CRIT. After this, the power-up sequence is executed in the same way as in the cold boot, as described in Section 4.1.

4.6 System Supply Under-Voltage

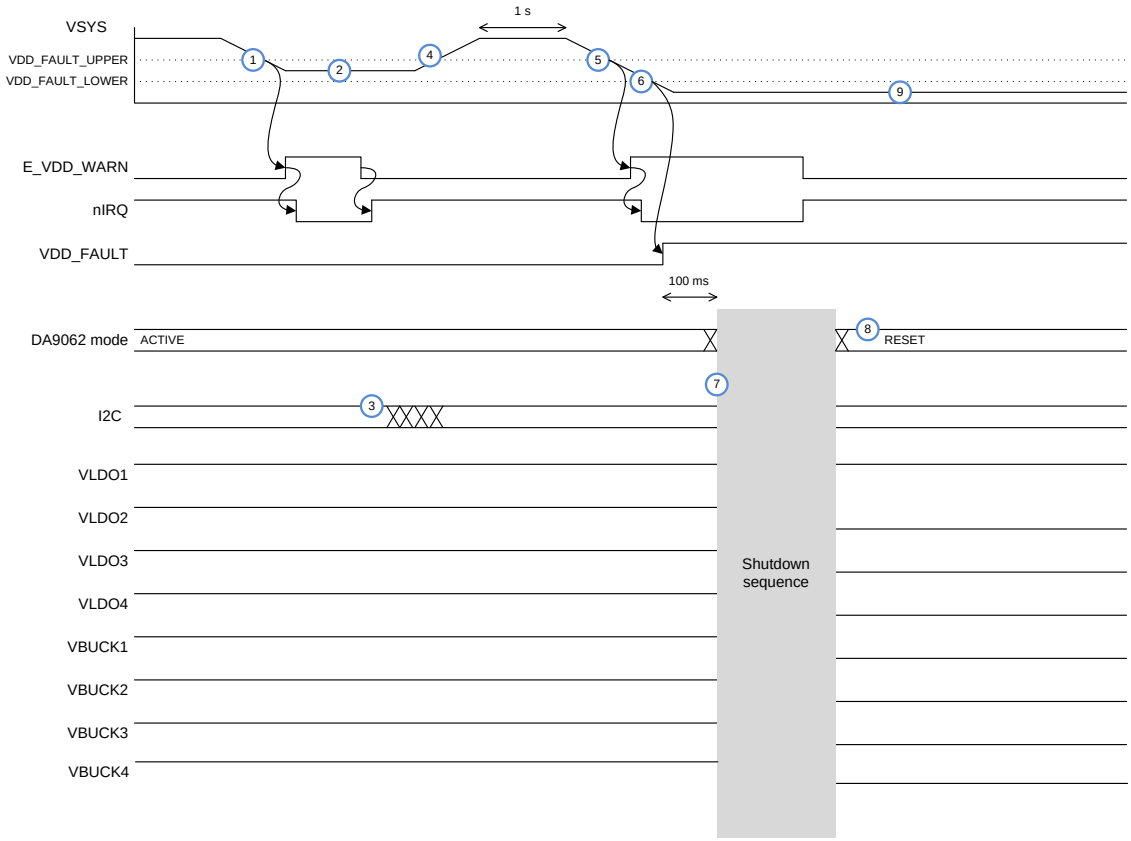

Figure 7: Timing Diagram for System Supply Under-Voltage

1. The system supply (VSYS) drops below VDD_FAULT_UPPER which causes the event E_VDD_WARN to be asserted. The event, if not masked, then asserts nIRQ.
2. Atlas7 software sees the system supply warning and reduces the activity of the platform. This should reduce the current draw of the platform and stabilize the system supply.
3. Atlas7 software clears the event E_VDD_WARN. If no other events are active, this de-asserts nIRQ.
4. The system supply recovers above the VDD_FAULT_UPPER threshold. After this, there is a 1 s debounce period for VSYS. During this period, the system supply comparators are not enabled and, if VSYS drops below VDD_FAULT_UPPER, no event is generated.
5. The system supply (VSYS) drops below VDD_FAULT_UPPER again which causes the event E_VDD_WARN to be asserted. The event, if not masked, asserts nIRQ.
6. The system supply drops below VDD_FAULT_LOWER which causes the system supply error flag VDD_FAULT to be set, and a shutdown sequence is triggered.
7. DA9062 executes a shutdown sequence which is the same as the power-down sequence described in Section 4.2, but a shutdown sequence triggered by a voltage error proceeds straight to the RESET mode.
8. DA9062 completes the shutdown sequence and enters the RESET mode. The retry count is reset, but the system supply error flag is not.
9. DA9062 stays in RESET mode as long as the system supply stays below VDD_FAULT_UPPER. After this, the power-up sequence is executed in the same way as in the cold boot described in Section 4.1.

5 Software Driver

After the DA9062 has started the Atlas 7 system, software can read and write to the PMIC via the I²C bus. This can be used for further PMIC configuration, such as the GPIOs, interrupt servicing, watchdog 'keep-alive' writes, and so on. Dialog drivers for Linux™ are available in the Linux kernel from https://kernel.org/ [3] or, if interim assistance is required, from your Dialog Sales representative.

6 Development Support Tools and PMIC Configuration Files

To assist with hardware and software development, Dialog provides the following:

- DA9062 Evaluation Kit

This contains motherboard and daughterboard for hardware evaluation and software development. It also includes the SmartCanvas™ GUI software.

- SmartCanvas GUI

This is PC-driven software to provide easy access to a device under test (DUT). The GUI is used to exercise the DUT using the I²C interface. Control or measurement of analog and digital pins is supported. SmartCanvas supports the Dialog PMIC OTP configuration file (.ini file) format.

- OTP configuration .ini file DA9062-0A_Atlas7_v01_2949.ini

This file defines the configuration of the DA9062 at boot. The file is available from the Dialog Support website. The .ini file is opened using the SmartCanvas GUI.

- Linux software driver. See Section 5.

For further information with development support tools, see the Dialog Support Site https://support.dialog-semiconductor.com/ and website http://www.dialog-semiconductor.com/.

Revision History

Revision	Date	Description
1.0	30-Nov-2016	Initial release
2.0	18-Feb-2022	File was rebranded with new logo, copyright and disclaimer

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