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H8SX Family

Counting of Two-Phase Encoder Pulse Output

Introduction

Relative phases of the two-phase pulse signal input from the two external clock pins are detected by the 16-bit timer pulse unit (TPU). Whether the timer counter counts up or down depends on the phase relation between the signals, and the timer counter value for a certain period is acquired.

Target Device

H8SX/1653, H8SX/1663

Contents

1. Specifications

Relative phases of the two-phase pulse signal input from the two external clock pins are detected by the 16-bit timer pulse unit (TPU) as shown in figure 1. The timer counter counts up or down according to the phase relation, and the timer counter value for a certain period is stored in RAM.

Relative phases of the two-phase pulse signal from an encoder is counted by configuring channel 4 of the TPU in phase counting mode and using channel 3 to measure a specific period.

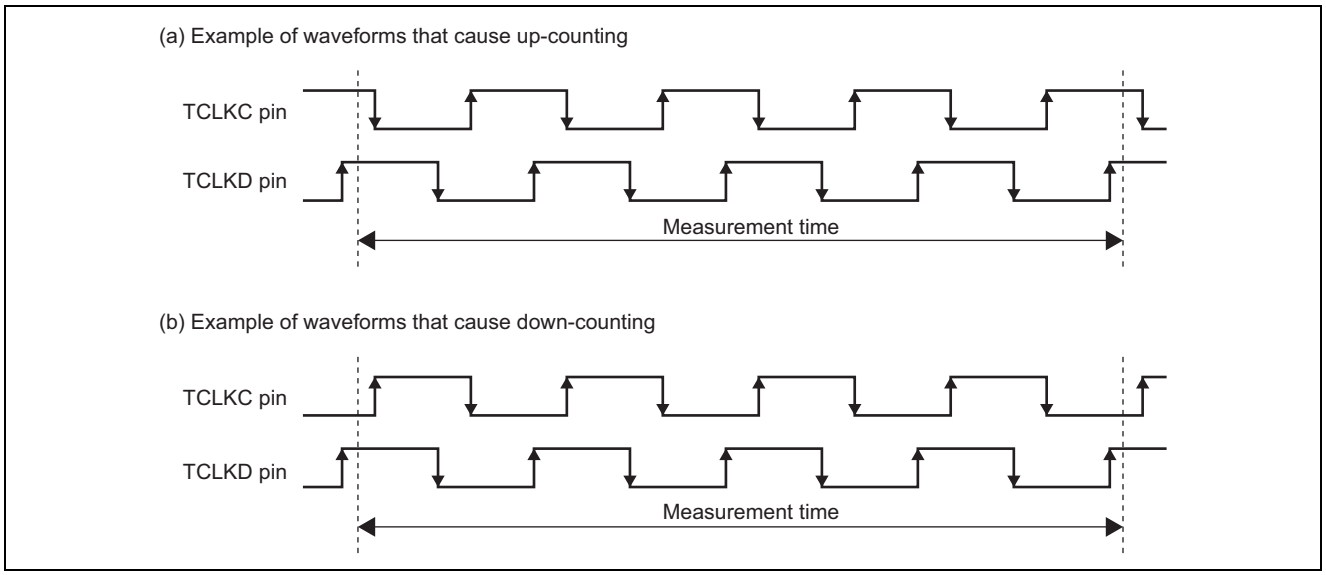


Figure 1 Counting of Two-Phase Encoder Pulse Output

2. Conditions for Application

Table 1 Conditions for Application

Item	Contents
Operating frequency	Input clock: 12 MHz System clock (Iϕ): 48 MHz Peripheral module clock (Pϕ): 24 MHz External bus clock (Bϕ): 48 MHz
Operating mode	Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0)
Development tool	High-performance Embedded Workshop Version 4.00.03
C/C++ compiler	H8S, H8/300 SERIES C/C++ Compiler Version 6.01.01 (from Renesas Technology Corp.)
Compile option	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3, -speed = (register, shift, struct, expression)

Table 2 Section Settings

Address	Section Name	Description
H'001000	P	Program area
H'FF2000	B	Non-initialized data area (RAM area)

3. Description of Modules Used

3.1 Description of TPU_3 and TPU_4 Functions

Channel 4 (TPU_4) of the TPU is used in phase counting mode 1. In this case, the external input clock pins used are TCLKC and TCLKD. Relative phases of the two-phase pulse signal input from TCLKC and TCLKD are detected and the timer counter of TPU_4 is incremented or decremented accordingly. Channel 3 (TPU_3) of the TPU is used to provide a certain time period for the measurement of the two-phase pulse signal form an encoder. Upon compare match on TPU_3, which is configured to occur after a measurement period has elapsed, the TPU_4 timer counter value is transferred to the corresponding general register. The timer counter value transferred to the general register is obtained as the result of two-phase encoder pulse counting.

Figure 2 shows a block diagram. The TPU registers are described below.

- Timer start register (TSTR)
  TSTR starts or stops TCNT operation for channels 0 to 5. Before setting the operating mode in TMDR or setting the TCNT counter clock in TCR, counting by TCNT should be stopped.

- Timer control register_3, _4 (TCR_3, TCR_4)
  TCR controls the TCNT on each channel. The TPU has a total of six TCR registers, one for each channel. TCR register settings should be made only while TCNT operation is stopped.

- Timer I/O control register H_3, timer I/O control register_4 (TIORH_3, TIOR_4)
  TIOR controls timer general registers (TGR). The TPU has eight TIOR registers, two each for channels 0 and 3, and one each for channels 1, 2, 4, and 5. Care is required since TIOR is affected by the TMDR setting.
  The initial output specified by TIOR is applied while the counter is stopped (the CST bit in TSTR is cleared to 0). In PWM mode 2, TIOR specifies the output at the point when the counter is cleared to 0.
  When TIOR is set to specify TGRC or TGRD for buffer operation, the above setting becomes invalid and the TGR register operates as a buffer register.
  When TIOR is set to configure an input capture function, the DDR and ICR bits for the corresponding pin should be set to 0 and 1, respectively.

- Timer counter_3, _4 (TCNT_3, TCNT_4)
  TCNT is a 16-bit readable/writable counter. The TPU has six TCNT counters, one for each channel. TCNT is initialized to H'0000 by a reset or in hardware standby mode. TCNT cannot be accessed in 8-bit units and must always be accessed in 16-bit units.

- Timer general register A_3, A_4 (TGRA_3, TGRA_4)
  TGR is a 16-bit readable/writable register that can be used as either an output-compare or input-capture register. The TPU has 16 general registers, four each for channels 0 and 3, and two each for channels 1, 2, 4, and 5. TGRC and TGRD for channels 0 and 3 can also be designated as buffer registers. TGR cannot be accessed in 8-bit units and must always be accessed in 16-bit units. Combinations of TGR and buffer register in buffer operation are TGRA−TGRC and TGRB−TGRD.

- Timer mode register_4 (TMDR_4)
  TMDR sets the operating mode for each channel. TPU_4 is set in phase counting mode 1 in this sample task.

- Timer interrupt enable register_4 (TIER_4)
  TIER controls enabling or disabling of interrupt requests on each channel.

- Timer status register_4 (TSR_4)
  TSR indicates the statuses of each channel.

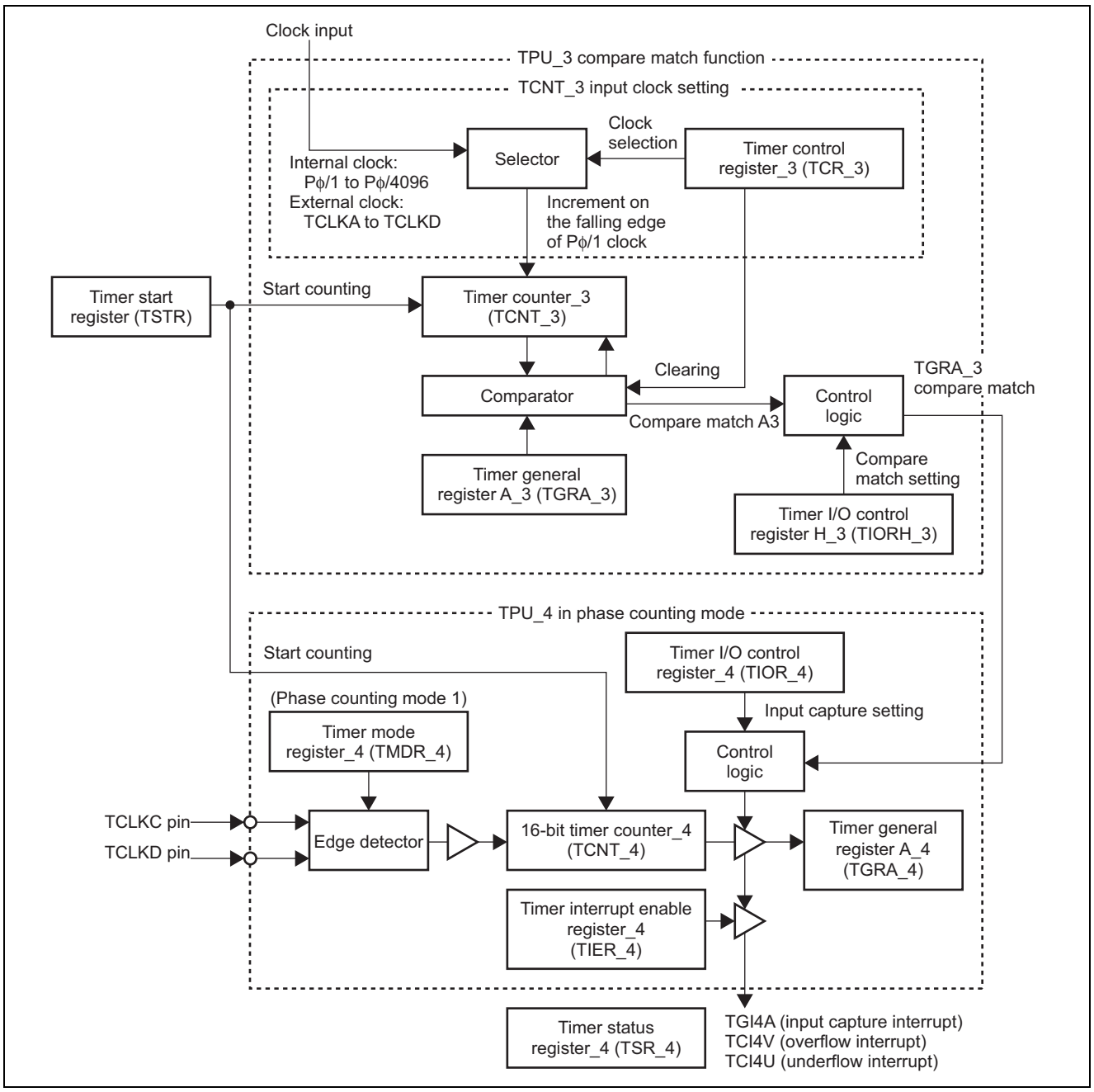


Figure 2 Block Diagram of Two-Phase Encoder Pulse Counting

3.2 Example of Phase Counting Mode 1 Operation

In phase counting mode, relative phases between the two signals on the external clock input pins are detected, and TCNT is incremented/decremented accordingly. There are four phase counting modes that use different counting conditions. Phase counting mode 1 is used in this sample task. Figure 3 shows an example of phase counting mode 1 operation, and table 3 summarizes the TCNT up/down-counting conditions.

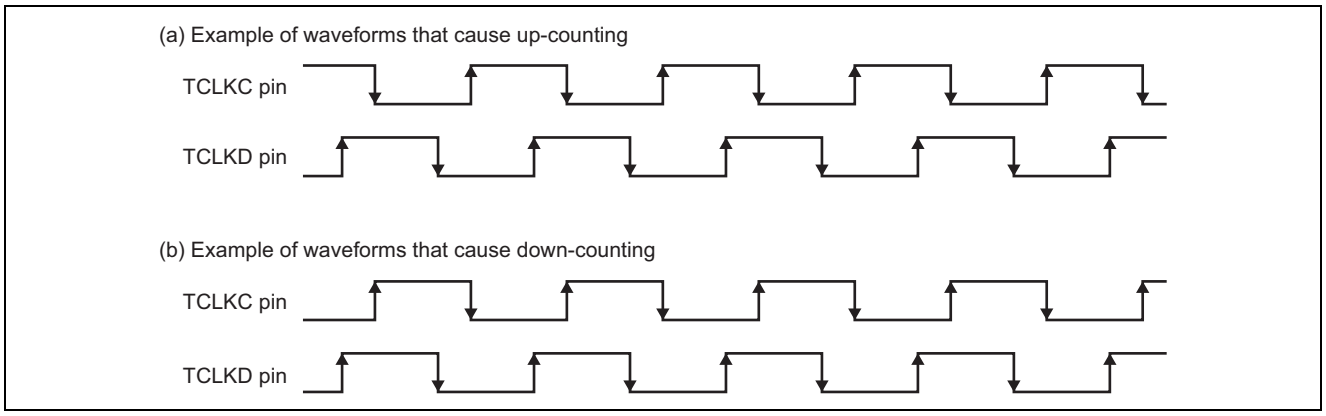


Figure 3 Example of Phase Counting Mode 1 Operation

Table 3 Up/Down-Counting Conditions for Phase Counting Mode 1

TCLKC	TCLKD	Operation
High level	Rising edge	Up-counting
Low level	Falling edge	
Rising edge	Low level	
Falling edge	High level	
High level	Falling edge	Down-counting
Low level	Rising edge	
Rising edge	High level	
Falling edge	Low level	

4. Description of Operation

4.1 Example of Up-Counting Operation

Figure 4 illustrates the up-counting operation for the two-phase pulse signal from an encoder. The hardware processing and software processing of figure 4 are explained in table 4.

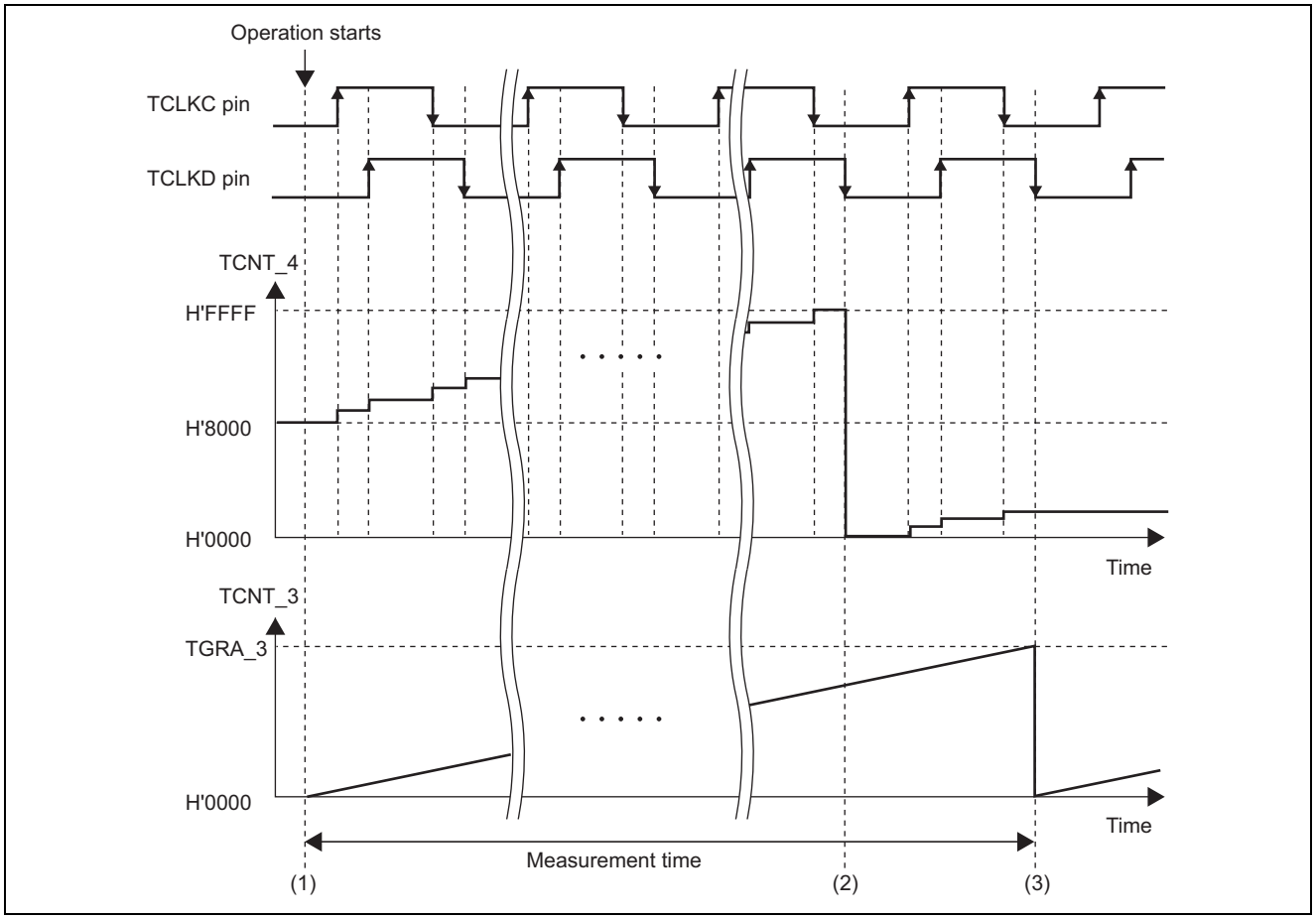


Figure 4 Example of Up-Counting Operation with Two-Phase Encoder Pulse Signal

Table 4 Hardware and Software Processing

	Hardware Processing	Software Processing
(1)	No processing	Initial settings: (a) Set the measurement time in TGRA_3 of TPU_3. (b) Put TPU_4 in phase counting mode 1. (c) Perform input capture of TGRA_4 on compare match with TGRA_3. (d) Load TCNT_4 with the initial value H'8000. (e) Set up the interrupts. (f) Start counting by TCNT_3 and TCNT_4.
(2)	(a) Generate an overflow interrupt (TCI4V).	TCI4V interrupt processing (a) Set the error flag.
(3)	(a) Transfer the TCNT_4 value to TGRA_4. (b) Generate a TGRA_4 input capture interrupt (TGI4A).	TGI4A interrupt processing (a) Store the value of TGRA_4 (result of two-phase encoder pulse counting) in RAM (tcnt).

4.2 Example of Down-Counting Operation

Figure 5 illustrates the down-counting operation for the two-phase pulse signal from an encoder. The hardware processing and software processing of figure 5 are explained in table 5.

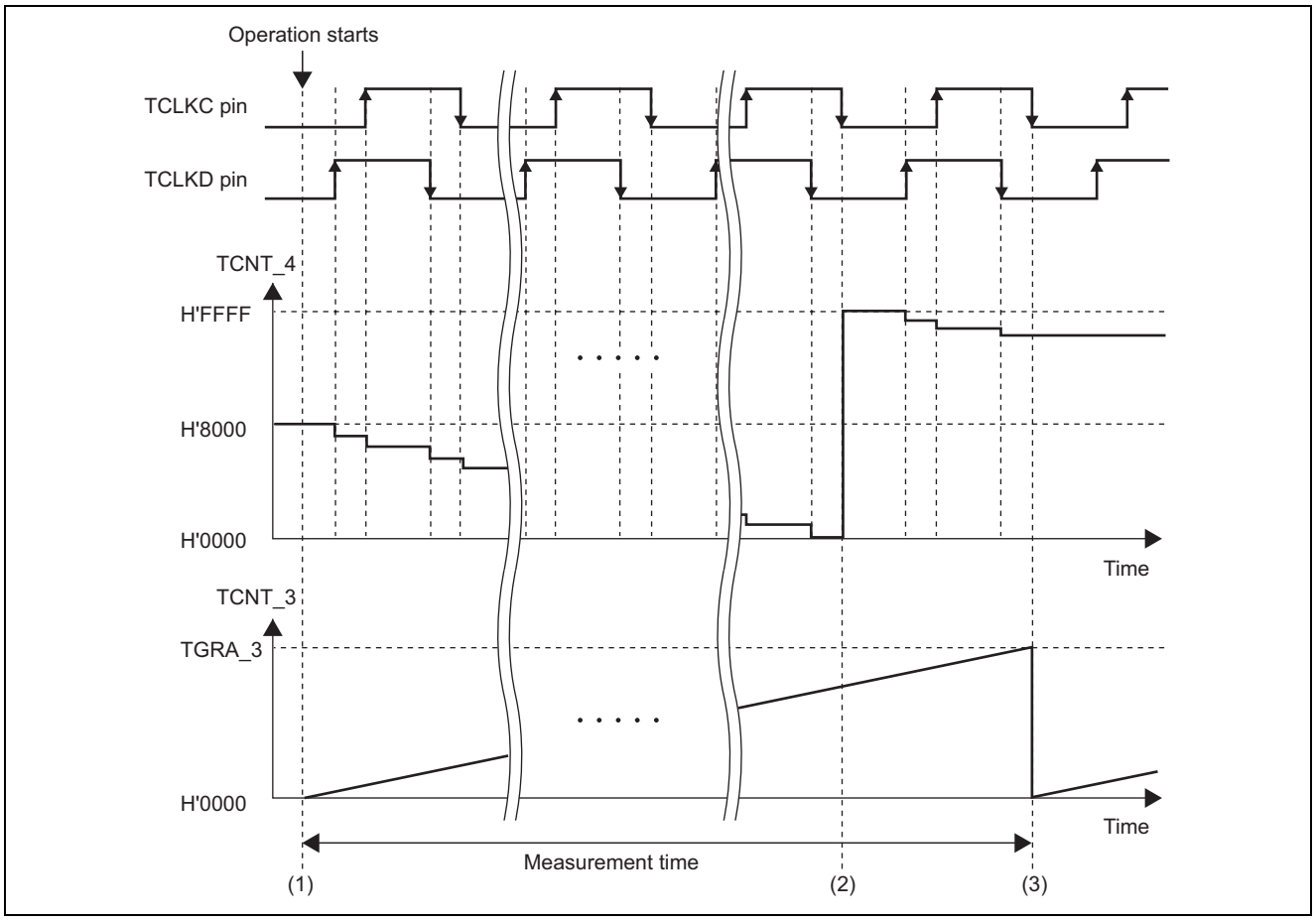


Figure 5 Example of Down-Counting Operation with Two-Phase Encoder Pulse Signal

Table 5 Hardware and Software Processing

	Hardware Processing	Software Processing
(1)	No processing	Initial settings: (a) Set the measurement time in TGRA_3 of TPU_3. (b) Put TPU_4 in phase counting mode 1. (c) Perform input capture of TGRA_4 on compare match with TGRA_3. (d) Load TCNT_4 with the initial value H'8000. (e) Set up the interrupts. (f) Start counting by TCNT_3 and TCNT_4.
(2)	(a) Generate an underflow interrupt (TCI4U).	TCI4U interrupt processing (a) Set the error flag.
(3)	(a) Transfer the TCNT_4 value to TGRA_4. (b) Generate a TGRA_4 input capture interrupt (TGI4A).	TGI4A interrupt processing (a) Store the value of TGRA_4 (result of two-phase encoder pulse counting) in RAM (tcnt).

5. Description of Software

5.1 List of Functions

Table 6 List of Functions

Function Name	Functions
init	Initialization routine Sets the CCR and configures the clocks, cancels the module stop mode, and calls the main function.
main	Main routine Configures TPU_3 and TPU_4, including selection of phase counting mode 1. Starts counting by TCNT_3 and TCNT_4.
tgi4a_int	Input capture interrupt handling routine
tci4v_int	Overflow interrupt handling routine
tci4u_int	Underflow interrupt handling routine

5.2 Vector Table

Table 7 Interrupt and Exception Handling Vector Table

Exception Handling Source	Vector Number	Vector Table Address	Exception Handling Routine
Reset	0	H'000000	main
TPU_4 TGI4A	106	H'0001A8	tgi4a_int
TPU_4 TCI4V	108	H'0001B0	tci4v_int
TPU_4 TCI4U	109	H'0001B4	tci4u_int

5.3 Constants

Table 8 List of Constants

Label Name	Setting	Description	Used In
SETTGRA	H'2000	Setting value of TGRA_3	main
SETTCNT	H'8000	Initial value of TCNT_4	main

5.4 RAM Usage

Table 9 RAM Usage

Type	Variable Name	Description	Used In
unsigned char	tcnt	Result of two-phase encoder pulse counting (counter value)	main, tgi4a_int
unsigned char	tflg	Result of two-phase encoder pulse counting (status) 0: Counting 1: Normal termination 2: Overflow error occurred 3: Underflow error occurred	main, tgi4a_int, tci4v_int, tci4u_int

5.5 Description of Functions

5.5.1 init Function

(1) Functional overview

Initialization routine which cancels the module stop mode, configures clocks, and calls the main function.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- System clock control register (SCKCR) Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Function
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock, which is
8	ICK0	0	R/W	supplied to the CPU, DMAC, and DTC. 000: Input clock × 4
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module
4	PCK0	1	R/W	clock. 001: Input clock × 2
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	0	R/W	000: Input clock × 4

- MSTPCRA, MSTPCRB, and MSTPCRC control module stop mode. Setting a bit in these registers to 1 places the corresponding module in module stop mode, while clearing the bit to 0 cancels module stop mode.

- Module stop control register A (MSTPCRA) Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Function
15	ACSE	0	R/W	All-module-clock-stop mode enable Enables or disables transition to all-module-clock-stop mode. If this bit is set to 1, all-module-clock-stop mode is entered when the SLEEP instruction is executed by the CPU while all the modules under control of the MSTPCR registers are placed in module stop mode. In all-module-clock-stop mode, even the bus controller and I/O ports are stopped to reduce the supply current. 0: Disables transition to all-module-clock-stop mode. 1: Enables transition to all-module-clock-stop mode.
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timer (TMR_3, TMR_2)
8	MSTPA8	1	R/W	8-bit timer (TMR_1, TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
0	MSTPA0	0	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

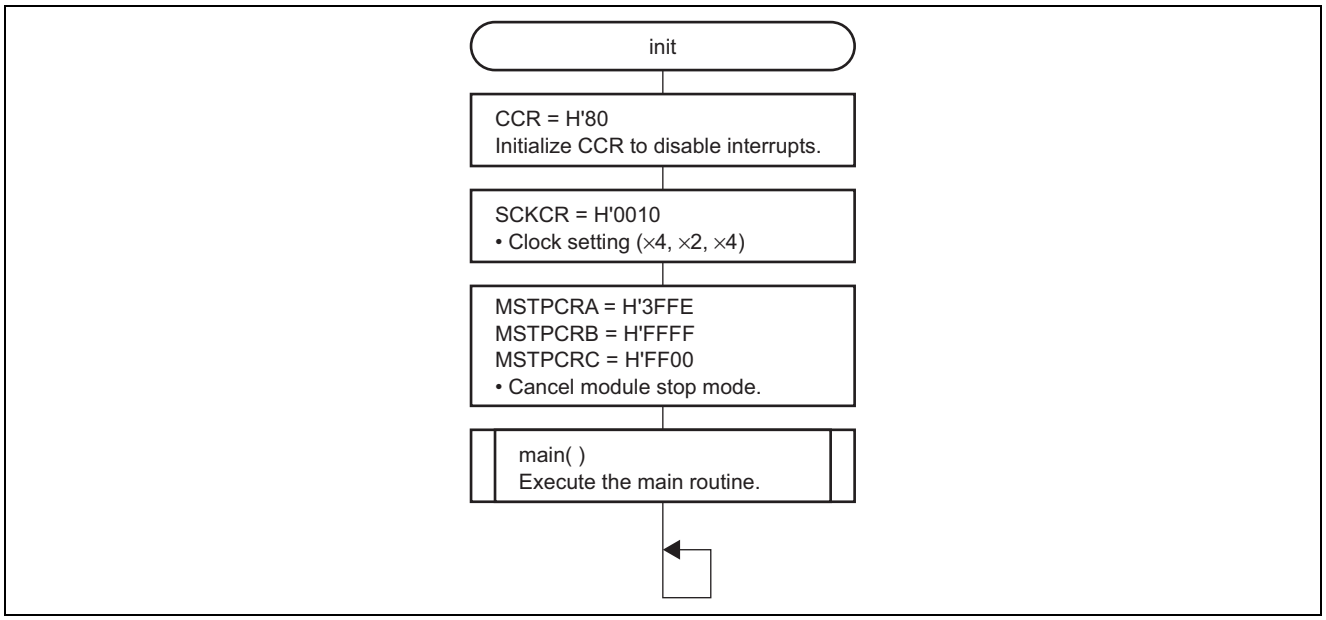
- Module stop control register B (MSTPCRB) Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Function
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communication interface_4 (SCI_4)
10	MSTPB10	1	R/W	Serial communication interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communication interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial communication interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus interface_1 (IIC_1)
6	MSTPB6	1	R/W	I^2C bus interface_0 (IIC_0)

- Module stop control register C (MSTPCRC) Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Function
15	MSTPC15	1	R/W	Serial communication interface_5 (SCI_5), (IrDA)
14	MSTPC14	1	R/W	Serial communication interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timer (TMR_4, TMR_5)
12	MSTPC12	1	R/W	8-bit timer (TMR_6, TMR_7)
11	MSTPC11	1	R/W	Universal serial bus interface (USB)
10	MSTPC10	1	R/W	Cyclic redundancy check
4	MSTPC4	0	R/W	On-chip RAM_4 (H'FF2000 to H'FF3FFF)
3	MSTPC3	0	R/W	On-chip RAM_3 (H'FF4000 to H'FF5FFF)
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF8000 to H'FF9FFF)
0	MSTPC0	0	R/W	On-chip RAM_0 (H'FFA000 to H'FFBFFF)

(5) Flowchart



5.5.2 main Function

(1) Functional overview

Main routine which configures TPU_3 and TPU_4, including selection of phase counting mode 1.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Port 1 input buffer control register (P1ICR) Address: H'FFFB90

Bit	Bit Name	Setting	R/W	Function
5	P15ICR	1	R/W	0: Input buffer of the P15 pin is disabled, and the input signal is fixed high 1: Input buffer of the P15 pin is enabled, and the pin state is reflected in the corresponding on-chip peripheral module
4	P14ICR	1	R/W	0: Input buffer of the P14 pin is disabled, and the input signal is fixed high 1: Input buffer of the P14 pin is enabled, and the pin state is reflected in the corresponding on-chip peripheral module

- Port function control register 6 (PFCR6) Address: H'FFFBC6

Bit	Bit Name	Setting	R/W	Function
3	TCLKS	1	R/W	TPU External Clock Input Pin Select Selects external clock input pins for the TPU. 0: External clock input pins cannot be used 1: Specifies pins P14 to P17 as external clock input pins

- Timer mode register_4 (TMDR_4) Address: H'FFFEE1

Bit	Bit Name	Setting	R/W	Function
3	MD3	0	R/W	Modes 3 to 0
2	MD2	1	R/W	These bits set the timer operating mode.
1	MD1	0	R/W	0100: Phase counting mode 1
0	MD0	0	R/W	Note: When phase counting mode is set, an external clock is selected as the counter input clock and TCNT operates as an up/down-counter regardless of the setting of bits TPSC2 to TPSC0, CKEG1, and CKEG0 in TCR.

- Timer I/O control register_4 (TIOR_4) Address: H'FFFEE2

Bit	Bit Name	Setting	R/W	Function
3	IOA3	1	R/W	I/O Control A3 to A0
2	IOA2	1	R/W	These bits specify the function of TGRA_4.
1	IOA1	0	R/W	1100: TGRA_4 functions as an input capture register.
0	IOA0	0	R/W	Input capture is performed on compare match or input capture of TGRA_3.

- Timer interrupt enable register_4 (TIER_4) Address: H'FFFEE4

Bit	Bit Name	Setting	R/W	Function
5	TCIEU	1	R/W	Underflow Interrupt Enable Enables/disables interrupt requests (TCIU) by the TCFU flag when the TCFU flag in TSR is set to 1 in channels 1, 2, 4, and 5. 0: Interrupt requests (TCIU) by TCFU disabled 1: Interrupt requests (TCIU) by TCFU enabled
4	TCIEV	1	R/W	Overflow Interrupt Enable Enables/disables interrupt requests (TCIV) by the TCFV flag when the TCFV flag in TSR is set to 1. 0: Interrupt requests (TCIV) by TCFV disabled 1: Interrupt requests (TCIV) by TCFV enabled
0	TGIEA	1	R/W	TGR Interrupt Enable A Enables or disables interrupt requests (TGIA) by the TGFA bit when the TGFA bit in TSR is set to 1. 0: Interrupt requests (TGIA) by TGFA bit disabled 1: Interrupt requests (TGIA) by TGFA bit enabled

- Timer counter_4 (TCNT_4) Address: H'FFFEE6
  Function: 16-bit readable/writable counter
  Setting: H'8000

- Timer start register (TSTR) Address: H'FFFFBC

Bit	Bit Name	Setting	R/W	Function
5	CST5	0	R/W	Counter Start 5 to 0
4	CST4	1	R/W	These bits start or stop the operation of the corresponding TCNT.
3	CST3	1	R/W	
2	CST2	0	R/W	0: Stops counting by TCNT_5 to TCNT_0
1	CST1	0	R/W	1: Starts counting by TCNT_5 to TCNT_0
0	CST0	0	R/W	

- Timer I/O control register H_3 (TIORH_3) Address: H'FFFFF2

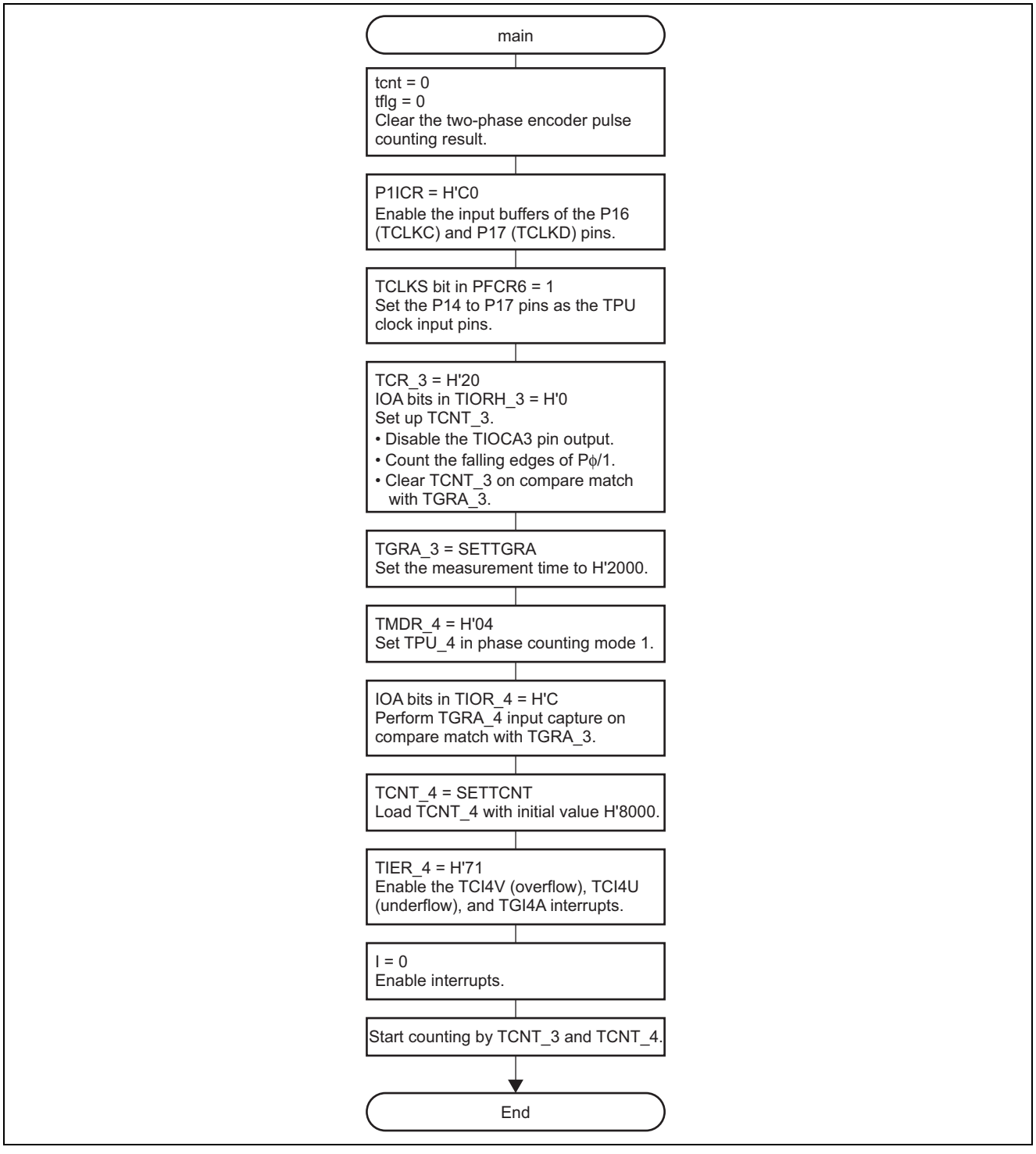
Bit	Bit Name	Setting	R/W	Function
3	IOA3	0	R/W	I/O Control A3 to A0
2	IOA2	0	R/W	These bits specify the function of TGRA_3.
1	IOA1	0	R/W	0000: TGRA_3 functions as an output compare register.
0	IOA0	0	R/W	The TIOCA3 pin output is disabled.

- Timer control register_3 (TCR_3) Address: H'FFFFF0

Bit	Bit Name	Setting	R/W	Function
7	CCLR2	0	R/W	Counter Clear 2 to 0
6	CCLR1	0	R/W	These bits select the TCNT_3 counter clearing source.
5	CCLR0	1	R/W	001: TCNT_3 is cleared on compare match/input capture of TGRA_3
4	CKEG1	0	R/W	Clock Edge 1 and 0
3	CKEG0	0	R/W	These bits select the input clock edge for counting.
				00: Falling edge
2	TPSC2	0	R/W	Timer Prescaler 2 to 0
1	TPSC1	0	R/W	These bits select the TCNT_3 counter clock.
0	TPSC0	0	R/W	000: Counting is driven by internal clock Pϕ/1

- Timer general register A_3 (TGRA_3) Address: H'FFFFF8
  Function: Used as an output compare register.
  Setting: H'2000

(5) Flowchart


main
tcnt = 0
tflg = 0
Clear the two-phase encoder pulse counting result.
P1ICR = H'C0
Enable the input buffers of the P16 (TCLKC) and P17 (TCLKD) pins.
TCLKS bit in PFCR6 = 1
Set the P14 to P17 pins as the TPU clock input pins.
TCR_3 = H'20
IOA bits in TIORH_3 = H'0
Set up TCNT_3.
• Disable the TIOCA3 pin output.
• Count the falling edges of Pϕ/1.
• Clear TCNT_3 on compare match with TGRA_3.
TGRA_3 = SETTGRA
Set the measurement time to H'2000.
TMDR_4 = H'04
Set TPU_4 in phase counting mode 1.
IOA bits in TIOR_4 = H'C
Perform TGRA_4 input capture on compare match with TGRA_3.
TCNT_4 = SETTCNT
Load TCNT_4 with initial value H'8000.
TIER_4 = H'71
Enable the TCI4V (overflow), TCI4U (underflow), and TGI4A interrupts.
I = 0
Enable interrupts.
Start counting by TCNT_3 and TCNT_4.
End

5.5.3 tgi4a_int Function

(1) Functional overview

Input capture interrupt processing

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Timer status register_4 (TSR_4) Address: H'FFFEE5

Bit	Bit Name	Setting	R/W	Function
0	TGFA	0	R/(W)*	Input Capture/Output Compare Flag A When TGRA_4 functions as an input capture register: [Setting condition] • When the TCNT_4 value is transferred to TGRA_4 by an input capture signal [Clearing condition] • When 0 is written to TGFA after reading TGFA = 1

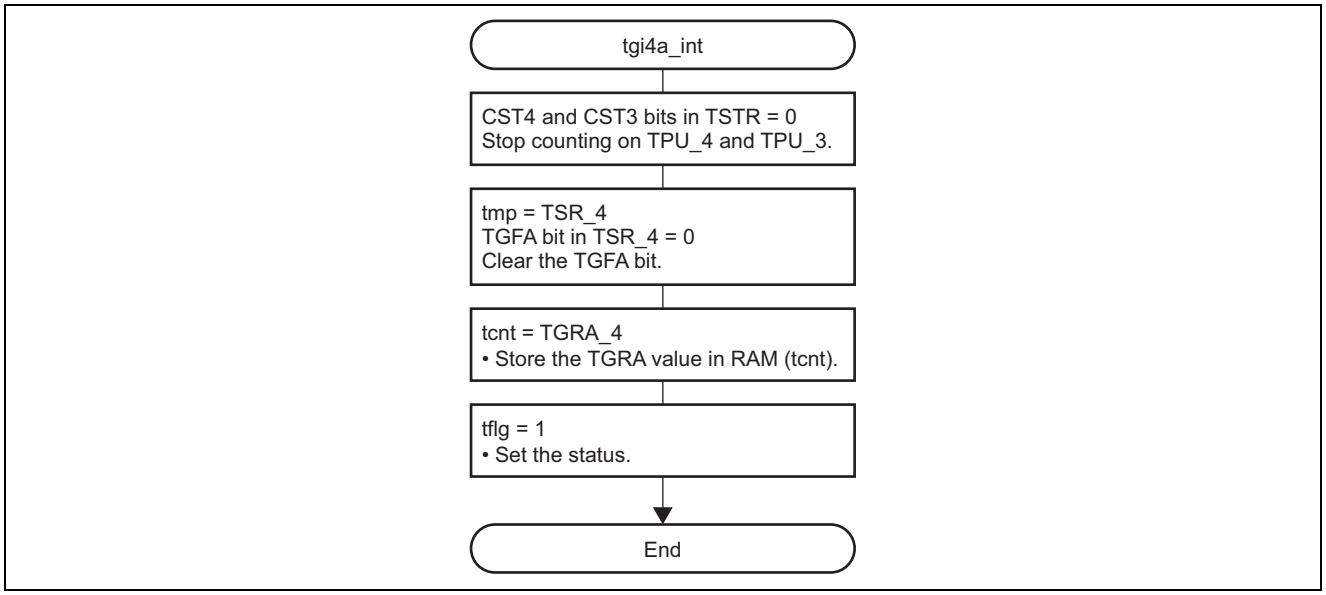
Note: * Only 0 can be written to clear the flag.

- Timer general register A_4 (TGRA_4) Address: H'FFFEE8
  Function: Captured period counter value is stored here.
  Setting: Undefined

- Timer start register (TSTR) Address: H'FFFFBC

Bit	Bit Name	Setting	R/W	Function
5	CST5	0	R/W	Counter Start 5 to 0
4	CST4	0	R/W	These bits start or stop the operation of the corresponding
3	CST3	0	R/W	TCNT.
2	CST2	0	R/W	0: Stops counting by TCNT_5 to TCNT_0
1	CST1	0	R/W	1: Starts counting by TCNT_5 to TCNT_0
0	CST0	0	R/W	

(5) Flowchart


tgi4a_int
CST4 and CST3 bits in TSTR = 0
Stop counting on TPU_4 and TPU_3.
tmp = TSR_4
TGFA bit in TSR_4 = 0
Clear the TGFA bit.
tcnt = TGRA_4
• Store the TGRA value in RAM (tcnt).
tflg = 1
• Set the status.
End

5.5.4 tci4v_int Function

(1) Functional overview

Overflow interrupt processing

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

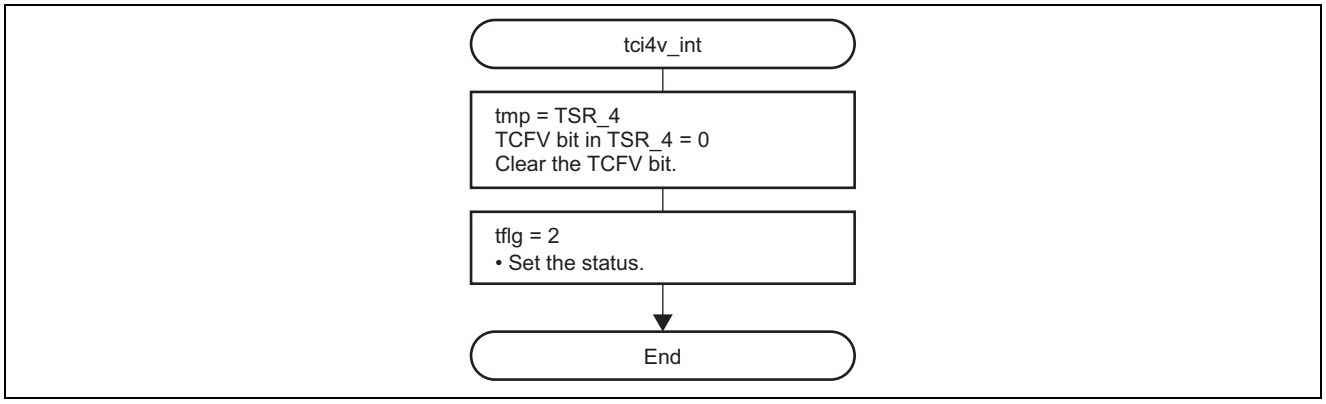
The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Timer status register_4 (TSR_4) Address: H'FFFEE5

Bit	Bit Name	Setting	R/W	Function
4	TCFV	0	R/(W)*	Overflow Flag Status flag that indicates that TCNT_4 has overflowed. [Setting condition] • When the TCNT_4 value has overflowed [Clearing condition] • When 0 is written to TCFV after reading TCFV = 1

Note: * Only 0 can be written to clear the flag.

(5) Flowchart



5.5.5 tci4u_int Function

(1) Functional overview

Underflow interrupt processing

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

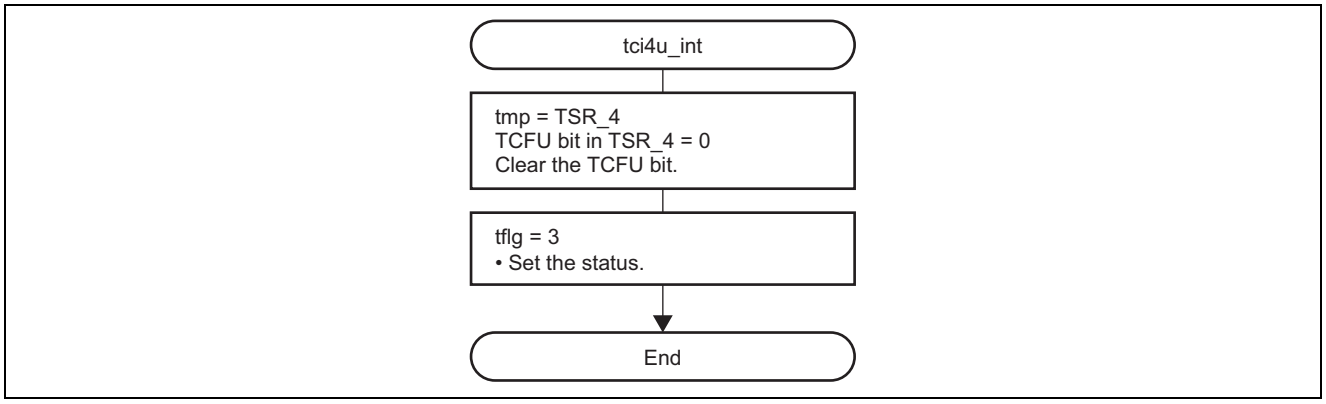
The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Timer status register_4 (TSR_4) Address: H'FFFEE5

Bit	Bit Name	Setting	R/W	Function
5	TCFU	0	R/(W)*	Underflow Flag Status flag that indicates that TCNT_4 has underflowed when TPU_4 is in phase counting mode. [Setting condition] • When the TCNT_4 value has underflowed [Clearing condition] • When 0 is written to TCFU after reading TCFU = 1

Note: * Only 0 can be written to clear the flag.

(5) Flowchart



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		Description	
Rev.	Date	Page	Summary
1.00	Sep.11.06	—	First edition issued

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