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Renesas Electronics Corporation

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H8/300L Super Low Power Series

Counting Interrupts Generated by the 16-Bit Timer Counter

Introduction

Timer F interrupts are counted, and operation stops when 50 interrupts are counted. Timer F interrupts are set to be generated every 52.429 ms, which is the time when the Timer Counter F (TCF) overflows.

Target Device

H8/38024

Contents

1. Specifications

1. Timer F is used as a 16-bit interval timer counter. 1-byte variable is decremented during Timer F interrupt processing. Timer F interrupt request is disabled and operation stops when 50 interrupts are counted.
2. Timer F interrupts are set to be generated every 52.429 ms, which is the time when the Timer Counter F (TCF) overflows.
3. 1-byte variable, which is set on RAM, is used to count interrupts.

2. Description of Functions Used

1. In this sample task, Timer F interrupts are counted using the 16-bit timer counter function of Timer F.
   a. Figure 1 shows the block diagram of the 16-bit timer counter function of Timer F, which is described below.
      - The system clock (ϕ) is a 5-MHz clock and also a reference clock to operate the CPU and its peripheral functions.
      - The Prescaler S (PSS) is a 13-bit counter using ϕ as its input clock and is counted up every cycle.
      - The Timer Counter F (TCF) is a 16-bit readable/writable up-counter and is counted up by an internal or external clock which is input. The input clock can be selected from four clocks obtained by dividing the system clock by 4, 16 and 32, and an external clock. In this sample task, a clock obtained by dividing the system clock by 4 is selected as the TCF input clock.
      - The Timer Control Register F (TCRF) is an 8-bit readable/writable register. It switches over 16-bit/8-bit modes, selects an input clock from among the four internal clocks and external events, sets the output level of both TMOFH and TMOFL pins.
      - The Timer Control/Status Register F (TCSRF) is an 8-bit register. It selects the counter clearing, sets overflow flag and compare match flag, and enables/disables the overflow interrupt requests.
      - The Timer Counter F (TCF) overflow period in this sample task is given by the equation below:

$$\text{TCF overflow period} = \frac{1}{\text{System clock}/4} \times 65536$$
$$= \frac{1}{5\ \text{MHz}/4} \times 65536$$
$$= 52.429\ \text{ms}$$

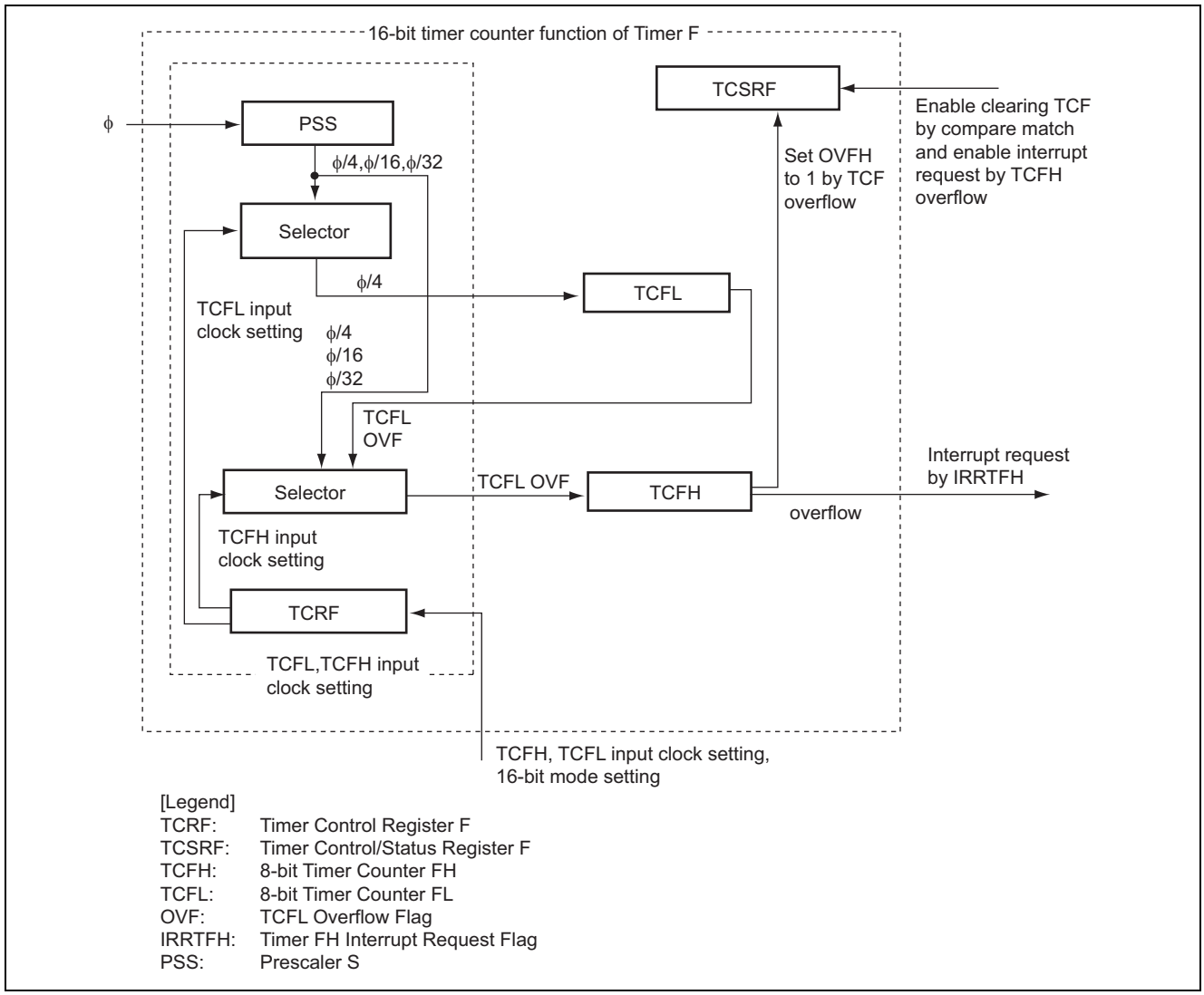


Figure 1 Block Diagram of Timer F 16-bit Timer Counter Function

2. Table 1 shows function assignment in this sample task. The functions are assigned as shown in table 1 and interrupts are counted by the 16-bit timer counter function of Timer F.

Table 1 Assignment of Functions

Function	Assignment
PSS	A 13-bit up-counter using the system clock as input
TCRF	Sets TCF input clock
TCSRF	Enables TCF overflow interrupt requests and selects TCF clearing
TCFH, TCFL	A 16-bit counter using a clock obtained by dividing the system clock by 4 as input
IENTFH	Enables interrupt requests by Timer FH overflow
IRRTFH	An interrupt flag by Timer FH overflow
counter_sub	An 8-bit counter to count timer F interrupts for 50 times

3. Principle of Operation

1. Figure 2 illustrates the principle of operation of this sample task. As shown in figure 2, interrupts are counted by the 16-bit timer counter function of Timer F by means of hardware processing and software processing.

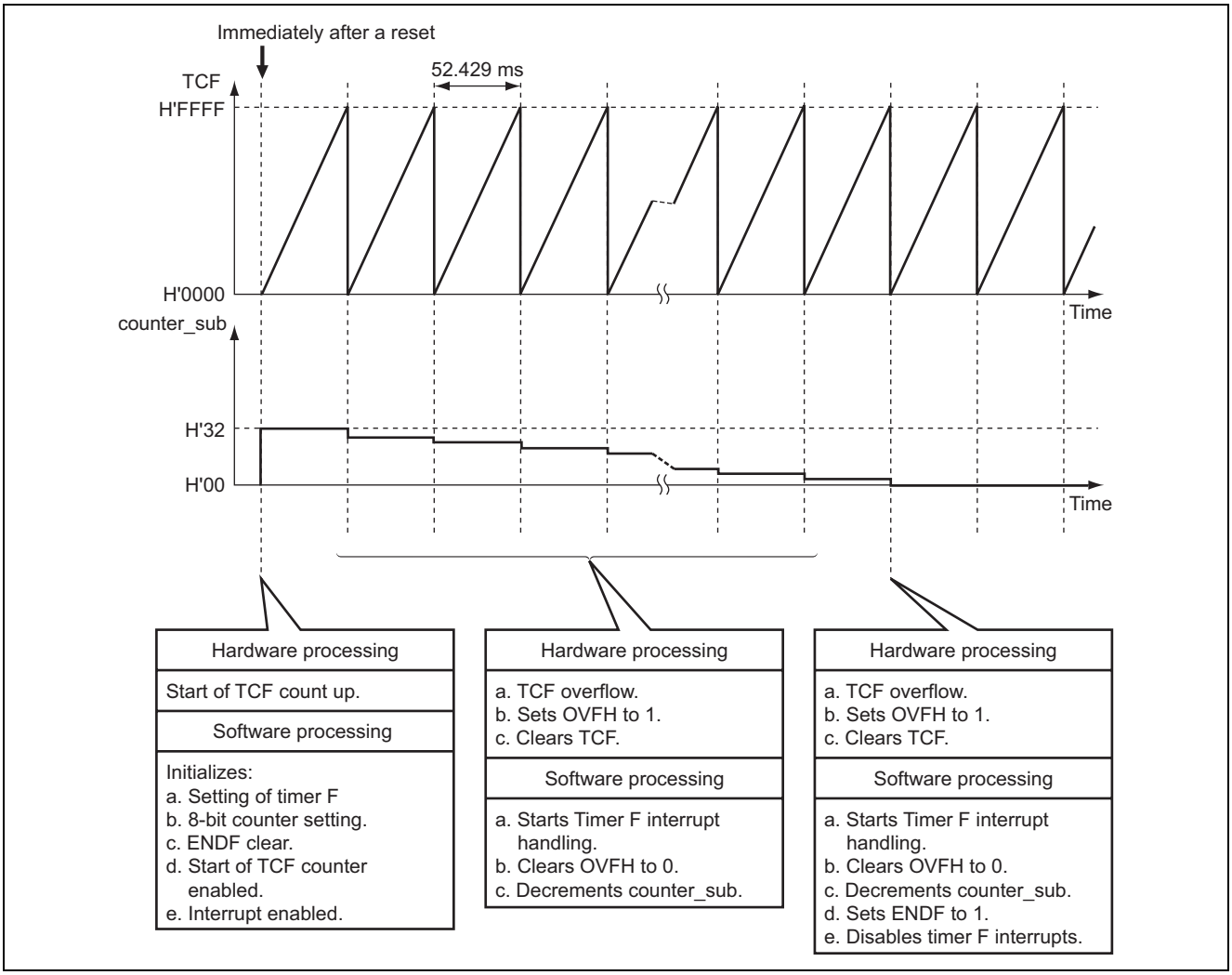


Figure 2 Operation Principle of Interrupt Counting by 16-Bit Timer Counter Function of Timer F

4. Description of Software

4.1 Modules

Table 2 describes the modules in this sample task.

Table 2 Description of Modules

Module	Label	Function
Main Routine	main	Sets the 16-bit timer counter function of timer F, sets the 8-bit counter, enables interrupts, sets start of TCF counter, and stops operation when ENDF is set to 1.
Interrupt Count	tfint	Decrements the value of the 8-bit counter, sets ENDF to 1 when the counter value becomes H'00 and disables Timer F interrupts by Timer F interrupt handling.

4.2 Arguments

No arguments are used in this sample task.

4.3 Internal registers

Table 3 describes the internal registers in this sample task.

Table 3 Description of Internal Registers

Register		Function	Address	Setting
TCRF	CKSH2 CKSH1 CKSH0	Timer Control Register F (Clock Select H) When (CKSH2 = 0, CKSH1 = 0 and CKSH0 = 0), (CKSH2 = 0, CKSH1 = 0 and CKSH0 = 1) or (CKSH2 = 0, CKSH1 = 1 and CKSH0 = 0), TCF operates as a 16-bit counter.	H'FFB6 Bit 6 Bit 5 Bit 4	CKSH2 = 0 CKSH1 = 0 CKSH0 = 0
	CKSL2 CKSL1 CKSL0	Timer Control Register F (Clock Select L) When CKSL2 = 1, CKSL1 = 1 and CKSL0 = 0, TCF counts at the rising edge of system clock/4.	H'FFB6 Bit 2 Bit 1 Bit 0	CKSL2 = 0 CKSL1 = 0 CKSL0 = 0
TCSRF	OVFH	Timer Control/Status Register F (Timer Overflow Flag H) When OVFH = 0, TCF does not overflow. When OVFH = 1, TCF overflows.	H'FFB7 Bit 7	0
	CMFH	Timer Control/Status Register F (Compare Match Flag H) When CMFH = 0, compare match F is not generated. When CMFH = 1, compare match F is generated.	H'FFB7 Bit 6	0
	OVIEH	Timer Control/Status Register F (Timer Overflow Interrupt Enable H) When OVIEH = 1, TCF overflow interrupt requests are enabled.	H'FFB7 Bit 5	1
	CCLRH	Timer Control/Status Register F (Counter Clear H) When CCLRH = 0, clearing TCF by compare match is disabled.	H'FFB7 Bit 4	0

Register		Function	Address	Setting
TCF		Timer Counter F A 16-bit up-counter using a clock obtained by dividing the system clock by 4 as input.	H'FFB8	H'0000
IENR2	IENTFH	Interrupt Enable Register 2 (Timer FH Interrupt Enable) When IENTFH = 0, Timer FH interrupt requests are disabled. When IENTFH = 1, Timer FH interrupt requests are enabled.	H'FFF4 Bit 3	1
IRR2	IRRTFH	Interrupt Request Register 2 (Timer FH Interrupt Request Flag) When IRRTFH = 0, a Timer FH interrupts are not requested. When IRRTFH = 1, a Timer FH interrupts are requested.	H'FFF7 Bit 3	0

4.4 RAM

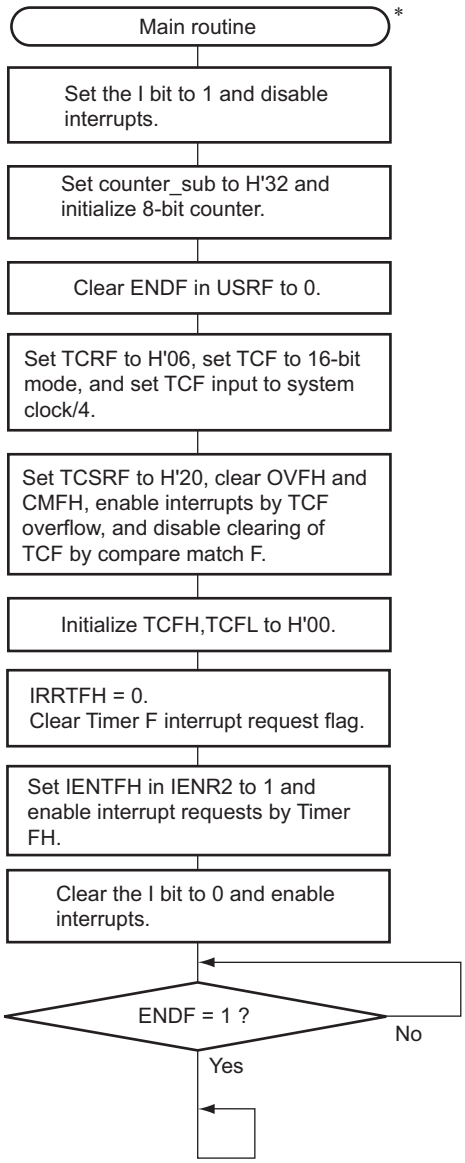
The RAMs used in this sample task are described in table 4 below.

Table 4 Description of RAM Used

Label		Function	Address	Used in
counter_sub		8-bit counter	H'FB80	Main Routine Interrupt Count
USRF	ENDF	Flag to indicate whether or not the counter value of the 8-bit counter has become H'00.	H'FB81 Bit 0	Main Routine Interrupt Count

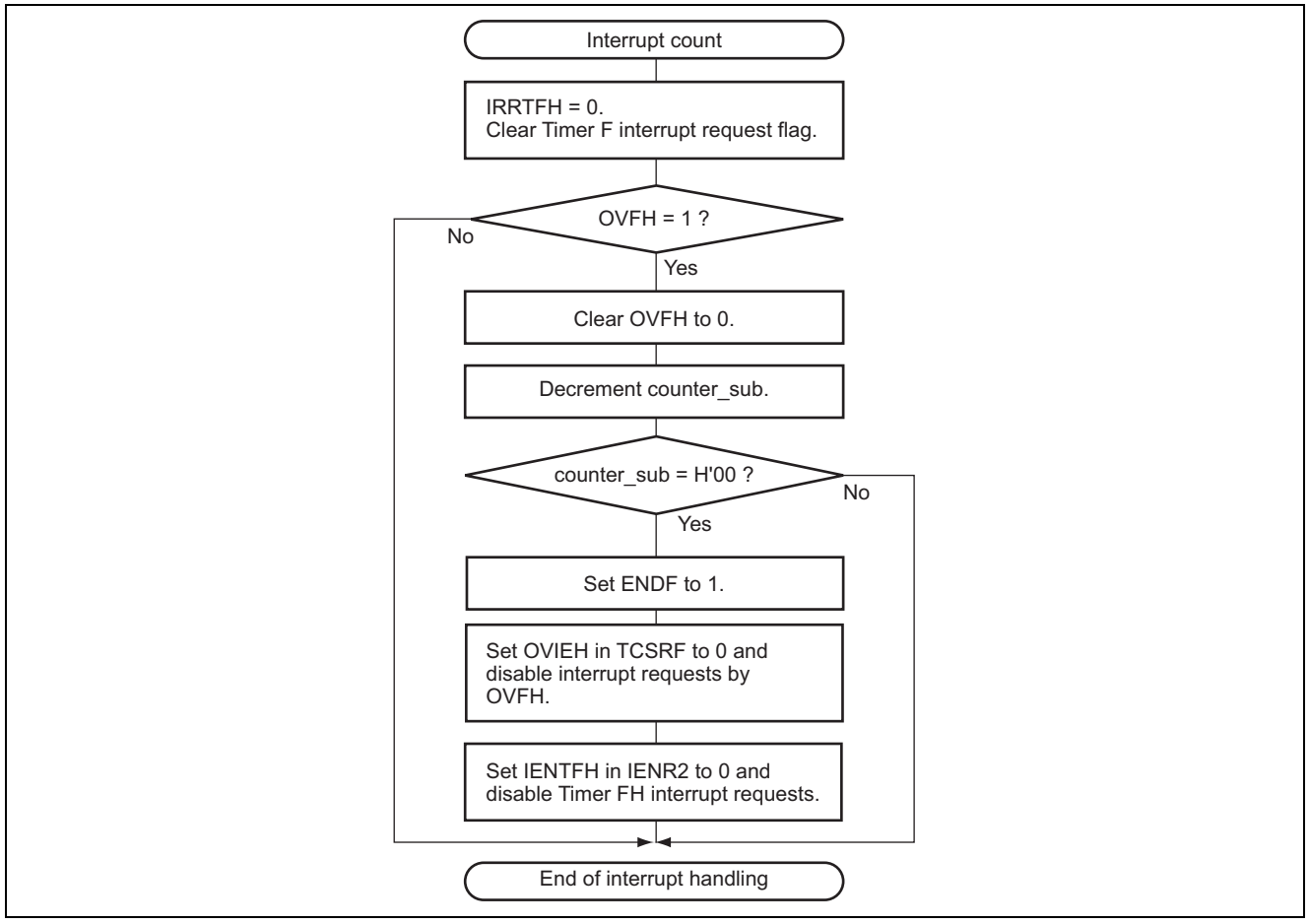
5. Flowchart

1. Main routine



Note: * In this sample task, the stack pointer is set in INIT.SRC (assembly language).

2. Timer F overflow interrupt routine



6. Program Listing

INIT.SRC (Program listing)

```
   .EXPORT   _INIT
   .IMPORT   _main
;
   .SECTION  P,CODE
_INIT:
   MOV.W     #H'FF80,R7
   LDC.B     #B'10000000,CCR
   JMP       @_main
;
   .END
```

```
/************************************************************************************************/
/*                                                                                              */
/*  H8/300L Super Low Power Series                                                              */
/*      -H8/38024 Series-                                                                       */
/*  Application Note                                                                            */
/*                                                                                              */
/*  'Interrupt Counting by 16-bit Timer Counter                                                 */
/*   Function'                                                                                  */
/*                                                                                              */
/*  Function                                                                                    */
/*  : Timer F 16bit Timer Counter                                                               */
/*                                                                                              */
/*  External Clock :  10MHz                                                                     */
/*  Internal Clock :  5MHz                                                                      */
/*  Sub Clock:        32.768kHz                                                                 */
/*                                                                                              */
/************************************************************************************************/

#include    <machine.h>

/************************************************************************************************/
/*  Symbol Definition                                                                           */
/************************************************************************************************/
struct BIT {
    unsigned char  b7:1;       /* bit7 */
    unsigned char  b6:1;       /* bit6 */
    unsigned char  b5:1;       /* bit5 */
    unsigned char  b4:1;       /* bit4 */
    unsigned char  b3:1;       /* bit3 */
    unsigned char  b2:1;       /* bit2 */
    unsigned char  b1:1;       /* bit1 */
    unsigned char  b0:1;       /* bit0 */
};
```

```
#define      TCRF        *(volatile unsigned char *)0xFFB6   /* Timer Control Register F         */
#define      TCRF_BIT    (*(struct BIT *)0xFFB6)             /* Timer Control Register F         */
#define      TOLH        TCRF_BIT.b7                         /* Toggle Output Level F            */
#define      CKSH2       TCRF_BIT.b6                         /* Clock Select H2                  */
#define      CKSH1       TCRF_BIT.b5                         /* Clock Select H1                  */
#define      CKSH0       TCRF_BIT.b4                         /* Clock Select H0                  */
#define      TCSRF       *(volatile unsigned char *)0xFFB7   /* Timer Control Status Register F  */
#define      TCSRF_BIT   (*(struct BIT *)0xFFB7)             /* Timer Control Status Register F  */
#define      OVFH        TCSRF_BIT.b7                        /* Timer Overflow Flag H            */
#define      CMFH        TCSRF_BIT.b6                        /* Compare Match Flag H             */
#define      OVIEH       TCSRF_BIT.b5                        /* Timer Overflow Interrupt Enable  */
#define      CCLRH       TCSRF_BIT.b4                        /* Output Select 3                  */
#define      OCRFL       *(volatile unsigned char *)0Xffbb   /* Output Compare Register FL       */
#define      TCFH        *(volatile unsigned char *)0xFFB8   /* Timer Counter FL                 */
#define      TCFL        *(volatile unsigned char *)0xFFB9   /* Timer Counter FL                 */
#define      IENR2       *(volatile unsigned char *)0xFFF4   /* Interrupt Enable Register 2      */
#define      IENR2_BIT   (*(struct BIT *)0xFFF4)             /* Interrupt Enable Register 2      */
#define      IENTFH      IENR2_BIT.b3                        /* Timer FH Interrupt Enable        */
#define      IENTFL      IENR2_BIT.b2                        /* Timer FH Interrupt Enable        */
#define      IRR2_BIT    (*(struct BIT *)0xFFF7)             /* Interrupt Request Register 2     */
#define      IRRTFH      IRR2_BIT.b3                         /* Timer FH Interrupt Request Flag  */
#define      IRRTFL      IRR2_BIT.b2                         /* Timer FH Interrupt Request Flag  */

#pragma interrupt (tfint)
/************************************************************************************************/
/*  Function define                                                                             */
/************************************************************************************************/
extern void  INIT ( void );                                  /* SP Set                           */
void         main ( void );
void         tfint ( void );

/************************************************************************************************/
/*  RAM define                                                                                  */
/************************************************************************************************/
unsigned char            counter_sub;
unsigned char            USRF;                               /* User Flag Area                   */

#define      USRF_BIT    (*(struct BIT *)& USRF)
#define      ENDF        USRF_BIT.b0                         /* End Flag                         */

/************************************************************************************************/
/*  Vector Address                                                                              */
/************************************************************************************************/
#pragma section          V1                                  /* Vector Section Set               */
void (*const VEC_TBL1[])(void) = {                           /* 0x0000 - 0x000F                  */
    INIT                                                     /* 0x0000 Reset Vector              */
};
#pragma section          V2                                  /* Vector Section Set               */
void (*const VEC_TBL2[])(void) = {
    taint                                                    /* 0x001E Timer F Interrupt Vector  */
};

#pragma section                                              /* P                                */
```

```
/*****************************************************************************************/
/*  Main Program                                                                         */
/*****************************************************************************************/
void         main ( void )
{
    set_imask_ccr(1);                                   /* Interrupt Disable            */

    counter_sub = 0x32;                                 /* Initialize 8bit Counter_sub  */
    ENDF = 0;                                           /* Initialize ENDF              */

    TCRF = 0x06;                                        /* Initialize Clock Select      */
    TCSRF = 0x20;                                       /* Initialize Overflow Interrupt*/

    TCFH = 0x00;                                        /* Clear Timer Counter F        */
    TCFL = 0x00;                                        /* Clear Timer Counter F        */

    IRRTFH = 0;
    IENTFH = 1;

    set_imask_ccr(0);                                   /* Interrupt Enable             */

    while(ENDF ! = 1){                                  /* ENDF = 1 ?                   */
        ;
    }

    while(1){
        ;
    }
}

/*****************************************************************************************/
/*  Timer F Interrupt                                                                    */
/*****************************************************************************************/
void    tfint ( void )
{
    IRRTFH = 0;

    if ( OVFH == 1 ){
        OVFH = 0;                                       /* Clear OVFH                   */
        counter_sub--;                                  /* Decrement 8bit Counter       */

        if ( counter_sub == 0x00 ){                     /* 8bit Counter ! = H'00        */
             ENDF = 1;                                  /* Set ENDF                     */
             OVIEH = 0;
             IENTFH = 0;
        }
    }
}
```

Link address specifications

Section Name	Address
CV1	H'0000
CV2	H'001E
P	H'0100
B	H'FB80

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		Description	
Rev.	**Date**	**Page**	**Summary**
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2.00	Nov.30.06	All pages	Content correction

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