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H8/300L Super Low Power Series

Conversion from Single-Precision Floating-Point to Signed 32-Bit Binary (FKTR)

Introduction

The software FKTR converts a single-precision floating-point number, which is placed in general-purpose registers, to a signed 32-bit binary number.

Target Device

H8/38024

Contents

1. Arguments

Description		Memory area	Data length (bytes)
Input	Single-precision floating-point number	R0, R1	4
Output	Signed 32-bit binary number	R2, R3	4

2. Changes to Internal Registers and Flags

R0	R1	R2	R3	R4	R5	R6	R7
×	×	○	○	—	×	—	—

I	U	H	U	N	Z	V	C
—	—	×	—	×	×	×	×

Legend
—: No change
×: Undefined
○: Result

3. Specifications

Program memory (bytes)
100
Data memory (bytes)
0
Stack (bytes)
0
Clock cycle count
108
Reentrant
Possible
Relocation
Possible
Interrupt
Possible

4. Notes

The clock cycle count (108) in the specifications is for the example shown in figure 1.

For the format of floating-point numbers, see "About Single-Precision Floating-Point Numbers <Reference>."

5. Description

5.1 Details of functions

1. The following arguments are used with the software FKTR:
   a. Input arguments:
      R0: Sets the upper 2 bytes of a single-precision floating-point number.
      R1: Sets the lower 2 bytes of a single-precision floating-point number.
   b. Output arguments:
      R2: The upper 2 bytes of the signed 32-bit binary number are placed here.
      R3: The lower 2 bytes of the signed 32-bit binary number are placed here.
2. The following figure illustrates the execution of the software FKTR. When the input arguments are set as shown in (1), the converted result is placed in R2 and R3 as shown in (2).

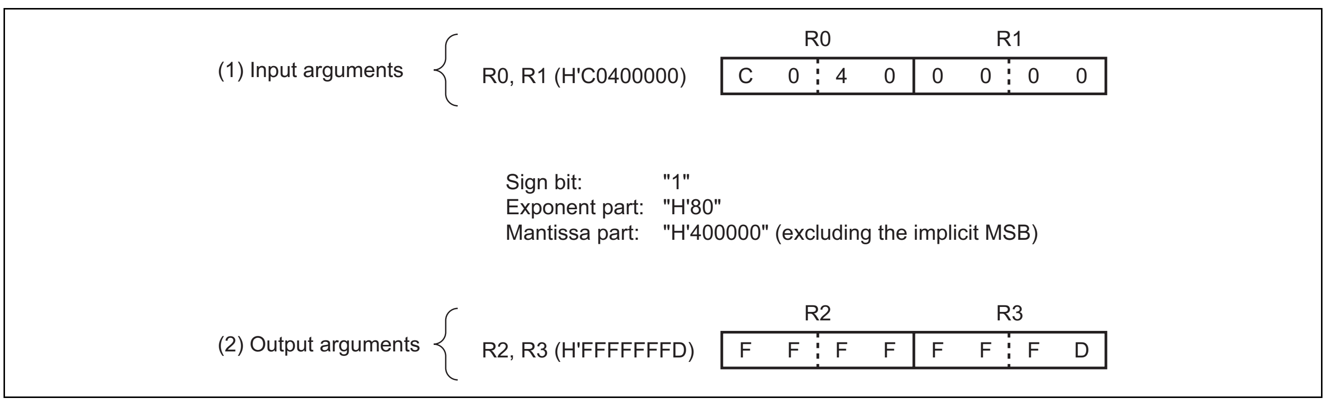


Figure 1 Example of Software FKTR Execution

5.2 Notes on usage

1. When the given single-precision floating-point number is "0" or not more than |1|, "0" is output.
2. When the given single-precision floating-point number is not less than $|2^{31}|$, a maximum value with the same sign (H'7FFFFFFF or H'80000000) is output.
3. After execution of the software FKTR, the input arguments placed in R0 and R1 are lost. When the input arguments are still needed after software FKTR execution, save them in memory in advance.

5.3 Description of data memory

The software FKTR does not use data memory.

5.4 Example of usage

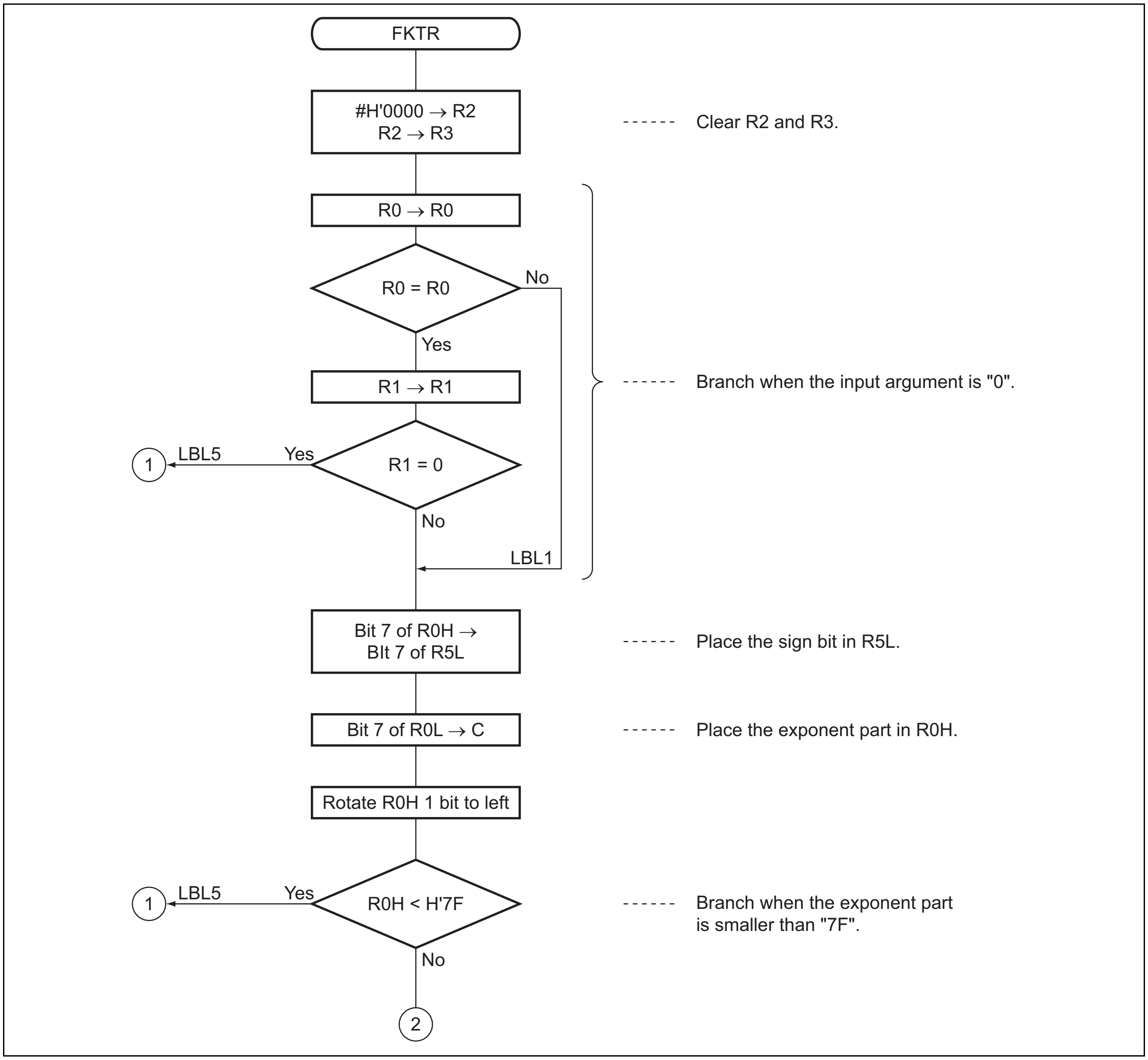
Set a single-precision floating-point number in the general-purpose registers and call the software FKTR as a subroutine.

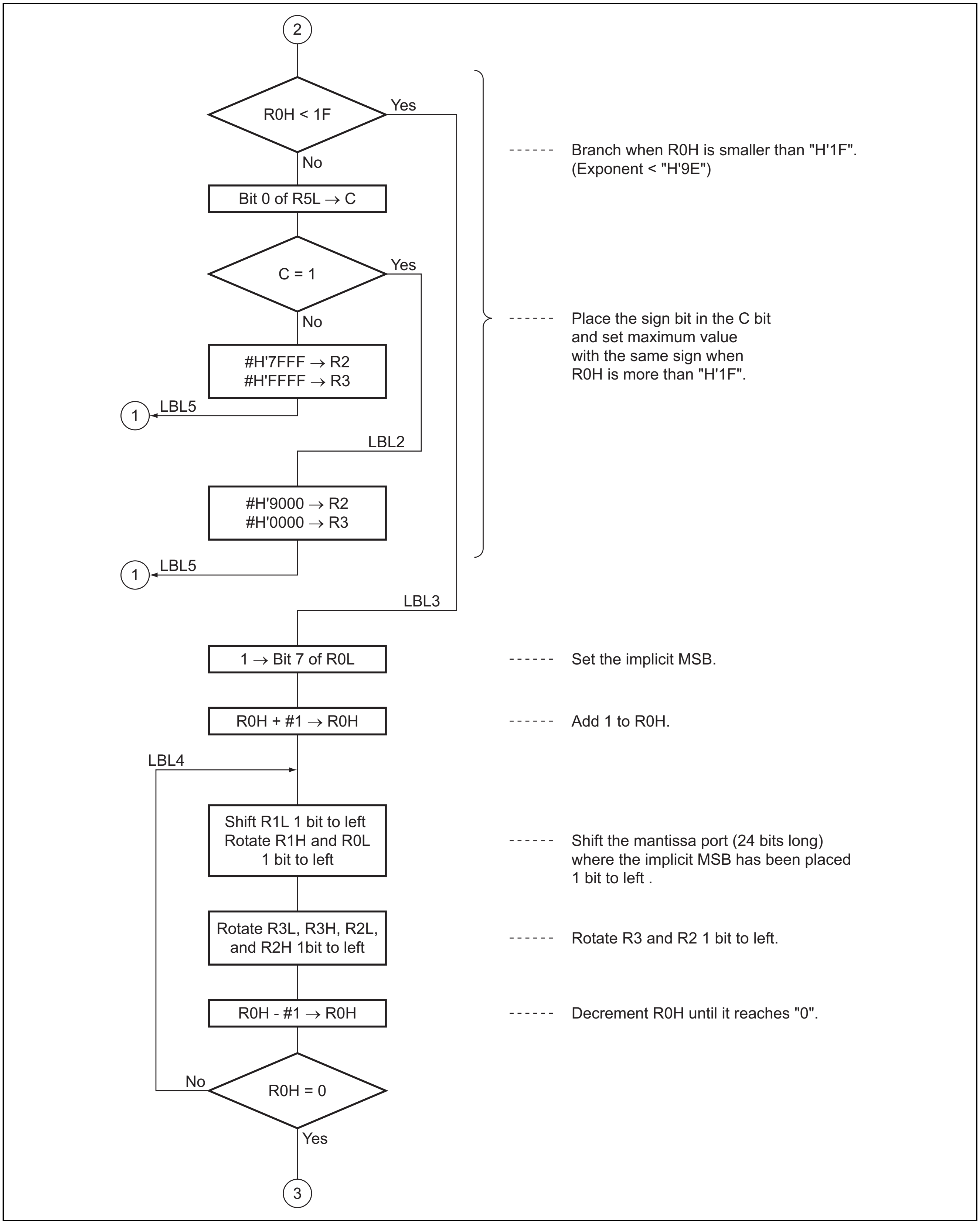
```
WORK1     .DATA.W    2,0  --------- Reserves a data memory area in which the user program places
                                    a short floating-point number.

WORK1     .DATA.W    2,0  --------- Reserves a data memory area in which the user program places
                                    a signed 32-bit binary number.
              .
              .
              .
          MOV.B      @WORK1,R0    }------- Places the short floating-point number set by the user
          MOV.W      @WORK1+2,R1  }        program in R0 and R1.

          JSR        @FKTR         ------- Calls the software FKTR as a subroutine.

          MOV.W      R2,@WORK3    }------- Places the signed 32-bit binary number set in the
          MOV.W      R3,@WORK2+2  }        output argument in R2 and R3 .
              .
              .
              .
```

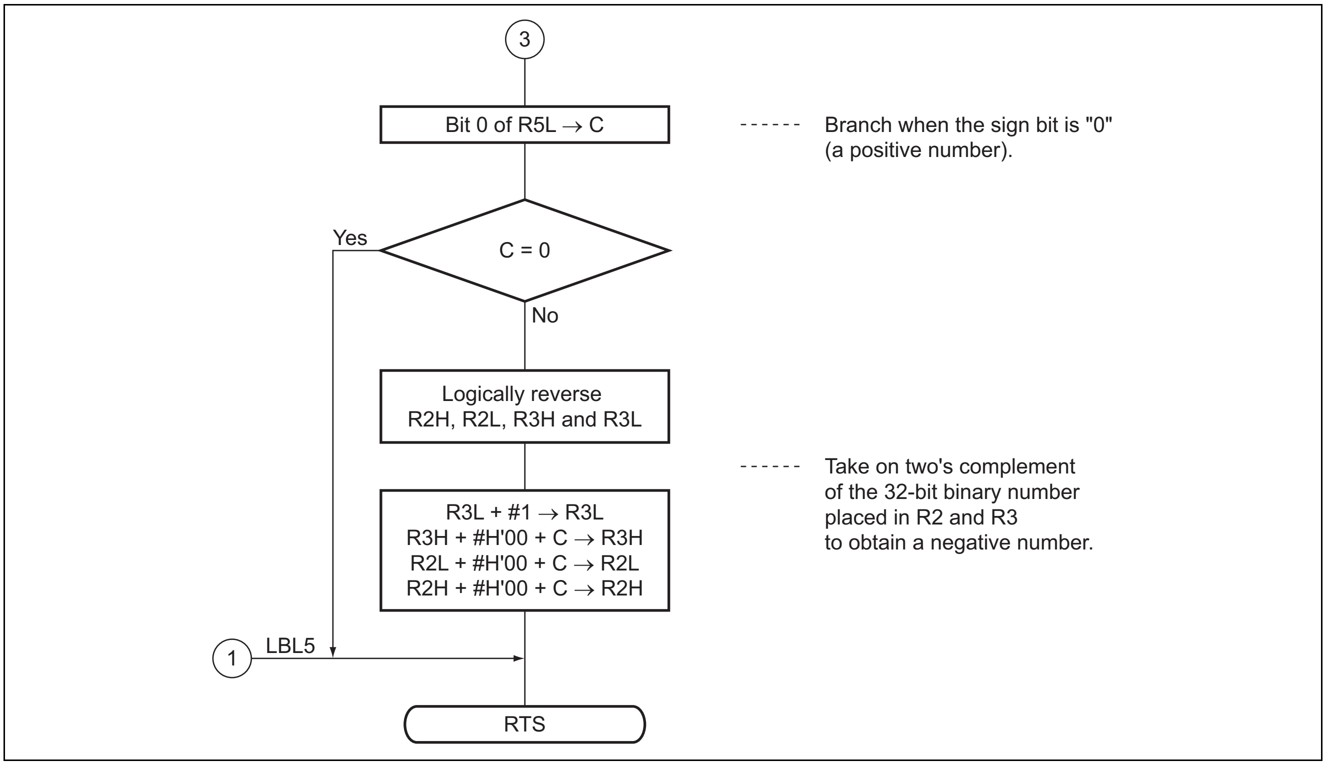
5.5 Operation

1. The software FKTR takes the following steps to convert the single-precision floating-point number to a signed 32-bit binary number:
2. First, the input argument is checked.
   a. When the input argument is "0", then "0" is output.
   b. When the exponent is smaller than "H'7F", then "0" is output.
   c. When the exponent is more than "H'9E", a maximum value with the same sign is output.
3. Next, when the input argument is not "0" and its absolute value is more than "1" (the exponent = H'7F) and smaller than 2^{31} (the exponent = H'9E), the following operations are performed:
   a. The implicit MSB is set.
   b. The mantissa (24 bits long) in which the implicit MSB is set is shifted 1 bit to left.
   c. R3 and R2 are rotated 1 bit to left.
   d. Steps b and c are repeated as many times as "R0H + 1".
   e. When the sign bit is negative, it is made into a negative number by taking its two's complement.

6. Flowchart


FKTR
#H'0000 → R2
R2 → R3
Clear R2 and R3.
R0 → R0
R0 = R0
No
Yes
R1 → R1
R1 = 0
Yes
LBL5
1
No
LBL1
Branch when the input argument is "0".
Bit 7 of R0H →
BIt 7 of R5L
Place the sign bit in R5L.
Bit 7 of R0L → C
Place the exponent part in R0H.
Rotate R0H 1 bit to left
R0H < H'7F
Yes
LBL5
1
No
2
Branch when the exponent part
is smaller than "7F".


2
R0H < 1F
Yes
No
Bit 0 of R5L → C
C = 1
Yes
No
#H'7FFF → R2
#H'FFFF → R3
1
LBL5
LBL2
#H'9000 → R2
#H'0000 → R3
1
LBL5
LBL3
1 → Bit 7 of R0L
R0H + #1 → R0H
LBL4
Shift R1L 1 bit to left
Rotate R1H and R0L
1 bit to left
Rotate R3L, R3H, R2L, and R2H 1bit to left
R0H - #1 → R0H
No
R0H = 0
Yes
3
------ Branch when R0H is smaller than "H'1F". (Exponent < "H'9E")
------ Place the sign bit in the C bit and set maximum value with the same sign when R0H is more than "H'1F".
------ Set the implicit MSB.
------ Add 1 to R0H.
------ Shift the mantissa port (24 bits long) where the implicit MSB has been placed 1 bit to left .
------ Rotate R3 and R2 1 bit to left.
------ Decrement R0H until it reaches "0".


3
Bit 0 of R5L → C
Branch when the sign bit is "0" (a positive number).
Yes
C = 0
No
Logically reverse R2H, R2L, R3H and R3L
Take on two's complement of the 32-bit binary number placed in R2 and R3 to obtain a negative number.
R3L + #1 → R3L
R3H + #H'00 + C → R3H
R2L + #H'00 + C → R2L
R2H + #H'00 + C → R2H
1
LBL5
RTS

7. Program List

```
*** H8/300 ASSEMBLER VER 1.0B ** 08/18/92 10:17:31
PROGRAM NAME =
                                  ;*****************************************************************
                                  ;*
                                  ;*      00 - NAME   :CHANGE FLOATING POINT TO 32 BIT BINARY
                                  ;*                   (FKTR)
                                  ;*
                                  ;*****************************************************************
                                  ;*
                                  ;*      ENTRY       :R0 (UPPER WORD OF FLOATING POINT)
                                  ;*                   R1 (LOWER WORD OF FLOATING POINT)
                                  ;*
                                  ;*      RETURNS     :R2 (UPPER WORD OF 32 BIT BINARY)
                                  ;*                   R3 (LOWER WORD OF 32 BIT BINARY)
                                  ;*
                                  ;*****************************************************************
                                  ;
FKTR_cod C    0000                       .SECTION             FKTR_code,CODE,ALIGN=2
                                         .EXPORT  FKTR
                                  ;
FKTR_cod C          00000000      FKTR   .EQU $               ;Entry point
FKTR_cod C    0000  79020000             MOV.W    #H'0000,R2  ;Clear R2
FKTR_cod C    0004  0D23                 MOV.W    R2,R3       ;Clear R3
                                  ;
FKTR_cod C    0006  0D00                 MOV.W    R0,R0
FKTR_cod C    0008  4604                 BNE      LBL1
FKTR_cod C    000A  0D11                 MOV.W    R1,R1
FKTR_cod C    000C  4754                 BEQ      LBL5        ;Branch if R0=R1=0
FKTR_cod C    000E                LBL1
FKTR_cod C    000E  7770                 BLD      #7,R0H
FKTR_cod C    0010  670D                 BST      #0,R5L      ;Set sign bit to bit 0 of R5L
FKTR_cod C    0012  7778                 BLD      #7,R0L
FKTR_cod C    0014  1200                 ROTXL.B  R0H         ;Set exporent
FKTR_cod C    0016  F57F                 MOV.B    #H'7F,R5H
FKTR_cod C    0018  1850                 SUB.B    R5H,R0H
FKTR_cod C    001A  4546                 BCS      LBL5        ;Branch if R0H<"H'7F"
FKTR_cod C    001C  A01F                 CMP.B    #H'1F,R0H
FKTR_cod C    001E  4518                 BCS      LBL3        ;Branch if R0H<"H'1F"
FKTR_cod C    0020  770D                 BLD      #0,R5L
FKTR_cod C    0022  450A                 BCS      LBL2        ;Branch if sign bit = 1
FKTR_cod C    0024  79027FFF             MOV.W    #H'7FFF,R2
FKTR_cod C    0028  7903FFFF             MOV.W    #H'FFFF,R3  ;Set "H'7FFFFFFF"
FKTR_cod C    002C  4034                 BRA      LBL5        ;Branch always
FKTR_cod C    002E                LBL2
FKTR_cod C    002E  79028000             MOV.W    #H'8000,R2
FKTR_cod C    0032  79030000             MOV.W    #H'0000,R3  ;Set "H'80000000"
FKTR_cod C    0036  402A                 BRA      LBL5
                                  ;
FKTR_cod C    0038                LBL3
FKTR_cod C    0038  7078                 BSET     #7,R0L      ;Set implicit MSB
FKTR_cod C    003A  8001                 ADD.B    #1,R0H      ;R0H + #1 -> R0H
```

```
FKTR_cod C    003C            LBL4
FKTR_cod C    003C  1009             SHLL.B   R1L          ;Shift mantissa 1 bit left
FKTR_cod C    003E  1201             ROTXL.B  R1H
FKTR_cod C    0040  1208             ROTXL.B  R0L
                              ;
FKTR_cod C    0042  120B             ROTXL.B   R3L         ;Rotate 32 bit binary 1 bit left
FKTR_cod C    0044  1203             ROTXL.B  R3H
FKTR_cod C    0046  120A             ROTXL.B  R2L
FKTR_cod C    0048  1202             ROTXL.B  R2H
FKTR_cod C    004A  1A00             DEC.B    R0H          ;Decrement R0H
FKTR_cod C    004C  46EE             BNE      LBL4         ;Branch if Z=0
                              ;
FKTR_cod C    004E  770D             BLD      #0,R5L       ;Bit load sign bit to C flag
FKTR_cod C    0050  4410             BCC      LBL5         ;Branch if C = 0
FKTR_cod C    0052  1702             NOT      R2H          ;2's complement 32 bit binary
FKTR_cod C    0054  170A             NOT      R2L
FKTR_cod C    0056  1703             NOT      R3H
FKTR_cod C    0058  170B             NOT      R3L
FKTR_cod C    005A  8B01             ADD.B    #H'01,R3L
FKTR_cod C    005C  9300             ADDX.B   #H'00,R3H
FKTR_cod C    005E  9A00             ADDX.B   #H'00,R2L
FKTR_cod C    0060  9200             ADDX.B   #H'00,R2H
FKTR_cod C    0062            LBL5
FKTR_cod C    0062  5470             RTS
                              ;
                                     .END
*****TOTAL ERRORS 0
*****TOTAL WARNINGS 0
```

About Single-Precision Floating-Point Numbers <Reference>

Single-Precision Floating-Point Formats:

1. Internal representation of single-precision floating-point numbers
   In this Application Note, the following formats are applied to single-precision floating-point numbers depending on their values (R = real number):

   A. Internal representation for R = 0

31	30	29	......	2	1	0
0	0	0	......	0	0	0

   All of the 32 bits are 0's.

   B. Normalized format

31	30 ... 23	22 ... 0
S	α	β 0

   α is an exponent whose field is 8 bits long. β is a mantissa whose field is 23 bits long. The value of R can be represented by the following equation (on conditions that $1 \leq \alpha \leq 254$) :

   $R = 2^{S} \times 2^{\alpha-127} \times (1 + 2^{-1} \times \beta_{22} + 2^{-2} \times \beta_{21} + \ldots\ldots + 2^{-23} \times \beta_{0})$

   where βi is the value of the i-th bit ($0 \leq i \leq 22$) and S is the sign bit.

   C. Denormalized format

31	30 ... 23	22 ... 0
S	0 0 0 0 0 0 0 0	β

   where β is a mantissa whose field is 23 bits long. This format is used to represent a real number too small to be represented in the normal format. In this format, R can be represented by the following equation:

   $R = 2^{S} \times 2^{-126} \times (2^{-1} \times \beta_{22} + 2^{-2} \times \beta_{21} + \ldots\ldots + 2^{-23} \times \beta_{0})$

   D. Infinity

31	30 ... 23	22 ... 0
S	1 1 1 1 1 1 1 1	β

   where β is a mantissa whose field is 23 bits long. In this Application Note, however, the following rules apply if all exponents are 1's;

   Positive infinity when S = 0
   $R = + \infty$
   Negative infinity when S = 1
   $R = - \infty$

2. Example of internal representation

If $S = B'0$ (binary)

$\alpha = B'10000011$ (binary)

$\beta = B'1011100......0$ (binary)

Then the corresponding real number is as follows:

$R = 2^{0} \times 2^{131-127} \times (1 + 2^{-1} + 2^{-3} + 2^{-4} + 2^{-5})$

$= 16 + 8 + 2 + 1 + 0.5 = 27.5$

A. Maximum and minimum values

The maximum value (R_{MAX}) and minimum value (R_{MIN}), in terms of the absolute value, are as follows:

$RMAX = 2^{254-127} \times (1 + 2^{-1} + 2^{-2} + 2^{-3} ......+ 2^{-23})$

$= 3.37 \times 10^{38}$

$RMIN = 2^{-126} \times 2^{-23} = 2^{-140} = 1.40 \times 10^{-45}$

The absolute values within the above range can be represented.

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http://www.renesas.com/inquiry
csc@renesas.com

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