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SH7262/SH7264 Group

Controller Area Network, Configuration to Receive Data Frames

Summary

This application note describes the configuration example of the SH7264 microcomputers (MCUs) to receive data frames using the Controller Area Network.

Target Device

SH7264 MCU (In this document, SH7262/SH7264 are described as "SH7264".)

Contents

1. Introduction

1.1 Specifications

- Uses the Controller Area Network channel 1
- Transmission speed: 1 Mbps
- Receive mailbox: Mailbox 0
- Receives the data frame with following specifications
  Identifier: 0; standard data frame; DLC: 2; Data: H'C1C2

1.2 Modules Used

- Controller Area Network (CAN) module

1.3 Applicable Conditions

MCU	SH7262/SH7264
Operating Frequencies	Internal clock: 144 MHz Bus clock: 72 MHz Peripheral clock: 36 MHz
Integrated Development Environment	Renesas Technology Corp. High-performance Embedded Workshop Ver.4.07.00
C Compiler	Renesas Technology SuperH RISC engine Family C/C++ Compiler Package Ver.9.03 Release 00
Compiler Options	Default setting in the High-performance Embedded Workshop (-cpu=sh2afpu -fpu=single -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 –nologo)

1.4 Related Application Notes

For more information, refer to the following application notes:

- SH7262/SH7264 Group Controller Area Network, Configuration to Transmit Data Frames
- SH7262/SH7264 Group Controller Area Network, Configuration to Transmit Remote Frames
- SH7262/SH7264 Group Controller Area Network, Configuration to Receive Remote Frames

2. Applications

This application note uses the Controller Area Network to receive a standard data frame with identifier 0.

2.1 CAN Overview

The SH7264 includes two channels of a CAN module which is compliant with the CAN protocol, version 2.0B active, and ISO 11898.

The CAN module has 31 programmable mailboxes for transmission/reception, one mailbox for reception, and one programmable receive filtering mask to provide flexible communication procedure. Figure 1 shows the CAN block diagram. For more details refer to the Controller Area Network chapter in the SH7262 Group, SH7264 Group Hardware Manual.

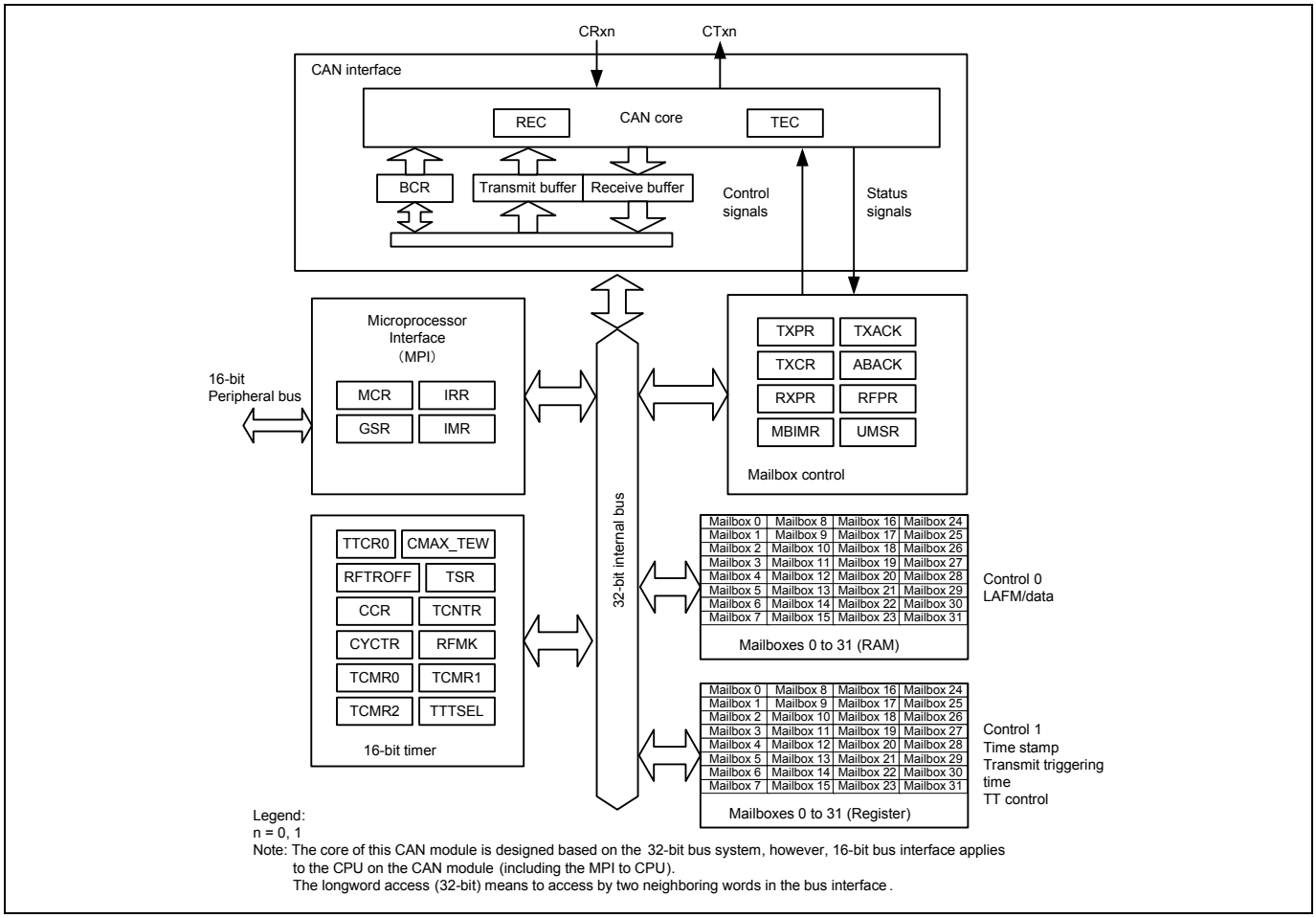


Figure 1 CAN Block Diagram (For One Channel)

2.2 Configuration Procedure

This section describes how to configure the SH7264 MCU to receive data frames using the CAN module channel 1.

Configure the CAN module in reset mode (configuration mode). After configuration is complete, clear the reset mode to join the CAN bus activity. The sample program sets two mailboxes in SH7264 - one transmit mailbox and one receive mailbox. Figure 2 and Figure 3 show the flow charts for configuring the CAN module. For details on register settings, refer to the Controller Area Network chapter in the SH7262 Group, SH7264 Group Hardware Manual.

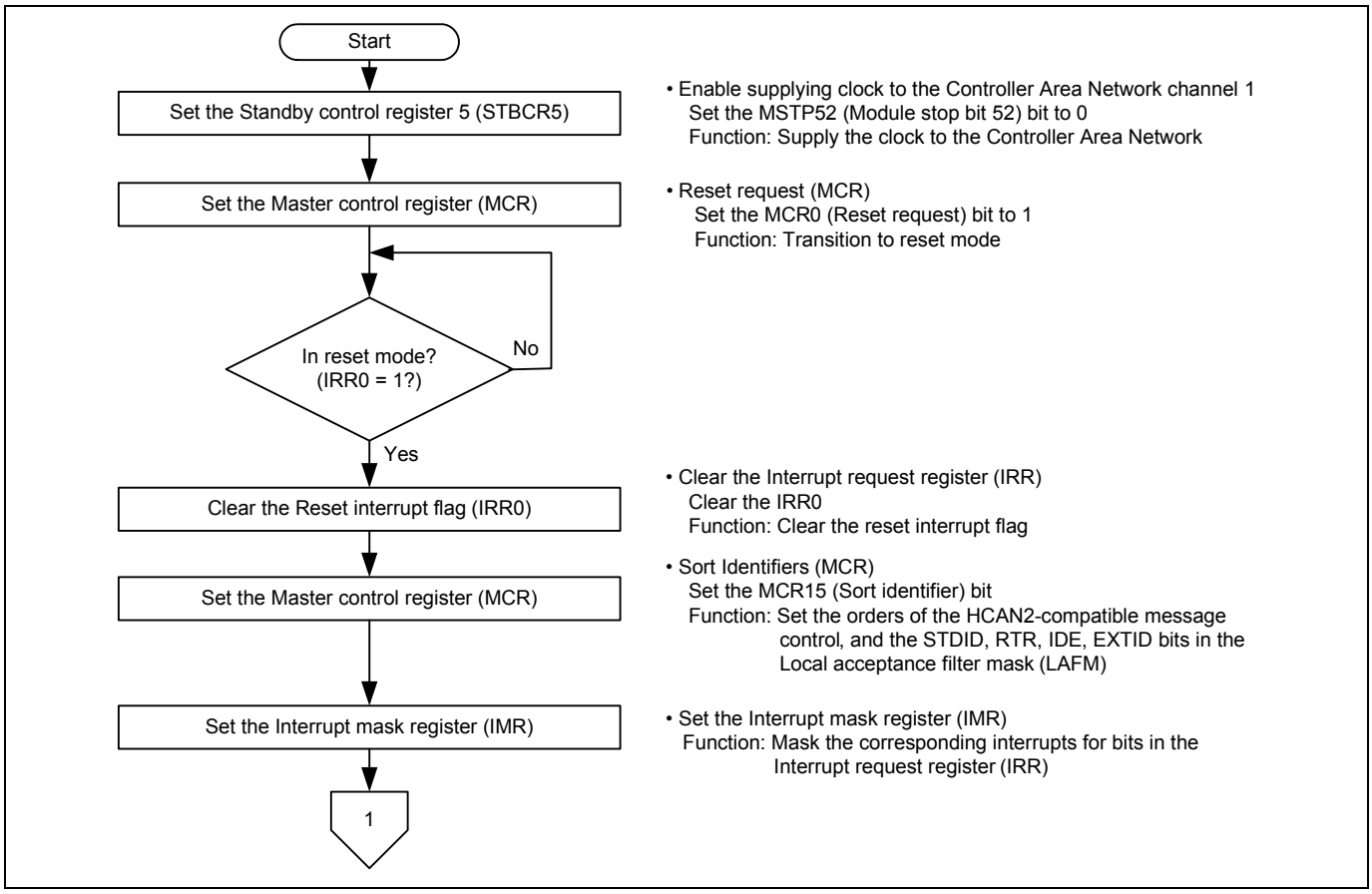
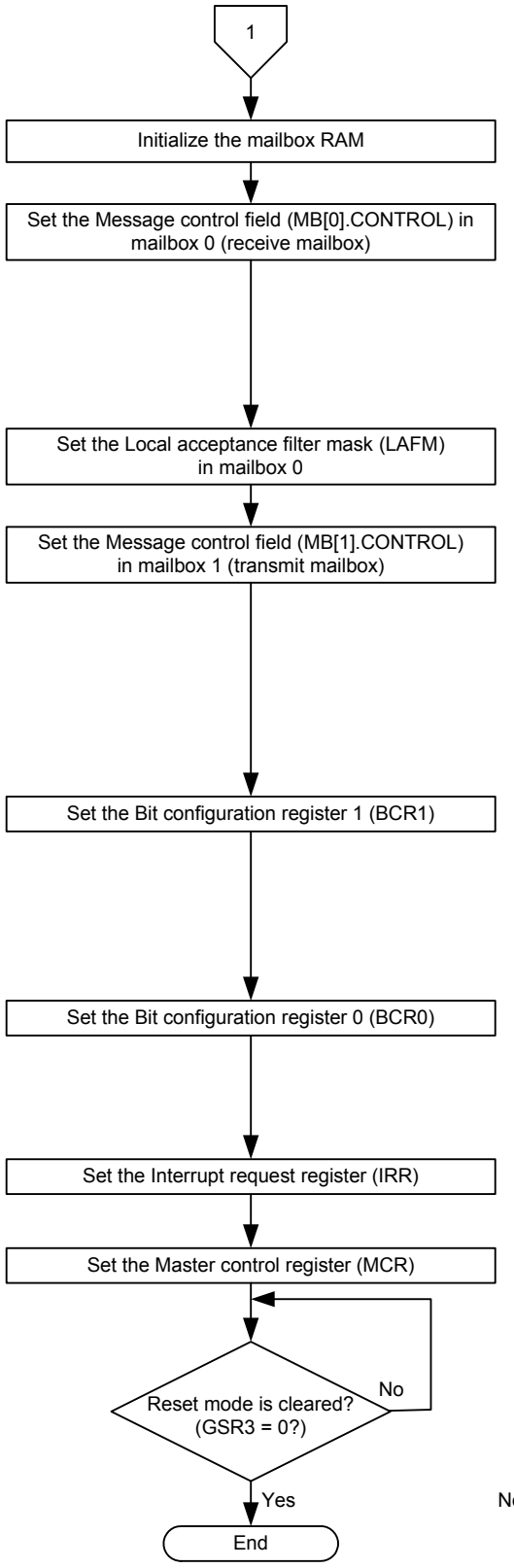


Figure 2 Flow Chart for Configuring the CAN Module (1/2)



• Clear the RAM area in the mailbox

• Set the Message control register (MB[0].CONTROL)
Specify "B'010" in MBC [2:0] bits (Mailbox configuration)
Function: Receiving a remote frame or a data frame is enabled
Specify "0" in the IDE bit (Identifier extension)
Function: Specify the standard format
Specify "0" in the RTR bit (Remote transmission request)
Function: Specify a data frame
Specify "0" in STDID [10:0] bits (Standard Identifier)
Function: Specify 0 as the ID

• Set the Local acceptance filter mask (LAFM)
Set "H'0000 0000" in the LAFM
Function: Mask is not specified

• Set the Message control register (MB[1].CONTROL) (1)
Specify "B'000" in MBC [2:0] bits (Mailbox configuration)
Function: Transmitting a remote frame or a data frame is enabled
Specify "B'010" in the DLC bit (Data length code)
Function: Specify the data length as 2 bytes
Specify "0" in the IDE bit (Identifier extension)
Function: Specify the standard format
Specify "0" in the RTR bit (Remote transmission request)
Function: Specify a data frame
Specify "0" in STDID [10:0] bits (Standard Identifier)
Function: Specify 0 as the ID

• Set the Bit configuration register 1 (BCR1)
Specify "B'1001" (10 time quanta) in TSG1 [3:0] bits (Time segment 1)
Specify "B'110" (7 time quanta) in TSG2 [2:0] bits (Time segment 2)
Specify "B'00" (1 time quantum) in SJW [1:0] bits (Resynchronization jump width)
Function: Avoid moving the sample point substantially
Set the BSP (Bit sample point)
Function: Specify to sample at one point or to sample at three points and decide by majority of them

• Set the Bit configuration register 0 (BCR0)
Specify "B'0000 0000" in BRP [7:0] bits (Baud rate prescaler)
Function: Specify 1 time quantum as 2 × peripheral bus clock
Specify the transfer speed as 1 Mbps by TSG1, TSG2 and the baud rate prescaler
(Refer to 2.3 Bit Configuration and Transmission Speed)

• Clear the Interrupt request register (IRR)
Clear IRR0 to IRR15 bits
Function: Clear interrupt flags

• Set the Master control register (MCR)
Clear the MCR0 bit (Reset request)
Function: Clear the reset mode transition request
Clear the MCR1 bit (Halt request)
Function: Clear the halt mode transition request

Note 1: This operation is not required in receiving data, however, this sample program assumes both transmission and reception.

Figure 3 Flow Chart for Configuring the CAN Module (2/2)

2.3 Bit Configuration and Transmission Speed

One bit in the CAN module consists of the following four segments:

1. Synchronization segment (SS)
2. Propagation time segment (PRSEG)
3. Phase buffer segment 1 (PHSEG1)
4. Phase buffer segment 2 (PHSEG2)

Each segment is composed of the reference time Tq (time quanta). Figure 4 shows the bit configuration example when SS = 1 Tq, PRSEG = 8 Tq, PHSEG1 = 8 Tq, and PHSEG2 = 8 Tq.

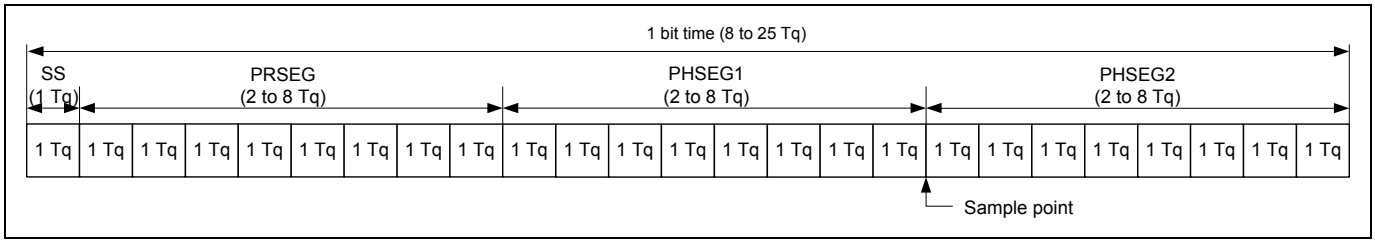


Figure 4 Bit Configuration

The CAN module sets the number of Tqs of PRSEG + PHSEG1 to bits TSG1 [3:0] in the BCR1 register, and the number of Tqs of PSEG2 to bits TSG2 [2:0] in this register (Value + 1 is the number of Tqs). Also, the number of peripheral bus clocks for 1 Tq is set to bits BRP [7:0] in the BCR0 register.

In the following description, bits BRP [7:0], TSEG1 [3:0], and TSEG2 [2:0] are register values, and bits BRP, TSEG1, TSEG2, and SJW are the corresponding values for the register values. For the corresponding values for register values, refer to the Controller Area Network chapter in the SH7262 Group, SH7264 Group Hardware Manual.

The CAN module defines $1\,\mathrm{Tq} = \frac{2\times(\mathrm{BRP}[7:0]+1)}{\text{Peripheral bus clock}}$ By this formula, the transmission speed is calculated as follows:

$$\text{Transmission speed} = \frac{\text{Peripheral bus clock}}{2\times(\mathrm{BRP}[7:0]+1)\times\text{the number of Tqs/bit}}$$

$$= \frac{\text{Peripheral bus clock}}{2\times(\mathrm{BRP}[7:0]+1)\times\{(\mathrm{TSEG}[3:0]+1)+(\mathrm{TSEG2}[2:0]+1)+1\}}$$

Following is the restriction on setting the bit configuration register.

TSEG1 (Min.) > TSEG2 ≥ SJW (Max.) (SJW = 1 to 4)

SJW is the resynchronization jump width. It is a segment that lengthens phase buffer segment 1 or shortens phase buffer segment 2 to correct the phase difference.

8 ≤ TSEG1 + TSEG2 + 1 ≤ 25 time quanta
TSEG2 ≥ 2

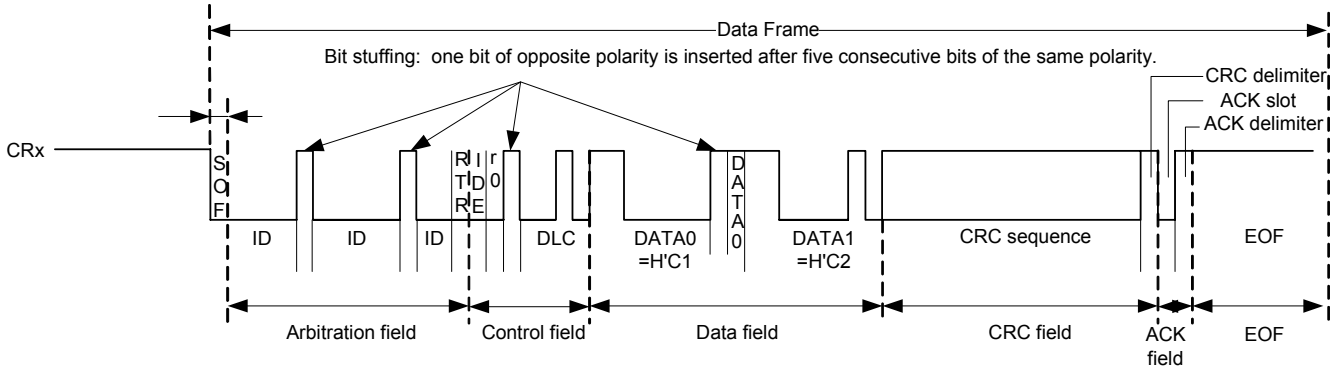
As this sample program specifies the peripheral bus clock as 36 MHz, BRP [7:0] = 0, TSEG 1 [3:0] = 9, and TSEG2 [2:0] = 6, the transmission speed is calculated as follows:

$$\text{Transmission speed} = \frac{36M}{2\times(0+1)\times\{(9+1)+(6+1)+1\}} = 1M....1\ \text{Mbps}$$

2.4 Sample Program Operation

This sample program receives a standard data frame in mailbox 0 at 1 Mbps. Figure 5 shows the reception waveform.

Note: The sample program transmits and receives data frames, however, this application note describes only the reception.



Legend:

SOF (Start of frame): Indicates the beginning of a data frame or remote frame
ID (Identifier): Indicates the data priority
RTR (Remote transmission request): Indicates differences between a data frame and a remote frame
IDE (Identifier extension): Indicates that it is the standard format or extended format
r0: This is a reserved bit.
DLC (Data length code): Indicates the number of bytes in the Data field (0 to 8 bytes can be specified.)
DATA: This is the data to transfer. Number of bytes DATA specified by the DLC is transferred.
CRC sequence: This is the value for frame check.
CRC delimiter: Delimits the CRC field and ACK field
ACK slot: When the transmitted message includes no error, this is overwritten by a dominant.
ACK delimiter: Delimits the ACK field and EOF
EOF (End of frame): Indicates the end of a frame

Figure 5 CAN Reception Waveform

2.5 Sample Program Procedure

The following table lists setting example of the CAN. Figure 6 shows the configuration flow chart of this sample program.

Note: The sample program transmits and receives data frames, however, this application note describes only the reception.

Table 1 Controller Area Network Settings

Register Name	Address	Setting	Description
Standby control register (STBCR5)	H'FFFE 0410	H'FB	MSTP52 = "0": Controller Area Network channel 1 is operating
Master control register (MCR)	H'FFFF 5800	H'0001	MCR0 = "1": Reset mode transition request
		H'8001	MCR15 = "1": The order of the RCAN message and of the HCAN2 message are different
		H'8000	MCR0 = "0": Reset mode is cleared
Interrupt mask register (IMR)	H'FFFF 580A	H'FFFF	All interrupts in the Controller Area Network are disabled
Bit configuration register 1 (BCR1)	H'FFFF 5804	H'9600	TSEG1 [3:0] = "B'1001": PRSEG + PHSEG1 = 10 Tq TSEG2 [2:0] = "B'110": PHSEG2 = 7 Tq SJW = "0": SJW = 1 Tq BSP = "0": Bit sampling at one point
Bit configuration register 0 (BCR0)	H'FFFF 5806	H'0000	BRP [7:0] = "0": 1 Tq = 2 × Pφ
Message control field in mailbox 0 (MB[0].CONTROL1)	H'FFFF 5910	H'0200	MBC [2:0] = "B'010": Receiving the data frame or remote frame is enabled
Message control field in mailbox 0 (MB[0].CONTROL0)	H'FFFF 5900	H'0000 0000	IDE = "0": Standard format RTR = "0": Data frame STDID [10:0] = "0": Standard identifier is 0
Message control field in mailbox 1 (MB[1].CONTROL1)	H'FFFF 5930	H'0002	MBC [2:0] = "B'000": Transmitting the data frame or remote frame is enabled DLC [3:0] = "B'0010": Data length is 2 bytes
Message control field in mailbox 1 (MB[1].CONTROL0)	H'FFFF 5920	H'0000 0000	IDE = "0": Standard format RTR = "0": Data frame STDID [10:0] = "0": Standard identifier is 0
Local acceptance filter mask in mailbox 0 (MB[0].LAFM)	H'FFFF 5904	H'0000 0000	Clear: Mask is not specified
Message data field in mailbox 1 (MB[1].MSG_DATA_0)	H'FFFE 5928	H'0000	Clear the data field (Clear the RAM area)
Data frame receive pending register (RxPR0)	H'FFFF 5842	H'0001	RXPR [31:0] = H'0001: Clear the receive pending flag

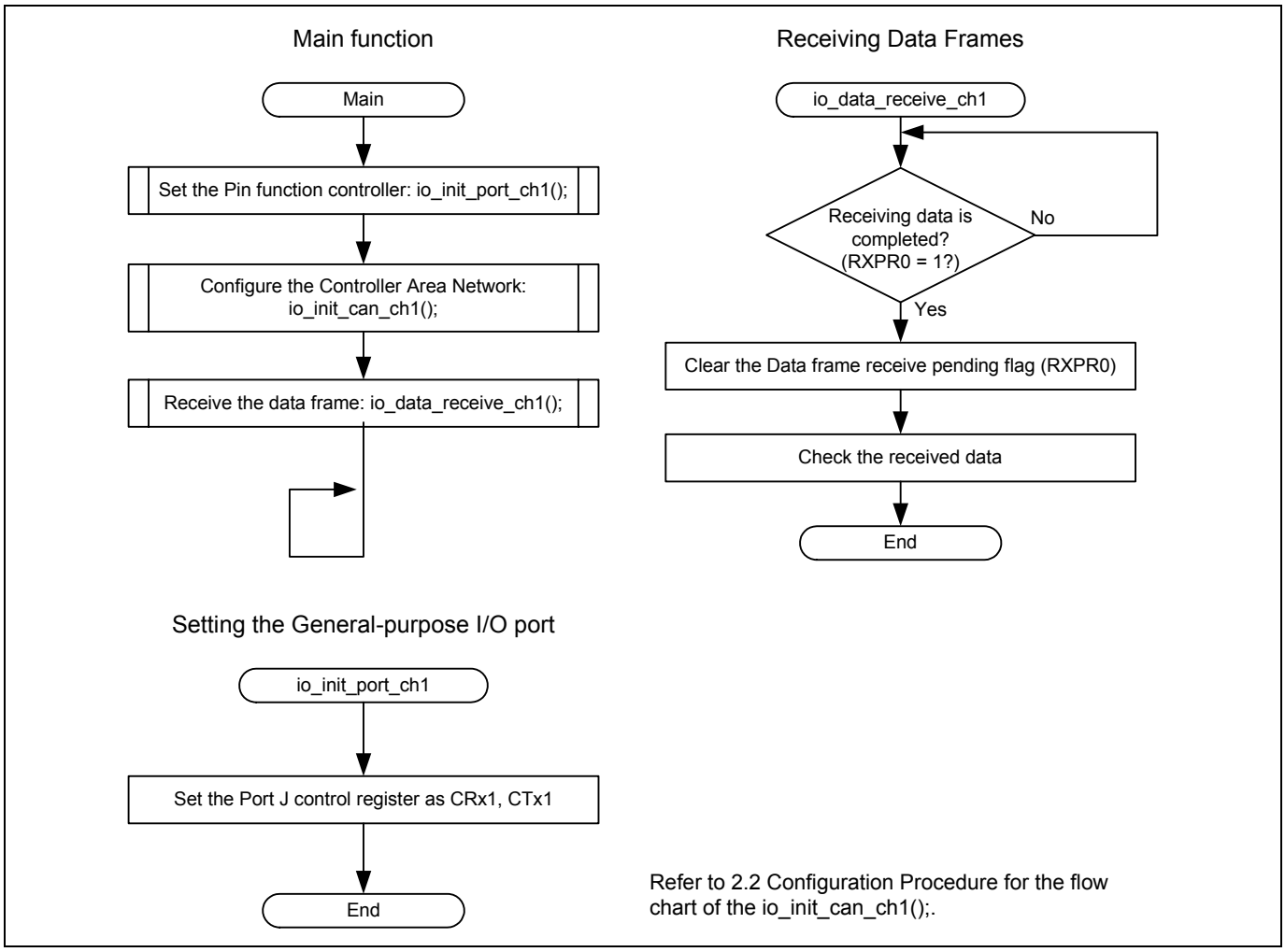


Figure 6 Sample Program Flow Chart

3. Sample Program Listing

3.1 Supplement to the Sample Program

As the capacity of the SH7264 large-capacity internal RAM varies as 1 MB or 640 KB, depending on the MCU type, the section alignment and register setting must be partly altered. To support both MCU types, this application note provides two types of sample programs (workspaces) for 1-MB RAM and 640-KB RAM.

As the MCU with 640-KB RAM must be write-enabled before writing data in the data-retention RAM, the System control register 5 (SYSCR5) is set to write-enable the RAM in the sample program for 640-KB RAM.

Review your product and use the appropriate workspace.

3.2 Sample Program Listing "main.c" (1/2)

```
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27      ************************************************************************
28      *   Copyright (C) 2009. Renesas Technology Corp., All Rights Reserved.
29      *""FILE COMMENT""*********** Technical reference data *********************
30      *   System Name : SH7264 Sample Program
31      *   File Name   : main.c
32      *   Abstract    : CAN Module Application (Data Frame Transmit and Receive)
33      *   Version     : 1.00.00
34      *   Device      : SH7262/SH7264
35      *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.07.00).
36      *               : C/C++ compiler package for the SuperH RISC engine family
37      *               :                             (Ver.9.03 Release00).
38      *   OS          : None
39      *   H/W Platform: M3A-HS64G50 (CPU board) + M3A-HS64G02 (IO board)
40      *   Description :
41      ************************************************************************
42      *   History     : Nov.20,2009 ver.1.00.00
43      *""FILE COMMENT END""*****************************************************/
44      #include "iodefine.h"       /* SH7264 iodefine  */
45
```

3.3 Sample Program Listing "main.c" (2/2)

```
46    /* ---- prototype declaration ---- */
47    void main(void);
48    extern void io_init_port_ch0(void);
49    extern void io_init_port_ch1(void);
50    extern void io_init_can_ch0(void);
51    extern void io_init_can_ch1(void);
52    extern void io_data_send_ch0(void);
53    extern void io_data_receive_ch1(void);
54
55    /*""FUNC COMMENT""*****************************************************************
56     * ID            :
57     * Outline       : Sample program main
58     *-------------------------------------------------------------------------------
59     * Include       : "iodefine.h"
60     *-------------------------------------------------------------------------------
61     * Declaration   : void main(void);
62     *-------------------------------------------------------------------------------
63     * Description   : After configuring the Controller Area Network (RCAN), channel 0
64     *               : transmits the data frame, and channel 1 receives the data frame.
65     *-------------------------------------------------------------------------------
66     * Argument      : void
67     *-------------------------------------------------------------------------------
68     * Return Value  : void
69     *-------------------------------------------------------------------------------
70     * Note          :
71     *""FUNC COMMENT END""*************************************************************/
72    void main(void)
73    {
74        /* ==== Initializing port ==== */
75        io_init_port_ch1();
76        io_init_port_ch0();
77
78        /* ==== Initializing CAN module ==== */
79        io_init_can_ch1();
80        io_init_can_ch0();
81
82        /* ==== CAN data frame transmission ==== */
83        io_data_send_ch0();
84
85        /* ==== CAN data frame reception ==== */
86      io_data_receive_ch1();
87
88        while(1){
89            /* loop */
90        }
91    }
92
93    /* End of File */
94
```

3.4 Sample Program Listing "can1.c" (1/5)

```
1     /***********************************************************************
2     *   DISCLAIMER
3     *
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27    ***********************************************************************
28    *   Copyright (C) 2009. Renesas Technology Corp., All Rights Reserved.
29    *""FILE COMMENT""*********** Technical reference data *************************
30    *   System Name : SH7264 Sample Program
31    *   File Name   : can1.c
32    *   Abstract    : CAN Module Application (Data Frame Receive)
33    *   Version     : 1.00.00
34    *   Device      : SH7262/SH7264
35    *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.07.00).
36    *               : C/C++ compiler package for the SuperH RISC engine family
37    *               :                             (Ver.9.03 Release00).
38    *   OS          : None
39    *   H/W Platform: M3A-HS64G50 (CPU board) + M3A-HS64G02 (IO board)
40    *   Description :
41    ***********************************************************************
42    *   History     : Nov.20,2009 ver.1.00.00
43    *""FILE COMMENT END""*****************************************************/
44    #include "iodefine.h"       /* SH7264 iodefine  */
45
```

3.5 Sample Program Listing "can1.c" (2/5)

```
46    /* ---- prototype declaration ---- */
47    void io_init_port_ch1(void);
48    void io_init_can_ch1(void);
49    void io_data_receive_ch1(void);
50
51    /* ---- symbol definition ---- */
52    #define CAN_GSR3 0x0008
53    #define CAN_IRR0 0x0001
54    #define CAN_MB0  0x0001
55    #define CAN_MB1  0x0002
56    #define CAN_MB01 0x00000002
57
58    /* ---- RAM allocation variable declaration ---- */
59    unsigned char   nIDE = 0;           /* ide */
60    unsigned char   nRTR = 0;           /* rtr */
61    unsigned char   nDLC = 0;           /* dlc */
62    unsigned int    nSID = 0;           /* sid */
63    unsigned int    nEID = 0;           /* eid */
64    unsigned char   gRcv_data[8];       /* data of message */
65
66    /*""FUNC COMMENT""*****************************************************************
67     * ID            :
68     * Outline       : PORT setting
69     *-------------------------------------------------------------------------------
70     * Include       : "iodefine.h"
71     *-------------------------------------------------------------------------------
72     * Declaration   : void io_init_port_ch1(void);
73     *-------------------------------------------------------------------------------
74     * Description   : Set pin functions (CRx1 input, and CTx1 output).
75     *-------------------------------------------------------------------------------
76     * Argument      : void
77     *-------------------------------------------------------------------------------
78     * Return Value  : void
79     *-------------------------------------------------------------------------------
80     * Note          :
81     *""FUNC COMMENT END""*************************************************************/
82    void io_init_port_ch1(void)
83    {
84        /* ==== Setting of PORT ==== */
85      PORT.PJCR0.BIT.PJ2MD = 0x1;     /* Set CTx1 */
86        PORT.PJCR0.BIT.PJ3MD = 0x1;     /* Set CRx1 */
87    }
88
```

3.6 Sample Program Listing "can1.c" (3/5)

```
/*""FUNC COMMENT""*****************************************************************
 * ID            :
 * Outline       : RCAN setting
 *-----------------------------------------------------------------------------
 * Include       : "iodefine.h"
 *-----------------------------------------------------------------------------
 * Declaration   : void io_init_can_ch1(void);
 *-----------------------------------------------------------------------------
 * Description   : Configure the Controller Area Network (RCAN) channel 1.
 *               : Transfer rate is set as 1 Mbps.
 *-----------------------------------------------------------------------------
 * Argument      : void
 *-----------------------------------------------------------------------------
 * Return Value  : void
 *-----------------------------------------------------------------------------
 * Note          :
 *""FUNC COMMENT END""*************************************************************/
void io_init_can_ch1(void)
{
    int i,j;

  /* ==== Setting of power down mode(RCAN) ==== */
  CPG.STBCR5.BIT.MSTP52 = 0;                /* Module Standby Clear (RCAN1)*/

  /* ==== Initializing CAN module ==== */
    RCAN1.MCR.WORD |= 0x0001;           /* CAN Interface reset mode */
    while((RCAN1.IRR.WORD & CAN_IRR0) != CAN_IRR0){
        /* Reset state waiting */
    }
    /* ==== IRR = 1, GSR = 1 (Auto SET) ==== */

    /* ---- Clear IRR0 ---- */
    RCAN1.IRR.WORD = 0x0001;

    /* ---- RCAN mode selection(MCR15) ---- */
    RCAN1.MCR.WORD |= 0x8000;           /* RCAN is not same as HCAN2 */

    /* ---- Disable all can interrupt ---- */
    RCAN1.IMR.WORD  = 0xffff;

    /* ----All mailbox init ---- */
    for(i = 0; i < 32; i++){
        RCAN1.MB[i].CONTROL0.LONG = 0x00000000;
        RCAN1.MB[i].LAFM.LONG = 0x00000000;
        for(j = 0; j < 8; j++){
            RCAN1.MB[i].MSG_DATA[j] =  0x00;
        }
    }
```

3.7 Sample Program Listing "can1.c" (4/5)

```
137
138         /* ---- Config mailbox0 as reception slot ---- */
139         RCAN1.MB[0].CONTROL1.WORD = 0x0200;       /* CAN receive data and remote frame */
140         RCAN1.MB[0].CONTROL0.LONG = 0x00000000;   /* Initialize the Message Control Field */
141         RCAN1.MB[0].LAFM.LONG = 0x00000000;
142         for(i = 0; i < 8; i++){                 /* data clear */
143             RCAN1.MB[0].MSG_DATA[i] =  0x00;
144         }
145         /* ---- Config mailbox1 as transmission slot ---- */
146         RCAN1.MB[1].CONTROL1.WORD = 0x0002;       /* CAN send data or remote frame, dlc=2 */
147         RCAN1.MB[1].CONTROL0.LONG = 0x00000000;   /* standard data frame, id=0x000 */
148         RCAN1.MB[1].LAFM.LONG = 0x00000000;
149         for(i = 0; i < 8; i++){                 /* data clear */
150             RCAN1.MB[1].MSG_DATA[i] =  0x00;
151         }
152
153         /* ---- Config baudrate ---- */
154         RCAN1.BCR1.WORD = 0x9600;      /* tsg1=9(10bit),tsg2=6(7bit),sjw=0(1bit),bsp=0 */
155         RCAN1.BCR0.WORD = 0x0000;      /*   1 Mbps */
156     //  RCAN1.BCR0.WORD = 0x0001;      /* 500 Kbps */
157     //  RCAN1.BCR0.WORD = 0x0003;      /* 250 Kbps */
158     //  RCAN1.BCR0.WORD = 0x0007;      /* 125 Kbps */
159
160         /* ---- Clear interrupt flags ---- */
161         RCAN1.IRR.WORD = 0xffff;
162
163         /* ---- Clear reset and halt ---- */
164         RCAN1.MCR.WORD &= 0xf8fc;      /* MCR0, MCR1 clear */
165         while( (RCAN1.GSR.WORD & CAN_GSR3) != 0x0000 ){
166             /* Reset state is end */
167         }
168     }
169
```

3.8 Sample Program Listing "can1.c" (5/5)

```
/*""FUNC COMMENT""*****************************************************************
 * ID            :
 * Outline       : Data frame receive
 *-----------------------------------------------------------------------------
 * Include       : "iodefine.h"
 *-----------------------------------------------------------------------------
 * Declaration   : void io_data_receive_ch1(void);
 *-----------------------------------------------------------------------------
 * Description   : After completing to receive the data frame, this function
 *               : stores the mailbox 0 received data in the gRcv_data[i].
 *-----------------------------------------------------------------------------
 * Argument      : void
 *-----------------------------------------------------------------------------
 * Return Value  : void
 *-----------------------------------------------------------------------------
 * Note          :
 *""FUNC COMMENT END""*************************************************************/
void io_data_receive_ch1(void)
{
    int i;

    /* ---- Reception completion waiting ---- */
    while((RCAN1.RXPR0.WORD & CAN_MB0) != CAN_MB0){
    }

    /* ---- Receive data storage ---- */
    nIDE = RCAN1.MB[0].CONTROL0.BIT.IDE;
    nRTR = RCAN1.MB[0].CONTROL0.BIT.RTR;
    nDLC = RCAN1.MB[0].CONTROL1.BIT.DLC;
    nSID = RCAN1.MB[0].CONTROL0.BIT.STDID;
    nEID = RCAN1.MB[0].CONTROL0.BIT.EXTID;
    if(nDLC > 8){
        nDLC = 8;
    }
    for(i = 0; i < nDLC; i++){
        gRcv_data[i] = RCAN1.MB[0].MSG_DATA[i];
    }

    /* ---- Reception completion flag clear ---- */
    RCAN1.RXPR0.WORD = CAN_MB0;
}

/* End of File */
```

4. References

- Software Manual
  SH-2A/SH2A-FPU Software Manual Rev. 3.00
  The latest version of the software manual can be downloaded from the Renesas website.

- Hardware Manual
  SH7262 Group, SH7264 Group Hardware Manual Rev. 2.00
  The latest version of the hardware manual can be downloaded from the Renesas website.

Website and Support

Renesas Technology Website
http://www.renesas.com/

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Revision History

		Description	
Rev.	Date	Page	Summary
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