Configuring VersaClock 7 for Low-Power Mode with the RICBox GUI Software

This document describes how to configure a VersaClock 7 (VC7) device for low-power consumption. The Renesas IC Toolbox (RICBox) software platform is used to configure the device.

Placing a VC7 device into a low-power state disables most of its internal logic in order to conserve power, while allowing the power rails of the device to remain active. This feature allows users to initiate operation of the device when the output of the power supply to the device has reached the level required for maximum performance. This feature also allows users to place the device into a low-power state with the current configuration and operating state ready to be resumed upon being taken out of the low-power state.

Contents

1. Power Down vs. Restart

The VersaClock 7 supports the use of both the Power-Down feature and the Restart feature. Both features rely on an active-low input applied to one of the GPI/GPIO inputs (Note: only GPIO 0-2 will support the Power-Down feature).

The Restart feature can be assigned to any GPI or GPIO pin and can work with any configuration type (Single Config, Multi Config, etc.). When the assigned input pin is set low, the device is in full reset, all configuration registers are reset to their initial states, and the start-up sequence is re-initialized. When set high, the device initialization continues.

The Power-Down feature relies on a copy of the power-on configuration that has been modified to reduce power consumption as low as possible. For this reason, DynamicMultiConfig must be used when using the Power-Down feature. There can be a low-power version for each configuration to be used on the device. When the assigned GPIO pin is set low, the device enters the appropriate low-power configuration determined by the status of the other GPIO pins. When set high, the device enters the power-on configuration determined by the status of the other GPIO pins.

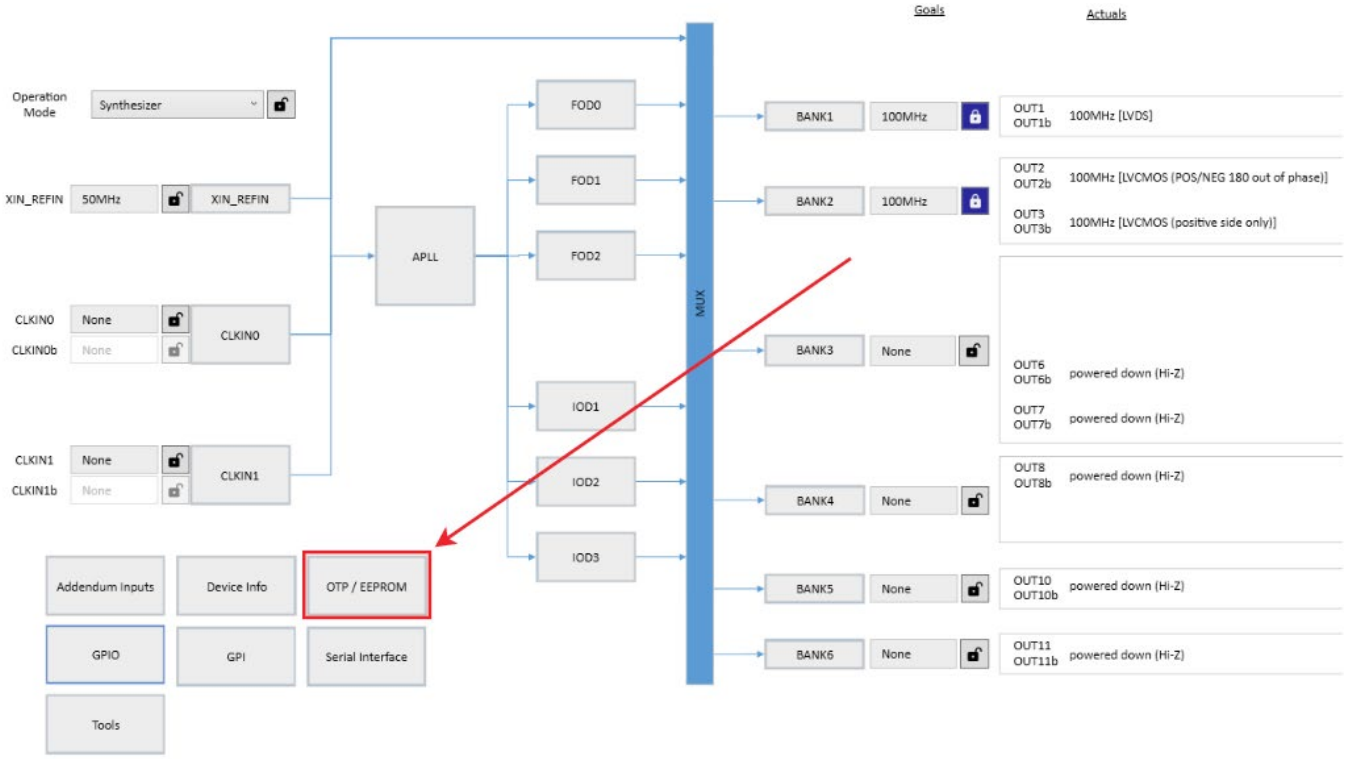
2. Using RICBox to Create a Power-Down Configuration

The RICBox is a software package that allows the user to create configurations for the VC7 device. For more information on RICBox, see the Renesas IC Toolbox Software Manual. For more information on how to use RICBox with the VC7 device, see the RICBox GUI Software for VersaClock 7 Software Manual. This document assumes the user is familiar with creating a configuration for the VC7 with RICBox, and focuses on the steps required to modify the configuration to allow for low-power consumption.

While this document applies to all VC7 devices, for the purpose of this application note, the RC21008A device was chosen for example purposes.

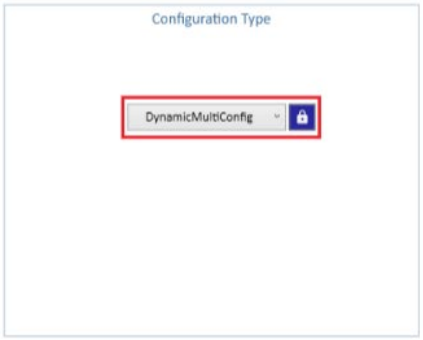
3. Creating the Power-Down Configuration

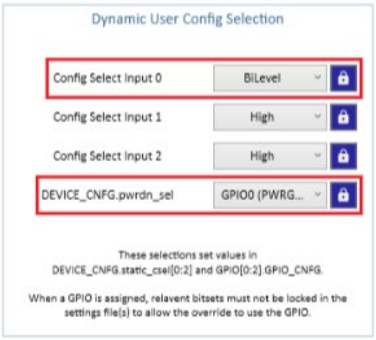
1. Starting with an open configuration file, click on the “OTP / EEPROM” button.

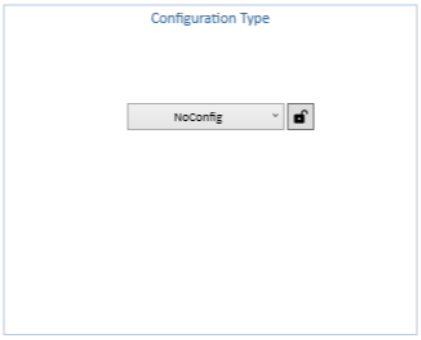


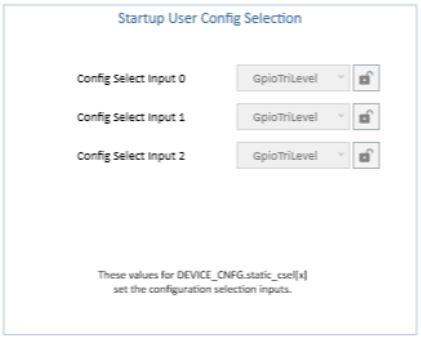
This will open a dialog box for the configuration screen on the following page.

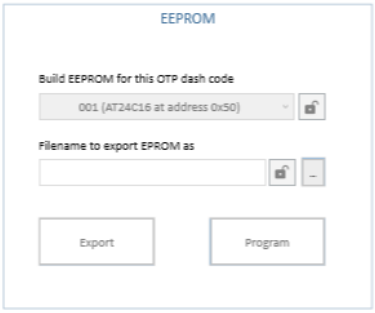
2. Set the “Configuration Type” to DynamicMultiConfig. In the “Dynamic User Config Selection” box, set the DEVICE_CNFG.pwrdn_sel field to the appropriate GPIO pin and function. For this document, GPIO0 was selected as the input pin and the PWRGD/PWRDN# function is used. The Config Select Input associated with the GPIO pin must be set to BiLevel (in this case, Config Select Input 0). Unused Config Select Inputs should be tied high.



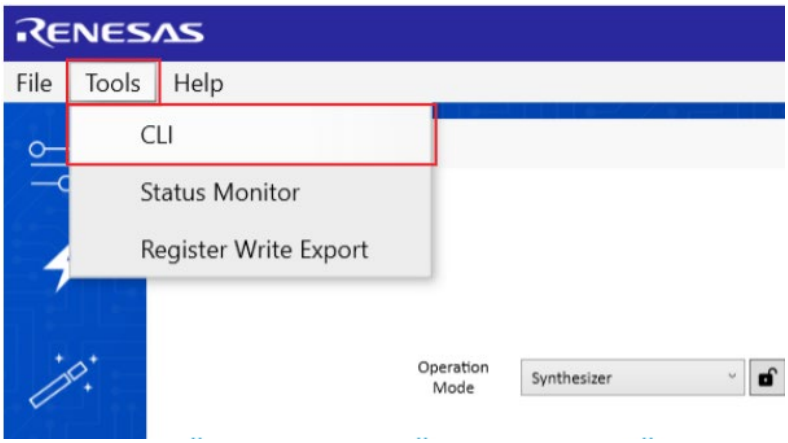




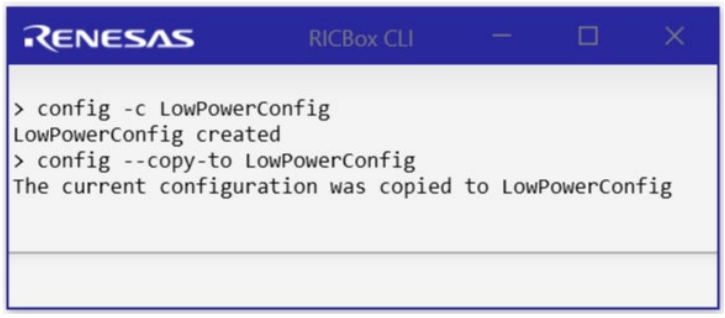




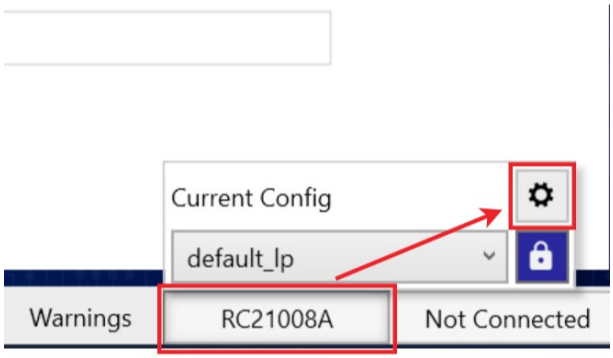
3. Return to the Block Diagram and click on “Tools > CLI”.



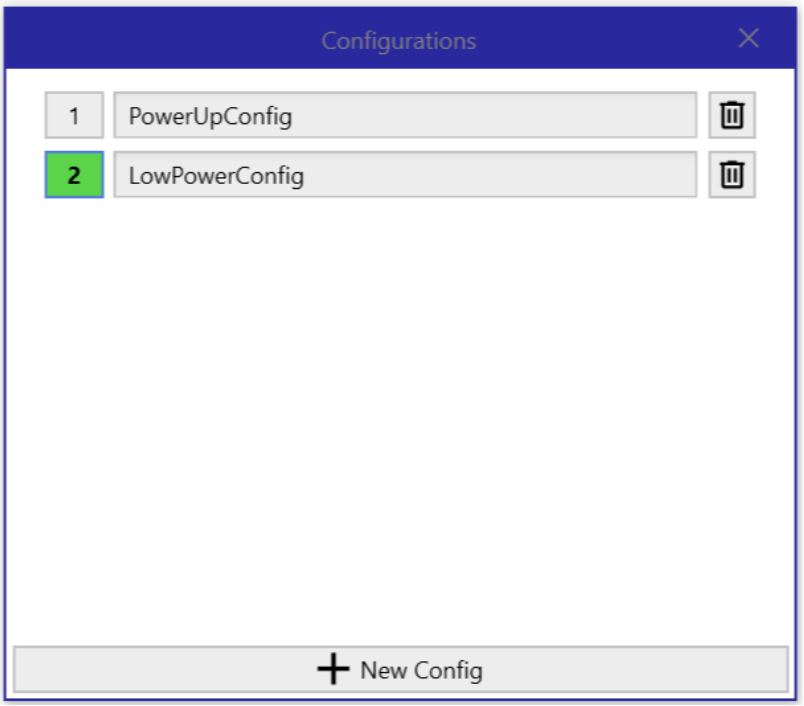
4. Enter “config -c LowPowerConfig” and press enter to create the low-power configuration. Enter “config –copy-to LowPowerConfig” and press enter to make a copy of the current power on configuration that can then be modified for low-power consumption.



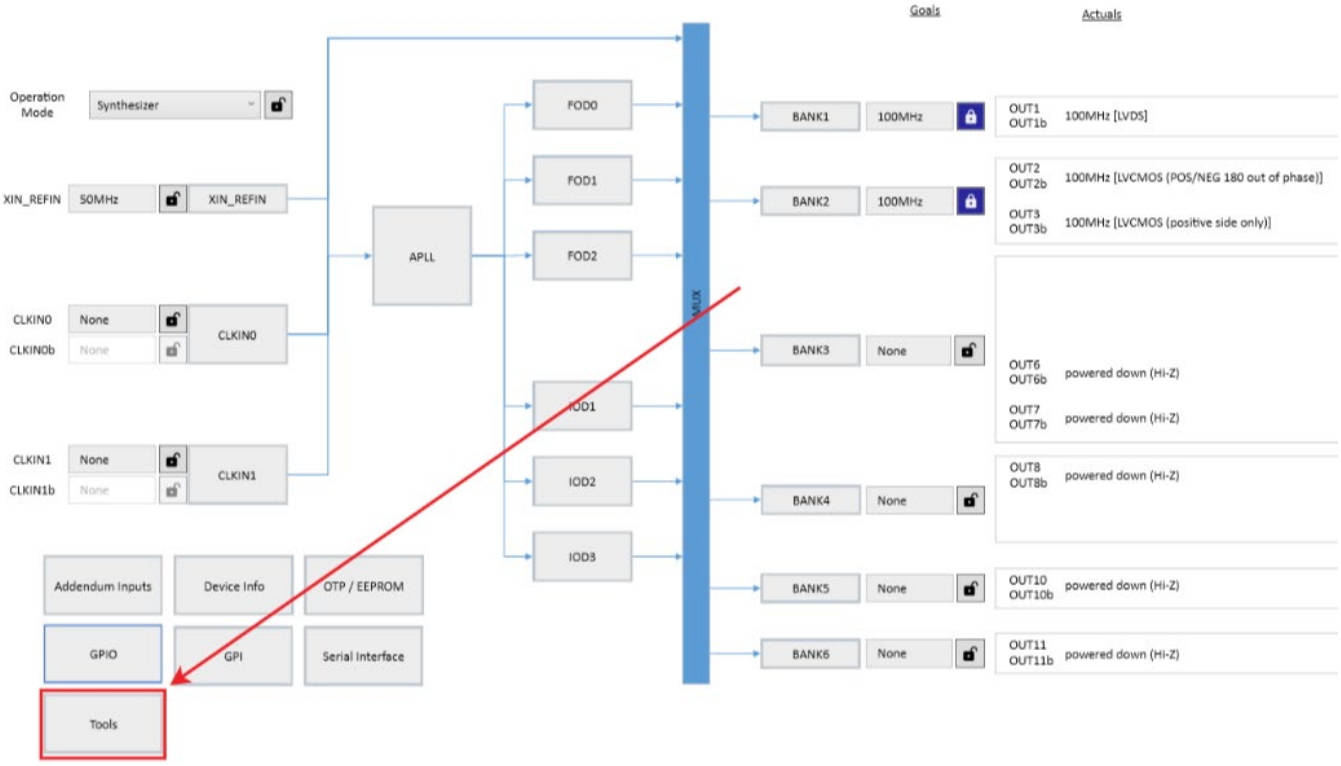
5. In the lower-right corner of the GUI, click on the part number box to view the current configuration.



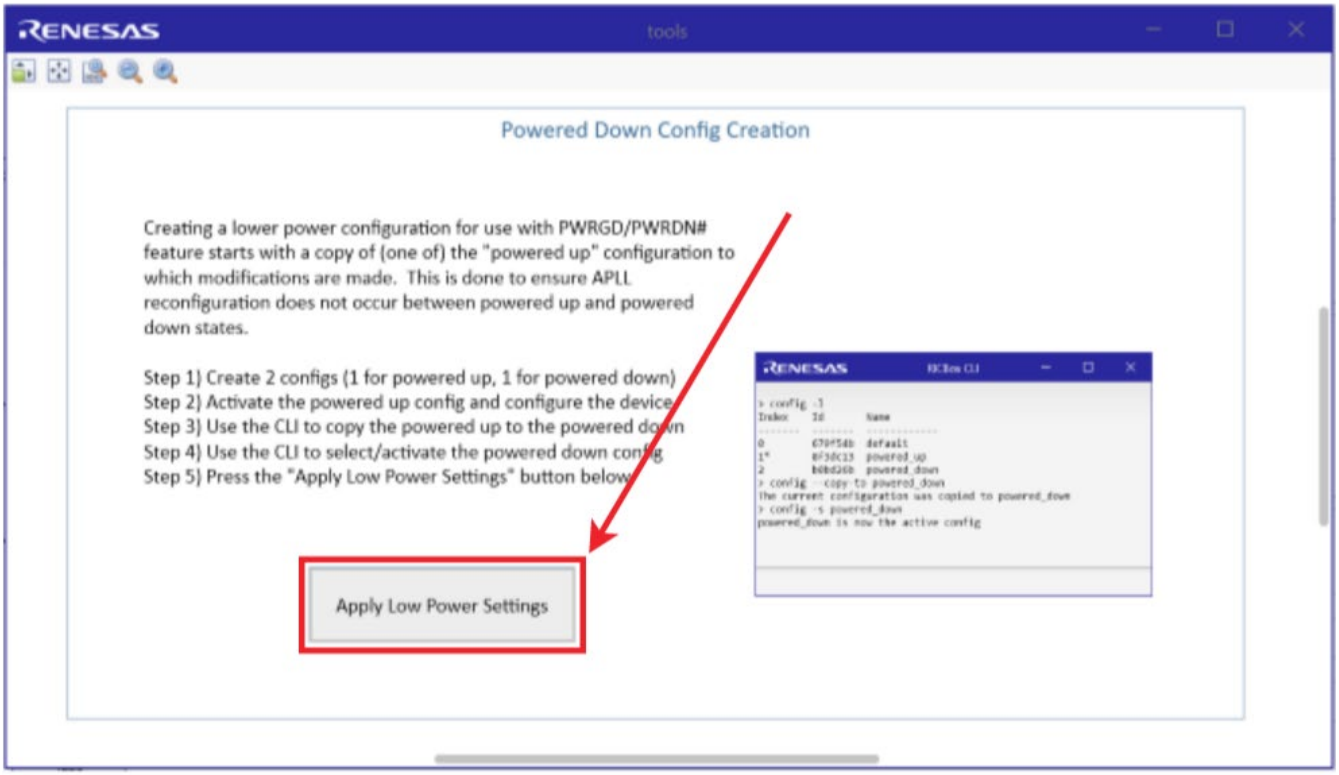
Make sure the current configuration is the low-power configuration that was just created.



6. In the Block Diagram view, click on “Tools”.

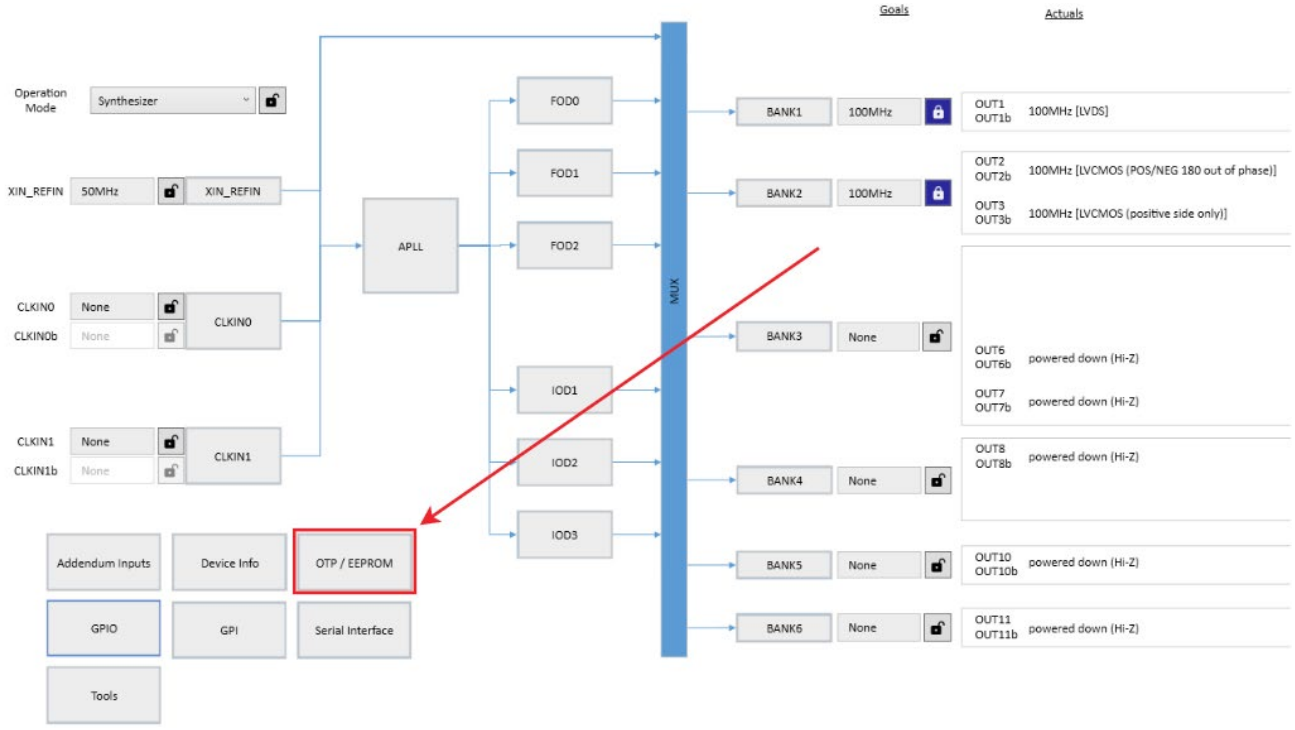


7. Click on “Apply Low Power Settings”.



4. Assigning the Power-Down Configuration to a Configuration Slot

1. In the Block Diagram view, click on the “OTP / EEPROM” button.



2. In the Config Assignment box, assign the configuration slots associated with the GPIO pin selected for the PWRGD/PWRDN# function as active low to the low-power configuration just created. The configuration slots that are active when the Power-Down GPIO pin is high are assigned to the active configurations used to create the low-power configurations.

Only one low power / power on pair of configurations are shown but it is possible to have up to nine pairs of low power / power-on configurations using the Power-Down feature.

5. Switching between the Power-Up Configuration and Power-Down Configuration

There are two methods for switching between the Power-Up configuration and the Power-Down configuration:

- Applying an appropriate logic level to the GPIO pin assigned to the PWRGD/PWRDN# function
- Writing the appropriate values to the relevant registers through I^2C

The first method uses the GPIO pin setup for the PWRGD/PWRDN# function. Setting this GPIO pin low will set the Power-Down configuration to the current configuration, and setting the GPIO pin high will set the Power-Up configuration to the current configuration.

The second method uses the I^2C interface to write to the relevant registers. The following registers determine which configuration is set as the current configuration:

- TOP.GLOBAL.DEVICE_CNFG.static_csel0
- TOP.GLOBAL.DEVICE_CNFG.static_csel1
- TOP.GLOBAL.DEVICE_CNFG.static_csel2

While the following shows which values correspond to the logic levels applied to the GPIO pins.

Register Value	GPIO Pin Logic Level
0x0	Logic Low Level
0x1	Logic Mid Level (Not used for PWRGD/PWRDN# function)
0x3	Logic High Level

Using the example discussed in this document, writing 0x0 to TOP.GLOBAL.DEVICE_CNFG.static_csel0 will set the Power-Down configuration as the current configuration while writing 0x3 to TOP.GLOBAL.DEVICE_CNFG.static_csel0 will set the Power-Up configuration as the current configuration.

6. Output State in Power-Down Configuration

The output behavior of the device is described in the following table.

output_mode	out_dis_state OUTx / OUTxn	bank_pd	output_power VDDO	output_disabled	Frequency	Output Behavior OUTx / OUTxn
LVDS	Low / Low	Power Down	x [1]	x	Disable	Low / Low
		x	Off	x	Disable	Low / Low
		Power On	On	Disabled	Disable	High / Low
		Power On	On	Enabled	156.25	
	Hi-Z / Hi-Z	Power Down	x	x	Disable	Low / Low
		x	Off	x	Disable	Hi-Z / Hi-Z
		Power On	On	Disabled	Disable	High / High
		Power On	On	Enabled	156.25	
	Low / High	Power Down	x	x	Disable	Low / Low
		x	Off	x	Disable	Hi-Z / Hi-Z
		Power On	On	Disabled	Disable	Low / High
		Power On	On	Enabled	156.25	
	High / Low	Power Down	x	x	Disable	Low / Low
		x	Off	x	Disable	Hi-Z / Hi-Z
		Power On	On	Disabled	Disable	High / Low
		Power On	On	Enabled	156.25	
HCSL	Low / Low	Power Down	x	x	Disable	Low / Low
		x	Off	x	Disable	Low / Low
		Power On	On	Disabled	Disable	Low / Low
		Power On	On	Enabled	156.25	
	Hi-Z / Hi-Z	Power Down	x	x	Disable	Low / Low
		x	Off	x	Disable	Hi-Z / Hi-Z
		Power On	On	Disabled	Disable	High / High
		Power On	On	Enabled	156.25	
	Low / High	Power Down	x	x	Disable	Low / Low
		x	Off	x	Disable	Hi-Z / Hi-Z
		Power On	On	Disabled	Disable	Low / Low
		Power On	On	Enabled	156.25	
	High / Low	Power Down	x	x	Disable	Low / Low
		x	Off	x	Disable	Hi-Z / Hi-Z
		Power On	On	Disabled	Disable	High / Low
		Power On	On	Enabled	156.25	

output_mode	out_dis_state OUTx / OUTxn	bank_pd	output_power VDDO	output_disabled	Frequency	Output Behavior OUTx / OUTxn
LVCMOS	Low / Low	Power Down	x	x	Disable	Low / Low
		x	Off	x	Disable	Low / Low
		Power On	On	Disabled	Disable	Low / Low
		Power On	On	Enabled	156.25	
	Hi-Z / Hi-Z	Power Down	x	x	Disable	Low / Low
		x	Off	x	Disable	Hi-Z / Hi-Z
		Power On	On	Disabled	Disable	Hi-Z / Hi-Z
		Power On	On	Enabled	156.25	
	Low / High	Power Down	x	x	Disable	Low / High
		x	Off	x	Disable	Low / High
		Power On	On	Disabled	Disable	Low / High
		Power On	On	Enabled	156.25	
	High / Low	Power Down	x	x	Disable	Low / Low
		x	Off	x	Disable	High / Low
		Power On	On	Disabled	Disable	High / Low
		Power On	On	Enabled	156.25	

1. x = Don't care

7. Power Consumption in Power-Down Configuration

The power consumption of the device is described in the following table.

Rail [1]	Minimum (mA)	Average (mA)	Maximum (mA)
VDDD	10.4	10.9	11.9
VDDX	0.1	0.1	0.2
VDDR	0.1	0.1	0.2
VDDA	4.8	4.8	4.9
VDDO0	0.2	0.3	0.3
VDDO1	0.1	0.3	0.3
VDDO2	0.5	0.5	0.6
VDDO3	0.8	1.1	1.5
VDDO4	0.5	0.5	0.5
VDDO5	0.3	0.4	0.5
VDDO6	0.1	0.3	0.4
Total [2]	18.7	19.3	20.0

1. 3.3V applied to power rails
2. Differences between Total value and sum of values due to rounding errors

8. Revision History

Revision	Date	Description
1.00	Apr 6, 2022	Initial release.

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