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R32C/100 Series

Configuring DMAC

1. Abstract

This document describes how to set-up DMAC in C language, and run the example program.

2. Introduction

The application described in this document applies to the following MCU:

- MCU: R32C/118 Group

This program can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the R32C/118 Group. Check the manual for any additions or modifications to functions. Careful evaluation is recommended before using this application note.

3. Notes on Configuration

3.1 Accessing DMAC Associated Registers in the CPU

In the R32C/100 Series, some DMAC associated registers are allocated to the CPU address space. By declaring “#pragma DMAC” in the R32C/100 Series C Compiler, DMAC associated registers in the CPU can be accessed.

3.2 Using #pragma DMAC

The “#pragma DMAC” declaration allocates DMAC associated registers in the CPU to specified external variables. State variables in the following order:
#pragma DMAC Variable name DMAC register name

The following must be adhered to:

- Variables to be specified must be declared before “#pragma DMAC”.
- Specifiable DMAC registers and variable types are listed in the table below.

Specifiable DMAC Registers and Variable Types (i = 0 to 3)

Symbol	Register	Variable Type
DMD0 to DMD3	DMAi Mode Register	unsigned long
DCT0 to DCT3	DMAi Terminal Count Register	
DCR0 to DCR3	DMAi Terminal Count Reload Register	
DSA0 to DSA3	DMAi Source Address Register	far pointer to an arbitrary type. However, a pointer to a function is not possible.
DSR0 to DSR3	DMAi Source Address Reload Register	
DDA0 to DDA3	DMAi Destination Address Register	
DDR0 to DDR3	DMAi Destination Address Reload Register	

- Multiple “#pragma DMAC” commands cannot be used with the same DMAC register.
- Variables used with “#pragma DMAC” cannot be specified by “&” (address operator), “( )” (function-call operator), “[ ]” (array subscript operator), or “- >” (member operator).

The following is an example of “#pragma DMAC” usage:

```
void    _far*dda0  ;
#pragma   DMAC   dda0   DDA0

void func(void)
{
      unsigned char buff[10] ;
      dda0 = buff ;
}
```

Figure 3.1 #pragma DMAC Usage

4. Setting

This section describes the DMAC settings. Refer to the hardware manual for details on each register.

4.1 Setting Overview

The figure below shows the settings in channel units. Refer to section **4.2 "Detailed Settings"** for more information.

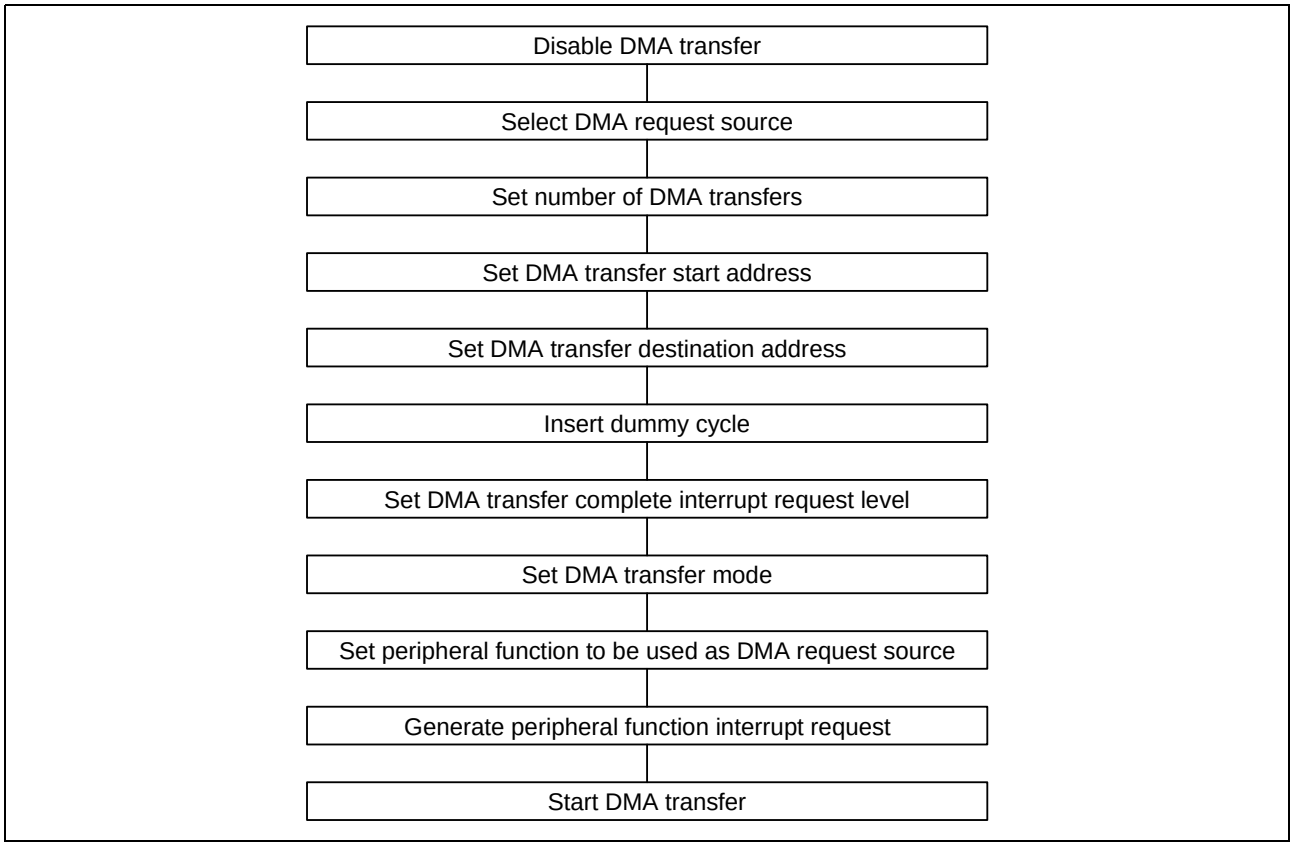
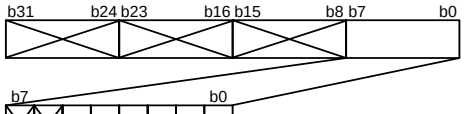
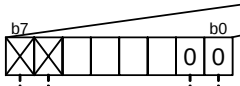


Figure 4.1 DMAC Settings

4.2 Detailed Settings

(1) Disable DMA transfer.



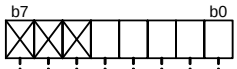


DMAi Mode Register (DMDi) (i = 0 to 3) (1)

MDi1 to MDi0	Transfer Mode Select Bit 00b: DMA transfer disabled
b7 to b6	Set to 0.
b31 to b8	Set to 0.

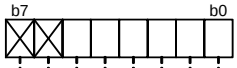
Note:
1. When setting the DMAC-associated register, set bits MDi1 to MDi0 in the corresponding channel to 00b (DMA transfer disabled). Then set the bits to 01b (single transfer) or 11b (repeat transfer).

(2) Select the DMA request source.



DMAi Request Source Select Register (DMiSL)

DSEL4 to DSEL0	DMA Request Source Select Bit Select corresponding source.
b7 to b5	Set to 0.



DMAi Request Source Select Register 2 (DMiSL2)

DSEL24 to DSEL20	DMA Request Source Select Bit Select corresponding source.
DSR	Software DMA Transfer Request Bit When a software trigger is selected, a DMA transfer request is generated by setting this bit to 1.
b7 to b6	Set to 0.

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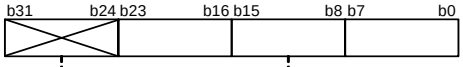
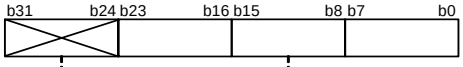
(3) Set number of DMA transfers.



DMAi Terminal Count Register (DCTi) (i = 0 to 3)

Set the transfers to be performed (1)

Set to 00h.



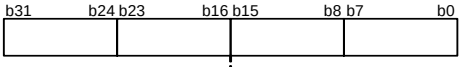
DMAi Terminal Count Reload Register (DCRi)

Set the transfers to be performed (2)

Set to 00h.

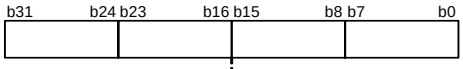
Notes:
1. After setting the DCTi register to 000000h, even if a DMA transfer request is accepted, data is not transferred.
2. This register is used for repeat transfers. It cannot be used for single transfers.

(4) Set DMA transfer source address.



DMAi Source Address Register (DSAi)

Set a source address

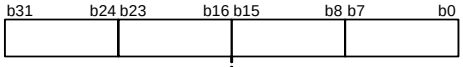


DMAi Source Address Reload Register (DSRi) (1)

Set a source address

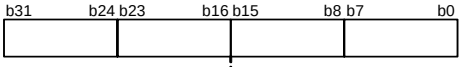
Note:
1. This register is used for the repeat transfer. It cannot be used for single transfer.

(5) Set DMA transfer destination address.



DMAi Destination Address Register (DDAi)

Set a destination address



DMAi Destination Address Reload Register (DDRi) (1)

Set a destination address

Note:
1. This register is used for the repeat transfer. It cannot be used for a single transfer.

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(6) Insert a dummy cycle.
After setting the DMiSL register (i = 0 to 3), wait six clocks of the peripheral bus clock before enabling DMA transfer.

(7) Select the DMA transfer complete interrupt request level.

Interrupt Control Register (DMiIC)

ILVL2 to ILVL0	Interrupt Request Level Select Bit 000b: Level 0 (interrupt disabled) 111b: Level 7
IR (1)	Interrupt Request Flag 0: Interrupt not requested 1: Interrupt requested
b7 to b4	Set to 0.

Note:
1. Set this bit to 0.

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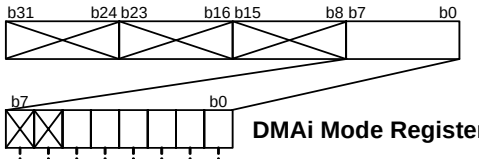
(8) Set the DMA transfer mode.



When bits UDAi, USAi, BWi1 to BWi0 are rewritten, bits should be rewritten while bits MDi1 to MDi0 are 0 (DMA transfer disabled).

DMAi Mode Register (DMDi) (i = 0 to 3)

MDi1 to MDi0 (1)	Transfer Mode Select Bit 01b: Single transfer 11b: Repeat transfer
BWi1 to BWi0 (2)	Transfer Size Select Bit 00b: 8-bit 01b: 16-bit 10b: 32-bit
USAi	Source Addressing Mode Select Bit 0: Non-incrementing addressing 1: Incrementing addressing
UDAi	Destination Addressing Mode Select Bit 0: Non-incrementing addressing 1: Incrementing addressing
b7 to b6	Set to 0.
b31 to b8	Set to 0.

Notes:
1. Do not set these bits to 10b.
2. Do not set these bits to 11b.

(9) Set the peripheral function to use as the DMA request source.

(10) Generate a peripheral function interrupt request.

(11) Start DMA transfer.
Subsequently, DMA is transferred each time a DMA transfer request is generated.

5. Sample Program

A sample program can be downloaded from the Renesas Technology website.

5.1 Explanation

The sample program uses four channels of DMAC.

Bits in the port P2 register are inverted in each DMA transfer complete interrupt handler.

The table below lists DMAC channel settings in the sample program and bits in the port P2 register that is inverted in transfer complete interrupt handler.

Table 5.1 DMAC Channel Settings

DMAC	Transfer Mode	Transfer Size	Request Source	Transfer Source Update	Transfer Destination Update	Number of Transfers	Transfer Complete Interrupt Routine
DMAC0	Repeat transfer	8-bit	Timer A0	Not updated	Not updated	14	Invert P2_0 bit
DMAC1	Repeat transfer	8-bit	Timer A0	Updated	Not updated	8	Invert P2_1 bit
DMAC2	Repeat transfer	8-bit	Timer A0	Not updated	Updated	8	Invert P2_2 bit
DMAC3	Single transfer	32-bit	Timer A0	Updated	Updated	8	Invert P2_3 bit

Table 5.2 Timer A Settings

Timer	Operation Mode	Count Source	Count Source Division Ratio
Timer A0	Timer mode	f8	65536

5.1.1 Operation of DMAC0

After a timer A0 interrupt request is generated, DMAC0 repeatedly transfers data from the transfer source's internal RAM to the transfer destination's port P0 register in 8-bit units.

The figure below shows DMAC0 operation.

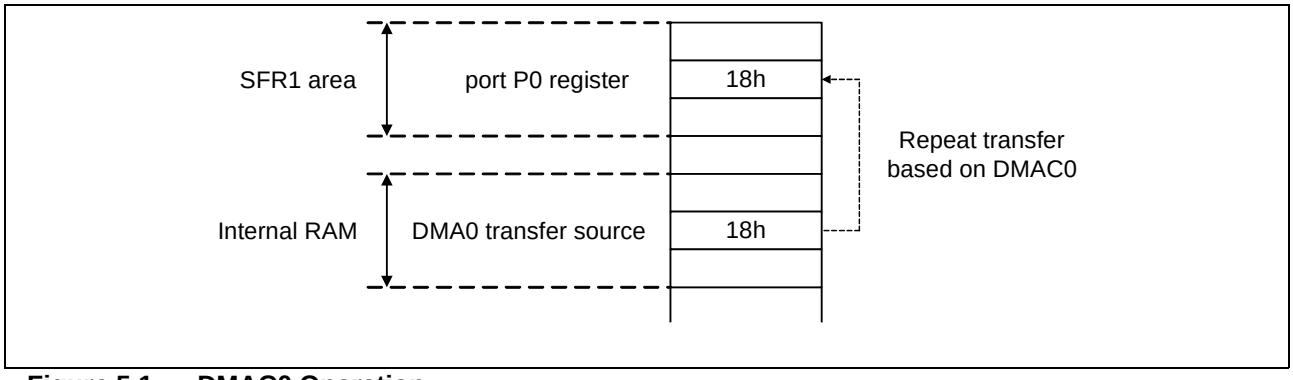


Figure 5.1 DMAC0 Operation

5.1.2 DMAC1 and DMAC2 Operation

After a timer A0 interrupt request is generated, DMAC1 and DMAC2 repeatedly transfer data from memory to memory (via the port P1 register) in 8-bit units.

When multiple DMA transfer requests are generated simultaneously during DMAC1 or DMAC2 transfer, the sample program's specification is such that the DMA transfer with a higher priority level is given priority. In this case, priority ranking is as follows: DMA0 > DMA1 > DMA2 > DMA3.

When a timer A0 interrupt request is generated, DMAC1, which has a high priority level, transfer data from the transfer source's internal RAM to the transfer destination's port P1 register. At the same time, the DMAC1 transfer source address increments.

Then, DMAC2 transfers data from the transfer source's port P1 register to the transfer destination's internal RAM. At the same time, the DMAC2 transfer source address increments.

The figure below shows DMAC1 and DMAC2 operation. Numbers in brackets ([ ]) indicate the transfer order. When the first transfer request is generated, data is transferred in order of [1] and [2]. The next transfer request continues with [3] and [4]. When the eighth transfer request transfers data [15] and [16], the DMAC1 and DMAC2 transfer source address, transfer destination address, and number of transfers are reloaded, and the next transfer request restarts with [1] and [2]. This process of data transfer repeats.

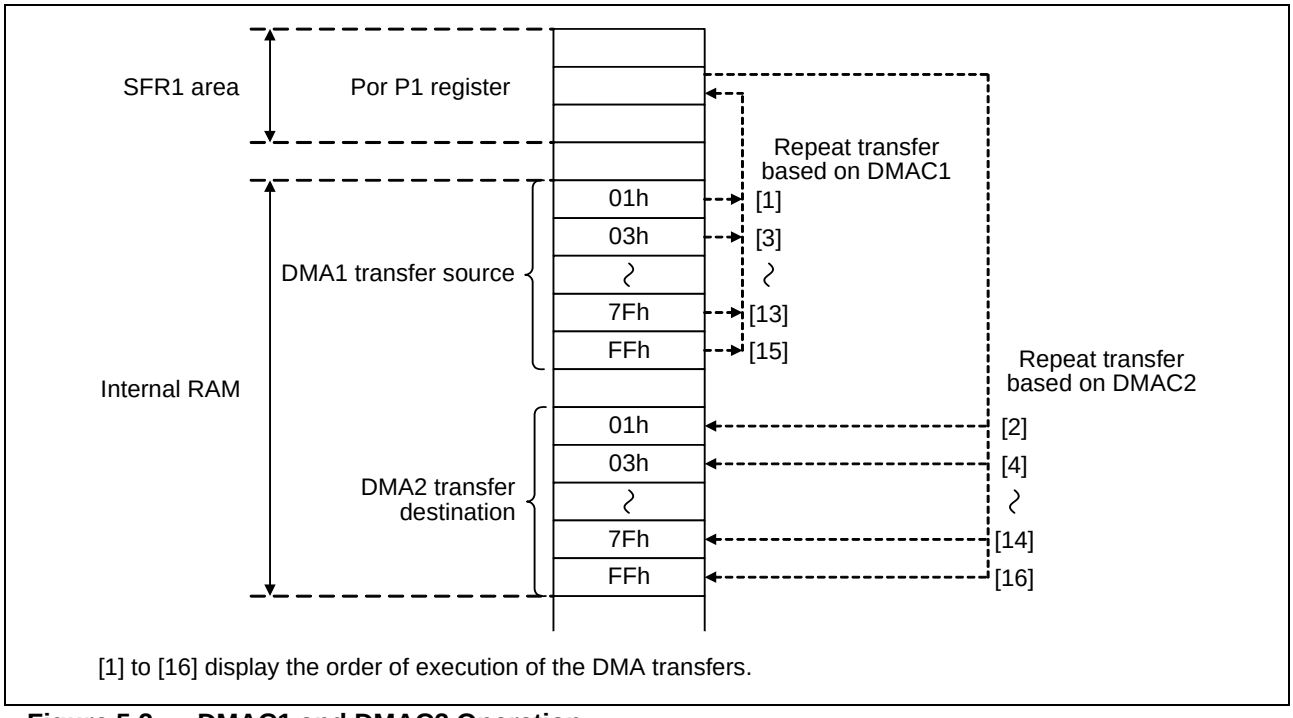
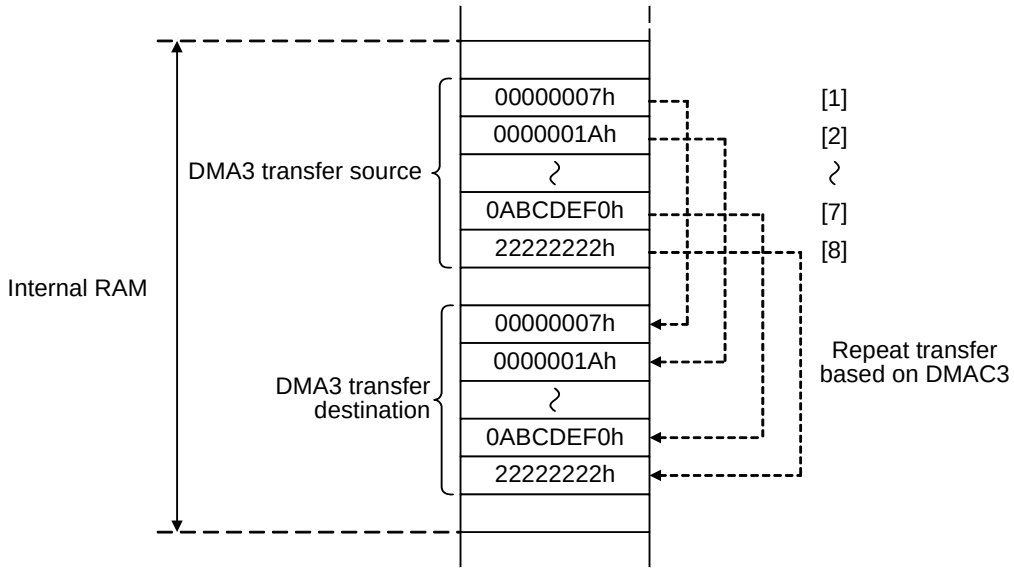


Figure 5.2 DMAC1 and DMAC2 Operation

5.1.3 DMAC3 Operation

When a timer A0 interrupt request is generated, data is transferred from the transfer source's internal RAM to the transfer destination's internal RAM in 32-bit units. Then, the DMAC3 transfer source address and transfer destination address increment.

The figure below shows DMAC3 operation. Numbers in brackets ([ ]) indicate the transfer order. When the first transfer request is generated, [1] data is transferred. When the next request is generated, [2] data is transferred. When the eighth transfer request is generated, [8] data is transfered and the transfer is completed. Even if there are additional transfer requests, no data is transferred.



[1] to [8] display the order of execution of the DMA transfers.

Figure 5.3 DMAC3 Operation

5.1.4 Sample Program Flowchart

The sample program is made up of a main function and channel transfer complete interrupt function for each DMAC.

The diagram below shows a flowchart of the main function. The subsequent four diagrams are flowcharts showing individual DMAC channel transfer complete interrupt functions. Bracketed numbers (1) through (17) correspond to the sample program flow numbers.

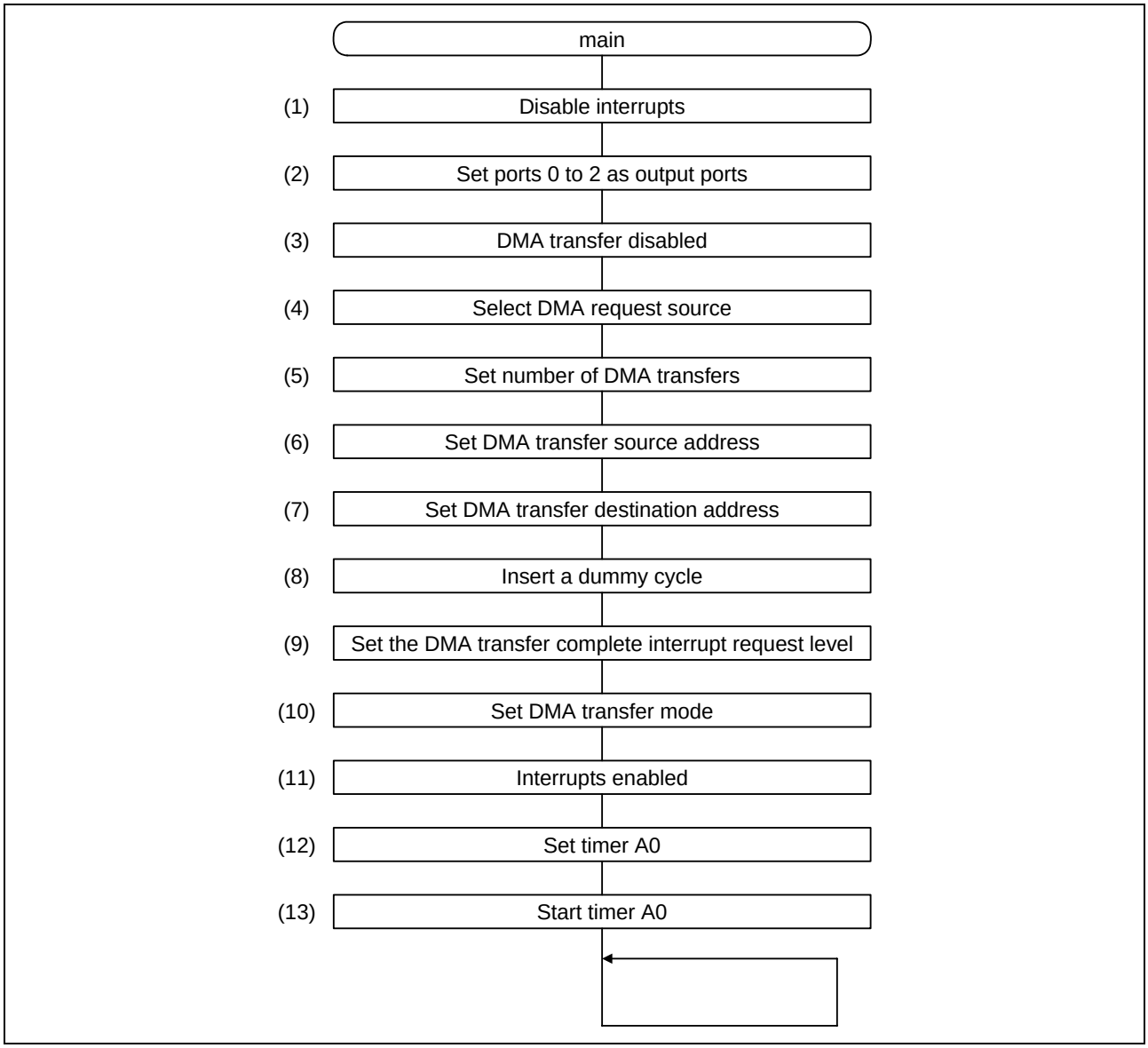


Figure 5.4 Main Function Program Flowchart

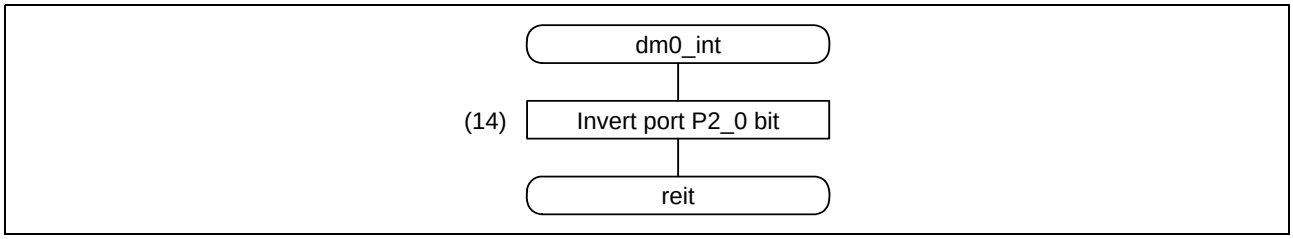


Figure 5.5 DMA0 Transfer Complete Interrupt Function Flowchart

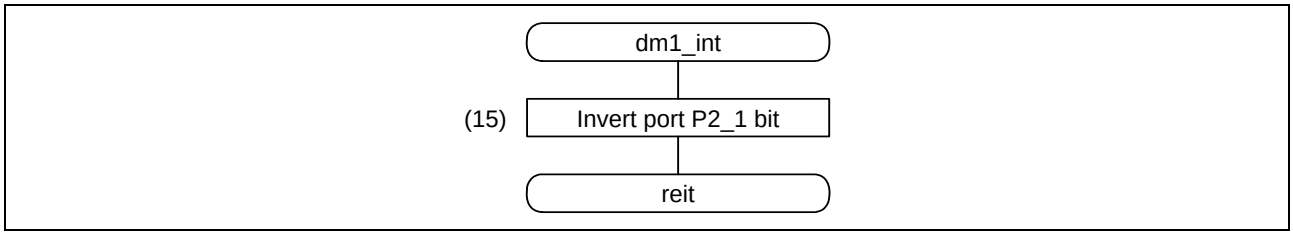


Figure 5.6 DMA1 Transfer Complete Interrupt Function Flowchart

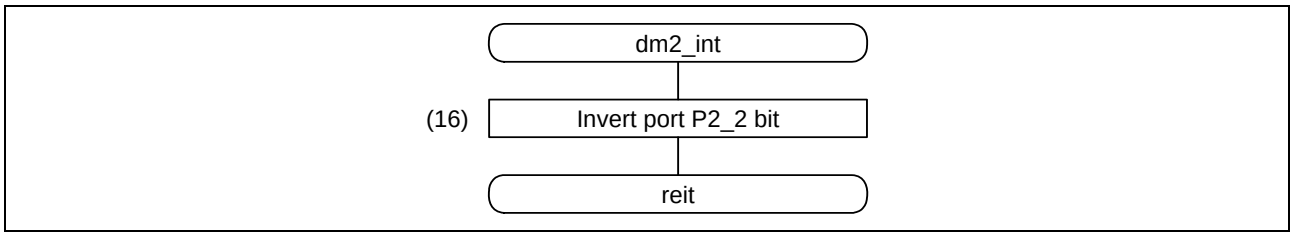


Figure 5.7 DMA2 Transfer Complete Interrupt Function Flowchart

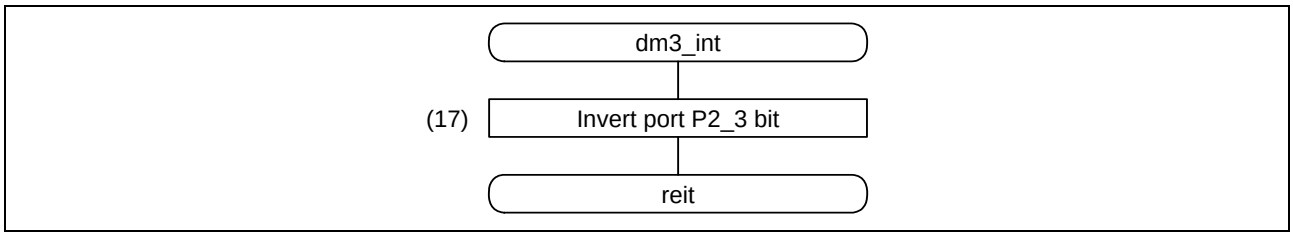


Figure 5.8 DMA3 Transfer Complete Interrupt Function Flowchart

6. Reference Documents

Hardware Manual
R32C/118 Group Hardware Manual Rev.1.00
The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Technology website.

C Compiler Manual
R32C/100 Series C Compiler Package Ver. 1.02 Compiler User's Manual Rev. 1.00
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REVISION HISTORY	Configuring DMAC

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 12, 2010	—	Initial release

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