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April 1st, 2010
Renesas Electronics Corporation

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1. **Abstract**
   This document describes how to set-up DMAC in C language, and run the example program.

2. **Introduction**
   The application described in this document applies to the following MCU:
   
   • MCU: R32C/118 Group

   This program can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the R32C/118 Group. Check the manual for any additions or modifications to functions. Careful evaluation is recommended before using this application note.
3. Notes on Configuration

3.1 Accessing DMAC Associated Registers in the CPU

In the R32C/100 Series, some DMAC associated registers are allocated to the CPU address space. By declaring “#pragma DMAC” in the R32C/100 Series C Compiler, DMAC associated registers in the CPU can be accessed.

3.2 Using #pragma DMAC

The “#pragma DMAC” declaration allocates DMAC associated registers in the CPU to specified external variables. State variables in the following order:

```c
#pragma DMAC Variable name DMAC register name
```

The following must be adhered to:

- Variables to be specified must be declared before “#pragma DMAC”.
- Specifiable DMAC registers and variable types are listed in the table below.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Register</th>
<th>Variable Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMD0 to DMD3</td>
<td>DMAi Mode Register</td>
<td>unsigned long</td>
</tr>
<tr>
<td>DCT0 to DCT3</td>
<td>DMAi Terminal Count Register</td>
<td></td>
</tr>
<tr>
<td>DCR0 to DCR3</td>
<td>DMAi Terminal Count Reload Register</td>
<td></td>
</tr>
<tr>
<td>DSA0 to DSA3</td>
<td>DMAi Source Address Register</td>
<td>far pointer to an arbitrary type.</td>
</tr>
<tr>
<td>DSR0 to DSR3</td>
<td>DMAi Source Address Reload Register</td>
<td>However, a pointer to a function is not possible.</td>
</tr>
<tr>
<td>DDA0 to DDA3</td>
<td>DMAi Destination Address Register</td>
<td></td>
</tr>
<tr>
<td>DDR0 to DDR3</td>
<td>DMAi Destination Address Reload Register</td>
<td></td>
</tr>
</tbody>
</table>

- Multiple “#pragma DMAC” commands cannot be used with the same DMAC register.
- Variables used with “#pragma DMAC” cannot be specified by “&” (address operator), “( )” (function-call operator), “[ ]” (array subscript operator), or “- >” (member operator).

The following is an example of “#pragma DMAC” usage:

```c
void _far*dda0 ;
#pragma DMAC dda0 DDA0

void func(void)
{
    unsigned char buff[10] ;
    dda0 = buff ;
}
```

Figure 3.1 #pragma DMAC Usage
4. Setting
This section describes the DMAC settings. Refer to the hardware manual for details on each register.

4.1 Setting Overview
The figure below shows the settings in channel units. Refer to section 4.2 “Detailed Settings” for more information.

![Diagram of DMAC Settings]

*Figure 4.1* DMAC Settings
4.2 Detailed Settings

(1) Disable DMA transfer.

**DMAi Mode Register (DMDi) (i = 0 to 3)**

<table>
<thead>
<tr>
<th>b31 b30 b29 b28 b27 b26 b25 b24 b23 b22 b21 b20 b19 b18 b17 b16</th>
<th>b15 b14 b13 b12 b11 b10 b9 b8</th>
</tr>
</thead>
<tbody>
<tr>
<td>MDi1 to MDi0 Transfer Mode Select Bit</td>
<td>b7 to b6 Set to 0.</td>
</tr>
<tr>
<td>b31 to b8</td>
<td>b31 to b8 Set to 0.</td>
</tr>
</tbody>
</table>

Note:
1. When setting the DMAC-associated register, set bits MDi1 to MDi0 in the corresponding channel to 00b (DMA transfer disabled). Then set the bits to 01b (single transfer) or 11b (repeat transfer).

(2) Select the DMA request source.

**DMA Request Source Select Register (DMiSL)**

<table>
<thead>
<tr>
<th>b7 b6 b5 b4 b3 b2 b1 b0</th>
<th>DSEL4 to DSEL0 DMA Request Source Select Bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>b7 to b5</td>
<td>Set to 0.</td>
</tr>
</tbody>
</table>

**DMA Request Source Select Register 2 (DMiSL2)**

<table>
<thead>
<tr>
<th>b7 b6 b5 b4 b3 b2 b1 b0</th>
<th>DSEL24 to DSEL20 DMA Request Source Select Bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>b7 to b6</td>
<td>Software DMA Transfer Request Bit</td>
</tr>
<tr>
<td></td>
<td>When a software trigger is selected, a DMA transfer request is generated by setting this bit to 1.</td>
</tr>
<tr>
<td></td>
<td>Set to 0.</td>
</tr>
</tbody>
</table>

Continued on next page
### Configuring DMAC

#### (3) Set number of DMA transfers.

<table>
<thead>
<tr>
<th>b31 b24 b23 b16 b15 b8 b7 b0</th>
</tr>
</thead>
</table>

**DMAi Terminal Count Register (DCTi) (i = 0 to 3)**

- Set the transfers to be performed
- Set to 00h.

<table>
<thead>
<tr>
<th>b31 b24 b23 b16 b15 b8 b7 b0</th>
</tr>
</thead>
</table>

**DMAi Terminal Count Reload Register (DCRi)**

- Set the transfers to be performed
- Set to 00h.

**Notes:**
1. After setting the DCTi register to 000000h, even if a DMA transfer request is accepted, data is not transferred.
2. This register is used for repeat transfers. It cannot be used for single transfers.

#### (4) Set DMA transfer source address.

<table>
<thead>
<tr>
<th>b31 b24 b23 b16 b15 b8 b7 b0</th>
</tr>
</thead>
</table>

**DMAi Source Address Register (DSAi)**

- Set a source address

<table>
<thead>
<tr>
<th>b31 b24 b23 b16 b15 b8 b7 b0</th>
</tr>
</thead>
</table>

**DMAi Source Address Reload Register (DSRi)**

- Set a source address

**Note:**
1. This register is used for the repeat transfer. It cannot be used for single transfer.

#### (5) Set DMA transfer destination address.

<table>
<thead>
<tr>
<th>b31 b24 b23 b16 b15 b8 b7 b0</th>
</tr>
</thead>
</table>

**DMAi Destination Address Register (DDAi)**

- Set a destination address

<table>
<thead>
<tr>
<th>b31 b24 b23 b16 b15 b8 b7 b0</th>
</tr>
</thead>
</table>

**DMAi Destination Address Reload Register (DDRi)**

- Set a destination address

**Note:**
1. This register is used for the repeat transfer. It cannot be used for a single transfer.
(6) Insert a dummy cycle. After setting the DMiSL register (i = 0 to 3), wait six clocks of the peripheral bus clock before enabling DMA transfer.

(7) Select the DMA transfer complete interrupt request level.

Note:
1. Set this bit to 0.
(8) Set the DMA transfer mode.

When bits UDAi, USAi, BWi1 to BWi0 are rewritten, bits should be rewritten while bits MDi1 to MDi0 are 0 (DMA transfer disabled).

(9) Set the peripheral function to use as the DMA request source.

(10) Generate a peripheral function interrupt request.

(11) Start DMA transfer.

Subsequently, DMA is transferred each time a DMA transfer request is generated.
5. Sample Program
   A sample program can be downloaded from the Renesas Technology website.

5.1 Explanation
   The sample program uses four channels of DMAC.

   Bits in the port P2 register are inverted in each DMA transfer complete interrupt handler.

   The table below lists DMAC channel settings in the sample program and bits in the port P2 register that is inverted in transfer complete interrupt handler.

### Table 5.1 DMAC Channel Settings

<table>
<thead>
<tr>
<th>DMAC</th>
<th>Transfer Mode</th>
<th>Transfer Size</th>
<th>Request Source</th>
<th>Transfer Source Update</th>
<th>Transfer Destination Update</th>
<th>Number of Transfers</th>
<th>Transfer Complete Interrupt Routine</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMAC0</td>
<td>Repeat transfer</td>
<td>8-bit</td>
<td>Timer A0</td>
<td>Not updated</td>
<td>Not updated</td>
<td>14</td>
<td>invert P2_0 bit</td>
</tr>
<tr>
<td>DMAC1</td>
<td>Repeat transfer</td>
<td>8-bit</td>
<td>Timer A0</td>
<td>Updated</td>
<td>Not updated</td>
<td>8</td>
<td>invert P2_1 bit</td>
</tr>
<tr>
<td>DMAC2</td>
<td>Repeat transfer</td>
<td>8-bit</td>
<td>Timer A0</td>
<td>Not updated</td>
<td>Updated</td>
<td>8</td>
<td>invert P2_2 bit</td>
</tr>
<tr>
<td>DMAC3</td>
<td>Single transfer</td>
<td>32-bit</td>
<td>Timer A0</td>
<td>Updated</td>
<td>Updated</td>
<td>8</td>
<td>invert P2_3 bit</td>
</tr>
</tbody>
</table>

### Table 5.2 Timer A Settings

<table>
<thead>
<tr>
<th>Timer</th>
<th>Operation Mode</th>
<th>Count Source</th>
<th>Count Source Division Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer A0</td>
<td>Timer mode</td>
<td>f8</td>
<td>65536</td>
</tr>
</tbody>
</table>

5.1.1 Operation of DMAC0

After a timer A0 interrupt request is generated, DMAC0 repeatedly transfers data from the transfer source’s internal RAM to the transfer destination’s port P0 register in 8-bit units.

The figure below shows DMAC0 operation.
5.1.2 DMAC1 and DMAC2 Operation

After a timer A0 interrupt request is generated, DMAC1 and DMAC2 repeatedly transfer data from memory to memory (via the port P1 register) in 8-bit units.

When multiple DMA transfer requests are generated simultaneously during DMAC1 or DMAC2 transfer, the sample program’s specification is such that the DMA transfer with a higher priority level is given priority. In this case, priority ranking is as follows: DMA0 > DMA1 > DMA2 > DMA3.

When a timer A0 interrupt request is generated, DMAC1, which has a high priority level, transfers data from the transfer source’s internal RAM to the transfer destination’s port P1 register. At the same time, the DMAC1 transfer source address increments.

Then, DMAC2 transfers data from the transfer source’s port P1 register to the transfer destination’s internal RAM. At the same time, the DMAC2 transfer source address increments.

The figure below shows DMAC1 and DMAC2 operation. Numbers in brackets ([ ]) indicate the transfer order. When the first transfer request is generated, data is transferred in order of [1] and [2]. The next transfer request continues with [3] and [4]. When the eighth transfer request transfers data [15] and [16], the DMAC1 and DMAC2 transfer source address, transfer destination address, and number of transfers are reloaded, and the next transfer request restarts with [1] and [2]. This process of data transfer repeats.

![Figure 5.2 DMAC1 and DMAC2 Operation](image)

[1] to [16] display the order of execution of the DMA transfers.
### 5.1.3 DMAC3 Operation

When a timer A0 interrupt request is generated, data is transferred from the transfer source’s internal RAM to the transfer destination’s internal RAM in 32-bit units. Then, the DMAC3 transfer source address and transfer destination address increment.

The figure below shows DMAC3 operation. Numbers in brackets ([ ] ) indicate the transfer order. When the first transfer request is generated, [1] data is transferred. When the next request is generated, [2] data is transferred. When the eighth transfer request is generated, [8] data is transferred and the transfer is completed. Even if there are additional transfer requests, no data is transferred.

![DMAC3 Operation Diagram](image)

Figure 5.3 DMAC3 Operation
5.1.4 Sample Program Flowchart

The sample program is made up of a main function and channel transfer complete interrupt function for each DMAC.

The diagram below shows a flowchart of the main function. The subsequent four diagrams are flowcharts showing individual DMAC channel transfer complete interrupt functions. Bracketed numbers (1) through (17) correspond to the sample program flow numbers.

![Main Function Program Flowchart](image-url)
Invert port P2_0 bit
(14) dm0_int

Invert port P2_1 bit
(15) dm1_int

Invert port P2_2 bit
(16) dm2_int

Invert port P2_3 bit
(17) dm3_int

Figure 5.5 DMA0 Transfer Complete Interrupt Function Flowchart

Figure 5.6 DMA1 Transfer Complete Interrupt Function Flowchart

Figure 5.7 DMA2 Transfer Complete Interrupt Function Flowchart

Figure 5.8 DMA3 Transfer Complete Interrupt Function Flowchart
6. Reference Documents

Hardware Manual
R32C/118 Group Hardware Manual Rev. 1.00
The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Technology website.

C Compiler Manual
R32C/100 Series C Compiler Package Ver. 1.02 Compiler User’s Manual Rev. 1.00
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<table>
<thead>
<tr>
<th>REV.</th>
<th>DATE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>Mar. 12, 2010</td>
<td>Initial release</td>
</tr>
</tbody>
</table>

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