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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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SH7206 Group

CMT: Example of Using Compare Match Interrupts

Introduction

This note describes a simple application of the compare match timer function of the SH7206.

Target Device

SH7206

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1. Overview

1.1 Specifications

- A compare match timer (CMT 0) is used as a 1-second timer.
- With the aid of compare match interrupts (CMI0), the output of port E1 is inverted every second.
- Register values are saved to and restored from the register bank.

1.2 Module Used

Compare match timer (CMT 0)

1.3 Applicable Conditions

- MCU: SH7206 (R5S72060)
- Operating frequency: Internal clock at 200 MHz
Bus clock at 66.67 MHz
Peripheral clock at 33.33 MHz
- C compiler: Manufactured by Renesas Technology Corp.
Version 9.00 C/C++ compiler package for the SuperH RISC engine Family
- Compile option: Default settings of the High-performance Embedded Workshop (-cpu=sh2a -debug -gbr=auto -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1)

1.4 Related Application Note

Operation of the sample program in this application note has been confirmed with the setting conditions given in the application note on *Example of SH7206 Initial Configuration*. Please refer to that document when setting up this sample task.

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2. Description of Application Example

In this sample task, the compare match timer (CMT 0) is used to count a constant number of cycles.

2.1 Functions Used: Overview of Operation

A compare match timer can be made to count a constant number of cycles by setting the value for comparison in the compare match constant register (CMCOR) and then operating the compare match counter (CMCNT). When the two values match, CMCNT is cleared to 0, and the compare match flag (CMF) in the compare match timer control/status register (CMCSR) is set to 1. Then, if the compare match interrupt enable bit (CMIE) of CMCSR register is set to 1, a compare match interrupt (CMI) is generated. Also, counting up by CMCNT restarts from 0.

Table 1 gives an overview of the CMT, and figure 1 shows the scheme of CMT_0.

Table 1 Overview of compare match timers

Item	Overview
Number of available units	2
Counter	16-bit counter (counting up only)
Pin function	None
Clock sources	P ϕ /8, P ϕ /32, P ϕ /128, P ϕ /512 P ϕ : internal peripheral clock
Start-up method	Software control
State where compare match occurs	The final state, i.e. that where the values in the compare match counter (CMCNT) and compare match constant register (CMCOR) match (at this time the value in CMCNT is updated to H'0000)
Interrupt request	Compare match interrupt (CMI)

Note: Please refer to the section on the compare match timers in the *SH7206 Group Hardware Manual* for more detailed information.

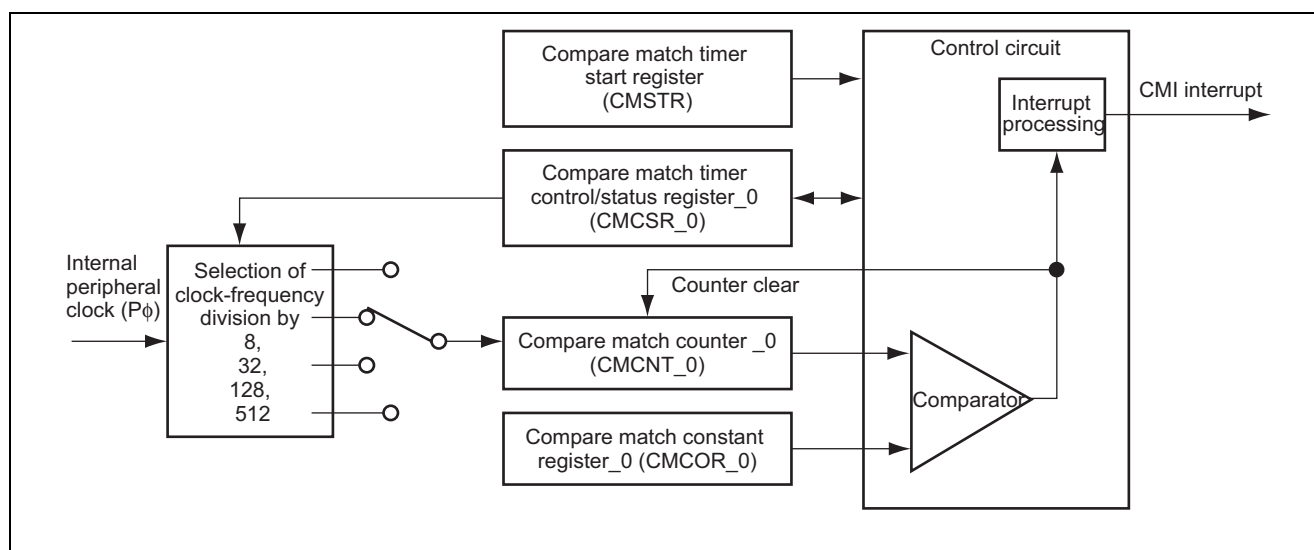


Figure 1 CMT_0 Scheme

CMT: Example of Using Compare Match Interrupt

2.2 Procedure for Setting up the Functions

The procedure used to set up the compare match timer (CMT_0) for cyclic-counting operation is described below.

The flowchart in figure 2 gives an example of the procedure used to set the number of cycles for counting by the compare match timer. Refer to the SH7206 Group Hardware Manual for detailed information on the setting of individual registers.

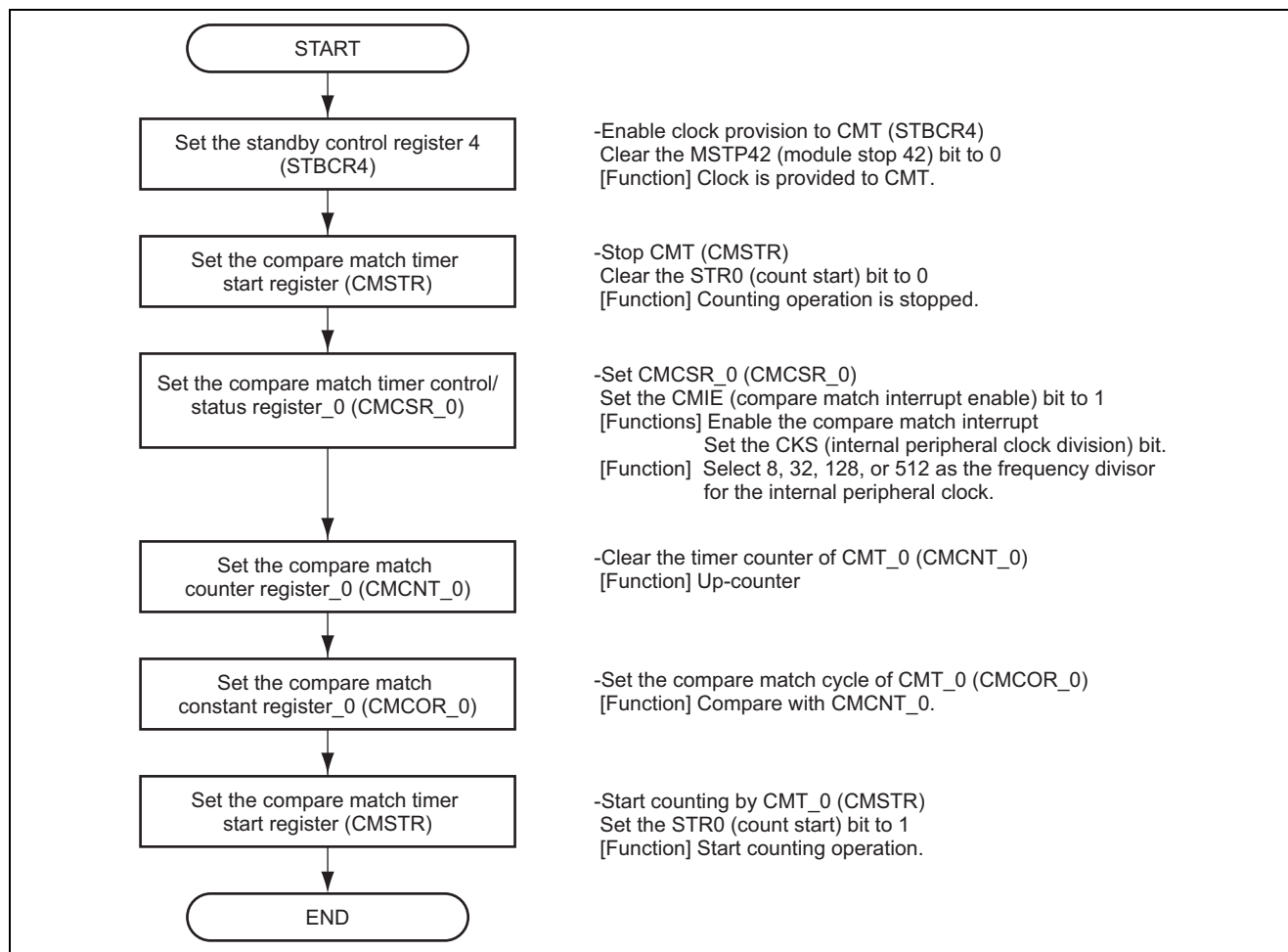


Figure 2 Example Flow for Setting up a Compare Match Timer for Cycle Counting

CMT: Example of Using Compare Match Interrupt

2.3 Operation of the Sample Program

In the sample program, the compare match timer (CMT) is used as a timer that counts a constant number of cycles. The timer generates compare match interrupts (CMIs) at every second, and these drive inversion of the output of port E pin 1 at every second.

Figure 3 shows the timing of operation of the sample program.

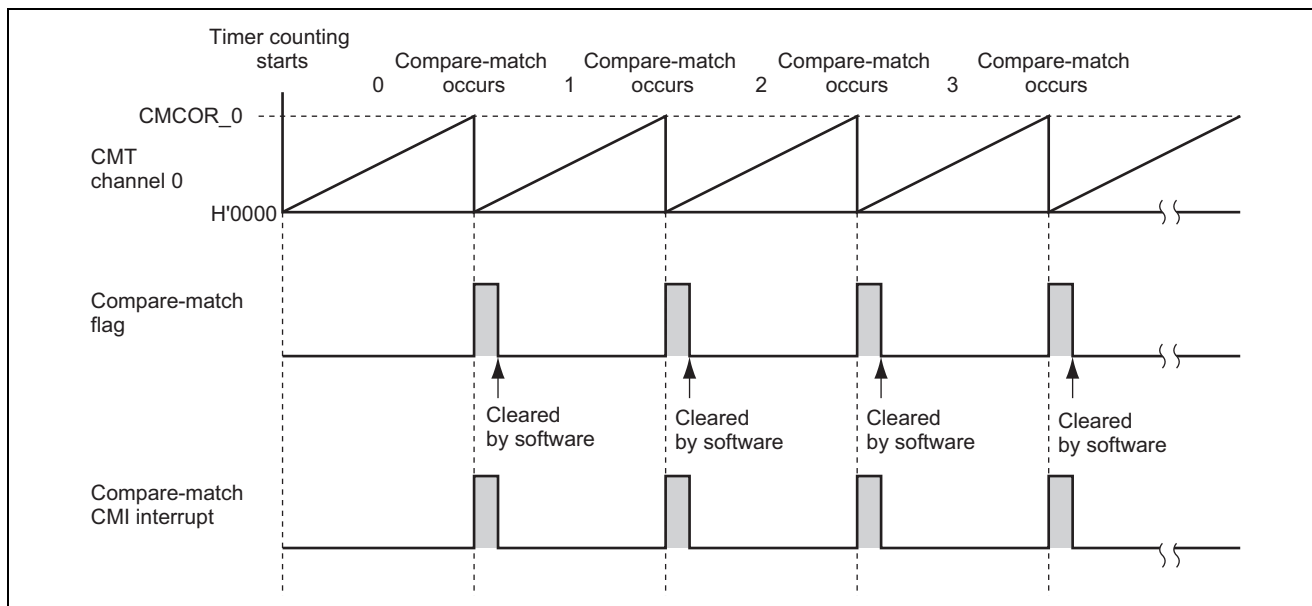


Figure 3 Timing of Operation of the Sample Program

2.4 Procedure for Processing by the Sample Program

Table 2 describes how to set the compare match timer. Also, figures 4 and 5 show the flow of processing by the sample program.

Table 2 Compare match Timer Settings

Name of Register	Address	Setting Value	Function
Standby control register 4 (STBCR4)	H'FFFE 040C	H'F0	MSTP42 = 0: CMT operates.
Compare match timer start register (CMSTR)	H'FFFE C000	H'0000	STR0 = 0: Counting is stopped.
		H'0001	STR0 = 1: Counting is started.
Compare match timer control/status register_0 (CMCSR_0)	H'FFFE C002	H'0043	-CMIE = 1: Compare match interrupt is enabled. -CSK1 = B'11: P ϕ /152
Compare match counter_0 (CMCNT_0)	H'FFFE C004	H'0000	Timer counter is cleared (H'0000).
Compare match constant register_0 (CMCOR_0)	H'FFFE C006	H'FFE5	65509 (H'FFE5): About 1 second.

CMT: Example of Using Compare Match Interrupt

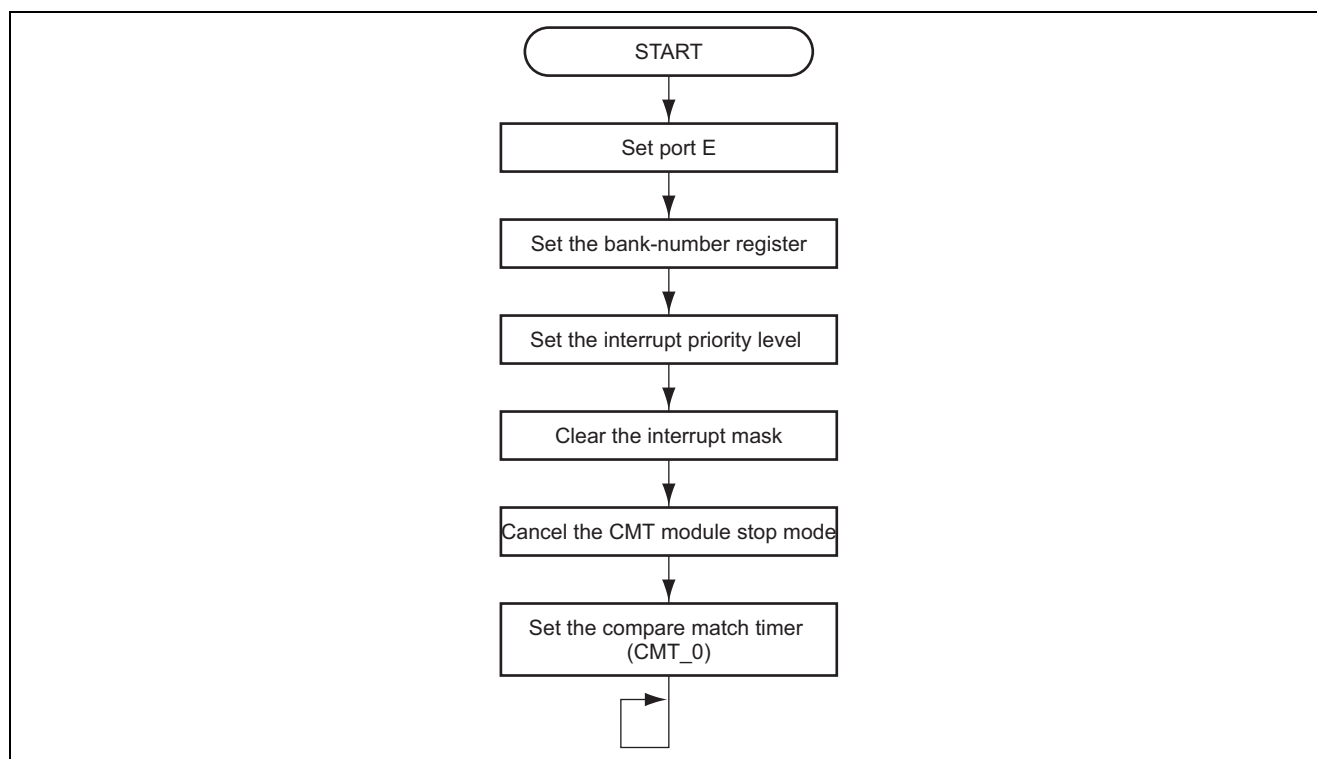


Figure 4 Flow of Processing by the Sample Program (Constant Cycle Timer: Example of Using CMI)

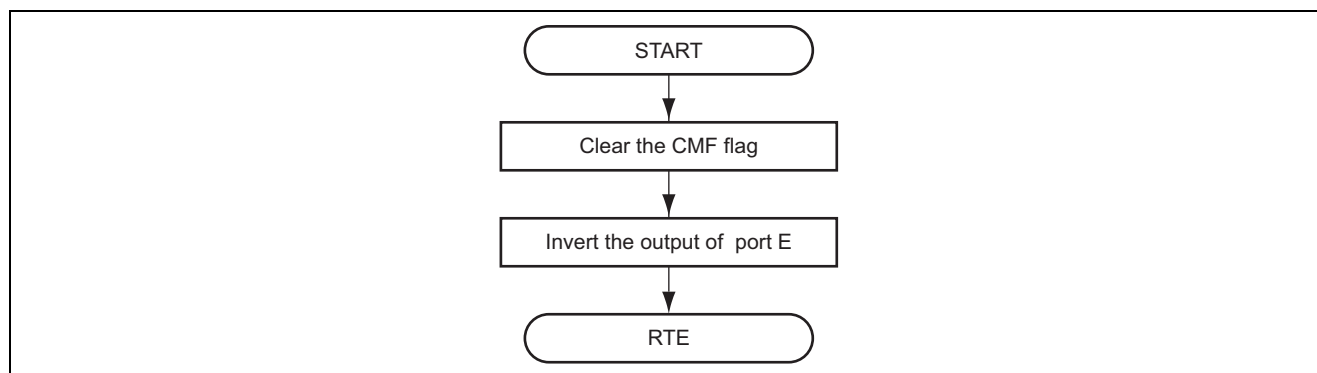


Figure 5 Example Flow of CMI Interrupt Processing

3. Sample Program

- Sample Program: Listing of "main.c" (1)

```

1  /*"FILE COMMENT"******/
2  *
3  *   System Name : SH7206 Sample Program
4  *   File Name   : main.c
5  *   Contents    : Sample program: constant cycle counting (CMT: CM interrupt)
6  *   Version     : 1.00
7  *   Model       : M3A-HS60
8  *   CPU         : SH7206
9  *   Compiler    : SHC9.0.00
10 *
11 *   Note        : Demonstrates use of CMT0 to count for a constant cycle
12 *                (1 second). Output of port E1 is inverted each time the
13 *                1-second-elapsed flag (compare match flag) is set.
14 *
15 *                <Caution>
16 *                This entire sample program is for reference only and its
17 *                operation is not guaranteed. Please use this sample as a
18 *                technical reference in software development.
19 *
20 *   Copyright (C) 2004 Renesas Technology Corp. All Rights Reserved
21 *   and Renesas Solutions Corp. All Rights Reserved
22 *
23 *   History      :2004.10.26 ver.1.00
24 *"FILE COMMENT END"******/
25 #include <machine.h>
26 #include "iodefine.h"
27
28
29 /* ==== Prototype declaration ==== */
30 void main(void);
31
32 /*"FUNC COMMENT"******/
33 * ID           :
34 * Overview of module : Sample program main (counting set no. of cycles)
35 * -----
36 * Include       : #include "iodefine.h"
37 * -----
38 * Declaration   : void main(void)
39 * -----
40 * Function      : Port E, interrupt mask and priority rank, and compare-
41 *                : match timer (CMT0) are set (1 second). Counting is then
42 *                : started.
43 * -----
44 * Argument      : None
45 * -----
46 * Return value  : None
47 * -----
48 * Caution      :

```

CMT: Example of Using Compare Match Interrupt

- Sample Program: Listing of “main.c” (2)

```

49  *"FUNC COMMENT END"*****/
50  void main(void)
51  {
52
53  /* ==== Setting port E ==== */
54  PORT.PECRL1.BIT.PE1MD=0x0; /* Set port E pin 1 for IO port operation */
55  PORT.PEIORL.BIT.PE1IOR=0x1; /* Set PE1 as an output. */
56  PORT.PEDRL.BIT.PE1DR=0x1; /* Output value of pin E1 is 1. */
57
58  /* ==== Setting of bank number register ==== */
59  INTC.IBNR.BIT.BE=0x01; /* Register bank is used for all interrupts*/
60
61  /* ==== Setting of interrupt priority rank ==== */
62  INTC.IPR08.BIT._CMT0=0x1; /* CM interrupt priority rank is set to 1.*/
63
64  /* ====Canceling interrupt mask ==== */
65  set_imask(0); /* Interrupt mask is cleared. */
66
67  /* ==== Canceling stoppage of CMT module ==== */
68  /* ---- Setting standby control register 4 (STBCR4) ---- */
69  CPG.STBCR4.BYTE=0xF0; /* Stoppage of CMT module is cancelled. */
70
71  /* ==== Setting compare match timer (CMT0) ==== */
72  /* ----Compare match timer start register (CMSTR) ---- */
73  CMT.CMSTR.BIT.STR=0x0; /* Counting is stopped. */
74  /* ----Compare match timer control/status register (CMCSR_0) ---- */
75  CMT.CMCSR0.WORD=0x0043; /* Compare match interrupt is enabled, and clock
76                          selection is made. */
77  /* ---- Compare match counter register (CMCNT_0) ---- */
78  CMT.CMCNT0.WORD=0x0000; /* Clear the timer counter */
79  /* ----Setting compare match constant register (CMCOR_0) ---- */
80  CMT.CMCOR0.WORD=0xFFE5; /* Cycles before compare match is set (1 second) */
81  /* ----Setting compare match timer start register (CMSTR) ---- */
82  CMT.CMSTR.BIT.STR=0x1; /* Counting is started. */
83
84  while(1){
85  /* Program end */
86  }
87  }
88
/* End of file */

```

CMT: Example of Using Compare Match Interrupt

- Sample Program: Listing of "intprg.c" (1)

```

1  /*"FILE COMMENT"******/
2  *
3  *      System Name : SH7206 Sample Program
4  *      File Name   : intprg.c
5  *      Version     : 1.00.00
6  *      Contents    : Interrupt processing function definition
7  *      Model       : M3A-HS60
8  *      CPU         : SH7206
9  *      Compiler    : SHC9.0.00
10 *      OS          : None
11 *
12 *      Note        : The current file is to be exchanged for a file
13 *                   generated by Ver.3.1 of Renesas Project Generator,
14 *                   our current standard for application notes.
15 *      <Caution>
16 *      This entire sample program is for reference only and
17 *      its operation is not guaranteed.
18 *      Please use this sample as a technical reference in
19 *      software development.
20 *
21 *
22 *      This file is generated by Renesas Project Generator (Ver.3.1).
23 *
24 *      Copyright (C) 2004 Renesas Technology Corp. All Rights Reserved
25 *      AND Renesas Solutions Corp. All Rights Reserved
26 *
27 *      History     : 2004.10.14 ver.1.00.00
28 *"FILE COMMENT END"******/
29 #include <machine.h>
30 #include "vect.h"
31 #include "iodefine.h"
32 #pragma section IntPRG

```

Lines 33 to 305 are omitted.

4. Documents for Reference

- Software manual
SH-2A SH2A-FPU Software Manual Rev.3.00
If you don't already have it, please download the latest version from the homepage of Renesas Technology Corp.
- Hardware manual
SH7206 Group Hardware Manual Rev.1.00
If you don't already have it, please download the latest version from the homepage of Renesas Technology Corp.

5. Website and Support Window

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CMT: Example of Using Compare Match Interrupt

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Sep.05.05	—	First edition issued

CMT: Example of Using Compare Match Interrupt

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