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SH7206 Group

CMT: Example of Setting

Introduction

This application note describes compare match timer function for the SH7206.

Target Device

SH7206

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1. Overview

1.1 Specifications

- Compare match timer (CMT channel 0) is set to 1-ms timer.
- Using software, compare match flag of CMT_0 is polled and counted 1000 times.
- Output of port E is inverted at every count of 1000 times.

1.2 Function Used

Compare match timer (CMT channel 0)

1.3 Applied Conditions

- MCU: SH7206 (R5S72060)
- Operating frequency: Internal clock of 200 MHz
Bus clock of 66.67 MHz
Peripheral clock of 33.33 MHz
- C compiler: Manufactured by Renesas Technology Corp.
C/C++ compiler package Version 9.00 of the SuperH RISC engine Family
- Compile option: Default setting of High-performance Embedded Workshop (-cpu=sh2a -debug -gbr=auto -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1)

1.4 Related Application Note

Sample program in this application note is confirmed in the setting conditions of *Example of SH7206 Initial Configuration*. Please refer to the conditions, as well.

2. Description of Application Examples

In this sample task, compare match timer (CMT channel 0) is used to count constant cycles.

2.1 Operation Overview of Function Used

Compare match timer is a timer that counts constant cycles by operating CMT counter. When the value of compare match counter (CMCNT) matches the value of compare match constant register (CMCOR), CMCNT is cleared as 0, and the compare match flag (CMF) of compare match timer control/status register (CMCSR) is set to 1. Then, when the compare match interrupt enable bit (CMIE) of CMCSR register is set to 1, compare match interrupt (CMI) occurs. Also, CMCNT restarts counting up from 0.

Table 1 describes the overview of CMT, and figure 1 shows the scheme of CMT_0.

Table 1 Overview of CMT

Item	Overview
Number of usable channels	2 channels
Counter	16-bit counter (up counter only)
Pin function	None
Clock source	P ϕ /8, P ϕ /32, P ϕ /128, P ϕ /512 P ϕ : internal peripheral clock
Start-up method	Starting up by software
State of compare match occurrence	Occurs in the final state where compare match counter (CMCNT) matches compare match constant register (CMCOR) (in the timing when the value of CMCNT is updated to H'0000).
Interrupt request	Compare match interrupt (CMI)

Note: Please refer to the section of compare match timer in the SH7206 Group Hardware Manual for detailed information.

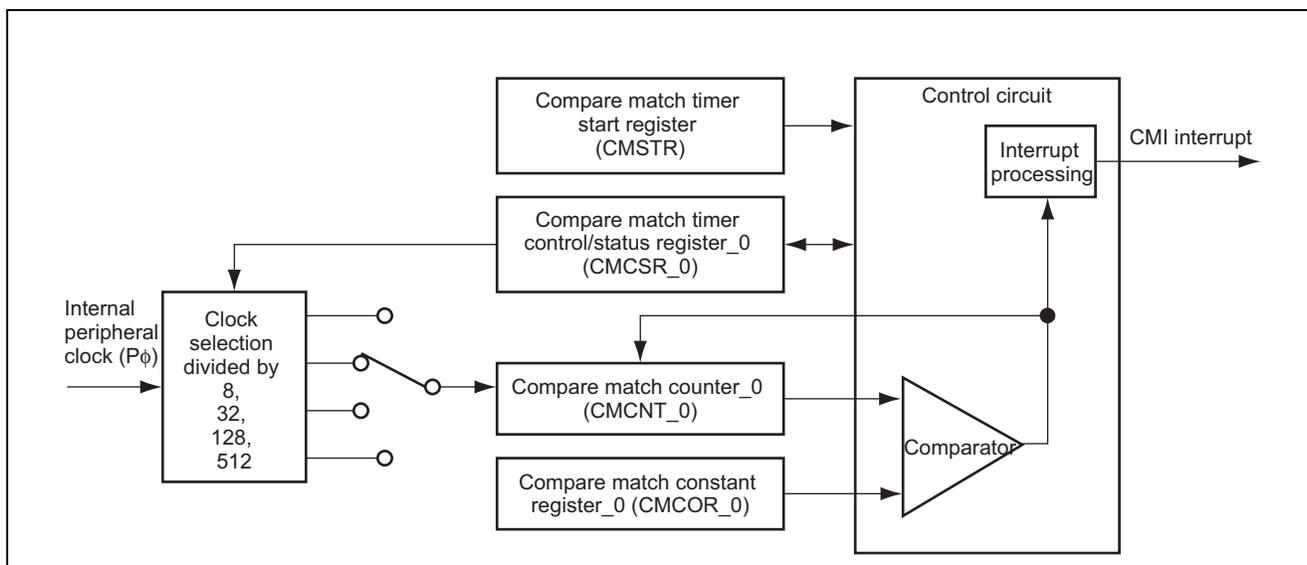


Figure 1 CMT_0 Scheme

2.2 Setting Procedure of Functions Used

Setting procedure of cycle count operation for compare match timer (CMT_0) is described as follows.

Figure 2 shows an example of flowchart to set the cycle count of compare match timer. Refer to the SH7206 Group Hardware Manual for detailed information on each register.

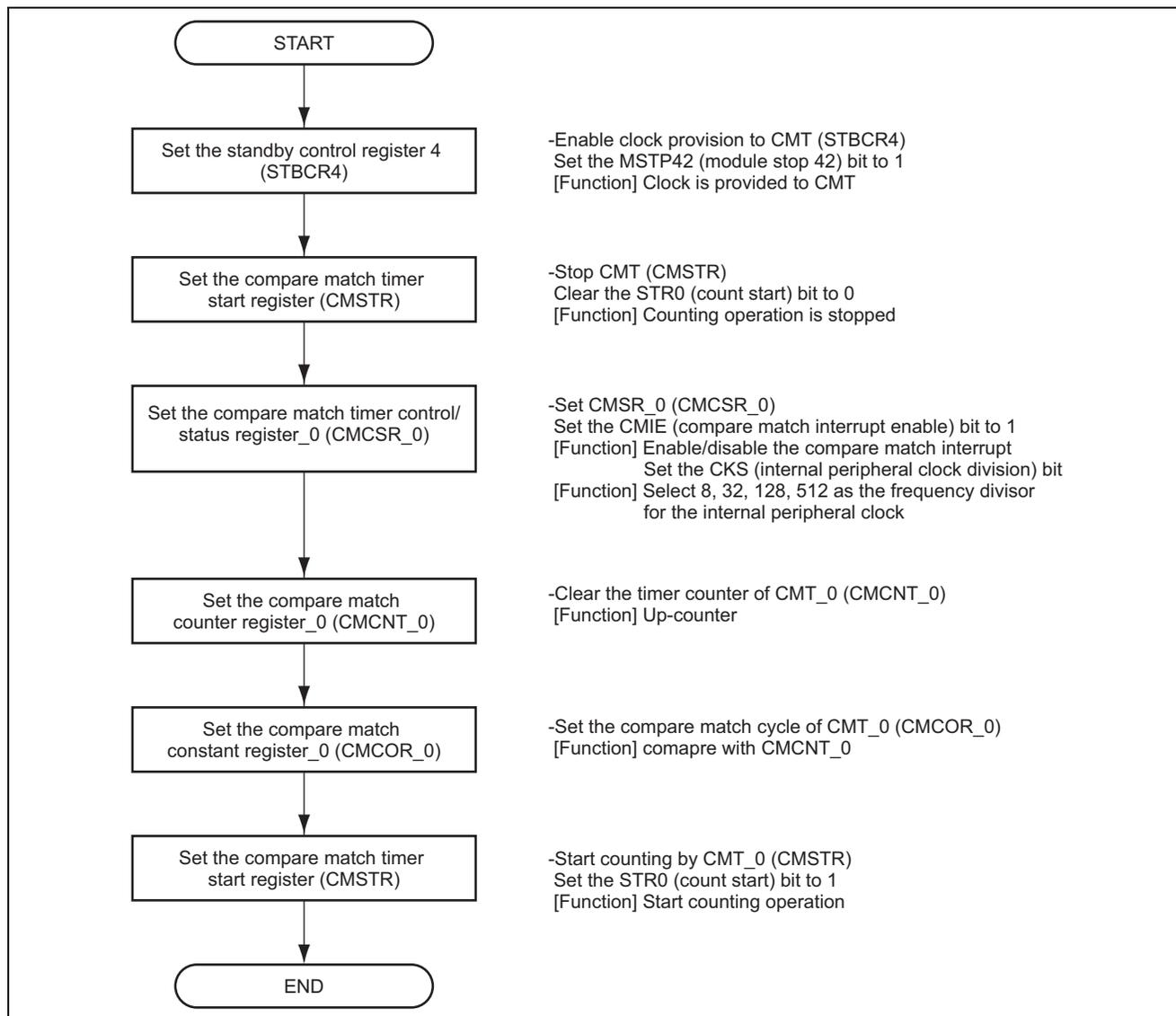


Figure 2 Example of Setting Cycle Count of Compare Match

2.3 Sample Program Operation

In the sample program, the compare match timer (CMT channel 0) is used as a timer that counts constant cycles per 1 ms.

Compare match flag set per 1 ms is counted 1000 times. At every 1000 times, port PE1 output is inverted.

Figure 3 shows the operation timing of sample program.

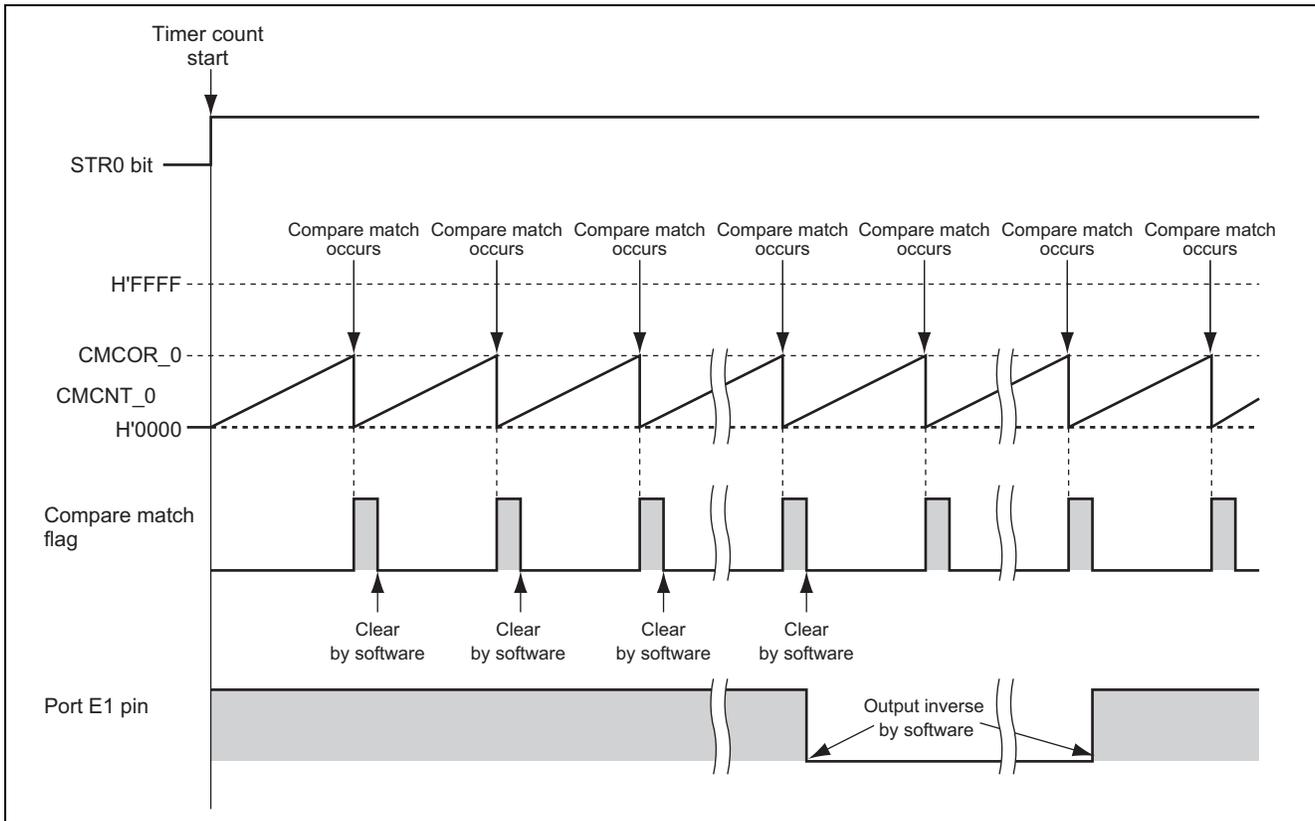


Figure 3 Operation Timing of Sample Program

2.4 Processing Procedure of Sample Program

Table 2 describes how to set compare match timer, and table 3 shows the variable and flag used in the sample program. Also, figure 4 shows processing flow of sample program.

Table 2 Compare Match Timer Setting

Name of Register	Address	Setting Value	Function
Standby control register 4 (STBCR4)	H'FFFE 040C	H'F0	MSTP42 = 0: CMT operates.
Compare match timer start register (CMSTR)	H'FFFE C000	H'0000	STR0 = 0: count is stopped.
		H'0001	STR0 = 1: count is started.
Compare match timer control/status register_0 (CMCSR_0)	H'FFFE C002	H'0002	-CMIE = 1: compare match interrupt is disabled. -CSK1 = B'11: P ϕ /128
Compare match counter_0 (CMCNT_0)	H'FFFE C004	H'0000	Timer counter is cleared (H'0000).
Compare match constant register_0 (CMCOR_0)	H'FFFE C006	H'0104	260 times (H'0104): About 1 ms. (1000000 ns/3840 ns (520 KHz))

Table 3 Variable and Flag Used in the Sample Program

Variable/Flag Name	Setting Value	Function
CountCMT0	H'000003E8	1-second software counter (1000 times)
1-ms elapsed flag (CMF bit of CMCSR_0)	H'0040	Compare match flag is used as the 1-ms passed flag

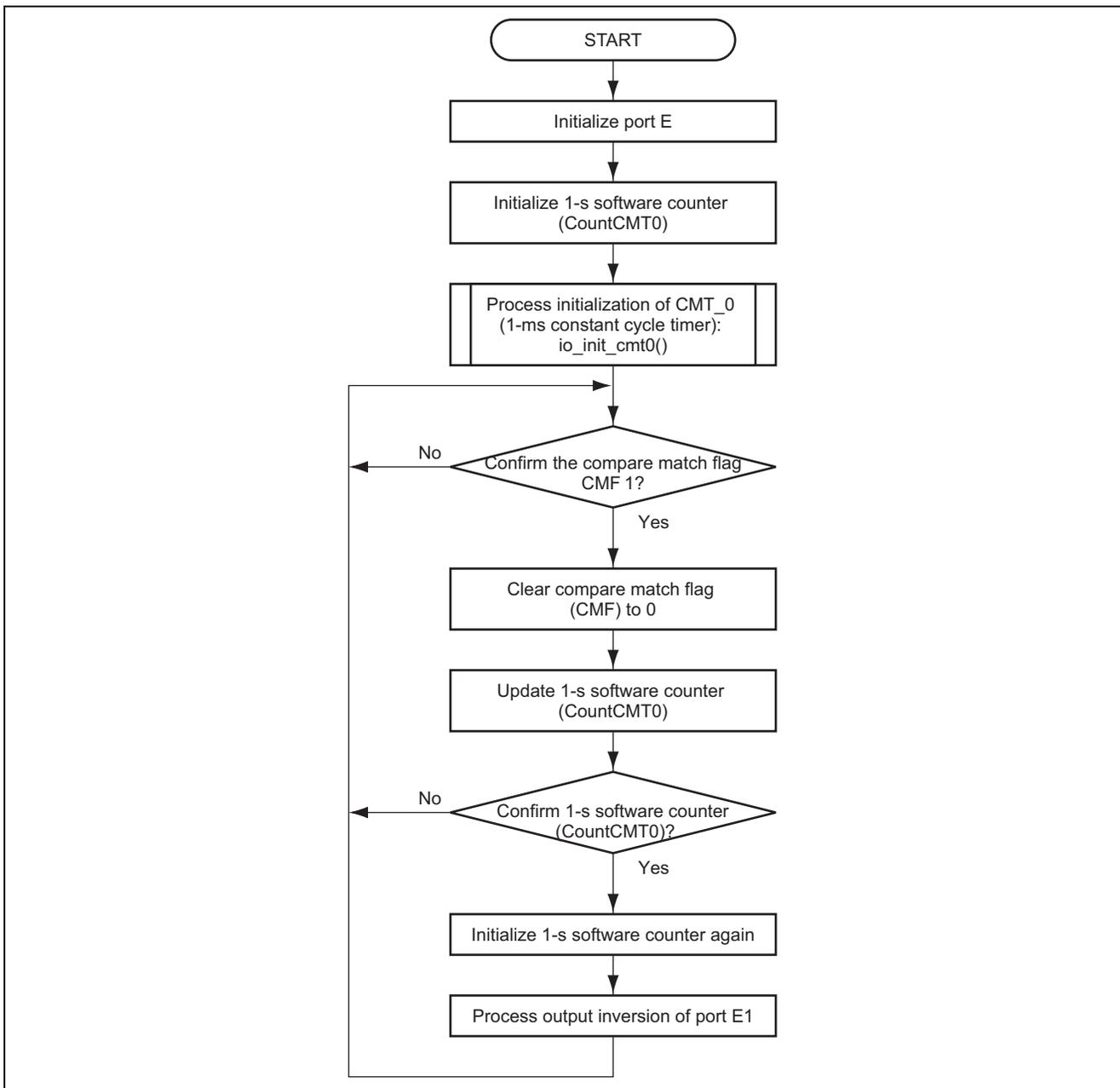


Figure 4 Example: Processing Flow of Sample Program

3. Sample Program

- Sample Program List of the “main.c” (1)

```

1      /*"FILE COMMENT"*****
2      *   System Name : SH7206 Sample Program
3      *   File Name  : main.c
4      *   Contents  : Constant cycle count (CMT:CMF polling) sample program
5      *   Version   : 1.00
6      *   Model     : M3A-HS60
7      *   CPU       : SH7206
8      *   Compiler  : SHC9.0.00
9      *
10     *   Note      : Sample of constant cycle timer (1 ms) using CMT0
11     *                LED connected to PE1 is turned on or off at every 1000
12     *                times of 1-ms passed flag (compare match flag).
13
14     *                <Cautions>
15     *                This entire sample program is for reference only and
16     *                will not guarantee the operation.
17     *                Please use this sample as your technical reference
18     *                at software development.
19     *
20     *   Copyright (C) 2003 Renesas Technology Corp. All Rights Reserved
21     *   and Renesas Solutions Corp. All Rights Reserved
22
23     *   History    : 2004.10.26 ver.1.00.00
24     /*"FILE COMMENT END"*****
25     #include <machine.h>
26     #include "iodefine.h"
27
28     /* ==== Prototype Declaration ==== */
29     void main(void);
30     void io_init_cmt0(void);
31
    
```

• Sample Program List of the “main.c” (2)

```

32  /*"FUNC COMMENT"*****
33  * ID          :
34  * Overview of module : Sample program main (constant cycle count)
35  *-----
36  * Include      : #include "iodefine.h"
37  *-----
38  * Declaration  : void main (void)
39  *-----
40  * Function     : IO port PE1 (connected to LED) and compare match
41  *              : timer CMT0 (1-ms) are initialized. At every 1000
42  *              : times of 1-ms (interrupt request bit) flag count,
43  *              : LED connected to PE1 is turned on or off.
44  *-----
45  * Argument     : None
46  *-----
47  * Return value : None
48  *-----
49  * Caution     :
50  /*"FUNC COMMENT END"*****/
51 void main(void)
52 {
53 volatile unsigned int CountCMT0; /* For 1-second software count */
54
55 /* ==== Initializing of port E ==== */
56 PORT.PECRL1.BIT.PE1MD = 0x0; /* Set the pin to PE1 */
57 PORT.PEIORL.BIT.PE1IOR = 0x1; /* Set PE1 to output */
58 PORT.PEDRL.BIT.PE1DR = 0x1; /* Write output value = 1 to the port E data
59                             register */
60
61 /* ==== Initializing of 1-s software counter (CountCMT0) ==== */
62 CountCMT0 = 1000u; /* Count 1000 times */
63
64 /* === Initializing processing of CMT0 (1-ms constant cycle timer) === */
65 io_init_cmt0();
66
67 while(1){
68 /* ---- Confirming compare match (1 ms) flag ---- */
69 while (CMT.CMCSR0.BIT.CMF == 0){
70 /* Wait for flag set */
71     }
72
73 CMT.CMCSR0.BIT.CMF = 0; /* Clear compare match flag (CMF) to 0 */
74 CountCMT0--; /* Update 1-s software counter (CountCMT0)*/
75
76 /* ---- Confirming 1-s software counter ---- */
77 if(CountCMT0 == 0u){
78 CountCMT0 = 1000u; /* Initialize 1-s software counter again */
79 PORT.PEDRL.BIT.PE1DR ^=1u; /* Process inversion of port E1 output */
80     }
81 }
82 }
    
```

• Sample Program List of the “main.c” (3)

```

83  /*"FUNC COMMENT"*****
84  * ID          :
85  * Overview of module: Setting of CMT0 constant cycle timer
86  *-----
87  * Include     : #include "iodefine.h"
88  *-----
89  * Declaration : void io_init_cmt0 (void)
90  *-----
91  * Function    : CMT0 is set to count CMF flag at every 1 ms.
92  *-----
93  * Argument    : None
94  *-----
95  * Return value : None
96  *-----
97  * Caution    :
98  *"FUNC COMMENT END"*****/
99  void io_init_cmt0(void)
100 {
101  /* ==== Initial setting of cycle (1 ms) timer ==== */
102  /* ---- Setting standby control register 4 (STBCR4) ---- */
103  CPG.STBCR4.BIT.MSTP42=0x0; /* Cancel CMT module stop */
104
105  /* ---- Setting compare match timer start register (CMSTR) ---- */
106  CMT.CMSTR.WORD=0x0000; /* Stop channel 0 counter */
107
108  /* --- Setting compare match timer control/status register (CMCSR0) --- */
109  CMT.CMCSR0.WORD=0x0002; /* Disable compare match interrupt and
110                          set 1/128 peripheral clock */
111
112  /* ---- Setting compare match counter (CMCNT0) ---- */
113  CMT.CMCNT0.WORD=0x0000; /* Clear timer counter */
114
115  /* ---- Setting compare match constant register (CMCOR0) ---- */
116  CMT.CMCOR0.WORD=0x0104; /* Set the period until compare match (1 ms)*/
117
118  /* ---- Setting compare match timer start register (CMSTR) ---- */
119  CMT.CMSTR.BIT.STR=0x1; /* Start counting */
120
121  }
122  /* End of file */
    
```

4. Documents for Reference

- Software manual
SH-2A SH2A-FPU Software Manual Rev.3.00
(Please download the latest version from the homepage of Renesas Technology Corp.)
- Hardware manual
SH7206 Group Hardware Manual Rev.1.00
(Please download the latest version from the homepage of Renesas Technology Corp.)

5. Website and Support Window

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Rev.	Date	Description	
		Page	Summary
1.00	Sep.05.05	—	First edition issued

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