Analog/Digital PWM in the AnalogPAK
SLG47004

This application note describes how the AnalogPAK SLG47004 can be used to generate a PWM signal in various ways to act as the main controller of a device such as a dimmer. It can also be useful in modern electronic systems, automation systems, lighting installations, automotive applications, etc. It describes the implemented logic, the AnalogPAK configuration and the results obtained from testing the finished prototype of the device.

Contents

1. Introduction 2

2. Device Implementation 3

3. PWM Signal Generation 5

3.1 Manual Digital PWM Signal Generation 5

3.1.1. Changing the Duty Cycle 6

3.1.2. Limit Tracking Circuit 7

3.2 Automatic Digital PWM Signal Generation 9

3.3 Analog PWM Signal Generation 10

4. Conclusion 13

5. Revision History 14

Terms and Definitions

CNT	Counter
DC	Duty cycle
DFF	D flip-flop
IC	Integrated circuit
LED	Light emitting diode
LUT	Look up table
OP	Operational amplifier
OSC	Oscillator
PWM	Pulse width modulation
RH	Rheostat

References

For related documents and software, please visit:

GreenPAK™ Programmable Mixed-Signal Products | Renesas

Download our free Go Configure Software Hub [1] to open the .aap files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Renesas provides a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the Dialog IC.

[1] Go Configure Software Hub, Software Download and User Guide, Renesas Electronics
[2] AN-CM-379 Analog/Digital PWM by Analog PAK.aap, AnalogPAK Design File, Renesas Electronics
[3] GreenPAK Development Tools, Development Tools Webpage, Renesas Electronics
[4] GreenPAK Application Notes, Application Notes Webpage, Renesas Electronics
[5] SLG47004, Datasheet, Renesas Electronics

1. Introduction

This application note demonstrates the use of the AnalogPAK by Renesas, used as the main control component of another more complex device. Many primary devices in modern electronic systems, automation systems, lighting installations, etc. are generally controlled by a PWM signal, which is generated by a particular control system by changes to certain parameters. We will demonstrate how to build such a control system using only one Analog PAK device, in this example the SLG47004. Another important purpose of this application note is to highlight and demonstrate the application of the unique components of the AnalogPAK which, in addition to its analog components (operational amplifiers, comparators, etc.), also contains powerful digital functionality. Thus, it is capable of both digital and analog signal processing simultaneously.

The developed device, built on a single SLG47004 chip, can operate in three modes which are selected using two switches, SA1 "Manual/Avto" and SA2 "Di/Ai PWM".

- mDigital PWM signal generation mode with manual duty cycle adjustment using two buttons – “Duty cycle increase” SB2 and “Duty cycle decrease” SB1. This mode can be selected using the SA1 switch in the “Manual” position and the SA2 switch in the “Di PWM” position. By default, after power on, the duty cycle of the PWM signal is lk (0% Duty cycle), indicated by LED1 (green). Pressing the “Duty cycle increase” button increases the duty cycle by one step and pressing the “Duty cycle decrease” button decreases the duty cycle by 1 step accordingly. When no adjustment is made with the buttons, the device saves the last duty cycle value and retains it until the next change (until any button is pressed). This is a very convenient function, for example, to adjust the light brightness of a lighting lamp, which will be demonstrated later. LED2 (red) indicates that the maximum (100%) value of the duty cycle has been reached.
- Digital PWM signal generation mode with automatic duty cycle change. This mode is designed to demonstrate automatic duty cycle change from 0% to 100% and back. To do this, the digital PWM generation mode must be selected, which is done by setting the SA2 switch to the “Di PWM” position and the SA1 switch to the “Avto” position.
- Analog PWM signal generation mode. The SA2 switch must be placed in the “Ai PWM” position. In this case, a PWM signal with the same frequency is generated entirely by the analog functions of the SLG47004. To control the duty cycle in this mode, an interesting method is used. The value of the duty cycle of the PWM signal is directly proportional to the value of the external magnetic field measured by an external Hall sensor. In other words, the closer the permanent magnet is to the Hall sensor, the greater the value of the duty cycle of the PWM signal.

Thus, the first two operation modes are implemented using the digital functions of the device, and the third mode is implemented using the analog functions.

2. Device Implementation

The electric circuit diagram of our device is shown in Figure 1. An N-channel MOSFET transistor (Q1) is used in the circuit to control a powerful load (e.g., a 12 V bulb lamp or many connected LEDs), allowing for loads with a consumption current of up to 10 A (at 12 V voltage). The SLG47004 and the Hall sensor are powered by LDO (U1), which provides a constant 5 V supply voltage.

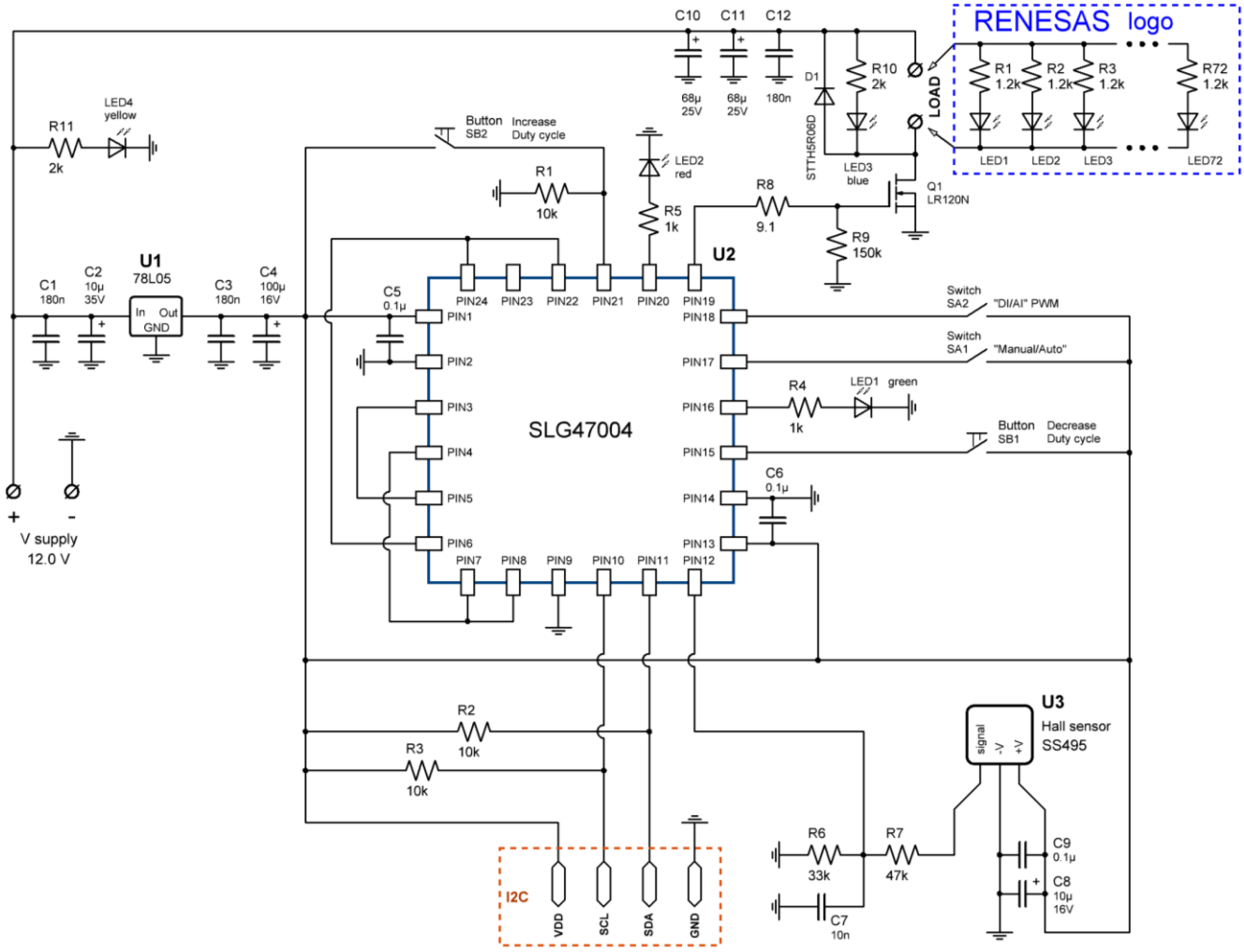

Figure 1: The electrical circuit diagram of the device

Figure 2 shows the first prototype of the device.

The circuit has four LEDs with different colors, indicating the following:

- LED1 (green) – indicates the duty cycle value of the digital PWM signal is 0%
- LED2 (red) – indicates the duty cycle value of the digital PWM signal is 100%
- LED3 (blue) – indicates the current value of the output duty cycle of the digital/analog PWM signal
- LED4 (yellow) – indicates the presence of a common input voltage of 12 V.

Also, as mentioned earlier, two mechanical switches are used to select operation modes:

- SA1 switch – selects manual or automatic duty cycle change mode for the PWM signal in digital generation mode
- SA2 switch – selects between digital or analog generation mode.

To change the duty cycle in digital generation mode, two buttons are used:

- SB1 – "Duty cycle decrease".
- SB2 – "Duty cycle increase"

Top view **Bottom view**

Figure 2: The first prototype of the device

An LED pattern in the form of the RENESAS logo is used as a load.

Figure 3: The device prototype displaying the RENESAS logo with LEDs

3. PWM Signal Generation

3.1 Manual Digital PWM Signal Generation

So, let us analyze how the PWM generator and its control circuit using digital components work.

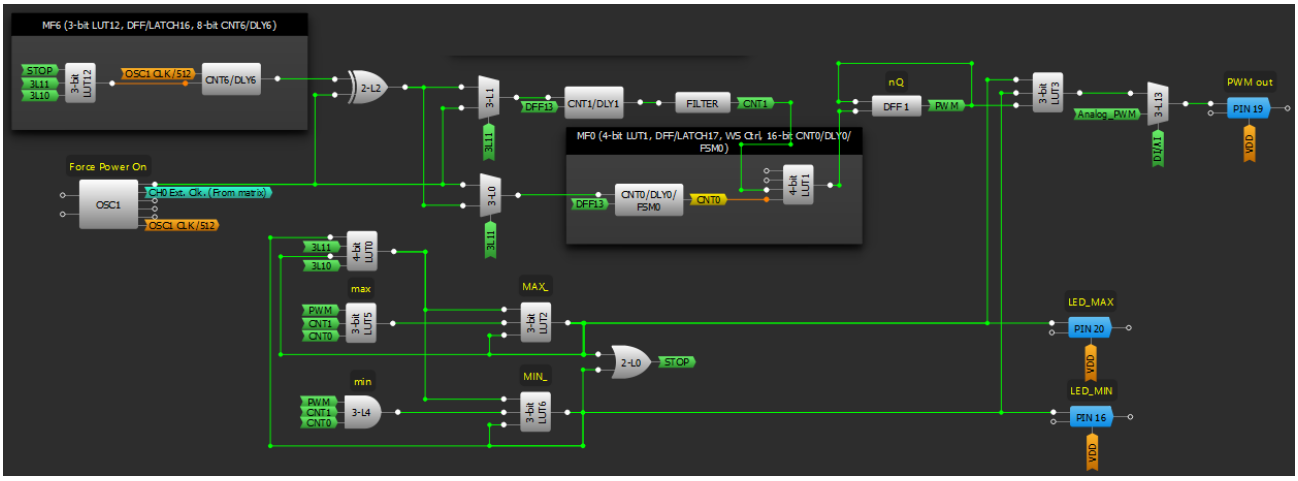

Figure 4: Digital Design in the GoConfigure Software

The main components of this PWM generator consists of three counters: CNT6, CNT1, and CNT0. The frequency of the PWM signal is 1 kHz and is determined by the CNT1 and CNT0 counters. These counters together with 4-bit LUT1, FILTER, and DFF1 form a classic PWM generator circuit operating on the principle of alternating state changes of the DFF1 trigger. The CNT0 counter sets the DFF1 trigger and the CNT1 counter resets the DFF1 trigger. However, an additional technique is used in our circuit – the counter data of both CNT1 and CNT0 counters are the same, ensuring a constant duty cycle of the PWM signal over time. In order to increase or decrease the duty cycle, a third counter (CNT6) is used. Together with the 2-bit LUT2 element configured as a logic XOR, it periodically inverses the clock frequency of the CNT1 and CNT0 counters (please see Figure 5 through Figure 7). The period of this change is determined by the counter data of the CNT6 counter.

Figure 5: The duration of the low signal level from 3-bit LUT12 (yellow upper line) indicating the unlocking of the CNT6 counter (teal) corresponds to the duration of pressing the SB1 or SB2 buttons

Figure 6: Zoomed-in image of Figure 5. The polarity of the clock frequency of the corresponding multiplexers corresponds to the increasing value of the duty cycle (when the SB2 button is pressed)

Figure 7: Zoomed-in image of Figure 5. The polarity of the clock frequency of the corresponding multiplexers corresponds to the decreasing value of the duty cycle (when the SB1 button is pressed)

3.1.1. Changing the Duty Cycle

Using the 3-bit LUT1 and 3-bit LUT0 elements configured as multiplexers, we can independently feed these two clock streams (inverted and non-inverted) to the CNT1 and CNT0 counters.

A high-level from the PIN21 input switches the multiplexers so that the CNT1 counter is fed with the non-inverted clock from the OUT0 output of the OSC1 oscillator, while the CNT0 counter is fed with the inverted clock from the 2-bit LUT2 XOR element resulting in this combination corresponding to an increase in the duty cycle.

Alternatively, a high-level from the PIN15 input switches the multiplexers so that the CNT1 counter is fed with the inverted clock from the OUT0 output of the OSC1 oscillator, while the CNT0 counter is fed with the non-inverted clock from the 2-bit LUT2 XOR element resulting in this combination corresponding to a decrease in the duty cycle.

By default (when there is a low-level signal from PIN21), the 3-bit LUT1 and 3-bit LUT0 multiplexers are configured to decrease the duty cycle, and a high-level signal from PIN15 allows only the CNT6 counter to operate, which was previously in “high level reset” mode due to the high-level signal from 3-bit LUT12. This allows the current duty cycle value to be maintained when no buttons are pressed.

In general, the 3-bit LUT12 logic element allows the duty cycle to be changed (unlocks the CNT6 counter) only when the SB1 or SB2 buttons are pressed and the duty cycle itself has not reached one of the two extreme limits of 0% or 100%. If the duty cycle limits have been reached, then we can only decrease it with the SB1 button at duty cycle 100% (see section 3.1.2).

Accordingly, if the duty cycle value is 0%, that is, there is no PWM signal at the output, we can only increase the duty cycle value with the SB2 button. This is also the default state of the system after it is turned on. When power is applied, all the counters of the system are blocked by a high signal from the DFF13 trigger, and the system is waiting for a high-level signal from PIN21 to change the state of the DFF13 output to low, which in turn will allow normal operation of all counters.

3.1.2. Limit Tracking Circuit

The duty cycle limit tracking circuit is built using the 4-bit LUT0, 3-bit LUT5, 3-bit LUT4, 3-bit LUT2, 3-bit LUT6, 2-bit LUT0, and 3-bit LUT3 elements. This circuit tracks and prevents further changes in the duty cycle when it reaches the min and max limits of 0% or 100%. 3-bit LUT5 and 3-bit LUT4 act as the limit detectors, which track the state of two specific combinations between three signals (see Figure 8):

- "PWM Duty cycle" – output of DFF1
- "Reset signal" – output of FILTER/CNT1
- "Set signal" – output of CNT0

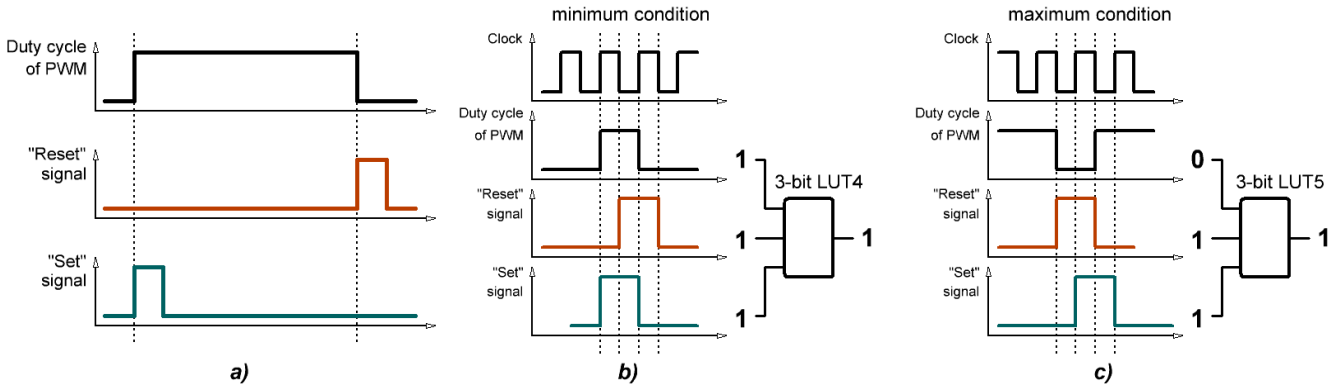

Figure 8: Timing diagrams describing the operation of the min/max duty cycle detection circuit

When the maximum condition is met (100%), the corresponding latch on 3-bit LUT2 is activated preventing further changes in the duty cycle (and sets the CNT6 counter to its "high level reset" state) and, using 3-bit LUT3, outputs a high-level signal corresponding to 100% duty cycle. Similarly, when the minimum condition is met (0%), the corresponding latch on 3-bit LUT6 is triggered preventing further changes in the duty cycle and outputs a low-level signal to 3-bit LUT3 corresponding to 0% duty cycle. These latches are reset when the duty cycle is at 100% and then is decreased and vice versa (at 0% and duty cycle is increased). Figure 9 through Figure 11 show the timing diagrams for the PWM signals under normal, minimum, and maximum duty cycle states, respectively.

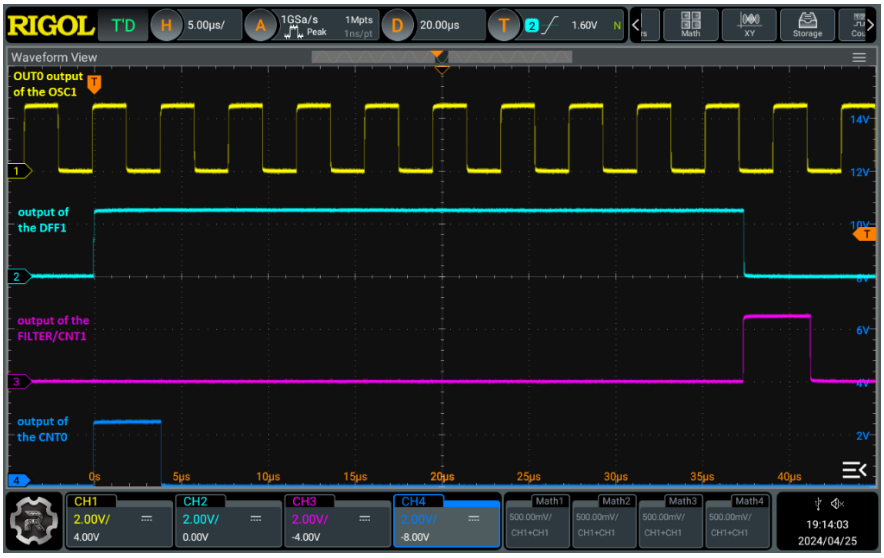

Figure 9: Normal PWM signal

Figure 10: Minimum of the PWM signal

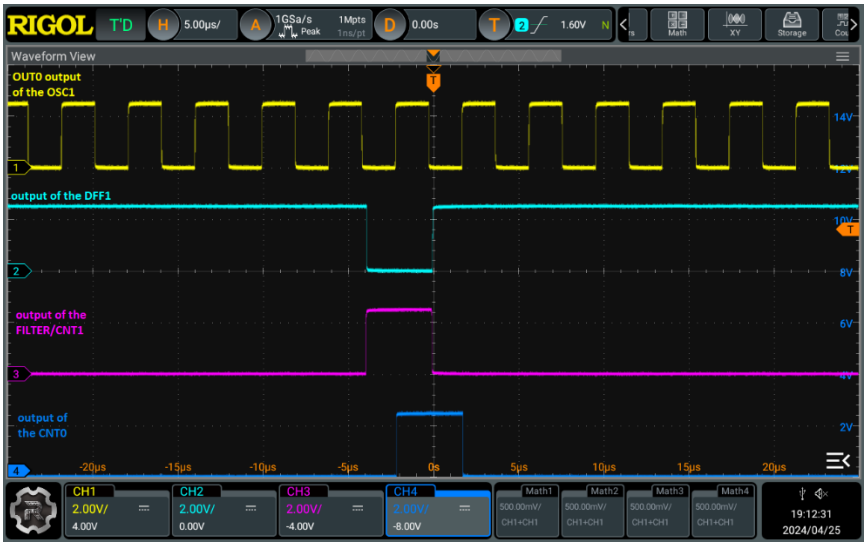

Figure 11: Maximum of the PWM signal

3.2 Automatic Digital PWM Signal Generation

To demonstrate the automatic duty cycle change mode (when digital PWM generation mode is active, the SA2 switch is set in the “Di PWM” position), we need to apply a high-level signal to PIN17 (flip the SA1 switch to the “Auto” position). This high-level signal switches the two digital multiplexers (using 3-bit LUT10 and 3-bit LUT11) to use the internal oscillator to be the source of the “increase/decrease” duty cycle signals, instead of the externally connected SB1 and SB2 buttons. This internal oscillator is built using DLY4, DLY5, and 3-bit LUT8 and functions similarly to pressing the “Duty cycle increase” (SB2) button until the duty cycle reaches 100% and then pressing the “Duty cycle decrease” (SB1) button until it reaches 0% at an interval of ~ 5 seconds and then repeating. This interval is enough to demonstrate a smooth increase from 0% to 100% and a smooth decrease from 100% to 0% of the duty cycle of the PWM signal.

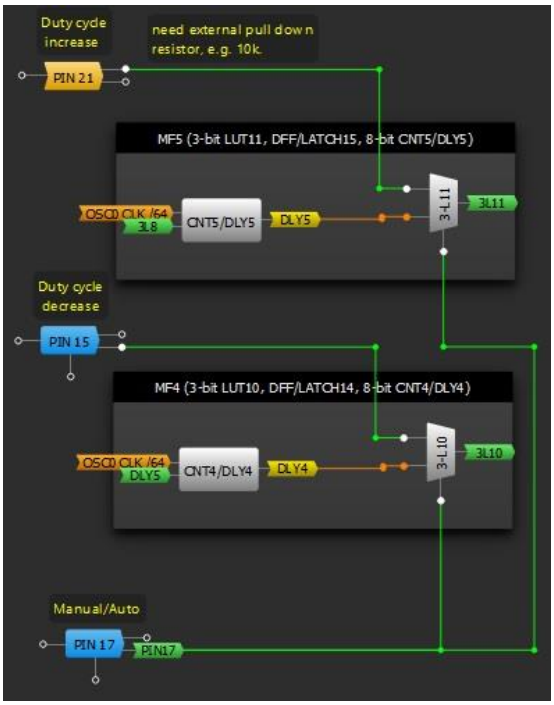

Figure 12: Part of the Digital Design that operates as an internal OSC to change PWM duty cycle automatically

3.3 Analog PWM Signal Generation

To enter analog PWM signal generation mode, SA2 needs to be switched to the “Ai PWM” position. A high-level signal from PIN18 will switch the 3-bit LUT13 multiplexer to receive the input signal from the analog component of the circuit (see Figure 13), namely the ACMP0L comparator, instead of the digital generation circuit (the output of 3-bit LUT3).

The PWM signal generated by the analog component of the circuit is based on a traditional scheme where the analog comparator compares the linearly variable voltage input signal (which in our case the variable voltage ranges from 0 mV to 1000 mV) received from an external sensor to a voltage amplitude having a sawtooth shape. This sawtooth voltage is created with the help of two 10-bit digital rheostats RH0 and RH1, which are innovative components of the SLG47004 AnalogPAK. By taking advantage of the ability to incrementally change the resistance of the two rheostats simultaneously (in the range from ~98 Ω to 100 kΩ) and the ability to operate under the influence of an external clock signal, a digital potentiometer is built based on these two rheostats.

Together with a constant voltage source, based on V_{REF} OA1 and operational amplifier OPAMP1, the digital potentiometer acts as a sawtooth voltage generator, a necessary element for the PWM signal synthesis circuit. A unique aspect of this potentiometer is that by default, when the circuit is turned on, the resistance of the upper arm RH0 is at a maximum (~100 kΩ), and the lower arm RH1 is, respectively, at a minimum, and with each clock signal of the internal oscillator OSC1 (the selected period is ~ 1024 kHz), the arm resistances change by the value of the resistance of one signal step (step resistance = 99 Ω). The resistance of the upper arm decreases, and the resistance of the lower arm increases until all 1024 steps are completed. In parallel, CNT2 and CNT3 also count the number of clock signals sent to the rheostats and after every 1024 steps, the CNT3 counter generates a signal to reset the rheostats (i.e., the potentiometer). In other words, the virtual slider of the potentiometer starts at the bottom of the potentiometer, under the ground potential GND (zero voltage at the slider output). Then, the potentiometer changes the resistance step by step (the slider moves upwards to the potential of the voltage source, the output of OPAMP1) and after 1024 steps, the slider reaches the maximum of 1024 mV, and at the same time, returns to its initial position due to the signal from the CNT3 counter. This generates a sawtooth voltage with a maximum amplitude of 1024 mV and a frequency of 1024 kHz/1024 = 1 kHz, which is equal to the frequency of the digital PWM signal (see Figure 14 through Figure 17).

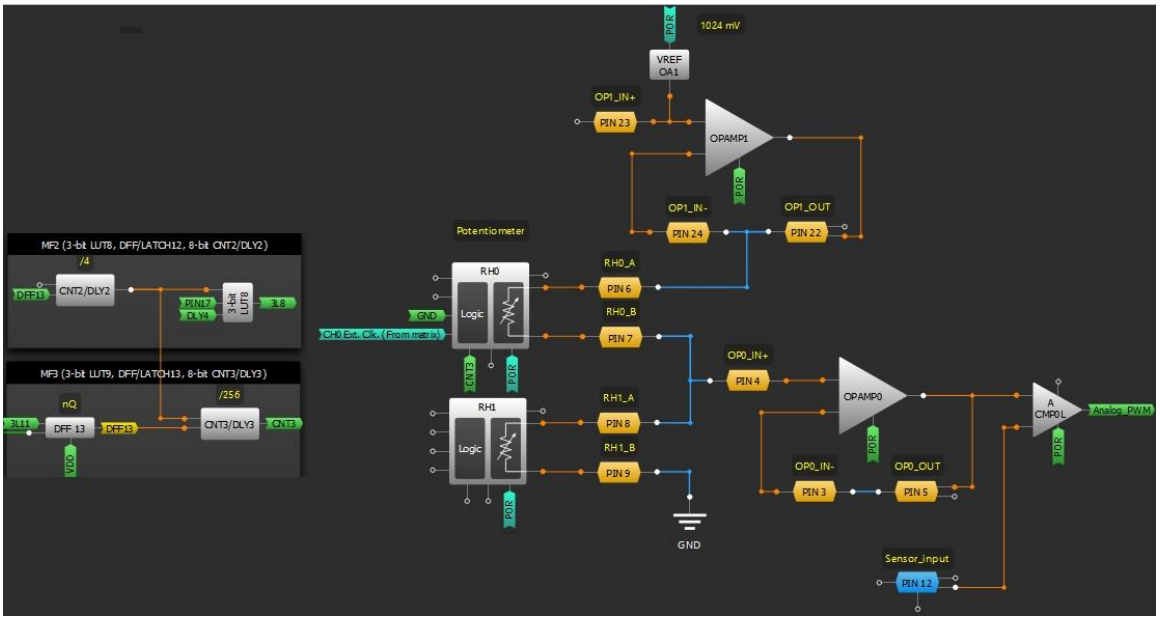

Figure 13: Analog component of the PWM signal generator

Figure 14: Operation of the PWM generation circuit. Duty cycle is ~1%

Figure 15: Operation of the PWM generation circuit. Duty cycle is ~10%

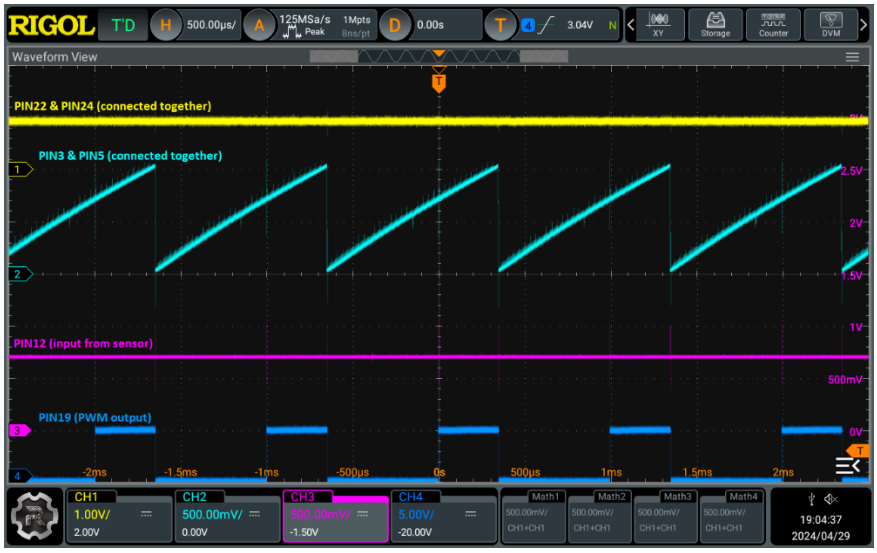

Figure 16: Operation of the PWM generation circuit. Duty cycle is ~35%

Figure 17: Operation of the PWM generation circuit. Duty cycle is ~95%

As can be seen from Figure 14 through Figure 17, the duty cycle of the analog PWM signal depends on the amplitude of the voltage signal coming from the external Hall sensor. This signal is fed to the negative analog input of the ACMP0L comparator, which ensures the absence of a PWM signal when the magnetic field strength is zero (duty cycle is 0% when no permanent magnet is near the sensor). Under such conditions, our Hall sensor (type SS495) outputs half of the supply voltage ($V_{DD}/2$ = 2.5 V) and, thanks to the resistor dividers R6 and R7 (see Figure 1), normalizes its output signal to ~1030 mV. When the permanent magnet approaches the sensor, the magnitude of the magnetic field increases and the amplitude of the signal voltage from the sensor decreases proportionally, leading to a corresponding increase in the duty cycle of our PWM signal. Thus, we can set the desired value of the duty cycle of our analog PWM signal by changing the magnitude of the external magnetic field (i.e., by changing the distance between the sensor and the magnet).

4. Conclusion

This Application Note contains complete information on the following:

- the functional structure of the developed device and its main control element, the SLG47004 chip
- a description of the system's operating principles and a description of the methods used to generate the PWM signal
- demonstrations of the prototypes.

The AnalogPAK consists of a large number of both digital and analog universal components that allow simple and efficient implementation of countless numbers of circuit solutions. This further reduces the number of external circuit elements required. The functionality of the device we have demonstrated unquestionably supports this point. It should also be noted that although the lower power consumption of GreenPAK devices and their relatively small size are the main advantages, there are other unique advantages, such as significantly lower cost, faster design and configuration made possible by our free GoConfigure Software Hub software, etc., which serve serves as additional incentives to choose RENESAS products.

Based on this Application Note, a demoboard for Embedded World 2024 was created. Please see Figure 18.

Figure 18: The demoboard for Embedded World 2024

By using the example described in this application note demonstrating the use of our AnalogPAK device as a control element as a starting point, the possible designs based on this example are only limited by the developer's imagination.

5. Revision History

Revision	Date	Description
1.00	May 13, 2024	Initial release.

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