DC-DC Boost & Buzzer Driver
SLG47105

This application note describes how to create a Piezo Driver and Boost DC-DC Converter using one HVPAK SLG47105.

The application note comes complete with design files which can be found in the Reference section.

Contents

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1. Terms and Definitions

DFF	D Flip-Flop
HV	High Voltage
LUT	Look-up Table
MF	Multi-function
OSC	Oscillator

2. References

For related documents and software, please visit: HVPAK™ | Renesas

Download our free Go Configure Software Hub [1] to open the .hvp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Find out more in a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the GreenPAK IC.

[1] Go Configure Software Hub, Software Download, and User Guide

[2] AN-CM-378 DC-DC Boost & Buzzer Driver, GreenPAK Design File

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage

[5] SLG47105 Datasheet, Renesas Electronics

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3. Introduction

The HVPAK SLG47105 is a flexible configurable mixed-signal IC able to combine a boost DC-DC converter and a piezo driver in a single package with a small number of external components.

The main goal of this application note is to show how to configure HVPAK to drive a 1 kHz piezo and how to create a Boost DC-DC converter from 3 V to 9.5 V. The whole circuit is powered with a 3V CR2032 battery. Such a schematic can be used in devices that require short-term notifications (keychains for finding things, and others). When the push button is pressed, the DC-DC converter boosts the voltage to 9.5 V which powers the piezo driver. Then the short pattern is played, and the circuit goes to sleep mode until the button is pressed again. When the circuit is ON – it consumes nearly 8.5 mA RMS, and in sleep mode less than 50 nA.

4. Operating Principle and HVPAK Design

The DC-DC Boost & Buzzer Driver Circuit Diagram is shown in Figure 1.

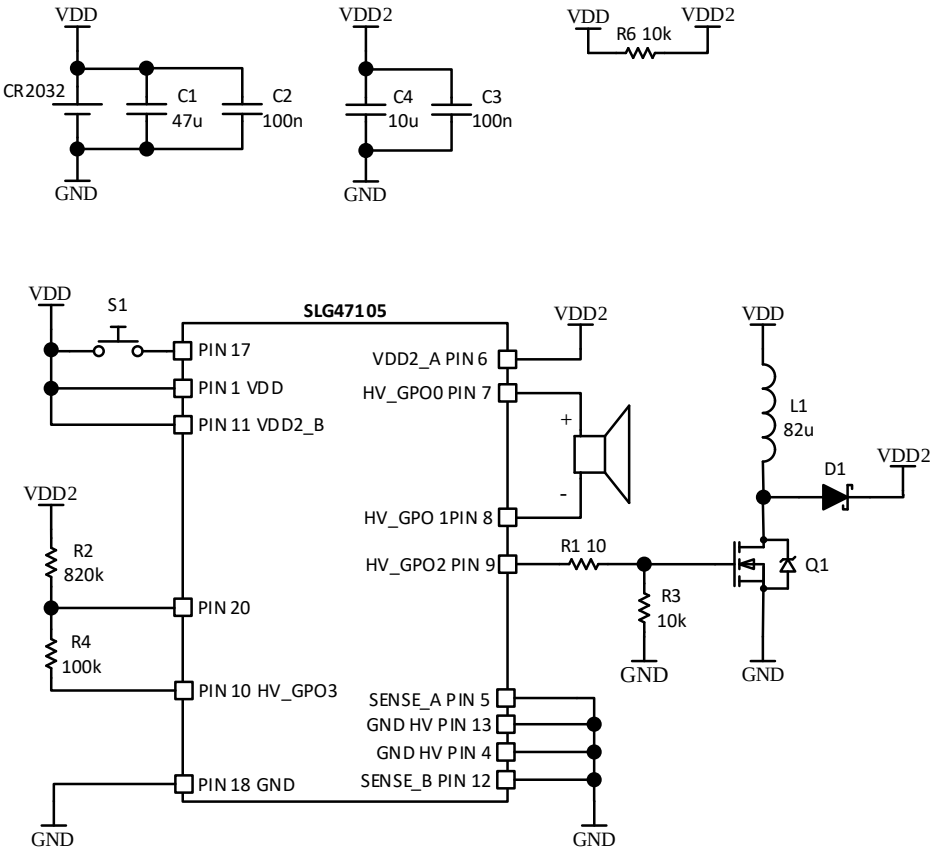

Figure 1. DC-DC Boost & Buzzer Driver Circuit Diagram

The design consists of a DC-DC Boost Converter and Buzzer Driver parts.

For the DC-DC Boost Converter, the PWM0 forms the ~197 kHz signal. The OSC0 forms the 1 kHz clock for a soft start to reduce inrush current, which can occur when the device is first turned on. Pipe Delay and CNT4/DLY4 set minimum and maximum duty cycles. The maximum duty cycle is limited to 2.32 us (D ~ 45.7%) to limit the inductor current.

$$\Delta I_L = \frac{V_{IN(\min)} \cdot D}{f_{PWM} \cdot L}$$

$$\Delta I_L = \frac{2.5 \cdot 45.7}{196.85 \cdot 82 \cdot 10^{-1}} = 70\ mA$$

The VDD and VDD2_B are connected to a 3 V battery (V_{DD}). VDD2_A (V_{DD2}) is connected to the boost output. To monitor this voltage, the resistors R2 and R4 form the resistive divider with a feedback signal, which goes to PIN 20 (Analog Input). This feedback voltage is compared with 1024 mV Vref by ACMP1H forming the ACMP signal which goes to the CHOP input of the PWM Chopper 0. If the V_{DD2} exceeds 9.5 V, the ACMP signal is HIGH and chops the formed PWM signal. The PWM Chopper 0 output goes to HV OUT CTRL1 (Half Bridge) input IN0. Then PIN 9 drives an NFET of the boost converter.

To reduce the current consumption in sleep mode, a resistive divider is connected to PIN 10 (Low Side ON) with a GND input.

Note: it's possible to change the ACMP1H Vref and boost the voltage up to 13 V ensuring up to 26 V peak-to-peak on a piezo buzzer.

The HVPAK Design is shown in Figure 2.

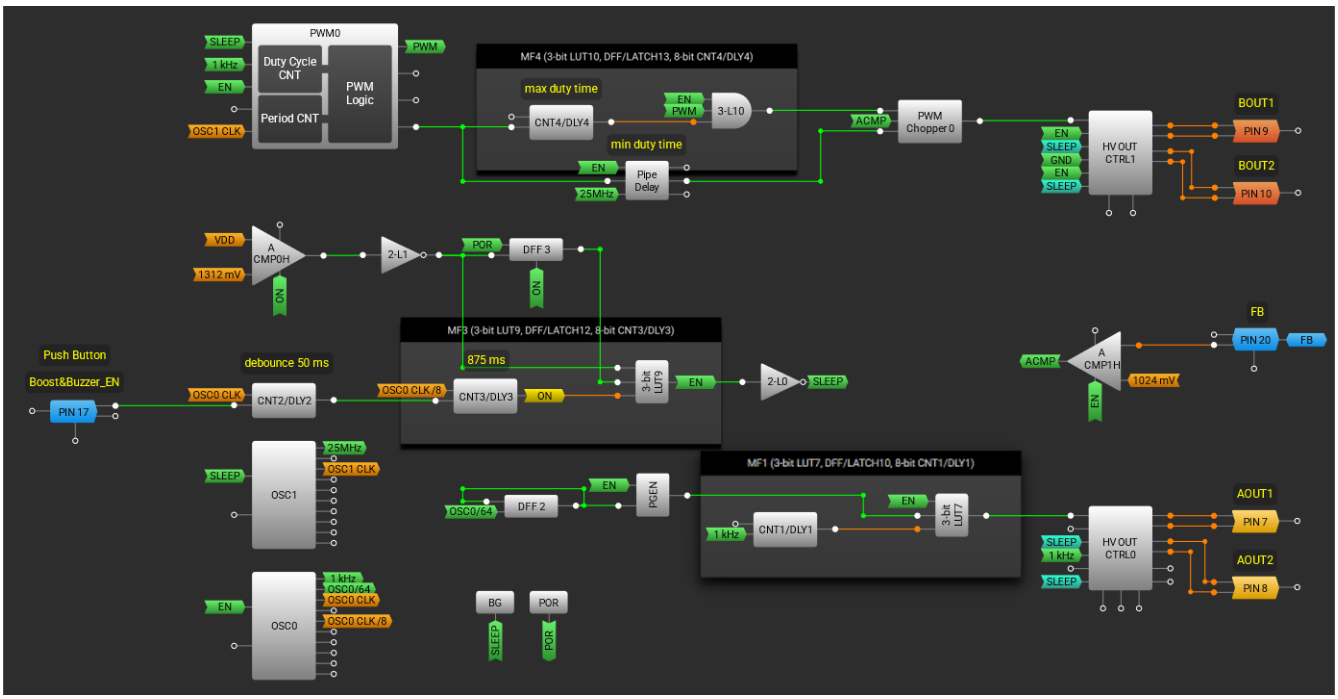

Figure 2. DC-DC Boost & Buzzer Driver HVPAK Design

The HV OUT CTRL0 (Full Bridge) drives a piezo buzzer. The peak-to-peak voltage on the piezo buzzer equals 2xV_{DD2} or 19 V. OSC0 forms a 1 kHz signal for a piezo, this signal comes to the PH input of HV OUT CTRL0. CNT1/DLY1 is configured as a One-shot and outputs the 520 ns signals on each edge of the 1 kHz signal. During these 520 ns pulses, HV pins will be in a Hi-Z state. Therefore, while switching the phase, N-FETs will not be ON simultaneously.

The 3-bit LUT7 forms the EN signal for the HV OUT CTRL0. It consists of the sound pattern signal, the general EN signal, and the CNT1/DLY output. The PGEN generates the sound pattern (01010101101011). The EN signal – the general ENABLE signal for the whole design is HIGH for 875 ms (CNT3/DLY3 One Shot) if the button is pressed (CNT2/DLY2 50 ms debounce) and the V_{DD} is higher than ~2.5 V (ACMP0H + 2-bit LUT1 + DFF3).

The 2-bit LUT0 inverts the EN signal forming the SLEEP signal to shut down the blocks when they are not used to reduce the power consumption.

5. Design Testing

Channel 1 (blue / 1st line) – V_{DD} (Vbat).

Channel 2 (red / 2nd line) – V_{DD2}.

Channel 3 (green / 3rd line) – battery current (Ibat).

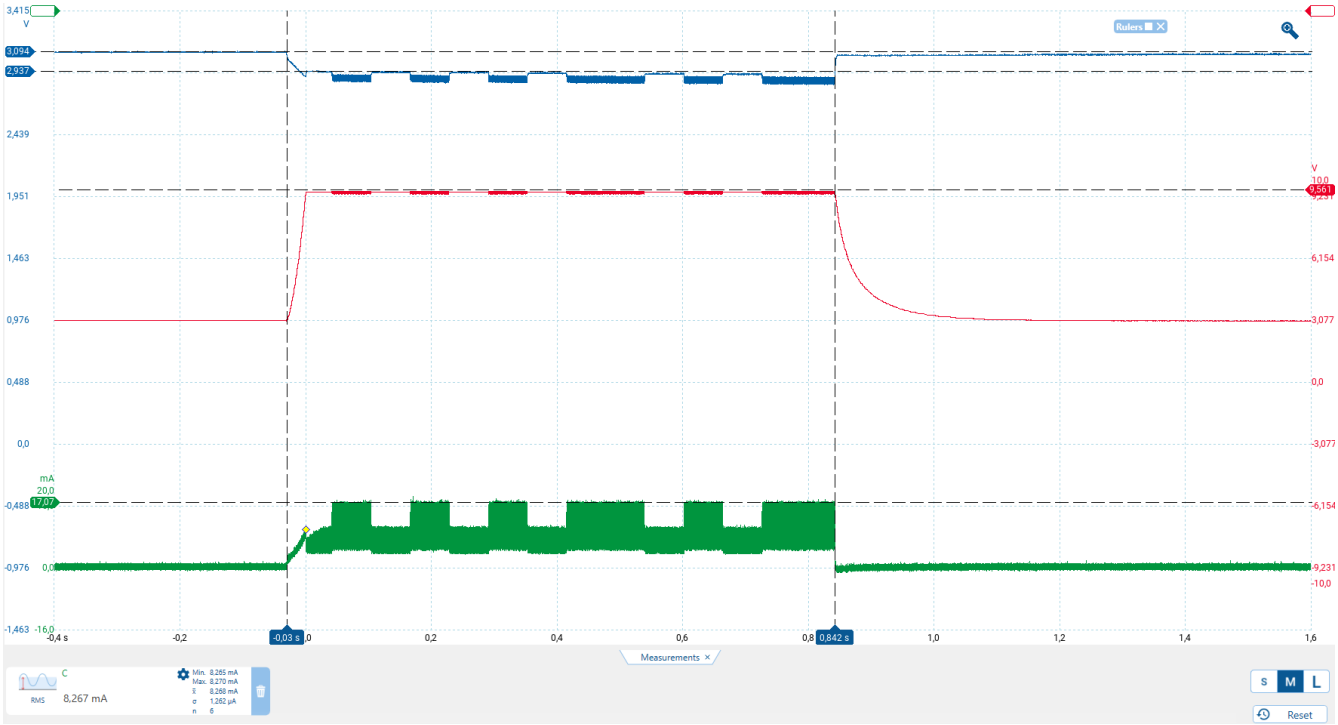

Figure 3. Whole Trace Test Results

As can be seen in Figure 3, the V_{DD2} level is 9.5 V as expected. The average current consumption is ~8.5 mA. The voltage drop on the battery is about 150 mV.

Channel 1 (blue / 1st line) – V_{DD2}.

Channel 2 (red / 2nd line) – HV GPO2 (PIN 9).

Channel 3 (green / 3rd line) – battery current (Ibat).

Channel 4 (yellow / 4th line) – inductor current.

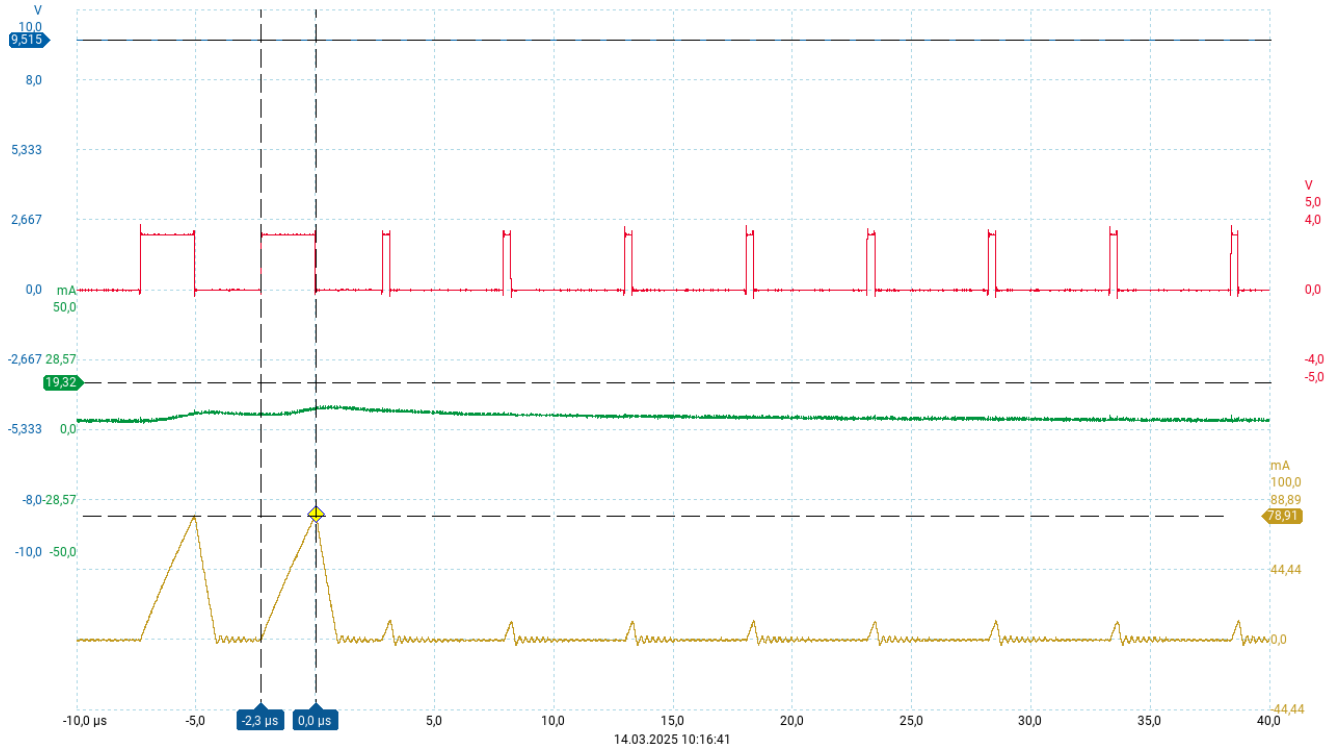

Figure 4. Maximum Duty Cycle Test Results

Figure 4 shows the maximum duty cycle of 2.3 us as was set by CNT4/DLY4 and the corresponding inductor current of 70 mA as calculated.

6. PCB Design

The proposed Demo PCB Design is shown in Figure 5 (top) and Figure 6 (bottom). As can be seen in Figure 5, the design is so compact that it can be placed under the buzzer.

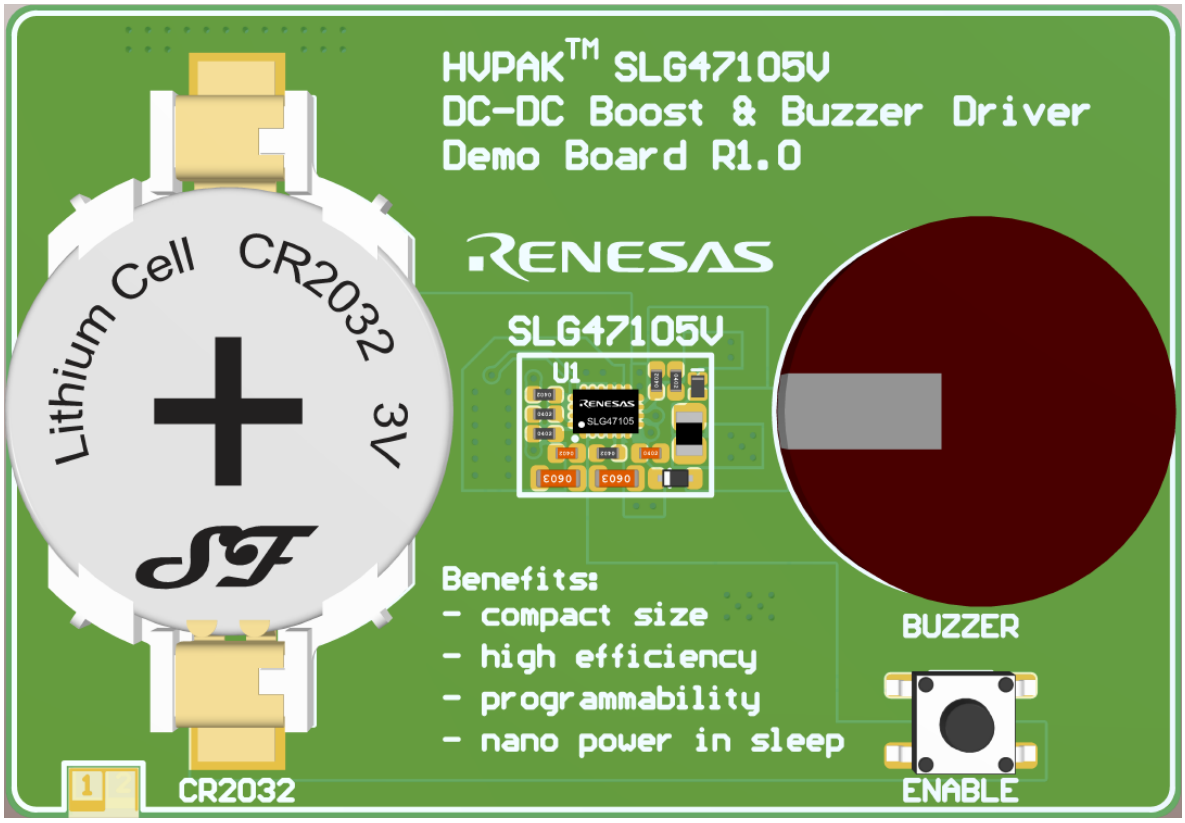

Figure 5. Boost & Buzzer Driver Demo PCB Design (Top Side)

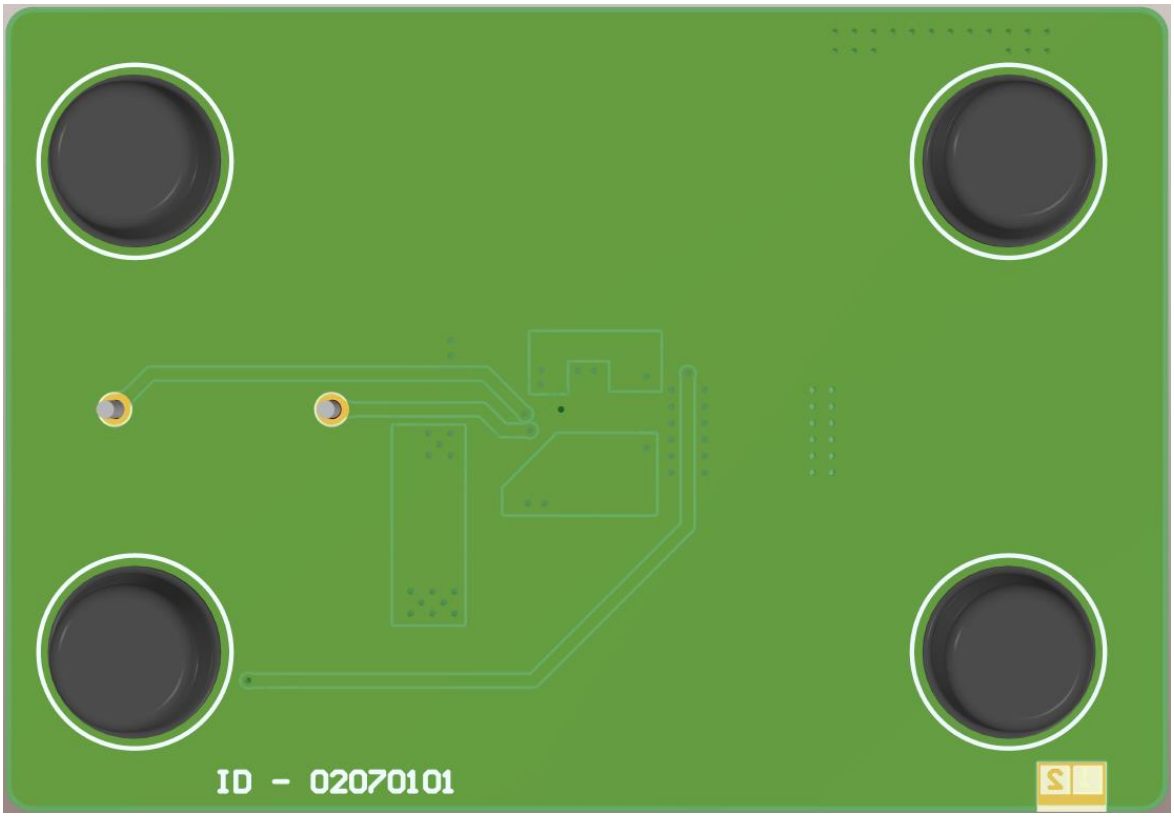

Figure 6. Boost & Buzzer Driver Demo PCB Design (Bottom Side)

7. BOM

#	Designator	Name	Manufacturer Part Number	Manufacturer	Quantity
1	BH1	Battery Holder	BU2032SM-BT-GTR	Memory Protection Devices	1
2	BP1- BP4	SJ61A6	7010334512	3M	4
3	BT1	CR2032	CR-2032L/BN	Panasonic	1
4	C1	47uF 20% 6.3V X5R 0603	GRM188R60J476ME15D	Murata Electronics	1
5	C2, C3	0.1uF 10% 25V X5R 0402	CL05A104KA5NNNC	Samsung Electro-Mechanics	2
6	C4	10uF 20% 25V X5R 0603	CL10A106MA8NRNC	Samsung Electro-Mechanics	1
7	D1	RB521S30T1G	RB521S30T1G	ON Semiconductor	1
8	L1	82uH 150mA	LQH2MPN820MGRL	Murata Electronics	1
9	LS1	SFN-17-B	SFN-17-B	Global Tone	1
10	Q1	MOSFET-N	DMN2400UFB-7	Diodes	1
11	R1	10R 1% 0402	RC0402FR-0710RL	YAGEO	1
12	R2	820k 1% 0402	RC0402FR-07820KL	YAGEO	1
13	R3, R6	10k 1% 0402	RC0402FR-0710KL	YAGEO	2
14	R4	100k 1% 0402	RC0402FR-07100KL	YAGEO	1
15	S1	Sw Tactile NO	PTS647SK38SMTR2LFS	ITT C&K	1
16	U1	SLG47105V	SLG47105V	Renesas Electronics America Inc	1

8. Conclusion

This application note describes how to configure the HVPAK SLG47105 to create a Boost & Buzzer Driver device that can work with a single 3 V CR2032 battery. SLG47105V ensures less than 50 nA sleep current and 19 V peak-to-peak voltage on a piezo buzzer.

The flexibility of the internal resources allows adapting it to the needs of the customer without effort.

9. Revision History

Revision	Date	Description
1.01		Updated section Design Testing Updated BOM Updated section Operating Principle and HVPAK Design Updated DC-DC Boost & Buzzer Driver Circuit Diagram
1.00	June 26, 2024	Initial release

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