Application Note

Implementation of 555 Timer using GreenPAK

AN-CM-278

Abstract

This application note illustrates the behavior of all operation modes of the 555 timer IC and shows the implementation details of the 555 timer internals, with all its operation modes, using the SLG46110V.

This application note comes complete with design files which can be found in the References section.

Contents

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1 Terms and Definitions

IC	Integrated circuit
IR	Infrared
LED	Light-emitting diode

2 References

For related documents and software, please visit:

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Download our free GreenPAK™ Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Find out more in complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the GreenPAK IC.

[1] GreenPAK Designer Software, Software Download and User Guide

[2] AN-CM-278 Implementation of 555 Timer using GreenPAK.gp, GreenPAK Design File

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage

[5] 555 timer IC, en.wikipedia.org (2018)

3 Introduction

This application note demonstrates the implementation of the monostable, astable, and bistable behavior of the 555 timer IC using SLG46110V. As SLG46110V has most of the resources necessary, such as two analog comparators, an open-drain configurable output pin, and LUTs, it is possible to implement the 555 timer internals and use SLG46110V as an alternative. The SLG46110V is very small in size when compared with standard 555 timer ICs, which saves PCB space. This version of the 555 Timer is especially useful for wearable electronics.

This implementation could also be used in all applications that use a multivibrator:

- Debounce a momentary/pushbutton switch using monostable operation.
- Turn ON the actuator for a set period or after a fixed period using monostable operation.
- Create a clock signal using astable mode of operation.
- Use for modulating transmitters such as ultrasonic or IR transmitters using astable mode.
- Use as a frequency divider.
- Use as a toggle flip-flop or memory cell in the bistable mode of operation.

4 System Overview

This internal block has five main sections: HIGH to LOW cutoff monitor, LOW to HIGH cutoff monitor, SR flipflop block, charging/discharging switch, and output driver. ACMP0 monitors LOW to HIGH cutoff whereas ACMP1 monitors HIGH to LOW cutoff. In case of LOW to HIGH cutoff, ACMP0 sets the SR flip-flop. Likewise, ACMP1 resets the SR flip-flop during HIGH to LOW cutoff event. The SR flip-flop block remembers the current state and gives the signal to both the charging/discharging switch and the output driver. The charging/discharging switch is achieved by configuring PIN8 as open-drain output, and the output driver is performed using a buffered output connected to PIN12. The internal block diagram is shown in Figure 1.

Analog comparators available in GreenPAK have the following characteristics: The VIN- connections of both analog comparators share the same external Vref pin, PIN4, which must not exceed 1.2 V at 3.3 V VDD. VIN+ of another comparator has access to either an external pin or VDD as input with a range of VDD. Considering these limitations and the non-availability of a resistor network as found in the standard 555 timer IC, it is necessary to map the input voltage range within acceptable criteria and use an internal Vref block over a resistor network to derive the cutoff voltage. The rationale is explained in detail in sections 4.1 and 4.2.

As for the pinout of our version of the 555 timer using SLG46110V, the availability of those analog inputs, VDD, and GND pins in GreenPAK does not match the pinout of the standard 555 timer IC. So the input and output pins are assigned based on the internal component requirements (like the characteristics of comparators) of GreenPAK generally. Table 1 lists the pinout of this version and its functionality.

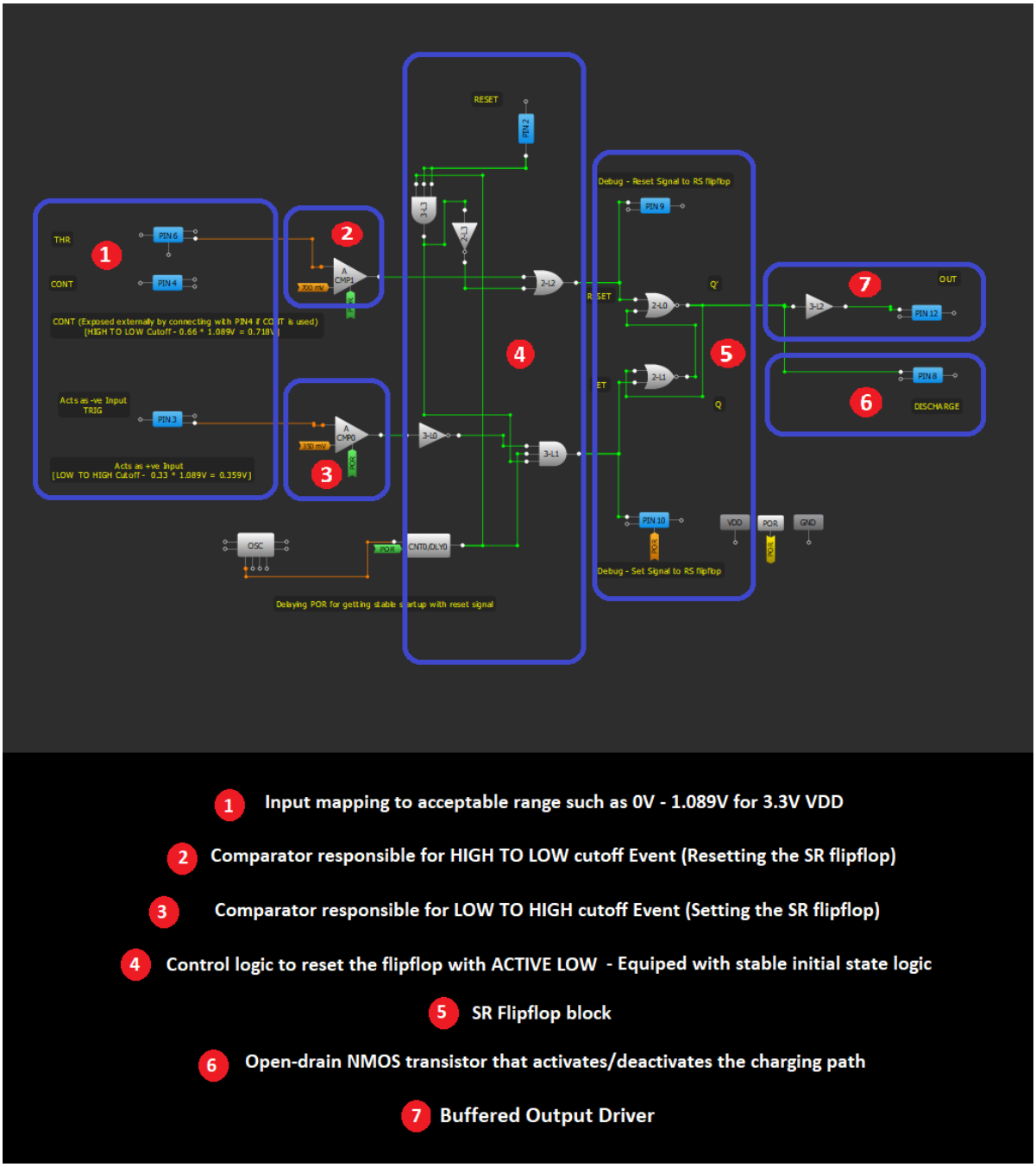

Figure 1: Internal Block Diagram of the 555 Timer with GreenPAK

4.1 Pinout of SLG46110V 555 Timer

Table 1 shows the functionality of each pin, and pinout of our SL46110V version of the 555 timer against the standard 555 timer IC. Figure 2 shows the pinout of SLG46110V IC.

Table 1: Pinout of a SLG46110V Version of 555 Timer

PIN NAME	PIN TYPE	DESCRIPTION (AS PER STANDARD 555 TIMER IC)	PINOUT 555 IC	PINOUT SLG46110V	REMARKS
GND	Power	This pin is the ground reference voltage (zero volts).	1	7	SLG46110V has PIN7 as ground.
TRIG	Input	When the voltage at this pin falls below 1⁄2 of CTRL pin voltage (1⁄3 VCC except when CTRL is driven by an external signal), the OUT pin goes high and a timing interval starts. As long as this pin continues to be kept at a low voltage, the OUT pin will remain high.	2	3	ACMP0 comparator, which is responsible for setting the SR flipflop, has PIN3 tied to its VIN+ input. Yes, TRIG is supposed to be fed into VIN- input of the comparator. However, ACMP0 is configured with a NOT gate which gives the exact functionality of that comparator (setting SR fliflop) in the standard 555 IC. More on this section 4.3.
OUT	Output	This is a push-pull (P.P.) output that is driven to either a LOW state (ground supply at GND pin) or a HIGH state (positive supply at VCC pin minus approximately 1.7 Volts). (Note: for CMOS timers, the HIGH state is driven to VCC.)	3	12	Since PIN3 is already used for the purpose of TRIG signal, we have to use PIN12. PIN2 (nearest number PIN) in SLG46110V is not possible to use because it is of input type.
RESET	Input	A timing interval may be reset by driving this pin to GND, but the timing does not begin again until this pin rises above approximately 0.7 Volts. This pin overrides TRIG (trigger), which overrides THR (threshold). If this pin is not used, it should be connected to VCC to prevent electrical noise causing a reset.	4	2	As PIN4 is shared as VIN- input of ACMP1 comparator (in case CTRL is used in application), PIN2 is used for RESET signal to SR flipflop.

PIN NAME	PIN TYPE	DESCRIPTION (AS PER STANDARD 555 TIMER IC)	PINOUT 555 IC	PINOUT SLG46110V	REMARKS
CTRL	Input	This pin provides "control" access to the internal voltage divider (by default it is 2⁄3 VCC). By applying a voltage to the Control Voltage input one can alter the timing characteristics of the device. In most applications this pin is not used, thus a 10nF decoupling capacitor (film or C0G) should be connected between this pin and ground pin to ensure electrical noise isn't added to the higher reference voltage. This control pin input can be used to build an astable multivibrator with a frequency-modulated output.	5	4	PIN4 is used as control voltage input since ACMP1's VIN- input has access to this pin only.
THR	Input	When the voltage at this pin is greater than the voltage at CTRL pin (2/3 VCC except when CTRL is driven by an external signal), then the timing (OUT high) interval ends.	6	6	Same as standard 555 IC.
DIS	Output	This is an open-collector output (CMOS timers are open-drain), which can be used to discharge a capacitor between intervals in phase with the output.	7	8	Since PIN7 is GND pin, the nearest number pin PIN8 is used as open drain output pin.
VDD	Power	The guaranteed voltage range of bipolar timers is typically 4.5 to 15 Volts (some timers are specified for up to 16 Volts or 18 Volts), though most will operate as low as 3 Volts. (Note: CMOS timers have a lower minimum voltage rating depending on the part number).	8	1	SLG46110's VDD pin is PIN1 and not pin 8. This device is operated at 3.3V and the reason will be discussed in section 4.2.

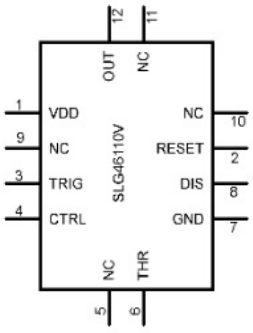

Figure 2: Pinout of SLG46110V 555 Timer

4.2 Signal Mapping with Comparator

The key idea is that the VIN+ input of both comparators is attenuated with 0.33 gain to map the signal in the acceptable region. That is, the input range of 0 - 3.3 V is mapped to 0 - 1.089 V (3.3 * 0.33). VIN- input is already in the acceptable range.

Below are the reasons for attenuating and mapping the input signal:

- As per issue 4 mentioned in the SLG46110V errata document, the device may be damaged if more than 2 V is applied externally to VIN- input of the comparators.

- According to the datasheet, section 5.3, the voltage range of the VIN+ input of comparators is 0 V - VDD, whereas it is 0V - 1.2 V for VIN- input of comparators. This specification is for VDD of 3.3 V.

- VIN+ input of the comparator provides a gain of *0.25, *0.33 and *0.5. VIN- input of comparator has no gain options.

- By mapping the VIN+ input range within 0 - 1.089 V and getting 1/3 and 2/3 of 1.089 V for VIN-, the input of the comparators preserves all the equations of the standard 555 IC timer.

4.3 How Does it Work?

In the case of resetting the SR flipflop (ACMP1 comparator), THR signal is fed into its VIN+ input and 0.66 * 1.089 V is derived from Vref, which is connected to VIN- input of ACMP1. In the scenario where this CONT signal is necessary for the application, PIN4 is connected to the VIN- input rather than deriving from Vref. Since Vref is derived as a fixed value, this setup has to be powered with a 3.3 V regulator with low dropout or else change the derived Vref value based on voltage regulator output. Figure 3 shows the settings for resetting the comparator path.

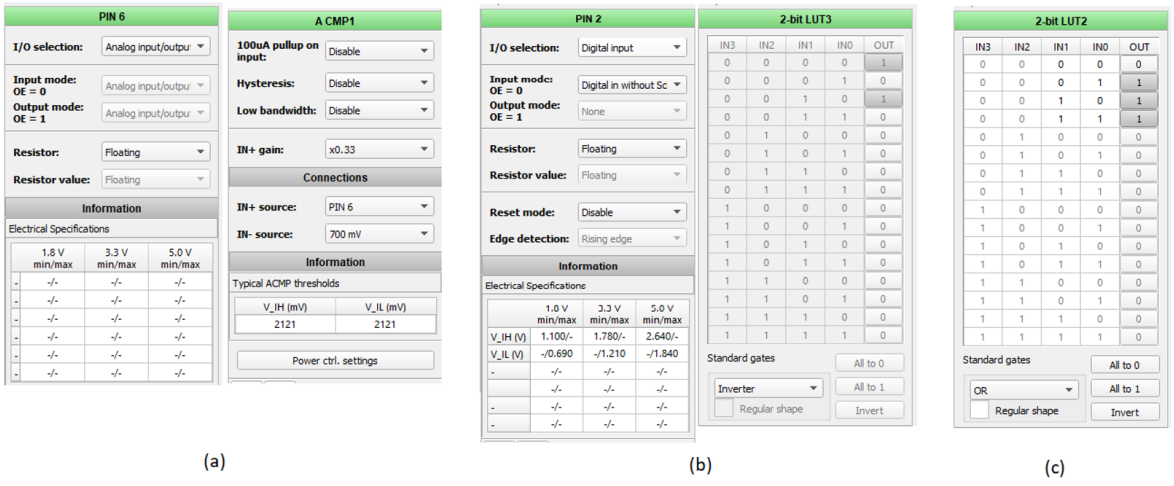

Figure 3: Comparator that Resets the Flip-Flop

(a) Settings of PIN6 and ACMP1. PIN6 is set as analog input and ACMP1 is configured for accepting PIN6 THR signal with 0.33 gain. ACMP1 resets the flip-flop when THR goes beyond configured 700mV (approximately equivalent to 2VDD/3). (b) PIN2 as input followed by inverter using 2-bit LUT3 (with the help of stable state logic) achieves the RESET functionality of an SR flip-flop. (c) Output of analog comparator and RESET functionality is ANDed to reset the SR flip-flop.

The SR flip-flop has VDD/3 connected to its VIN+ input and TRIG signal connected to its VIN- input in the standard 555 IC. This connection topology is achieved differently in SLG46110. Swapping VIN+ and VIN- inputs of the comparator with inverted output is equal to the normal connection topology of VIN+ and VIN- input without inverted output in the comparator. By using this property, TRIG signal is connected to the VIN+ input whereas the 0.33 * 1.089V from Vref is connected to the

VIN- input of the ACMP0 comparator and the output is inverted. Thereby we achieve the standard connection as in the 555 IC.

From the device datasheet, page 45: "During powerup, the ACMP output will remain low, and then become valid 110 µs (max) after POR signal goes high." We are using inverted output, so there is a possibility of setting the SR latch at startup, which is wrong. The system has to be started and stay in a known stable state to avoid this problem. Stable startup logic is implemented using reset functionality of the SR flipflop. The POR signal is delayed by around 80 mS which is ANDed with RESET signal, forcing the system to start with the proper RESET signal. Figure 4 illustrates the settings of the comparator path.

ACMP0 monitors LOW to HIGH cutoff whereas ACMP1 monitors HIGH to LOW cutoff. In the case of LOW to HIGH cutoff, ACMP0 sets the SR flipflop. Likewise, ACMP1 resets the SR flipflop during HIGH to LOW cutoff event.

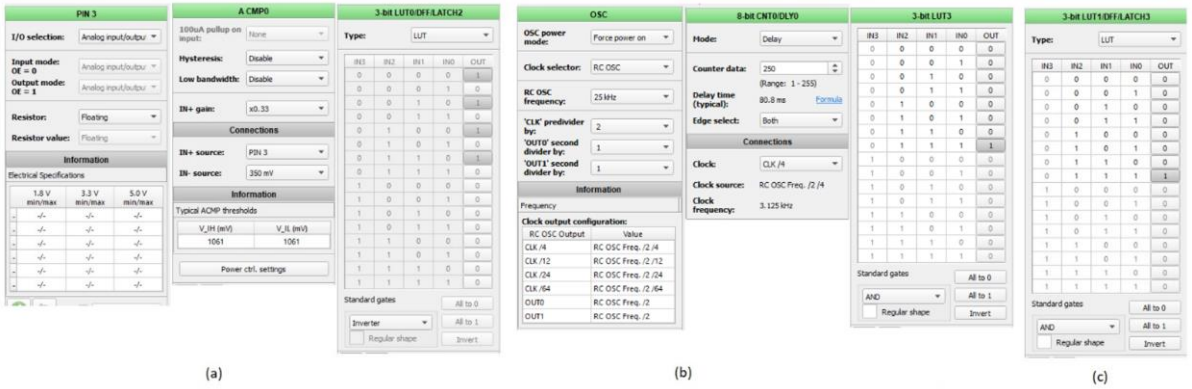

Figure 4: Comparator that Sets the Flip-Flop

(a) PIN3, ACMP0 and 3-bit LUT0 accomplishes the set operation signal generation. PIN3 is set as analog input. ACMP0 is configured with 0.33 gain of accepting TRIG signal from PIN3. When TRIG goes below 350 mV (which is approximately VDD/3), it gives the inverted signal due to a special input connection topology. 3-bit LUT0 is acting as an inverter to give the proper setting signal. (b) OSC, 8-bit CNT0, and 3-bit LUT3 are used to provide stable startup reset signal by delaying the POR signal by 80.8 mS. (c) Output of ACMP0, and delayed POR signal (with the help of stable state logic) are ANDed to get the final set signal for SR flipflop directly.

The SR flip-flop is implemented using two NOR gates. This SR flip-flop implementation includes the RESET control logic of SR flipflop which is active low. When the RESET pin is set LOW, then the ORed output is always HIGH, which resets the flip-flop whether ACMP1 is asserted or not. Figure 5 shows the configuration for the SR flip-flop.

When TRIG is applied LOW, the inverted ACMP0 output sets the SR flip-flop as the voltage in TRIG goes below 0.33 * 1.089 V available in PIN6. ACMP1 resets the SR flip-flop when the voltage in THR goes beyond 0.66 * 1.089 V. An external RC circuit controls the TRIG and THR voltage variation, and it also depends on the mode of operation.

PIN8 is configured as open-drain output mode and acts as charging/discharging path for an external capacitor. PIN12 is an output driver that has a buffered value of Q'.

Figure 5:

a) PIN8 is set as digital output for DIS signal with open drain configuration. This acts as discharging and charging path for capacitor. (b) PIN12 is configured as output with push-pull mode that follows the buffer using 3-bit LUT2.

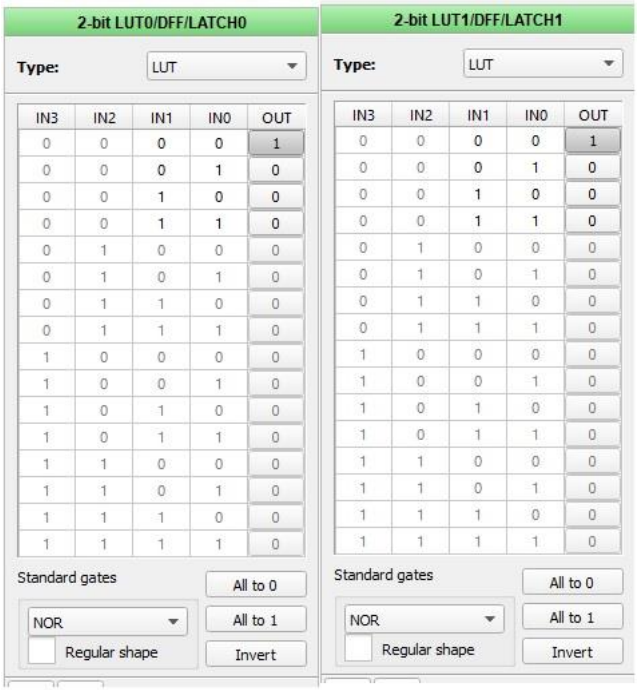

Figure 6: Configuration for SR Flip-Flop Using Two NOR Gates

5 555 Timer Operation Mode

5.1 Monostable Mode

In this mode, the external RC circuit is created to output a one-shot pulse of width t.

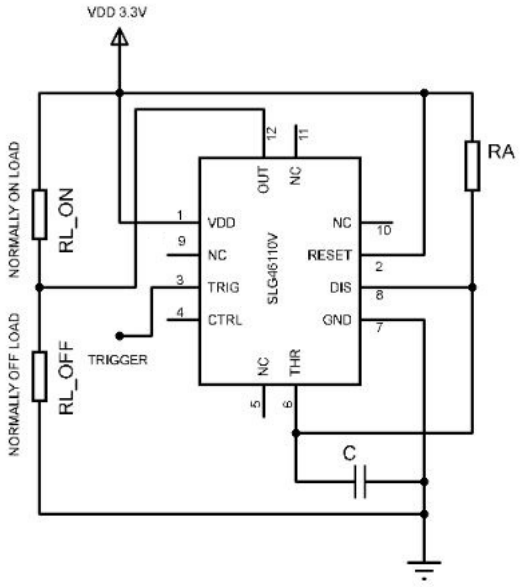

Figure 7: Monostable Mode with SLG46110V 555 Timer

When a negative going (0V) pulse is applied at TRIG input in this monostable configuration, ACMP0 sets the flip-flop. This action, in turn, switches OFF the NMOS transistor in PIN8, thereby removing the short circuit across the external capacitor C. This step allows the capacitor to charge up through the resistor RA until the voltage across the capacitor reaches the threshold voltage of 2*VDD/3. At this point, ACMP1 resets the flip-flop which in turn switches ON the NMOS transistor. The NMOS transistor makes the capacitor discharge through the ground. A negative pulse is applied at TRIG input again to get another one-shot pulse.

The width of the one-shot pulse is given as follows

$$t = 1.1 * R_A * C \quad (Eq. 1)$$

Once the system is powered ON, the delayed POR forces the SR flip-flop to stay in reset state which is shown in Figure 8. Figure 9 illustrates the behavior of the monostable mode in our SLG46110V version of the 555 timer when RA is 47 kOhms and C is 10 uF.

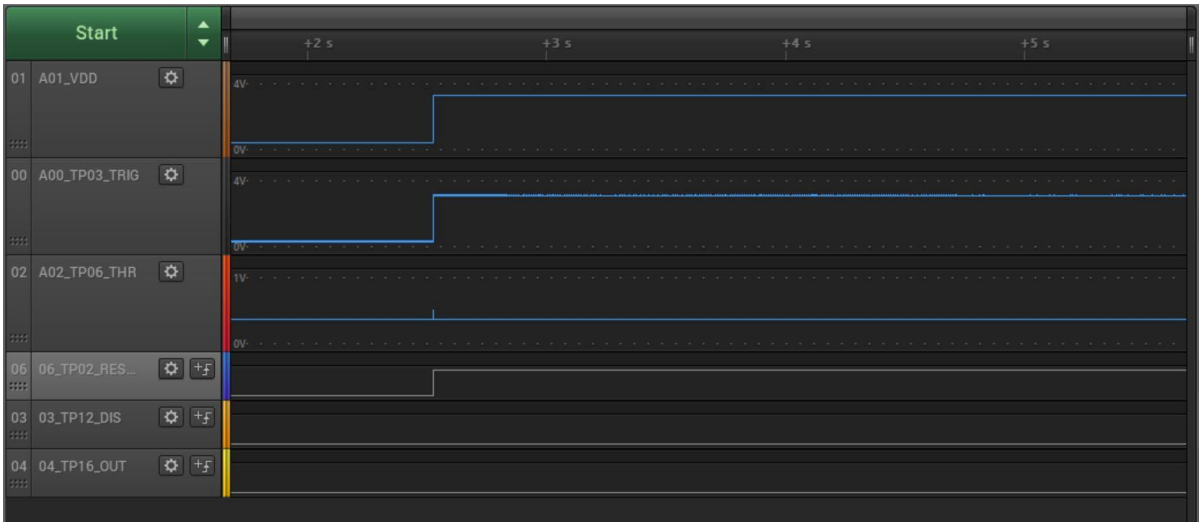

Figure 8: Stable Start After Power ON

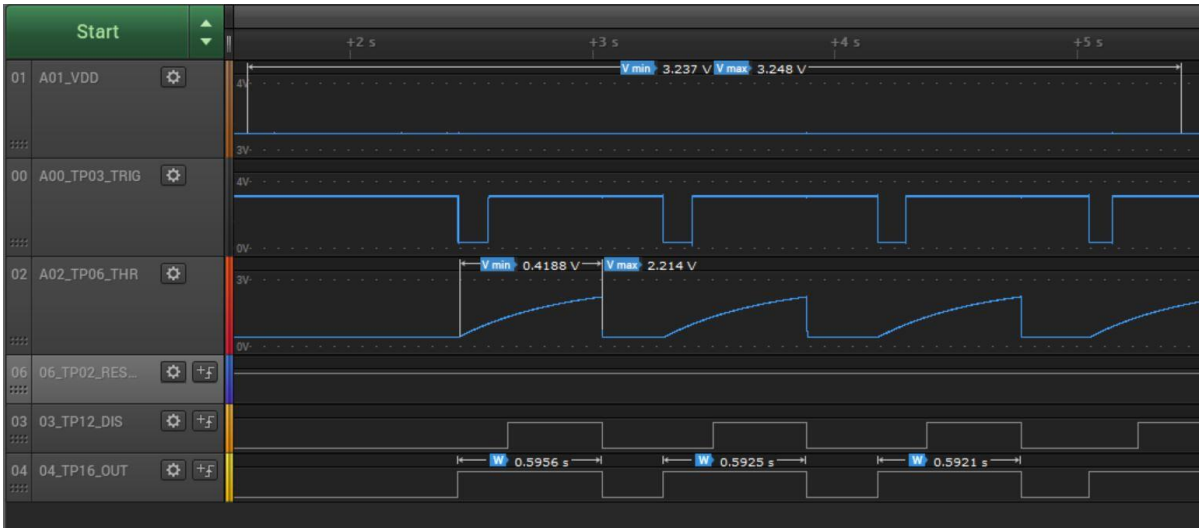

Figure 9: Monostable Mode

Let us take C as 10 uF and the standard resistors (with 5% tolerance) as follows. Table 2 represents the measured value of pulse width in seconds from our SLG46110V version against the calculated values. It is observed that when the resistor value gets higher, the accuracy drops.

Table 2: Experimental Data - Monostable Mode

RA in Ohms	C in uF	Width in mS	SLG46110V Version in mS
12000	10	132	136
22000	10	242	257
33000	10	363	398
47000	10	517	593
56000	10	616	755
68000	10	748	934
82000	10	902	1174

5.2 Astable Mode

In this mode, the timer generates a clock signal. In a nutshell, it acts as an oscillator.

Since the TRIG pin and THR pin are connected to capacitor C, the voltage is the same in C, THR, and TRIG. At the start the voltage across these points is LOW. Whenever the voltage at TRIG is LOW, the output becomes high and the NMOS transistor is opened. Since the discharge path is open, current can flow through RA and RB, which in turn charges the capacitor C. Once C is charged to 2*VDD/3, ACMP1 resets the flip-flop, which closes the discharge path that leads to the discharge of capacitor C through RB. Once the voltage across C drops to VDD/3, the discharge path opens and capacitor C starts charging again. This cycle continues and generates the clock signal.

The circuit diagram of astable mode is shown in Figure 10.

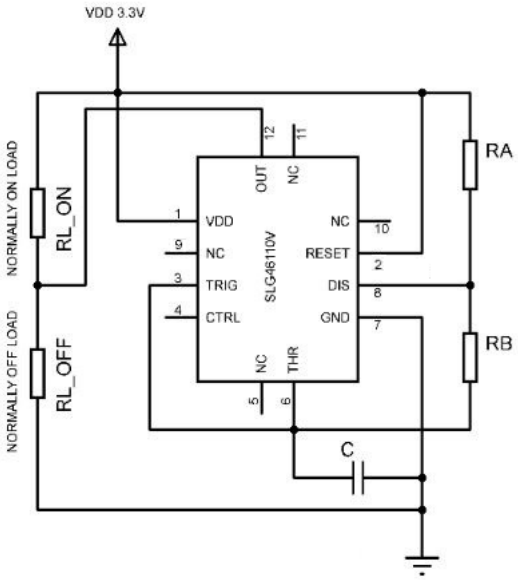

Figure 10: Astable Mode with SLG46110V 555 Timer

The charging time when output is HIGH is given by:

$$t_{ON} = 0.693 * (R_A + R_B) * C \quad (Eq.2)$$

The discharging time when output is LOW is given by:

$$t_{OFF} = 0.693 * R_B * C \quad (Eq. 3)$$

The period of the clock signal generated in astable mode is given below using equation 2 and 3:

$$t_P = t_{ON} + t_{OFF}$$

$$t_P = 0.693 * (R_A + 2R_B) * C$$

The frequency of the generated signal is $F = \frac{1}{t_P}$

$$F = \frac{1.44}{(R_A + 2R_B) * C} \quad (Eq. 4)$$

The duty cycle is given by the formula mentioned in equation 5

$$D = \frac{R_B}{R_A + 2R_B} \quad (Eq. 5)$$

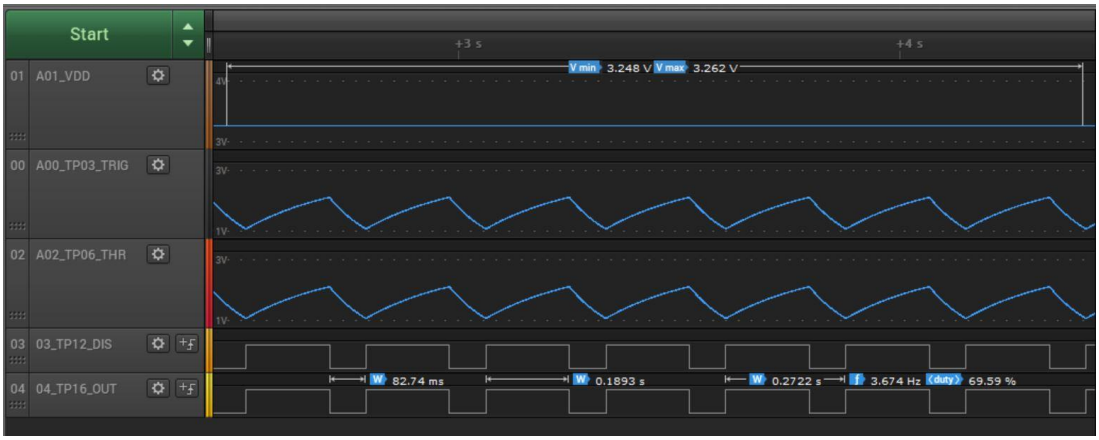

Figure 11:

Let us take C as 10 uF and the standard resistor (with 5% tolerance) as shown in Table 3. It is observed that increases in resistor value decrease the accuracy of the pulse width (ON or OFF), which leads to a decrease in the accuracy of the frequency. The yellow shaded cells represent that for the chosen RC circuits, the capacitor does not charge until 2*VDD/3 and has only an ON period.

Table 3: Experimental Data - Astable Mode

Calculated Values						SLG46110V Version				
RA in Ohms	RB in Ohms	C in uF	Freq in Hz	Duty Cycle in %	Ton in mS	Tlow in mS	Freq in Hz	Duty Cycle in %	Ton in mS	Tlow in mS
12000	12000	10	3.968254	66.67	166.3	83.1	3.674	69.6	189	82.75
22000	22000	10	2.164502	66.67	304.9	152.4	2.959	79.8	270	68.41
33000	33000	10	1.443001	66.67	457.3	228.7	1.024	78.6	767	208.8
47000	47000	10	1.013171	66.67	651.4	325.7	0.497	86.2	1746	280
56000	56000	10	0.85034	66.67	776.2	388.1	-	-	-	-
68000	68000	10	0.70028	66.67	9.425	4.712	-	-	-	-
82000	82000	10	0.58072	66.67	11.365	5.683	-	-	-	-

5.3 Bistable Mode

In this mode the timer acts like a flip-flop or memory cell. As this is a bistable configuration, switching the output waveform from one state to another is achieved by controlling the TRIG and RESET signals with an active LOW pulse. In this case, two buttons are connected and pulled high with pull-up resistors R1_PR and R2_PR respectively. When the button that is connected to TRIG is pressed, it sets the SR flip-flop and the output is driven HIGH. When the RESET signal is applied LOW by pressing its corresponding button, then the output is driven LOW. Since the THR pin is grounded, the SR flip-flop does not get reset, which makes the state stay indefinitely.

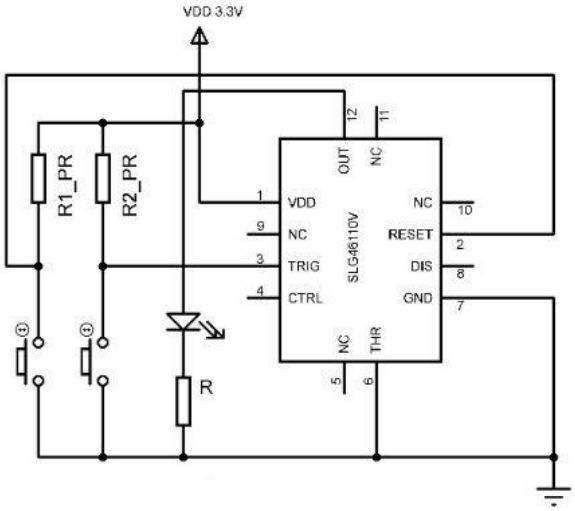

Figure 12: Bistable Mode with SLG46110V 555 Timer

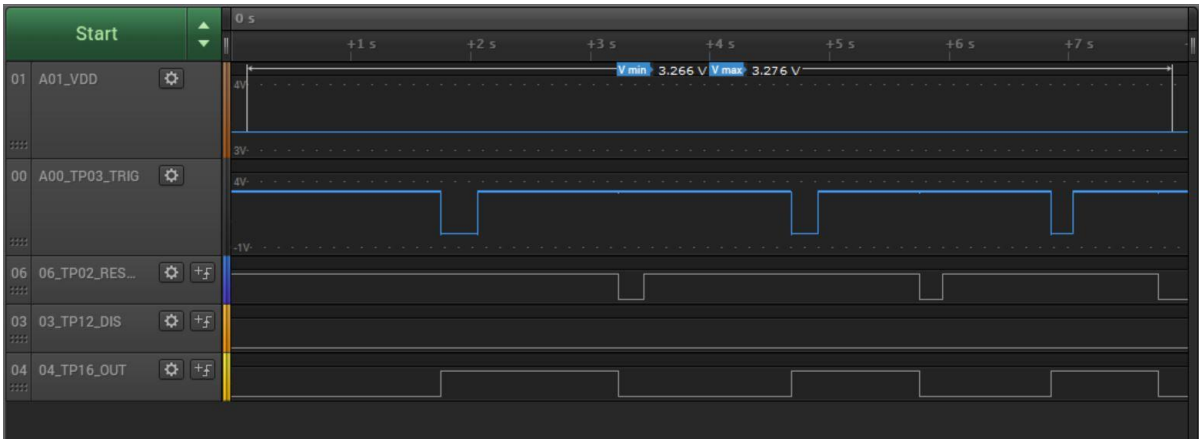

Figure 13

6 Conclusions

The GreenPAK SLG46110V has the necessary internal resources to implement the behavior of a 555 timer IC. In this application note, we implemented monostable, astable, and bistable operation modes using the SLG46110V. Testing results showed that the standard 555 timer can be replaced with our SLG46110V version. SLG46110V is also small in size, which makes it a good alternative for 555 timer operations in wearable electronics.

Revision History

Revision	Date	Description
1.0	13-Sep-2018	Initial Version

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
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